
CONTROL DATA®
1748-2 MULTIPLEXER CONTROLLER

REFERENCE MANUAL

FOREWORD

SCOPE

This manual contains introductory information, details concerning the operation, and programming considerations pertinent to the 1748-2 Multiplexer Controller (MC). The information contained in this manual is primarily descriptive and, therefore, is not of specific use for maintenance purposes. For maintenance information and a detailed theory of operation, refer to the Customer Engineering Manual (pub. no. 416 017 00).

REFERENCE DOCUMENTS

Other publications or documents which furnish information relative to the MC but beyond the scope of this manual are as follows:

304-1 Communications Multiplexer, Reference Manual,
pub. no. 137 964 00.

303-1 Communications Expansion Unit, Reference Manual,
pub. no. 137 974 00.

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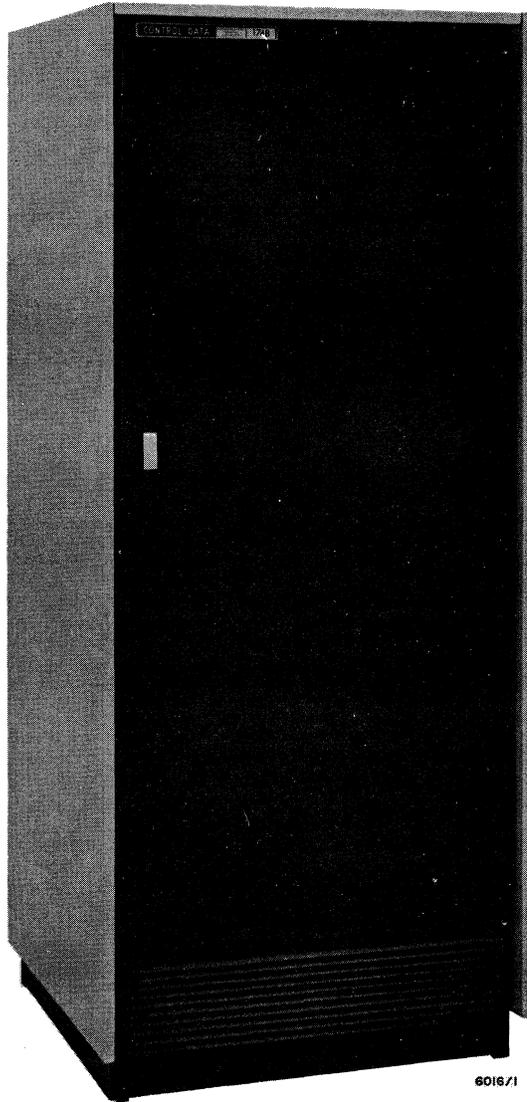
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1748-2 Multiplexer Controller

SECTION I INTRODUCTION

GENERAL

This section provides a basic description, functional description, a discussion on systems application, and a physical description of the 1748-2 Multiplexer Controller (MC).

BASIC DESCRIPTION

The MC (see frontispiece) is a high-speed multiplexing device which enables real-time communications between a 1700 Computer System and a communications expansion network. As many as 512 low-speed terminal units (TUs) with their associated communications lines, may be serviced by the MC in a maximum capacity communications system. When the system consists of a mixture of low- and high-speed lines, the maximum number of lines serviceable by the MC is reduced as a function of the total system input/output (I/O) transfer rate. MC operation requires that the 1700 Computer have the 1705 Interrupt Data Channel (IDC).

FUNCTIONAL DESCRIPTION

The MC services each TU and associated communications line on a character-by-character basis. Such service may consist of a bidirectional character transfer (half-duplex) between the TU and the computer through an expansion network and the MC. Because of the MC's high-speed capability it can receive one character from a TU, service the remaining TUs in the network, and return to the first TU before the next character is ready for transfer.

The high-speed operation and character-by-character service capability of the MC are due to the unit's direct storage access capability. Direct storage access allows the MC to store and remove characters from memory without direct program concern. In addition, control words placed in memory for each TU and communications line provide individual line control. The control words are referenced by the MC directly when the corresponding TU is selected for service. The instructions contained in the control words determine the MC modes of operation during service of the TU. Address information, also contained in the control words, determines the storage locations for data handling purposes with the TU.

A second MC and computer, through the use of the 10128 Dual Mode standard option, may be added to an existing system to form a dual system, thus providing a redundant capability. When the primary MC or computer malfunctions, the secondary MC and computer continue servicing of the TUs. Signals are exchanged between the two MCs so that each computer, through its own MC, is aware of the status of both sections of the dual system.

SYSTEM APPLICATION

SYSTEM FUNCTIONAL DESCRIPTION

The MC-oriented communications system uses a time-divisional expansion network of multiplexing devices to handle a large number of communications lines. The multiplexing devices used in forming an expansion network are the 303-1 Communications Expansion Units (CEUs) and the 304-1 Communications Multiplexers (CMs). The number of multiplexing devices in combination in an expansion network determines the number of communications lines that may be handled by the system. To facilitate the operational description, three distinct multiplexing device combinations, forming individual types of MC-oriented communications systems, are discussed in this section. The system types are as follows: a two-level expansion network, a three-level expansion network, and a dual-mode network. In actuality, a practical MC-oriented system application may use elements of all three system types (i.e., a two-level/three-level/dual-mode network combination).

The following paragraphs provide a general description of system multiplexing. In addition, the paragraphs describe each MC-oriented system in detail to provide an understanding of the relationships and the system functions.

Expansion Networks

Expansion networks are formed in levels of multiplexing devices. The number of multiplexing devices in each level is limited by the multiplexing capacity of the preceding level. The number of levels is determined by the number of communications lines which the system must service. Actual multiplexing operations, and the selection of TUs and associated communications lines for service by the MC, are accomplished by direct sequential addressing (expansion addressing) in each level.

Expansion Addressing

Each multiplexing device in the network (the MC, the CEUs, and the CMs) contains logic circuits necessary for expansion addressing. The addressing circuits in each unit consist of a three-stage counter, a count compare circuit, and an address compare circuit. Refer to figure 1-1 as an aid to understanding the interrelationships of the circuits in the network.

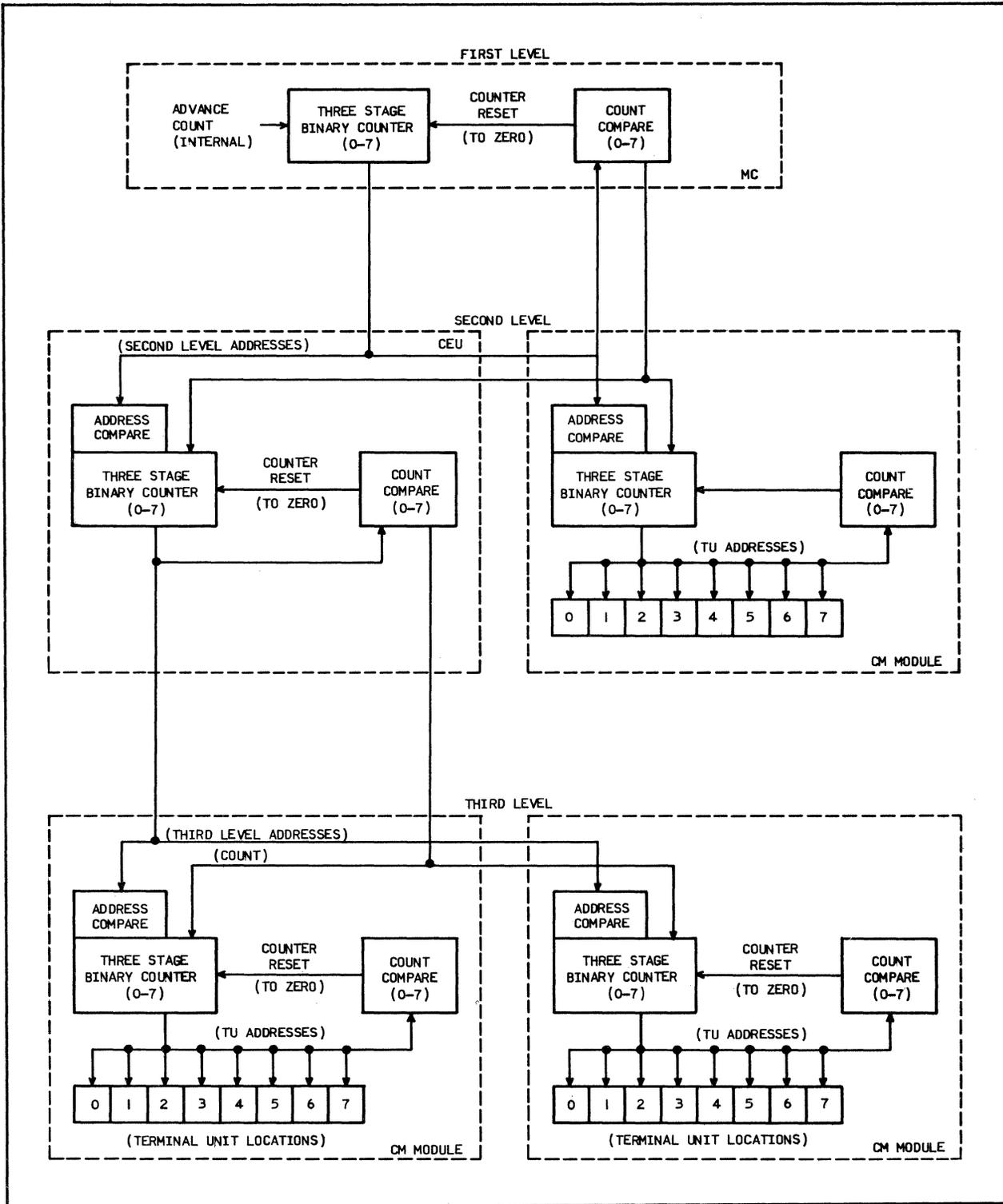


Figure 1-1. Expansion Addressing Circuits

Three-Stage Counter - Every expansion network unit contains a three-stage counter which is used to sequentially develop three-bit addresses that select the units in the next expansion level. Each address is a binary representation of an octal number. The counter may develop eight addresses (octal 0 through 7) before resetting to reinitiate the addressing sequence. Thus, one multiplexing device may select as many as eight devices in the next level of expansion.

In figure 1-1, the first-level, three-stage counter in the MC is advanced by an internally developed count pulse. The three-bit address output of the counter selects one of the second-level multiplexing devices. The selected second-level device has a three-stage counter, which, in turn, selects either a third-level device or a TU with its associated communications line.

The second-level CEU or CM module (each CM contains two modules) counters can advance only to the next sequential address upon receipt of a count pulse issued by the MC as its counter resets to the first address of a new sequence. This means that all second-level devices are selected once before their counters are allowed to advance.

When a three-level expansion network is in use, the third-level CM module counters function in the same manner as the second-level devices with one exception. Third-level counters are advanced by the count pulse issued by the MC and gated through the second level by a CEU when its counter (the CEU's) resets to repeat the address sequence. The address output of each third-level CM module counter selects a TU and associated communications line for service.

Count Compare Circuit - Each multiplexing device in an expansion network has a count compare circuit controlled by three toggle switches. The toggle switches on the MC are called the SCAN TERMINATION ADDRESS switches. On the CEU and the CM modules, the toggle switches are called the LAST COUNT switches. The count compare circuit senses each address developed by the three-stage counter in the unit and compares it to the address represented by the settings of the three toggle switches. When the two addresses are identical, the count compare logic enables gate signals to reset the three-stage counter to repeat the address sequence and to gate a Count pulse to the next expansion level.

Address Compare Circuit - All multiplexing devices have an address compare circuit which is controlled by EQUIPMENT NUMBER or ADDRESS toggle switches. On the MC, there are four EQUIPMENT NUMBER toggle switches which are set to the hexadecimal code for the equipment number assigned to differentiate the unit from the other units connected to the I/O channel. On the CEUs

and the CM modules, three ADDRESS toggle switches are set to differentiate each unit from the other units in the expansion level. Units in one expansion level are selected by the addresses developed in the previous level. Each address is sensed simultaneously by all units in the level. The address compare circuit in each unit rejects all addresses except the one which is identical to the settings of the ADDRESS toggle switches. Each unit in the same level must have its ADDRESS toggle switches set to a unique octal address from 0 through 7.

Two-Level Expansion Networks

The expansion network shown in figure 1-2 indicates the maximum communications line capacity of a two-level expansion network (64 communications lines).

In such a system, the MC sequentially develops eight addresses which are sensed by the eight CM modules. The settings of the ADDRESS switches in each CM module determine which module responds. The CM module ADDRESS switches need not be set to correspond sequentially to the order in which the modules are interconnected to the MC, but the switches of each module must be set to a unique address.

Each CM module in the second level of a two-level network can address and control as many as eight TUs. Since the TUs are physically mounted in the CM, the addresses developed by the CM module progress sequentially, selecting TUs by location, from left to right within the CM module. The TU located farthest to the left in the CM module is selected by address 0. When less than a full complement of TUs is installed in a CM module, the module's LAST COUNT switches must be set to indicate the address of the TU physically located farthest to the right. This address is the highest address value to be developed by the three-stage counter in the CM module. With a full complement of TUs the LAST COUNT switches must be set to octal 7.

Network Operation - When multiplexing (scanning) first begins at the start of system operation, a Master Cleared condition is in effect and each CM module in the second level has selected the TU corresponding to address 0. The MC also is issuing address 0 and has, thereby, selected the second-level CM module set to respond to that address. That CM module's selected TU is connected through the module to the MC for service. Service may consist of a character transfer in both directions (half-duplex) or no transfer at all if conditions pertaining to that TU's operation, as sensed by the MC, so dictate. In any case, the MC continues to address and select each CM module sequentially, and, at each selected CM module, the TU responding to address 0 receives service as previously described. After selecting the last CM module in the level, the MC resets its three-stage counter to address 0 to repeat the sequence (address scan). The MC then issues a Count pulse which advances the TU addresses being developed by the counters in each CM module to

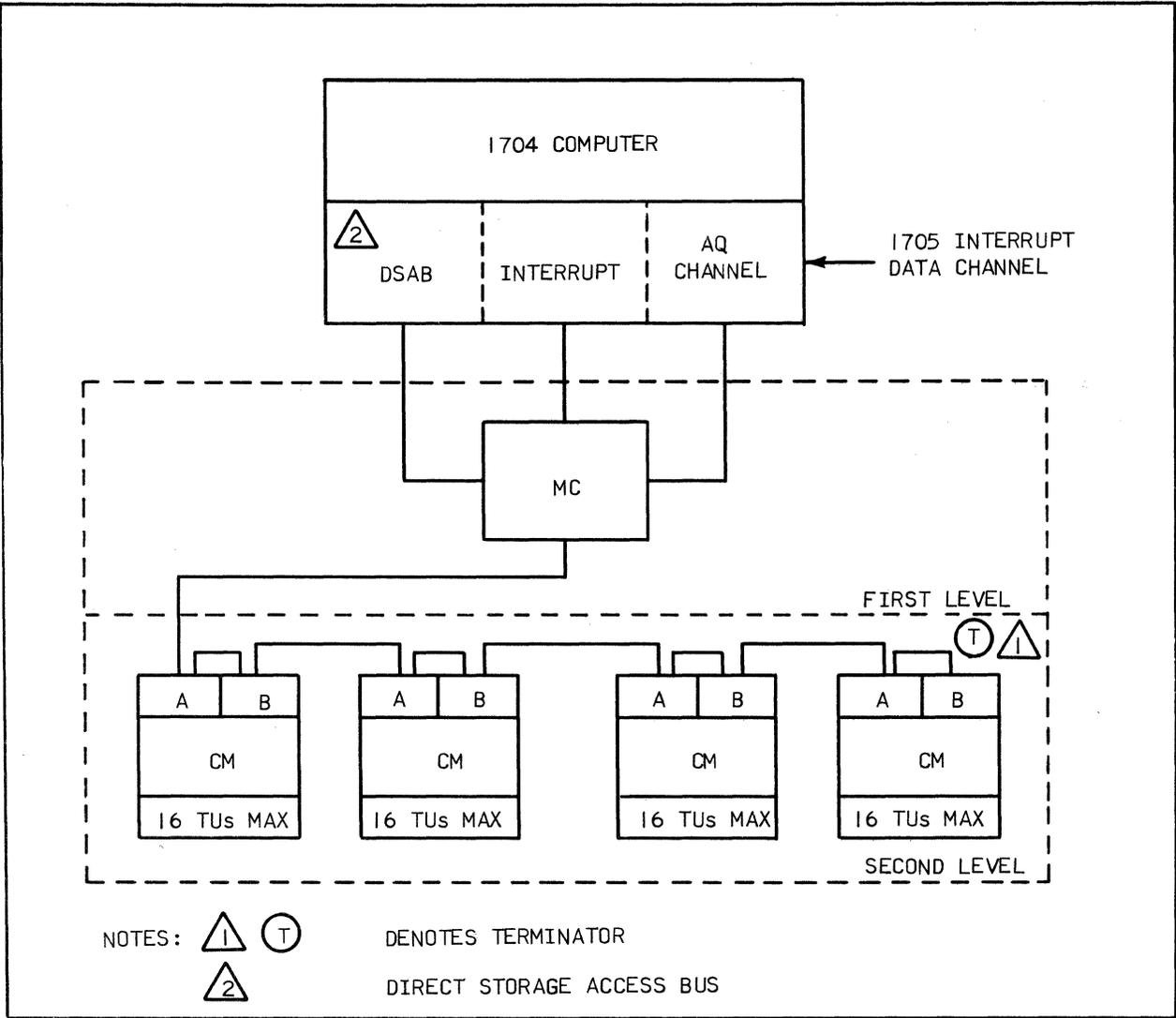


Figure 1-2. Two-Level Expansion Network

address 1. As the MC repeats its address scan, each CM module is again selected, and service is provided to the TUs responding to address 1. The MC continues to repeat its address scan, and as each CM module reaches the TU address represented by the setting of its LAST COUNT switches, the CM module counter resets to address 0 and begins anew its address scan.

In a practical two-level expansion network, some TUs and associated communications lines may be serviced more frequently than others. For example, should one of the CM modules contain four TUs instead of eight, the LAST COUNT switches in the module are set to represent address 3, causing that module to repeat its address scan when the other modules are midway in their respective scans. Therefore, each TU in that CM module receives service twice, whereas the TUs in the other CM modules having a full complement receive service once.

Three-Level Expansion Networks

The expansion network shown in figure 1-3 is a true three-level expansion network; that is, all TUs are located in the third level of expansion. The network illustrated does not indicate the maximum capacity of a three-level network in that 192 TUs and associated communications lines may be serviced. However, with the addition of five CEUs in the second level and twenty CMs in the third level, the illustrated network could then service the maximum of 512 low-speed TUs with their respective communications lines.

Network Operation - In a three-level network, the MC sequentially addresses and selects CEUs in the same manner as previously described for the CMs in the second level of a two-level network. Each CEU in the second level as illustrated in figure 1-3 with its eight associated CM modules may be considered a complete two-level expansion network with the CEU duplicating the multiplexing function of the MC. In a maximum capacity network, therefore, the MC is multiplexing or scanning eight separate two-level expansion networks.

A communications system such as that just described, is perfectly symmetrical and all TUs are serviced at the same frequency rate. The high-speed capability of the equipment involved allows the MC to service a TU in one network, transferring one input and/or output character, service the remaining TUs in all eight networks, and return to the first TU before the next character is ready for transfer.

In figure 1-3, the SCAN TERMINATION ADDRESS switches would be set to represent address 2, since only three CEUs are contained in the second level. The LAST COUNT switches on each CEU would be set to represent address 7 because of the eight CM modules in the third level connected to each unit.

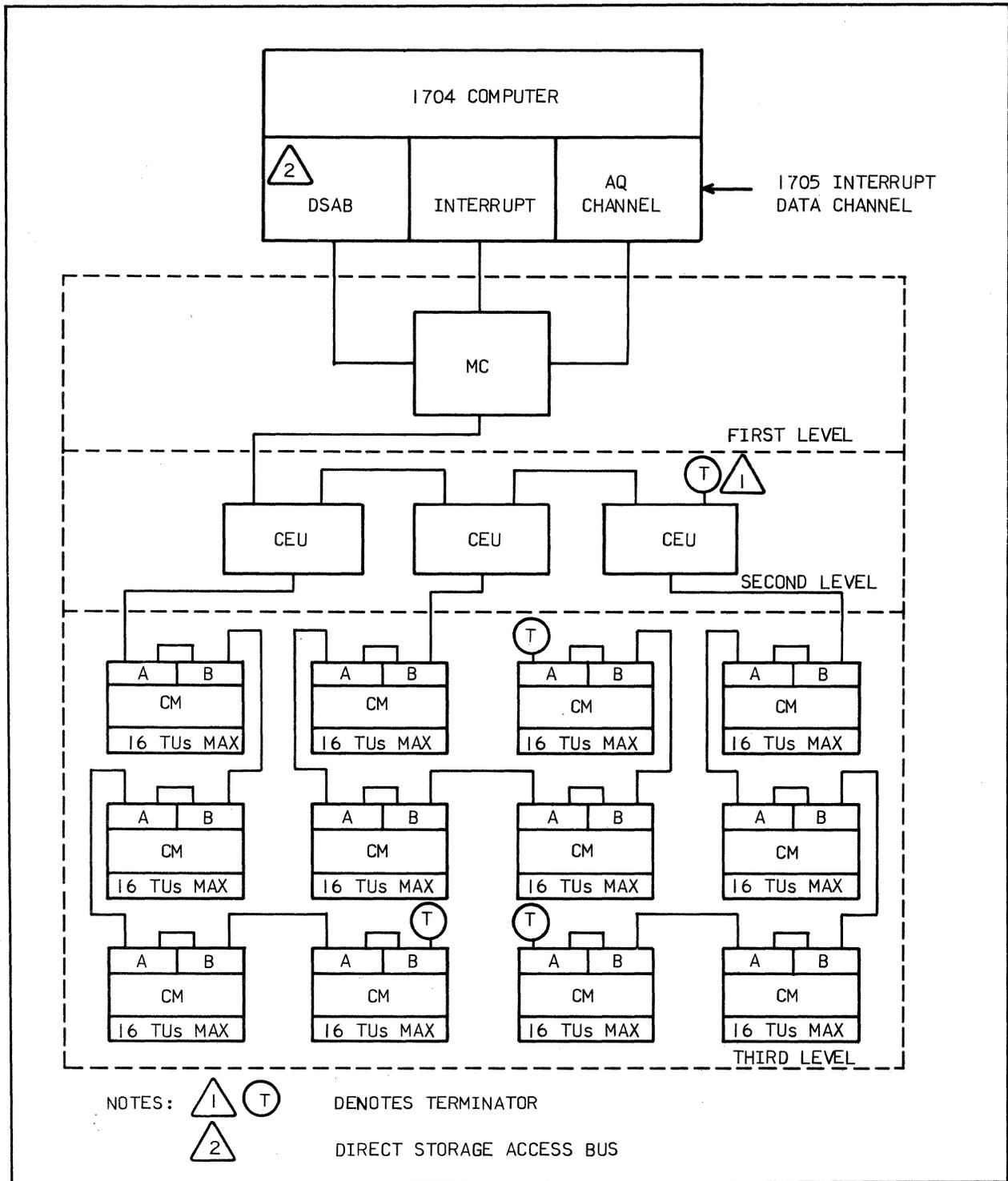


Figure 1-3. Three-Level Expansion Network

Dual-Mode Expansion Network

The dual-mode expansion network (figure 1-4) utilizes the 10128 Dual Mode Option (DMO) so that two 1700 Computer Systems, each having an MC, can provide a redundant service capability for a common expansion network. Data loss, in the event of a system failure, is prevented by the ability of the remaining system to service the network through the DMO. The DMO assumes the task of expansion addressing from the MCs to ensure that all input data is received simultaneously by both systems. If one of the 1700/MC systems fail during dual-mode operation, the DMO automatically reverts to the single-scan mode of operation with the remaining 1700/MC system.

In figure 1-4, the expansion network illustrated is a combination two- and three-level network. Because of the combination and the necessary method of addressing which results, the second-level TUs are addressed more frequently than the third-level TUs.

PHYSICAL DESCRIPTION

GENERAL

The MC is contained in an upright cabinet. The logic chassis is on a standard, vertical, 19-inch rack and consists of eight pans of 3000-type logic cards in horizontal rows. The logic chassis contains the logic cards for the two major sections of the MC, the control logic section, and the expansion module (EM) logic section. The EM logic section performs the MC's addressing function and serves as the communication interface between the control logic section and the TUs.

POWER SUPPLY

The power supply is mounted as a separate assembly on the 19-inch vertical rack. The assembly may be easily disconnected and removed to facilitate maintenance. Test points, screwdriver voltage adjustments, a circuit breaker, and the AC ON/OFF switch are located on the power supply assembly front panel. Normally, the standard 120-vac, single-phase, 60-Hertz power supply is furnished with the MC. However, a 220-vac, single-phase, 50-Hertz power supply is available and can be obtained by special order.

VENTILATION SYSTEM

The ventilation system is at the bottom of the cabinet and consists of a blower, ducts, blower fuses, and a filter. The air filter may be removed by opening the front door and lifting the filter up and out.

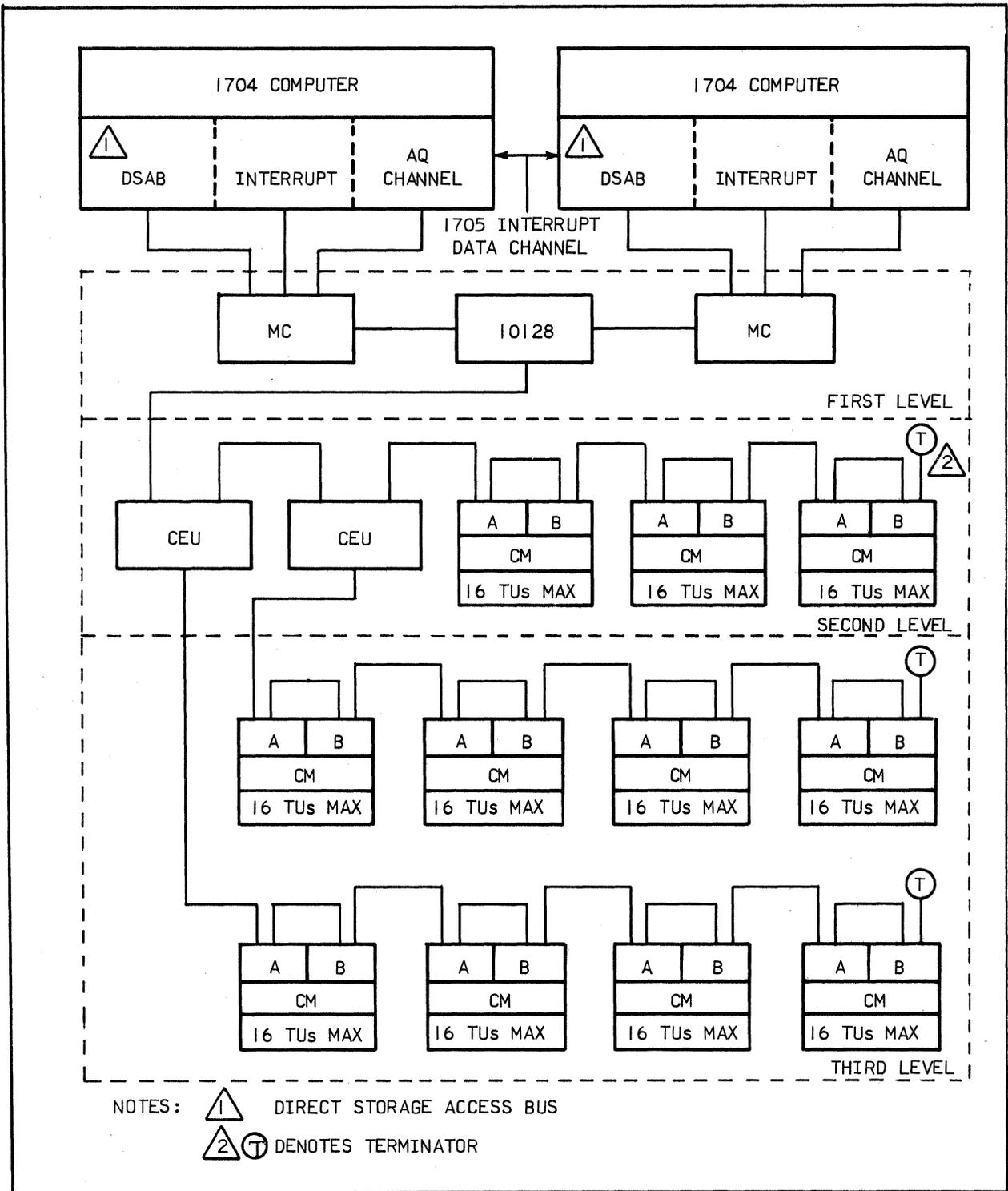


Figure 1-4. Dual-Mode Expansion Network

LEADING PARTICULARS

Table 1-1 lists the physical characteristics and environmental requirements of the MC.

TABLE 1-1. LEADING PARTICULARS

Dimensions:	
Height	68-3/4 in.
Width	28 in.
Depth	26 in.
Weight	500 lb
Operating Environment:	
Temperature	+40° to 120°F
Relative Humidity	20 to 90%
Heat Dissipation	2200 Btu/hr
Storage and Shipping Environment:	
Temperature	-40° to 160°F
Relative Humidity	0 to 100%
Power Requirements:	
AC Power	120 ±15 vac, 60.0 ±0.3 Hz, single phase
Nominal Current	5.5 amperes
Terminator Power	Central system; 40 vdc supply



**SECTION II
OPERATION**

GENERAL

The MC operates under computer program control and does not normally require operator attention. With the exception of the main power switch and the power supply AC ON/OFF switch, all switch settings depend on fixed characteristics of the system. The switch settings are changed only when the associated system characteristics change. The following paragraphs describe the purpose of the switches and the system considerations required for their use.

MC SWITCH PANEL

GENERAL

Figure 2-1 illustrates the MC switch panel. The switch panel is mounted above the logic chassis on the 19-inch vertical rack and is easily accessible after opening the front door of the MC. The switch panel contains 27 toggle switches, 4 indicator lights, and one rotary switch.

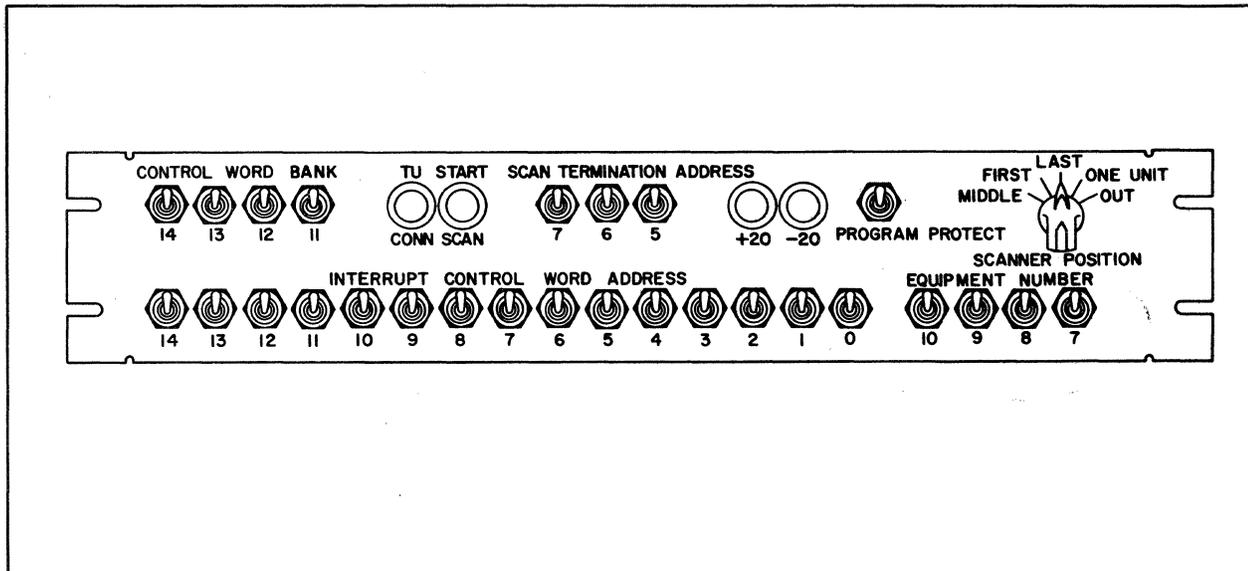


Figure 2-1. MC Switch Panel

SCANNER POSITION

The Direct Storage Access Bus (DSAB), part of the Interrupt Data Channel (IDC), can allow up to eight external equipments to have direct reference to computer storage. In a complete system, the MC is one of these devices. Since only one device may have access to storage at a time, a scanner circuit is necessary to provide systematic use of computer storage. Each user device must have, as a part of its logic, a section of the scanner circuit (distributed scanner). An address cable interconnects the scanner sections of the devices in series and connects the last device back to the first device to form a chain. A device having a need for access to storage may stop the scanner at its position in the chain and perform its storage reference. The device then allows the scanner operation to continue so that other devices can stop the scanner as they develop needs for access to storage. The SCANNER POSITION switch in the MC provides the connections and polarity reversals necessary to accommodate the MC to its position in the device chain. The switch has five positions: MIDDLE, FIRST, LAST, ONE UNIT, and OUT. Positions MIDDLE, FIRST, and LAST are self-explanatory. The ONE UNIT position is used when the MC is the only device in the system that requires direct reference to storage. The OUT position allows the scanner operation to bypass the MC, effectively removing the unit from the device chain.

EQUIPMENT NUMBER

The EQUIPMENT NUMBER switches consist of four toggle switches which are set to represent the binary form of the hexadecimal equipment code number assigned to the MC. The equipment code number identifies the MC in the system. The MC responds only to its assigned number. Any switch in the up position represents a logical "1". Table 2-1 may be used as a cross-reference between decimal, hexadecimal, and binary numbers.

TABLE 2-1. DECIMAL-HEXADECIMAL-BINARY CROSS-REFERENCE

DECIMAL	HEXA- DECIMAL	BINARY	DECIMAL	HEXA- DECIMAL	BINARY
0	0	0000	8	8	1000
1	1	0001	9	9	1001
2	2	0010	10	A	1010
3	3	0011	11	B	1011
4	4	0100	12	C	1100
5	5	0101	13	D	1101
6	6	0110	14	E	1110
7	7	0111	15	F	1111

SCAN TERMINATION ADDRESS

The SCAN TERMINATION ADDRESS switches consist of three toggle switches which are set to represent, in binary form, the highest expansion unit address required in the second level of expansion. The MC compares the second-level addresses that it generates with the settings of the SCAN TERMINATION ADDRESS switches. When the two addresses compare, the address scan is reset to address zero and the MC issues a Count pulse to the expansion network. The SCAN TERMINATION ADDRESS switches eliminate the time-consuming task of generating unused second-level addresses.

CONTROL WORD BANK

The four CONTROL WORD BANK toggle switches are set to represent, in binary form, the hexadecimal number identifying the initial address of a block of computer storage assigned to the MC. The block of storage is used by the MC for storage of the control words assigned to each TU in the system. The MC uses the switch settings and the nine address bits developed by the levels of the expansion network to address the appropriate storage location within the control word storage block.

INTERRUPT CONTROL WORD ADDRESS

The 15 INTERRUPT CONTROL WORD ADDRESS toggle switches are set to represent, in binary form, the 15-bit address of one 16-bit location in computer storage. The computer stores the current Interrupt Control Word address in this location. This address is the indirect Interrupt Word address. Each time the MC needs to write an Interrupt Word into storage, it must read the storage location addressed by the switches to obtain the address specified by the computer for the Interrupt Word. The MC then writes the Interrupt Word at the specified address. The MC also writes the specified address +1 back into the location addressed by the switches.

PROGRAM PROTECT

The use of the PROGRAM PROTECT switch depends on the system in which the computer is used and the intentions of the system operator. In the MC, the switch determines which AQ commands the unit will accept or reject. When the switch is in the down or NOT Program Protect position, the MC replies to both protected and unprotected I/O commands. When the switch is in the up or Program Protect position the MC rejects all unprotected I/O commands except a request for status and replies to all protected I/O commands assuming the equipment number is correct and W=0 signal is present. When a Program Protect fault is detected, the MC provides a status bit indicating the detection of the fault.

TU CONNECT INDICATOR

The TU CONN indicator is located on the upper left-hand section of the MC switch panel. The indicator lights when the MC is transmitting a Connect signal to a TU.

START SCAN INDICATOR

The START SCAN indicator is located on the upper left-hand section of the MC switch panel next to the TU CONN indicator. The indicator lights when the Start Scan flip-flop in the MC is set by a Start Scan function code issued by the 1700 Computer.

LOGIC POWER INDICATORS

These indicators are located on the upper right-hand section of the switch panel. One indicator is labeled +20 and lights when the +20 vdc logic power is on. The other indicator is labeled -20 and lights when the -20 vdc logic power is on.

PRIMARY POWER SWITCH

The Primary Power switch is a toggle switch mounted in a utility box located midway down the left-hand side of the MC cabinet, and is easily accessible after opening the front door. This switch controls all AC power to the MC.

LOGIC POWER SWITCH

The logic power switch (AC ON/OFF) is located on the front panel of the power supply assembly and controls the ± 20 vdc logic power.

SECTION III PROGRAMMING CONSIDERATIONS

GENERAL

This section discusses the factors which must be considered in programming for MC operation in a real-time communications system. Additional information of concern to the programmer may be obtained from the documents listed in the foreword of this manual.

GENERAL PROGRAMMING OPERATIONAL DESCRIPTION

The MC is a high-speed, I/O device which enables real-time communications between a 1700 Computer and a communications expansion network. The computer program controls the MC operation with address and control commands issued by the AQ channel.

Input and Output Control Words stored in the computer memory provide the MC with operational control pertinent to the individual system communications line and associated TU. The MC references memory to obtain these words when each TU connects to the unit for service. The TU provides status to the MC to indicate the service required and to convey information about the current data transmission. Each communications line is serviced in accordance with the information obtained from the TU status bits and Control Words in use with that line.

COMPUTER INTERFACE

The MC is one of up to eight peripheral devices which communicate with the computer through the IDC. The IDC contains three major sections that link the MC with the computer: AQ channel, Interrupt, and DSAB.

AQ CHANNEL

The computer addresses, or selects, the MC for operation, sends commands, and receives MC status information via the AQ channel. No data transfers take place between the MC and the computer on the AQ channel.

Q REGISTER

The computer Q Register sends address and command information. Since peripheral equipment shares the AQ channel, the address information is necessary to identify which peripheral device is to receive the commands. (Refer to figure 3-1 for the Q register format.)

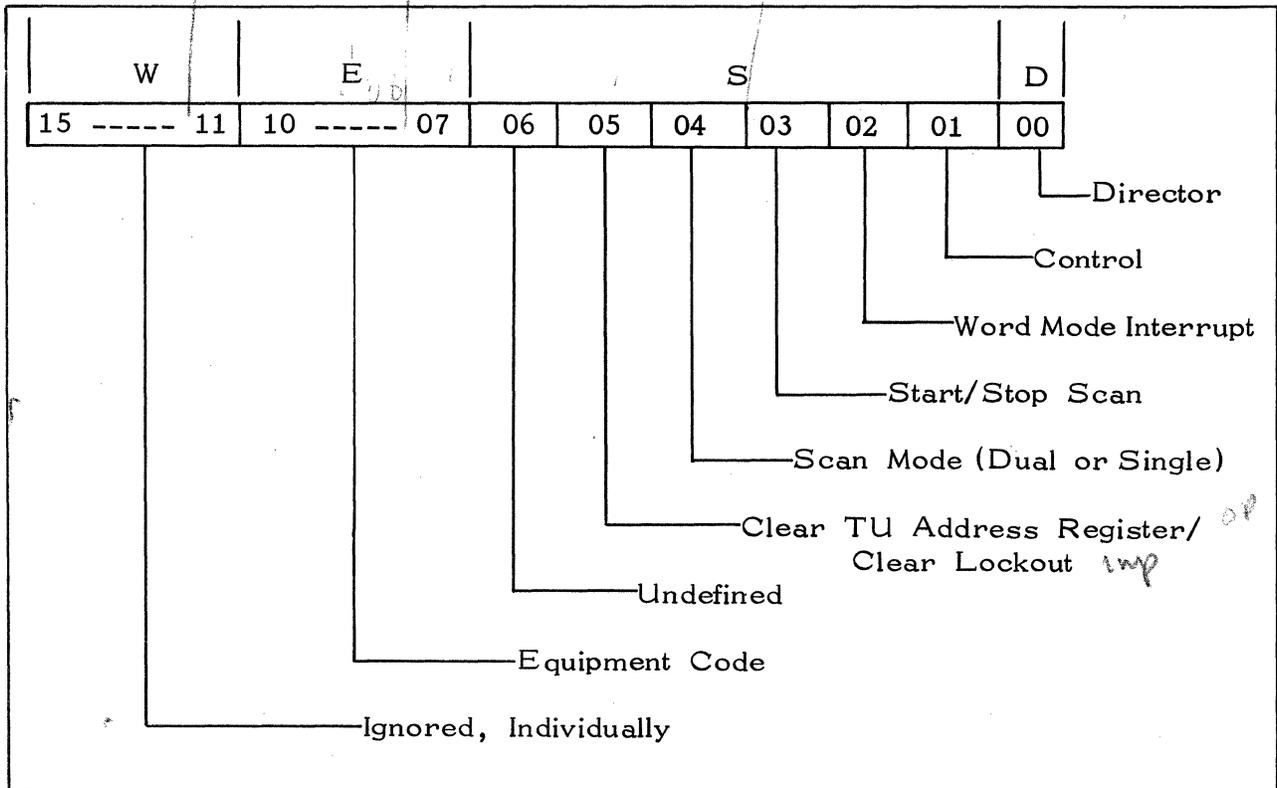


Figure 3-1. Q Register Format for Addressing and Commands

The W and E fields of the Q register format provide the addressing capability. The S field provides the commands.

W Field

The MC does not examine each bit of the W field. A separate W=0 signal as a "1" from the computer is required for selection of the MC, therefore all W field bits must equal zero.

E Field

The E field, bits Q10 through Q07, must reflect the Equipment Code number assigned to the MC in the system. When the combination of bits in the E field, and the settings of the EQUIPMENT NUMBER switches on the MC switch

panel match, the MC sends a Reply signal to the computer and responds to the commands. A Reply or Reject signal is sent to the computer 400 nanoseconds after selection of the MC occurs.

S Field

The S field of the Q register format consists of bits Q06 through Q01. Bit Q06 is undefined and is not used by the MC. Bits Q05 through Q01 identify the type of command being issued to the MC. Reference should be made to table 3-1 for the bit configurations and the commands they represent.

TABLE 3-1. Q REGISTER COMMANDS

S FIELD BITS						COMMAND	REMARKS
Q05	Q04	Q03	Q02	Q01	Q00		
X	1	X	X	0	1	Single Scan	These commands are used to establish the scan mode of the MC.
X	1	X	X	1	1	Dual Scan	
X	X	1	X	0	1	Stop Scan	The Stop Scan command causes a scanning MC to stop scanning when it has completed servicing the TU connected when the command is received. The Start Scan command causes scanning to resume with the next sequential address to be developed by the MC.
X	X	1	X	1	1	Start Scan	
X	X	X	1	0	1	Disable Word Mode Interrupt	The Word Mode Interrupt is a periodic interrupt used at the computer program's discretion.
X	X	X	1	1	1	Enable Word Mode Interrupt	The interrupt interval begins when the Enable Word Mode Interrupt command is received by the MC.
0	0	0	0	0	1	Status	Both commands request the MC to send its status information to the computer's A register. Interrupt Status also clears the interrupt at completion of the input to the computer's A register and deactivates the interrupt line.
0	0	0	0	1	1	Interrupt Status	

TABLE 3-1. Q REGISTER COMMANDS (CONT)

S FIELD BITS						COMMAND	REMARKS
Q05	Q04	Q03	Q02	Q01	Q00		
1	X	X	X	X	1	Clear TU Address Register	This command directs the MC to clear the last TU address transmitted to the MC.
1	X	X	X	X	0	Set TU Address Register	This command directs the MC's TU Address register to accept the address transmitted by the computer.
1	0	0	0	0	1	Clear Lockout and Status	This command directs the MC to clear the lockout and thus allow the MC to write an Interrupt word when another Input Acknowledge Failure occurs.

D Field (Director)

The Director bit Q00 and bit Q05 indicate to the MC that the A register contains a TU address to enable Character Request for that TU.

A REGISTER

The computer A register receives status information from the MC when the Q register performs a Status or Interrupt input on the channel. Refer to table 3-2 for the significance of the bit positions found in the A register format. The A register is also used to transfer TU addresses to the MC.

MC SELECTION

The MC requires that the following three conditions occur or exist simultaneously for selection of the unit by the computer:

- (1) All bits in the W field must be "0"s.
- (2) The E field bits must match the EQUIPMENT NUMBER switch settings.
- (3) An input or an output must be occurring.

TABLE 3-2. STATUS SIGNALS TO COMPUTER A REGISTER

STATUS BIT	SIGNAL NOMENCLATURE	DEFINITION
A10	Program Protect Fault	A "1" signal indicates that a Program Protect fault has been detected by the MC.
A09	Input Acknowledge Failure Lockout	A "1" indicates that an Input Acknowledge timeout failure has occurred. Subsequent Input Acknowledge Failure interrupts will be locked out until this condition is cleared with a Clear Lockout function from the computer.
A08	End of Operation Interrupt	A "1" signal is issued when the TU address transmitted from the computer compares with the address from the multiplexing system.
A07	Dual Mode Established	A "1" signal is issued when Dual Scan mode has been established and each unit is monitoring the other and each computer is doing a read or write within every 200 ms on the AQ channel.
A06	Not Scanning, Other Unit	A "1" signal issued in dual-system operation to notify the computer program that the secondary MC is not scanning.

TABLE 3-2. STATUS SIGNALS TO COMPUTER A REGISTER (CONT)

STATUS BIT	SIGNAL NOMENCLATURE	DEFINITION
A05	Scan Failure Interrupt, Other Unit	A "1" signal issued in dual system operation to notify the computer program that the secondary MC is scanning too slowly or not at all.
A04	Scan Failure Interrupt, This Unit	A "1" signal issued in dual system operation to notify the computer program that the MC is scanning too slowly or not at all.
A03	TU Interrupt	A "1" signal indicates that the MC has detected one or more of the following interrupt conditions while servicing a TU: End of Input or Output Buffer, TU Bit 08 or 09, Input or Output Acknowledge Failure.
A02	Word Mode Interrupt	A "1" signal issued periodically to notify the computer program of the occurrence of the interrupt. This interrupt is enabled or disabled by the computer program.
A01	Busy	A "1" signal is present as long as the MC is processing each TU address transmitted by the computer.

PROGRAM PROTECT OPERATION

When the PROGRAM PROTECT switch is in the Protected position, the MC rejects all unprotected commands for which it is selected except a request issued for status. The rejected commands include Interrupt Status. When the switch is not on, the MC responds to all commands for which it is selected.

INTERRUPT CHANNEL

The MC develops an Interrupt signal each time it detects a scan failure in the unit or in a secondary MC when a dual system is used. The MC also develops an Interrupt signal each time a TU Interrupt, Program Protect, End of Operation, or the Word Mode Interrupt (periodic) condition occurs. The Interrupt signal is transferred to the IDC via a separate signal cable carrying only the Interrupt signal. The IDC Interrupt channel is responsible for controlling the Interrupt signal once developed and transmitted by the MC. The computer acknowledges the Interrupt by requesting Interrupt Status via the Q register. The MC then transmits the status information to the computer via the A register. The status information identifies the reason(s) for the Interrupt signal. The interrupt condition is cleared after the MC completes transfer of the status information to the computer's A register. When the Interrupt signal is caused by a TU Interrupt condition, the MC automatically activates an Interrupt sequence which takes place after all data transfers are completed. The Interrupt sequence writes an Interrupt Word into storage which identifies the reason for the TU Interrupt, the network expansion devices, and the TU connected to the MC at that time.

DIRECT STORAGE ACCESS BUS (DSAB)

All data communications between the MC and the computer storage take place via the DSAB section of the IDC. Storage addresses and control words are also transferred via the DSAB.

STORAGE ADDRESSES

Each time the MC references storage, the MC must develop and transfer to the computer a Storage address to identify the desired storage location. The MC develops the individual addresses required for the control words, interrupt words, and data. The address format contains 15 bits.

CONTROL WORDS

The computer program must store control words for each TU in the system to provide the MC with instructions and buffer storage addresses for input and output data operations. The control words are stored in a block of storage locations reserved for this purpose. The MC must reference storage to read

two control words each time an Input-to-Storage or an Output-from-Storage data transfer is performed.

CONTROL WORD ADDRESS

Refer to figure 3-2 to obtain the Control Word Address format. The CONTROL WORD BANK switches on the MC switch panel are used to manually address the particular block of storage locations reserved for control words. The CONTROL WORD BANK switches determine the status of bits 14 through 11 of the 15-bit address. Bits 10 through 08, 07 through 05, and 04 through 02 are the addresses generated by the individual levels of the expansion network. Bits 10 through 02 identify the individual TU connected to the MC at the time the storage reference takes place. Bit 01 indicates whether the storage reference concerns an Input-to-Storage data transfer or an Output-from-Storage data transfer. This bit determines whether the control word desired is an Input or Output Control Word. If the bit is a "1" the control word is an Output Control Word. Bit 00 indicates which of the two control words (CW-1 or CW-2), available in either the Input or Output category, is desired. If the bit is a "0", CW-1 is addressed.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Control Word Bank Switches				3rd-Level Address			2nd-Level Address (MC)			TU <i>glw</i> Address					

NOTES:

- (1) Bit 15 is undefined.
- (2) Bit 01 indicates whether the desired Control Word is Input or Output.
- (3) Bit 00 indicates which of the two Control Words, CW-1 or CW-2, is desired.
- (4) Bits 10, 09, and 08 are not used and are always "0"s when the system does not have a third expansion level.

Figure 3-2. Control Word Address Format

Input Control Word-1 (Input CW-1)

Refer to figure 3-3 for the Input CW-1 format. Input CW-1 provides storage activity information and operating instructions necessary for MC performance of the Input-to-Storage data transfer. Input CW-1 also provides the partial address of the last storage location in the series of the buffered storage locations assigned to the TU. The last buffered storage location is called the Last Word Address (LWA). Bit 15 of Input CW-1 is the Activity bit. When the Activity bit is a "1", the MC proceeds according to the instructions contained in Input CW-1. Bit 14 is an instruction bit and specifies the mode of operation necessary for the MC to complete the Input-to-Storage data transfer. Bit 14 as a "1" indicates the Buffer mode; as a "0", the Word mode. Bit 13 specifies the submode of operation that the MC must use when the Buffer mode is specified. When bit 13 is a "1", the computer specifies the character submode; a "0" indicates the NOT character submode. Bit 12 provides computer control of the TU Status Bit Interrupt. A "1" enables and a "0" disables the Interrupt. Bits 11 through 00 form the partial LWA. The LWA is not used by the MC when bit 14 specifies the Word mode.

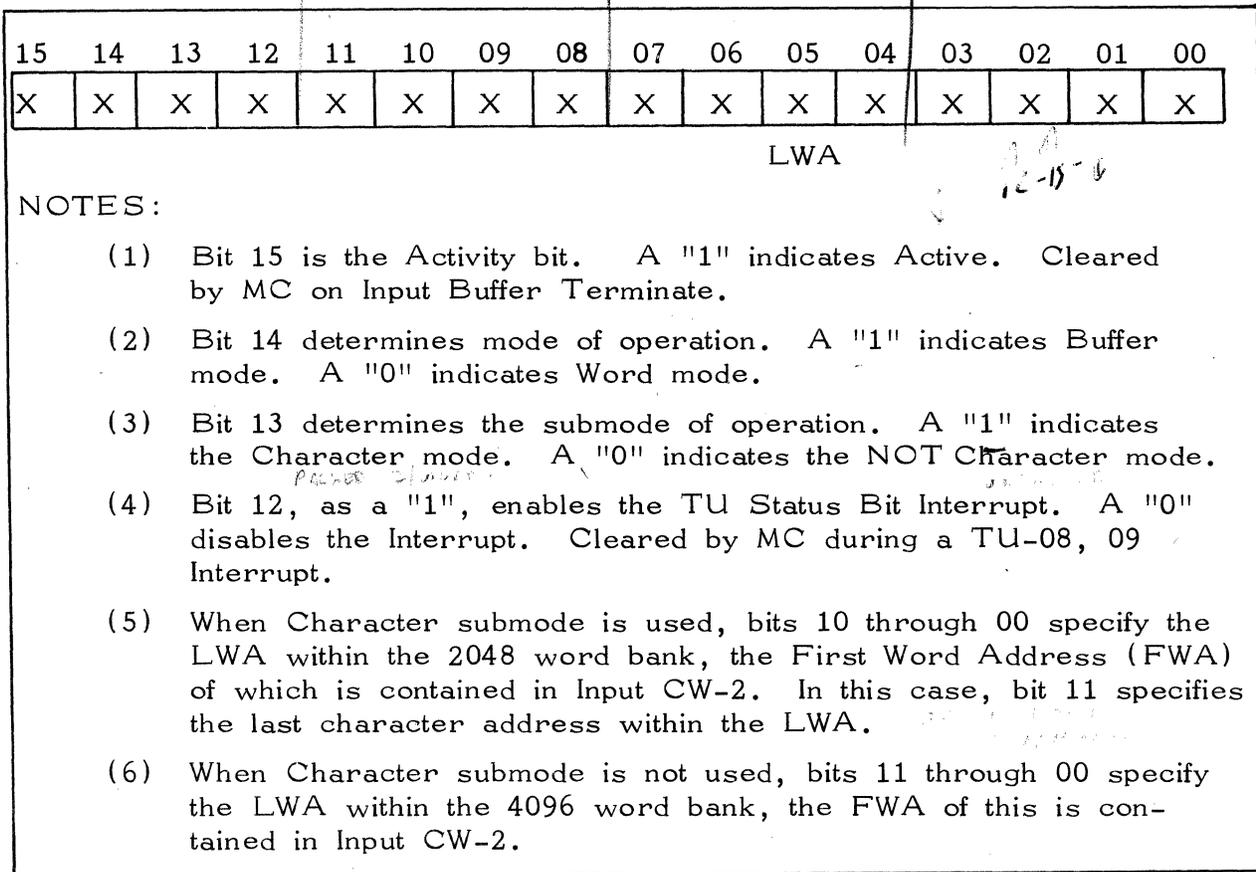


Figure 3-3. Input CW-1 Format

Input Control Word-2 (Input CW-2)

Refer to figure 3-4 for the Input CW-2 format. Input CW-2 provides the address of the next consecutive storage location available in the series of buffered storage locations assigned to the TU. This address is initially the First Word Address (FWA) and becomes the current word address as the data transfer progresses. Input CW-2 also provides a Flag bit, bit 15. In the Word submode, bit 15 is complemented from a "0" to a "1" by the MC, and the MC will not write into the indicated storage location until bit 15 is changed from "1" to "0" by the computer program. In the Character submode, bit 15 identifies the current Character address within the first or current word address. Bits 14 through 00 form the FWA.

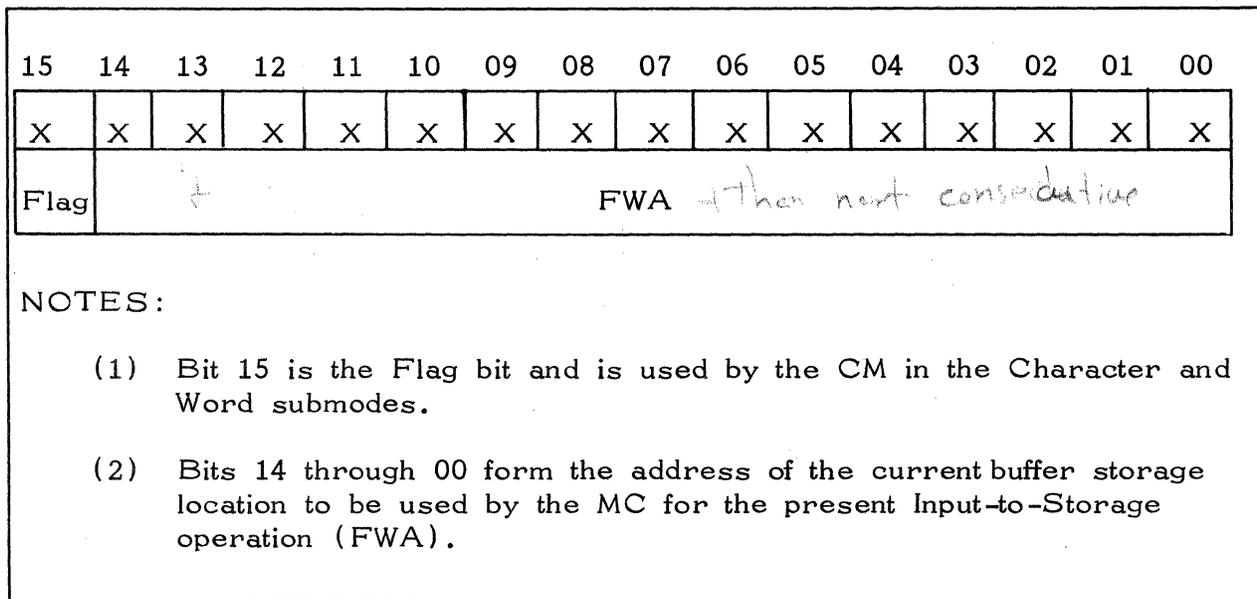


Figure 3-4. Input CW-2 Format

Output Control Word-1 (Output CW-1)

The Output CW-1 control word format is identical to the Input CW-1 format except that bit 12 of Output CW-1 is used to enable or disable Character Request. The MC responds to the control word to perform an Output-from-Storage sequence of operation.

ECR

Output Control Word-2 (Output CW-2)

The Output CW-2 control word format is identical to the Input CW-2 format. Output CW-2 contains a Flag bit, bit 15, and an FWA, the latter being the address of the storage location containing data for the TU. In the Word sub-mode the Flag bit must be a "1" before the MC will output the data. After performing the output the MC complements the Flag bit and stores a "0" at bit 15.

INTERRUPT

The MC monitors certain conditions while servicing each TU. When the MC detects a situation that requires the attention of the computer program, an Interrupt signal is generated and sent to the computer. The computer acknowledges the Interrupt signal by requesting Interrupt Status via the AQ channel.

The MC then sends its status information to the computer A register. The status bits identify the type of interrupt for the computer. When the type involved is a TU Interrupt, the MC must also write an Interrupt Word into storage. The Interrupt Word identifies the specific condition causing the interrupt and also the network expansion devices and TU connected at the time the interrupt occurred.

Interrupt Control Address

When the MC is required to write an Interrupt Word into storage, the unit must first develop an Interrupt Control Word Address. The MC switch panel contains 15 INTERRUPT CONTROL WORD ADDRESS switches which provide manual insertion of a permanent 15-bit address. The Interrupt Control Word Address identifies a fixed location in storage. The fixed location in storage contains the address of the storage location that the computer intends to use for receiving and storing the Interrupt Word. The address contained in the fixed storage location is the Interrupt Word Address.

Interrupt Word Address

The MC reads the fixed storage location determined by the INTERRUPT CONTROL WORD ADDRESS switches to obtain the Interrupt Word Address. The Interrupt Word Address contains 15 bits. The MC, in turn, uses the Interrupt Word Address to write the Interrupt Word into storage. The MC also adds one to the Interrupt Word Address and writes it back into the fixed storage location represented by the INTERRUPT CONTROL WORD ADDRESS switches. The Interrupt Word Address, advanced by one, becomes the new Interrupt Word Address referenced when the next TU Interrupt occurs.

TU 6 2

Interrupt Word

The MC writes an Interrupt Word into storage to inform the computer of the specific TU Interrupt condition responsible and of the TU and expansion devices connected to the MC at the time. Refer to figure 3-5 for the Interrupt Word format.

3A3
36A

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Exp 00B 8-1 9-1 11-1

NOTES:

3rd level 2nd level TU

- (1) Bit 15 as a "1" indicates an End of Input Buffer condition.
- (2) Bit 14 as a "1" indicates an End of Output Buffer condition.
- (3) Bit 13 as a "1" indicates that TU Status bit 08 is a "1".
- (4) Bit 12 as a "1" indicates that TU Status bit 09 is a "1".
- (5) Bit 11 as a "1" indicates that TU Status bit 11 is a "1" (not an interrupt; included for information purposes only).
- (6) Bits 10 through 08 identify the 3rd-level CM by octal address when a third level is used in the expansion network.
- (7) Bits 07 through 05 identify the 2nd-level CEU or CM module by octal address.
- (8) Bits 04 through 02 identify the TU by octal address.
- (9) Bit 01 as a "1" indicates a TU Acknowledge Failure, Input.
- (10) Bit 00 as a "1" indicates a TU Acknowledge Failure, Output.

Figure 3-5. Interrupt Word Format

DATA

Data transfers between the MC and storage occur on a data cable containing 16 bidirectional data lines. Data transfers from the MC to storage may contain either 8 or 16 actual data bits. When eight data bits are transferred to storage, the remaining eight bits are read and written back into the location.

A data transfer from storage to the MC always consists of 16 data bits. Since the MC can transfer only 12 bits to the TU (eight data bits), circuits within the MC select which eight bits (upper or lower) are to be processed. Two TU service periods are required to complete transfer of a 16-bit word from storage to a TU.

EXPANSION NETWORK INTERFACE

Communication between the MC and the TUs via the expansion network consists of addresses, control signals, and data and status bits. The addresses and control signals provide the multiplexing function of the MC. A multiplexing function is necessary since the MC can service only one TU at a time. The TUs individually send their service requirements to the MC via the status bits. The MC exchanges data with each TU as required by the status bits and the control words.

MULTIPLEXING FUNCTION

The MC performs its multiplexing function by sequentially developing octal addresses from 0 to 7. These first-level addresses are issued by the MC to the second level of the expansion network as the MC completes the service of a TU. Only the expansion device (CEU or CM) assigned to the address issued by the MC responds. The expansion device responding to the address is, in turn, addressing either a third-level device or a TU, depending on whether or not the system has a third level of expansion. The expansion devices make available to the MC, as connection is established, the four TU status bits (if present), and the addresses developed by each expansion device connected. The addresses developed by the selected expansion device in each level of the network serve to identify the TU connected for service. The MC and the expansion devices are hardwired to perform the address changeovers resulting in progressive scanning of the TUs without program consideration.

Operation of the MC's scan of the TUs, through the expansion network, starts with a Start Scan command issued by the program on the AQ channel, and stops with a Stop Scan command from the same source. Refer to figure 3-6 for a typical TU data and status format.

4 TU 8 bits

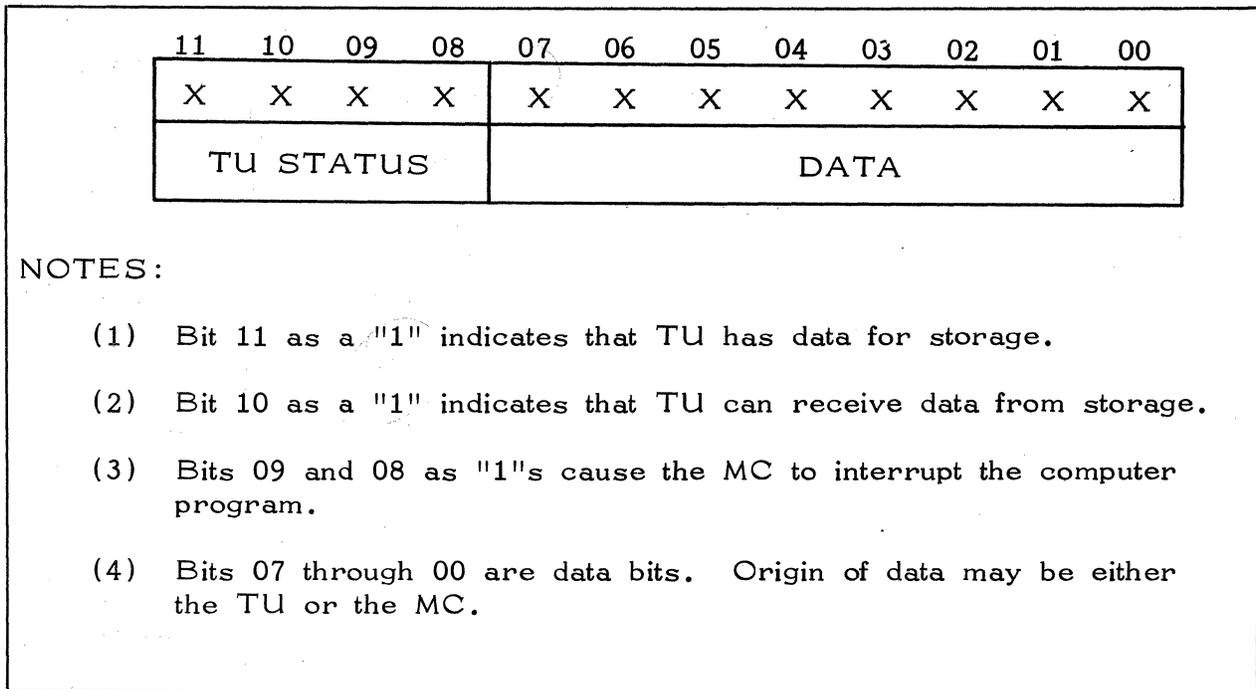


Figure 3-6. TU Data and Status Format

EXPANSION NETWORK CONTROL

The MC addresses and connects to each expansion device in the second level in sequence. While connected to each expansion device, the MC services the one TU addressed by the device. When the TU addressed by the last device in the second level has been serviced, the MC develops a Count signal which goes to each second-level device. The Count signal advances the address scan counter in each device by one. This action connects a new TU to each device for service. The MC again generates each address and services the TU as each expansion device connects to the MC.

DUAL SYSTEM INTERFACE

In a dual system, two MCs are connected, through the DMO, to the expansion network. With a dual system, input data can be transferred to either one, or the other, or both computers at the same time. However, only one computer can output data to a selected TU at the same time. Should both computers initiate an output at the same time the DMO will block both outputs causing the generation of an Output Acknowledge Failure.

To initiate dual system operation, one MC must be in the stop scan condition and the other MC must be in the single scan condition. Issuing a Dual Scan command to the stopped MC will cause it to enter Dual Scan mode and the MC in Single Scan mode will change to Dual Scan mode. Both MC's must not issue a Start Scan command at the same time.

FUNCTIONAL DESCRIPTION

The functional description contained in the following paragraphs is intended to convey an operational familiarity with the MC.

COMPUTER PROGRAM CONTROL

The computer controls MC operation, issuing the contents of its Q register to the unit via the AQ channel of the IDC. The contents of the Q register consist of address and command information which simultaneously arrives at the MC. Since the MC may be one of up to eight peripheral devices connected to the computer, the address selects the MC for receipt of the commands. When selected, the MC interprets the commands and responds by controlling the scan operation and other operational functions of the unit. The commands may also request that the MC send status information to the computer A register via the AQ channel in the IDC.

INTERRUPT SYSTEM

The MC, while having only one interrupt cable to the IDC, develops a variety of interrupts. The following paragraphs describe the interrupt operations of the MC.

Interrupt Detection

When the MC services a TU, certain prerequisite conditions must be satisfied for a successful data transfer. The MC monitors the prerequisite conditions and the TU status to detect a condition requiring computer program attention or a fault that would invalidate the data transfer. When the MC detects an interrupt condition or a fault, the unit issues an Interrupt signal to the computer. The computer acknowledges the Interrupt signal by sending a request for Interrupt Status via the Q register section of the AQ channel. The MC then sends status information to the computer A register via the AQ channel to identify the type of interrupt in effect.

Types of Interrupts

The types of Interrupts that may occur are as follows:

- (1) Word Mode Interrupt (Bit 02) - This is a periodic interrupt available for use by the computer program. The computer program may enable or disable the Word Mode Interrupt by command on the AQ channel. Once enabled, the interrupt occurs at regular intervals. The first interval begins with receipt of the Enable Word Mode Interrupt command by the MC. The interval between interrupts is adjusted to less than the inter-character interval of the TUs being used. The interrupt interval is pre-adjusted to 40 milliseconds.
- (2) TU Interrupt (Bit 03) - The MC develops the TU Interrupt when the monitoring circuits internal to the unit detect one of the following conditions.
 - (a) End of Input Buffer - Indicates that the block of computer storage locations assigned to the TU being serviced is filled with data received from the TU. This interrupt clears bit 15 of Input CW-1.
 - (b) End of Output Buffer - Indicates that all data in the block of computer storage locations assigned to the TU being serviced has been transferred to the TU. This interrupt generates a disable Character Request signal to the CM.
 - (c) TU Bit 08 - Indicates that status bit 08, received from the TU, is a "1". This interrupt is enabled when Input CW-1 bit 12 is a "1". Occurrence of this interrupt will clear bit 12.
 - (d) TU Bit 09 - Indicates that status bit 09, received from the TU, is a "1". This interrupt is enabled when Input CW-1 bit 12 is a "1". Occurrence of this interrupt will clear bit 12.
 - (e) TU Acknowledge Failure - Indicates that the TU being serviced has failed to acknowledge an input or output from the MC. Input Acknowledge Failure Interrupt is enabled when either Input CW-1 bit 15 or bit 12 is a "1". Output Acknowledge Failure Interrupt is enabled when Output CW-1 bit 15 is a "1".
- (3) Scan Failure Interrupt, This Unit (Bit 04) - Indicates that this MC is scanning more slowly than is acceptable, or has stopped scanning.
- (4) Scan Failure Interrupt, Other Unit (Bit 05) - Indicates that the other MC in a dual system is scanning more slowly than is acceptable or has stopped scanning.

- (5) End of Operation Interrupt (Bit 08) - Indicates that the TU address has compared with the address transmitted by the computer and Busy status has been cleared and Enable Character Request was sent to the TU.
- (6) Input Acknowledge Failure Lockout (Bit 09) - Indicates that an Acknowledge from a TU was not received for an Input signal within 20 milliseconds. All further Input Acknowledge Interrupts will be disabled until this lockout is cleared by the software with a Clear Lockout function from the computer AQ channel.
- (7) Program Protect Fault (Bit 10) - Indicates that the MC violated Program Protect. This status is cleared by any Read on the AQ channel.

Writing Interrupt Word

When a TU interrupt condition is detected while servicing a TU, the MC generates an interrupt. The computer acknowledges receipt of the interrupt by sending an Interrupt Status command to the MC on the AQ channel. The MC then sends the status information to the computer, also via the AQ channel. The data transfer in progress on the DSAB continues uninterrupted during the AQ-channel exchange. After completion of the data transfers required for TU service, and before advancing to the next TU, the MC forms an Interrupt Control Word Address using the settings of the INTERRUPT CONTROL WORD ADDRESS toggle switches on the MC switch panel. This address identifies the assigned location in storage which contains the Interrupt Control Word. The Interrupt Control Word contains the current Interrupt Word address to be used by the MC for storage of the Interrupt Word. The MC uses the Interrupt Control Word address to obtain the Interrupt Control Word from storage. The MC then uses the current Interrupt Word address obtained from the Interrupt Control Word to write the Interrupt Word into storage. The MC also updates and writes the Interrupt Control Word back into the assigned storage location. The Interrupt Word identifies the TU Interrupt condition responsible for the interrupt and identifies by address the expansion devices and the TU connected to the unit when the interrupt occurred. There is no hardware termination of an interrupt buffer area. The program must monitor and control the memory area assigned as an interrupt buffer.

Programming Considerations

There is no interlock to prevent a subsequent Interrupt Word from being written while the interrupt corresponding to the previous Interrupt Word is being processed. Therefore, the MC could write a subsequent Interrupt Word and initiate an interrupt between program actions of clearing the interrupt corresponding to the previous Interrupt, and reading that previous Interrupt Word.

A program scheme, independent of the last used Interrupt Word address, and which enables identification of unevaluated Interrupt Words, is required.

DATA TRANSFER

When a TU requiring service is connected to the MC, the unit transfers data, bidirectionally when necessary, to satisfy the requirements of the TU in accordance with commands and instructions from the computer. A TU can send one 8-bit data character and receive one 8-bit data character while connected to the MC for service. Data communication in either direction between the MC and the computer during one service period can be via one or two characters. Two characters form a 16-bit word. The number of characters transferred between the MC and the computer depends on the mode of operation in effect at the time of transfer.

SEQUENCE DEVELOPMENT

Each time a TU connects to the MC for service, the MC can perform from one to three operational sequences. The three operational sequences are the Input-to-Storage sequence, the Output-from-Storage sequence, and the Interrupt sequence. As a TU is connected to the MC, four status bits (11 through 08) and an 8-bit character (bits 07 through 00) arrive at the unit. The MC sequence circuits examine the status bits to determine the TU's service requirements. If TU Status bit 11 is a "1", the TU has a data character ready for storage, and an Input-to-Storage sequence is required. An Input sequence is also started if TU bits 08 and/or 09 are "1"s. TU Status bit 10 as a "1" indicates that the TU can receive a data character if a character is available in storage. Therefore, an Output-from-Storage sequence is required. If either Status bit 09 or 08 is a "1", an Interrupt sequence is required to inform the computer of the condition. The occurrence of this interrupt depends on an enabling instruction from the computer. An Interrupt sequence can still develop because of other conditions previously described even though Status bits 09 and 08 are both "0"s.

CONTROL WORDS

The computer controls the general operation of the MC with the commands sent via the AQ channel. The computer also controls the handling of data for each TU individually with four 16-bit control words in storage locations assigned to each TU. Two of the control words (Input CW-1 and Input CW-2) are necessary to control an Input-to-Storage sequence. The remaining two control words (Output CW-1 and Output CW-2) control the Output-from-Storage sequence.

MC-TU
inp
out
int
p-3-14

The control words contain the control information and the address information necessary for placement or removal of the data in storage. The Input and Output control word formats are the same except for bit 12. After the MC examines the TU Status bits and determines that service is required, the unit performs a storage operation to read the Input or Output CW-1, whichever is required. CW-1 contains both control information and address information for the placement or removal of data from storage. The control information tells the MC if it should continue, and if so, what modes of operation to use. The two major modes are the Word mode and the Buffer mode.

The Buffer mode is further subdivided into the Character submode or NOT Character submode. The address information contained in a CW-1 corresponds to the last storage location in a block of storage locations assigned to the TU being serviced. The address is the LWA or Last Character Address. The LWA applies only to buffer-mode operation and is not used when the Word mode is specified in the control information. When the Word mode is in effect, the MC either writes or reads (Input-to-Storage or Output-from-Storage, respectively) data into or out of the CW-2 storage location. The MC does not write data into the CW-1 location. The MC performs a second storage operation to read the Input or Output CW-2, whichever is required. CW-2 contains a Flag bit and additional address information. The Flag bit tells the MC what operation is required in the character submode or if the Word mode transfer is to be executed. The address portion of CW-2 identifies the storage location farthest from the LWA in the block of storage locations assigned to the TU connected for service. This address is the FWA or First Character Address and is used during the Buffer mode only. During the Buffer mode, the MC writes or reads data from the FWA (current word address). The MC also compares the current word address and the LWA to be certain the two addresses are not the same. When the current word address and LWA are the same, all storage locations in the assigned block have been filled with data or have been read out to the TU, depending on which data transfer sequence is in effect. When the current word address and the LWA are not the same, indicating the availability of additional storage locations in the block, the MC advances the current word address to the next consecutive address. The MC writes the new address (current word address +1) into the CW-2 storage location. The new address becomes the FWA used during the next service period for the TU presently connected to the MC.

MODES AND SUBMODES

Word - data to CW-2
Buffer

The MC transfers data by one of the two modes of operation previously mentioned, i.e., the Word mode or the Buffer mode. The Word mode is the least complex from the standpoint of MC operation. When the Word mode is in effect, the MC simply transfers data to and from the CW-2 storage location assigned to the TU being serviced. The Buffer mode speeds operation by minimizing the amount of attention required of the computer program. The MC further subdivides the Buffer mode into two submodes, the Character submode and the NOT Character submode.

Character Submode During Input to Storage Sequence

Buffer

During Character submode operation in an Input-to-Storage sequence, the MC examines the Flag bit in CW-2. For two-character buffer operation when the Flag bit is a "0", the MC must perform the first of two service periods required for the connected TU to supply two characters. During the first of the two service periods, the MC writes the data character from the TU into the upper eight bit positions of the 16-bit buffer storage location represented by the FWA. The lower eight bit positions are read and rewritten unchanged. The first character supplied by the TU becomes the upper character of the assembled word. After the first service period is completed, the MC continues to service other TUs before returning to the TU to perform the second of two service periods. The MC recognizes the second service period when the Flag bit in CW-2 is a "1". The MC reads the upper character (written into storage during the first service period) from storage into a register in the unit. The upper character also occupies the upper eight bit positions in the MC register. The MC adds the second data character to the register in the lower eight bit positions. Now the word, having both upper and lower characters, is complete. The MC writes the complete word into storage at the location previously occupied by the upper character. The FWA is then incremented by "1" and the Flag bit in CW-2 is set to a "0". For one-character buffer operation when the Flag bit is a "1", the MC performs one service period and transfers one character only to the storage location represented by the FWA. The data character is written into the lower eight bit positions and the upper eight bit positions are read and rewritten unchanged. The next service period for the connected TU will involve the next storage location.

ch

MC sets Flag bit in CW-2

Character Submode During Output from Storage Sequence

During Character submode operation in an Output-from-Storage sequence, the MC examines the Flag bit in CW-2. For ~~two-character buffer operation~~, when the Flag bit is a "0", the MC performs the first of two service periods necessary to transfer a word (two characters) to a TU. In the first service period, the MC reads the upper character from the storage location and into a register for transfer to the TU. After transfer of the character, the MC continues on to service other TUs before returning to the TU to perform the second of the two service periods. The MC recognizes the second service period when the Flag bit in CW-2 is a "1". During the second service period the MC reads the lower character from storage into a register in the unit for transfer to the TU. Transfer of the lower character completes the transfer of a data word to the TU. The FWA is then incremented by "1" and the Flag bit in CW-2 is set to a "0". For ~~one-character buffer operation~~ when the Flag bit is a "1", the MC performs one service period and transfers only one character (lower eight bit positions) from the storage location into an MC register. This character is transferred by the MC to the connected TU. The next service period will involve the next storage location.

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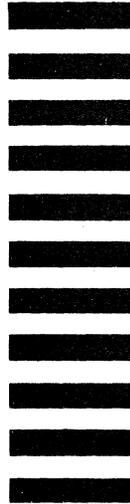
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