

**3600 SYSTEM
DESIGN HANDBOOK**

CONTROL DATA
CORPORATION

COMPUTER DIVISION

September 25, 1962

TO: *Bob Hesslund*

This Design Handbook is the result of the efforts of many individuals in the Computer Division. It has been prepared for the purpose of disseminating technical information concerning circuits and logic to the other groups within the corporation and to provide a ready reference source for the useage of 3600 building blocks.

I would like to call your attention to the paragraph on the cover sheet concerning the confidential nature of the information in this Handbook. Your attention is also called to the registration number which is assigned to each individual copy. You will be held responsible for this particular copy, and further additions and deletions will be sent to you.

Any comments concerning the use, improvement, and criticism of the Handbook would be appreciated and should be addressed to the undersigned.

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CDC # 8

Registration Number

3600 DESIGN HANDBOOK

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NOTE

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CHAPTER 1
COMPONENT SPECIFICATIONS

The following pages list significant characteristics of electronic components used in 3600 system printed circuit development.

DIODES

	Parameter	Condition	Limit	CDC Item No.
HD4416 Hughes Silicon	Forward Voltage V_f Dynamic Impedance Z_D	$I_f = 2 \text{ ma}$ $I_f = 2 \text{ ma}$ $f = 1000 \text{ cps}$	$0.67\text{v} \pm 50 \text{ mv}$ < 100 ohms	4203
FD 1032 Fairchild Silicon	Forward Current I_f Reverse Current I_r (Other characteristics similar to FD 100)	$V_f = 1 \text{ v}$ $V_r = 40 \text{ v}$	> 10 ma < 0.1 ua	4210
HD 2969 Hughes Germanium	Forward Voltage V_f Working Inverse Voltage WIV Recovery Time T_{rr} (Covered by Control Data Corporation spec. 118-012)	$I_f = 3 \text{ ma}$ Switching from $I_f = 3 \text{ ma}$ to $V_r = 5 \text{ v}$	0.35v max. 40v min. 0.6 usec max.	4200
FDS 2055 Fairchild Silicon	Forward Current I_f Forward Voltage V_f Breakdown Voltage B_v (Other characteristics similar to FD 400)	$I_f = 150 \text{ ma}$ $I_r = 100 \text{ ua}$	400 ma max. < 1.0v > 75v	4211
HD 1871 Hughes Germanium	Forward Voltage V_f Breakdown Voltage B_v Recovery Time T_{rr}	$I_f = 10 \text{ ma}$ Switching from $I_f = 10 \text{ ma}$ to $V_r = 6 \text{ v}$	0.42v max. 10v min. 0.35 usec max.	

ZENER DIODES

	Zener Breakdown Voltage V_z at 25° C		Dynamic Impedance ZD	Reverse Current
	Min.	Max.	Max.	Max.
1N703 Hughes Silicon	3.0v	3.9v at 5ma	55Ω at 10ma	
1N704A Hughes Silicon	3.9v	4.3v at 5ma	45Ω at 10ma	5ua at -1v
1N965B Motorola Silicon	14.25v	15.75v at 8.5ma	16Ω at 8.5ma	
1N753 Motorola Silicon	5.6v	6.8v at 20ma		
1N705A Hughes Silicon	4.6v	5.1v at 5ma	35Ω at 10ma	5ua at -1.5v

TUNNEL DIODES

		Current		Peak-to-Valley	Voltage		Forward	Valley-to-Peak
		Peak	Valley	Current Ratio	Peak	Valley	Voltage	Voltage Ratio
		I_p	I_v	I_p/I_v	V_p	V_v	V_{fp}	V_v/V_p
TD-1 G. E. Germanium	Maximum	1.1ma	0.18ma		65mv	350mv	500mv	
	Typical	1.0ma	0.12ma					
	Minimum	0.9ma						
IN2931 Hoffman Silicon	Maximum	11ma		3.5	65mv	470mv	790mv	6.8
Typical	10ma							
Minimum	9ma							

TYPE C01
TRANSISTOR
(PNP GERMANIUM)

PARAMETER	CONDITION	LIMIT
Breakdown Voltage BVCEO	IC = 10 ma	> 7v
Breakdown Voltage BVEBO	IE = 100 μ a	> 1v
Current Gain hFE	IC = 20 ma VCE = 1v	> 40
Gain Bandwidth ft	IC = 20 ma VCE = 1v	> 300 mc

NOTE:

- I. Basic transistor similar to a 2N964
- II. Case size to conform to T0-18 outline
- III. Case to be marked C01

TYPE C02
TRANSISTOR
(PNP GERMANIUM)

PARAMETER	CONDITION	LIMIT
Breakdown Voltage BVCBO	$I_C = 100 \mu a$	> 25v
Breakdown Voltage BVEBO	$I_E = 100 \mu a$	> 1v
Current Gain h_{FE}	$I_C = 10 \text{ ma}$ $V_{CE} = 5v$	> 20
Gain Bandwidth f_t	$I_C = 10 \text{ ma}$ $V_{CE} = 5v$	> 300 mc

NOTE:

- I. Basic transistor similar to a 2N960
- II. Case size to conform to T0-18 outline
- III. Case to be marked C02

TYPE C03
TRANSISTOR
(PNP GERMANIUM)

PARAMETER	CONDITION	LIMIT
Breakdown Voltage BVCBO	$I_C = 100 \mu a$	$> 10v$
Breakdown Voltage BVEBO	$I_E = 100 \mu a$	$> 4v$
Current Gain h_{FE}	$I_C = 10 \text{ ma}$ $V_{CE} = 0.3v$	> 20
Gain Bandwidth f_t	$I_E = 20 \text{ ma}$ $V_{CB} = 1v$	$> 200 \text{ mc}$

NOTE:

- I. Basic transistor similar to a 2N705 or 2N960 through 2N966.
- II. Case size to conform to T0-18 outline
- III. Case to be marked C03

TYPE C04
TRANSISTOR
(NPN SILICON)

PARAMETER	CONDITION	LIMIT
Breakdown Voltage BVCBO	IC = 10 μ a	> 90v
Breakdown Voltage BVCEO	IE = 10 μ a	> 5v
Saturation Voltage VCE (Sat.)	IC = 400 ma IB = 40 ma	< 1.25v
Saturation Voltage VBE (Sat.)	IC = 400 ma IB = 40 ma	< 2v
Current Gain hFE	IC = 400 ma VCE = 10v	> 25
Gain Bandwidth ft	IC = 20 ma VCE = 20v	> 300 mc
Collector Capacitance COB	VCB = 10v IE = 0	< 8 uuf

NOTE:

- I. Basic transistor similar to a 2N2218a
- II. Case size to conform to T0-5 outline
- III. Case to be marked C04

TYPE C05
TRANSISTOR
(NPN SILICON)

PARAMETER	CONDITION	LIMIT
Breakdown Voltage BVCBO	$I_C = 10 \mu a$	$> 50v$
Breakdown Voltage BVEBO	$I_E = 10 \mu a$	$> 5v$
Saturation Voltage VCE (Sat.)	$I_C = 150 ma$ $I_B = 15 ma$	$< 0.4v$
Saturation Voltage VBE (Sat.)	$I_C = 150 ma$ $I_B = 15 ma$	$< 1.3v$
Current Gain hFE	$I_C = 10 ma$ VCE = 10v	> 35
Gain Bandwidth ft	$I_C = 20 ma$ VCE = 20v	$> 250 mc$

NOTE:

- I. Basic transistor similar to a 2N2218a
- II. Case size to conform to T0-5 outline
- III. Case to be marked C05

TYPE C07
TRANSISTOR
(PNP GERMANIUM)

PARAMETER	CONDITION	LIMIT
Breakdown Voltage BVCEO	IC = 1 ma	> 15v
Breakdown Voltage BVCEs	IC = 100 ua	> 20v
Breakdown Voltage BVEBO	IE = 1 ma	> 2v
Collector Leakage ICBO	VCB = 5v	< 5 ua
Current Gain hFE	IC = 10 ma VCE = 0.5v	> 30
Base-Emitter Saturation VBE (Sat)	IC = 10 ma IB = 1 ma	< 0.4v
Gain Bandwidth ft	IC = 5 ma VCE = 3v	> 100 mc
Collector Capacitance COB	VCB = 6v f = 4 mc	< 3 uuf

NOTE:

- I. Basic transistor similar to a 2N980.
- II. Case size to conform to TO-18 outline.
- III. Case to be marked C07.

TYPE 2N404
TRANSISTOR
(PNP GERMANIUM)

PARAMETER	CONDITION	LIMIT
Breakdown Voltage BV_{CBO}	$I_C = 20\mu a$	> 25v
Breakdown Voltage BV_{EBO}	$I_E = 20\mu a$	> 12v
Saturation Voltage $V_{CE} \text{ (Sat.)}$	$I_C = 12 \text{ ma}$ $I_B = 0.4 \text{ ma}$	< 0.35v
Current Gain h_{FE}	$I_C = 12 \text{ ma}$ $V_{CE} = 0.15v$	> 30 50, typical
Alpha-Cutoff Frequency $f_{\alpha b}$	$V_{CB} = 6v$ $I_C = 1 \text{ ma}$	> 4 mc 13 mc, typical

NOTE:

- I. Other characteristics covered by 2N404 specification.
- II. Case size to conform to TO-5 outline.

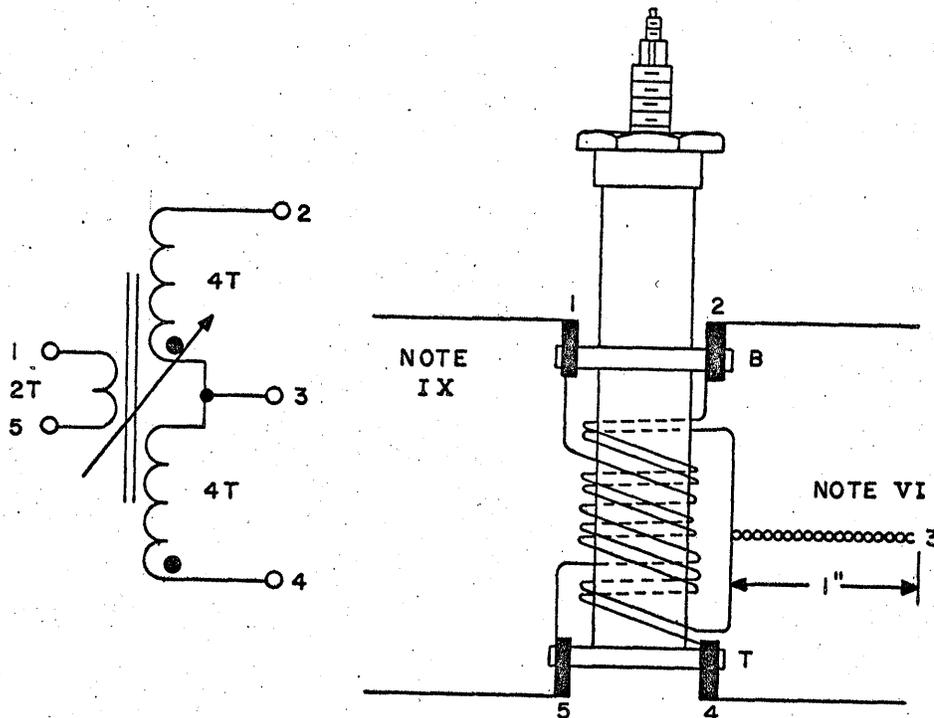
2N1760
TRANSISTOR
(PNP GERMANIUM)

PARAMETER	CONDITION	LIMIT
Breakdown Voltage BV_{CBO}	$I_C = 3.0 \text{ ma}$	$> 60\text{v}$
Breakdown Voltage BV_{BEO}	$I_E = 3.0 \text{ ma}$	$> 30\text{v}$
Saturation Voltage $V_{CE} \text{ (Sat.)}$	$I_C = 3.0 \text{ amp}$ $I_B = 200 \text{ ma}$	$< 0.7\text{v}$
Current Gain h_{FE}	$I_C = 0.5 \text{ amp}$ $V_{CE} = 2\text{v}$	> 60 100, typical

NOTE:

- I. Basic transistor similar to Clevite CTP1736 or 2N1760.
- II. Other characteristics covered by Clevite Bulletin TB226-2.

COIL
CLOCK OSCILLATOR-AMPLIFIER

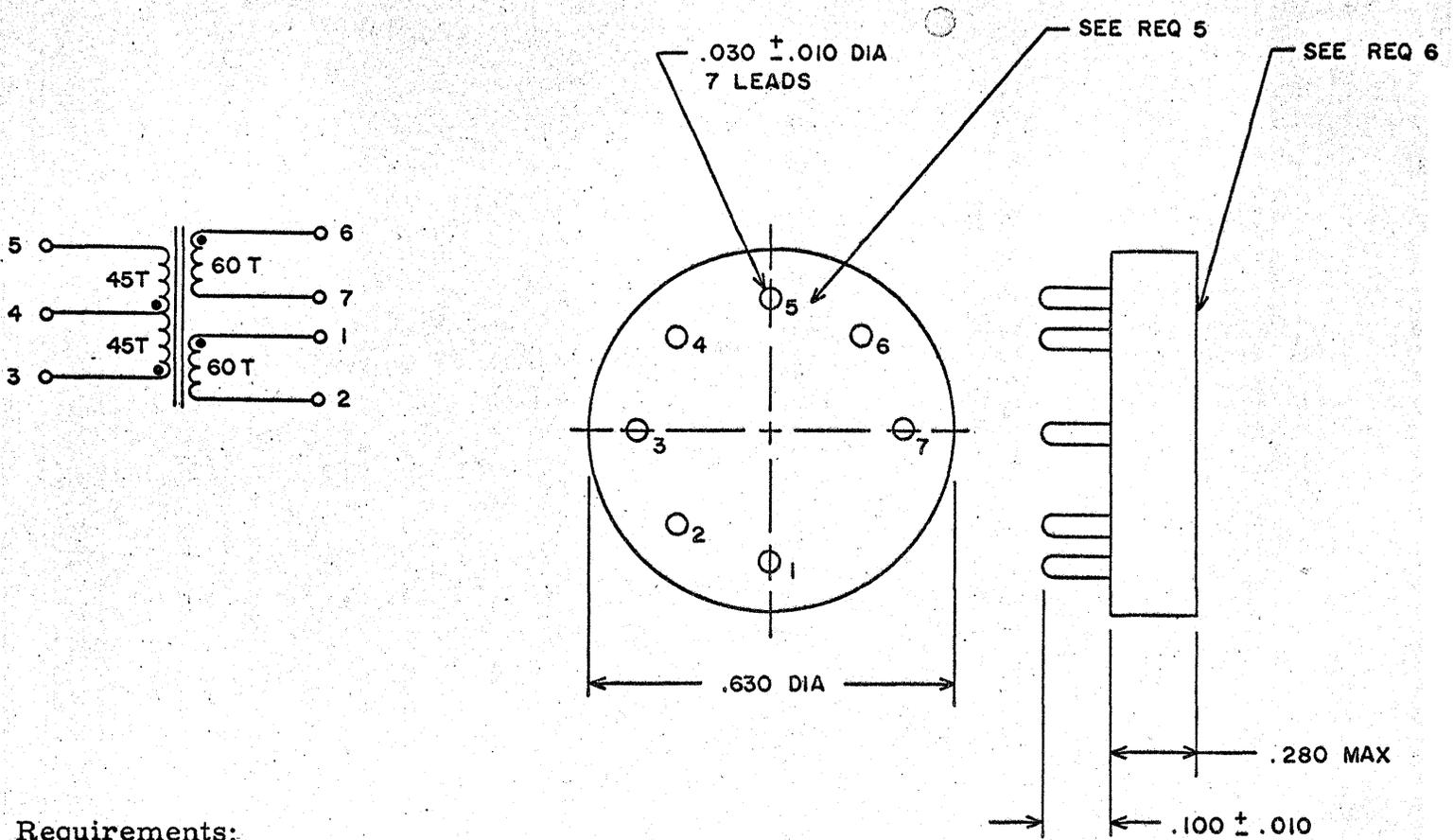


NOTES:

- I. Coil form similar to Cambridge Thermionic Corp. PLST-2C4L/H.
- II. Coil to be wound single layer with no spacing between turns.
- III. Coil to be wound bifilar with #32 enameled copper wire.
- IV. Coil to be adjacent to "T" collar with "B" collar to be moved to support winding.
- V. Center tap (#3) to be brought out twisted with a minimum length of 1 inch from collar edge.
- VI. Last 1/2 inch of twisted center tap lead to be tinned.
- VII. Solder lugs to be formed parallel to length of coil form.
- VIII. Tuning slug to be type 20063-H.
- IX. Tinned leads to be brought out 1 inch on terminals 1, 2, 4 and 5.

Figure 1

TRANSFORMER, PULSE
CARD TYPE C10



Requirements:

1. Workmanship shall be consistent with best commercial practices. Part shall conform to dimensions and tolerances on drawing.
2. **Material and Finish:**
 Core: General ceramics, Ferramic CF-102, type H.
 Winding: Phelps - Dodge #34 heavy Nyleze.
 Terminals: Brass. Copper preplate .00005 thick. Gold plate .00005 thick.
 Base and Cover: Mineral filled Phenolic type CFG per MIL-M-14F, color black, (Durez 11540) or equivalent pending approval by Control Data Corp.
3. Cement base to cover using Minnesota Mining and Manufacturing cement #505.
4. Wind the two 60-turn secondaries bifilar for 15 turns. Continue fourfilars for 45 turns. Connect the two 45 turn windings together to make the 90-turn center tap primary.
5. Mark terminals in approximate position as shown.
6. Mark part "300010" and revision letter to which part is manufactured, manufacturer's name or symbol, in approximate position as shown.

Figure 2

CHAPTER 2
LOGIC CARD TYPES

NAME	CIRCUIT	NUMBER
Single Inverter	One inverter circuit	C11-C17, and C51-C58
Double Inverter	Two separate inverter circuits	C21-C28
Flip-Flop	Two inverter circuits having cross-coupled feed back	C31-C37
Control Delay	Flip-flop having its feedback ANDED with a clock phase	C40-C49

Logic circuits are constructed with two types of inputs, logical AND and logical OR. All of the various logic cards and their respective input configurations are presented in the tables on the following pages.

The input configuration of a circuit is also represented by a number. For instance, card type C11 is a single inverter 116. This means that the circuit has two OR inputs and a six-way AND input.

Double inverter and flip-flop cards contain two circuits designated A and B. Each has separate inputs and the configurations are not necessarily symmetrical.

Control delay cards also contain two circuits designated A and B. All logic inputs pertain to circuit A, and all OR inputs are effectively single-way ANDs and must be grounded if not used.

INPUT SYMBOLS

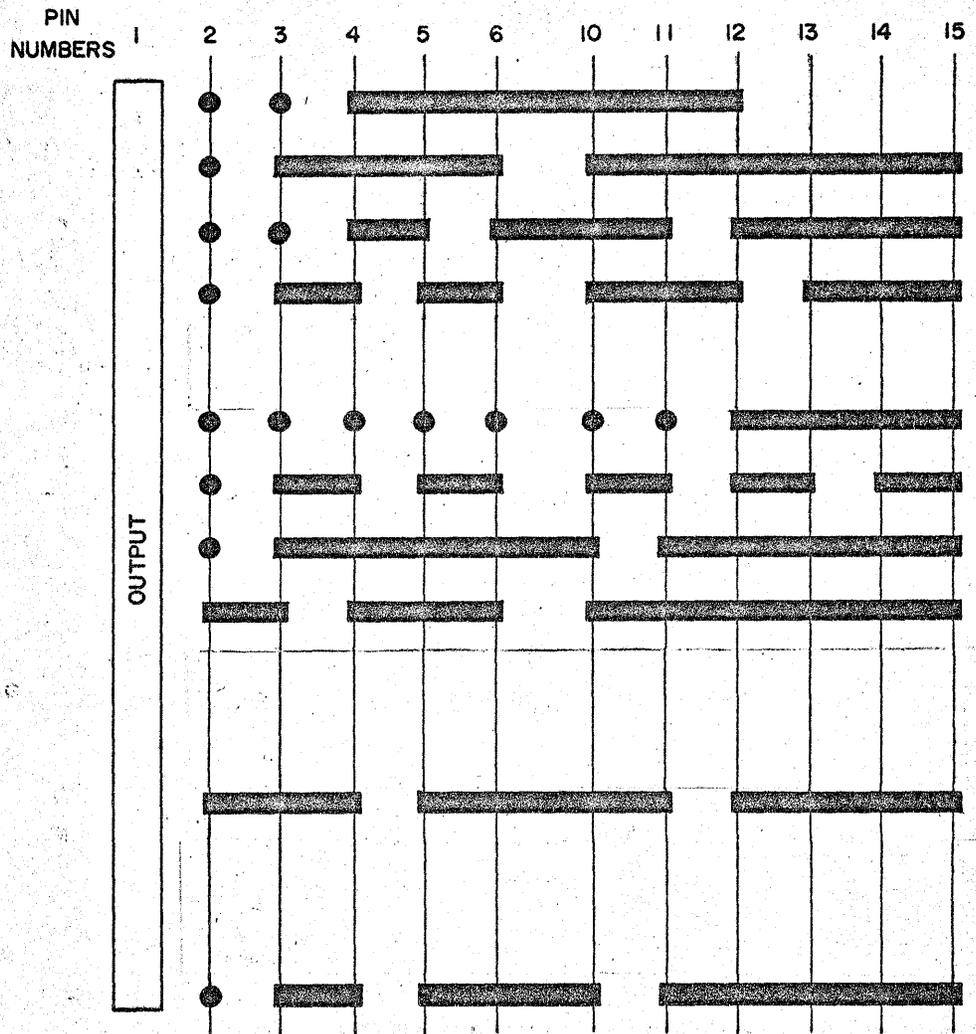
OR ●

AND ■

LOGIC CARD PIN CONNECTIONS

Single Inverter

C11	116
C12	146
C13	11234
C14	12233
C16	11111114
C17	122222
C51	155
C52	236
C55	344
C58	1235



NOTE:

PIN 7, +20v
 PIN 8, GND
 PIN 9, -20v

Figure 1. Single Inverter

INPUT SYMBOLS

OR ●

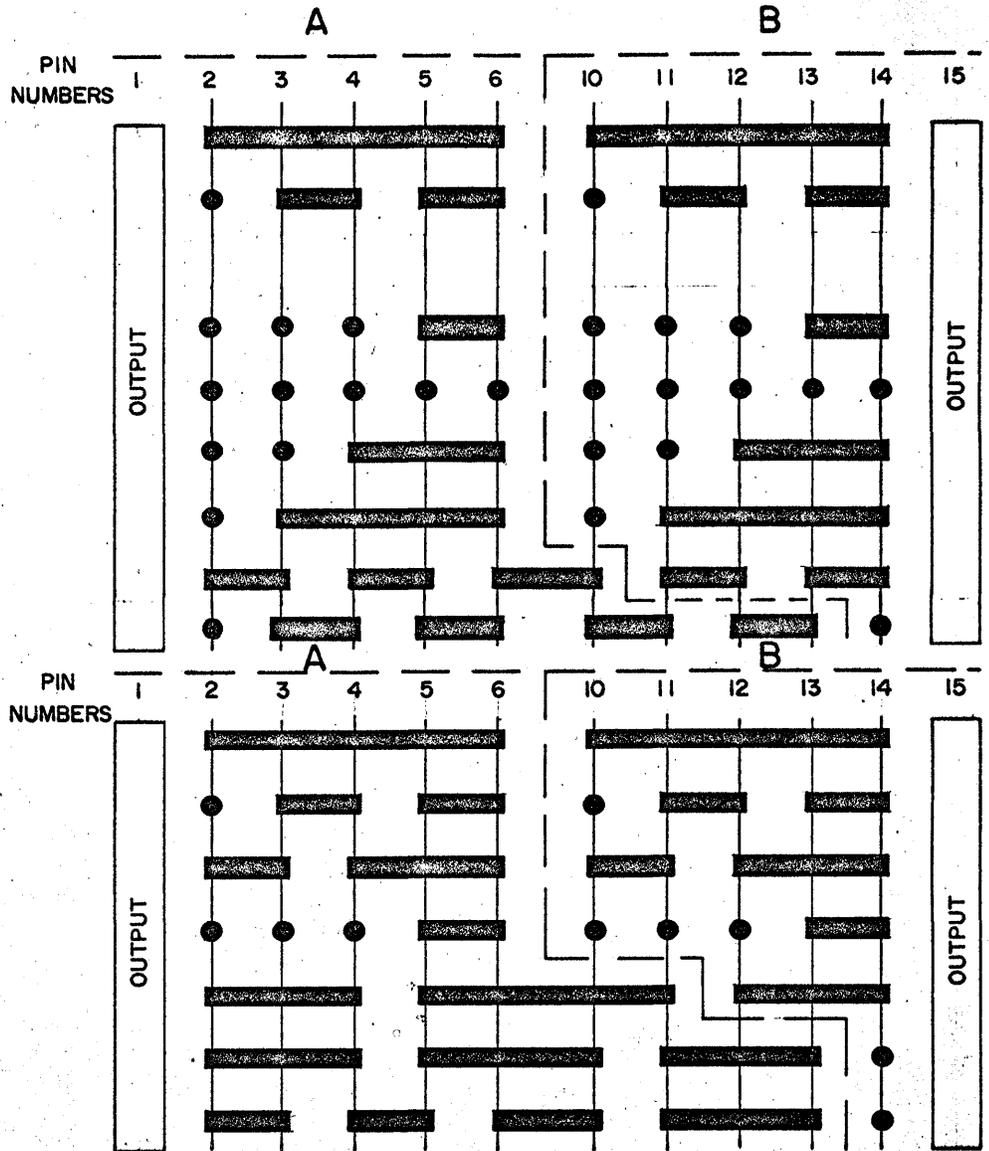
AND ■

Double Inverter

- C21 5-A&B
- C22 122-A&B
- C24 1112-A&B
- C25 11111-A&B
- C26 113-A&B
- C27 14-A&B
- C28 222-A, 22-B
- C29 12222-A, 1-B

Flip-Flop

- C31 5-A&B
- C32 122-A&B
- C33 23-A&B
- C34 1112-A&B
- C35 34-A, 3-B
- C36 333-A, 1-B
- C37 2223-A, 1-B



NOTE:

- PIN 7, + 20v
- PIN 8, GND
- PIN 9, - 20v

Figure 2. Double Inverter and Flip-Flop

INPUT SYMBOLS

OR  (a single-way AND on Control Delay Cards)

AND 

Control Delay

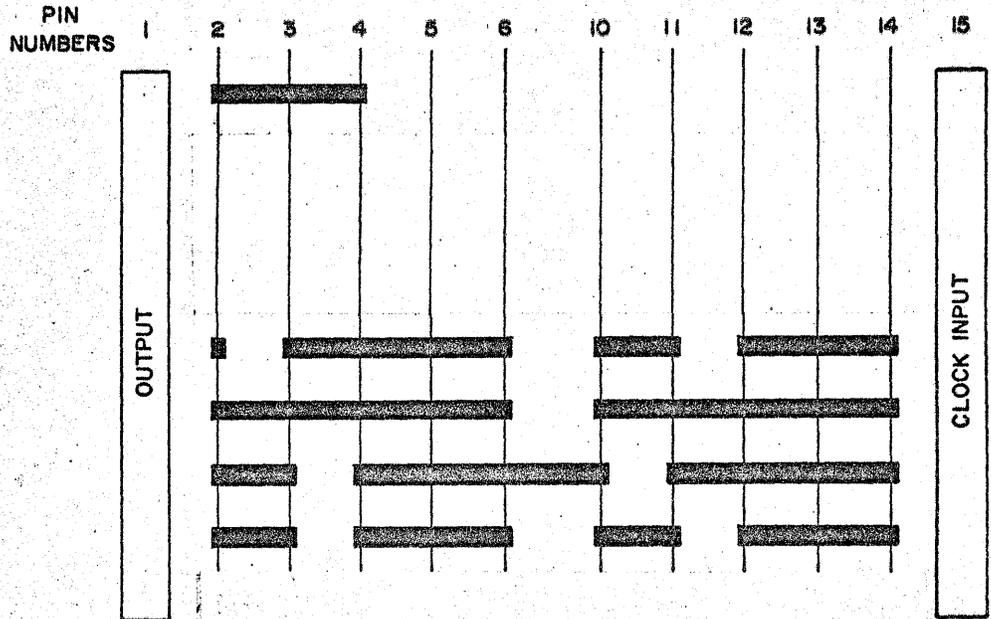
C40 3

C44 1423

C46 55

C47 244

C48 2323



NOTE:

- PIN 7, + 20v
- PIN 8, GND
- PIN 9, - 20v

Figure 3. Control Delay

CHAPTER 3

CIRCUIT DESCRIPTIONS

The following pages contain descriptions and schematic diagrams of type "C" printed circuit cards developed for the 3600 system. These prototype cards are designated by a two-digit number preceded by the letter C; for example, C65.

The following descriptions are presented in numerical order.

ODD PLANE
INHIBIT GENERATOR
Card Type C00

FUNCTION

The function of the circuits on this card is to allow a 340 ma inhibit current to flow from the +40v source at pin 6 to the inhibit winding at pin 1 or pin 15. This occurs whenever all inputs to the respective circuit are at the logical "1" level of -5.8v. The inhibit circuit contains a series 120-ohm resistor so that the resulting current is approximately 340 ma.

OPERATION

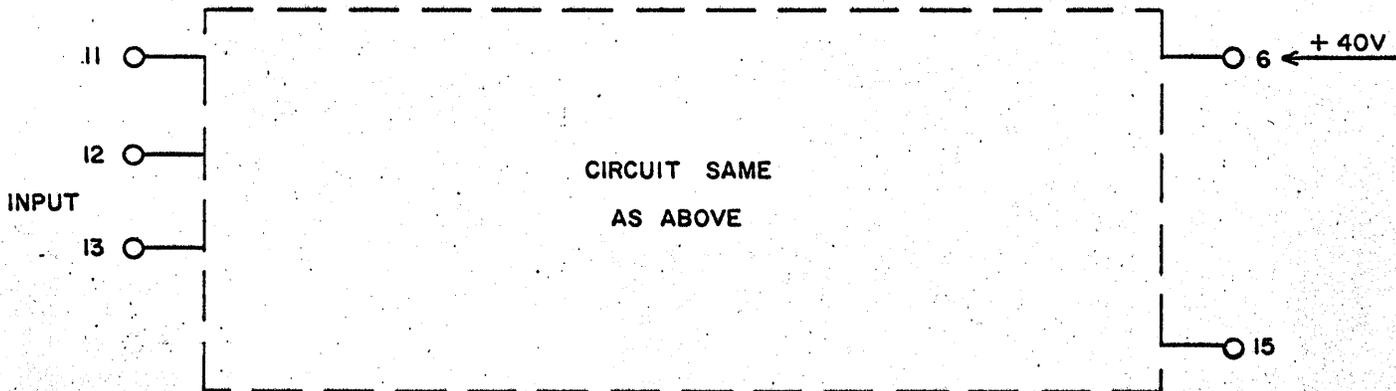
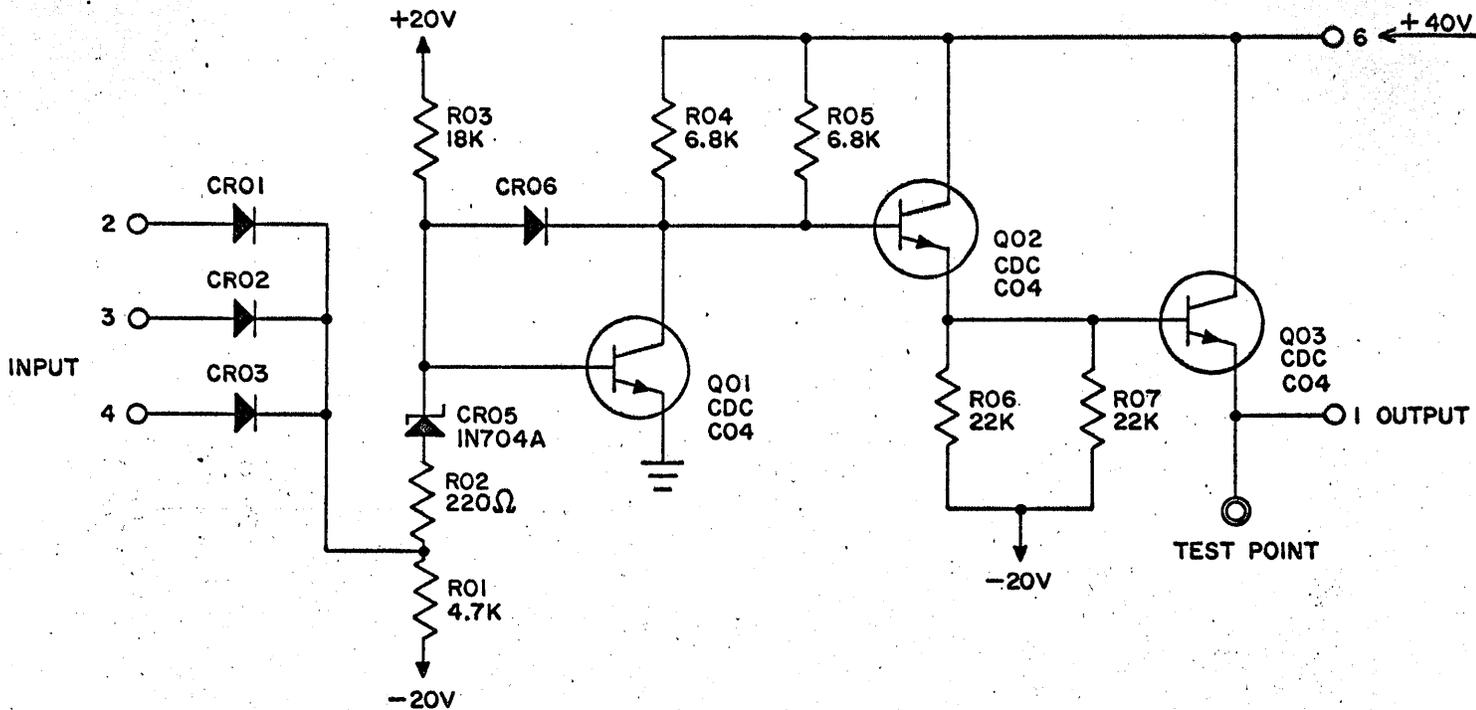
Each circuit has a three-way logical AND input, meaning that all inputs must be at the -5.8v "1" level in order for an input to be sensed. A -1.1v "0" signal on any input will disable the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

A level-shifting action is provided to the base of Q01 by resistors R01, R02, R03, and the 4.1v zener diode CR05. The zener diode CR05 is reverse-biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

When a -1.1v "0" signal appears at an input, the zener diode CR05 places a forward bias on the base of Q01. Transistor Q01 then switches to a state of heavy conduction. It is held out of saturation by the feedback diode CR06 and its collector voltage is approximately +0.4v. The low collector voltage of Q01 is also the base voltage of Q02, which is connected as an emitter follower. The emitter voltage of Q02 is equal to its +0.4v base voltage minus its base-emitter junction drop, and is approximately -0.3v. This provides sufficient forward bias so that a minimum conduction is maintained through Q02. Transistor Q03 is connected as an emitter follower with the inhibit winding load in series with the emitter. The emitter of Q03 is connected to ground through

INHIBIT GENERATOR

CARD TYPE COO



NOTES:

1. EACH CIRCUIT HAS THREE "AND" INPUTS.
2. TRANSISTORS Q02 & Q03 CONDUCT WHEN ALL INPUTS ARE $-5.8V$ "1".
3. ALL DIODES ARE HD2969 UNLESS OTHERWISE INDICATED.

ODD PLANE

the inhibit line. The base-emitter junction is therefore reverse-biased by the -0.3v input, so that Q03 is cut off. This disables the current path from the +40v supply to the inhibit winding.

With the AND input satisfied by -5.8v "1" signals, the base of Q01 is biased at approximately -1.5v and Q01 is cut off. The collector voltage of Q01 rises to approximately +38.5v (40v minus the IR drop across R03 and R04). This provides drive to the base-emitter junction of Q02. Transistor Q02 is connected as an emitter follower; thus its emitter voltage becomes approximately +38v. This provides a strong forward bias to the base of Q03, causing Q03 to conduct heavily. The voltage applied to the inhibit line is the emitter voltage of Q03 and is approximately +37.5v. The 340 ma inhibit current is also the emitter current of Q03, and is allowed to flow when Q03 switches to the conduction state.

CLOCK OSCILLATOR-AMPLIFIER

Card Type C01

General

The clock oscillator-amplifier shown in figure 1 is essentially a tank circuit which may be tuned through a small range around 8 megacycles, with drive provided to the tank by two transistor amplifiers. The transistors are connected in a push-pull configuration, with the two circuit inputs directly connected to their bases. When the transistor inputs are provided with cross-coupled feedback from the oscillator transformer secondary, a continuous self-oscillation is maintained.

The circuit is designed so that, if external drive is provided to the inputs, the two transistors will operate as sine wave amplifiers, providing a two-phase output at the tank frequency.

Pyramid Connection

The computer timing configuration for which this circuit is designed is an oscillator-amplifier pyramid, as shown in figure 2. The master oscillator is a clock circuit connected as a feedback oscillator. To avoid undue loading effects, the master oscillator is permitted to drive only 2 amplifiers.

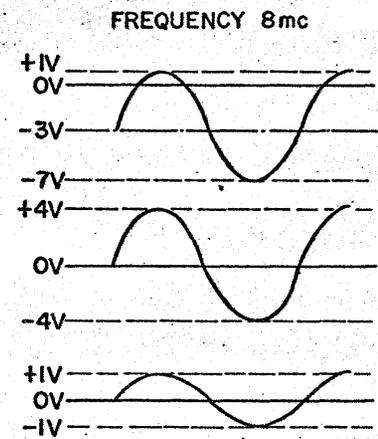
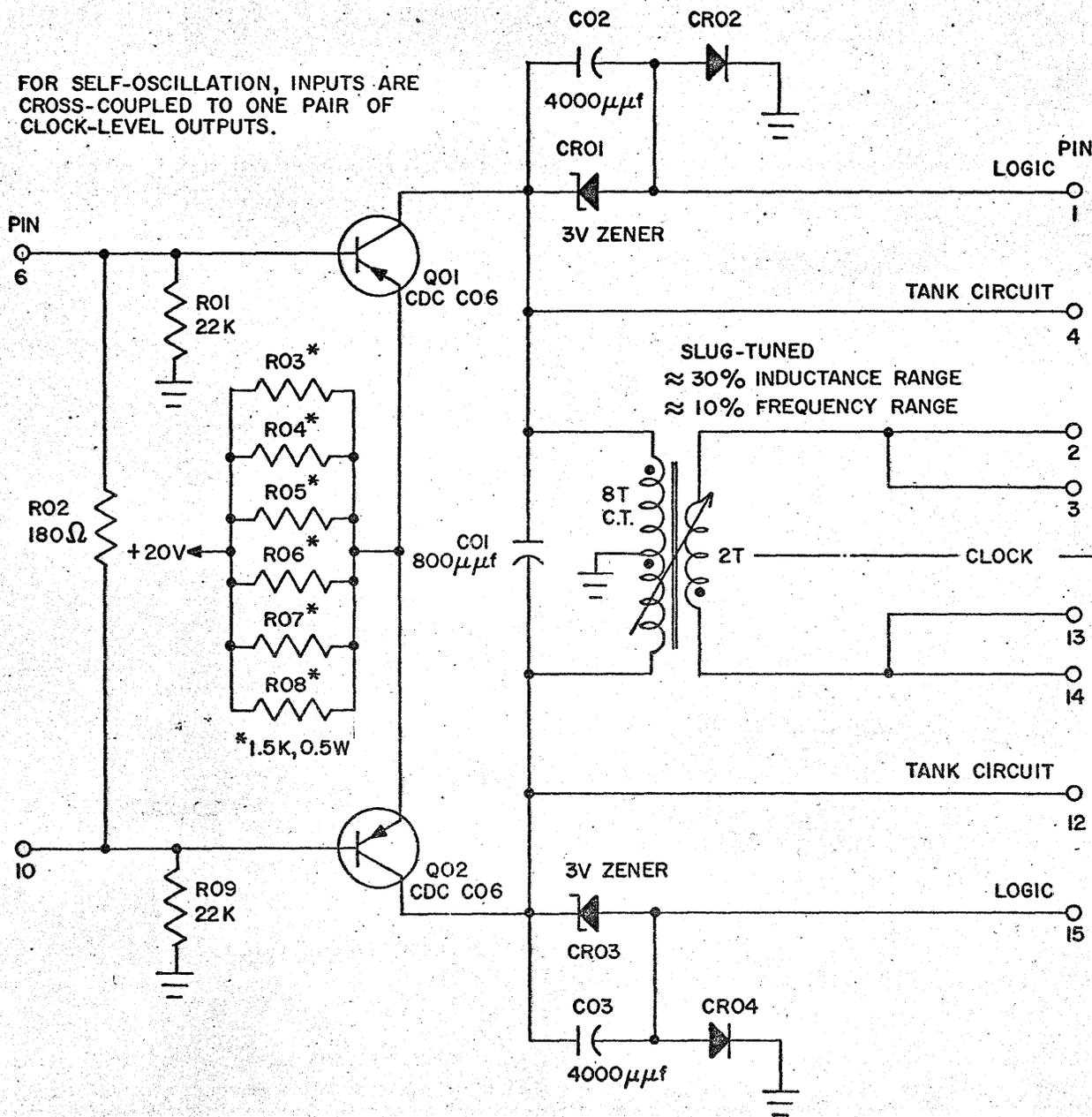
The ranks of amplifiers are clock circuits which receive external inputs and function as push-pull sine wave amplifiers. Each amplifier is capable of driving 4 others; thus, the pyramid effect is produced. Each amplifier in a rank must be in phase with every other amplifier in that same rank, although it is not necessary for the ranks to be in phase with each other or with the master oscillator. Outputs to the logic are taken only from the final rank of amplifiers.

Circuit Operation

The driving transistors Q01 and Q02 are CDC C06's and are connected in a push-pull configuration. Only one transistor would be necessary to sustain oscillation; however, two transistors greatly increase the ability of the circuit to drive an unsymmetrical load.

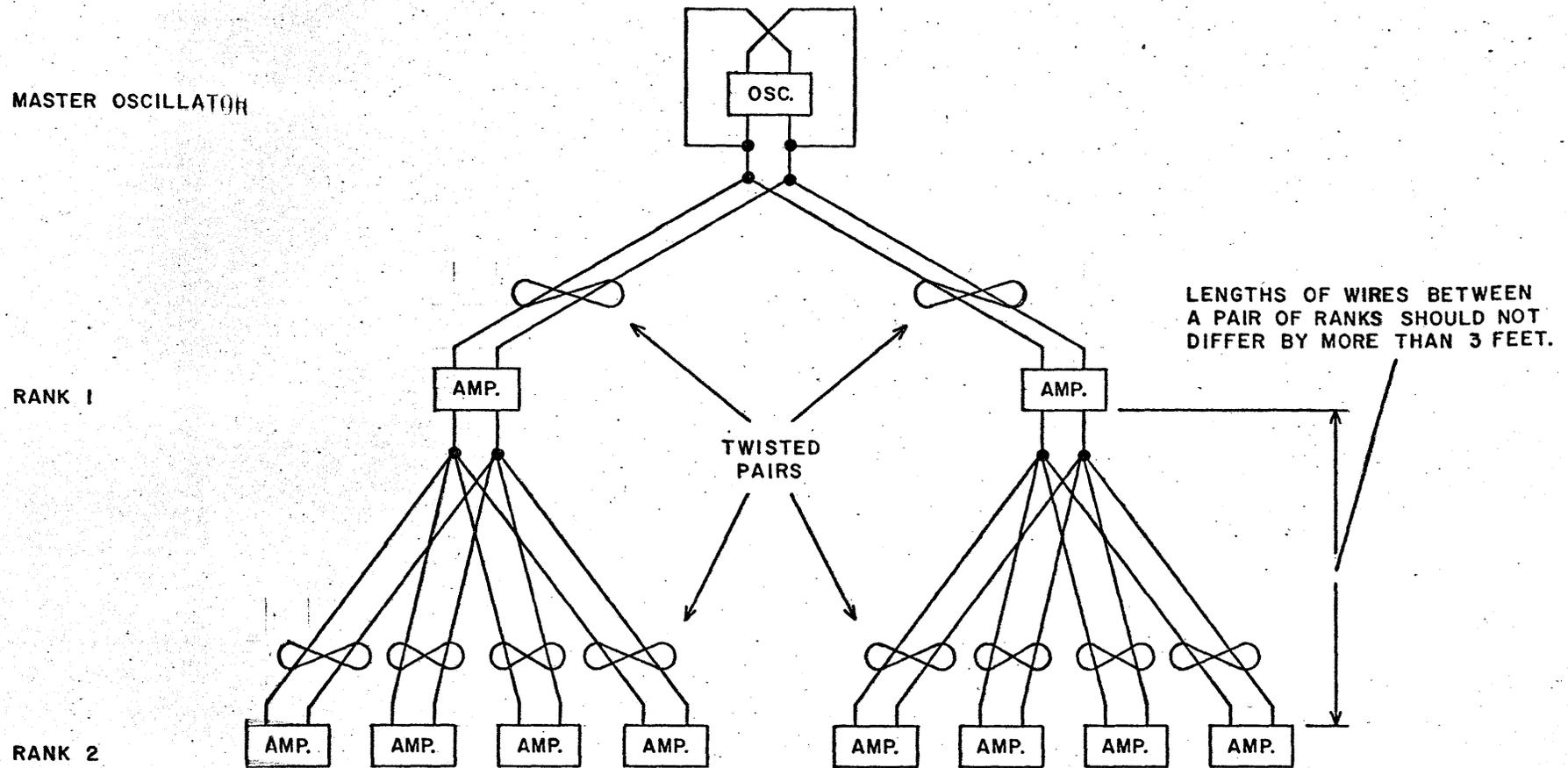
CLOCK OSCILLATOR - AMPLIFIER

FOR SELF-OSCILLATION, INPUTS ARE CROSS-COUPLED TO ONE PAIR OF CLOCK-LEVEL OUTPUTS.



LEVELS AND WAVE FORMS SAME AS ABOVE, EXCEPT 180° PHASE SHIFT.

CLOCK PYRAMID



3-7

RANK 2
(RANK 3, 32 AMPLIFIERS)
(RANK 4, 128 AMPLIFIERS)

NOTE 1

1. MASTER OSCILLATOR MAY DRIVE 2 AMPLIFIERS.
2. EACH AMPLIFIER MAY DRIVE 4 FOLLOWING AMPLIFIERS.
3. ALL AMPLIFIERS IN THE SAME RANK ARE IN PHASE WITH EACH OTHER, BUT NOT NECESSARILY IN PHASE WITH ANY OTHER RANK OR WITH THE MASTER OSCILLATOR.

Clock amplifier logic outputs are restricted to driving AND loads, only. By means of jumpered connections, an amplifier may drive up to 10 loads. Ideally, this would be distributed with 5 loads on each output phase; however, the loading may be unbalanced to 8 and 2, if necessary.

The characteristics of transistors Q01 and Q02 are presented in the component section of this report; however, these transistors have a power handling capability of 150 mw at 25° C ambient. The average transistor dissipation in an oscillator circuit is of the order of 60 mw.

An 800 μmf silver-mica capacitor C01 having a low temperature coefficient and good stability with life is used in the tank circuit to resonate with the transformer inductance at a center frequency of 8 megacycles. The transformer inductance may be tuned through a range of approximately 30% by means of a low permeability ferrite slug. This has the effect of shifting the tank frequency through a range of approximately 10%.

The peak-to-peak signal developed across the tank is restricted to approximately 8v by the clamp diodes CR01 and CR04. The printed circuit card provides outputs at pins 4 and 12 at which this sine wave appears. All of the tanks in a rank of amplifiers may be locked in phase with one another by connecting these outputs in parallel, in case this is ever necessary.

A logic-level signal is a sine wave about -3v, with peaks at +1v and -7v. It is produced by using a zener diode to shift the d-c reference level of the tank output. Logic-level outputs are taken only from the last rank of the clock pyramid, and are available at pins 1 and 15.

The circuit in figure 1 provides a clock-level output at pins 2, 3, 13, and 14, which is taken from the secondary of the tank transformer. The secondary winding consists of 2 turns, while the primary winding is 8 turns, center-tapped; therefore the clock-level output is a sine wave about ground with a peak-to-peak amplitude of approximately 2v.

The clock-level signals are used as drive signals throughout the clock pyramid, as shown in figure 2. All wires used to transmit clock-level signals must be twisted pair, and the distance over which the signal is transmitted should be less than 15 feet. In addition, there should be less than a 3 foot variation in the lengths of wires used to transmit drive signals between a given pair of ranks.

Ground Rules

A. Clock-level outputs.

1. The oscillator may drive 2 amplifiers, in addition to providing its own feedback.
2. Each amplifier may drive 4 other amplifiers.
3. Interconnecting wires between ranks of amplifiers and from the master oscillator to rank 1 must be twisted pair.
4. Signals may be transmitted up to 15 feet.
5. There should be no more than a 3-foot difference in the lengths of interconnecting wires between a given pair of ranks.

B. Tank circuit output.

1. This is used only to phase-lock the tanks within a single rank of amplifiers, if necessary.

C. Logic-level outputs.

1. Clock outputs must always connect to logic card AND inputs.
2. A maximum of 10 loads may be driven.
3. A maximum of 8 loads may be driven by any single output; with 8 loads on one output, the opposite-phase output of that amplifier may drive only 2 loads, so that the total number does not exceed 10.

Procedure for Tuning a Clock Pyramid

A scope equipped with a differential or dual-trace preamplifier, such as a Tektronix type CA, may be used for tuning the pyramid. The probe leads should be of equal length and must be grounded at the cards. The scope should be externally synchronized during step 3, and it is convenient to use the master oscillator for this.

Step 1.

Adjust the transformer of the master oscillator to the correct computer frequency. This may be done by setting the horizontal sweep at $0.1 \mu\text{sec/cm}$ and adjusting until 8 peaks are seen across the 10 cm scope grid, if the desired frequency is 8 megacycles.

Step 2.

With the scope on a sensitive range, adjust one of the amplifiers in Rank 1 for maximum amplitude.

Step 3.

Using external sync, adjust the remaining amplifiers in Rank 1 to be in phase with the reference amplifier tuned in step 2. With a differential preamplifier, this may be done by inverting one signal and adding algebraically, and adjusting for minimum deflection with the scope on a sensitive range.

Other ranks are tuned according to steps 2 and 3.

CLAMP
Card Type C02

This circuit provides a clamp for logic circuit connecting lines, so that ringing will be minimized. If sufficient energy is removed from the first overshoot, the remainder of the ringing will have an amplitude less than the logic circuit threshold. A schematic of the clamp circuit is presented in figure 1, with typical waveforms showing its effect on a line having excessive ringing.

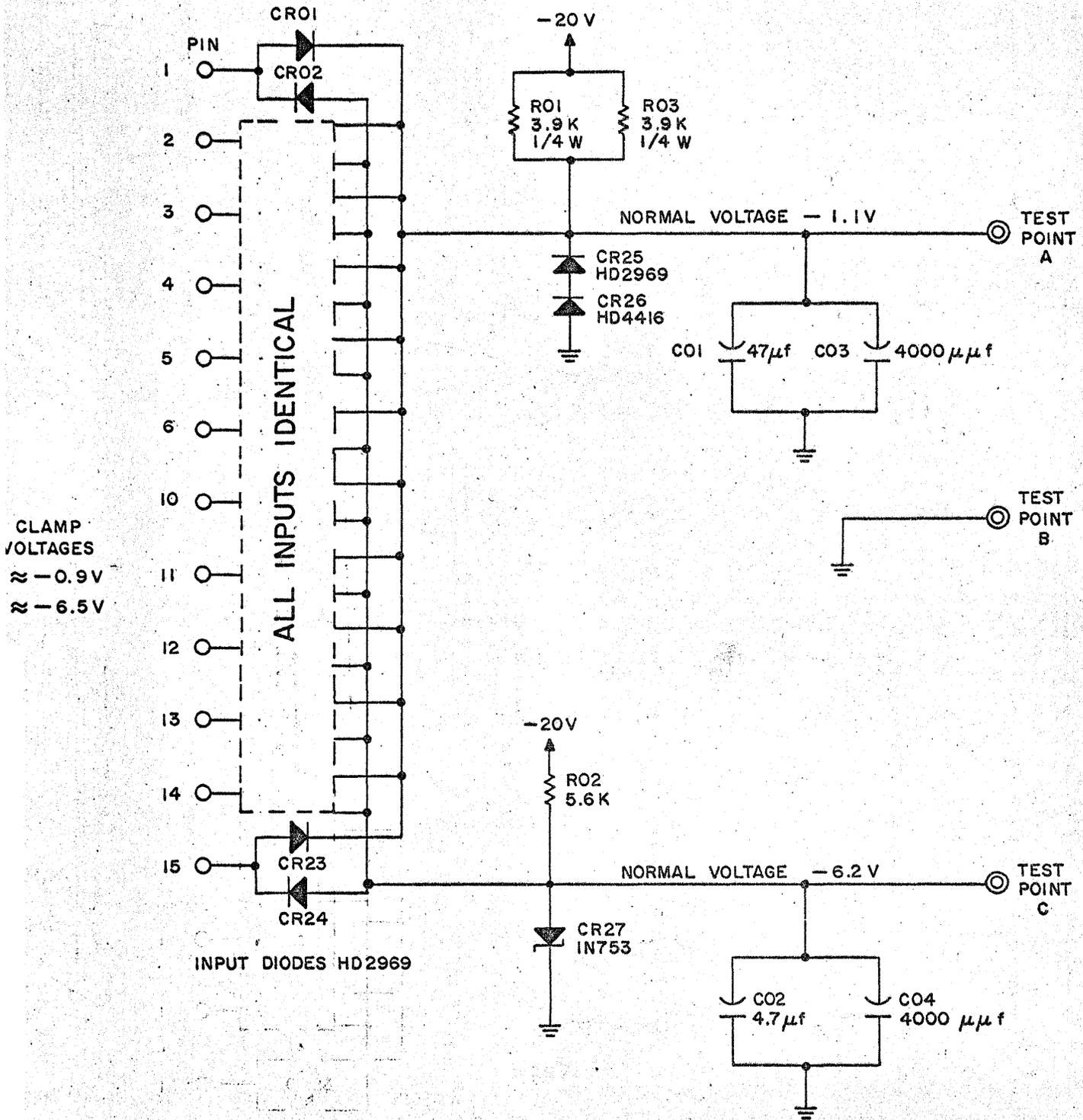
The clamp voltage in the positive direction is the sum of the forward drops across diodes CR25 and CR26, less the drop across the input diodes, and is approximately -0.9v.

The clamp voltage in the negative direction is the sum of the drop across zener diode CR27 plus the drop across the input diodes, and is approximately -6.5v.

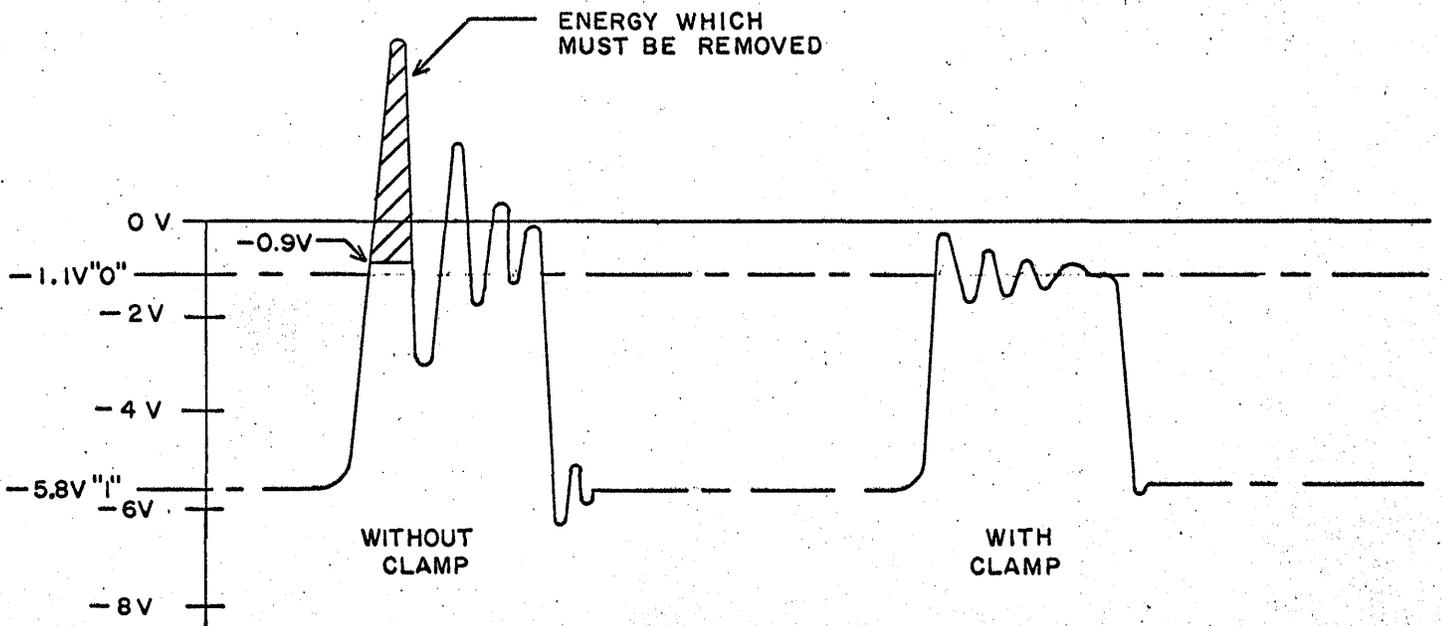
Filtering is provided by capacitors C01, C02, C03, and C04. Due to their large areas, C01 and C02 present an appreciable amount of inductive reactance. It is therefore necessary to include the small capacitors C03 and C04 in order to filter out high-frequency spikes.

CLAMP

CARD TYPE C02



TYPICAL LOGIC LINE VOLTAGE



TRANSFORMER DRIVER

Card Type C03

FUNCTION

The function of the circuits on this card is to enable 450 ma of positive current to flow from the output pins 1 or 15 to ground, whenever all inputs to the respective circuit are at the logical "0" level of -1.1v. Pins 1 and 15 connect to the two ends of the primary windings of eight memory driver transformers. During the memory cycle, one transformer will be center-tapped to +20v; thus current flow in either direction may be obtained by selecting one of the circuits on the C03 card.

The output pins 1 and 15 are connected as shown in figure 1 by capacitor C03 and resistor R06, which form a series differentiating network. This connection will transmit only those signals having a high rate of change, such as a sharp noise spike, and will block entirely a steady d-c voltage. Thus, a noise spike appearing at pin 1 will also appear at pin 15, and their total effect will be to cancel each other. However, the d-c levels of pins 1 and 15 will be completely separated if either circuit switches to the conduction state while the other remains cut off.

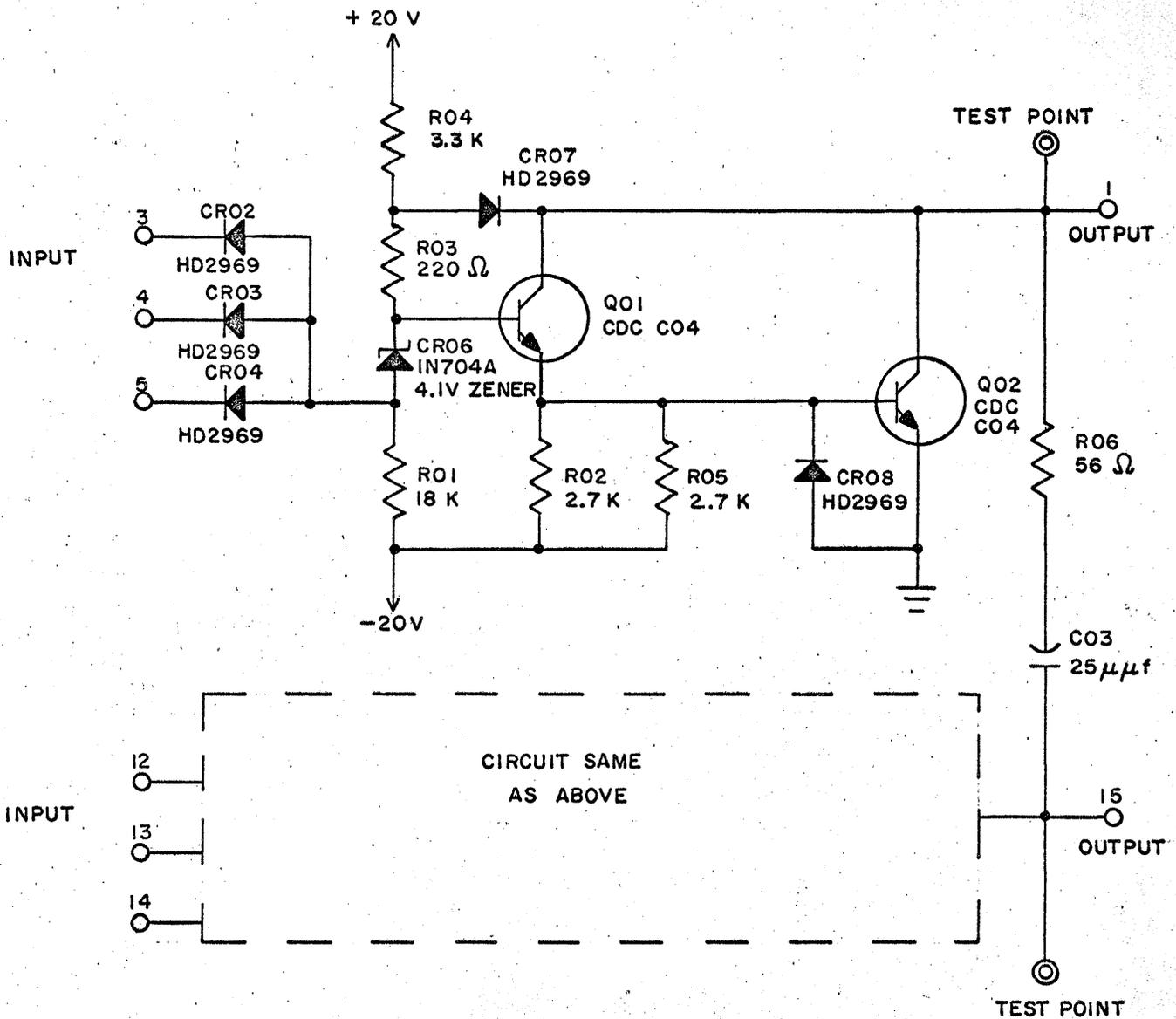
OPERATION

The two circuits on the card are identical and are labeled A and B. The following discussion of operation applies to either circuit, however, the component numbers mentioned are those appearing in circuit A.

A level-shifting action is provided to the base and emitter of Q01 by resistors R01, R03, R04, and the 4.1v zener diode CR06. The zener diode CR06 is reverse-biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

TRANSFORMER DRIVER

CARD TYPE C03



NOTES:

1. EACH CIRCUIT HAS 3 "OR" INPUTS.
2. TRANSISTORS SWITCH TO CONDUCTION STATE WHEN ALL INPUTS ARE -1.1V "0".

Each circuit has three logical OR inputs, meaning that a -5.8v "1" signal on any input will be sensed, although a -1.1v "0" signal may be present simultaneously at another input. Any unused input acts as a steady "0", regardless of whether it is grounded or left open.

When a -5.8v "1" signal appears at an input, the base of Q01 will be biased at about -1v and it will be cut off. The base of Q02 will be held at approximately -0.3v by the forward drop of diode CR08, and Q02 will likewise be cut off. Thus, except for negligible leakage effects, pin 1 is completely isolated from ground and will rise to a high positive voltage. Diode CR07 therefore provides a blocking action, preventing current from flowing through the transformer primary into pin 1.

If all of the circuit inputs are at the -1.1v "0" level, zener diode CR06 holds the base of Q01 at a positive voltage. This forward bias is sufficient so that Q01 conducts heavily, but it is held out of deep saturation by diode CR07 and resistor R03. Transistor Q01 in its conduction state allows the +20v source, which connects to pin 1 through the transformer primary, to bias the base of Q02 at a positive potential. Thus transistor Q02 also conducts heavily, and positive current is allowed to flow from pin 1 to ground with only a drop of approximately 1v across Q02.

Transistor Q02 is a grounded emitter stage driven by the emitter follower stage Q01. The base drive for Q02 is taken directly from the emitter of Q01; thus the input to Q02 follows the input to Q01 and is increased by the gain of Q01. When Q01 switches on, it attempts to bias the base of Q02 well into the positive voltage domain, so that Q02 also switches on and conducts heavily. Likewise, when Q01 switches off, Q02 also switches off, and the voltage drop across diode CR08 applies a reverse bias of approximately 0.3v to the base-emitter junction of Q02 so that it is well into the cut off region.

EVEN PLANE
INHIBIT GENERATOR
Card Type C04

FUNCTION

The function of the circuits on this card is to allow a 340 ma inhibit current to flow from pin 1 or 15 to ground, whenever all inputs to the respective circuit are at the logical "0" level of -1.1v. The inhibit wires are energized by a source of +40v, and each inhibit circuit contains a series 120-ohm resistor so that the resulting current is approximately 340 ma. The even plane inhibit wires terminate at either pin 1 or pin 15 of a C04 card, and the path will be completed to ground allowing current to flow, if the respective inhibit generator circuit switches to its conduction state.

OPERATION

The two circuits contained on the card are identical and are labeled A and B. The following discussion of operation applies to either circuit but the component numbers mentioned are those appearing in circuit A.

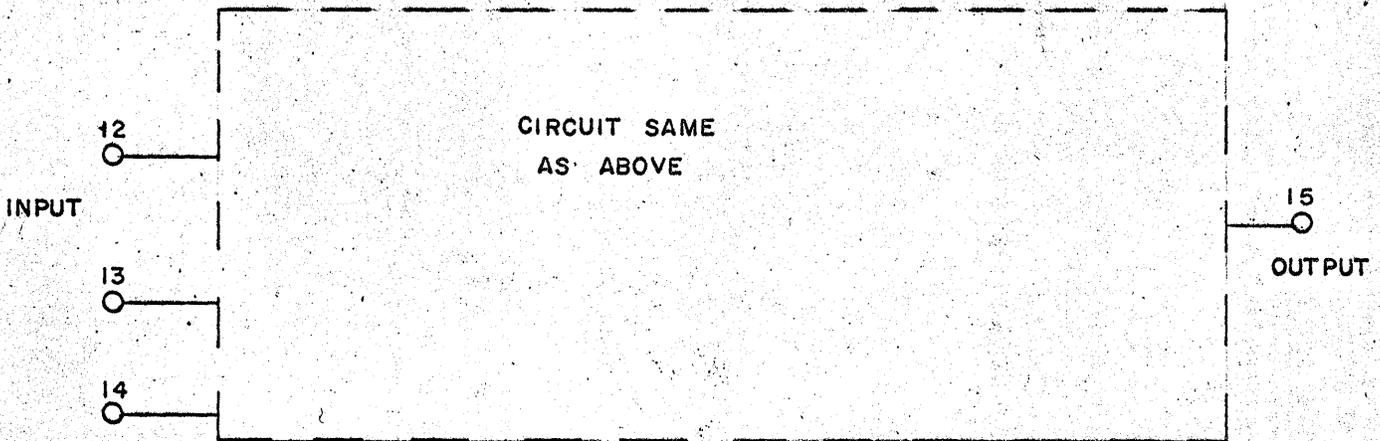
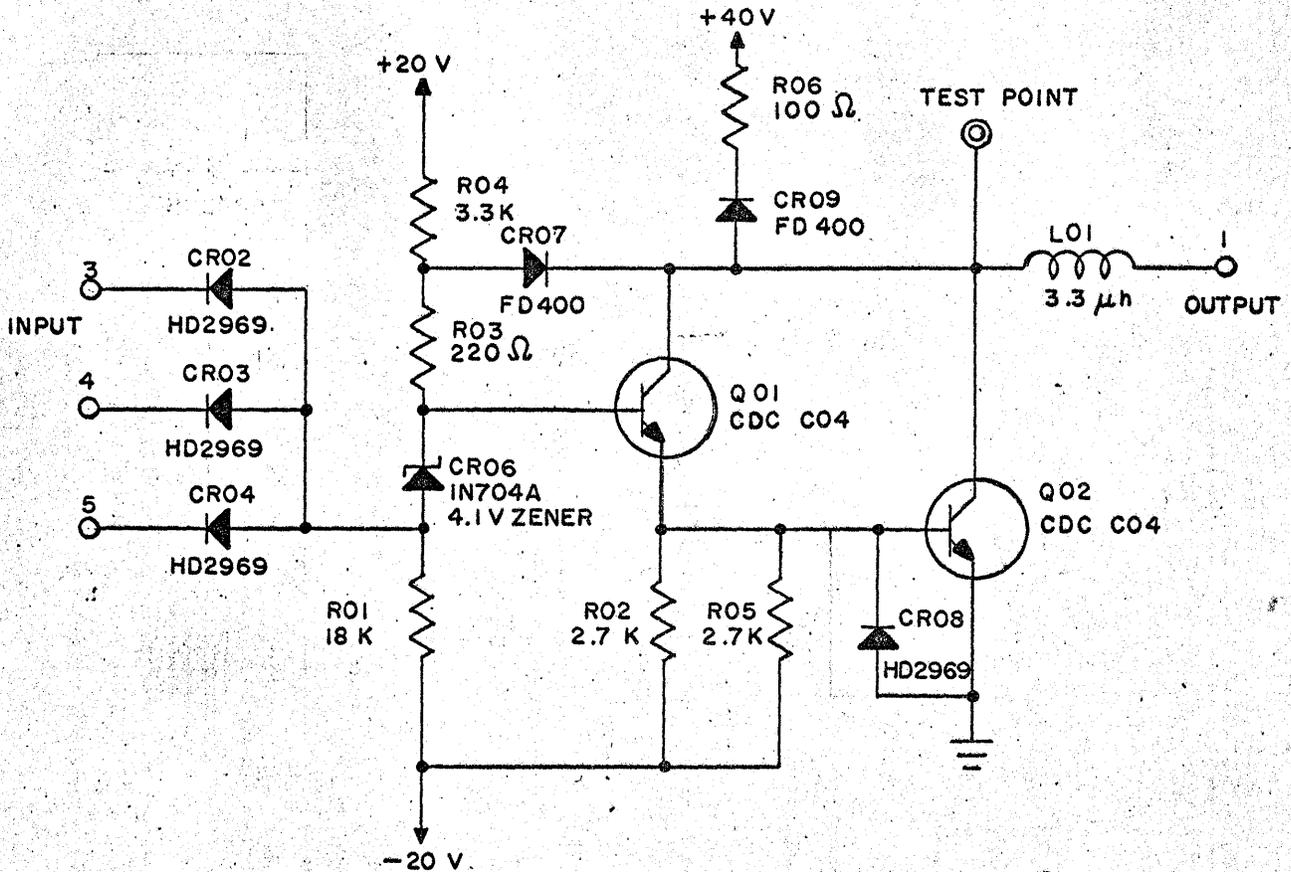
A level-shifting action is provided to the base and emitter of Q01 by resistors R01, R03, R04, and the 4.1v zener diode CR06. The zener diode CR06 is reverse-biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

Each circuit has three logical OR inputs, meaning that a -5.8v "1" signal on any input will be sensed, although a -1.1v "0" signal may be present simultaneously at another input. Any unused input acts as a steady "0", regardless of whether it is grounded or left open.

When a -5.8v "1" signal appears at an input, the base of Q01 is biased at about -1v and Q01 is cut off. The base of Q02 will be held at approximately -0.3v by the forward drop of diode CR08, and Q02 will also be cut off. Thus, except for

INHIBIT GENERATOR

CARD TYPE C04



NOTES:

1. EACH CIRCUIT HAS THREE "OR" INPUTS.
2. A CIRCUIT WILL SWITCH TO ITS CONDUCTION STATE WHEN ALL INPUTS ARE -1.1V "0".

EVEN PLANE.

negligible leakage effects, pin 1 is completely isolated from ground and will rise to a high positive voltage. Diode CR07 therefore provides a blocking action, preventing current from flowing through the inhibit wire into pin 1.

If all of the circuit inputs are at the -1.1v "0" level, zener diode CR06 holds the base of Q01 at a sufficiently positive voltage so that Q01 conducts heavily. In this state, diode CR07 holds Q01 out of saturation. Transistor Q01 in its conduction state allows the +40v source, which connects through the inhibit wire to pin 1, to bias the base of Q02 at a positive level. Thus transistor Q02 also conducts heavily, and positive current is allowed to flow from pin 1 to ground with only a drop of approximately 1v across Q02.

Transistor Q02 is a grounded emitter stage driven by the emitter follower stage Q01. The base drive for Q02 is taken directly from the emitter of Q01; thus the input to Q02 follows the input to Q01 and is increased by the gain of Q01. When Q01 switches on, it attempts to bias the base of Q02 well into the positive voltage domain, so that Q02 also switches on and conducts heavily. Likewise, when Q01 switches off, Q02 also switches off, and the voltage drop across diode CR08 applies a reverse bias of approximately 0.3v to the base-emitter junction of Q02 so that it is well into the cut off region.

The connection of diode CR07, the 100-ohm resistor R06, and the +40v source provides a clamp for the collector voltage of the transistors. When the transistors switch to the non-conducting state, the inductance of the inhibit wire will tend to induce high-voltage transients; however, these inductive transients are clamped at +40v plus the drop across the silicon diode.

The 3.3 microhenry inductor in series with the output pin is for the purpose of reducing ringing on the inhibit wire. The inductor increases the current rise time and hence reduces the overshoot.

GATE

Card Type C05

FUNCTION

The function of the Gate circuit is to enable a current path from a +20v source through which current of the order of 900 ma flows to the primary windings of two memory driver transformers. Pin 4 connects to +20v and pins 1, 2, and 3 provide the output. The path from pin 4 to the output is enabled only when all inputs to the Gate circuit are at the logical "0" level of -1.1v.

The function of the Discharger circuit is to ground the primary windings of the two memory driver transformers which were previously energized. This removes stored charge from the windings and neutralizes the transformers. The Discharger circuit is enabled by a -1.1v "0" input.

OPERATION

Pins 10 through 13 provide four logical OR inputs to the Gate circuit, and pin 6 provides an OR input to the Discharger. An unused input is interpreted as a steady "0", regardless of whether it is grounded or left open.

A level-shifting action for the Gate inputs is performed by resistors R01, R03, R05, and the 4.1v zener diode CR06. The zener diode CR06 is reverse-biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations. Resistors R02, R06, and zener diode CR08 perform the level-shifting action for the Discharger.

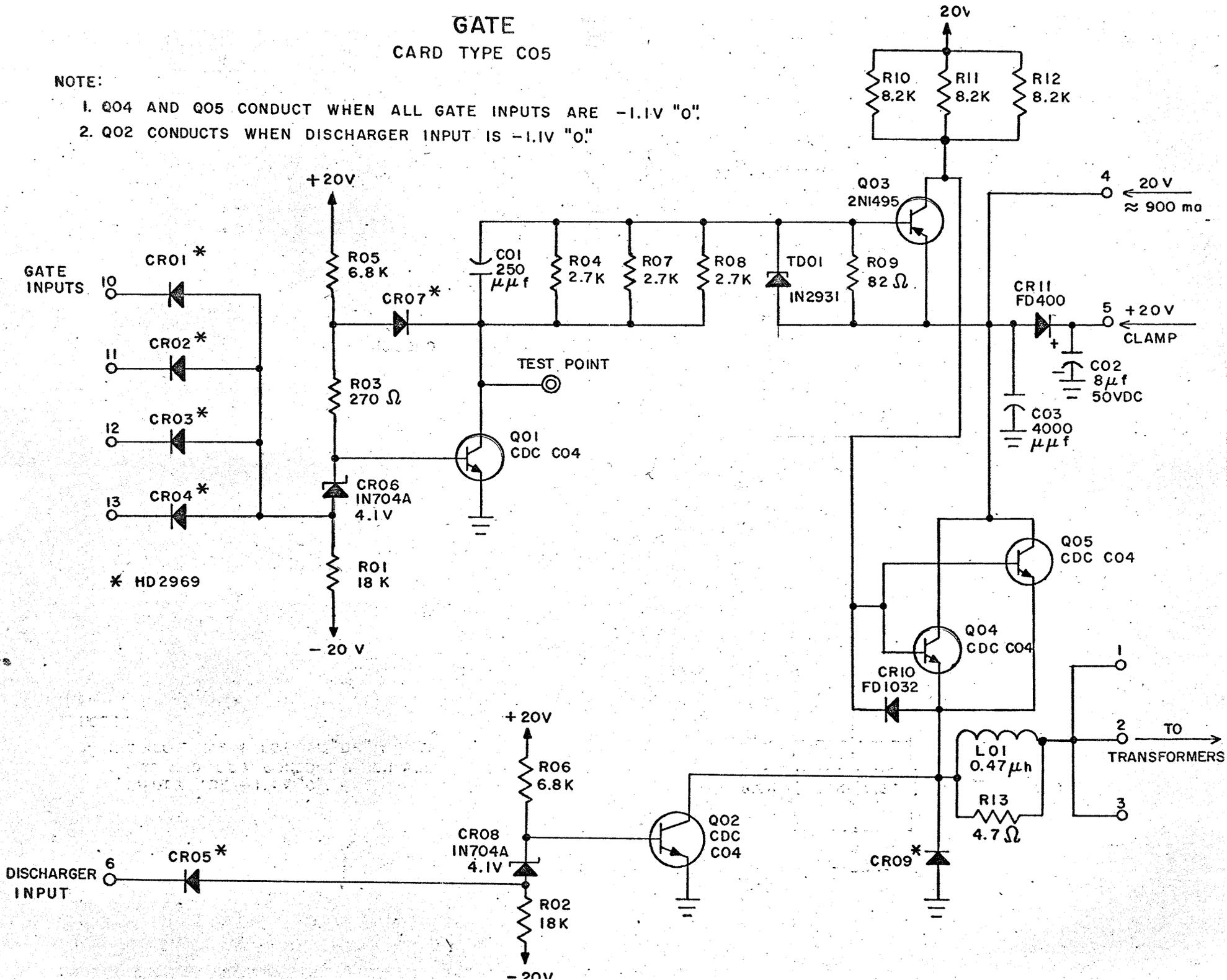
With open circuits or logical "0" signals on all Gate inputs, the base of Q01 will be at a potential of around +0.7v. It is prevented from going further positive by the low forward base-emitter impedance of Q01. During this time, Q01 will be in the conduction state. However, if any input receives a -5.8v "1", the zener diode CR06 will hold the base of Q01 at approximately -1.7v and Q01 will be cut off.

GATE

CARD TYPE C05

NOTE:

1. Q04 AND Q05 CONDUCT WHEN ALL GATE INPUTS ARE -1.1V "0".
2. Q02 CONDUCTS WHEN DISCHARGER INPUT IS -1.1V "0".



During the time that Q01 is cut off by a "1" signal, its collector potential will be raised to a high positive value by the +20v source attached to pin 4. Since no appreciable current now flows through the 82-ohm resistor and tunnel diode between base and emitter of Q03, it is also essentially cut off.

When Q01 switches to its conducting state, current is allowed to flow from the +20v source at pin 4 through the tunnel diode and 82-ohm resistor between emitter and base of Q03, through the three parallel 2.7k resistors, and through Q01 to ground. A threshold level is provided by the tunnel diode, since in its low-voltage state, it does not allow Q03 to conduct. However, when current through the tunnel diode increases to 10 ma, it switches to its high-voltage state. This places approximately 0.8v forward potential on the base of Q03 causing it to switch to its conduction state. This enables the series circuit from +20v at pin 4 through Q03 and through the three parallel 2.7k resistors to -20v. The base drive for Q04 and Q05 is taken from the collector of Q03, and when Q03 conducts, turn-on current is provided for Q04 and Q05 so that they switch to the conduction state. Thus the circuit is completed, allowing positive current to flow from pin 4 to the output. When Q03 switches off, the voltage drop across diode CR10 applies a reverse bias of approximately 0.6v to the base-emitter junctions of Q04 and Q05, cutting them off.

Transistors Q04 and Q05 control a current of the order of 900 ma flowing in a highly inductive load. Diode CR09 is therefore provided so that when Q04 and Q05 interrupt the current, the induced high-voltage transient will be dissipated harmlessly.

Diode CR11 acts as a clamp against positive voltage surges at the collectors of Q04 and Q05 when current is interrupted. Pin 5 connects to a separate +20v buss and prevents pin 4 from becoming more positive than +20.6v, taking into account the 0.6v drop across the silicon diode.

Capacitors C02 and C03 provide a smoothing filter for spikes and ripple in the +20v sources at pins 4 and 5. The 8 microfarad capacitor C02 is sufficient for ripple and low frequency fluctuations; however, it exhibits a certain amount of

inductive reactance due to its large area. For this reason, it is necessary to include C03 which has negligible inductive reactance and is therefore effective in filtering high frequency spikes.

The Discharger circuit is enabled by a -1.1v "0" input on pin 6. This causes zener diode CR08 to apply sufficient forward bias to the base of Q02 so that Q02 switches to its maximum conduction state. Transistor Q02 thus provides a low impedance path to ground for any stored charge remaining in the primary windings of the two memory driver transformers.

SENSE AMPLIFIER

Card Type C06

This card amplifies and detects the pulses induced in a sense winding when a magnetic memory core switches polarity. The two ends of the sense winding are connected to pins 4 and 5, and when a core switches its magnetic state, the circuit produces a logical "0" output on pin 15.

The circuit may be conveniently divided into two sections: a differential voltage amplifier having a gain of approximately 100, and a discriminator having an output of approximately -13.6v representing a logical "1" which changes to a logical "0" when a memory core switches its magnetic state. The following logic card will interpret any signal more positive than -3v as being a logical "0", however the discriminator output approaches -1.6v when a core switches.

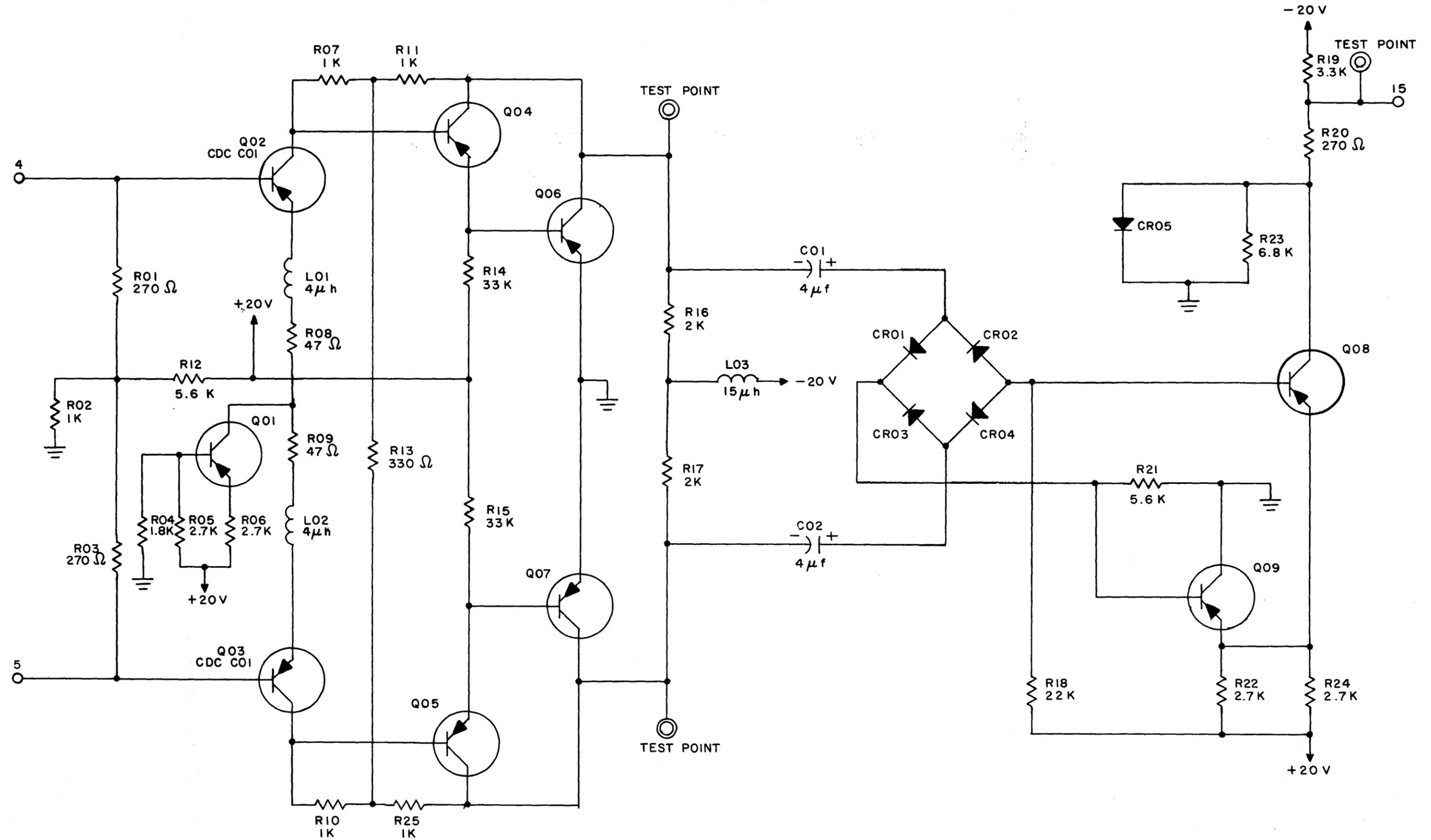
AMPLIFIER

The differential voltage amplifier is the symmetrical portion of the circuit to the left of the diode bridge, as shown in the accompanying diagram. Input signals from the sense winding are received on pins 4 and 5. The ends of the sense winding are connected to these two pins, forming a series loop which threads all of the memory cores in a plane quadrant. The only ground reference to this loop is through the 1000-ohm resistor R02, thus the nominal 30 mv potential induced in the sense winding by the switching of a core is applied equally and oppositely to both input pins. This is amplified into a 3v signal which appears across the diode bridge.

The amplifier circuit is sensitive only to the difference in potential between pins 4 and 5, which is produced by the application of a double-ended signal from the sense winding. A simultaneous shift of the d-c reference level of both input pins produces only a negligible effect. It is possible for both inputs to fluctuate simultaneously by as much as 2v without producing more than 0.2v fluctuation at the diode bridge.

SENSE AMPLIFIER

CARD TYPE C06



NOTE:

1. ALL DIODES FD 1032.
2. ALL TRANSISTORS CDC C02, UNLESS OTHERWISE INDICATED.

The degree of sensitivity exhibited by a differential amplifier to potential differences between its inputs as opposed to simultaneous shifts of both inputs in the common mode is often represented by a number called the "common mode rejection ratio", which figure for this circuit is of the order of 40,000.

Resistors R01 and R03 are connected in series across the two inputs, as shown. This relatively low resistance is in parallel with the input impedance of the amplifier, so that the total terminating impedance across the sense line is reduced. This has the effect of making the amplifier less sensitive to noise induced by the flow of inhibit current.

The 4 uh inductors in the emitter circuits of Q02 and Q03 determine the high frequency roll-off of the amplifier. This inductance reduces the gain at high frequencies, and prevents the amplifier from responding to noise spikes.

The signals produced by the memory cores are received and amplified in the double-ended fashion. As an example of operation, assume that the 30 mv potential from the memory core is of a direction such that pin 4 shifts negative 15 mv and pin 5 shifts positive 15 mv from the rest state. These potentials are applied to the bases of Q02 and Q03, causing Q02 to conduct more heavily while conduction through Q03 decreases. This action is further regulated by the constant-current source through Q01, so that an emitter current increase in Q02 must be accompanied by a corresponding decrease in Q03.

The results of the preceding action are such that the collector of Q02 becomes more positive and the collector of Q03 becomes more negative. This, in turn, causes transistors Q04 and Q06 to conduct less heavily while conduction through Q05 and Q07 increases. The collectors of Q04 and Q06 therefore shift approximately 1.5v in the negative direction and the collectors of Q05 and Q07 shift a similar amount in the positive direction, so that a potential difference of 3v exists across the diode bridge.

The signals from the collectors of Q02 and Q03 are amplified by a factor of 100 by Q04 and Q06, and by Q05 and Q07, respectively, which are connected as an emitter follower and a grounded emitter amplifier. Depending upon their particular characteristics, the two transistors are capable of providing a maximum

available gain of the order of 1000. To insure stable operation, this is reduced to around 30 by the negative feedback connection of the two 1000-ohm resistors from collector to base. A portion of this negative feedback, however, is nullified by the 330-ohm resistor connected between the two feedback lines, so that the over-all voltage gain of each of the stages is approximately 100.

DISCRIMINATOR

The discriminator is the portion of the circuit to the right of the diode bridge, whose function is to provide outputs at voltage levels suitable for use by logic circuits. The output of the discriminator is taken from pin 15, and is at approximately -13.6v during the rest state. However, when a voltage appears across the diode bridge, the output at pin 15 approaches -1.6v which is interpreted as a logical "0".

The diodes used in the bridge are high speed silicon devices having a forward voltage drop of the order of 0.6v. Therefore, during the rest state a voltage-dividing action is provided from +20v to ground through the 22,000-ohm resistor R18, the diode bridge, and the 5600-ohm resistor R21. Due to the forward drop of the diodes, the base of Q08 is held at around 1.2v higher positive potential than the base of Q09. Transistor Q09 thus conducts quite heavily while Q08 conducts very little. Under these conditions the output at pin 15 is around -13.6v, due to the voltage dividing action of R19, R20, and R23. Transistor Q09 provides a low impedance path to ground, so that the emitter of Q08 cannot rise to a high positive potential when it is in a state of low conduction.

The diode bridge rectifies the potential across it, so that an input of either polarity results in a negative input to the base of Q08 and a positive input to the base of Q09. This has the effect of causing Q08 to conduct heavily while Q09, in turn, conducts very little. Transistor Q08 thus enables a low impedance path from +20v to ground through diode CR05, which is a silicon diode having a forward drop of approximately 0.6v. The anode of CR05 is therefore at approximately +0.6v, so that pin 15 is biased at approximately -1.6v by resistors R20, R19, and the +20v source. This output voltage level is interpreted as a logical "0".

EMITTER FOLLOWER

Card Type C07

FUNCTION

The function of this circuit is to convert inputs received from a terminated 200-ohm delay line into outputs suitable for driving a logic card load. This circuit is designed to provide a high impedance load for the delay line, avoiding excessive current drain which will affect its operating characteristics.

OPERATION

The delay line is driven by the circuit contained on card type C08; thus its input signal levels are approximately -0.3v and -10v. However, due to integrating characteristics and attenuation, the peak voltage levels tend to diminish slightly as the signal travels down the delay line. The input signal levels of the emitter follower circuit are therefore of the order of -0.3v and -10v, depending upon the point of the delay line from which the signal is taken.

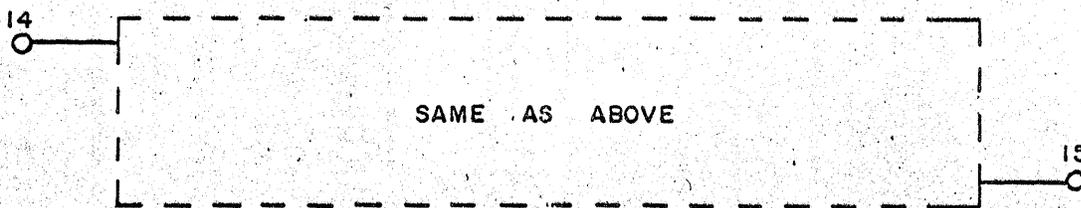
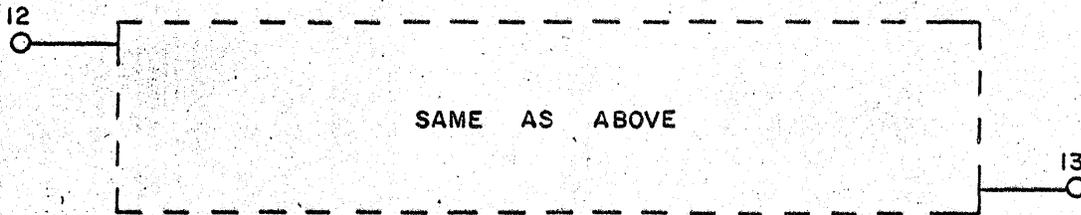
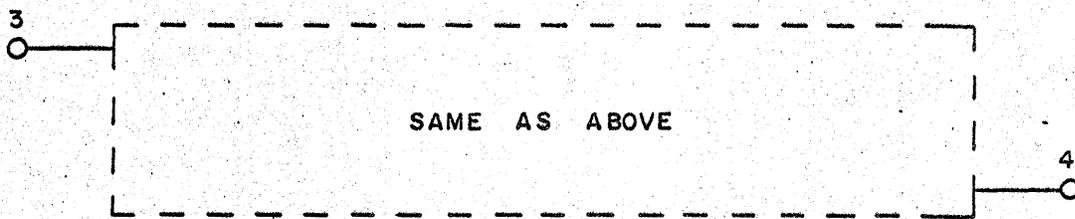
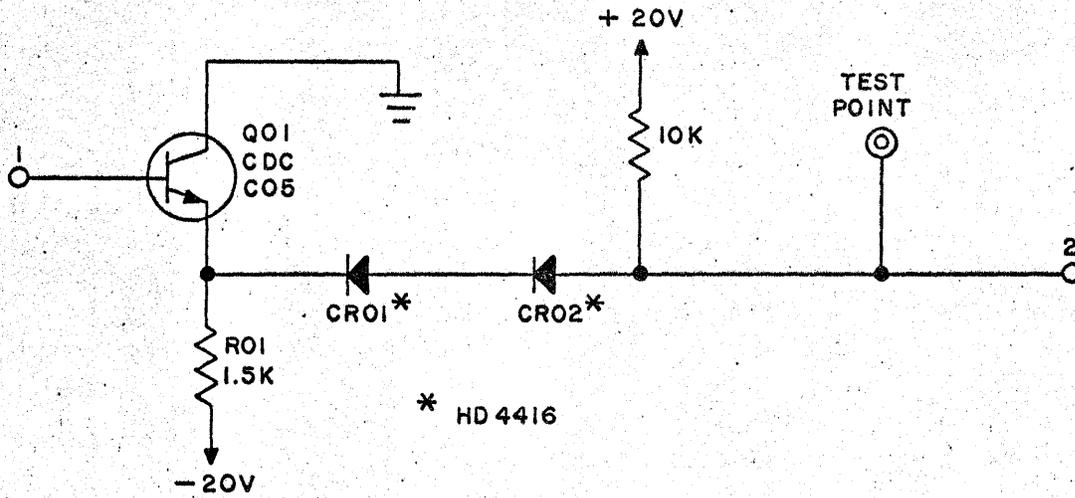
A -0.3v input results in an output near ground which is interpreted as a logical "0". A -10v input results in an output of approximately -9.3v which is interpreted as a logical "1".

Transistor Q01 is an NPN silicon type CDC C05. It is connected as an emitter follower; thus its emitter voltage is always approximately 0.7v more negative than the circuit input.

CR01 and CR02 are silicon diodes having a forward voltage drop of approximately 0.7v. The series connection of these two diodes holds the circuit output 1.4v more positive than the emitter of Q01.

EMITTER FOLLOWER

CARD TYPE C07



DELAY LINE DRIVER

Card Type C08

FUNCTION

The function of this circuit is to provide an output suitable for driving a terminated 200-ohm delay line. With a 200-ohm load at pin 1 and the circuit in its quiescent state, the output voltage level is approximately -10v. Upon receipt of a -5.8v "1" input, both transistors switch to a state of heavy conduction and the output voltage becomes approximately -0.3v.

OPERATION

The circuit has 5 logical OR inputs; thus a -5.8v "1" on any input will activate the circuit. An unused input is effectively a steady "0", regardless of whether it is grounded or left open.

An input level-shifting action is provided by the two forward-drop diodes CR06 and CR07. These are silicon diodes having a forward voltage drop of approximately 0.7v. The two diodes in series provide a voltage shift of +1.4v from the cathode of CR06 to the anode of CR07.

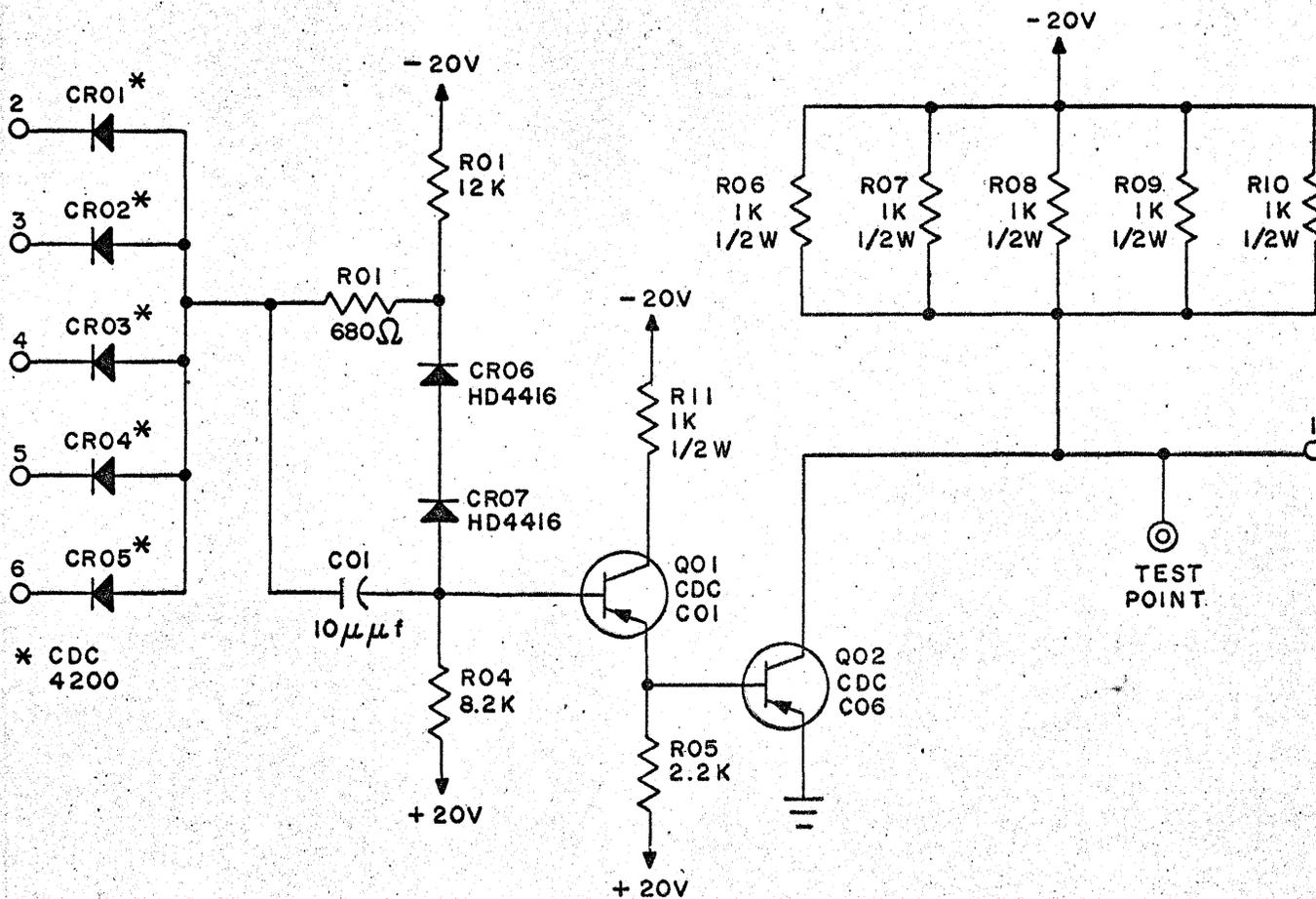
With -1.1v "0" inputs, the base of Q01 is held at approximately +1.3v by the level-shifting diodes. Transistor Q01 is connected as an emitter follower; thus its emitter voltage is equal to the base voltage plus the base-emitter junction drop, and is approximately +1.6v. This provides sufficient forward bias so that minimum conduction is maintained through Q01. The emitter voltage of Q01 drives the base of Q02, which is a grounded emitter stage. The base-emitter junction of Q02 is therefore back-biased by the +1.6v input, and Q02 is cut off.

A -5.8v "1" input holds the base of Q01 at approximately -0.6v causing Q01 to conduct heavily. The emitter voltage of Q01 goes to approximately -0.3v, which causes Q02 to switch on and conduct heavily. In this state, the circuit output is equal to the drop across Q02, and approaches -0.3v.

With Q02 in the cut off state, its collector voltage tends to rise toward -20v. However, the 200-ohm load acts as a voltage divider with the equivalent 200-ohm resistance of the five 1000-ohm resistors, and the output stabilizes at -10v.

DELAY LINE DRIVER

CARD TYPE C08



* CDC
4200

NOTES:

1. CIRCUIT HAS 5 "OR" INPUTS.
2. A -5.8V "1" INPUT CAUSES TRANSISTORS TO CONDUCT.

DUMMY INHIBIT GENERATOR

Card Type C09

FUNCTION

The function of the circuits on this card is to enable a 340 ma current to flow from pin 1 or 15 to ground, whenever at least one input to the respective circuit is a -1.1v "0". The dummy inhibit circuits are energized by a +40v supply, and each circuit contains a series 133-ohm resistor external to the circuit on the card. Each dummy inhibit circuit terminates at either pin 1 or pin 15 of a C09 card, and the path will be completed to ground allowing current to flow if the respective dummy inhibit generator switches to its conduction state.

OPERATION

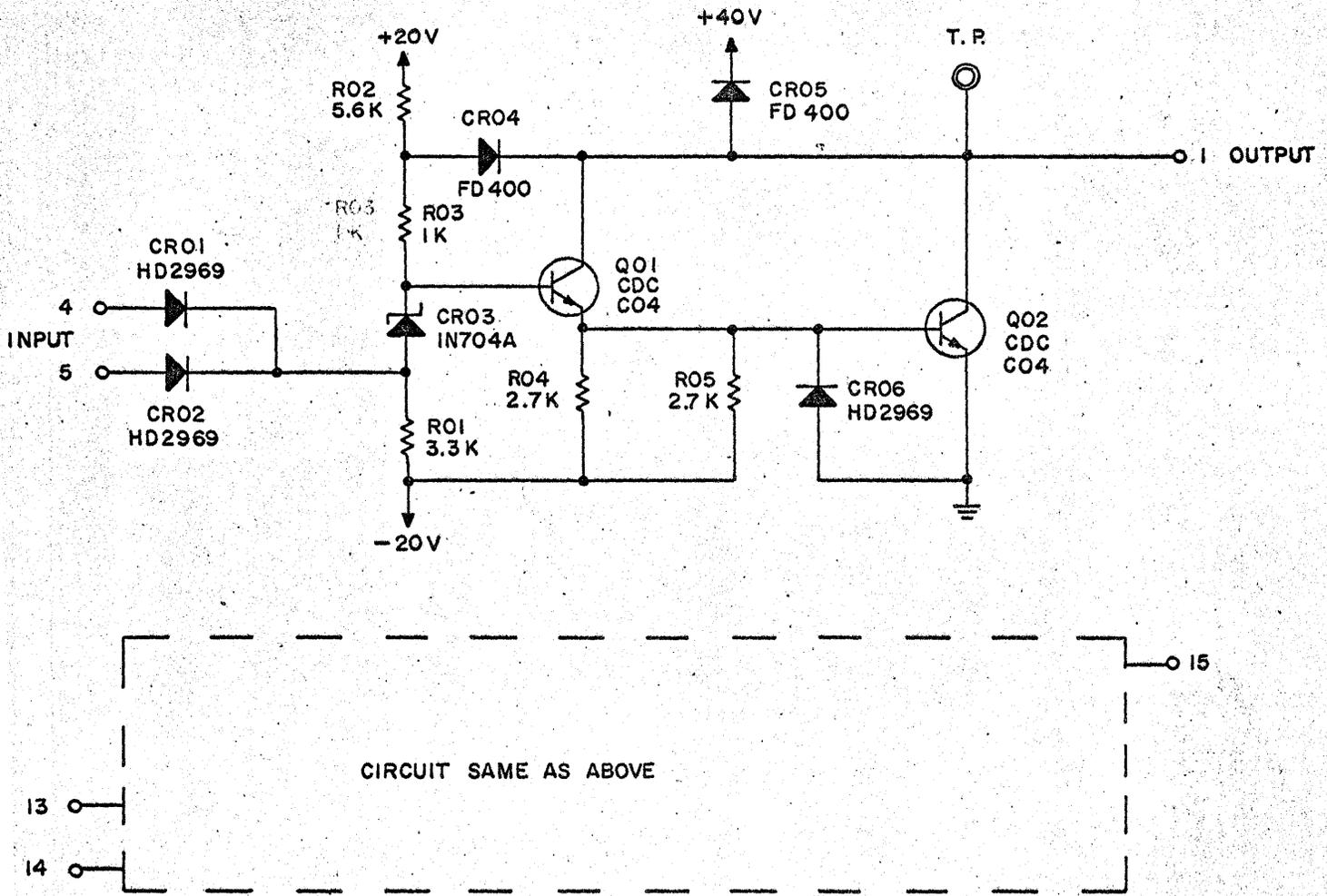
Each circuit has a two-way logical AND input, meaning that both inputs must be at the -5.8v "1" level in order for an input to be sensed. A -1.1v "0" signal on either input will disable the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

The transistors are disabled if the AND is satisfied by two -5.8v "1" inputs, preventing dummy inhibit current from flowing. If either input receives a -1.1v "0", the transistors switch to the conduction state and current is allowed to flow from the output pin to ground.

A level-shifting action is provided by the 4.1v zener diode CR03. This diode is reverse-biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

When the AND is satisfied by -5.8v "1" inputs, this voltage level plus the forward drop of diodes CR01 and CR02 holds the anode of CR03 at approximately -6.1v. The base of Q01 is therefore at approximately -2v. The emitter of Q01 is held at approximately -0.3v by the forward drop of CR06. This places a reverse bias of 1.7v across the base-emitter junction of Q01, so that it is well into the cut off region. In addition, the 0.3v drop of CR06 reverse-biases the base-emitter

DUMMY INHIBIT GENERATOR CARD TYPE C09



CIRCUIT SAME AS ABOVE

NOTES:

1. EACH CIRCUIT HAS A TWO-WAY "AND" INPUT.
2. A -1.1V "0" ON EITHER INPUT ENABLES CIRCUIT TO CONDUCT.
3. -5.8V "1"s ON BOTH INPUTS PREVENT CIRCUIT FROM CONDUCTING.

junction of Q02, so that it is also cut off. Thus, except for negligible leakage effects, the output pin is completely isolated from ground.

When either input receives a -1.1v "0", the anode of CR03 is held at approximately -1.4v . The 4.1v voltage differential across the zener diode CR03 attempts to hold the base of Q01 at approximately $+2.7\text{v}$. This causes Q01 to switch on and conduct heavily, but it is clamped out of saturation by CR04. The emitter voltage of Q01 rises to approximately $+2.2\text{v}$, providing drive to the base of Q02. Transistor Q02 thus switches to the conduction state, allowing current to flow from the output pin to ground.

The connection of diode CR05 and the $+40\text{v}$ supply provides a clamp for the collector voltage of the transistors. When the transistors switch to the non-conducting state, the inductance of the dummy inhibit line will tend to induce high-voltage transients; however, these inductive transients are clamped at $+40\text{v}$ plus the drop across the silicon diode CR05.

DRIVER TRANSFORMER

Card Type C10

FUNCTION

The function of this card is to provide half-currents of 340 ma at approximately 44v to the memory stack when supplied with primary power at the +20v level. The card contains four 6:4.5 voltage step-up transformers, each having two secondary windings of 60 turns and a center-tapped primary of 90 turns. The transformers are connected so that two operate simultaneously with their primary windings energized in parallel from +20v and their secondaries connected in series. The output voltages are therefore additive, resulting in levels of approximately 44v.

This card operates in conjunction with three other cards; a gate card which switches a source of +20v into the center taps of the transformer primaries, and with two transformer driver cards which allow current to flow from one of the primary windings to ground.

OPERATION

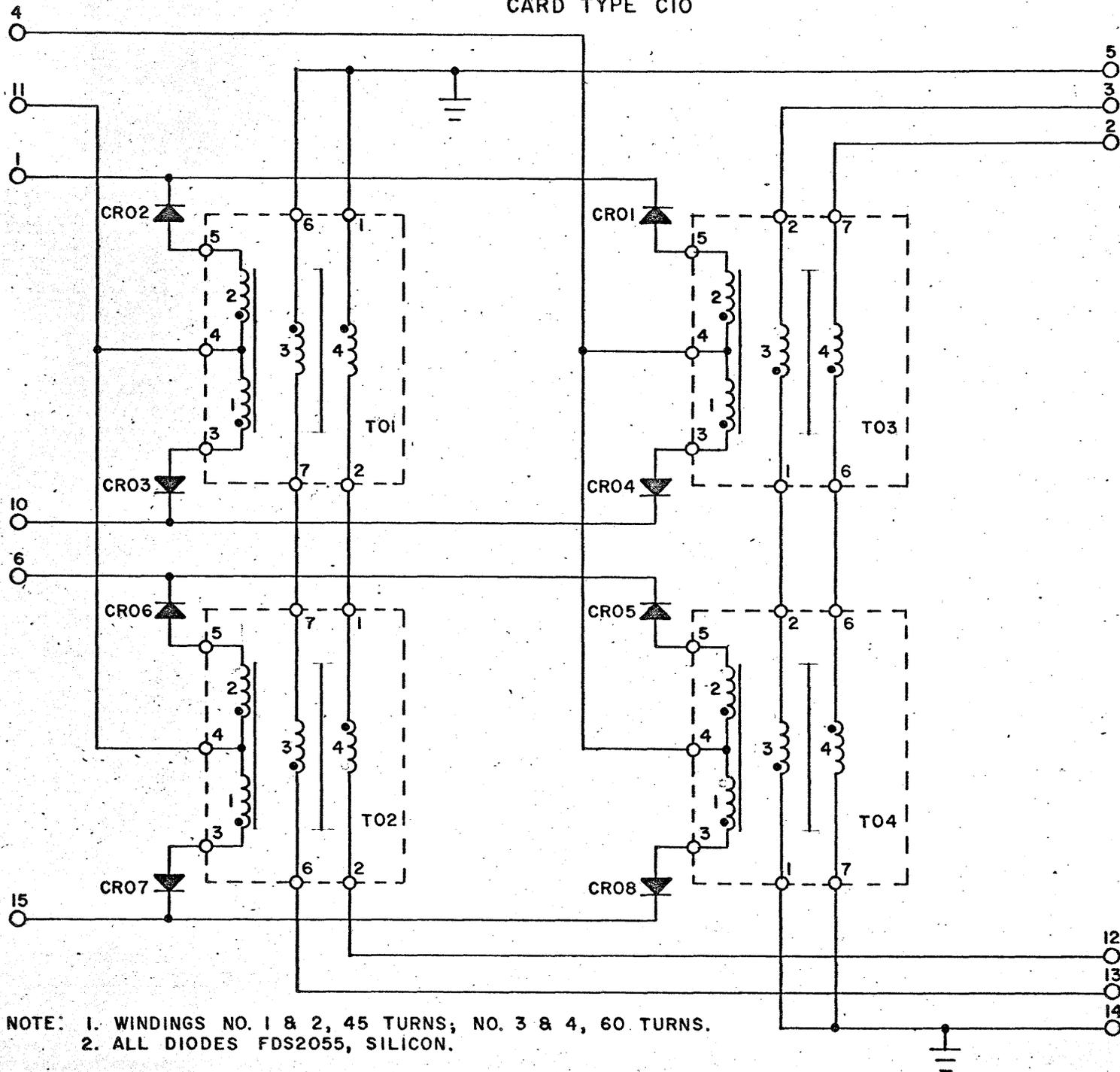
A schematic of the circuit contained on card type C10 is presented in the accompanying diagram, with the transformers indicated by dashed outlines. The transformers are identical, each having four windings and seven connecting pins as shown. Silicon diodes at transformer pins 3 and 5 provide isolation so that current cannot flow through a primary winding in the wrong direction, and prevent interaction between transformers.

The dots on the transformer windings indicate the direction of current flow. For example, if current flows into the dotted end of the primary winding, current will also flow into the dotted end of the secondary winding. There will consequently be a voltage reversal between the dotted ends of the primary and secondary windings.

As an example of operation, assume that card pin 11 is energized from a source of +20v. This is fed to the center tap of the primary windings of transformers T01 and T02. Then, by connecting card pins 1 or 10, and 6 or 15 to ground, it is possible to produce either +44v or -44v at either pin 12 or pin 13 while the

MEMORY DRIVER TRANSFORMER

CARD TYPE C10



NOTE: 1. WINDINGS NO. 1 & 2, 45 TURNS; NO. 3 & 4, 60 TURNS.
 2. ALL DIODES FDS2055, SILICON.

3-37

other pin remains at essentially zero potential. The positive and negative potentials correspond to the memory cycle, in which a current of one polarity is used to "read" and the other to "write".

To produce -44v at pin 12, the external circuitry would connect card pins 10 and 15 to ground, allowing 450 ma to flow through windings #1 of T01 and T02. The primary voltage is of the order of +18v, due to the drop across the silicon diode and external circuitry; however, the 6:4.5 transformer step-up produces a secondary voltage of approximately +22v.

It is seen that windings #4 of T01 and T02 are connected in series so that the voltages are additive, resulting in -44v at pin 12. It is further seen that windings #3 are connected oppositely, so that the voltages cancel and only a negligible effect is produced at pin 13. However, -44v will appear at pin 13 with negligible voltage at pin 12 if the external circuitry grounds pin 6 instead of pin 15.

If it is desired to produce +44v at pin 12, then pins 1 and 6 will be grounded; and if the +44v is to appear at pin 13, pins 1 and 15 will be grounded.

Under the preceding sets of conditions, the voltages appearing on pins 12 and 13 will appear on pins 2 and 3, if the source of +20v is gated into pin 4 instead of pin 11.

The various outputs available at pins 2, 3, 12, and 13 and the conditions necessary to produce them, are listed below. Pin 5 provides a common return for pins 12 and 13, and pin 14 provides a common return for pins 2 and 3.

Gate +20v into:	Enable Ground Connection From:	Resulting Voltages at:			
		Pin 2	Pin 3	Pin 12	Pin 13
Pin 4	Pins 6 & 10	-44v			
Pin 4	Pins 1 & 15	+44v			
Pin 4	Pins 10 & 15		-44v		
Pin 4	Pins 1 & 6		+44v		
Pin 11	Pins 10 & 15			-44v	
Pin 11	Pins 1 & 6			+44v	
Pin 11	Pins 6 & 10				-44v
Pin 11	Pins 1 & 15				+44v

BASIC INVERTER CIRCUIT

The basic inverter circuit consists of two transistor stages, as shown in figure 1. Transistor Q01 is a grounded emitter stage which supplies AND current to the load, and transistor Q02 is an emitter follower stage which supplies OR current to the load.

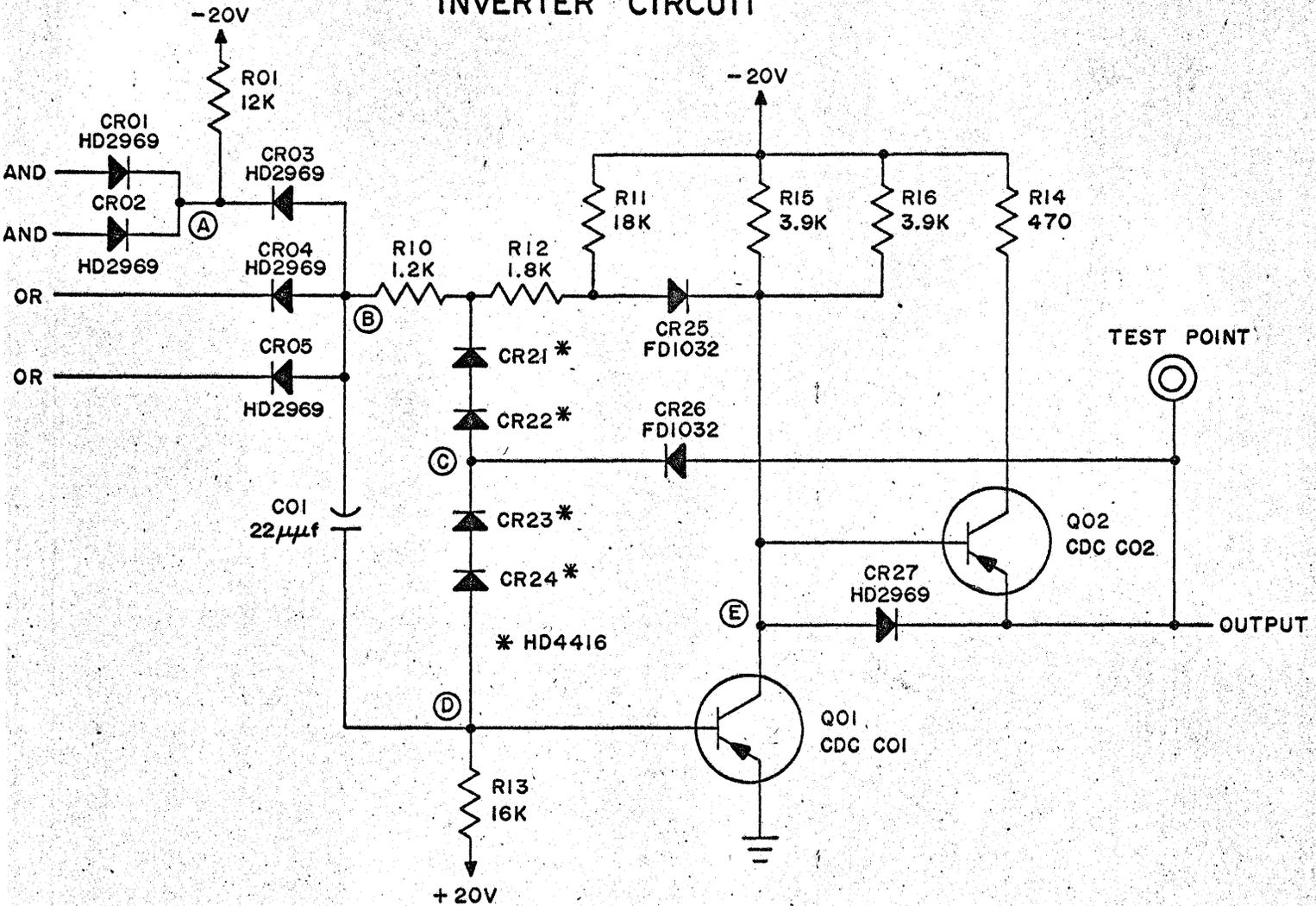
The input to the circuit consists of two levels of diode logic. The maximum number of inputs is limited by the number of available input pins on a circuit card; however, the maximum number of individual inputs to any single AND cannot exceed 6. The number of OR inputs has no similar restriction, and is limited only by the number of input pins.

The input logic diodes are Hughes HD2969, which are medium speed germanium devices. A set of graphs is included in this report which shows the comparative recovery time of these diodes.

The response of an AND input is a function of the time constant of the AND resistor R01, shunt circuit capacitance at point (A), and the recovery speed of the input diodes. Because additional AND diode inputs increase the shunt capacitance, it is necessary to decrease the size of the AND resistor a proportionate amount as the number of inputs to the AND increases beyond 3. Since the OR inputs are not affected by this time constant, the output of an inverter circuit has better switching characteristics with an OR input than with AND inputs.

The transition speed of the AND circuit varies inversely with the recovery speed of the AND diodes. Slow diodes allow additional recovery current to be drawn, which in effect, allows a larger turn-on current in the first transistor stage.

INVERTER CIRCUIT



SIGNAL LEVELS	
LOGICAL "0"	-1.1V
LOGICAL "1"	-5.8V

The input resistor and diode network of transistor Q01 establishes the clamping levels for the output signal. This network also provides feedback to the base of Q01 which stabilizes the two quiescent values of the output voltage.

The input network establishes an input threshold level of approximately -3 volts. Thus, the input signal must be more negative than -3 volts before transistor Q01 turn-on current is allowed to flow. Silicon forward drop diodes CR21 through CR24 are used in the input network to obtain a constant d-c level for signal threshold. These diodes also have a low dynamic impedance which causes little attenuation of the input signal current.

The 22 uuf speed-up capacitor C01 on the input of the first stage bypasses the 1.2 k resistor R10 and the diode network during the initial rise or fall of the input signal. This provides additional drive to the base of Q01 during the input signal transition, thereby speeding the switching of this stage.

Feedback is accomplished through two high speed silicon diodes CR25 and CR26, which have very low stored charge characteristics. If these diodes were capable of storing excessive charge, there would be additional delay in switching. By using diodes with very low storage, the initial switching speed is greatly improved.

When the grounded emitter stage Q01 is turned on, collector current flows out of the circuit through the series diode CR27. In this state, Q01 can supply current to 8 AND loads. Transistor Q01 is clamped out of saturation by the silicon feedback diode CR26, and the output voltage settles at a nominal value of -1.1 volt. The voltage drop across diode CR27 insures a back bias being applied to the base-emitter junction of Q02, thereby keeping this stage turned off.

When Q01 turns off, the collector voltage starts to rise toward -20 volts. Since the voltage across the load cannot change as quickly as the collector voltage of Q01, the series output diode CR27 is back-biased and the output emitter follower stage Q02 is turned on.

The turn-on current is applied to the base of Q02 at the rate at which Q01 turns off. The turn-on current is the current that is drawn through the first stage collector resistors R15 and R16, and this current is available to turn on the output stage only as fast as it is turned off in the first stage.

Transistor Q02 in the on state proceeds to drive the output voltage negative. At about -5.8 volts, the output is fed back to the input of the first stage by diode CR25 to start the clamping action. Since this process has delay associated with it, the output signal overshoots the -5.8 volt mark and may carry as far as -8 volts. The circuit then settles the voltage back to the -5.8 volt level. During this time, transistor Q02 can pass the current of 8 OR loads through to the -20 volt supply.

The switching speed of the circuit is slightly faster when driving OR loads instead of AND loads. With full AND loading, the turn-on and turn-off transition times are less than 30 nanoseconds. The transition time to the -3 volt threshold is approximately 10 to 15 nanoseconds. This accounts for the majority of the inverter circuit delay, which is less than 20 nanoseconds.

In the case of driving 8 OR loads, the transitions are faster. This is because transistor Q02 is being driven by Q01 and the gain of both transistors is effective in switching the load. This additional gain causes the output load to be driven harder and therefore switches it faster.

Ground Rules

1. An inverter may simultaneously drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.
2. A flip-flop or a control delay may drive only 7 loads, because it is required to provide its own feedback which constitutes 1 load.
3. The switching time for a circuit output to change from a -5.8v "1" to a -1.1v "0", or vice versa, is approximately 30 nanoseconds.
4. The delay time required for a circuit output to reach the -3v threshold is approximately 10 to 20 nanoseconds and is dependent upon the loading.
5. A circuit having an OR input will switch faster than a circuit having an AND input; thus the delay time is reduced with an OR input.
6. Generally, two electronic inversions and a total of 60 inches of lead length are allowed between successive clock phases. This rule may be violated in cases where the logic circuits are very lightly loaded, but all such cases must be individually inspected to certify satisfactory operation.
7. Any interconnecting lead more than 80 inches long must be clamped by means of the circuit on card type C02.
8. All drive lines from H⁻⁻⁻ terms to N⁻⁻⁻, V⁻⁻⁻, or Y⁻⁻⁻ terms must be clamped, regardless of length.
9. N⁻⁻⁻, V⁻⁻⁻, and Y⁻⁻⁻ terms having a clock signal on an AND input must use one of the special card types numbered C72, C73, and C74. The clock input must be on the following pins:

Card Type	Inverter A	Inverter B
C72	5 or 6	13 or 14
C73	2 or 3	10 or 11
C74	5 or 6	13 or 14

10. In case an entire AND input group is unused, at least one of the inputs must be grounded.
11. All OR inputs on control delay cards are effectively single-way ANDs, and must be grounded if not used.

Test Results

The following pages contain graphs showing the comparative recovery time of the logic diodes and the margins over which the +20v and -20v supplies may vary.

The voltage margin tests were made by varying the supply voltage of an entire chassis until failure occurred. The final version of the inverter circuit was tested in a chassis composed of 1170 cards which contained 2046 inverters.

DISTRIBUTION OF REVERSE RECOVERY TIME

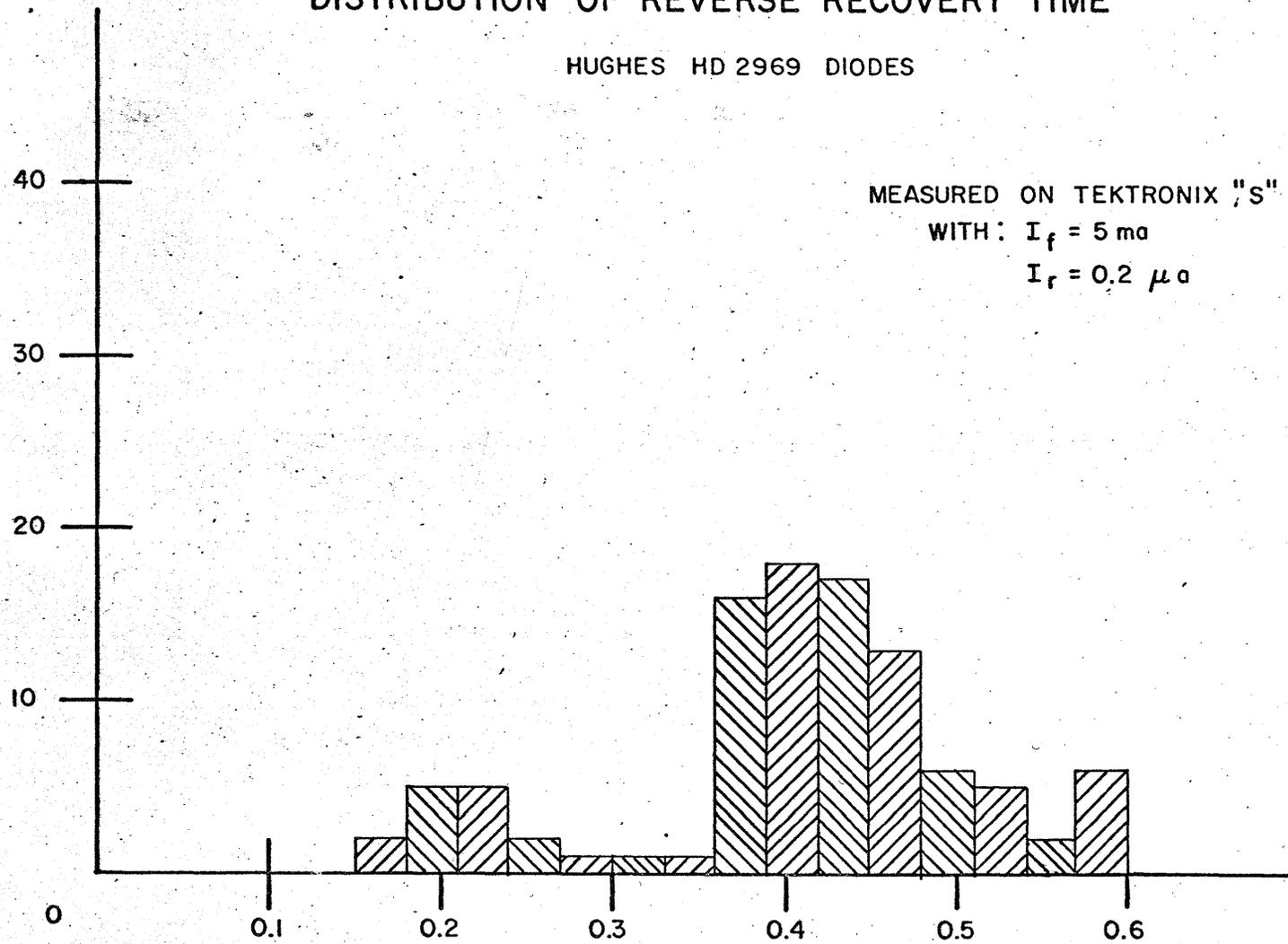
HUGHES HD 2969 DIODES

MEASURED ON TEKTRONIX "S" PLUG-IN

WITH: $I_f = 5 \text{ ma}$

$I_r = 0.2 \mu \text{ a}$

3-45
NUMBER OF UNITS



RECOVERY TIME (μ sec)

DISTRIBUTION OF REVERSE RECOVERY TIME

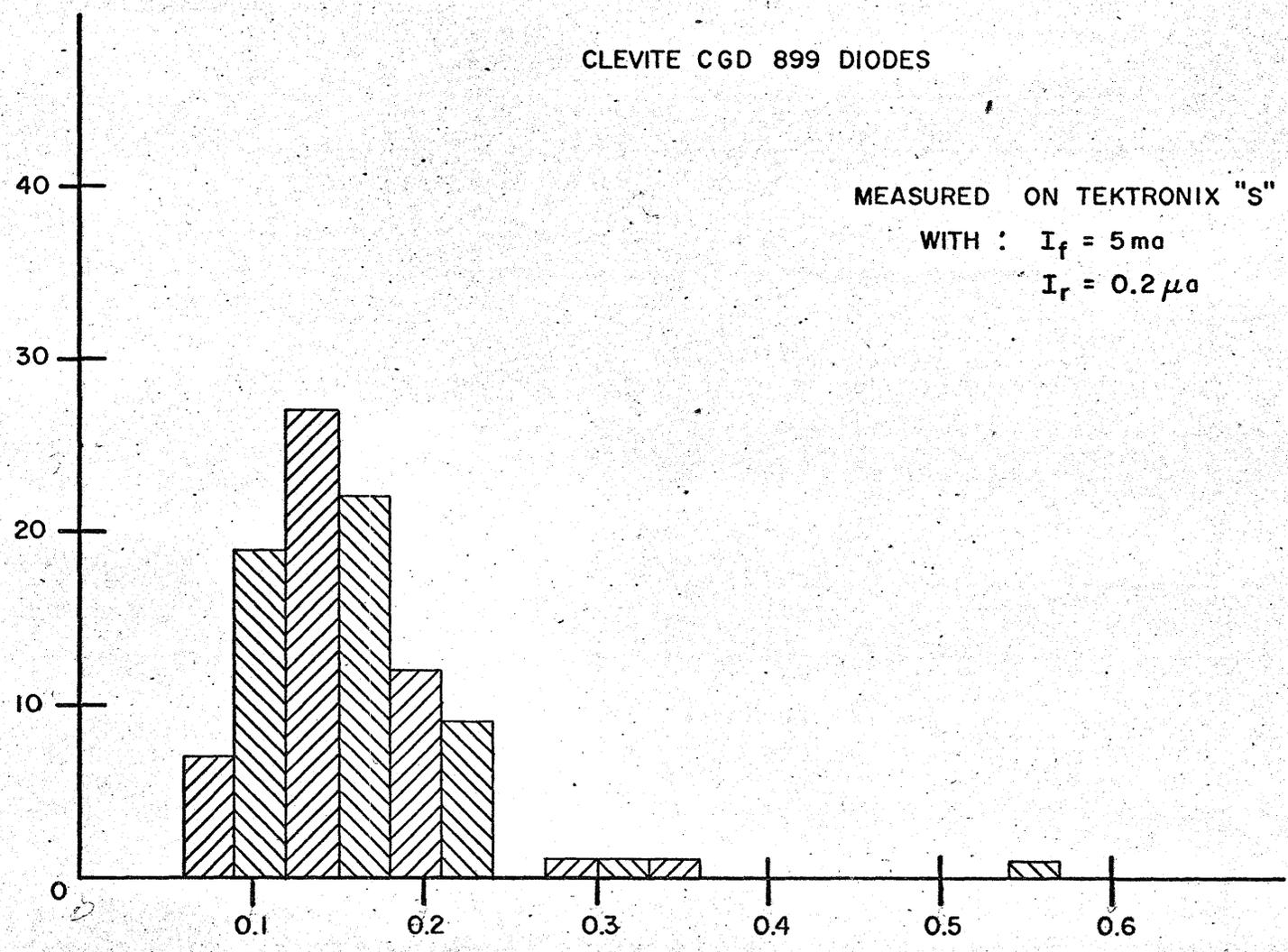
CLEVITE CGD 899 DIODES

MEASURED ON TEKTRONIX "S" PLUG-IN

WITH : $I_f = 5 \text{ ma}$

$I_r = 0.2 \mu\text{a}$

NUMBER OF UNITS

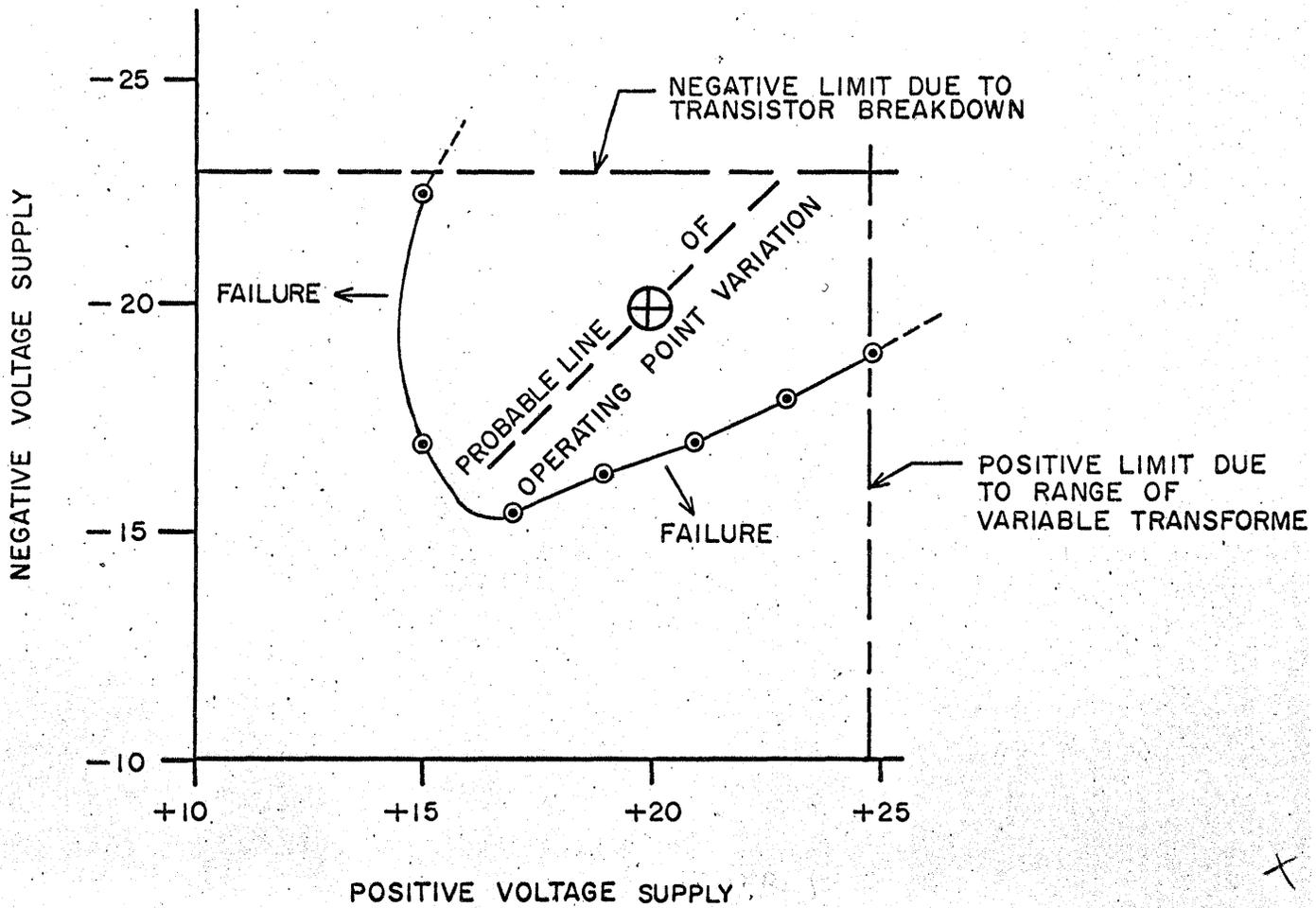


RECOVERY TIME (μSEC)

3-49

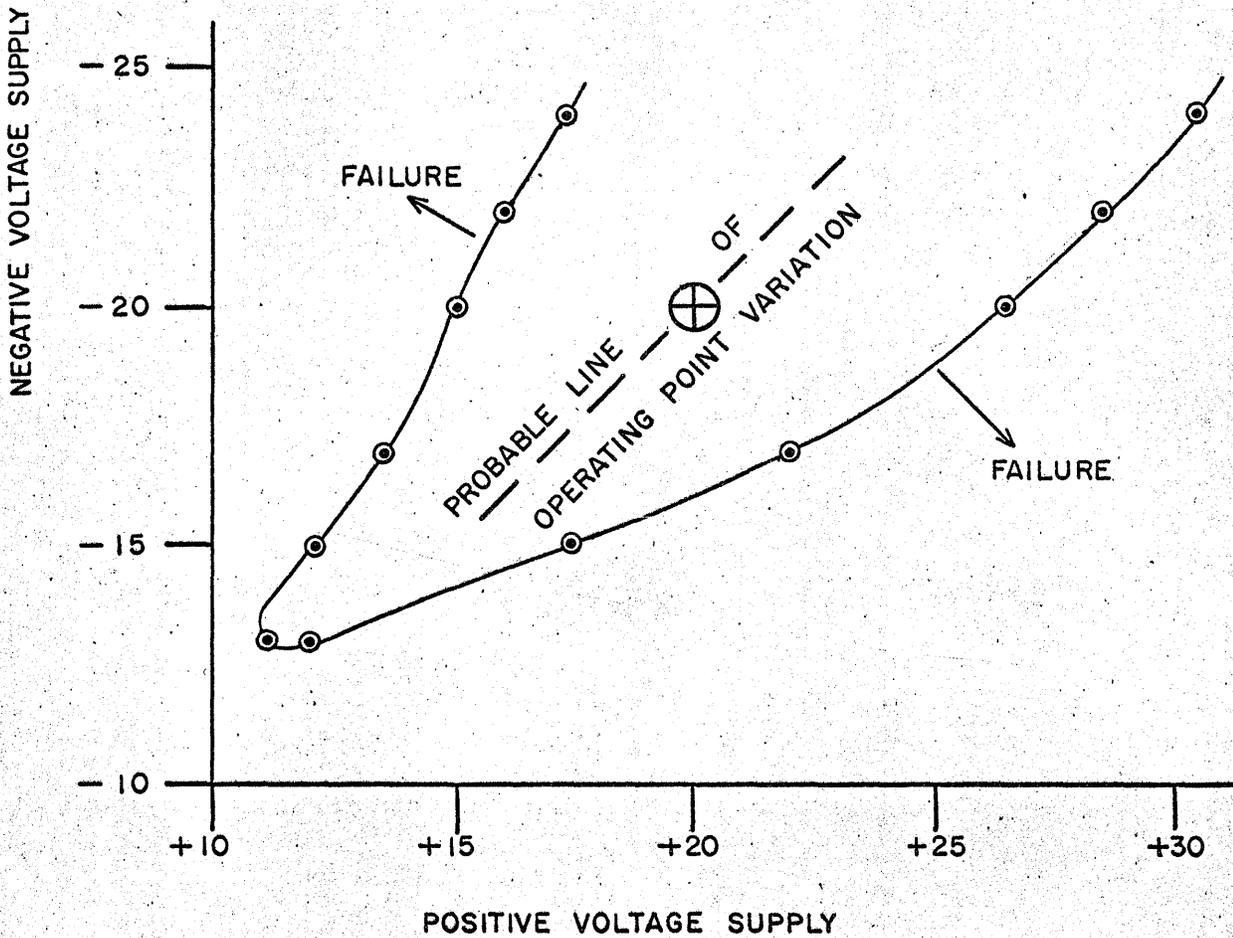
VOLTAGE MARGINS

TEST CHASSIS CONTAINING 1170 CARDS (2046 INVERTERS)
FINAL VERSION OF CIRCUIT AS SHOWN IN FIGURE 1



VOLTAGE MARGINS

8 mc "P" COUNTER CONTAINING 43 CARDS
LOGIC DIODES HD1804



TRANSMITTER AND RECEIVER

Card Types C62 and C61

GENERAL

The circuit configuration shown in figure 1 performs high speed transmission of digital information from one module to another. Inputs to the transmitter circuit are logical "1's" and "0's" of -5.8v and -1.1v, respectively. The transmitter converts these single-ended inputs to double-ended outputs suitable for transmission over a balanced transmission line. Tests using an 8-megacycle bit rate input have shown that 1 transmitter will satisfactorily drive 20 receivers and 19 unused transmitters located at any point along a 200 foot transmission line.

The transmission line is twisted-pair having a characteristic surge impedance of approximately 110 ohms and is terminated at each end in its characteristic impedance. Transmission signal levels are approximately 0.5v line-to-line, and a "1" is distinguished from a "0" by a full voltage reversal.

The line voltage levels which represent a "0" are established by current flow from the +20v to the -20v source at the terminating resistors. Each of these currents is of the order of 5 ma, so that the total voltage developed across the terminating resistors is approximately 0.5v.

When the 3-way AND input to the transmitter is disabled by a "0", transistor Q01 is turned on and current is shunted around the two constant current drivers Q02 and Q03. With the AND enabled by "1" inputs, Q01 is turned off, thus allowing Q02 and Q03 to drive a constant 20 ma into the transmission line. Originally, the bias networks on the line were producing a 5 ma current flow in one direction through the terminating resistors, but when the transmitter switches on, the direction of net current flow through the terminating resistors effectively reverses. The current from the transmitter divides into two 10 ma currents which flow through each line termination. This current is in the opposite direction to the 5 ma bias current; thus the net current flow is 5 ma in the opposite direction, producing a voltage drop equal and opposite to the original voltage. This results in a full voltage reversal for separating a "1" from a "0", although the signal level remains of the order of 0.5v line-to-line.

TRANSMITTER, Card Type C62

The printed circuit card contains two identical transmitter circuits designated A and B. A typical circuit is shown in figure 1.

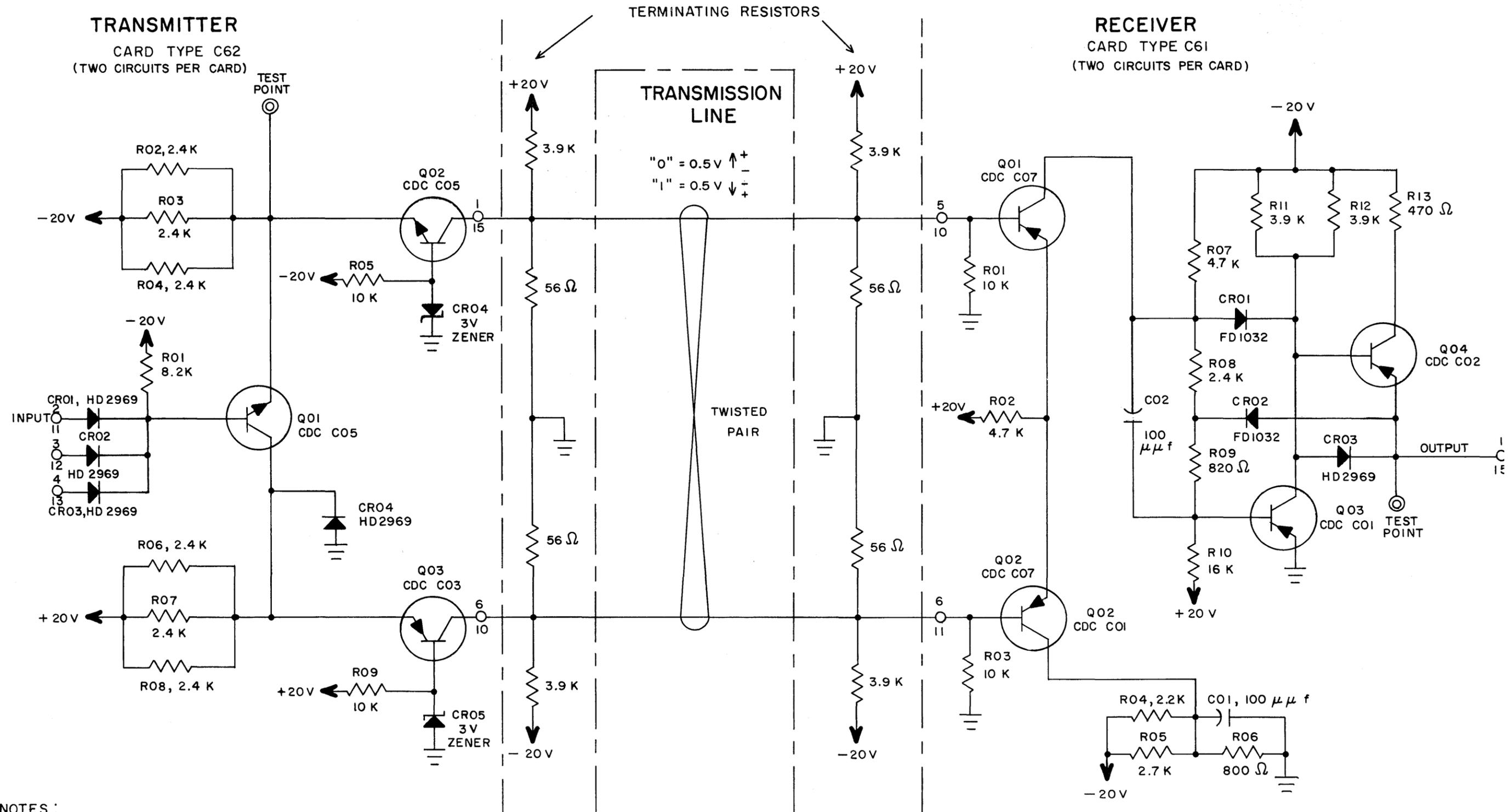
The logic input circuitry consists of a 3-way AND. The output of a standard logic card constitutes a proper input to a transmitter. A logical "1" input causes transistor Q01 to turn off and Q02 and Q03 to turn on, while a "0" input has the opposite effect.

Transistors Q01 and Q02 are NPN silicon CDC C05's and Q03 is a PNP germanium CDC C03. Their characteristics are listed in the component section.

A -1.1v "0" input to the base of Q01 causes the emitter-base junction to be forward biased, turning Q01 fully on. When Q01 is turned on, a shunt path for current is provided around Q02 and Q03. Since Q02 and Q03 no longer have a source of current, no current is injected into the transmission line.

When the "AND" input is satisfied, the base of Q01 will be held at approximately -6.4 volts. This reverse-biases the emitter-base junction by approximately 3 volts and causes Q01 to be turned off. Since the shunt path for current around Q02 and Q03 no longer exists, they become constant current generators of opposite polarities. Q03 injects a current of approximately 20 ma into the line and a like amount of current flows out of the line into Q02.

The base networks of Q02 and Q03 each contain a 3v zener diode which performs two functions. In the first case, the zener diode sets the voltage level at which the emitters of Q02 and Q03 will reach their turned-on state. This, in turn, sets the threshold that must be overcome at the base of Q01, since its emitter is at the same potential as the emitter of Q02. In the second case, the zener diodes set the base voltages of Q02 and Q03 which determine how much noise voltage will be allowed at the collectors before the collector-base junctions become forward biased. This value of noise voltage is something over 3 volts since the forward drop of the collector-base junctions adds to the zener diode voltage. This means that the transmitter will operate satisfactorily with up to 3 volts of random noise on the transmission line.



NOTES :

1. THE CONNECTION SHOWN DOES NOT PROVIDE A LOGICAL INVERSION; A "1" INPUT RESULTS IN A "1" OUTPUT.
2. TO PRODUCE AN OVER-ALL LOGICAL INVERSION, THE TRANSMISSION LINE CONNECTION AT THE RECEIVER WOULD BE REVERSED.
3. THE TRANSMISSION LINE CONNECTION AT THE TRANSMITTER CAN NOT BE REVERSED, BECAUSE OF VOLTAGE POLARITIES.

The transmitter must be connected to the line in only one polarity, as shown in figure 1. This is necessary in order to provide current through the terminating resistors in a direction opposite to the bias current.

TRANSMISSION LINE

A terminated balanced twisted-pair transmission line is used to carry digital information from the transmitter to the receiver. This information is in the form of line-to-line differential voltages of the order of 0.5v, with a complete voltage reversal distinguishing a "1" from a "0".

The surge impedance of the transmission line is 100 to 120 ohms. The line is terminated at each end with a 112-ohm resistive load, consisting of two 56-ohm resistors in series across the line with an optional center ground reference. This provides very good impedance matching and, as a result, reflections and standing waves are minimized.

Present plans call for biasing the line at each end by means of 3.9k resistors to +20v and -20v to achieve a 5 ma bias current through the terminating resistors. This holds the "0" state signal level at 0.5v line-to-line. In the future it may prove feasible to bias the line at one end only, or perhaps in the center. This modification would necessitate a change in the size of the bias resistors.

The length of a transmission line may be up to 200 feet, with up to 20 transmitters and 20 receivers placed in parallel anywhere along its length.

Bit rates of 8 mc or greater are possible on a 200 foot line. Low bit rates over longer distances are limited by the DC line losses, however transmitters may be paralleled for longer distances to overcome these losses.

The velocity of signal propagation along the line is approximately 50% to 60% of the velocity of light. This results in a time delay per foot of the order of 1.6 to 1.8 nanoseconds.

The balanced system using differential receiving techniques allows a difference in noise levels of up to 3v to be tolerated between the transmitter ground reference and the receiver ground reference.

RECEIVER, Card Type C61

The printed circuit card contains two identical receiver circuits designated A and B. A typical example is presented in figure 1. The portion of the circuit connected to the collector of Q01 is quite similar to a logical inverter, which is discussed elsewhere in this report.

This circuit functions as both a differential amplifier and a discriminator. It provides a logic output of either "1" or "0", according to the polarity of the differential 0.5v signal which the two input terminals receive from the transmission line.

The circuit inputs are connected directly into the bases of Q01 and Q02. The 0.5v differential input is centered about ground, so that one input shifts approximately 0.25v positive while the other input shifts negative a similar amount. The two input transistors Q01 and Q02 are PNP type CDC C07's; thus the transistor which receives the negative input will conduct more heavily while the one receiving the positive input will conduct less heavily.

The circuit is such that a negative input to the base of Q01 and a positive input to the base of Q02 results in a logical "1" at the receiver output. Under the opposite conditions of a positive input to Q01 and a negative input to Q02, the output will be a logical "0". Thus, by reversing the connections at the receiver inputs, it is possible for a given set of conditions on the transmission line to produce either a "1" or a "0" at the receiver output.

The circuit shown in figure 1 does not produce an inversion between input to the transmitter and output from the receiver. A "1" input to the transmitter produces a transmission line signal of approximately 0.5v line-to-line with the polarity as shown. This allows transistor Q01 to apply approximately 5 ma of collector current to the junction of R07, R08, and the anode of CR01, which causes Q03 to switch off and Q04 to switch on, providing a "1" output. In this state, transistor Q04 can drive 8 OR loads. With opposite conditions at the receiver input, the output can drive 8 AND loads.

Ground Rules

1. The output of a logic card constitutes a proper input to a transmitter.
2. The output of a receiver constitutes a proper input to a logic card.
3. A receiver may drive 8 OR loads, 8 AND loads, or any combination resulting in 8 loads total.
4. The transmission line is twisted-pair, having a surge impedance of 100 to 120 ohms.
5. The transmission line may be any length up to 200 feet.
6. The transmission line is terminated at each end in a resistive load approximately equal to its surge impedance.
7. A logical inversion between input to transmitter and output from receiver may or may not occur, depending upon the transmission line connections at the receiver.
8. The transmission line connections at the transmitter can not be reversed, due to the polarity of the line bias voltage.
9. Up to 20 transmitters and 20 receivers may be connected anywhere along a transmission line.
10. A transmitter having an 8 megacycle bit rate input will drive 20 receivers at the end of a 200 foot transmission line, with 19 inactive transmitters also connected to the line.
11. Inactive transmitters and receivers do not load a transmission line and do not have to be disconnected from it.

RESYNC CIRCUIT

Card Types C64, C65, C66

GENERAL

The resync circuit shown in figure 1 is contained on three printed circuit cards, the type numbers being C64, C65, and C66. The logical operation of this circuit is presented in figure 2, and a timing diagram is shown in figure 3.

The function of a resync circuit is to synchronize an asynchronous signal of random length with the computer clock. Upon receipt of a logical "1" input signal, the resync circuit produces a "1" output during a clock phase. This output is 62.5 nanoseconds long and is not repeated, regardless of the duration of the input.

The average time required for resynchronization is 2 clock phase times, taking into account the 40-nanosecond circuit delay. It is possible, however, for this to occur during 1 phase time, and it will never require more than 3. A simplified timing diagram of the resync circuit is shown in figure 3. The best case and worst case conditions refer to the length of time required for synchronization.

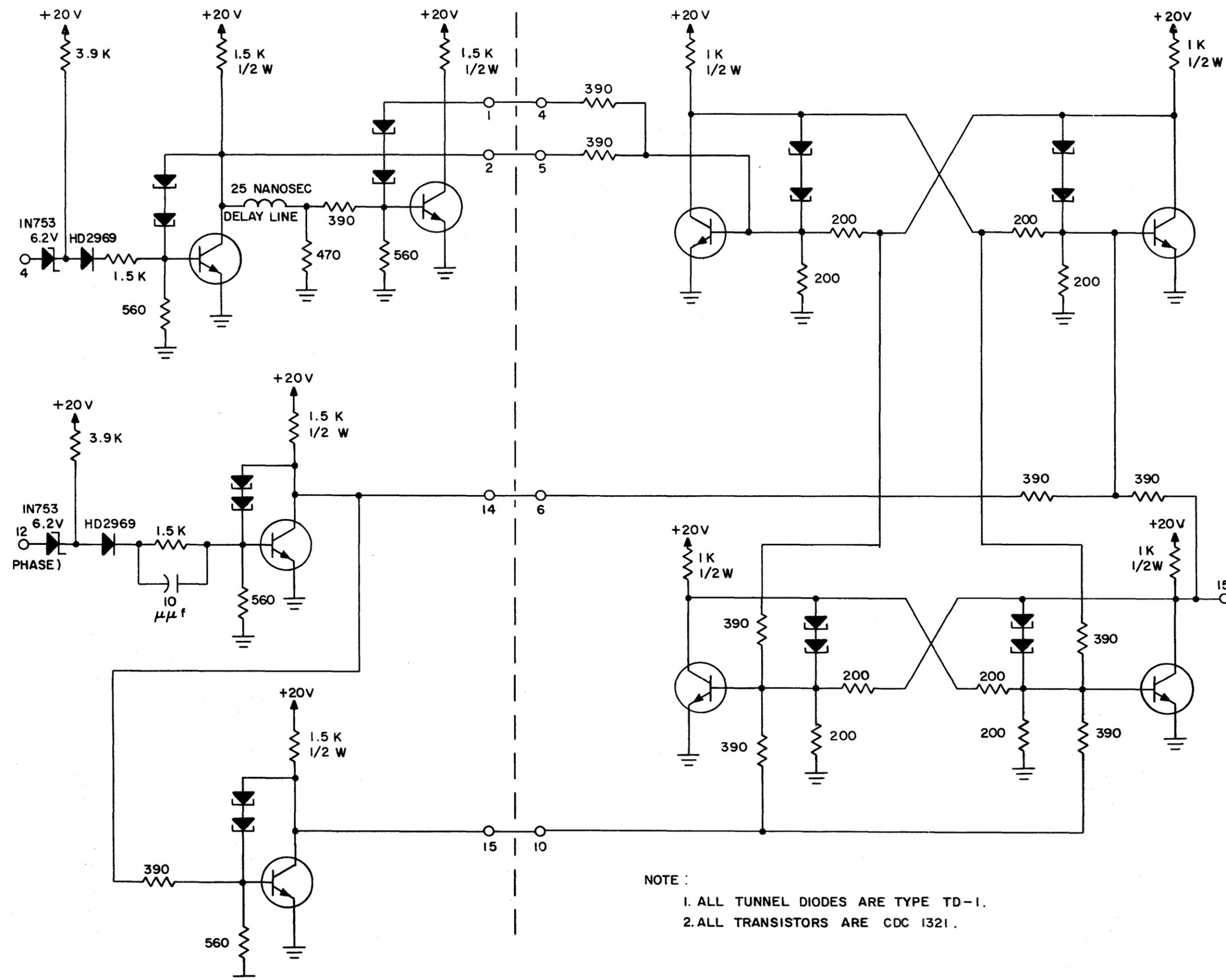
Logic levels within the resync circuit are in the positive voltage domain. A "0" is represented by +0.7v and a "1" by +1.7v.

LOGICAL FUNCTIONING

With initial conditions prevailing, the input to the circuit will be a steady "0" and the output of inverter 1 will be a steady "1". When a "1" input is received by the circuit, the delay line allows the output of inverter 1 to remain a "1" for approximately 25 nanoseconds, and it is during this time that FF 1 is set.

Next, FF 2 is set by the output of inverter 2. This output is timed by a clock phase which may be even or odd, but the relationship between the phases of the clock inputs must be as shown in figure 2.

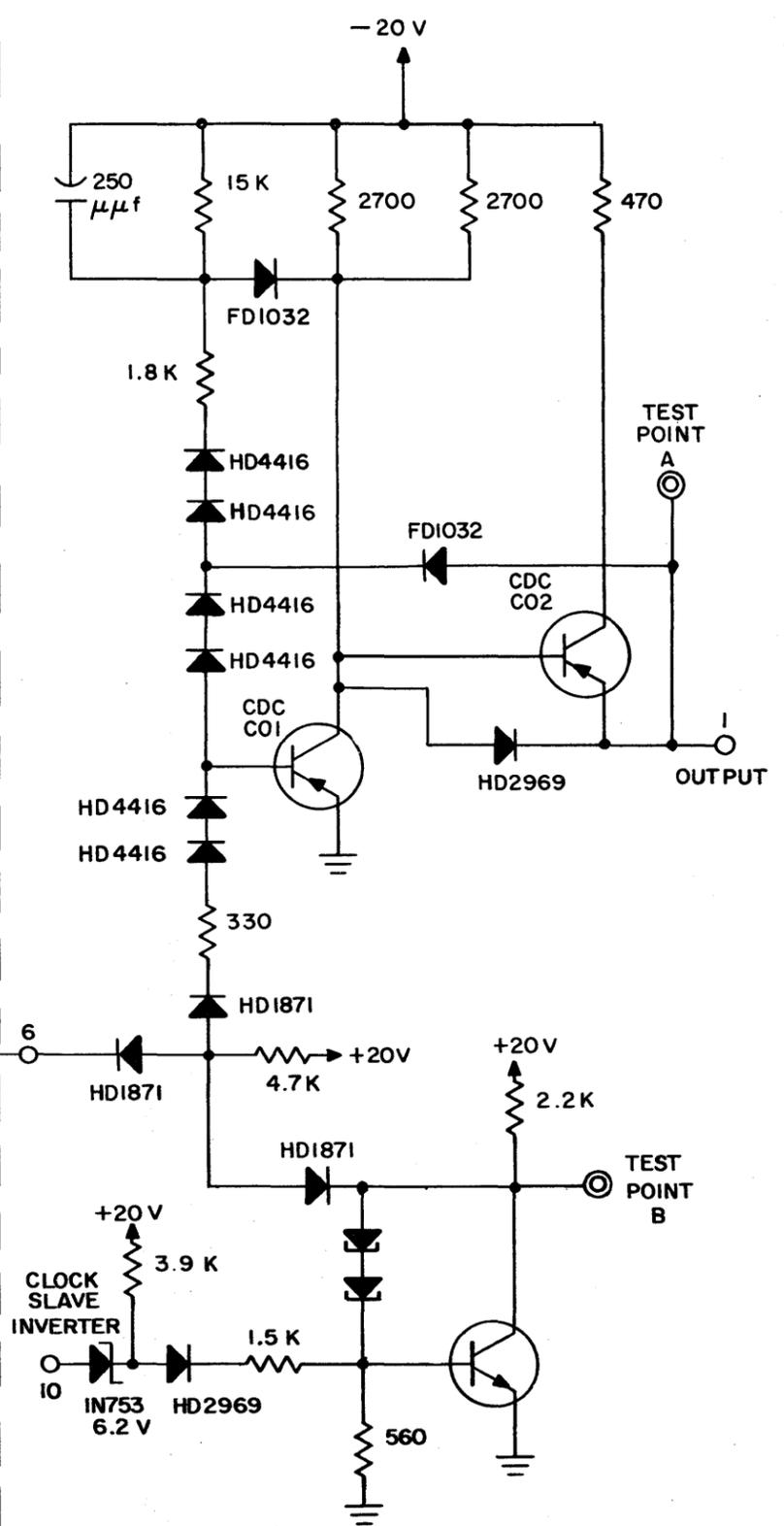
With FF 2 set, the "1" is gated out of the circuit by a full 62.5 nanosecond clock phase. Following this, the shifted phase clock input clears FF 1 and FF 2, and initial conditions prevail.



NOTE :
 1. ALL TUNNEL DIODES ARE TYPE TD-1.
 2. ALL TRANSISTORS ARE CDC I321.

CARD TYPE C64

CARD TYPE C65
 RESYNC CIRCUIT



CARD TYPE C66

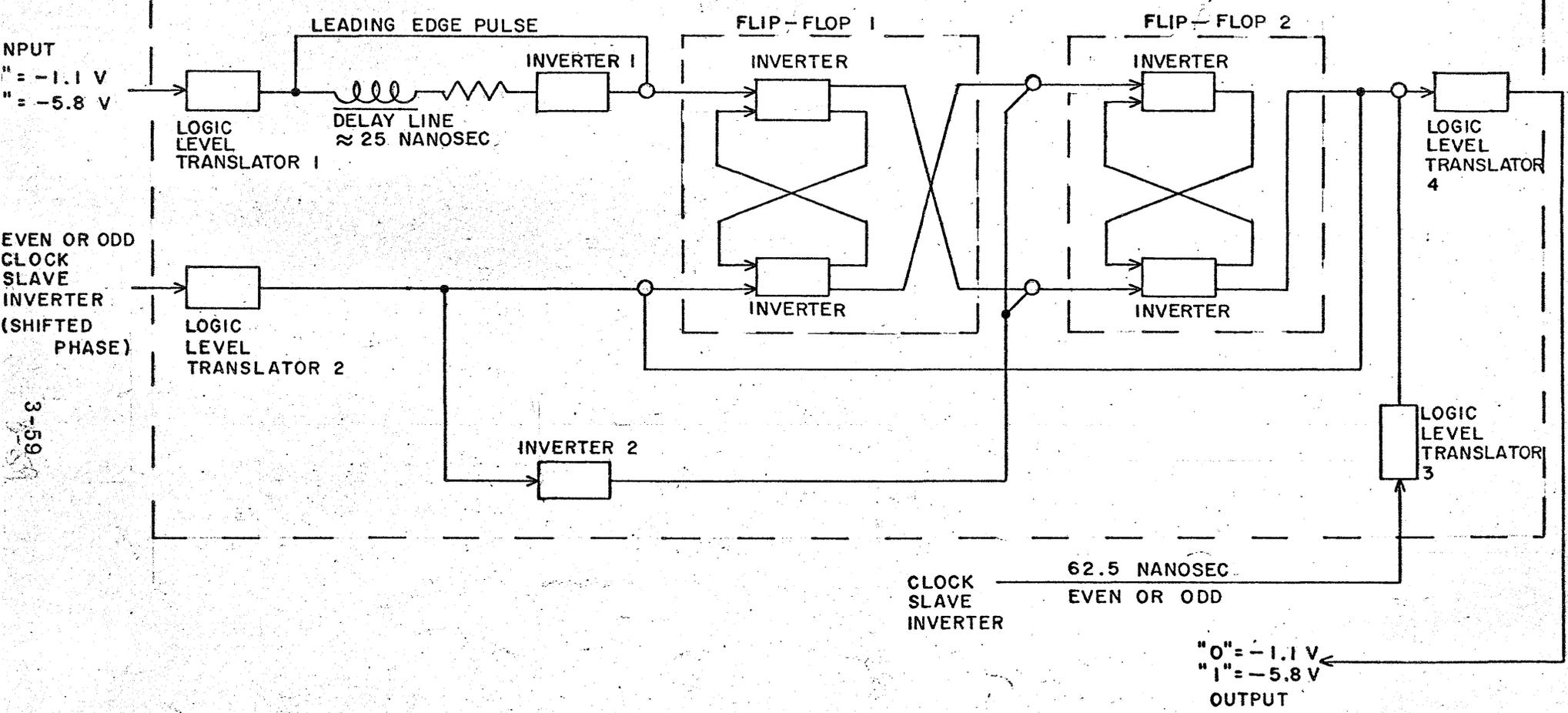
RESYNC CIRCUIT

INTERNAL LOGIC LEVELS :

"0" = +0.7 V

"1" = +1.7 V

≈ 4 NANOSEC
TIME PER INVERSION



INPUT
"0" = -1.1 V
"1" = -5.8 V

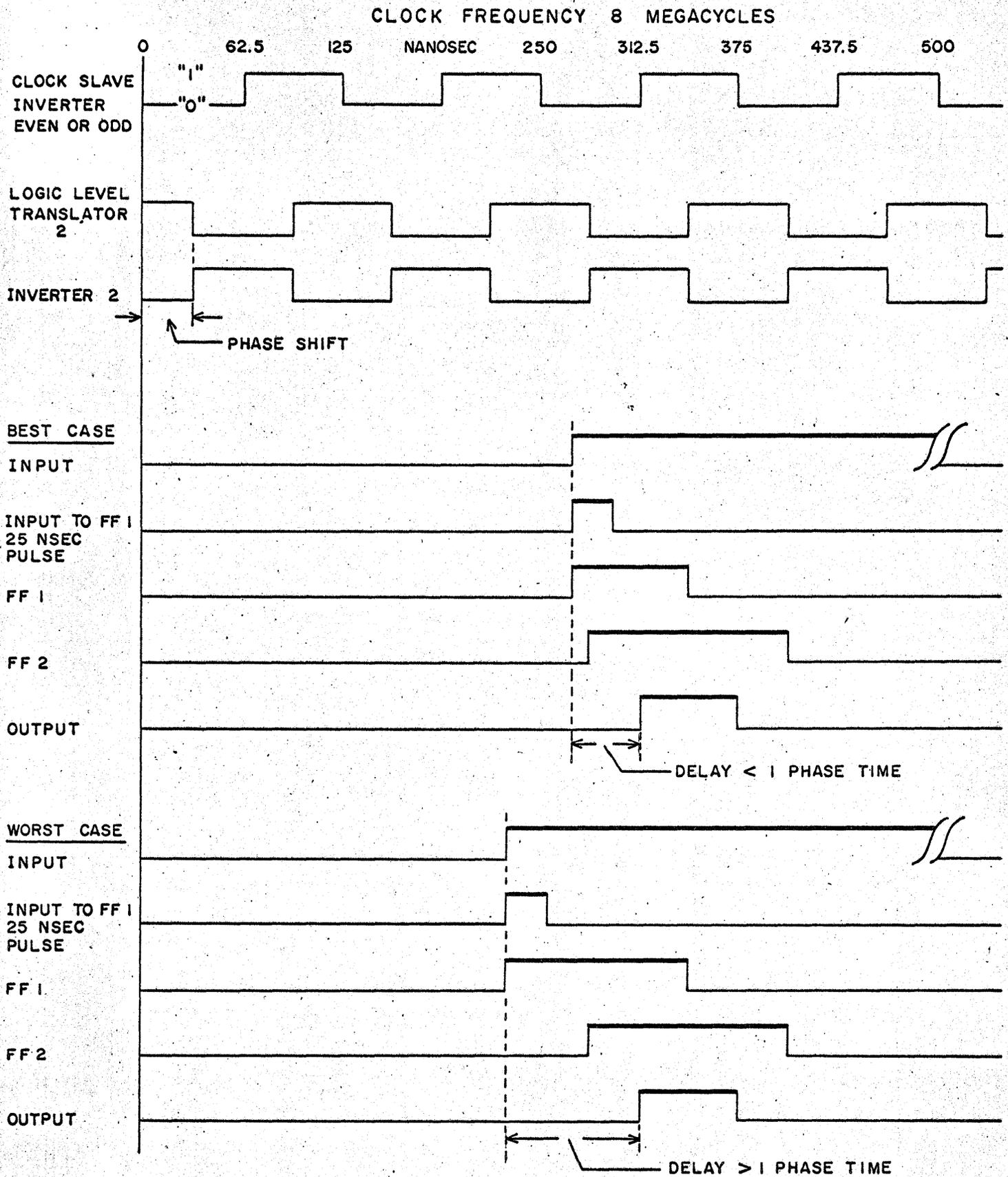
EVEN OR ODD
CLOCK
SLAVE
INVERTER
(SHIFTED
PHASE)

3-59

CLOCK
SLAVE
INVERTER
62.5 NANOSEC
EVEN OR ODD

"0" = -1.1 V
"1" = -5.8 V
OUTPUT

RESYNC CIRCUIT TIMING DIAGRAM



NOTE: THERE WILL BE AN ADDITIONAL DELAY OF \approx 40 NANoseconds FROM THE CLOCK SLAVE INVERTER INPUT AT PIN 10 OF THE C66 CARD TO THE RESYNC CIRCUIT OUTPUT.

CIRCUIT OPERATION

As shown in figure 1, except for the transistors in the output logic level translator, all of the resync circuit transistors are CDC 1321. This is a high speed silicon NPN type, having a gain-bandwidth of 1 kmc, which provides a time per inversion of approximately 4 nanoseconds, as used in this circuit. All of the CDC 1321 transistors have a base-to-collector tunnel diode network. This network establishes an input threshold level and holds the output voltage at the sum of the tunnel diode drops and the base-emitter junction drop.

The tunnel diodes are type TD-1. This is an axial tunnel diode having an $I_p = 1$ ma and a $V_{fp} = 500$ mv. Assuming an ideal case, two tunnel diodes in series would switch at 1 ma with a composite $V_{fp} = 1$ v. Due to slight individual differences, no two tunnel diodes will switch at exactly the same point, but the difference is negligible in this high speed circuit.

Logic level translators 1, 2, and 3 perform the function of changing a -5.8v "1" to a +1.7v "1", and a -1.1v "0" to a +0.7v "0". Upon receipt of a -1.1v "0" input, the tunnel diodes will be back-biased and they will be in the low voltage state. Thus the collector potential will be held at the potential of the base, which will be approximately +0.7v, being a grounded emitter silicon transistor. However, upon receipt of a -5.8v "1" input, the 6.2v drop across the zener diode causes tunnel diode current to increase to approximately 1.2 ma, so that they switch to the high voltage state. This causes transistor conduction to decrease, and the collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter voltage, a total of +1.7v.

The inverter circuits change a +1.7v "1" input to a +0.7v "0" output, and vice versa. Again, the output levels are taken from the collector, and the collector potential is equal to the sum of the tunnel diode voltages plus the base-emitter voltage of the silicon transistor. The time required for a transition from one state to the other is approximately 4 nanoseconds.

As shown in figure 1, the two flip-flops are each constructed of two inverter circuits provided with cross-coupled feedback from collector to base. These flip-flops are bistable circuits and are therefore capable of storing information.

The output logic level translator is quite similar to a logical inverter circuit, which is discussed elsewhere. This circuit converts a +0.7v "0" into a -1.1v "0", and a +1.7v "1" into a -5.8v "1". It is capable of driving up to 8 logic cards, all of which may be either AND or OR, or any combination resulting in 8 loads total. The input to this translator consists of the set output of FF 2, ANDed with the output of logic level translator 3. This produces an output pulse width of 62.5 nanoseconds, since the input from the clock slave inverter is a -5.8v "1" for this length of time. There will be a delay of approximately 40 nanoseconds from this input to the resync circuit output.

The grounded emitter transistor is a PNP type CDC C01. The base bias is such that a +0.7v "0" allows it to switch on, producing a -1.1v "0" output, while a +1.7v "1" input causes it to switch off, producing a -5.8v "1" output.

Ground Rules

1. The clock slave inverter input to pin 12 of the C64 card should be phase-shifted to obtain maximum resync speed.
2. The resync circuit may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.
3. There will be a delay of approximately 40 nanoseconds from the clock slave inverter input at pin 10 of the C66 card to the resync circuit output.

CAPACITIVE DELAY

Card Types C67, C68, C69, C70, C71

FUNCTION

The function of a capacitive delay is to provide an interval of time delay between successive logical operations. This is done by regulating the length of time required for a logical "1" to pass through the delay circuit. The delay time for a logical "0" will be approximately one-tenth of the delay time for a logical "1".

The circuits contained on card types C67, C68, C69, C70, and C71 provide delay times ranging from 20 nanoseconds to 40 milliseconds, and are shown in figures 2, 3, 4, 5, and 6. In addition, the delays on card types C68 and C69 may be varied through a range of approximately $\pm 15\%$ by means of the variable resistor R02.

OPERATION, Card Types C67, C70, and C71

A delay circuit configuration is shown in figure 1, with typical waveforms. It consists of a capacitor from the signal line to ground, having a source of charging current through a series resistance with the voltage regulated by a 15v zener diode. The delay time from A to B is the time required to charge the capacitor to the input threshold level of inverter B when the output of inverter A switches to a -5.8v "1".

The charging voltage on all card types except C70 is stabilized at a constant 15 volts by a zener diode. The delay time is therefore proportional only to the RC time constant of the series resistance and the capacitance, and is not affected by small line voltage variations. On card types C68 and C69, the series resistance is variable by means of a 2K potentiometer. This provides a close adjustment of the delay times through a range of approximately $\pm 15\%$.

On all card types except C70, the input to the delay is a 3-way AND, and any unused input is effectively a steady "1". The delay circuits on card types C67 and C71 may drive OR loads only, and the RC time constant resistance also acts as the AND resistance.

The AND input contains FD 1032 silicon diodes having a voltage drop of approximately 0.6v; thus point (1) on figure 1 is always 0.6v more negative than the logic-level input. The voltage across the capacitor is controlled by the level of the input signal. With a -1.1v "0" input, this voltage will be approximately -1.7v. When the input from A switches to a -5.8v "1", the voltage at point (1) approaches -6.4v in an exponential curve according to the rate at which charging current flows into the capacitor. At the threshold level of approximately -3v, inverter B will switch state.

OPERATION, Card Types C68 and C69

The circuit contained on these cards is designed to provide stable delay times of relatively long duration. It consists of a capacitive delay followed by a double inverting network such that the circuit does not produce an over-all logical inversion.

The circuit output characteristics are similar to those of a logic card, and it will drive a maximum of 8 logic card loads. These may be 8 AND loads, 8 OR loads, or any combination up to 8 loads total.

As discussed in the previous section, the delay time is the time required to charge the capacitor to the threshold level of the following inverter when the circuit input switches to the -5.8v "1" level. The threshold level at which the inverter will switch state is approximately -3v, but often varies slightly from card to card. From an examination of the exponential charge curve of the capacitor, it is seen that a small variation of the threshold level will make an appreciable difference in the delay time. This variation can be eliminated by always using the same inverter with a given capacitive delay. Mounting the inverter on the same card ensures that the capacitive delay will always drive the same inverter, and the threshold will remain essentially constant.

As discussed previously, the input logic diodes are high speed devices having a voltage drop of approximately 0.6v. This holds the anode of zener diode CR05 at a potential 0.6v more negative than the logic-level input.

Zener diode CR05 functions as a threshold-setting device. The breakdown voltage of CR05 is approximately 4.9v; thus with its anode held at -6.4v by "1" inputs, CR05 applies approximately 1.3v of forward drive to the base of Q01. As the circuit input goes negative, conduction increases through CR05 and resistor R05. When current flow through R05 reaches approximately 0.36 ma, the negative-going input starts to draw turn-on current from transistor Q01. The input continues moving negative to the -5.8v "1" level, causing Q01 to conduct heavily.

A -1.1v "0" input holds the anode of CR05 at approximately -1.7v. In this state, CR05 does not have sufficient bias to hold it in the zener breakdown region. The base of Q01 is therefore held at a low positive voltage by resistors R05 and R06, and Q01 is cut off.

Base drive for transistor Q02 is taken from the collector of Q01. When -5.8v "1" inputs cause Q01 to conduct heavily, its collector holds the base of Q02 at approximately -0.5v, so that Q02 is in a state of minimum conduction. The collector voltage of Q02 is clamped at approximately -6v by resistors R07, R08, and diode CR06.

The -6v level is applied to the base of Q03 and its emitter is isolated by CR07. Transistor Q03 is connected as an emitter follower, and in this state, it can supply OR current for 8 logic card loads.

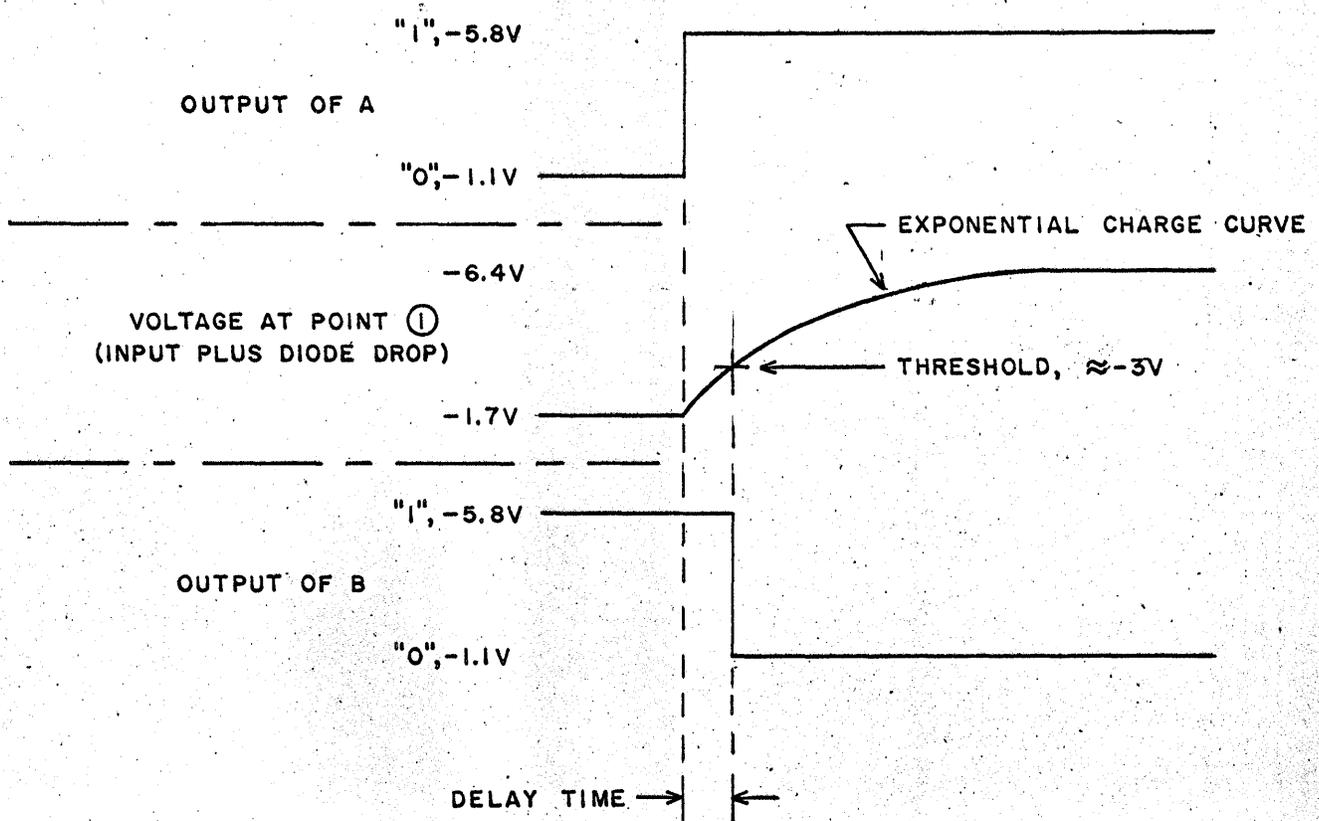
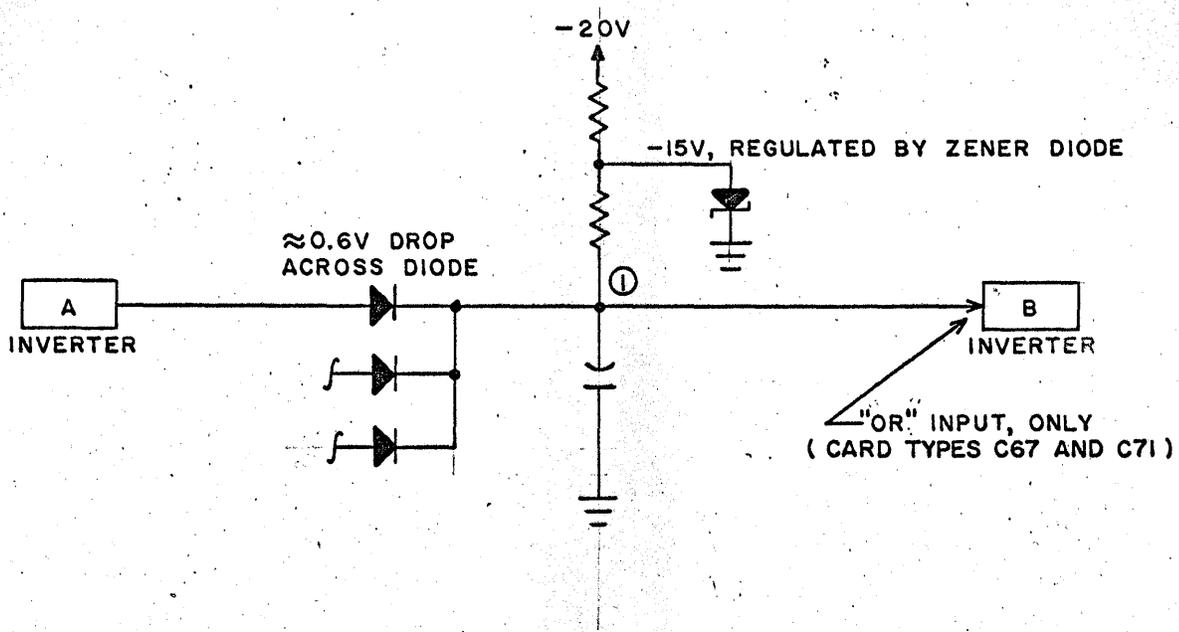
A -1.1v "0" input causes Q01 to cut off and its collector voltage rises toward -20v, causing transistor Q02 to conduct heavily. The collector voltage of Q02 approaches -0.5v, and the circuit output becomes a logical "0". In this state, transistor Q03 is cut off and Q02 can supply AND current for 8 logic card loads.

Positive feedback is provided from the collector of Q02 to the base of Q01 by resistors R05, R06, and capacitor C09. This produces a regenerative effect which speeds the switching action.

GROUND RULES

1. Each delay circuit contained on card types C67 and C71 may drive only one logic circuit.
2. The outputs of delay circuits contained on card types C67 and C71 must always connect to logic circuit OR inputs.
3. The delay circuits contained on card types C68 and C69 may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.
4. The nominal delay times pertain to a logical "1".
5. The delay time for a logical "0" will be approximately one-tenth of the corresponding delay time for a logical "1".

TYPICAL CIRCUIT CONFIGURATION

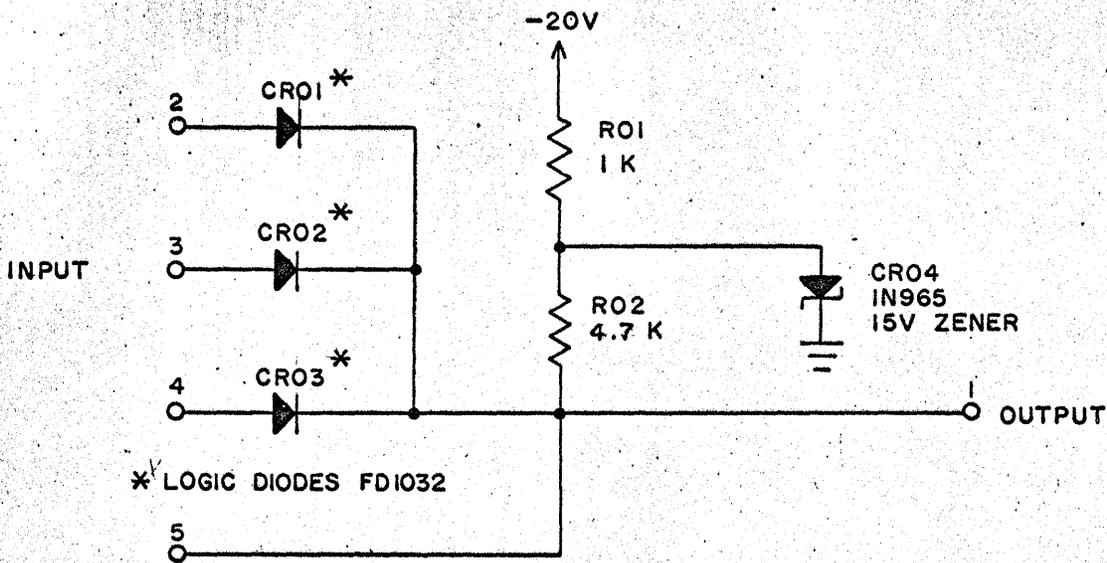


NOTE:

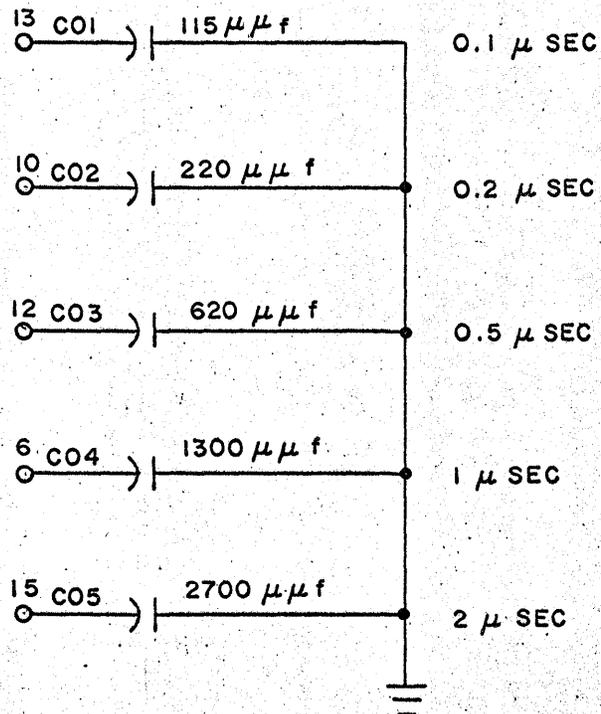
CARD TYPE C70 DOES NOT HAVE A SOURCE OF CHARGING CURRENT.

CAPACITIVE DELAY, FIXED

CARD TYPE C67



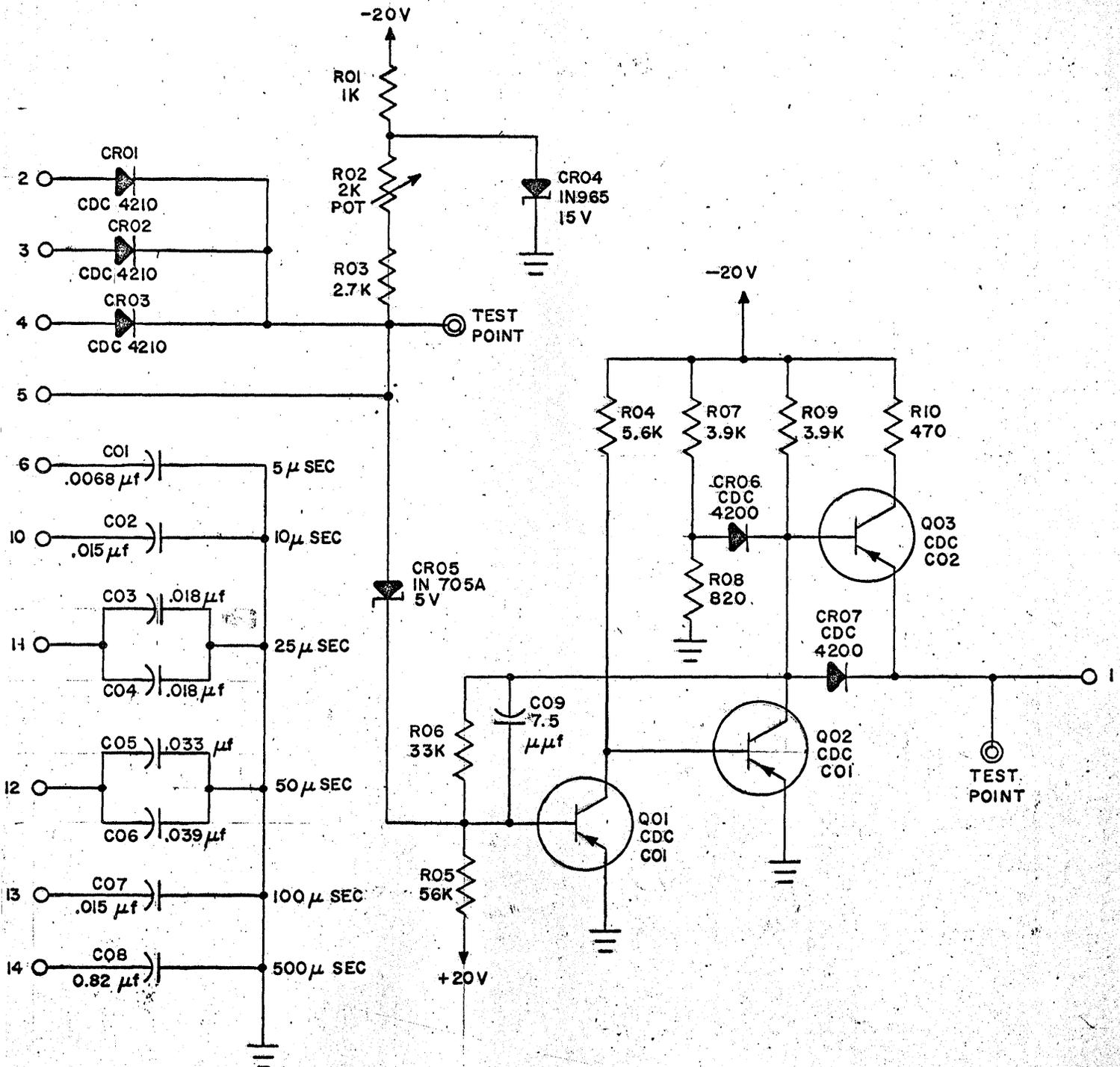
NOMINAL DELAY TIMES



AN EXTERNAL JUMPER CONNECTS PIN 5 TO THE DESIRED DELAY.

CAPACITIVE DELAY, VARIABLE

CARD TYPE C68

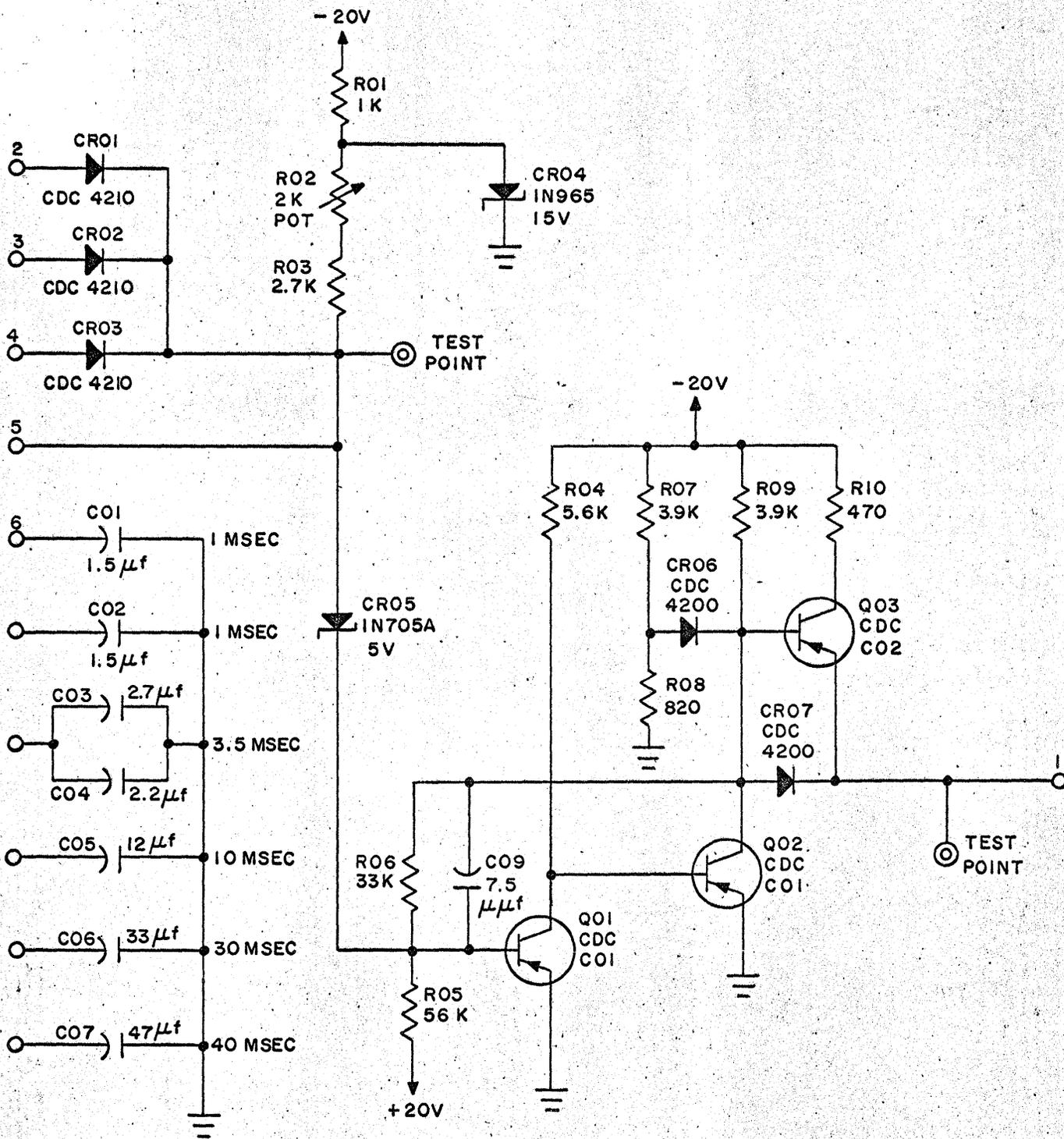


NOTES:

1. EXTERNAL JUMPER CONNECTS PIN 5 TO DESIRED DELAY.
2. NOMINAL DELAY TIMES VARIABLE $\pm 15\%$ BY ADJUSTING R02.
3. THE CIRCUIT DOES NOT PRODUCE AN OVERALL INVERSION.

CAPACITIVE DELAY, VARIABLE

CARD TYPE C69

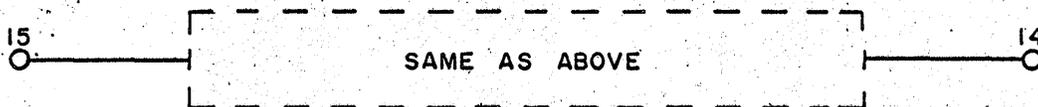
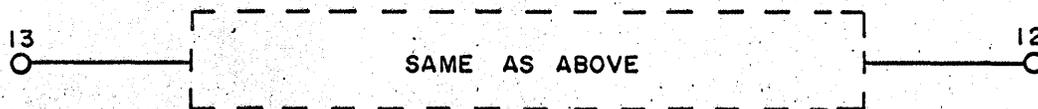
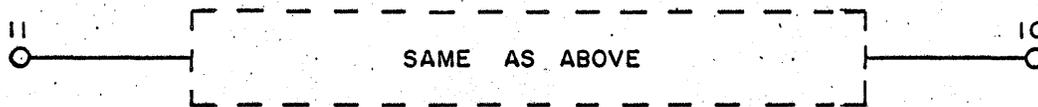
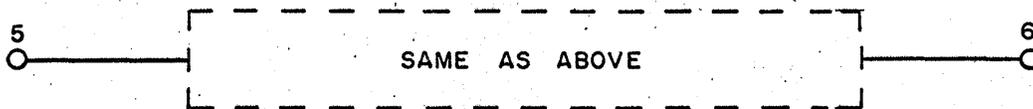
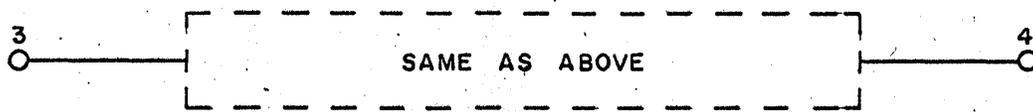
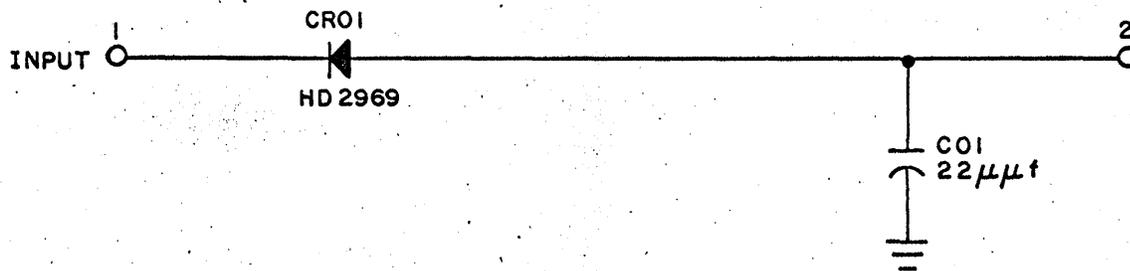


NOTES:

1. EXTERNAL JUMPER CONNECTS PIN 5 TO DESIRED DELAY.
2. NOMINAL DELAY TIMES VARIABLE $\pm 15\%$ BY ADJUSTING R02.
3. THE CIRCUIT DOES NOT PRODUCE AN OVERALL INVERSION.

CAPACITIVE DELAY, 20 nSEC

CARD TYPE C70

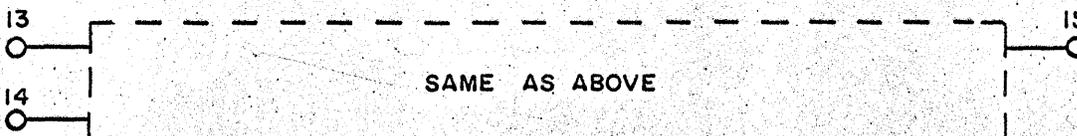
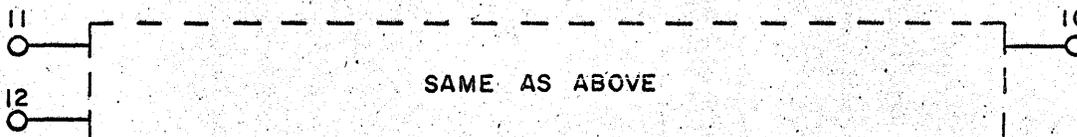
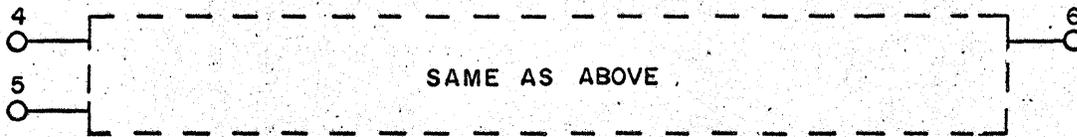
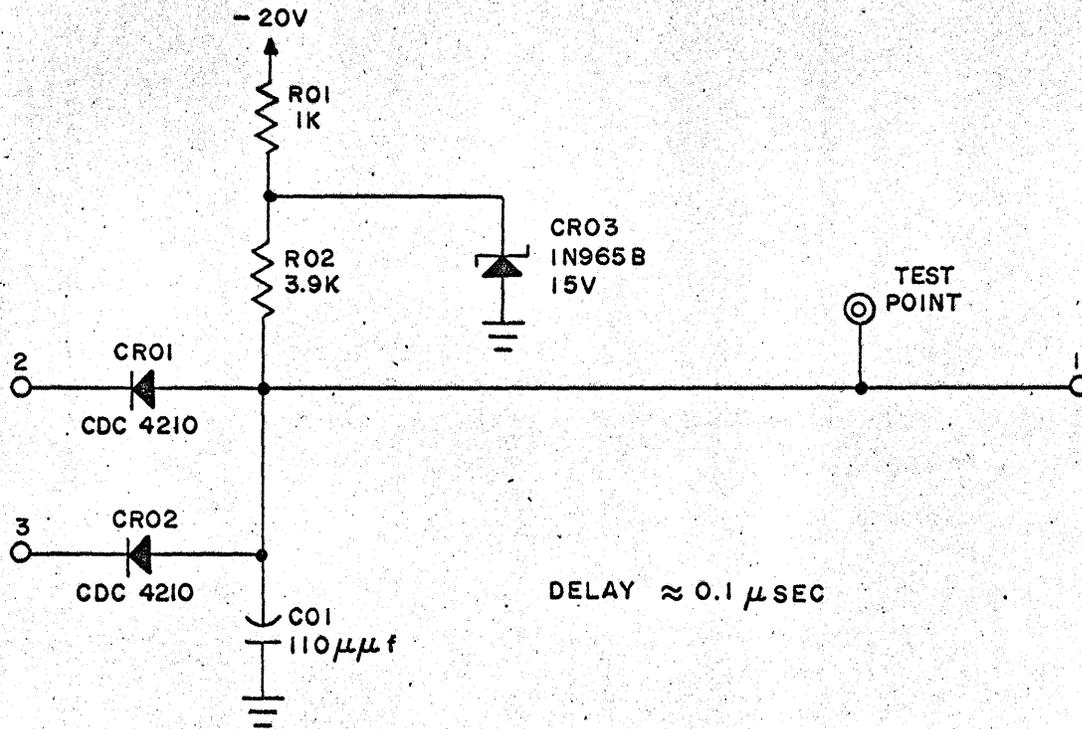


NOTE:

1. 20 NANOSECOND NOMINAL DELAY TIME, MAY VARY ACCORDING TO LOADING.

CAPACITIVE DELAY, 0.1 μ SEC

CARD TYPE C71



MODIFIED M--- INPUT
Card Type C75

FUNCTION

Two identical circuits are contained on this card, the function of which is to enable the 3600 computer system to receive information from a 1604 type input/output cable. This is done by converting the "1" and "0" signal levels from -0.7v and -18v to -5.8v and -1.1v, respectively.

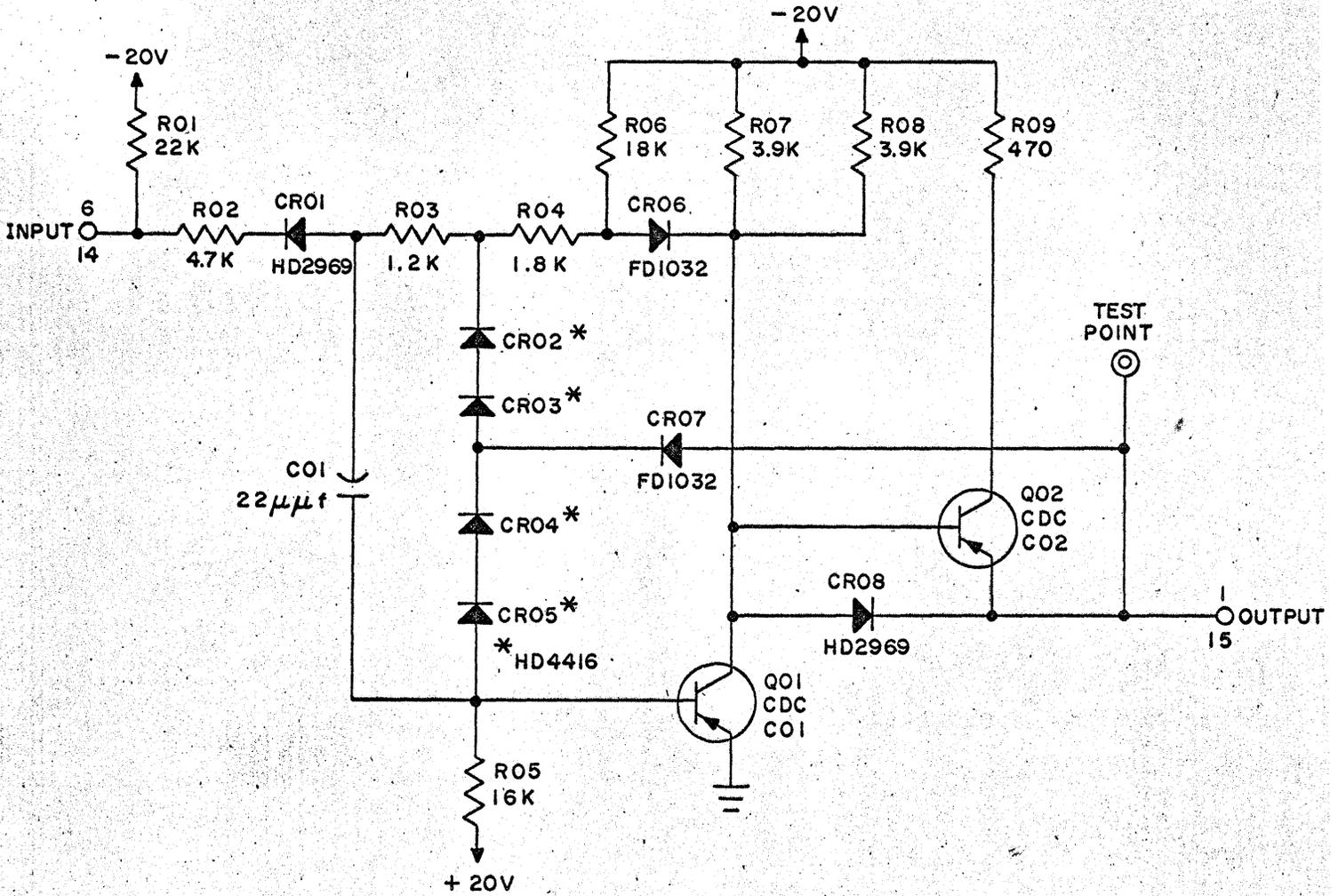
OPERATION

This circuit is essentially a single inverter having one OR input which has been modified by the addition of resistors R01 and R02. These provide a voltage dividing effect, so that a -18v input results in approximately -6v at the cathode of CR01. Similarly, a -0.7v input results in approximately -1v at that point.

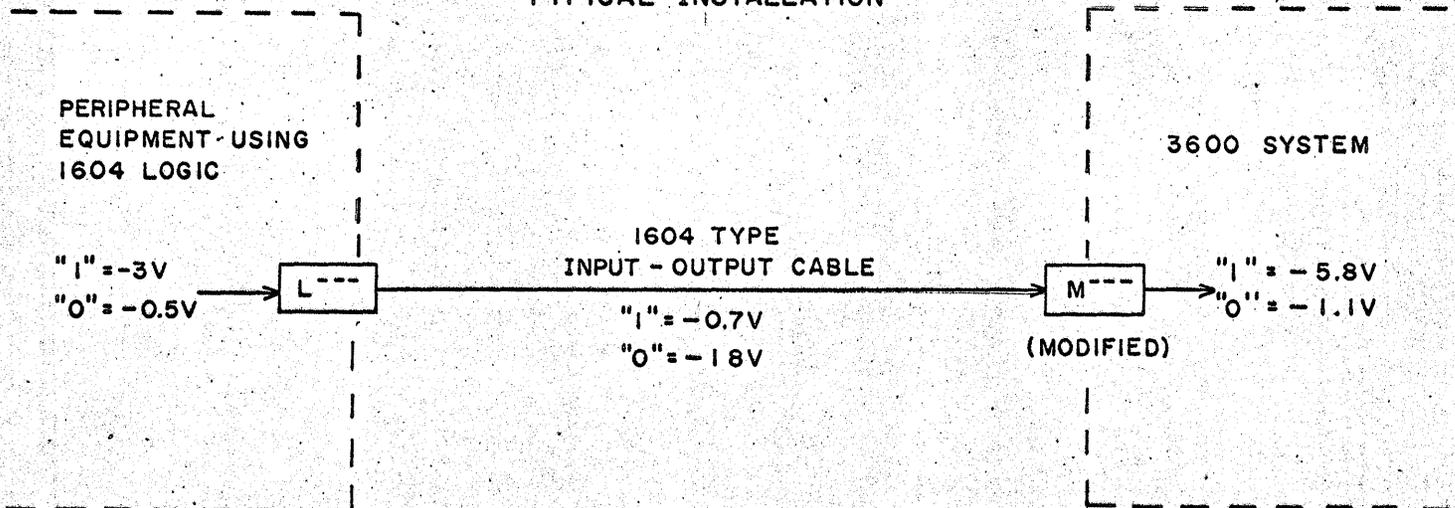
The remainder of the circuit is identical to a single inverter, which is discussed elsewhere. It is capable of driving 8 OR loads, 8 AND loads, or any combination resulting in 8 loads total.

MODIFIED M--- INPUT

CARD TYPE C75
(TWO CIRCUITS PER CARD)



TYPICAL INSTALLATION



MODIFIED L⁻⁻⁻ OUTPUT Card Type C76

GENERAL

Two identical circuits are contained on this card, the function of which is to enable the 3600 computer system to transmit information to peripheral equipment containing 1604 type logic. This is done by converting "1" and "0" levels from -5.8v and -1.1v to approximately -0.7v and -18v, which are the signal levels transmitted over a 1604 input/output cable. An M⁻⁻⁻ card in the peripheral equipment converts these signals to -3v and -0.5v, which respectively represent "1" and "0" in the 1604 type logic.

MODIFICATIONS

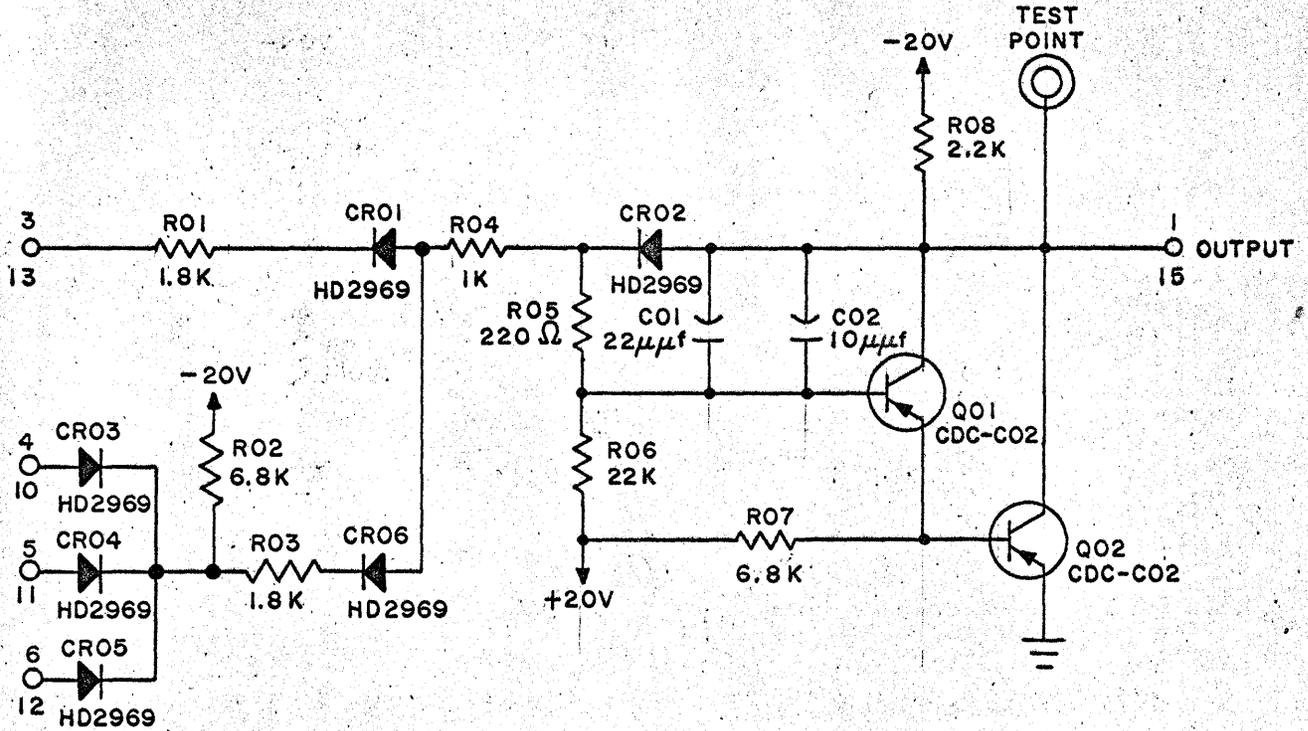
The modified L⁻⁻⁻ circuit shown in figure 1 is quite similar to one of the circuits contained on the 1604 card type 62. It has been modified through the use of CDC C02 transistors, reduction of the Miller feedback capacitance to 32 uuf, and the addition of 1.8 K resistors in the input networks. This enables the circuit to accept 3600 logic level inputs, and results in a switching time of approximately 1 usec.

OPERATION

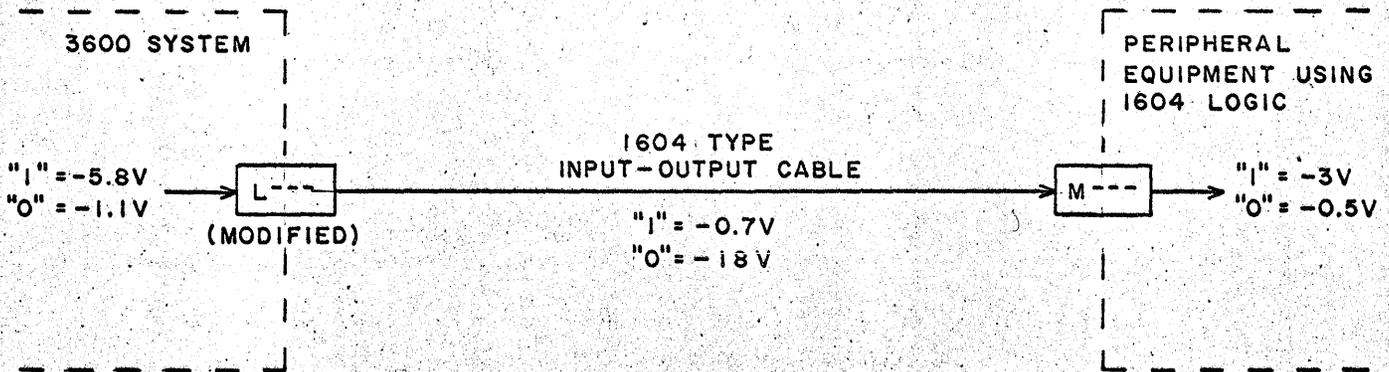
The circuit inputs are a three-way AND and an OR. The threshold level at the cathodes of CR01 and CR06 is approximately -1.5v. Thus as the circuit input becomes more negative, conduction increases from the +20v source through the resistor network. When the circuit input reaches the -3v level, the resulting voltage drop at the base of Q01 will provide sufficient forward bias to the base-emitter junction of transistor Q01, so that it starts to switch to its conduction state.

MODIFIED L--- OUTPUT

CARD TYPE C76
(TWO CIRCUITS PER CARD)



TYPICAL INSTALLATION



The voltage at the base of Q01 is clamped at the sum of the base-emitter junction drops of Q01 and Q02, which is approximately -0.6v. Thus, as the input goes negative, the voltage across R06 will be clamped at approximately 19.4v so that the current through it does not increase beyond approximately 0.9 ma. Therefore, as the input becomes more negative, turn-on current will be drawn through transistors Q01 and Q02. This action begins when the input reaches approximately -3v, and as the input continues moving negative to the -5.8v "1" level, Q01 and Q02 switch to a state of heavy conduction.

Transistor Q01 is connected as an emitter follower and Q02 as a grounded emitter stage. Thus when Q01 switches on, Q02 will conduct heavily, providing a low impedance path from ground to the circuit output. The transistors are clamped out of saturation by diode CR02, but their collector potential will be approximately -0.7v when both are in the conduction state.

A positive-going input causes transistor drive current to decrease, and when the input becomes more positive than -3v, the transistors switch off. The transistors in this state are quite far into the cut-off region, and the circuit output approaches -18v.

The switching time of the circuit is approximately 1 usec. The limiting factor is the 32 uuf of Miller feedback capacitance, which effectively slows the response of Q01.

PRIORITY CIRCUIT

Card Types C77, C78, C79

GENERAL

The priority circuit shown in figure 1 is contained on three printed circuit cards, the type numbers being C77, C78, and C79. The logical operation of this circuit is presented in figure 3, and a timing diagram is shown in figure 2.

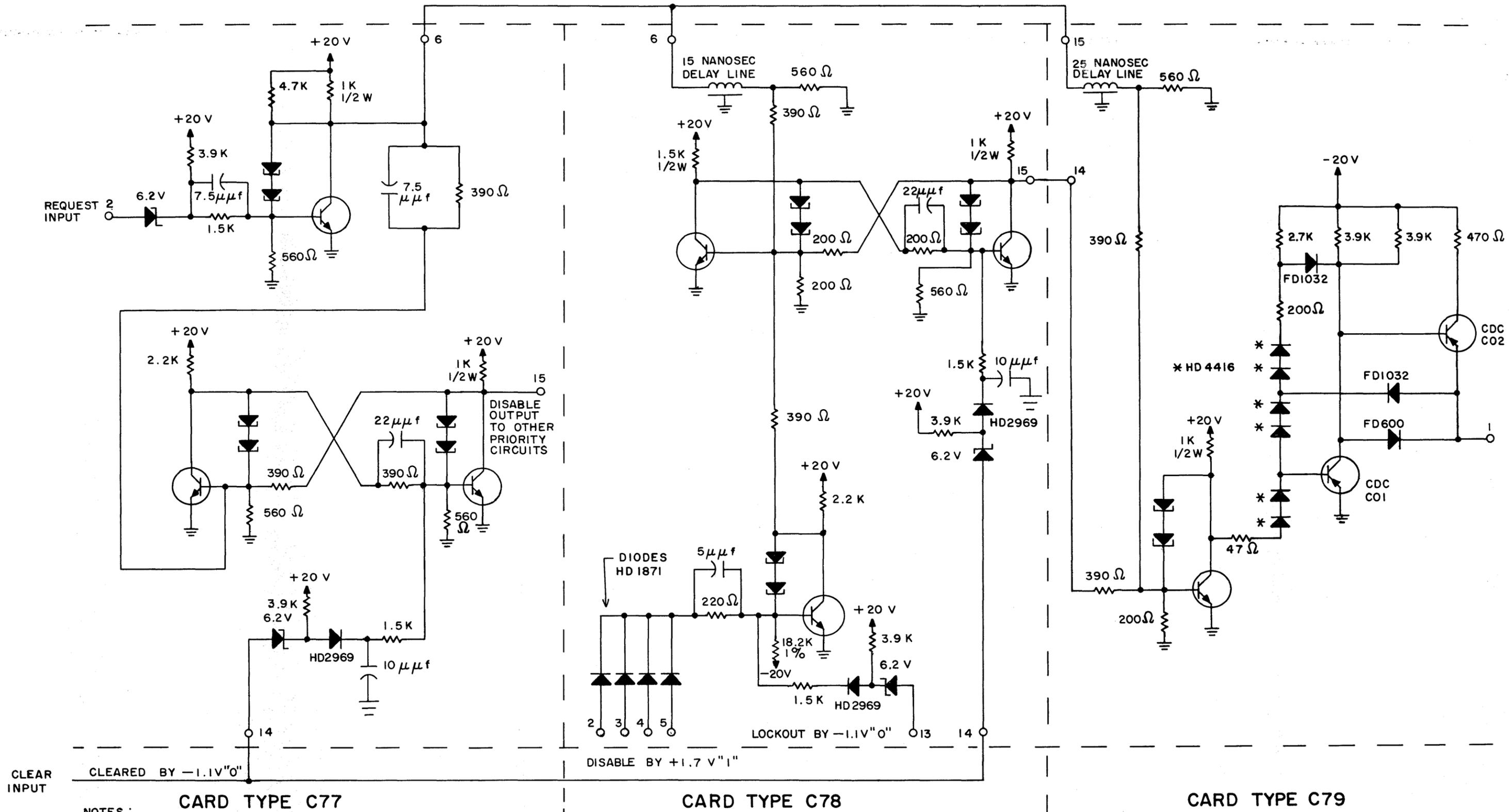
The function of the priority circuit is to enable a storage module to honor its five access channels on a "first-come, first-served" basis, without interference from any other access channel. Priority circuits are contained in the input logic of each of the five access channels, and when one of them receives a "1" input, it disables the priority circuits in the remaining four channels. Thus a request on any of the remaining channels will not be honored until the first channel is released.

The priority circuits will differentiate between access channel requests spaced down to approximately 7 to 8 nanoseconds. Requests arriving more closely than this are considered to have arrived simultaneously, and factors such as supply voltage and wire length will determine which channel is honored. If two requests should arrive simultaneously and all other factors are equal, then neither will be honored.

The delay time through a priority circuit is 30 to 40 nanoseconds. The 20-nanosecond delay line accounts for the majority of this, since the transistor and tunnel diode logic provides a time per inversion of approximately 3 to 4 nanoseconds. A priority circuit timing diagram is presented in figure 3.

Logic levels within the priority circuit are in the positive voltage domain. A "0" is represented by +0.7v and a "1" by +1.7v. The disable signal sent from one priority circuit to the other four is the set output of FF1, and is a +1.7v "1".

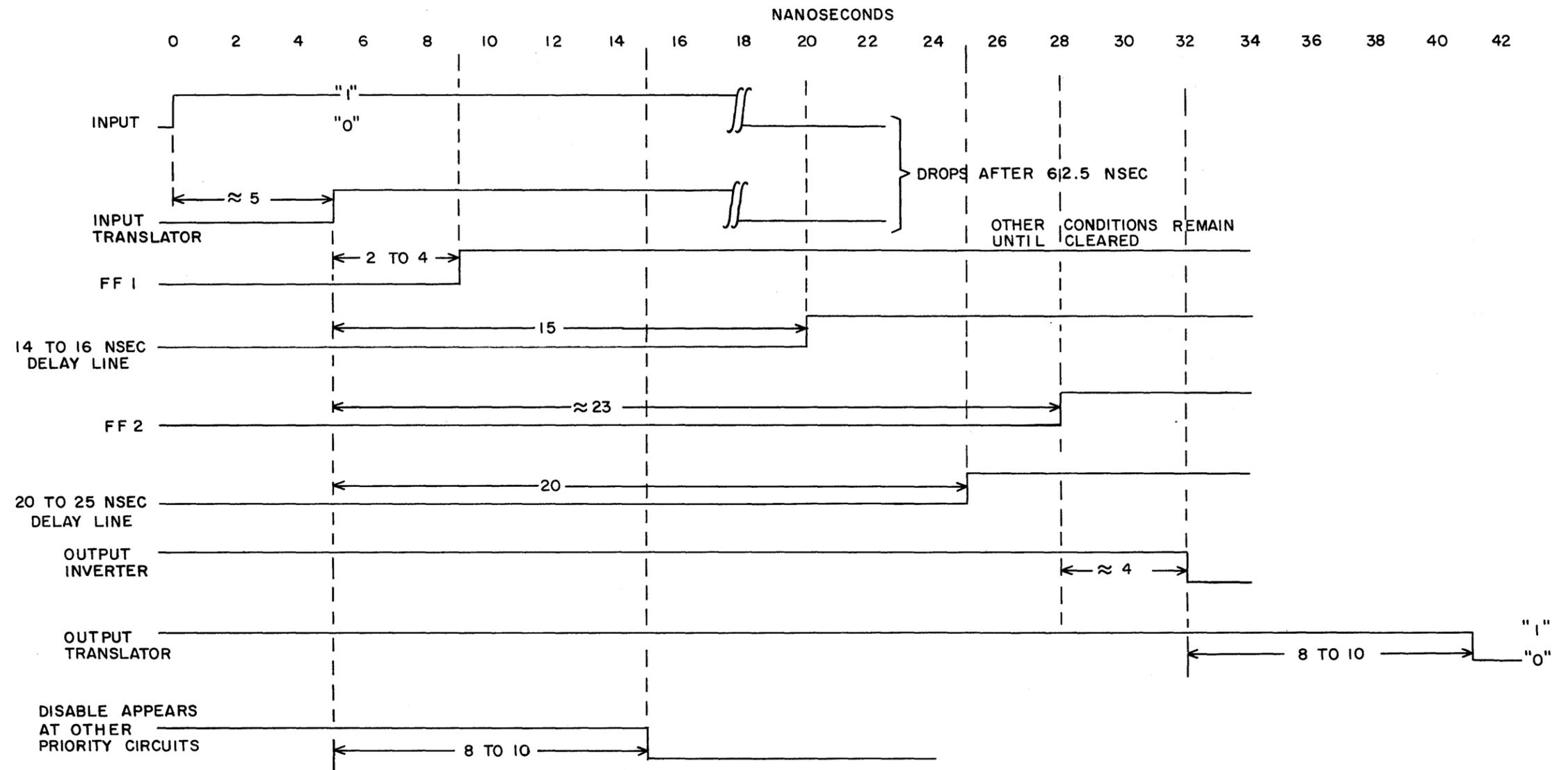
PRIORITY CIRCUIT



NOTES:

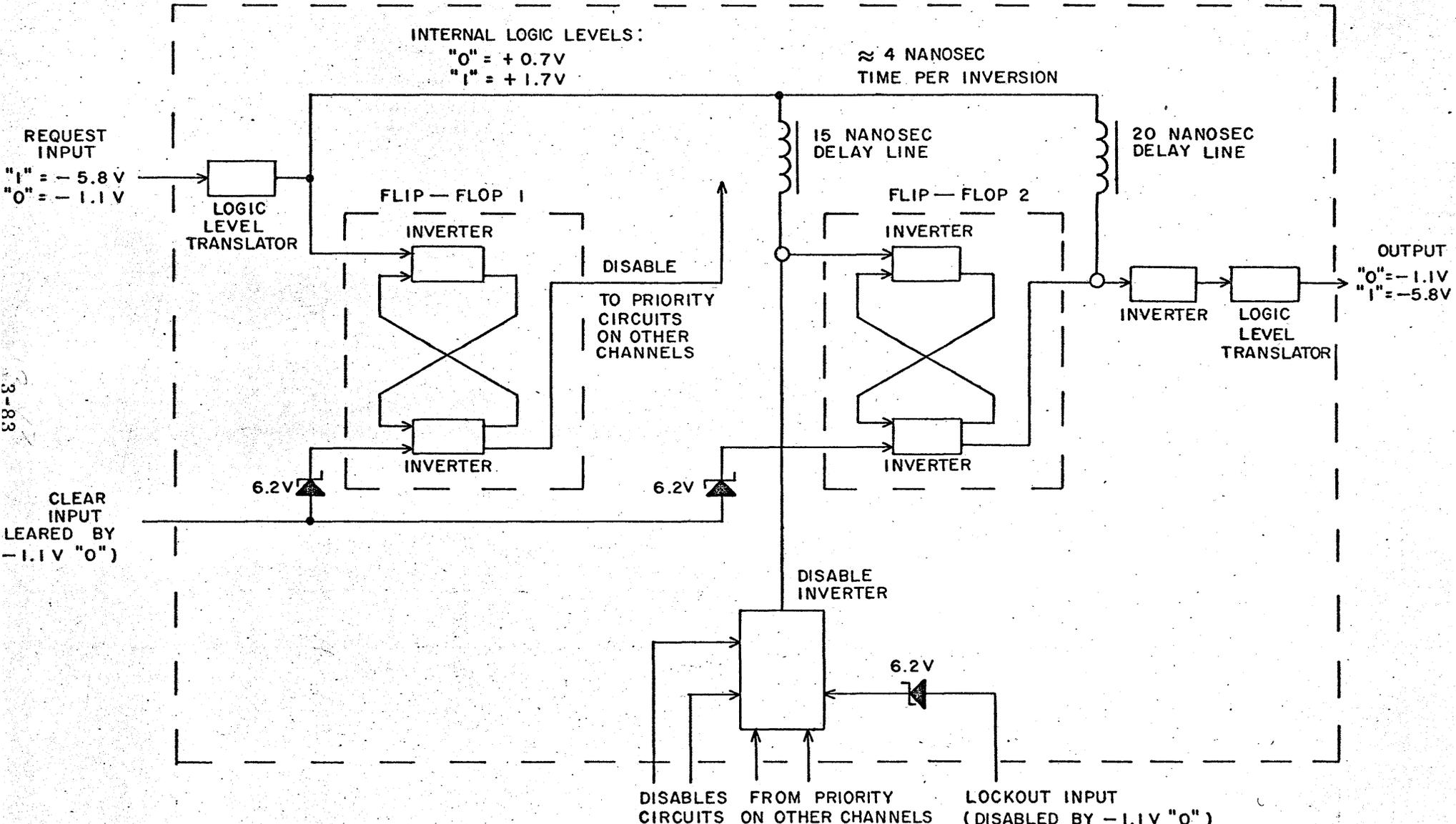
1. ALL TUNNEL DIODES ARE TYPE TD-1.
2. ALL ZENER DIODES ARE TYPE IN753, 6.2 V.
3. ALL TRANSISTORS ARE CDCI321 UNLESS OTHERWISE INDICATED.

PRIORITY CIRCUIT TIMING DIAGRAM



NOTE: OVER-ALL INVERSION BETWEEN INPUT AND OUTPUT

PRIORITY CIRCUIT



NOTE :

CIRCUIT PRODUCES A LOGICAL INVERSION BETWEEN INPUT AND OUTPUT.

3-83

LOGICAL FUNCTIONING

As shown in figure 3, the portions of the priority circuit are: an input logic level translator; flip-flop 1 which produces the signal disabling the other priority circuits; an inverter which disables flip-flop 2 if another access channel has priority; flip-flop 2; an output inverter; and an output logic level translator.

In addition, the priority circuit contains four 6.2v zener diodes, three of which function both as logic level translators and inverters. A -5.8v "1" input to a zener diode becomes a +0.4v output, and a -1.1v "0" input becomes a +5.1v output. These outputs act as "0" and "1", respectively, in the priority circuit logic. The remaining zener diode performs a level-shifting action in the input logic level translator.

A Request signal on an access channel results in a -5.8v "1" input. This signal is 62.5 nanoseconds long, and is repeated every other clock phase time until honored. It is fed into the input logic level translator, which converts it to a +1.7v "1". This sets FF1, which, in turn, disables the other priority circuits.

After a delay of 15 nanoseconds, the "1" will reach the AND into FF2. If a disable input is not being received, the output of the disable inverter will also be a "1", so that FF2 will be set.

Then, after an additional 5-nanosecond delay, the "1" is ANDed with the set output of FF2 into the output inverter, where it becomes a +0.7v "0". This is converted by the output logic level translator to a -1.1v "0". The priority circuit therefore produces a logical inversion between input and output.

As soon as the access channel has been honored, the priority circuit is cleared by a -1.1v "0" input, which is converted by zener diodes to +5.1v, and is applied to the clear inputs of FF1 and FF2. This removes the disable from the other priority circuits so that a request on another channel may be honored.

CIRCUIT OPERATION

As shown in figure 1, except for the transistors in the output logic level translator, all of the priority circuit transistors are CDC 1321. This is a high speed silicon NPN type, having a typical gain bandwidth of 1 kmc, which provides a time per inversion of approximately 2 to 4 nanoseconds, depending upon the loading.

All of the CDC 1321 transistors have a base-to-collector tunnel diode network. This establishes an input current threshold level and holds the output voltages at the sum of the tunnel diode drops and the base-emitter junction drop.

The tunnel diodes used are type TD-1. This is an axial tunnel diode having an $I_p = 1$ ma and a $V_{fp} = 500$ mv. Assuming an ideal case, two tunnel diodes in series would switch at 1 ma with a composite $V_{fp} = 1$ v. Due to slight individual differences, no two tunnel diodes will ever switch at exactly the same point, but the difference is negligible in this high speed circuit.

The input logic level translator performs the function of changing a -5.8 v "1" into a $+1.7$ v "1", and a -1.1 v "0" to a $+0.7$ v "0". Upon receipt of a -1.1 v "0" input, the tunnel diodes will be back-biased and they will be in the low voltage state. Thus the collector potential will be held at the potential of the base, which will be approximately $+0.7$ v, being a grounded emitter silicon transistor. However, a -5.8 v "1" input causes tunnel diode current to increase to a value

in excess of 1ma, so that they switch to the high voltage state. This causes transistor conduction to decrease, and the collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter voltage, a total of +1.7v.

The disable inverter and the output inverter circuits are for the purpose of changing a +1.7v "1" to a +0.7v "0", and vice versa. In addition, the disable inverter also changes the +5.1v signal received through the zener diode to a +0.7v "0". Again, the output levels are taken from the collector, and the collector potential is equal to the sum of the tunnel diode voltages plus the base-emitter voltage of the silicon transistor. The time required for a transition from one state to the other is approximately 4 nanoseconds.

The amount of speed-up capacitance used on inverters of this type is dependent upon the particular input. A single OR input may have a fairly large speed-up capacitor; however, the speed-up capacitance on the OR inputs to the disable inverter must be kept small. This is because FF 1 on each priority circuit must drive four disable inverter inputs and will be loaded too heavily if too much speed-up capacitance is used. Also, the speed-up capacitance on AND inputs must be small in order to prevent runt pulses and partial enables from satisfying the AND.

As shown in figure 1, the two flip-flops are each constructed of two inverter circuits provided with cross-coupled feedback from collector to base. These flip-flops are bistable circuits and are therefore capable of storing information.

The output logic level translator is quite similar to a logical inverter circuit, which is discussed elsewhere. This circuit converts a +0.7v "0" to a -1.1v "0", and a +1.7v "1" to a -5.8v "1". It is capable of driving up to 8 logic cards, all of which may be either AND or OR, or any combination resulting in 8 loads total. The grounded emitter transistor is a PNP type CDC C01.

The base bias is such that a +0.7v input allows it to switch on, producing a -1.1v "0" output, while a +1.7v input causes it to switch off, producing a -5.8v "1" output.

Ground Rules

1. The priority circuit may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.
2. Lead length from FF 1 to the disable inverters on the other priority circuits must be less than 5 inches.
3. Only one priority circuit may be cleared by any one inverter, because a priority circuit requires approximately 15 ma of current for clearing.
4. One inverter may drive the lockout inputs of 4 priority circuits, because a lockout input requires approximately 4 ma.

DELAY LINE, 1 USEC

Card Type C80

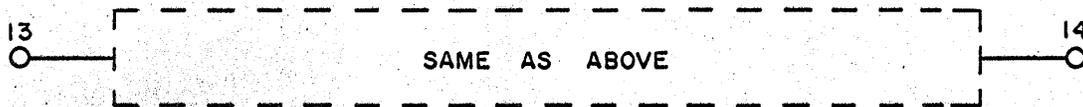
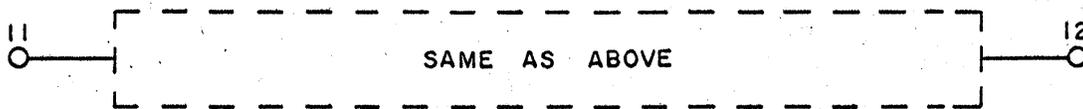
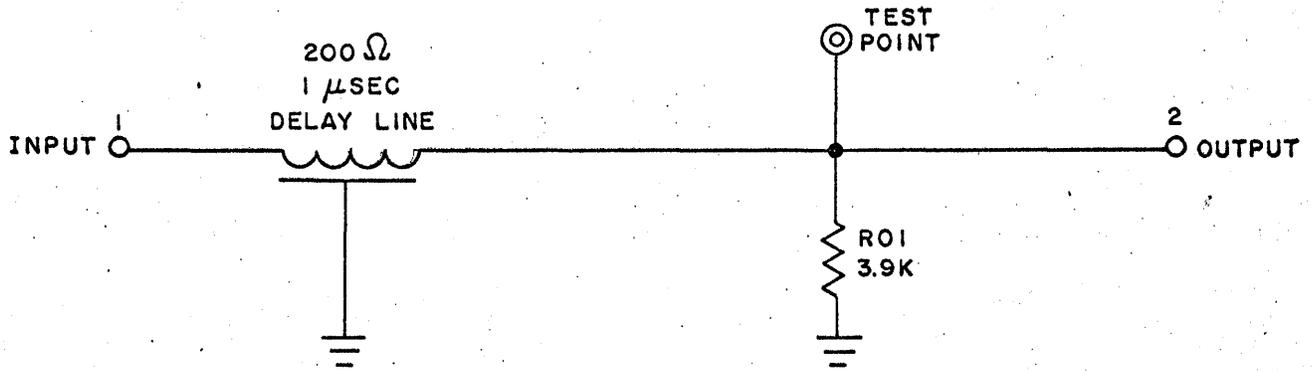
The function of this circuit is to provide an interval of time delay between successive logical operations. It is designed for use in applications requiring greater stability than may be obtained from capacitive delays.

The nominal 1 usec delay time applies to both "1's" and "0's", and the delay may be used to drive either an AND or an OR input. Attenuation through the delay line is negligible.

The characteristic impedance of the delay line is 200 ohms. The purpose of resistor R01 is to provide better impedance matching between the logic circuit input and the delay line output.

DELAY LINE, 1 μ SEC

CARD TYPE C80



NOTE:

1. EACH DELAY MAY DRIVE ONE LOGIC CIRCUIT USING EITHER AN "AND" OR AN "OR" INPUT.

CRYSTAL OSCILLATOR

Card Type C81, 30 kc
Card Type C82, 83.4 kc

FUNCTION

The function of these circuits is to produce accurately timed signals for controlling the Write operation in magnetic tape equipment. Information may be written on tape at rates of either 30,000 (Low Density) or 83,400 (High Density) characters per second. A single-phase sine wave output is taken from the oscillator tank and is converted by the circuit contained on card type C89 into a chain of square pulses at logic voltage levels.

OPERATION

The circuit is essentially a Colpitts oscillator having a crystal filtered power amplifier. Opposite-phase outputs are taken from the oscillator tank and are available at pins 1 and 2 of the printed circuit card. Each output is a sine wave about ground; however, the peak-to-peak amplitude of the output at pin 2 is approximately 3 volts while that at pin 1 is approximately 0.5v.

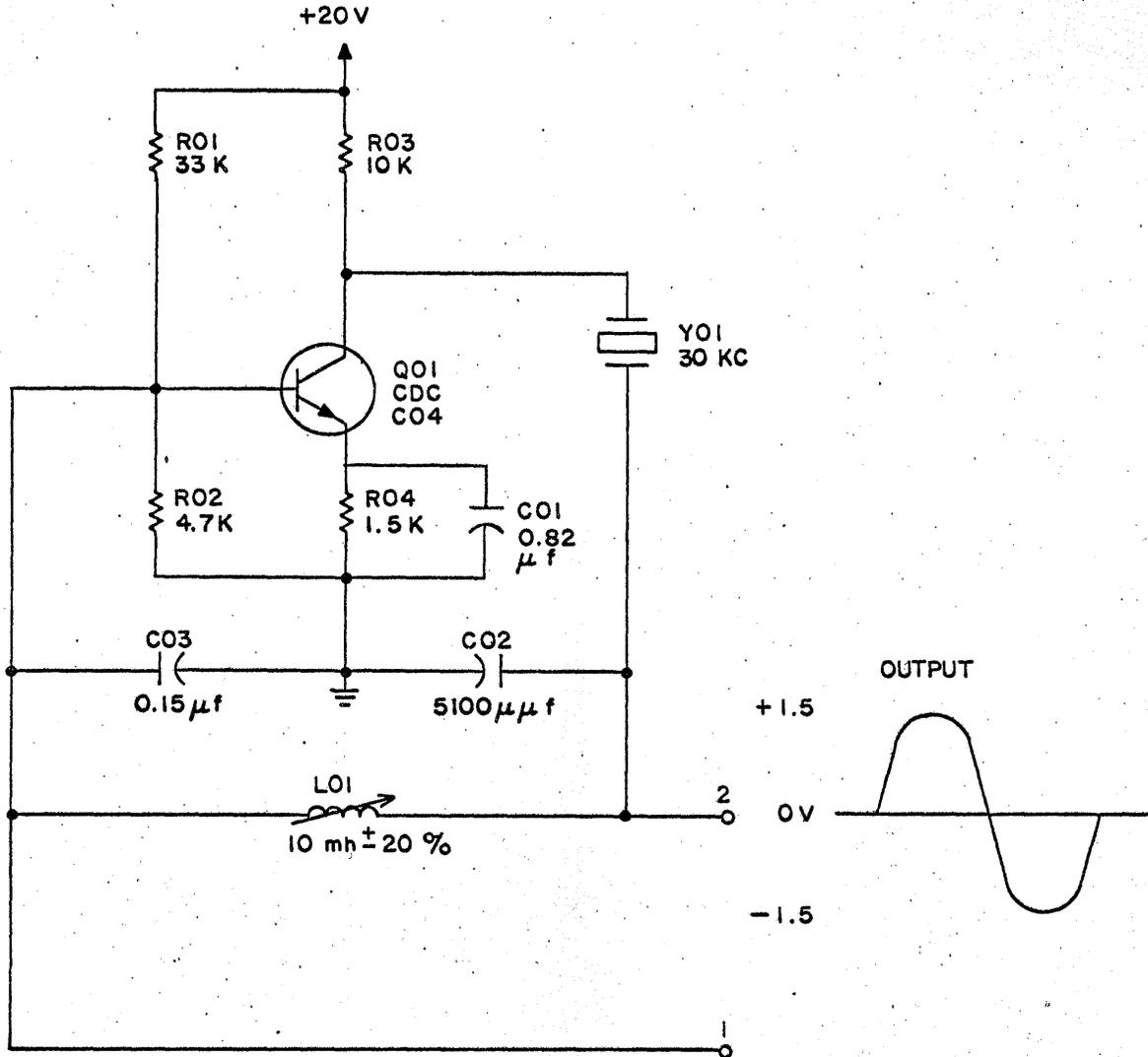
Sufficient gain to maintain oscillation is provided by transistor Q01, which is connected as a Class C power amplifier. The characteristics of Q01 are listed in the component section; however, it is an NPN silicon transistor capable of providing a current gain greater than 25 with a collector current of 400 ma. Transistor Q01 is driven both into saturation and cut off, so that its collector voltage is approximately a square wave.

The square wave signal from the collector of Q01 is filtered by the crystal filter Y01 into a sine wave at the fundamental frequency. Y01 is a high impedance quartz crystal having a Q value of the order of 10^5 . It exhibits a frequency stability of 0.005% over the range $25^{\circ}\text{C} \pm 35^{\circ}\text{C}$, and a long-term stability with time of 1 ppm per week.

The oscillator tank consists of capacitors C02, C03, and the inductance L01. The values of these components are shown in the accompanying diagrams. Inductance L01 is adjustable through a range of approximately $\pm 20\%$, so that the tank may be tuned to the center frequency of the crystal.

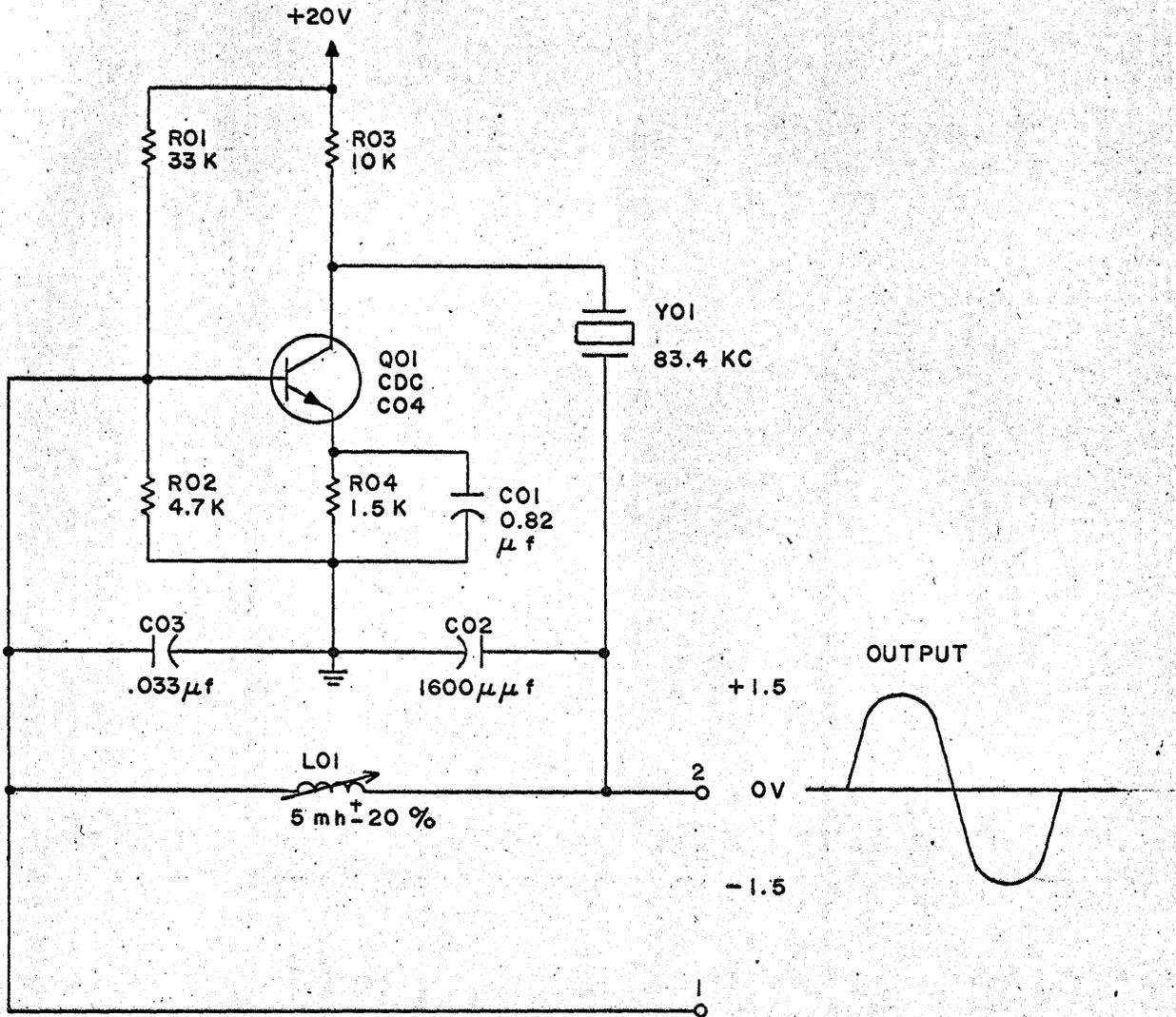
CRYSTAL OSCILLATOR, 30 KC

CARD TYPE C81



CRYSTAL OSCILLATOR, 83.4 KC

CARD TYPE C82



RELAY DRIVER

Card Type C84

FUNCTION

The function of this circuit is to enable a low impedance path from ground to the circuit output, upon receipt of a -5.8v "1" input. The circuit is designed to switch a current of the order of 1 ampere flowing in a highly inductive load such as a relay coil. A diode clamp connection is provided at the collector of Q02, so that a high-voltage inductive transient induced when current is interrupted will not damage the transistor.

OPERATION

The two circuits on the card are identical and are labeled A and B. The following discussion applies to either circuit, but the component numbers mentioned are those appearing in circuit A.

The circuit has one logical OR input, and a 3-way AND. An unused OR input will have no effect on the circuit, while an unused AND input, if left open, will act as a steady "1". Thus if the entire AND group is unused, at least one pin must be grounded.

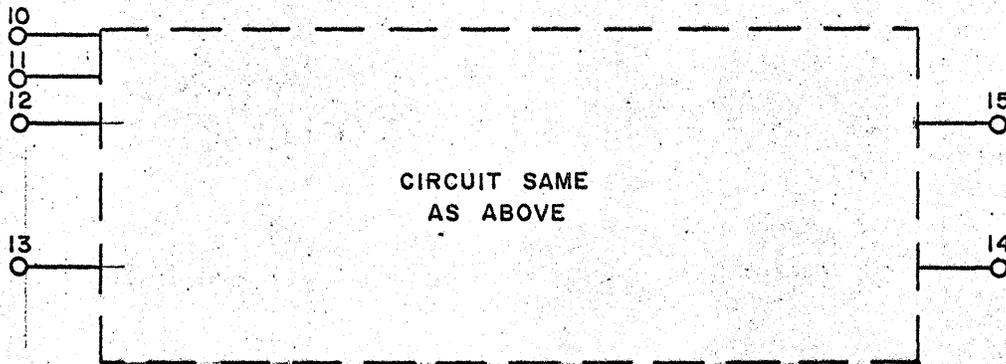
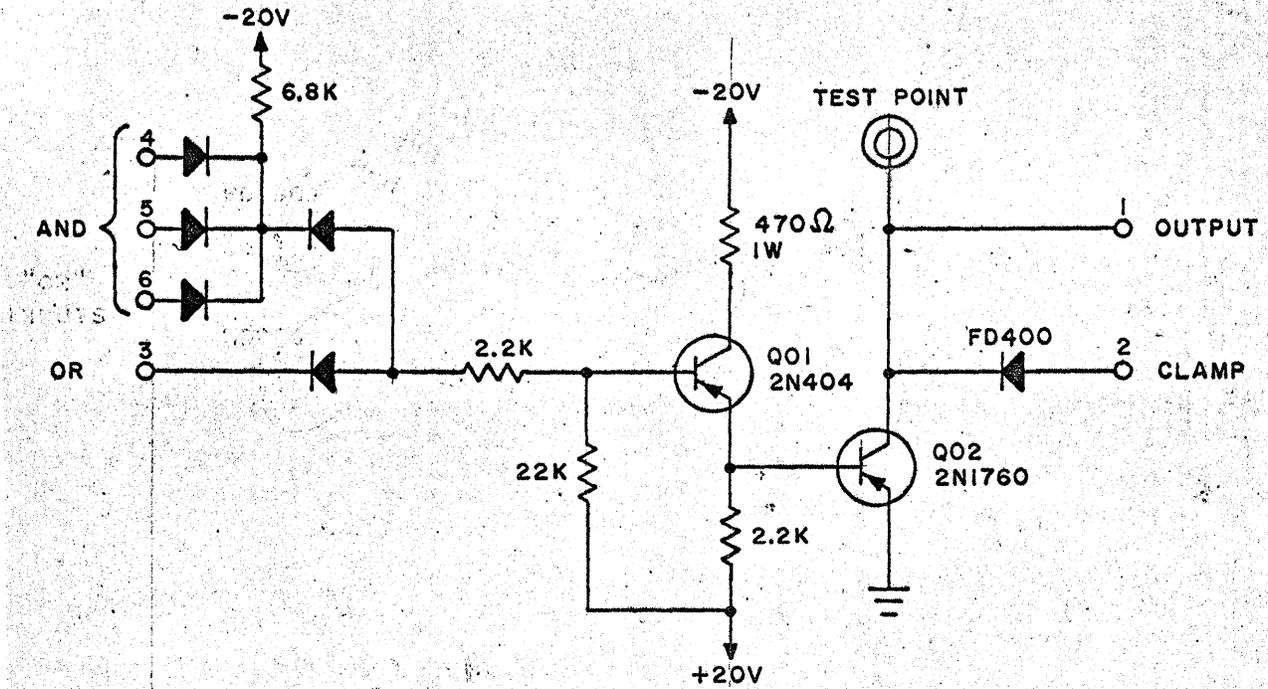
Transistor Q01 is a 2N 404 and Q02 is a 2N 1760. Both are PNP germanium, and their characteristics are listed in the component section.

A -1.1v "0" input holds the base of Q01 at a low negative voltage with respect to the emitter, so that Q01 conducts relatively little. However, a -5.8v "1" input results in a base current sufficiently large so that Q01 conducts heavily.

Transistor Q02 is a grounded emitter stage driven by the emitter follower Q01. When Q01 switches on, it attempts to bias the base of Q02 well into the negative voltage region, so that Q02 also switches on and conducts heavily. Likewise, when Q01 switches off, Q02 also switches off and the positive voltage source applies a reverse bias to the base-emitter junction of Q02 so that it is well into the cut off region.

RELAY DRIVER

CARD TYPE C84



- NOTE: 1. A -5.8V "1" INPUT CAUSES TRANSISTORS TO SWITCH TO CONDUCTION STATE.
2. LOGIC DIODES ARE HD 2969.

GROUND RULES

- 1) Any inductive load must be by-passed by the clamp diode.
- 2) The power supply voltage which drives the load must not exceed 40 volts.
- 3) With a 40v supply, load current can not exceed 0.5 ampere; with a 20v supply, load current can not exceed 1 ampere.
- 4) In case an entire AND group is unused, at least one of the inputs must be grounded.

I/O SENSE AMPLIFIER

Card Type C86

FUNCTION

The function of the circuits on this card is to detect, amplify, and shape the pulse induced in the sense winding when a magnetic memory core switches state during the Read phase of the memory cycle. The pulse produced during the Write portion of the cycle is not detected.

During the rest state, the circuit output is a logical "1" of approximately -5.7v. When a core is read, the output switches to a logical "0" of approximately -0.5v.

The circuits are restricted to driving AND loads, only.

OPERATION

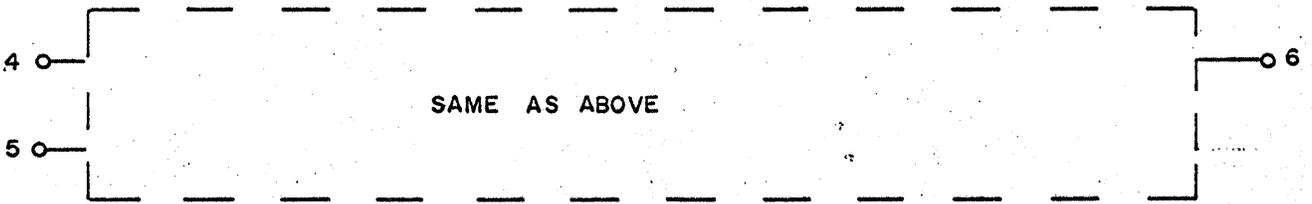
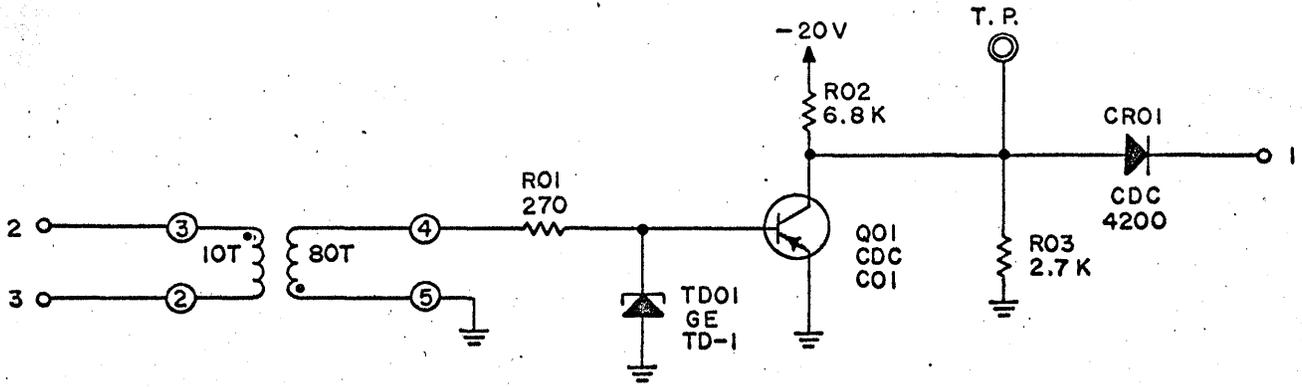
The Sense Amplifier circuit consists of a grounded emitter PNP transistor with a tunnel diode between base and ground. The tunnel diode provides a noise threshold rejection level and results in an essentially square output from the circuit.

In its low-voltage state, the tunnel diode holds transistor Q01 cut off. The circuit output is then produced by the voltage-dividing action of R02 and R03, and stabilizes at approximately -5.7v. The effect of the load is negligible, since the circuit is restricted to driving AND loads, only.

The tunnel diode in its high-voltage state places a forward bias of approximately 0.5v across the base-emitter junction of Q01, causing Q01 to switch on and conduct heavily. The output voltage becomes equal to the collector voltage of Q01 plus the drop across diode CR01, and is approximately -0.5v.

The output produced when a memory core switches state is approximately 0.47 mv. During the Read phase, the core outputs are of a polarity such that pin 4 of the input transformer goes negative. The 0.47 mv input is increased by the 1 : 8 voltage step-up of the input transformer.

I/O SENSE AMPLIFIER CARD TYPE C86



NOTE:

A SENSE AMPLIFIER IS RESTRICTED TO DRIVING
"AND" LOADS, ONLY.

Initially, the tunnel diode is in its low-voltage state and the circuit is providing a "1" output. The tunnel diode remains in its low-voltage state as current through it increases, until it reaches the "peak" of its characteristic curve where I and V are approximately 1 ma and 65 mv, respectively. A slight increase in current puts the tunnel diode in the regenerative region and the voltage increases almost instantaneously to 500 mv. This causes Q01 to conduct and the circuit output switches to "0". The tunnel diode remains in the high-voltage state until current through it decreases to approximately 0.12 ma. This is the characteristic curve "valley", and at this point, the voltage drops almost instantaneously to approximately zero. This cuts off transistor Q01 and the circuit output returns to "1".

I/O MEMORY DRIVER

Card Type C87

FUNCTION

The function of this circuit is to provide drive current to a memory unit upon receipt of a -5.8v "1" input. The output may be either a half-current of approximately 200 ma from pin 15, or a full current of up to 800 ma from pin 14. In order to obtain a maximum current from pin 14, pin 10 must be grounded.

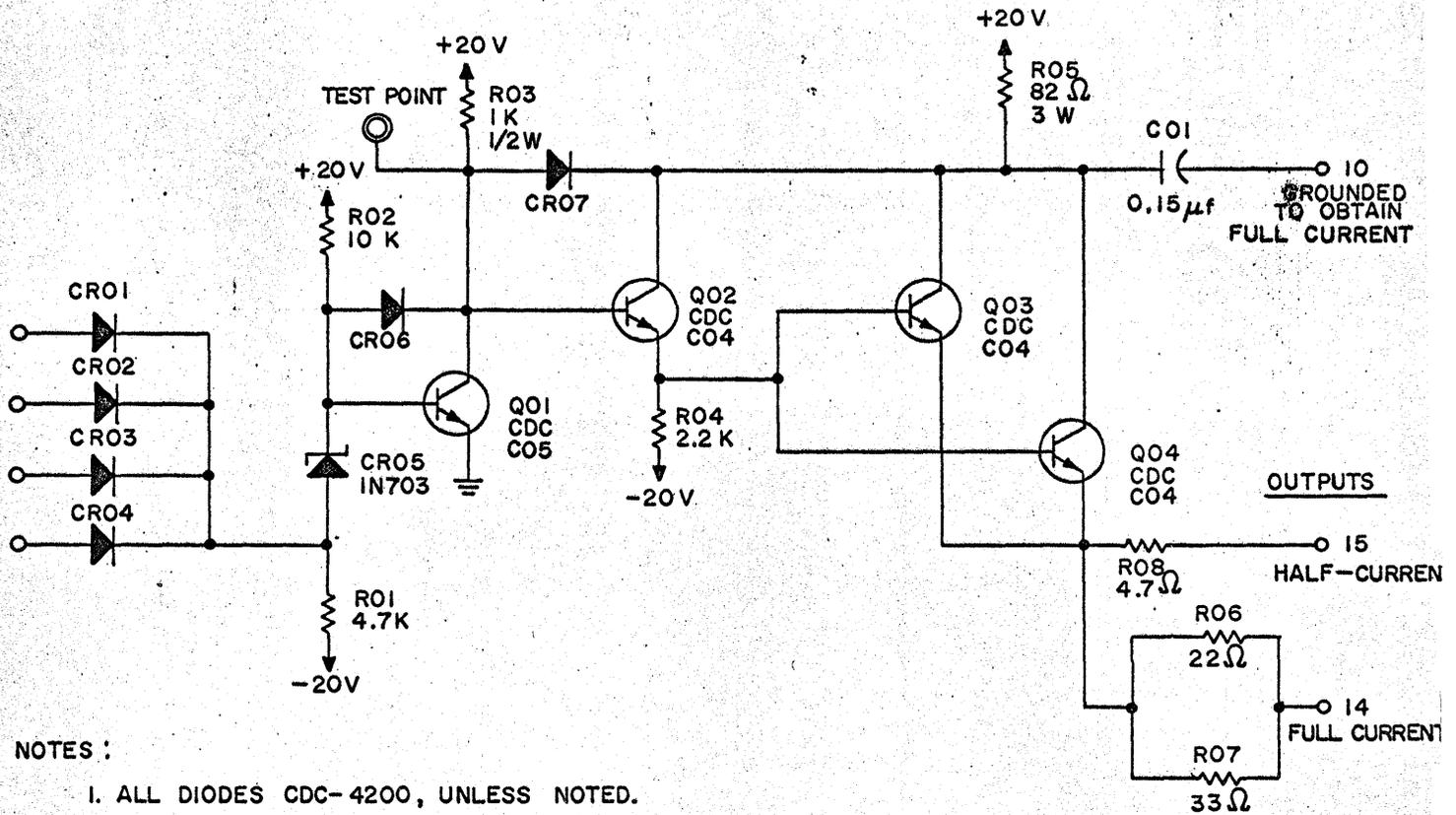
OPERATION

The circuit has a four-way logical AND input, meaning that all inputs must be at the -5.8v "1" level in order for an input to be sensed. A 1.1v "0" on any input will disable the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

An input level-shifting action is provided to the base of Q01 by resistors R01 and R02, and the 3.5v zener diode CR05. The zener diode CR05 is reverse-biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 3.5v positive with respect to the anode, regardless of current fluctuations.

With -1.1v "0" inputs, zener diode CR05 holds the base of Q01 sufficiently positive so that it conducts heavily. Transistor Q01 is held out of deep saturation by CR06, and its collector voltage is approximately +0.5v. The collector voltage of Q01 is applied to the base of Q02, which is connected as an emitter follower. The emitter voltage of Q02 is therefore equal to its base voltage less the base-emitter junction drop, and is approximately -0.1v. The emitter voltage of Q02 is applied to the bases of Q03 and Q04, which are also connected as emitter followers. The emitter circuits of Q03 and Q04 thread the memory plane and terminate at a Diverter circuit; thus the emitter voltage of Q03 and Q04 is approximately +0.9v. The -0.1v input from Q02 therefore back-biases the base-emitter junctions of Q03 and Q04, cutting them off.

I/O MEMORY DRIVER CARD TYPE C87



NOTES :

1. ALL DIODES CDC-4200, UNLESS NOTED.
2. CIRCUIT HAS A FOUR-WAY "AND" INPUT.
3. -5.8V "1's" ON ALL INPUTS CAUSE Q03 AND Q04 TO CONDUCT.

A -5.8v "1" input results in approximately -2.3v at the base of Q01, so that Q01 is cut off. If the circuit is providing a half-current, pin 10 will not be grounded and resistors R05 and R08 limit the current to approximately 200 ma. In addition, the voltage drop across R05 holds the collector voltage of the transistors at a relatively low level. The collector of Q01 rises to approximately +3.5v, providing drive to Q02. The emitter voltage of Q02 becomes approximately +2.9v, causing Q03 and Q04 to switch to the conduction state. Transistor Q02 is held out of deep saturation by CR07, and Q03 and Q04 are held out of deep saturation by the voltage drop across Q02. The emitter voltage of Q03 and Q04 is applied to the drive lines and is approximately +2.2v. The emitter currents of Q03 and Q04 combine to provide the memory drive current.

In order to obtain a peak value of full current from the circuit, pin 10 must be grounded. This allows capacitor C01 to become charged while the circuit is not providing drive current. When transistors Q03 and Q04 switch on, C01 discharges into the drive line, providing an initial high current surge. With Q01 cut off, its collector voltage rises to approximately +19v, providing drive to Q02. The emitter voltage of Q02 rises to approximately +18.4v, causing Q03 and Q04 to switch on and conduct heavily. The voltage applied to the drive lines is the emitter voltage of Q03 and Q04, and is approximately +17.8v during the initial high current surge. As capacitor C01 becomes discharged, the voltage levels within the circuit decrease toward the values given in the preceding paragraph.

I/O MEMORY DIVERTER

Card Type C88

FUNCTION

The function of this circuit is to enable memory drive current to flow from one of the output pins to ground, whenever all inputs are at the logical "0" level of -1.1v. The drive lines are energized with half-currents of 200 ma or full currents of up to 800 ma peak by the circuit contained on a Driver card C87. Each drive line terminates at one of the output pins of a Diverter card, and the circuit is completed to ground allowing current to flow when transistors Q02 and Q03 switch to the conduction state.

OPERATION

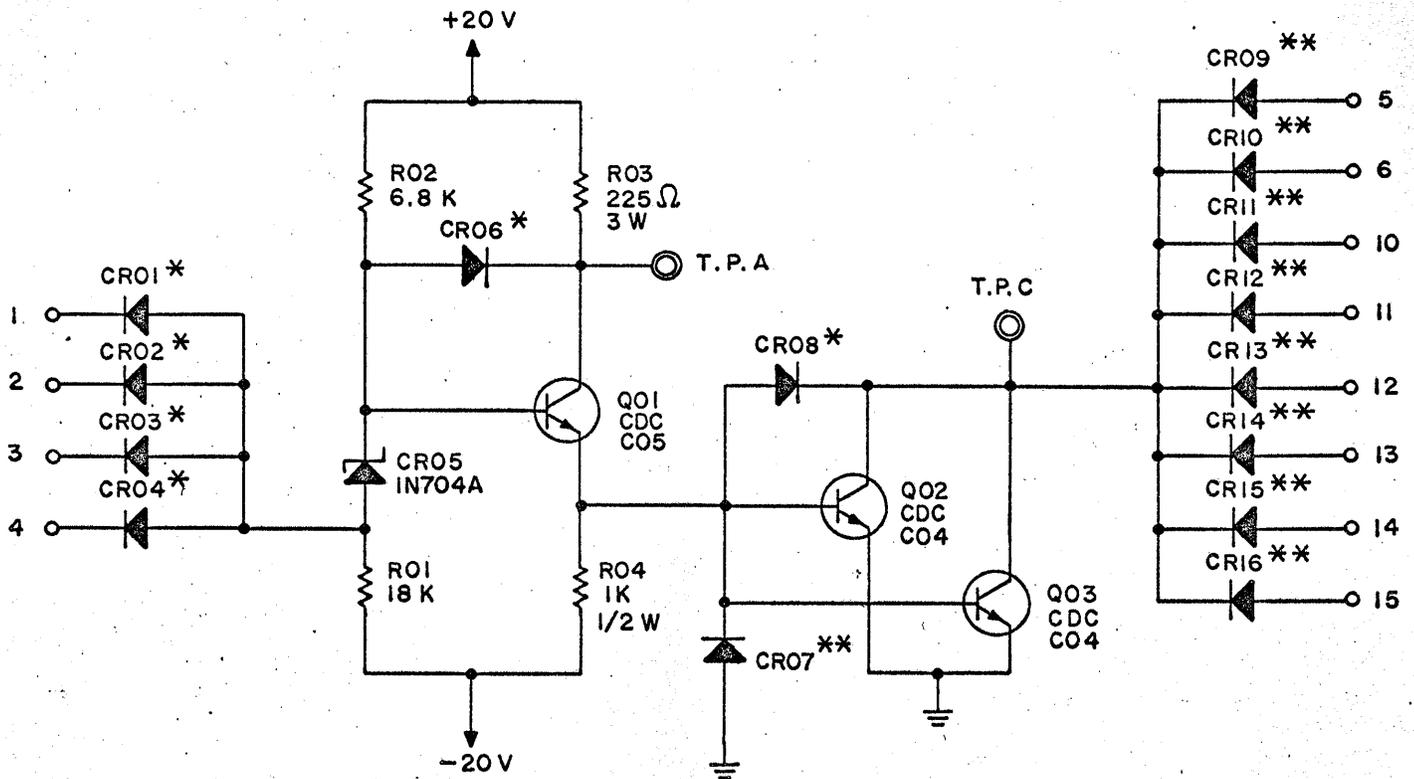
The circuit has four logical OR inputs, and transistors Q02 and Q03 switch to the conduction state only when all inputs are -1.1v "0". A -5.8v "1" on any input holds Q02 and Q03 in the cut off state.

An input level-shifting action is provided to the base of Q01 by resistors R01 and R02, and the 4.1v zener diode CR05. The zener diode CR05 is reverse-biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

A -5.8v "1" input results in approximately -1.5v at the base of Q01. This cuts off Q01, since its emitter is clamped at approximately -0.6v by diode CR07. The bases of Q02 and Q03 are also clamped at approximately -0.6v by diode CR06, and since their emitters are grounded, they are cut off.

If all inputs are at the -1.1v "0" level, zener diode CR05 holds the base of Q01 at approximately +1.4v. This causes Q01 to switch to a state of heavy conduction, but it is held out of deep saturation by diode CR06. Transistor Q01 is connected as an emitter follower; thus its emitter voltage rises to approximately +0.7v, providing drive for Q02 and Q03. The +0.7v input from Q01 causes Q02 and Q03 to switch on and conduct heavily, but they are held out of deep saturation by diode CR08.

I/O MEMORY DIVERTER CARD TYPE C88



* CDC 4200 (HD 2969)

** CDC 4211 (FD 400)

NOTES :

1. CIRCUIT HAS FOUR "OR" INPUTS.
2. TRANSISTORS Q02 AND Q03 SWITCH TO CONDUCTION STATE WHEN ALL INPUTS ARE -1.1V "0".

AMPLIFIER - SHAPER

Card Type C89

FUNCTION

The function of this circuit is to convert the sine wave output of a crystal oscillator into a chain of -5.8v "1" pulses of approximately 0.2 microseconds duration. The input is a sine wave about ground with a peak-to-peak amplitude of approximately 3v. The -5.8v "1" pulse output is produced immediately after the input crosses the zero axis in the positive-going direction.

OPERATION

The width of the output pulse is approximately 0.2 microseconds and is determined by the 220 microhenry inductance L01. The repetition rate of the output is determined by the frequency of the input signal.

The input signal is applied to the base of transistor Q01, which is an NPN silicon type CDC C04. In this application, it is used as an emitter follower current amplifier providing drive current for transistor Q02.

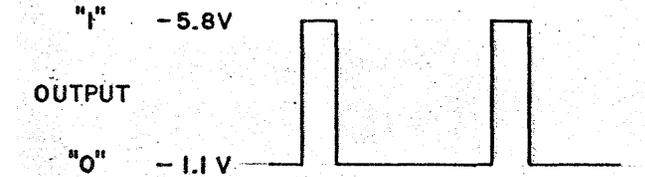
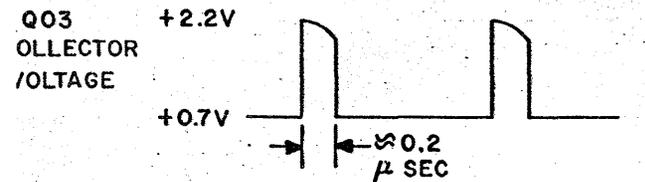
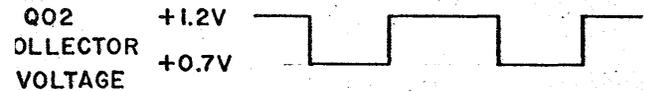
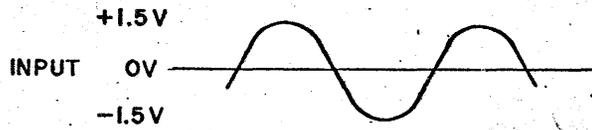
Transistors Q02 and Q03 are CDC 1321, which is a high speed NPN silicon type having a gain-bandwidth of 1 kmc. Each of these transistors has a base to collector tunnel diode network which produces an essentially square waveform and establishes its voltage level.

The tunnel diodes used are type TD-1. This is an axial tunnel diode having an $I_p = 1$ ma and a $V_{fp} = 500$ mv. Assuming an ideal case, the three tunnel diodes connected to Q03 would switch at 1 ma with a composite $V_{fp} = 1.5$ v. Due to slight individual differences, no two tunnel diodes will ever switch at exactly the same point, but the difference is negligible in this high speed application.

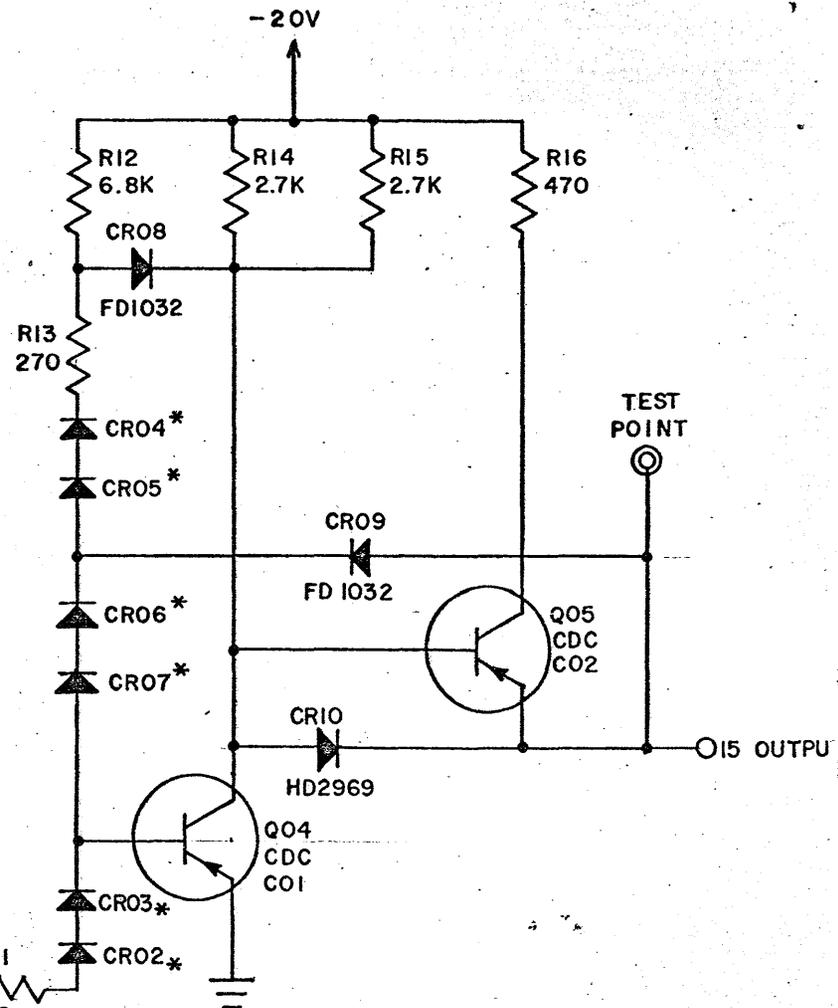
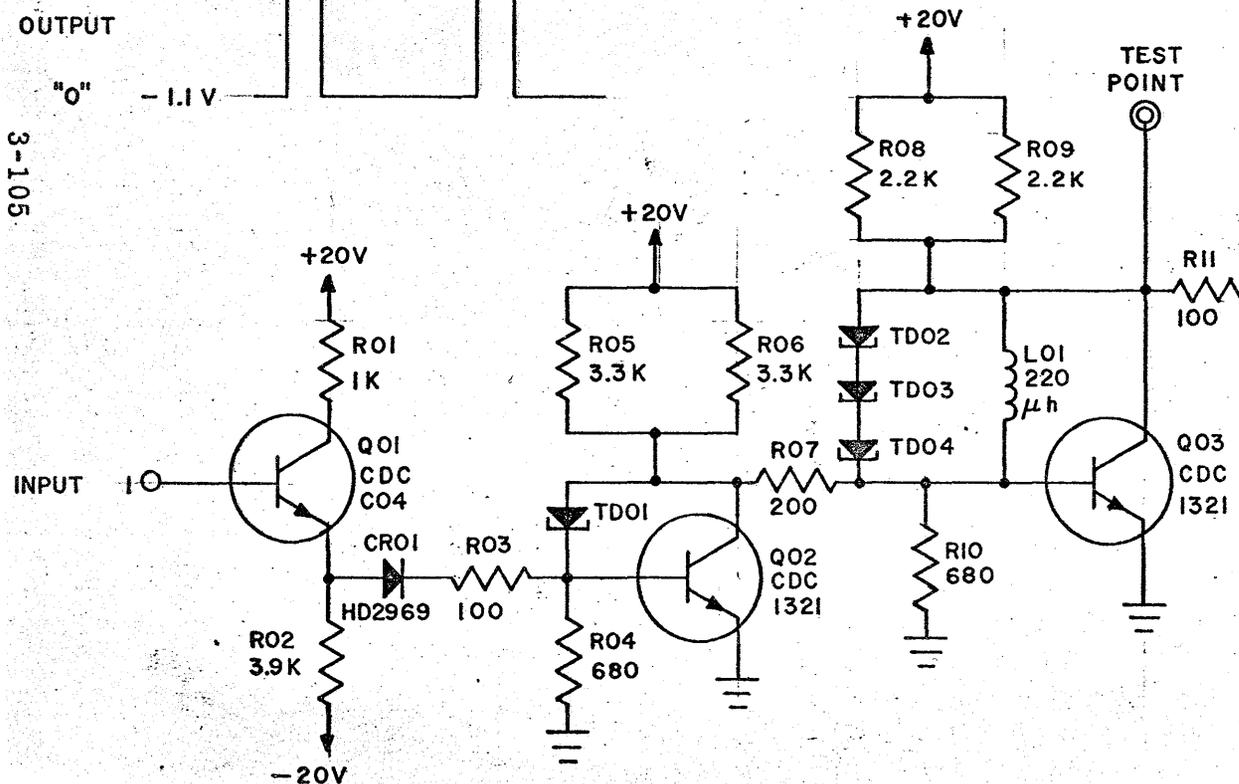
As shown in the accompanying diagram, a positive-going input results in a -5.8v "1" output of approximately 0.2 microseconds duration. As the input goes positive, Q01 provides drive current to Q02 so that it switches to a state of heavy conduction. This results in minimum current flow through TD01 so that it switches

AMPLIFIER SHAPER

CARD TYPE C89



3-105



NOTE:

1. TUNNEL DIODES TD-1
2. * HD 4416

to its low voltage state. The collector voltage of Q02 is therefore approximately equal to its base-emitter junction drop of +0.7v, being a grounded emitter silicon transistor. Transistor Q02 in its conduction state allows current flow to increase through TD02, TD03, and TD04, so that they switch to their high voltage states. This causes conduction through Q03 to decrease, and its collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter junction drop, a total of +2.2v. This voltage level causes Q04 to switch to a state of minimum conduction and the circuit output becomes a -5.8v "1".

The length of the -5.8v "1" output pulse is determined by the 220 microhenry inductance L01. The tunnel diodes are able to switch state almost instantaneously while current through the inductance increases exponentially. After a time of approximately 0.2 microsecond, current through the inductance will have increased to the point that the tunnel diodes are effectively by-passed and they return to their low voltage states. This reduces the collector voltage of Q03 to approximately +0.7v, which causes Q04 to conduct heavily and returns the circuit output to a -1.1v "0".

A negative-going circuit input prevents Q01 from providing drive current to Q02. This allows current through TD01 to increase, causing it to switch to its high voltage state. Conduction through Q02 decreases and its collector voltage becomes equal to the sum of the tunnel diode voltage and the base-emitter junction drop, a total of +1.2v. This provides forward drive to the base of Q03, holding the circuit in the quiescent state.

The portion of the circuit consisting of Q04, Q05, and their associated biasing network is quite similar to a logical inverter, which is discussed elsewhere. It is capable of driving 8 AND loads, 8 OR loads, or any combination resulting in 8 loads total.

I/O EMITTER FOLLOWER

Card Type C90

FUNCTION

The function of the circuits on this card is to convert the outputs from the brushes of a punched card reader into memory drive currents of approximately 200 ma. The circuit output is in series with a memory drive line, which connects to a -20v supply. The circuit input is driven by one of the brushes at a card reading station. When the brush senses a hole in the card, transistor Q01 conducts heavily, enabling memory drive current to flow.

OPERATION

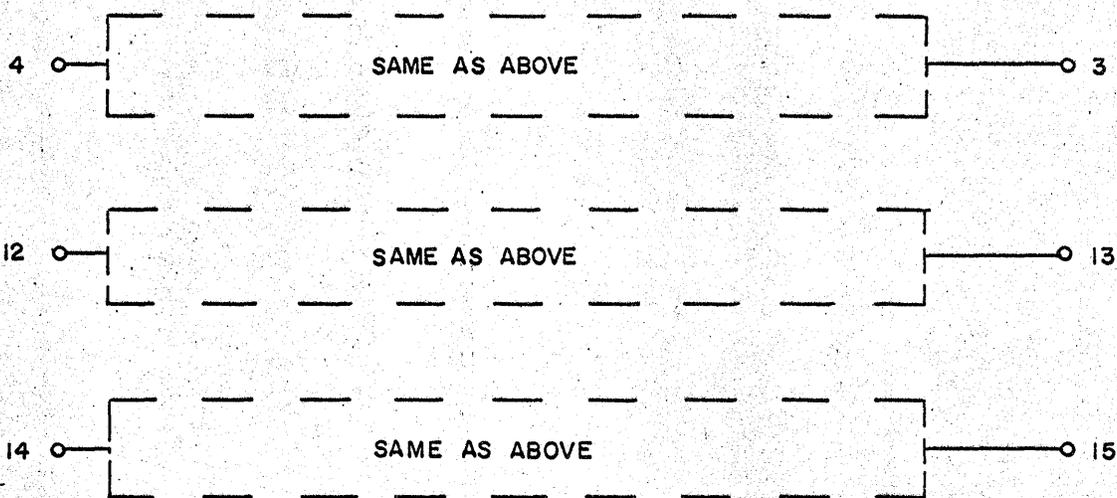
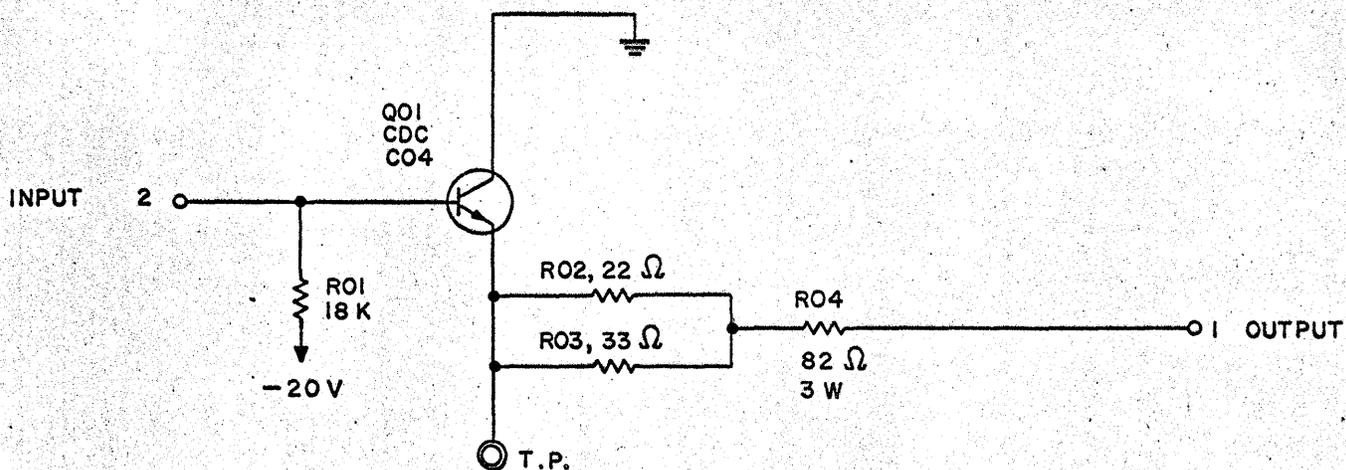
Inputs to the circuit are provided by a brush at the card reading station, and the signal levels are open circuit and approximately ground. The ground signal results when a hole in the punched card allows the brush to touch a metallic roller which is at approximately ground potential. If a hole is not present, the insulating effect of the card produces an open circuit.

The metallic roller at the reading station is held at approximately ground potential by a Relay Driver card type C84. The roller is thus at a potential equal to the saturation voltage of the Relay Driver transistor, which is approximately -0.6v.

An open circuit input allows the base voltage of Q01 to rise toward -20v. The emitter of Q01 is also at -20v, since it connects through the memory drive line to a -20v supply. This puts Q01 in the cut off condition, and memory drive current is prevented from flowing.

An input of approximately ground allows Q01 to switch on and conduct heavily. The voltage applied to the drive line is -20v, less the drop across the Relay Driver transistor and the base-emitter voltage of Q01, and is approximately -18.5v. The memory drive current is also the emitter current of Q01 and is limited by resistors R02, R03, and R04 to approximately 200 ma. The base current of Q01 is equal to the 200 ma emitter current divided by h_{FE} and is approximately 8.5 ma. The brush at the reading station is therefore required to carry the base current of Q01 plus enough additional current so that the voltage drop across R01 is approximately 19.4v; a total of approximately 9.5 ma.

I/O EMITTER FOLLOWER CARD TYPE C90



NOTES:

I. INPUT SIGNAL LEVELS ARE:

- A. OPEN CIRCUIT, Q01 CUTS OFF.
- B. \approx GROUND, Q01 CONDUCTS HEAVILY.

READER LEVEL AMPLIFIER

Card Type C91

FUNCTION

This card contains two identical circuits, the function of which is to convert solar cell outputs from a punched card reader into logical "0" signals of -1.1v. The circuit input is driven by one of the solar cells at a card reading station. When the solar cell senses a hole in the card, the circuit output switches to a -1.1v "0". If no hole is sensed, the output remains a -5.8v "1".

OPERATION

Inputs to the circuit are provided by a solar cell at the card reading station, and the signal levels are +0.4v and open circuit. The +0.4v signal results when light shining through a hole in the punched card activates the solar cell. If a hole is not present, light will be prevented from striking the solar cell and its high impedance produces essentially an open circuit. Any leakage current will not be more than a few microamperes.

The two circuits on this card are single inverters having one OR input which is fed by the network consisting of resistors R01, R02, and transistor Q01. In both circuits, the base of transistor Q01 is biased through resistor R01 to the -4.5v supply at pin 11.

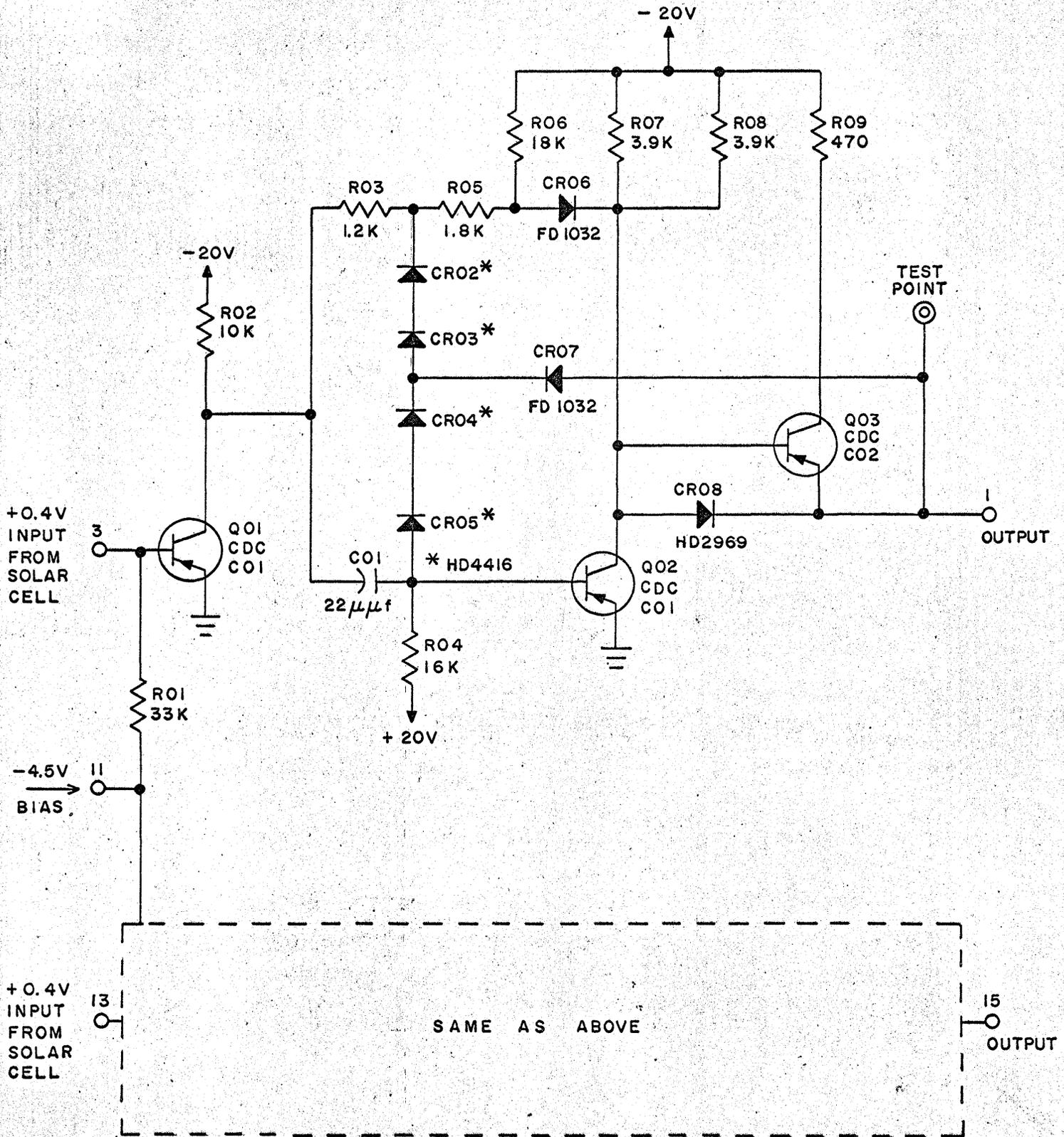
An open circuit input allows the -4.5v supply at pin 11 to apply a strong forward bias to the base of Q01. This causes Q01 to conduct heavily and its collector potential becomes approximately -0.5v. The low collector voltage of Q01 is applied to the cathode of input diode CR01 and causes the inverter to provide a -5.8v "1" output.

A +0.4v input reverse biases the base-emitter junction of Q01 so that Q01 is cut off. Its collector potential rises toward -20v, but is clamped at approximately -6v by the input impedance of the inverter and the drop across R02. The -6v collector potential of Q01 is applied as an input to the inverter and causes its output to switch to a -1.1v "0".

The remainder of the circuit is identical to a logical inverter which is discussed elsewhere. It is capable of driving 8 AND loads, 8 OR loads, or any combination resulting in 8 loads total.

READER LEVEL AMPLIFIER

CARD TYPE C91



CHAPTER 4

MAGNETIC CORE MEMORY

General

Magnetic core storage in the 3600 system is provided by the 3603 Storage Module. This module contains two independent units, each of which includes a magnetic core memory and the logic and control circuits necessary for its operation. Each memory has a capacity of 16,384 words, and both units operate together during the execution of a program, giving a total memory capacity of 32,768 words.

The length of the word stored in memory is 52 bits, of which 48 bits contain information, 3 bits are used for parity, and the 1 bit remaining is a spare. Information access time for the memory and its associated control and sensing circuits is approximately 0.5 microsecond, and the time for a complete memory cycle is approximately 1.5 microsecond.

The memory operates in the coincident current mode, using currents of one direction to Read and of the opposite direction to Write. These coincident half-currents are approximately 340 ma and are produced by the circuits contained on the Transformer Card C10, the Gate Card C05, and the Driver Card C03, which are individually discussed elsewhere.

An over-all block diagram of a 16,384-word, 52-bit memory is shown in figure 1.

Magnetic Cores

The magnetic cores have a nominal outside diameter of 0.032 inch. The core specifications and test conditions are listed in table 1, and representative waveforms are presented in figure 2.

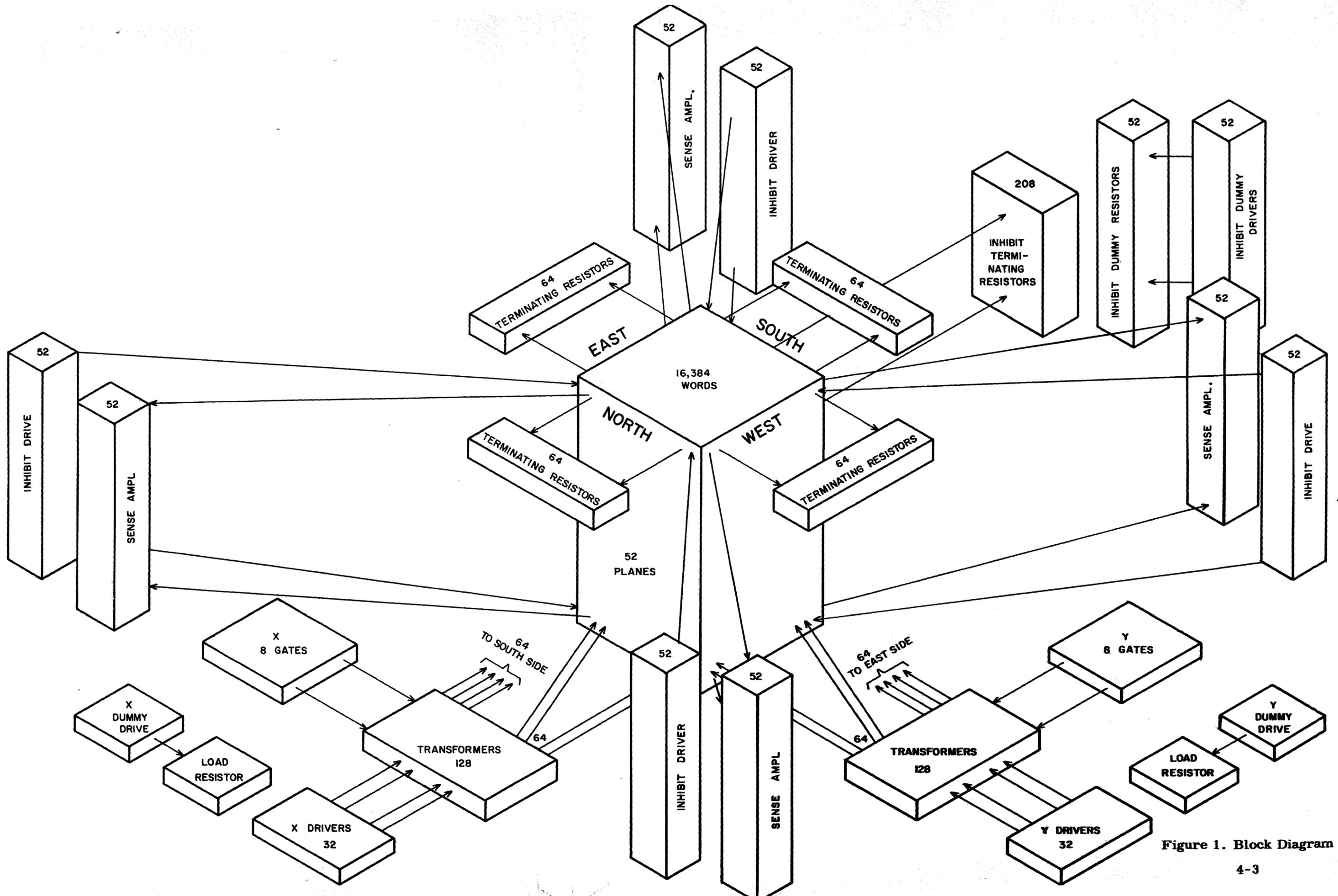


Figure 1. Block Diagram

Table 1

Core Specifications

rV_1 , disturbed voltage "1", output on sense line when core in "1" state is read after being disturbed by a Partial Read current	35 mv, min.
wV_2 , disturbed voltage "0", output on sense line when core in "0" state is read after being disturbed by a Partial Write Current	9 mv, max.
T_s , switching time *	0.35 to 0.45 microsecond
T_p , peaking time *	0.19 to 0.23 microsecond

* referred to 10% of full Read core output.

Conditions

Full Read Current	590 ma \pm 1%
Full Write Current	590 ma \pm 1%
Partial Read Current	360 ma \pm 1%
Partial Write Current	360 ma \pm 1%
T_r , rise time of full current	0.1 microsecond, linear
T_d , duration of full current	1.5 microsecond
Number of Partial Read or Write Disturb Pulses	32 min.
Sense Winding Termination	50 ohms
Temperature	40° C \pm 0.5°

REPRESENTATIVE CORE TEST WAVEFORMS

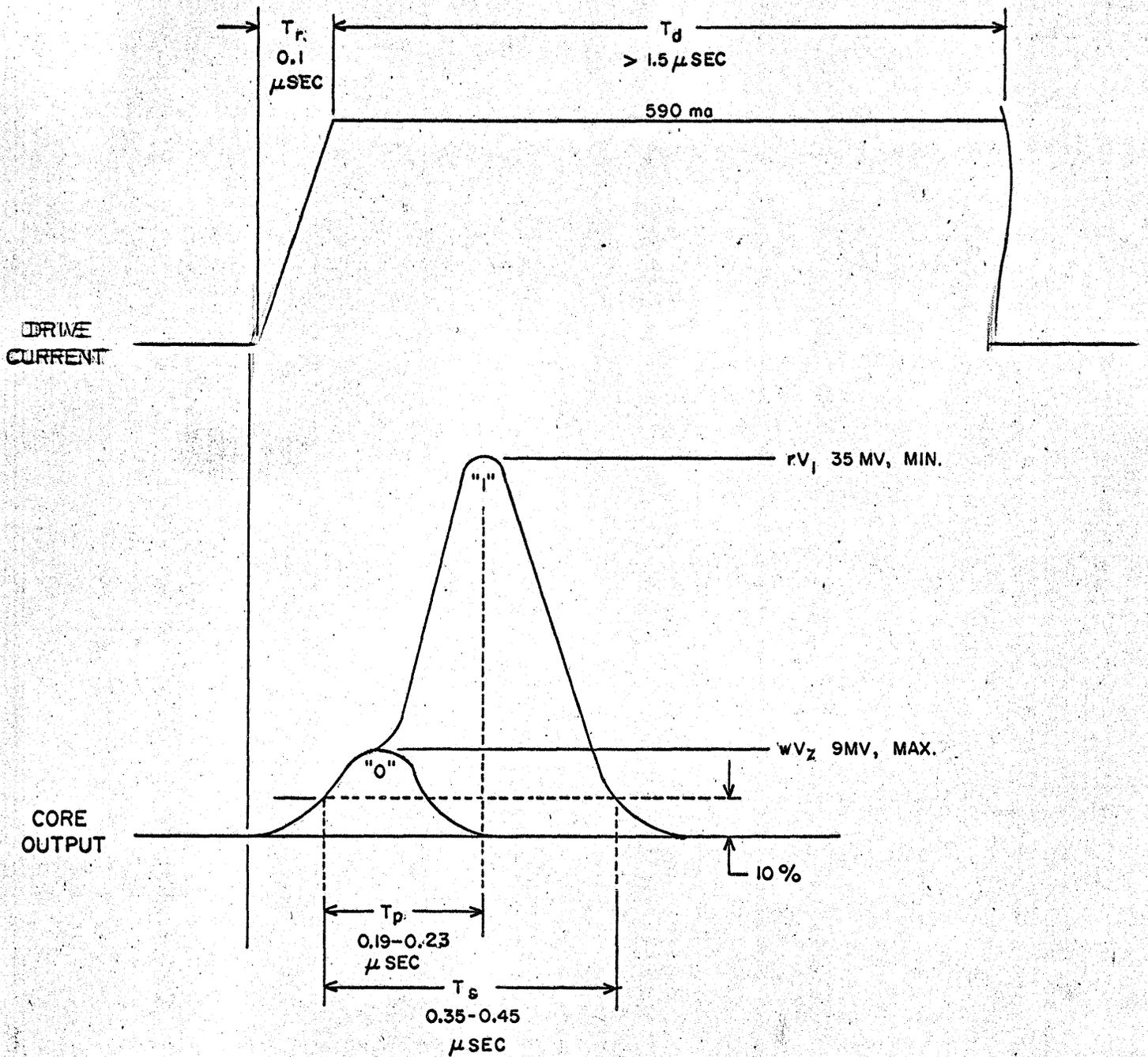


Figure 2

Each core is threaded by four wires, as shown in figure 3; X and Y half-current drive lines, an inhibit line, and a sense line. When information is written into a core, it is switched to the "1" state by two coincident 340 ma currents on the X and Y drive lines. Similarly, when information is read out of a core, it is switched to the "0" state by two coincident 340 ma currents of the other polarity.

The inhibit line carries a current of 340 ma parallel to one of the half-current drive lines, but in a direction opposite to the half-write current. Therefore, if the inhibit current is flowing during the memory Write phase, it will cancel one of the half-write currents and will prevent any core through which it passes from being switched to the "1" state.

The sense line has its two ends connected to a differential sense amplifier card. When a core switches state in either direction, the sense amplifier card produces a logical "0" output; however, this output is sampled only during the memory Read phase.

The memory core material has an approximately rectangular hysteresis loop. The high remanent magnetization of the core enables it to function as a memory element. The magnetic properties of a core are represented by its hysteresis loop shown in figure 4, in which magnetic flux density B is plotted as a function of field intensity H . If current flow sufficient to cause a field intensity of $+H_m$ is applied to the core, the flux density increases to saturation $+B_s$. When current is removed, the flux drops to the residual value $+B_r$ and stays there.

Application of current flow in the opposite direction sufficient to cause a field intensity of $-H_m$ reverses the flux density to $-B_s$. When current is removed, the flux density drops to the residual value $-B_r$.

The basic memory cycle is composed of 340 ma half-current pulses capable of producing a field intensity of $1/2H_m$. A half-current pulse is insufficient to switch a core; however, the coincidence of two half-currents results in an effective current of 680 ma, producing a net field intensity which is sufficient to switch the core.

MEMORY CORE

TYPICAL DIMENSIONS
(INCHES)

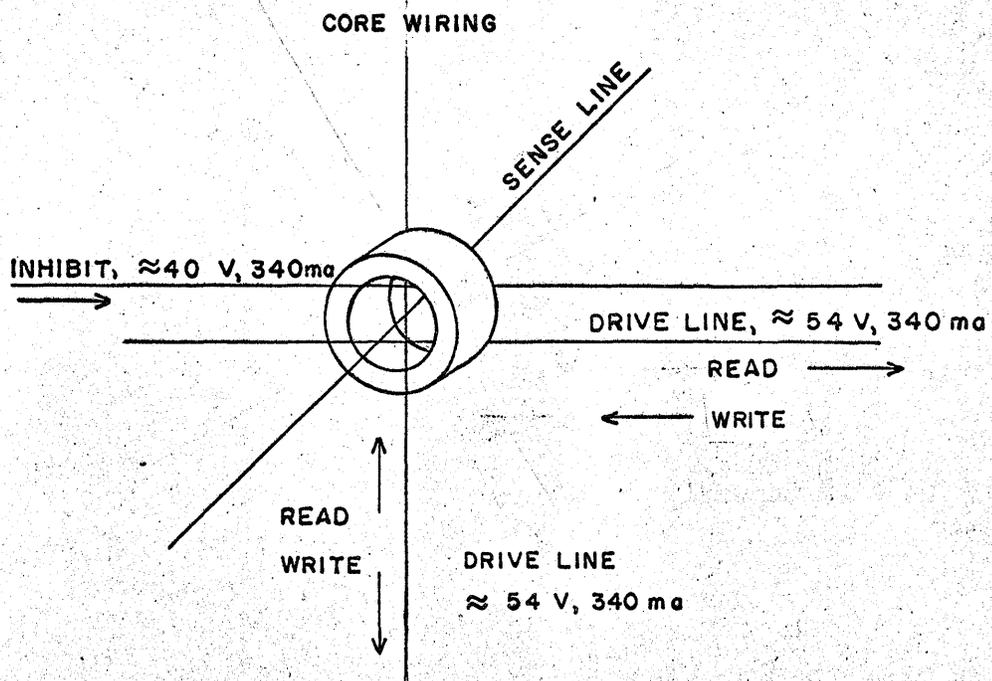
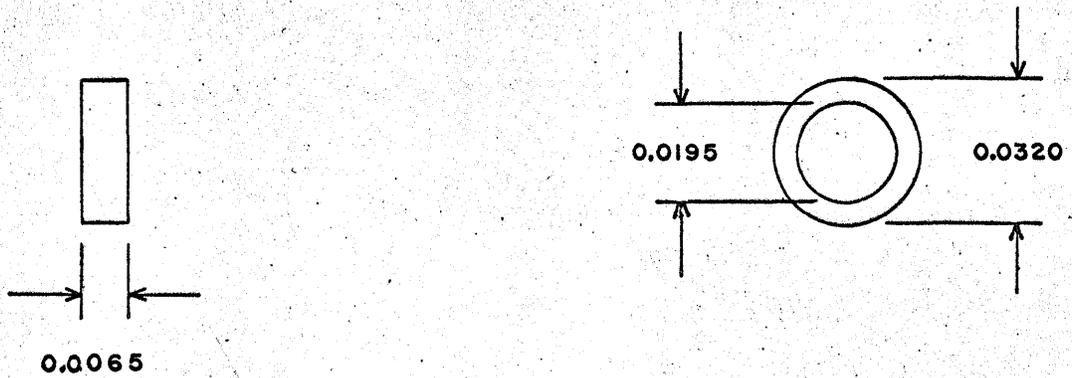


Figure 3

CORE HYSTERESIS CURVE

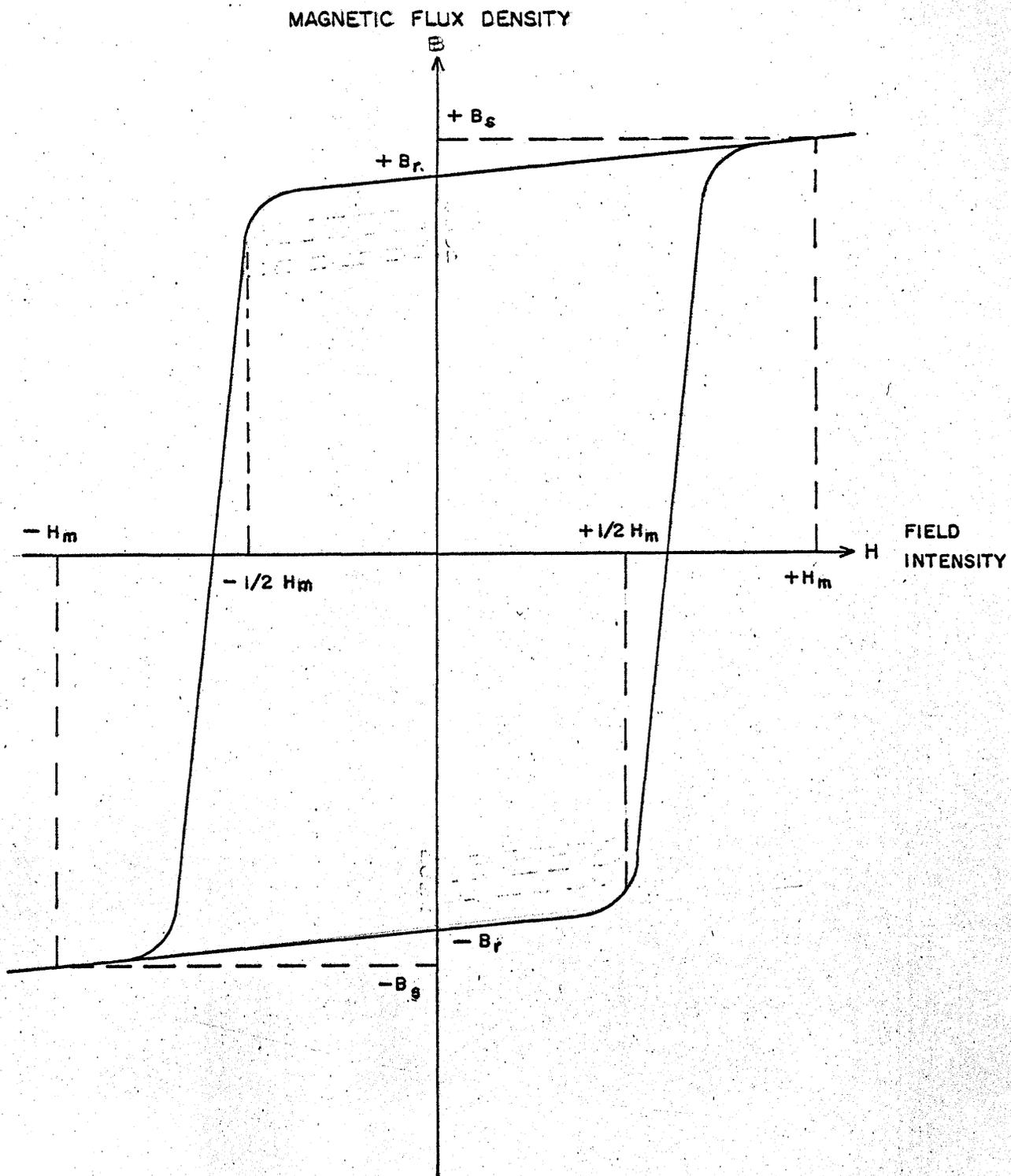


Figure 4

Memory Plane

The wires threading the memory cores are strung across the center area of square mounting frames. The wires used to drive and sense the cores also hold them in place. Each frame contains 16,384 cores in a two-dimensional arrangement called a memory plane.

The cores in each plane are divided into four quadrants of 64 x 64 cores. The four quadrants are effectively the sense quadrants; each quadrant contains its own separate sense line.

A representative memory plane is presented in figure 5. The X and Y dimensions and sense quadrant orientation are as they appear in the 3603 Module when viewed from above, with the top of the page toward the front of the module.

For purposes of reference, the four sides of the plane are designated "North", "South", "East", and "West". In the 3603 Module, the memory stack is placed with the "North" sides of the planes to the back. "South" is the side of the stack nearest the card connectors and backboard wiring. The other dimensions are as shown in figure 5.

Memory Stack

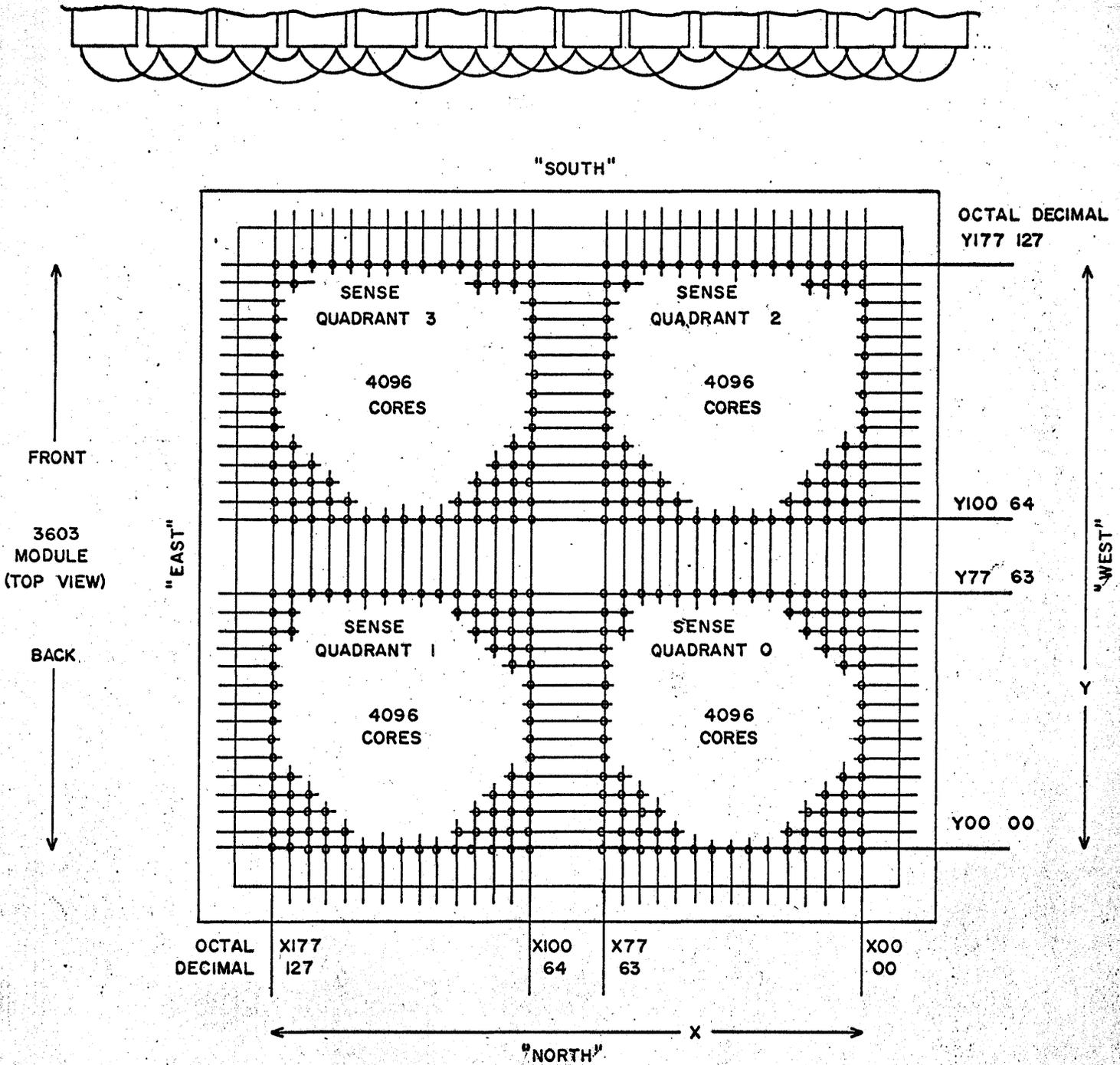
A memory plane contains only one bit of each computer word, and the 16,384 core locations correspond to the 16,384 word memory capacity. Thus, 52 planes are needed to contain the 48 bits of information, the 3 bits of parity, and the spare bit. The 52 planes are mounted one above the other in a "cubic" arrangement called a memory stack, as shown in figures 6 and 7.

The planes are numbered sequentially from bottom to top, beginning with plane 00 and ending with plane 51. The 48 bits of information are contained in planes 00 through 47. The 3 bits of parity are contained in planes 48, 49, and 50, and the spare bit of each word is in plane 51.

The half-current drive lines enter the stack at the bottom and progress from plane to plane to the top, where they are terminated by resistors approximately equal to their characteristic impedance. The drive lines are energized in the manner of transmission lines; thus each line exhibits a velocity of signal propagation dependent upon its line constants and distributed parameters.

MEMORY PLANE ORIENTATION

CARD CONNECTORS AND BACKBOARD WIRING

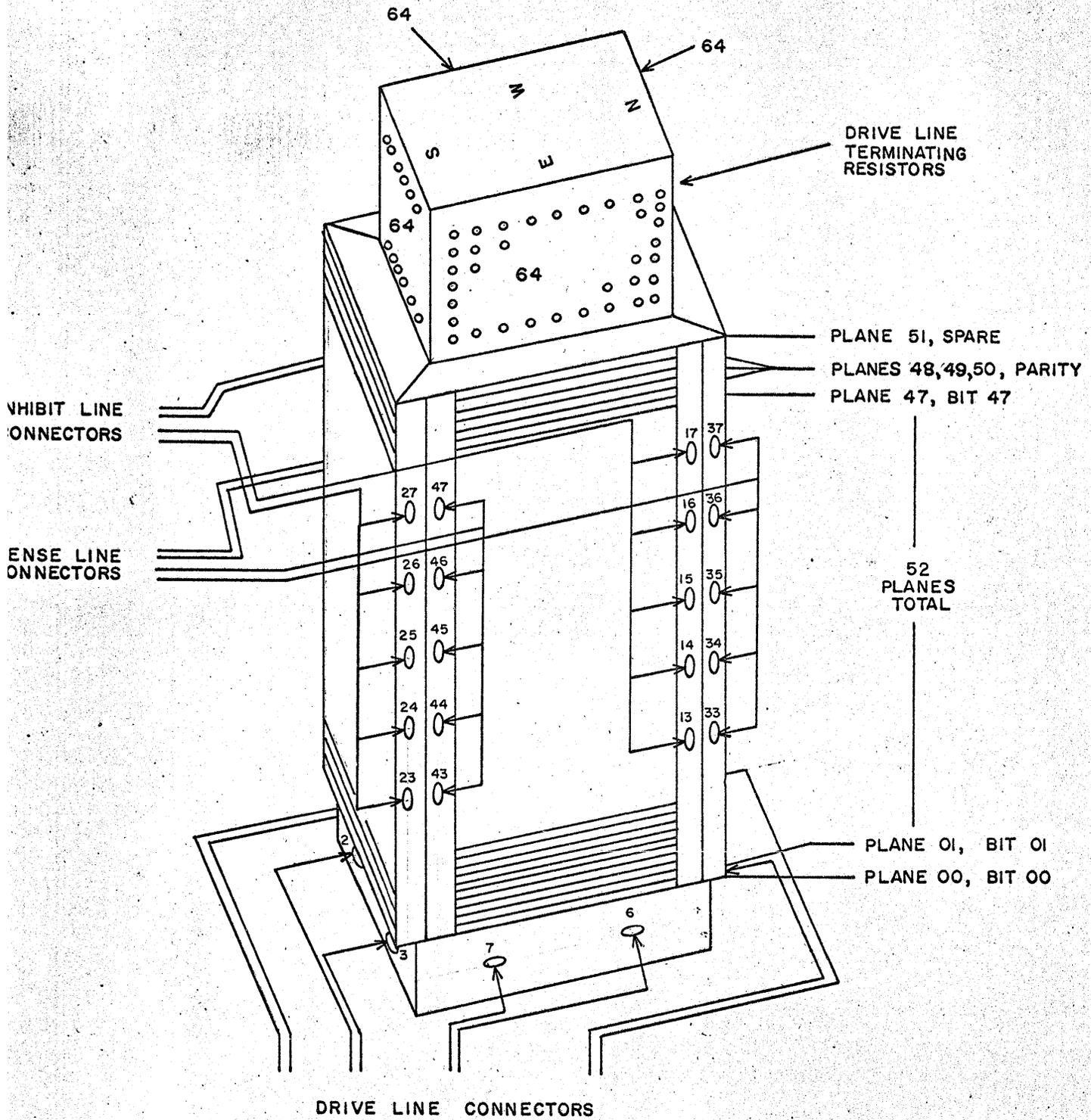


NOTE:

DRIVE LINE NUMBERS PERTAIN TO PLANE 00, AT BOTTOM OF STACK.

Figure 5

MEMORY STACK

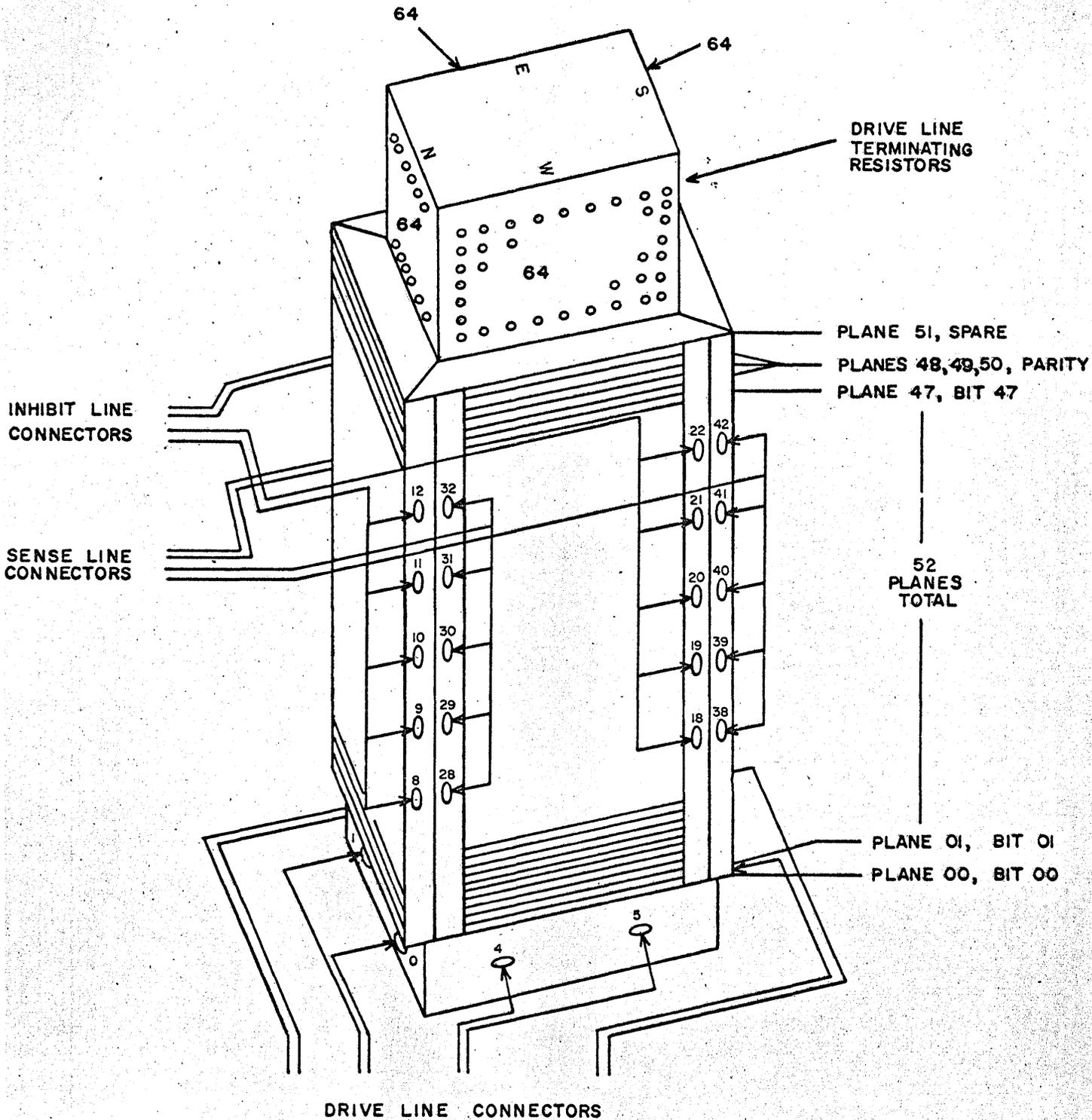


NOTE:

IN THE 3603 MODULE, THE STACK IS POSITIONED AS SHOWN, WITH PLANE 51 ON TOP AND PLANE 00 ON THE BOTTOM.

Figure 6

MEMORY STACK



NOTE:

IN THE 3603 MODULE, THE STACK IS POSITIONED AS SHOWN, WITH PLANE 51 ON TOP AND PLANE 00 ON THE BOTTOM.

The time required for a drive current to pass through the 52-plane stack is approximately 120 nanoseconds. Timing is provided by a tapped delay line, so that the sense quadrants and inhibit windings will be enabled in synchronism with the progression of the drive currents through the 52 planes.

Windings

A simplified representation of a memory plane sense quadrant is shown in figure 8. For purposes of illustration, the number of cores has been reduced from 4,096 to 16, but all other elements are as shown.

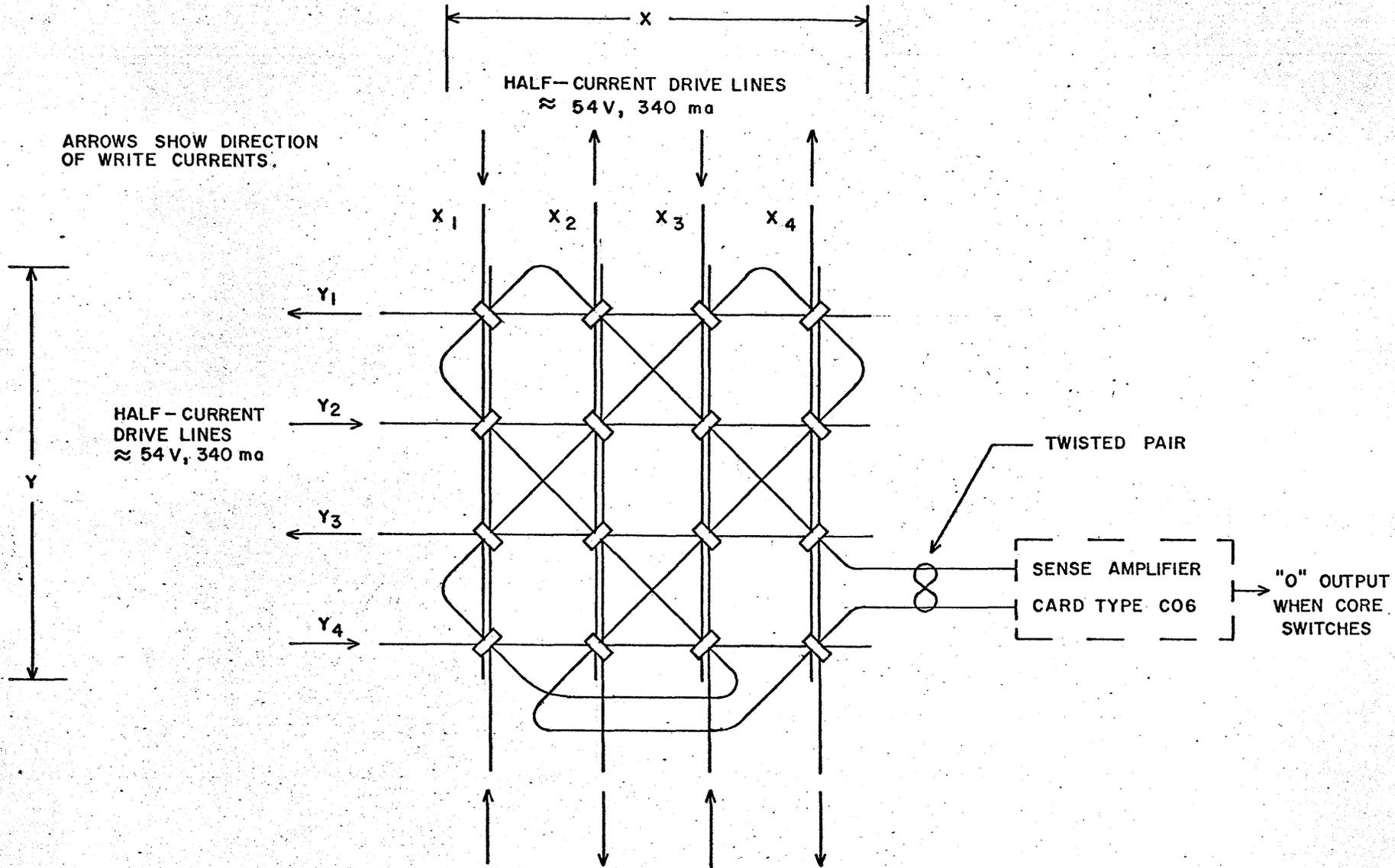
Two coincident 340 ma currents on an X and a Y drive line will intersect at one memory core in each plane, causing it to switch state. The remaining cores, through which only one of the drive currents passes, will merely shift slightly along the hysteresis loop and will not switch state.

The rapid flux change when a core switches induces a voltage on the sense line of approximately 35 mv. This appears across the differential amplifier inputs of the Sense Amplifier card type C06, and results in a logical "0" output. This output occurs when any core in the sense quadrant switches state in either direction, but the output is sampled only during the Read phase of the memory cycle.

The inhibit lines provide a means for preventing a core from being switched to the "1" state during the Write phase of the memory cycle. The drive currents, if allowed to act freely, will switch all 52 cores to the "1" state, representing a computer word in which each bit is a "1". Each of the memory planes is therefore provided with inhibit lines, so that the core in that plane can be prevented from switching, in case that particular bit of the word is to be a "0". The magnitude of the inhibit current is approximately 340 ma, and the direction of flow is opposite to one of the half-write currents. Thus, one half-write current is effectively canceled and the core does not change state.

The approximate timing of a memory cycle is presented in figure 9, with representative waveforms. Information access time is approximately 0.5 microsecond, and the time for a complete Read-Write cycle is approximately 1.5 microsecond. However, these times apply only to the memory stack and associated drive and sense circuits, and do not include time required by the logic of the 3603 Module.

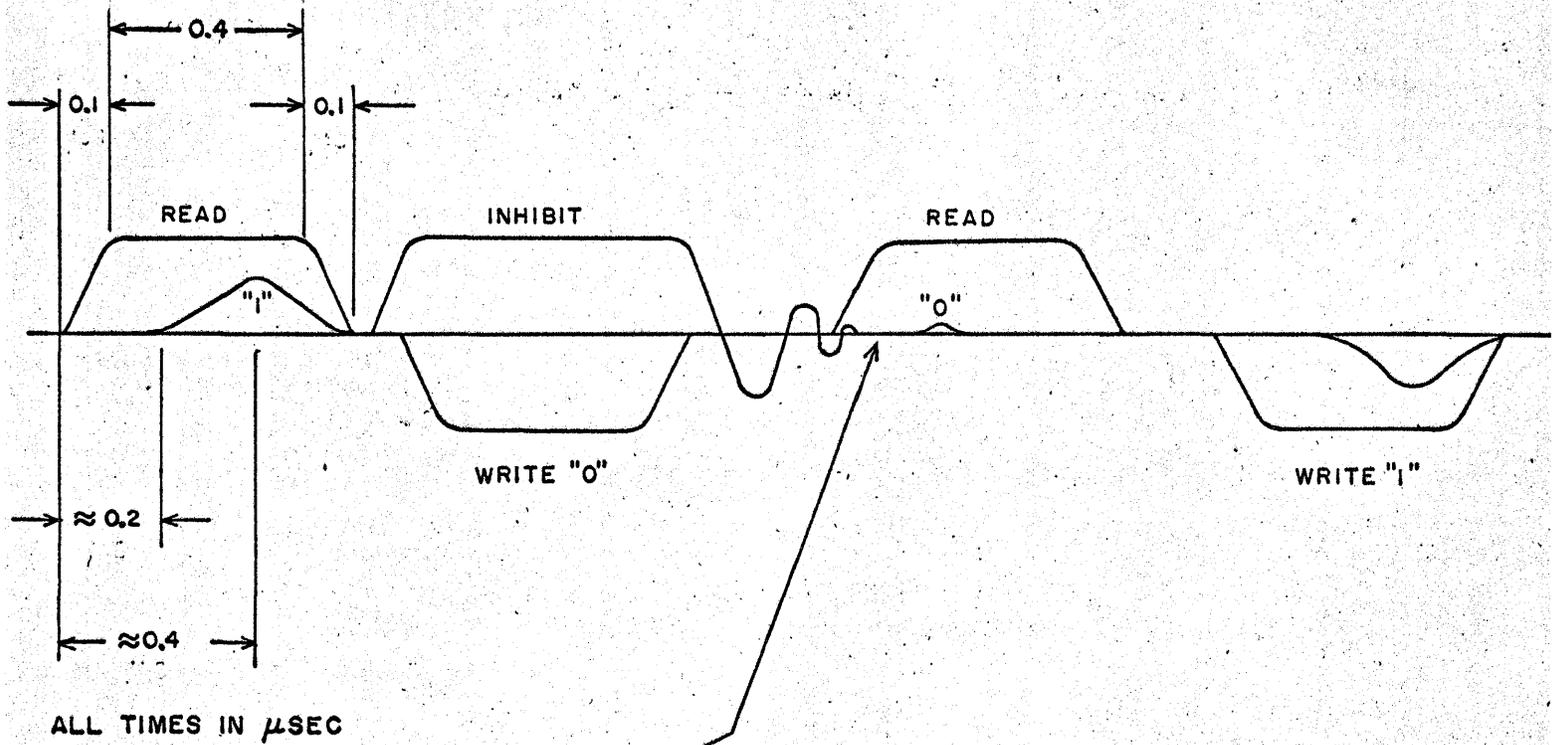
SIMPLIFIED SENSE QUADRANT



OPPOSES Y HALF-WRITE IN ODD NUMBERED PLANES; 1, 3, 5, ETC.
 OPPOSES X HALF-WRITE IN EVEN NUMBERED PLANES; 0, 2, 4, ETC.
 CONFIGURATION SHOWN IS TYPICAL FOR EVEN NUMBERED PLANE.

Figure 7
 4-15

REPRESENTATIVE MEMORY CYCLE WAVEFORMS



NOTE:

READING DOES NOT OCCUR UNTIL NOISE FROM PREVIOUS INHIBIT HAS DIED AWAY.

Figure 8

In a Write "0" operation, the flow of inhibit current will induce an appreciable amount of noise on the sense line. Therefore the following Read operation must be delayed until the noise has died away sufficiently to allow a "0" to be sensed.

Sense Line

A simplified example of a sense line is shown in figure 8. One sense line threads all 4,096 cores in a sense quadrant; thus each memory plane contains 4 sense lines. Each sense line is continuous and the two ends are brought out at terminals near a corner of the plane.

The resistance of a sense line is approximately 22 ohms. It is essential that the total resistance of the sense line and amplifier input leads be kept small, in order to avoid excessive signal attenuation.

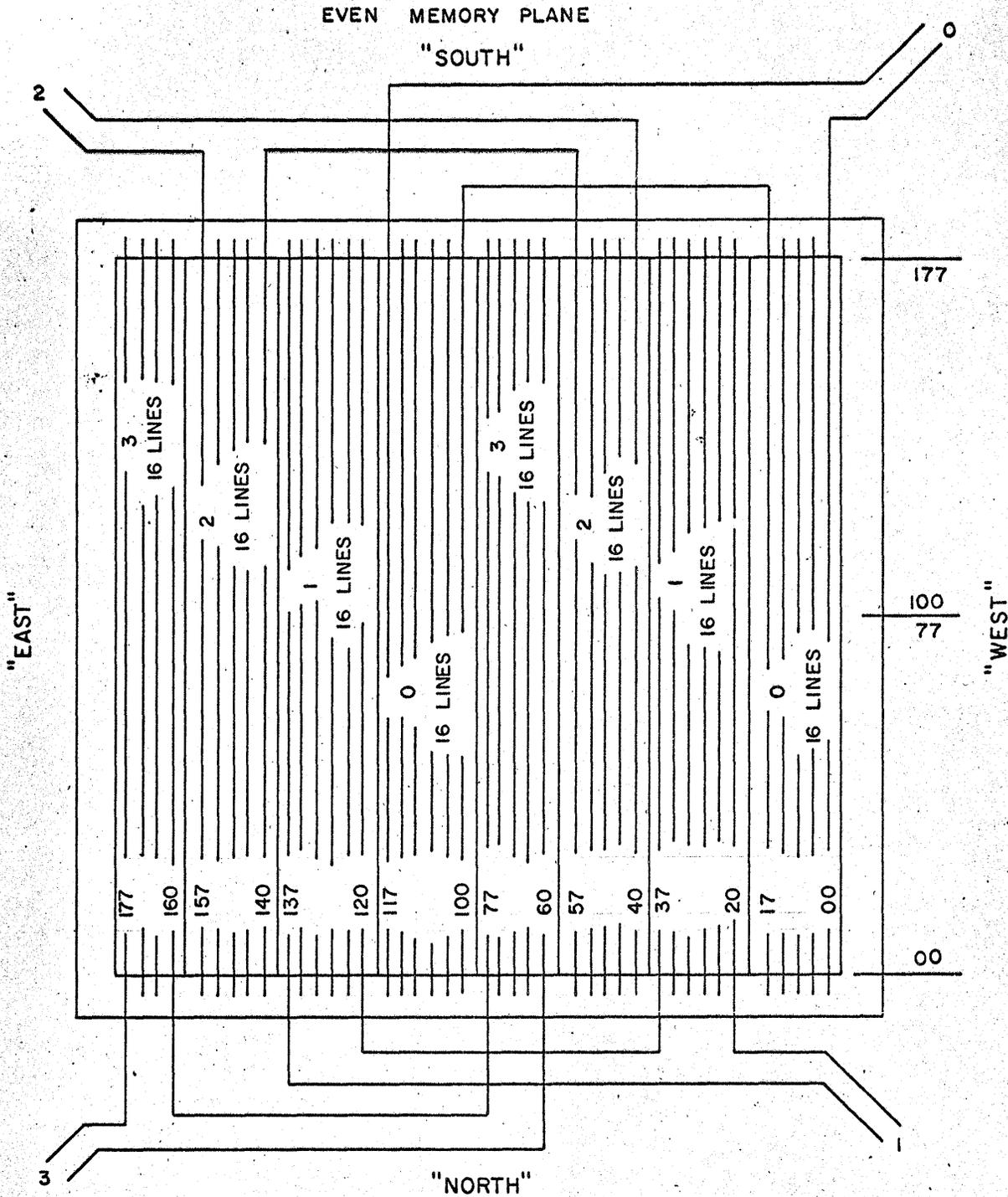
Inhibit Lines

The inhibit lines in each plane are arranged in 8 groups, or "stripes". Each stripe is 16 cores wide and extends all the way across the plane; thus each inhibit stripe controls $16 \times 128 = 2,048$ cores. The stripes are energized in groups of 2, so that $1/4$ of a plane, 4,096 cores, will be inhibited simultaneously. However, the 2 stripes are located in opposite halves of the plane, so that only $1/2$ of 1 stripe, 1,024 cores, is within any one sense quadrant. This is shown in figures 10 and 11.

To diminish induced noise, the direction of the inhibit lines is rotated 90° from plane to plane. In odd numbered planes (1, 3, 5, ---47, 49, 51), the inhibits run parallel to the Y drive lines and oppose the Y half-write currents. In even numbered planes (0, 2, 4, ---46, 48, 50), the inhibits run parallel to the X drive lines and oppose the X half-write currents.

Typical circuits of inhibit lines for odd and even planes are presented in figures 12 and 13. All external wiring is twisted pair, and the 120-ohm terminating resistor is non-inductive. The d-c resistance of an inhibit line is approximately 13 ohms.

INHIBIT STRIPE CONFIGURATION



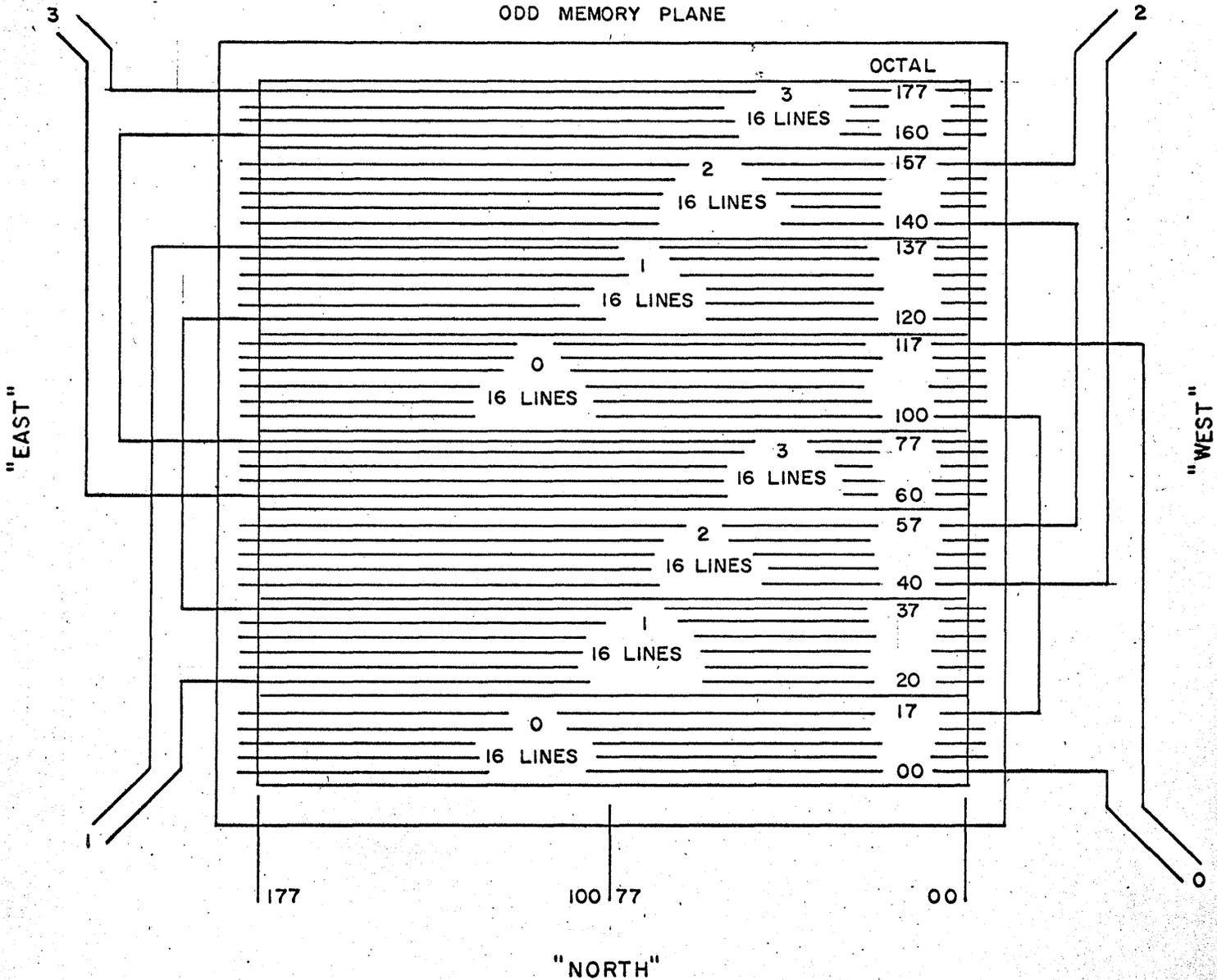
NOTE:

1. DIRECTION OF INHIBIT LINES IS ROTATED 90° FROM PLANE TO PLANE.
2. INHIBIT CURRENT OPPOSES Y HALF-WRITE IN ODD NUMBERED PLANES; 1, 3, 5, ETC.
3. INHIBIT CURRENT OPPOSES X HALF-WRITE IN EVEN NUMBERED PLANES; 0, 2, 4, ETC.

Figure 9

INHIBIT STRIPE CONFIGURATION

" SOUTH "



NOTE:

1. DIRECTION OF INHIBIT LINES IS ROTATED 90° FROM PLANE TO PLANE.
2. INHIBIT CURRENT OPPOSES Y HALF-WRITE IN ODD NUMBERED PLANES; 1, 3, 5, ETC.
3. INHIBIT CURRENT OPPOSES X HALF-WRITE IN EVEN NUMBERED PLANES; 0, 2, 4, ETC.

Figure 10

INHIBIT CIRCUIT

EVEN PLANE; 0, 2, 4, ETC.

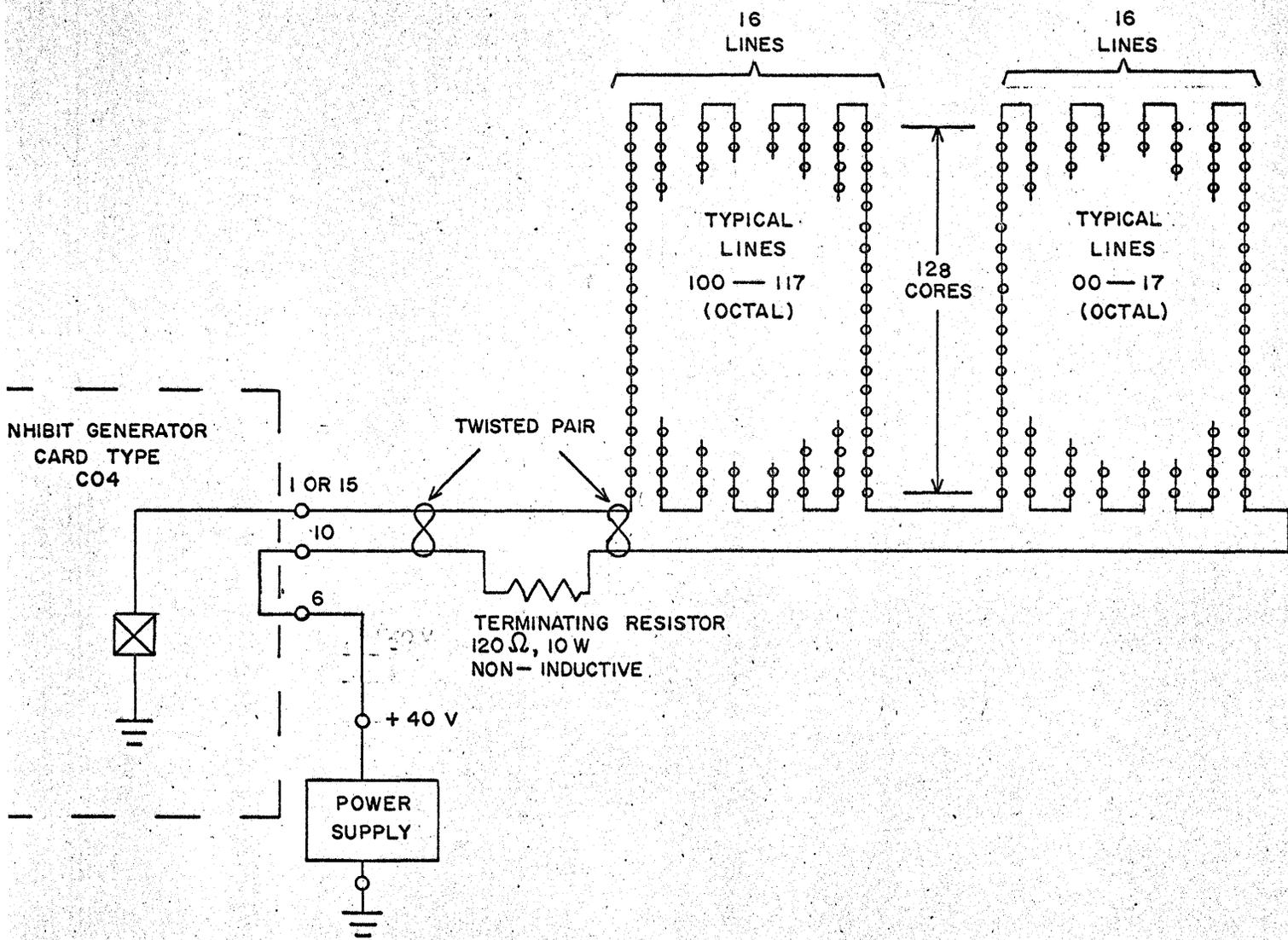
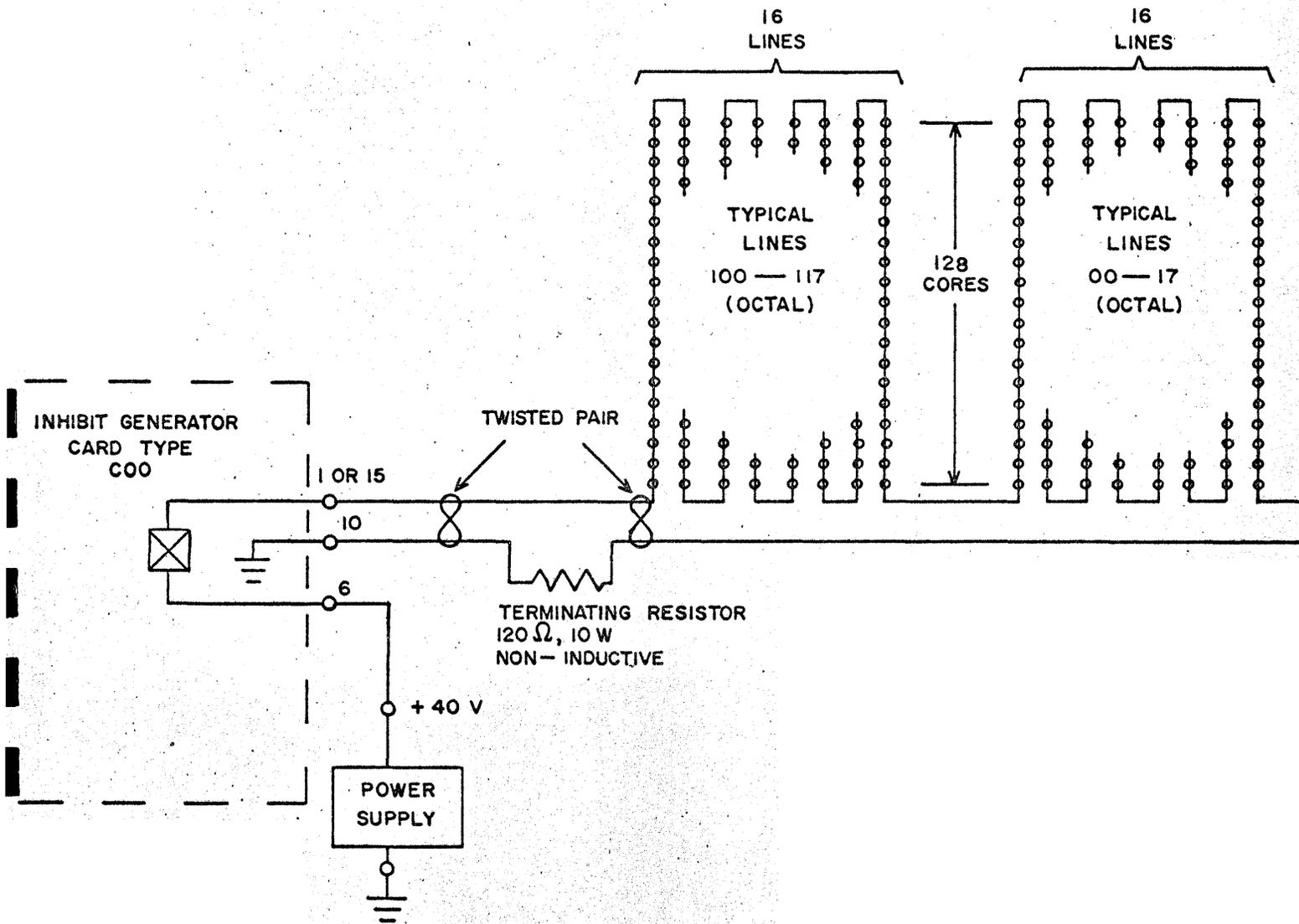


Figure 11

INHIBIT CIRCUIT

ODD PLANE; 1,3,5, ETC.



To minimize effects of capacitive coupling between the inhibit lines and the drive lines which parallel them, the inhibit lines are energized in a manner such that the direction of voltage change is the same as the direction of voltage change in the parallel drive lines carrying half-write currents.

The inhibit lines are energized by a power supply of +40v. In even numbered planes, current flow is controlled by an Inhibit Generator card type C04, which switches the end of the inhibit line to ground so that the voltage change within the plane is from +40v toward ground. In odd numbered planes, current flow is controlled by an Inhibit Generator card type C00, which switches the +40v into the inhibit line so that the direction of voltage change within the plane is from ground toward +40v. In a manner similar to the X and Y drive lines the inhibit lines are also treated as transmission lines. The characteristic impedance of an inhibit line is approximately 140 ohms. A terminating resistor of 120 ohms is in series with each inhibit line. Although this value produces a slight impedance mismatch, the resulting current flow from a 40v supply is approximately the required 340 ma.

Drive Lines

A 52-bit computer word consists of 1 bit in each of the 52 planes in the memory stack. The bit in each plane is located at the intersection of the X half-current line and the Y half-current line. These drive lines are jumpered from plane to plane, forming continuous windings which thread the entire stack, as shown in figure 14.

A typical drive line circuit is shown in figure 15. Detailed discussions of the printed circuit card types may be found elsewhere in this manual. External wiring from card type C10 to the memory stack is twisted pair, and the 130-ohm terminating resistor is non-inductive. The d-c resistance of a drive line threading the entire 52-plane stack is approximately 29.5 ohms.

The half-current drive lines are energized in the manner of transmission lines. The characteristic impedance of a drive line is approximately 130 ohms, therefore each line is terminated with a 130-ohm resistor. The lines are energized by pulses of about 54 volts, so that the resulting half-currents are about 340 ma.

As shown in figure 15, the drive lines may be energized with currents of either direction, corresponding to the memory Read-Write cycle. Current from the +20v source is switched by one of the C05 cards into the center-tapped primary windings of two of the transformers on card type C10. The current may then flow in either direction through the primaries to ground, as controlled by the C03 cards. It is seen that the transformers each have two secondary windings connected in series with the half-current drive lines. Also, one pair of windings is connected oppositely from the other, so that under any set of conditions of current flow in the primaries, one set of secondary voltages adds while the other set cancels. Thus it is possible to produce current flow in either direction on either drive line by enabling the proper combination of circuits on the C03 cards.

X AND Y DRIVE LINES

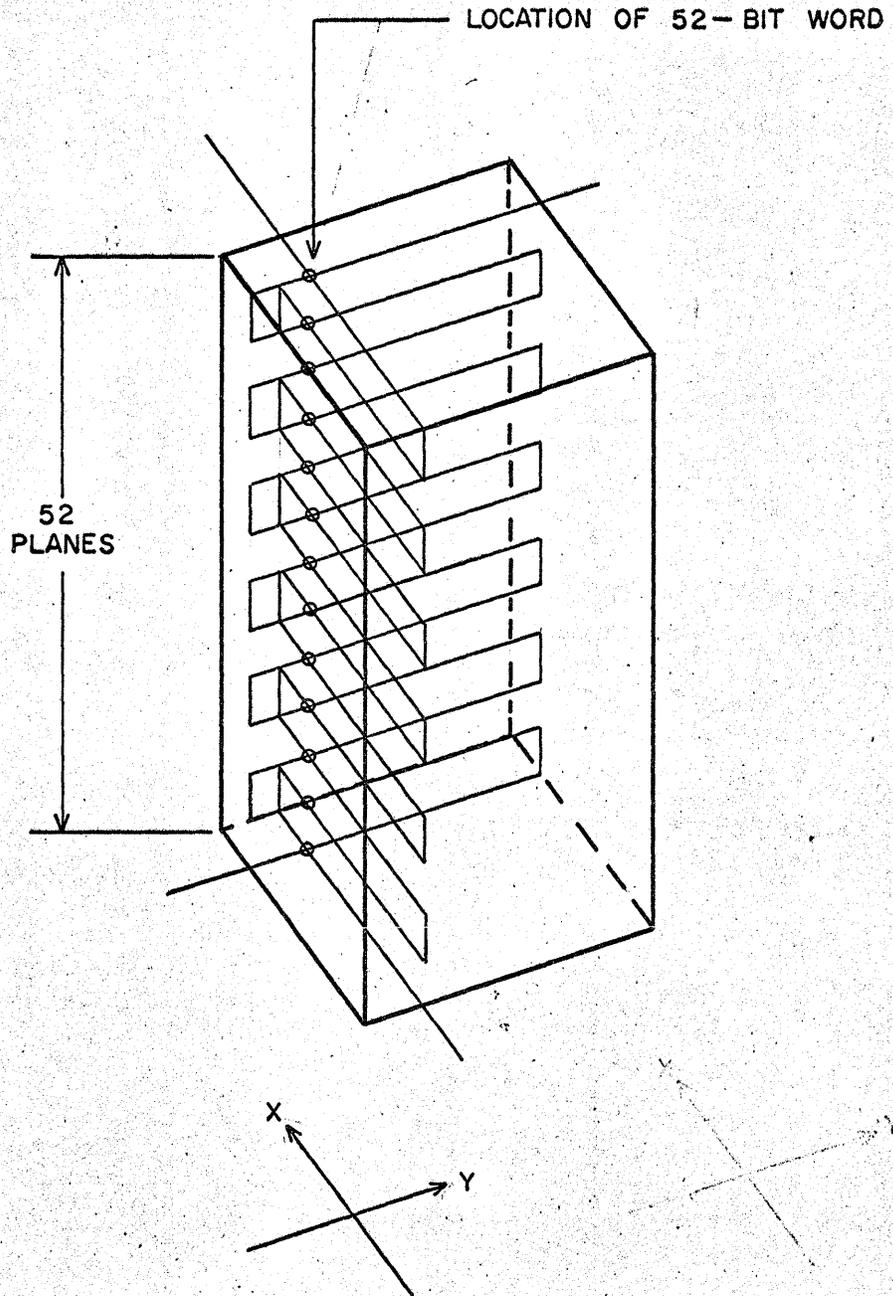
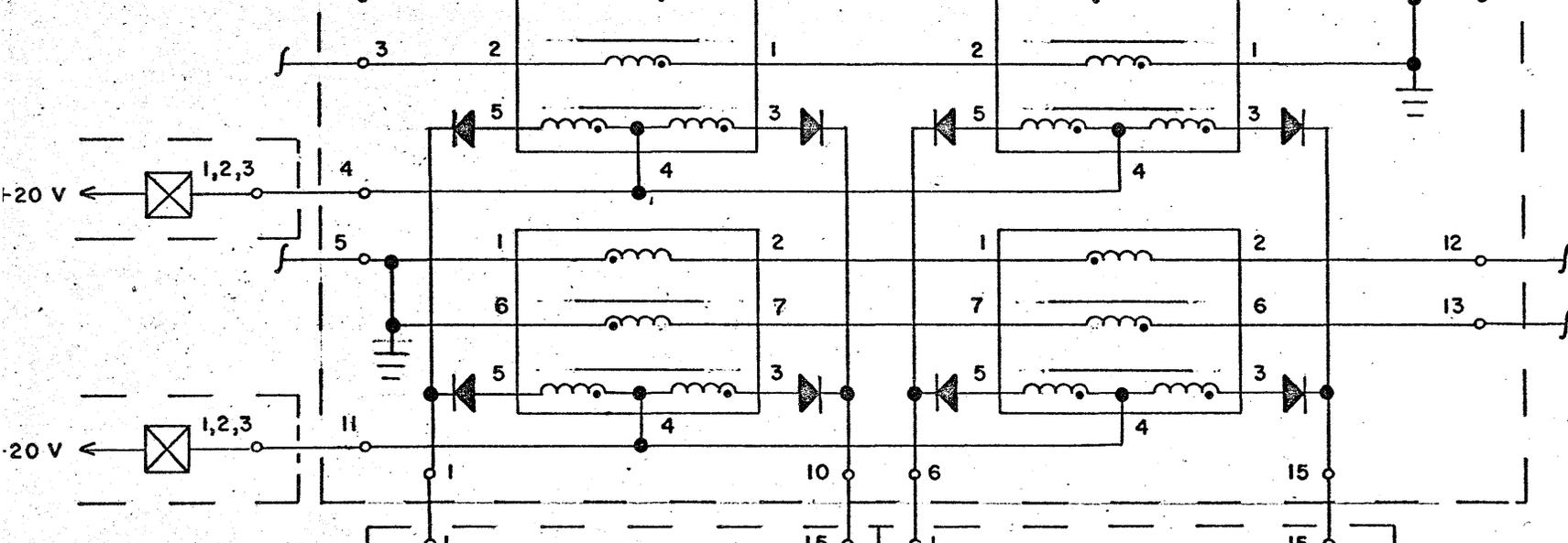
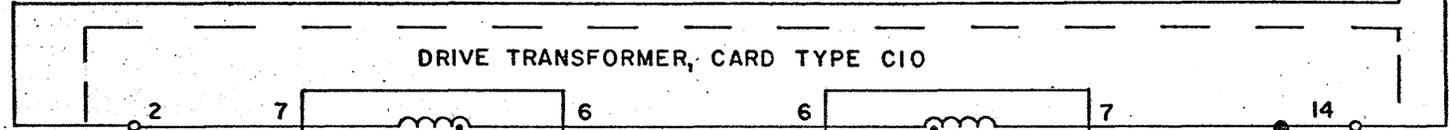
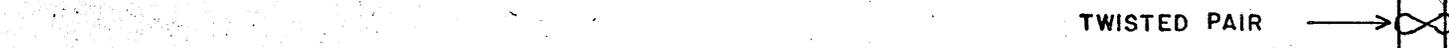
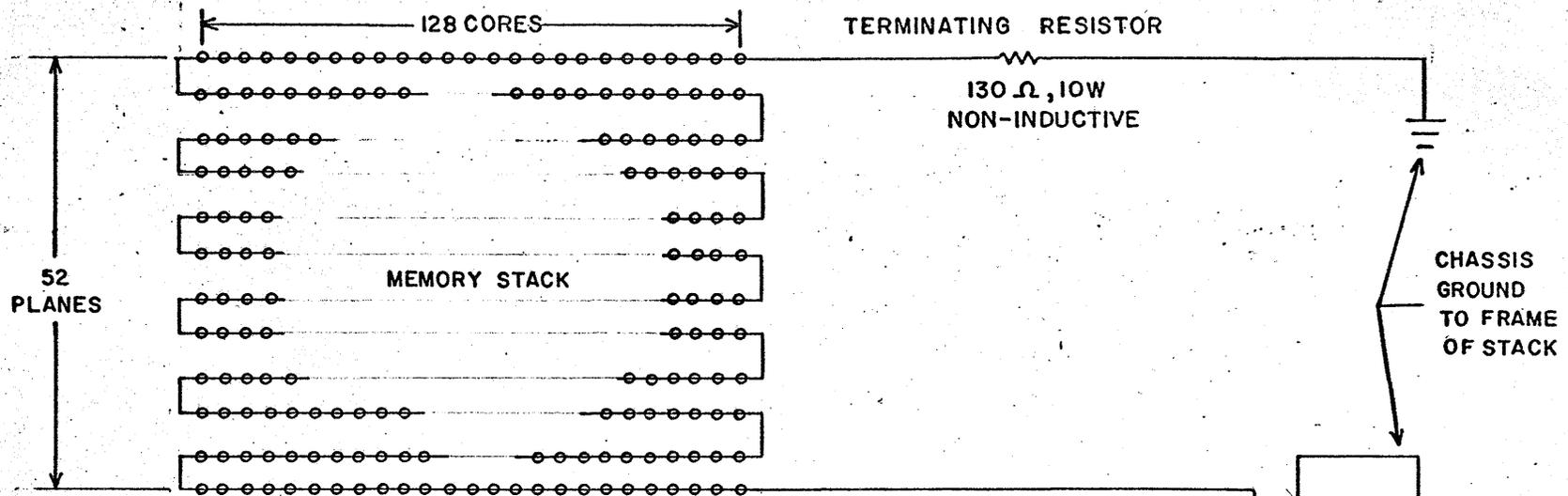


Figure 12

DRIVE LINE CIRCUIT



GATES
CARD TYPE C05

TRANSFORMER DRIVERS
CARD TYPE C03

Figure 13

4-25

Dummy Drive and Inhibit

In order to hold a constant load on the memory power supplies, dummy load circuits are enabled during times when the memory drive or inhibit circuits are not carrying current. The arrangement of these dummy load circuits is presented in figures 16 and 17.

The drive line circuits contain dummy loads in the Gate selection scheme of both the X and Y coordinates. Each coordinate contains 8 Gate cards, each of which carries a current of approximately 900 ma. However, only one Gate card is selected at a time, and when all 8 are turned off, the dummy load is enabled. The dummy load consists of a Transformer Driver card type C03, each half of which drives a current of approximately 400 ma through a 50-ohm, 10-watt, non-inductive load resistor.

The inhibit circuits contain a dummy load for each plane, in the Inhibit Generator selection scheme. Four Inhibit Generator circuits are required per plane, and a fifth circuit is included as a dummy. This fifth circuit is a Dummy Inhibit Generator and is contained on card type C09. The Inhibit Generators are selected one at a time, and when all four are turned off, the dummy is enabled. The dummy circuit drives approximately 340 ma of current through a 133-ohm, 25-watt, non-inductive resistor. The 133-ohm resistor is approximately equal to the sum of the 13-ohm d-c resistance and the 120-ohm terminating resistance of an inhibit line.

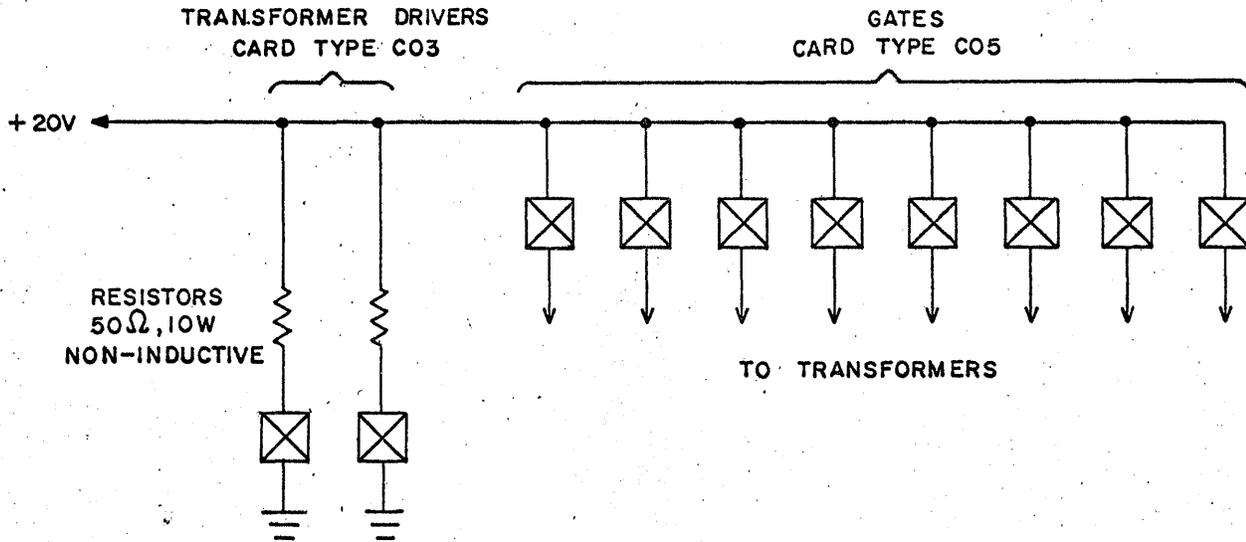
Transposition of Drive Lines

The drive lines enter the stack at the bottom, progressing upward from plane to plane, with the terminating resistors at the top. Referring to figure 5, it is seen that the four sides of the stack are referred to as "North", "South", "East", and "West", as shown.

The even (0, 2, 4, 6, etc.) X drive lines enter on the "North" side, and the odd (1, 3, 5, 7, etc.) X drive lines enter on the "South" side. Similarly, the even and odd Y drive lines enter on the "West" and "East" sides, respectively.

DUMMY DRIVE SCHEME

X OR Y COORDINATE



DUMMY INHIBIT SCHEME

TYPICAL FOR EVEN PLANE (0,2,4,ETC.)

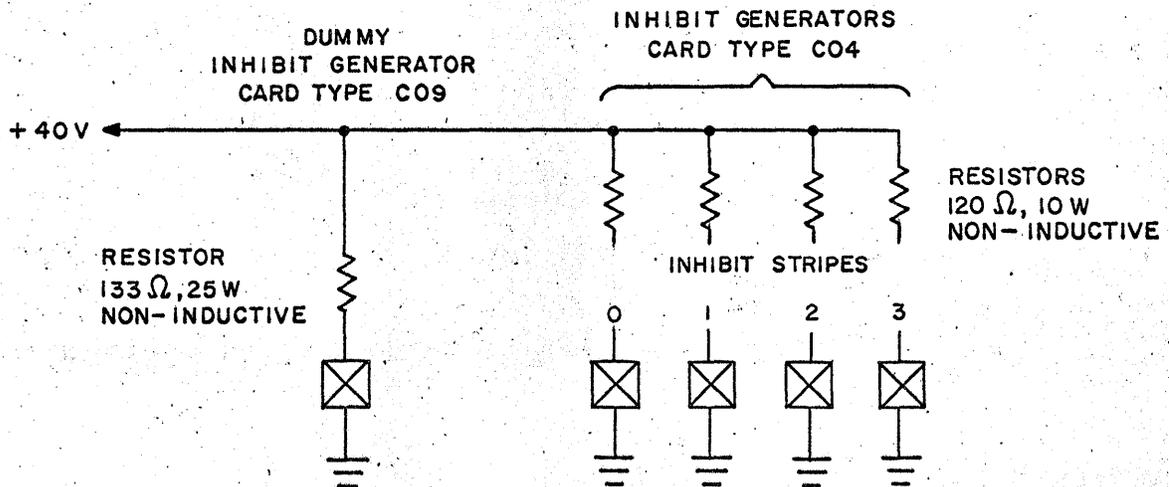


Figure 14

DUMMY INHIBIT SCHEME

TYPICAL FOR ODD PLANE (1,3,5, ETC.)

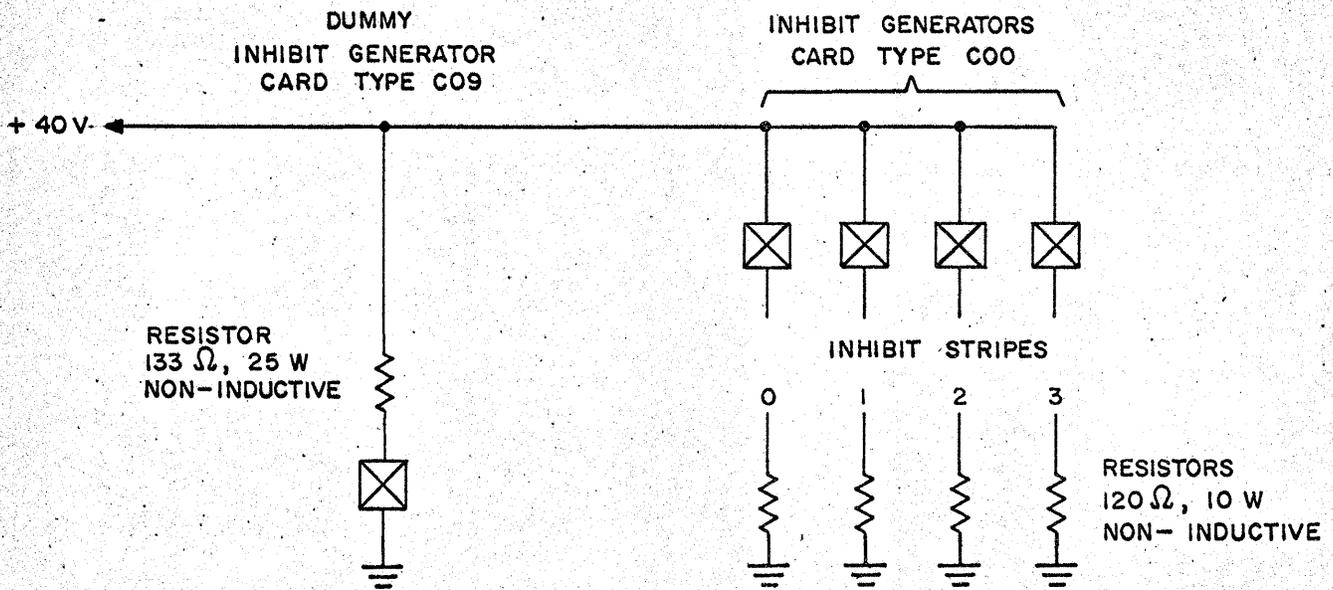


Figure 15

To minimize induced noise in adjacent drive lines, a drive line transposition occurs at intervals of 13 planes. Thus a given pair of drive lines run side by side for only 13 planes, and are transposed 3 times in traversing the 52-plane stack.

The following charts list the drive line transpositions for the 4 sides of the stack. Because 13 is an odd number, a line entering on the "South" side will emerge on the "North" side, and vice versa.

"NORTH"
(Outside View)

0 ↔ 12		13 ↔ 25		26 ↔ 38		39 ↔ 51	
126	127	119	126	118	115	123	118
124	125	117	124	124	121	113	124
122	123	115	122	114	127	119	114
120	121	113	120	120	117	125	120
118	119	127	118	126	123	115	126
116	117	125	116	116	113	121	116
114	115	123	114	122	119	127	122
112	113	121	112	112	125	117	112
110	111	103	110	102	99	107	102
108	109	101	108	108	105	97	108
106	107	99	106	98	111	103	98
104	105	97	104	104	101	109	104
102	103	111	102	110	107	99	110
100	101	109	100	100	97	105	100
98	99	107	98	106	103	111	106
96	97	105	96	96	109	101	96
94	95	87	94	86	83	91	86
92	93	85	92	92	89	81	92
90	91	83	90	82	95	87	82
88	89	81	88	88	85	93	88
86	87	95	86	94	91	83	84
84	85	93	84	84	81	89	84
82	83	91	82	90	87	95	90
80	81	89	80	80	93	85	80
78	79	71	78	70	67	75	70
76	77	69	76	76	73	65	76
74	75	67	74	66	79	71	66
72	73	65	72	72	69	77	72
70	71	79	70	78	75	67	78
68	69	77	68	68	65	73	68
66	67	75	66	74	71	79	74
64	65	73	64	64	77	69	64
62	63	55	62	54	51	59	54
60	61	53	60	60	57	49	60
58	59	51	58	50	63	55	50
56	57	49	56	56	53	61	56
54	55	63	54	62	59	51	62
52	53	61	52	52	49	57	52
50	51	59	50	58	55	63	58
48	49	57	48	48	61	53	48
46	47	39	46	38	35	43	38
44	45	37	44	44	41	33	44
42	43	35	42	34	47	39	34
40	41	33	40	40	37	45	40
38	39	47	38	46	43	35	46
36	37	45	36	36	33	41	36
34	35	43	34	42	39	47	42
32	33	41	32	32	45	37	32
30	31	23	30	22	19	27	22
28	29	21	28	28	25	17	28
26	27	19	26	18	31	23	18
24	25	17	24	24	21	29	24
22	23	31	22	30	27	19	30
20	21	29	20	20	17	25	20
18	19	27	18	26	23	31	26
16	17	25	16	16	29	21	16
14	15	7	14	6	3	11	6
12	13	5	12	12	9	1	12
10	11	3	10	10	15	7	2
8	9	1	8	8	5	13	8
6	7	15	6	14	11	3	14
4	5	13	4	4	1	9	4
2	3	11	2	10	7	15	10
0	1	9	0	0	13	5	0

Empty Plane with Wires Running from Inside of Plane to Connectors

For Transpositions

Empty Planes

For Transpositions

Empty Planes

For Transpositions

Empty Planes

Empty Plane with Wires Running from Inside of Plane to Terminating Resistors

Table 2

Table 2

"SOUTH"
(Outside View)

0 ↔ 12	13 ↔ 25	26 ↔ 38	39 ↔ 51		
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49 51 53 55 57 59 61 63 65 67 69 71 73 75 77 79 81 83 85 87 89 91 93 95 97 99 101 103 105 107 109 111 113 115 117 119 121 123 125 127	0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72 74 76 78 80 82 84 86 88 90 92 94 96 98 100 102 104 106 108 110 112 114 116 118 120 122 124 126	9 11 13 15 1 3 5 7 25 27 29 31 17 19 21 23 41 43 45 47 33 35 37 39 57 59 61 63 73 75 77 79 65 67 69 71 89 91 93 95 81 83 85 87 105 107 109 111 97 99 101 103 121 123 125 127 113 115 117 119	13 7 1 11 5 15 9 3 29 23 17 21 31 25 19 25 45 39 33 43 37 47 41 35 61 55 49 53 63 57 51 77 71 65 75 69 73 67 93 87 81 91 85 95 89 83 109 103 97 101 111 105 99 125 119 113 123 127 120 117 121 115	0 10 4 14 8 2 12 6 16 26 20 30 24 18 28 22 32 42 36 46 40 34 44 38 48 58 52 62 56 50 60 54 64 74 68 78 72 66 76 70 80 90 84 94 88 82 92 86 96 106 100 110 104 98 108 102 112 122 116 126 120 114 124 118	5 15 9 3 13 7 1 11 21 31 19 29 23 17 27 37 47 41 35 45 39 33 43 37 47 53 63 57 67 77 69 79 73 83 93 87 97 89 79 69 59 49 39 29 19 9 1 11 21 31 41 51 61 71 81 91 101 111 121 131 141 151 161 171 181 191 201 211 221 231 241 251 261 271 281 291 301 311 321 331 341 351 361 371 381 391 401 411 421 431 441 451 461 471 481 491 501 511
Empty Plane with Wires Running from Inside of Plane to Connectors	Empty Planes For Transpositions	Empty Planes For Transpositions	Empty Planes For Transpositions		

Table 3

Table 3

"EAST"
(Outside View)

0 ↔ 12		13 ↔ 25		26 ↔ 38		39 ↔ 51	
127	126	126	119	115	118	118	123
125	124	124	117	121	124	124	113
123	122	122	115	127	114	114	119
121	120	120	113	117	120	120	125
119	118	118	127	123	126	126	115
117	116	116	125	113	116	116	121
115	114	114	123	119	122	122	127
113	112	112	121	125	112	112	117
111	110	110	103	99	102	102	107
109	108	108	101	105	108	108	97
107	106	106	99	111	98	98	103
105	104	104	97	101	104	104	109
103	102	102	111	107	110	110	99
101	100	100	109	97	100	100	105
99	98	98	107	103	106	106	111
97	96	96	105	109	96	96	101
95	94	94	87	83	86	86	91
93	92	92	85	89	92	92	81
91	90	90	83	95	82	82	87
89	88	88	81	85	88	88	93
87	86	86	95	91	94	94	83
85	84	84	93	81	84	84	89
83	82	82	91	87	90	90	95
81	80	80	89	93	80	80	85
79	78	78	71	67	70	70	75
77	76	76	69	73	76	76	65
75	74	74	67	79	66	66	71
73	72	72	65	69	72	72	77
71	70	70	79	75	78	78	67
69	68	68	77	65	68	68	73
67	66	66	75	71	74	74	79
65	64	64	73	77	64	64	69
63	62	62	55	51	54	54	59
61	60	60	53	57	60	60	49
59	58	58	51	63	50	50	55
57	56	56	49	53	56	56	61
55	54	54	63	59	62	62	51
53	52	52	61	49	52	52	57
51	50	50	59	55	58	58	63
49	48	48	57	61	48	48	53
47	46	46	39	35	38	38	43
45	44	44	37	41	44	44	33
43	42	42	35	47	34	34	39
41	40	40	33	37	40	40	45
39	38	38	47	43	46	46	35
37	36	36	45	33	36	36	41
35	34	34	43	39	42	42	47
33	32	32	41	45	32	32	37
31	30	30	23	19	22	22	27
29	28	28	21	25	28	28	17
27	26	26	19	31	18	18	23
25	24	24	17	21	24	24	29
23	22	22	31	27	30	30	19
21	20	20	29	17	20	20	25
19	18	18	27	23	26	26	31
17	16	16	25	29	16	16	21
15	14	14	7	3	6	6	11
13	12	12	5	9	12	12	1
11	10	10	3	15	2	2	7
9	8	8	1	5	8	8	13
7	6	6	15	11	14	14	3
5	4	4	13	1	4	4	9
3	2	2	11	7	10	10	15
1	0	0	9	13	0	0	5

Empty Plane with Wires Running from Inside of Plane to Connectors

For Transpositions

Empty Planes

For Transpositions

Empty Planes

For Transpositions

Empty Planes

Empty Plane with Wires Running from Inside of Plane to Terminating Resistors

Table 4

Table 4

"WEST"
(Outside View)

0 ↔ 12	13 ↔ 25	26 ↔ 38	39 ↔ 51
0	1	0	5
2	3	10	15
4	5	4	9
6	7	14	3
8	9	8	13
10	11	2	7
12	13	12	1
14	15	6	11
16	17	16	21
18	19	26	31
20	21	20	25
22	23	30	19
24	25	24	29
26	27	18	23
28	29	28	17
30	31	22	25
32	33	32	19
34	35	34	45
36	37	36	39
38	39	46	33
40	41	40	43
42	43	34	37
44	45	44	47
46	47	38	41
48	49	48	35
50	51	50	61
52	53	52	55
54	55	54	49
56	57	56	59
58	59	58	53
60	61	60	63
62	63	62	57
64	65	64	51
66	67	66	61
68	69	68	55
70	71	70	49
72	73	72	59
74	75	74	53
76	77	76	63
78	79	78	57
80	81	80	61
82	83	82	63
84	85	84	57
86	87	86	51
88	89	88	77
90	91	90	71
92	93	92	65
94	95	94	75
96	97	96	69
98	99	98	73
100	101	100	77
102	103	102	79
104	105	104	73
106	107	106	67
108	109	108	71
110	111	110	65
112	113	112	75
114	115	114	69
116	117	116	73
118	119	118	77
120	121	120	71
122	123	122	65
124	125	124	75
126	127	126	69

Empty Plane with Wires Running from Inside of Plane to Connectors

For Transpositions

Empty Planes

For Transpositions

Empty Planes

For Transpositions

Empty Planes

Empty Plane with Wires Running from Inside of Plane to Terminating Resistors

Table 5

Table 5



CONTROL DATA
CORPORATION

COMPUTER DIVISION

501 PARK AVENUE, MINNEAPOLIS 15, MINNESOTA