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**CONTROL DATA®  
3000 SERIES COMPUTER SYSTEMS**

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**INPUT/OUTPUT  
SPECIFICATION MANUAL**



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## **SCOPE AND PURPOSE**

This specification applies to all devices used as external equipments with the 3000 series of computing systems. The purpose of this specification is to describe a uniform set of operating characteristics, consistent with accepted engineering practices and moderate hardware requirements, which will apply to all equipments.

## **CONTENTS**

This specification contains brief descriptions of the data channel interfaces and the basic operations. Tables 1, 2, and 3 define in detail the transmitted signals and their relation to the operations. Tables 4, 5, and 6 list signal and pin assignments in the cables.

### **APPENDIXES**

Appendix A discusses the physical characteristics and dimensions of the 29-pair signal cable and the 61-pin connector. Appendix B describes the electronic characteristics and operation of transmitter and receiver circuits and the twisted-pair transmission line. Appendix C contains schematic diagrams of the various types of transmitters and receivers currently in use.

**NOTE:** The items presented in the appendix section are subject to change by Engineering Change Order. The information given was valid and accurate as of revision C of this manual.

## **DATA CHANNEL INTERFACES**

A 3000 series computing system communicates with external equipment via bi-directional data channels. The standard 12-bit data channel transmits and receives information in the form of 12-bit bytes. The data channel contains assembly/disassembly logic as required. The special 24-bit and 48-bit channels communicate in 24-bit and 48-bit bytes, respectively.

## OPERATIONS

### CONNECT

A data channel may have eight possible equipments attached to its set of I/O cables. These are selected individually by means of the Connect instruction. A 12-bit connect code is transmitted; the upper 3 bits select one of the eight equipments and the lower 9 bits select the unit (if any) of that equipment. This is accomplished by a Connect signal (delayed 0.2 usec) directing all eight equipments to examine the code. The selected equipment returns a Reply or Reject, according to whether it is available for connection.

### FUNCTION

Various operating modes and conditions (such as Interrupt) are specified using the Function instruction. The 12-bit function code is placed on the data lines and a Function signal (delayed 0.2 usec) is sent. The connected external equipment responds by returning the Reply or the Reject signal. If the connected equipment is capable of executing the specified function at the time it receives the signal, it initiates the function and returns the Reply signal. If the connected equipment is not capable of performing the specified function at this time, it returns the Reject signal.

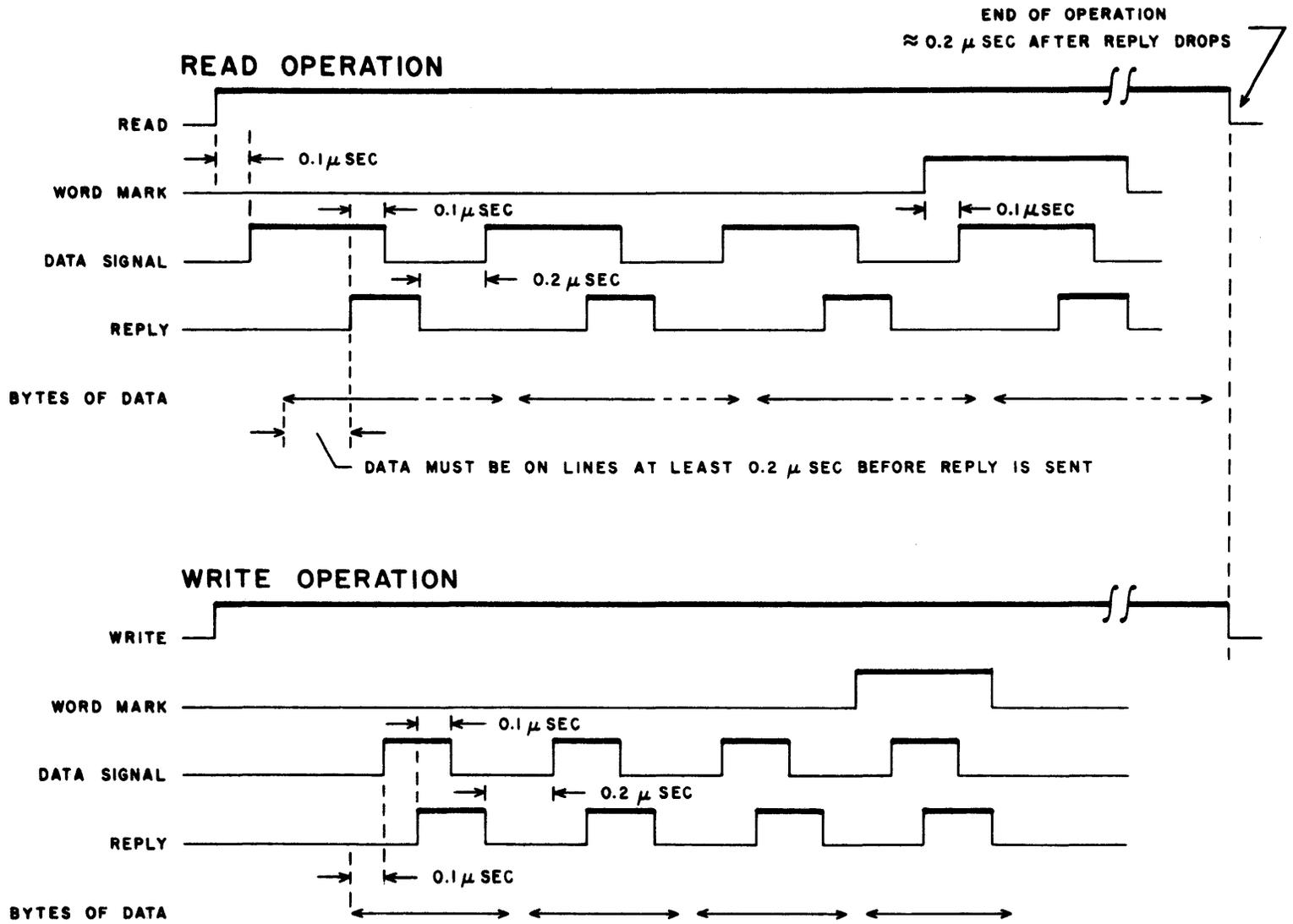
### READ

The signals transmitted during a read operation are as follows, and the timing sequence is shown in figure 1.

The read line comes up at the beginning of a read operation and remains up during the entire time of the operation. The Data signal is brought up when the channel is ready to accept data from the external equipment. When the external equipment has a word ready, it puts it on the data lines and sends the Reply signal. If the external equipment has reached an end of record condition, it sends the End of Record signal instead of the Reply, causing the read line to drop. The channel brings up the word mark line coincident with the Data signal during the transfer of the final byte.

### WRITE

The signals transmitted during a write operation are as follows, and the timing sequence is shown in figure 1.



NOTE: This figure uses the standard 12-bit channel as an example.

Figure 1. Signal Timing

The write line comes up at the beginning of a write operation and remains up during the entire time of the operation. The Data signal is brought up when the channel has placed data on the data lines. When the external equipment has sampled the data lines, it returns a Reply signal. The channel brings up the word mark line coincident with the Data signal during the final byte.

#### ALL OPERATIONS

In response to a Connect, Function, or Data signal, the external equipment returns a Reply, Reject, or End of Record. The channel then acknowledges the Reply, Reject, or End of Record by dropping the Connect, Function or Data signal. This in turn causes the external equipment to drop its Reply, Reject or End of Record.

**TABLE 1**  
**Bidirectional Signals**

Signal	Definition
Data Bits	<p>The lines which carry data are bidirectional and perform as follows:</p> <ol style="list-style-type: none"> <li>1. During a read (input) operation, data is transmitted from the external equipment to the channel.</li> <li>2. During a write (output) operation, data is transmitted from the channel to the external equipment.</li> <li>3. The connect code and function code are transmitted from the channel to the external equipment via the 12 data lines. In 24-bit and 48-bit interfaces, these codes are carried by the lower 12 lines (numbers 00 through 11).</li> </ol>
Parity Bit	<p>A parity bit accompanies each 12 bits transmitted between the channel and external equipment. Odd parity is used; thus the total number of "1's" transmitted is always an odd number. Parity bits accompany the connect code, the function code, and each 12 bits of data.</p>

**TABLE 2**  
**Signals from Data Channel to External Equipment**

Signal	Definition
Connect	<p>"1" signal sent to external equipment when 12-bit connect code is available on data lines. If the equipment is available, it connects and returns the Reply signal. If it is not available, it returns the Reject signal. The Connect signal and code drop when the external equipment returns the Reply or Reject.</p> <p>A data channel may have a maximum of eight external equipments attached to its set of I/O cables. The 12-bit connect code and the Connect signal are received by all eight equipments, but only one equipment (the equipment number switch setting of which matches the upper 3 bits of the connect code) will respond. (The other equipments do not return Reject signals.)</p> <p>No response is returned by any of the equipments if a parity error exists on the connect code; however, the Transmission Parity Error indicators on all equipments will light. After a delay of 100 microseconds, the computation module generates its own internal Reject.</p> <p>A connect code does not initiate any action, but merely selects an external equipment. The upper 3 bits of the connect code select one of the eight possible equipments attached to the data channel, and the lower 9 bits specify the unit (if any) of that equipment</p> <p>A connect code matching its equipment number switch setting will be accepted by the equipment if it is available, although it may be in the Not Ready condition. The connect code will be Rejected only if the equipment is already connected to or reserved by another data channel, or is otherwise not available. The equipment will, however, enable its status lines to the channel which attempted</p>

TABLE 2 (Cont'd)  
Signals from Data Channel to External Equipment

Signal	Definition
Connect (Cont'd)	<p>to connect, so that the reason for the Reject may be determined using the Copy Status instruction. The status lines remain enabled to that channel until it transmits another connect code to any of its external equipments.</p> <p>Once an equipment is connected to a data channel, it remains connected until the channel initiates a disconnect. Any connect code which does not match its equipment number switch setting will disconnect the equipment, including its status lines. The equipment must be capable of recognizing the code and disconnecting within 1 microsecond after receiving the Connect signal. When being selected, the equipment must not return a Reply or Reject earlier than 2 microseconds after receiving the Connect signal.</p> <p style="text-align: center;">NOTE</p> <p>In equipment designed after May 1, 1966, the leading edge of a Connect signal will simultaneously clear all Transmission Parity Error conditions existing in equipment attached to the data channel. Parity is checked after the clear on the current connect code. This clearing has no effect on other conditions, e. g. Interrupt in any equipment. Refer to the appropriate Reference Manual for information on specific peripheral equipment.</p>
Function	<p>"1" signal sent to external equipment when 12-bit function code is available on data lines. If the connected equipment is capable of executing the specified function at the time that it receives the Function signal, it initiates the function and returns the Reply signal. If the equipment cannot perform the function, it returns the Reject signal. The Function signal and code drop when the external equipment returns the Reply or Reject.</p> <p>The 12-bit function code and Function signal are received by all the equipments attached to the data channel, but only the connected equipment will respond. If no equipment is connected, the Function signal and code will be completely ignored. After a delay of 100 microseconds, the computation module generates its own internal Reject.</p>

**TABLE 2 (Cont'd)**  
**Signals from Data Channel to External Equipment**

Signal	Definition
Function (Cont'd)	<p>The specified function will not be performed if a parity error exists on the function code; however, a Parity Error signal is returned by the connected equipment. Also, the Transmission Parity Error indicator on the connected equipment will light.</p> <p>Once a function code is accepted, all other function codes will be locked out until the first one is acted upon. An equipment does not hold or stack up the function codes; a Reply or Reject is returned immediately. If a second function code is received which specifies the same function as the previous function code, the second function code will be rejected unless the function can immediately be performed a second time.</p>
Channel Busy	<p>Static "1" signal sent to external equipment while data channel is active during a read or write operation. The Channel Busy signal becomes "1" immediately when the computation module initiates the read or write operation and remains up until the operation is finished and no further chaining is specified. It does not drop between blocks of data in a chain, nor does it drop when an End of Record signal is received unless the End of Record actually terminates the operation.</p> <p>The connected equipment immediately becomes Busy (status response bit 01) when the channel busy line goes to "1", unless it is already Busy or is Not Ready. If the equipment is already Busy finishing a previous operation, it remains Busy and begins the new operation as soon as possible. The equipment does not become Busy if it is Not Ready; however, if the equipment becomes Ready while the Channel Busy signal is up, the equipment will become Busy.</p>

**TABLE 2 (Cont'd)**  
**Signals from Data Channel to External Equipment**

Signal	Definition
Read	Static "1" signal directing the connected equipment to begin reading information from its storage medium, and to continue as long as the Read signal is present. The read operation always starts at the beginning of a record. If the Read signal drops before the complete record is read, data transmission stops but the external equipment continues its action until the end of record is reached. If the Read signal drops and comes back up within a record, data transmission stops and does not begin again until the beginning of the next record
Write	Static "1" signal directing the connected equipment to begin writing information into its storage medium, and to continue as long as the Write signal is present. The write operation always starts at the beginning of a record. Each time the Write signal drops, the external equipment automatically ends the record.
Master Clear	"1" signal from computation module which returns data channel and external equipment to zero initial conditions and disconnects external equipment.
Data Signal	"1" signal used during read and write operations. Data signal drops when Reply (or End of Record) is received from external equipment. 1) During a read operation, the Data signal indicates that the channel is ready to accept data from the external equipment. 2) During a write operation, the Data signal indicates that the channel has placed output data on the data lines.
Computer Running	Static "1" when computer is operating

TABLE 2 (Cont'd)  
Signals from Data Channel to External Equipment

Signal	Definition
Negate BCD Conversion	<p>Static "1" signal which indicates that the computation module is operating in the 1604 mode. 1) During a read operation, this signal directs the external equipment to not convert BCD codes from external to internal. 2) During a write operation, this signal directs the external equipment to not convert BCD codes from internal to external.</p>
Suppress Assembly/Disassembly	<p>Many peripheral equipments handle data in the form of 6-bit bytes. These equipments and their controllers contain assembly/disassembly logic as required to convert between the 12-bit word length of the standard data channel and the 6-bit capability of the equipment. Normally, during a Read (input) operation, two 6-bit bytes are assembled into a 12-bit word; during a Write (output) operation, the opposite occurs.</p> <p>A "1" signal on the Suppress Assembly/Disassembly line prevents this conversion from occurring. This signal directs the equipment to utilize only the lower 6 bits (bits 00 - 05) of the 12-bit word. During a Read operation, bits 06-11 will be "0's"; during a Write operation, any data in bits 06-11 will not be used.</p> <p>Any equipment or controller which does not normally perform 12-bit/6-bit assembly and disassembly will ignore the Suppress Assembly/Disassembly signal.</p> <p>The Suppress Assembly/Disassembly signal comes up simultaneously with the Read or Write signal and drops when the Read or Write signal drops.</p>

TABLE 2 (Cont'd)  
Signals from Data Channel to External Equipment

Signal	Definition
Sample Status Time (A special signal)*	A "1" signal sent to the external equipment when the status sense lines have been enabled. The signal is used by the external equipment to clear specific status FF's. **
Word Mark	<p>A "1" signal sent to external equipment together with certain of the Data Signals on both Read and Write operations. The Word Mark signal comes up 0.1 microsecond in advance of the Data Signal, and remains up for the duration of the Data Signal.</p> <p>The Word Mark signal identifies the low-order byte of every addressed word, as follows:</p> <ol style="list-style-type: none"> <li>1. If the I/O operation is computer word addressed, the Word Mark will accompany the Data Signal for the final byte (bits 11 - 00) of the computer word.</li> <li>2. If the I/O operation is byte addressed or character addressed, the Word Mark will accompany every Data Signal because every Data Signal controls the transmission of an entire addressed word.</li> </ol>
Clear External Interrupt, Special Signal	A "1" signal sent to the source of an Interrupt external to the computer system, directing that external source to drop its Interrupt signal. This condition does not apply to standard peripheral equipments, but has application on special real-time devices. (This signal can be generated only by the 3100 and 3200 computers.)

\* Generated by 3100, 3200, 3300 and 3500 Computer Systems only.

\*\* Not used by all peripherals; refer to individual equipments to determine if the signal is used, and which status FF's are affected.

**TABLE 3**  
**Signals from External Equipment to Data Channel**

Signal	Definition
Reply	<p>"1" signal produced by external equipment in response to a Connect, Function, or Data signal. Signal drops when Connect, Function, or Data signal drops.</p> <ol style="list-style-type: none"> <li>1. If connection can be made when Connect signal is received, external equipment connects and returns a Reply.</li> <li>2. If specified function can be performed when Function signal is received, external equipment initiates function and returns a Reply.</li> <li>3. During a read operation, external equipment sends a Reply as soon as it has placed data on the data lines in response to the Data signal.</li> </ol> <p>During a write operation, external equipment sends a Reply as soon as it samples the data lines in response to the Data signal.</p> <p>(If end of record is reached during a read operation, the Reply is not returned in response to the Data signal. Instead, the external equipment transmits the End of Record signal.)</p>
Reject	<p>"1" signal produced by external equipment in response to a Connect or Function signal if the connection cannot be made or the function cannot be performed at the time that the external equipment receives the respective signal.</p>
End of Record	<p>"1" signal produced (instead of Reply) in response to the next Data signal following the end of every record during a read operation. The End of Record signal drops when the Data signal drops.</p>

**TABLE 3 (Cont'd)**  
**Signals from External Equipment to Data Channel**

Signal	Definition
End of Record (Cont'd)	<p>If the Read signal drops before the end of record is reached, the End of Record signal is not sent because none of the remaining data in the record is transmitted, although the external equipment continues its action until the end of record is reached. (This applies even though the Read signal may have dropped and come back up again within a record. See definition for Read signal.)</p> <p>Records of data written on magnetic tape are separated by blank spaces called inter-record gaps. In the case of punched cards, each card is a record.</p>
Parity Error	<p>"1" signal produced if data channel does not send an odd number of "1's" in 12 bits plus parity bit. (A parity bit accompanies each 12 bits; the 24-bit channel sends 2 parity bits and the 48-bit channel sends 4 parity bits. The external equipment checks each 12-bit portion separately and if there are any errors, it sends the Parity Error signal.) A transmission Parity Error condition can be cleared by a Master Clear signal.</p> <p style="text-align: center;">NOTE</p> <p>In equipment designed after May 1, 1966, a Transmission Parity Error condition can be cleared by a Connect operation. (See definition of Connect signal.)</p> <p>The following events occur when a parity error is detected.</p> <ol style="list-style-type: none"> <li>1. Parity Error on Connect Code <ol style="list-style-type: none"> <li>a. No equipment will connect.</li> <li>b. Any connected equipment will disconnect.</li> <li>c. No equipment returns a Reply or Reject.</li> <li>d. No equipment returns a Parity Error signal.</li> <li>e. The Transmission Parity Error indicators on all equipments attached to the data channel will light.</li> </ol> </li> <li>2. Parity Error on Function Code <ol style="list-style-type: none"> <li>a. Nothing happens if no equipment is connected.</li> <li>b. If an equipment is connected, the following occurs: <ol style="list-style-type: none"> <li>1) It returns a Parity Error signal.</li> <li>2) Its Transmission Parity Error indicator will light.</li> </ol> </li> </ol> </li> </ol>

**TABLE 3 (Cont'd)**  
**Signals from External Equipment to Data Channel**

Signal	Definition
<b>Parity Error (Cont'd)</b>	<ul style="list-style-type: none"> <li>3) It does not return a Reply or Reject.</li> <li>4) It does not perform the function.</li> </ul> <p>3. Parity Error on Data during Write Operation</p> <ul style="list-style-type: none"> <li>a. Nothing happens if no equipment is connected</li> <li>b. If an equipment is connected, the following occurs: <ul style="list-style-type: none"> <li>1) It returns a Parity Error signal.</li> <li>2) Its Transmission Parity Error indicator will light.</li> <li>3) It uses the data.</li> <li>4) It returns a Reply.</li> </ul> </li> </ul>
<b>Status Bits</b>	<p>The external equipment indicates its operating conditions by placing information on the 12 status lines. Each equipment has its own particular set of status response codes, some of which are unique to that equipment. Several status indications are normally common to all equipments, however, and occupy the same bit positions in the status response codes for all equipments. These are:</p> <p><u>Ready, Bit 00 = "1"</u></p> <p>An equipment is Ready if, when properly connected, a Read or Write signal can initiate a read or write operation. An equipment is Not Ready if, when properly connected, a Read or Write signal cannot initiate a read or write operation. Once Ready, an equipment remains continually Ready until operation is no longer possible; it then becomes Not Ready. An equipment cannot become Not Ready while it is actually transferring information; information transfer must first be halted.</p>

TABLE 3 (Cont'd)  
Signals from External Equipment to Data Channel

Signals	Definition
Status Bits (Cont'd)	<p>Any equipment which requires manual intervention in its normal operation (such as loading tape, cards, paper, etc.) is provided with switches to put it in either a manual mode or a computer controlled mode. When in the manual mode, the equipment is Not Ready. An equipment that has become Not Ready because of the need for manual intervention automatically goes into the manual mode. It becomes Ready again only after it has been attended to and manually switched back into the computer controlled mode.</p> <p><u>Busy, Bit 01 = "1"</u> An equipment is Busy when it is in operation. The equipment becomes Busy immediately upon initiation of the read or write operation.</p> <p>Normally, an equipment remains Busy until it has finished all activity and is ready to perform another operation; it then becomes Not Busy. However, an equipment will become Not Busy if a condition arises due to which the equipment can no longer continue the operation. (An example of such a condition is becoming Not Ready because of running out of cards, paper, etc. An equipment cannot be Busy if it is Not Ready.)</p> <p><u>Error, Bit 10 = "1"</u> This signal indicates information errors produced and detected by the external equipment. It does not indicate parity errors on information received from the data channel; the parity error line is reserved for this. It is not an indication of malfunction such as paper tearing or printed circuit card failure.</p> <p>If a read or write operation includes more than one record, the error bit is not cleared between records, but will indicate an error anywhere in the operation.</p>

TABLE 3 (Cont'd)  
Signals from External Equipment to Data Channel

Signal	Definition
Status Bits (Cont'd)	<p>The error indication is cleared by beginning a new operation.</p> <p><u>Reserved, Bit 11 = "1"</u></p> <p>This bit is used by multi-channel peripheral equipment to indicate that the equipment is reserved by one of the data channels to which it is attached. Once a multi-channel equipment has been connected by a data channel, it remains reserved by that channel even though the operation may terminate, the equipment may become Not Busy, and/or the channel may connect another equipment. No other data channel can communicate with the equipment until the first data channel releases the reservation. This may be done using the Master Clear facility, the Clear Channel instruction, or by issuing the appropriate function code.</p>
Status Bits 7, 8, & 9	<p>All equipment other than Magnetic Tape Controllers use status bits 7, 8, and 9 to indicate that the equipment has reached a certain pre-selected Interrupt condition and is producing an Interrupt signal because of it. Magnetic Tape Controllers, however, use status bits 7, 8, and 9 for other purposes. See below.</p> <p><u>All Equipment (except Magnetic Tape Controllers):</u></p> <p>Bit 07 = "1" Equipment has Interrupted on Ready and Not Busy.</p> <p>Bit 08 = "1" Equipment has Interrupted on End of Operation</p> <p>Bit 09 = "1" Equipment has Interrupted on Abnormal End of Operation</p> <p><u>Magnetic Tape Controllers, only:</u></p> <p><u>800 BPI, Bit 07 = "1"</u> The equipment is set to operate at a density of 800 bits per inch.</p>

**TABLE 3 (Cont'd)**  
**Signals from External Equipment to Data Channel**

Signal	Definition
Status Bits 7, 8, & 9 (Cont'd)	<p><u>Lost Data, Bit 08 = "1"</u></p> <p>This condition occurs if the Data signal from the data channel is not present when the equipment is ready to send data during a Read operation or to receive data during a Write operation. On a Read operation, reading continues to the end of the record; on a Write operation, tape motion stops immediately. Further Read or Write operations are impossible until the Lost Data condition is cleared by a new function. Any legal function code will clear the Lost Data condition. (The Lost Data condition can be cleared by a Master Clear, but this also disconnects the equipment.)</p> <p><u>End of Operation, Bit 09 = "1"</u></p> <p>This bit goes to a "0" whenever tape motion (except rewind) is initiated. It changes from "0" to "1" when an end of record is detected. Errors may be checked as soon as End of Operation status exists after Read, Write, Write File Mark, or Skip Bad Spot operations, even though tape is still in motion.</p> <p>During non-stop Read or Write data operations, new Read or Write operations may be initiated whenever End of Operation status exists from the previous Read or Write operation. Although errors may be checked when End of Operation occurs after Skip Bad Spot or Write File Mark operations, no new operation may be initiated until Not Busy status exists.</p> <p>During the execution of all select function instructions (except Write File Mark or Skip Bad Spot), End of Operation status is meaningless.</p>

TABLE 3 (Cont'd)  
Signals from External Equipment to Data Channel

Signal	Definition
Interrupt Lines	<p>A "1" signal on an interrupt line indicates that an external equipment has reached a predetermined condition. A data channel may communicate with a maximum of eight equipments, and each equipment uses one interrupt line. An interrupt signal may be dropped by reselecting the same selection, or by clearing the selection.</p> <p>Each equipment has a set of conditions upon which it will interrupt, if selected. Some of the interruptable conditions are common to all equipment and are described below.</p> <p><u>Interrupt on End of Operation</u></p> <p>With this selected, Interrupt will occur the next time an operation ends. The operation may be in progress at the time of the selection or it may be initiated later. Interrupt will not occur from an operation which has ended before the selection is made. Interrupt on end of operation can occur both at the end of an I/O read or write operation, and at the end of an operation specified by a function code. If a function code is accepted to initiate an operation that is already completed, an end of operation Interrupt will occur, if selected.</p> <p>Normally, the end of operation Interrupt for a read or write operation will occur when all data has been transferred, the Channel Busy signal has dropped, reading or writing of the current record is completed, and all error checking is completed. In some cases, this Interrupt may occur before the equipment becomes Not Busy. If for any reason (such as becoming Not Ready) the equipment is unable to continue the activity, the equipment will end its operation and Interrupt will occur.</p>

**TABLE 3 (Cont'd)**  
**Signals from External Equipment to Data Channel**

Signals	Definition
<p><b>Interrupt Lines (Cont'd)</b></p>	<p><u>Interrupt on Abnormal End of Operation</u>  This directs the external equipment to Interrupt if an operation ends under circumstances other than normal, such as becoming Not Ready or detecting an error. The operation may be in progress at the time of the selection or it may be initiated later. Interrupt will not occur from an operation which has ended before the selection is made, even though it may have ended under abnormal circumstances. If the equipment has become Not Ready before the Interrupt is selected, however, an attempt to initiate another operation after the selection is made will cause the equipment to Interrupt immediately.</p> <p>The equipment does not send the Interrupt signal while information is being transferred. All activity and information transfers are stopped at the most consistent point (such as at the end of the current record); then the Interrupt occurs. Automatic stopping on an error takes place only when this Interrupt is selected.</p> <p><u>Interrupt on Ready, or Interrupt on Ready and Not Busy</u>  The purpose of this Interrupt is to indicate that the external equipment is ready to start a new operation. It is often used to indicate the completion of any manual intervention.</p>
<p><b>Negate Channel Interrupt Lockout</b></p>	<p>The Negate Channel Interrupt Lockout is a signal produced by an equipment to accompany its Interrupt signal if the Interrupt has occurred because of an Abnormal End of Operation which prevented the equipment from completing a Read or Write operation. The Channel Interrupt Lockout condition is established by the computer to block the receipt of Interrupt signals from the equipments cabled to that data channel. The Negate Channel Interrupt Lockout signal, when generated by an external equipment to accompany its</p>

TABLE 3 (Cont'd)  
Signal from External Equipment to Data Channel

Signal	Definition															
Negate Channel Interrupt Lockout (Cont'd)	<p>Interrupt signal, will override the Lockout condition and will allow the channel to notify the computer that an Interrupt exists. All Interrupts present at the channel are then processed; the order of processing is not necessarily dependent upon the order received but may be determined by things such as program priority or a fixed-cycle scanner. The Negate Channel Interrupt Lockout signal drops when the Interrupt which it accompanied is processed; the channel then reverts back to the Interrupt Lockout condition.</p> <p>The purpose of the Negate Channel Interrupt Lockout signal is to prevent a possible "hang up" by the data channel if the computer had previously placed the channel in the Lockout condition and was waiting for the completion of the Read or Write operation. In this state, the channel could not accept the Interrupt on Abnormal End of Operation signal from the equipment, but neither could it complete the Read or Write operation.</p>															
Reverse Assembly	<p>This signal directs the data channel to reverse the order of byte positions when assembling a 48-bit word from data received from the equipment. The bytes are assembled as follows, using the standard 12-bit channel as an example:</p> <table style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;"></th> <th style="text-align: center; border-bottom: 1px solid black;">Normal</th> <th style="text-align: center; border-bottom: 1px solid black;">Reverse</th> </tr> </thead> <tbody> <tr> <td style="padding-left: 40px;">Byte 1</td> <td style="text-align: center;">Bits 47 - 36</td> <td style="text-align: center;">Bits 11 - 00</td> </tr> <tr> <td style="padding-left: 40px;">Byte 2</td> <td style="text-align: center;">Bits 35 - 24</td> <td style="text-align: center;">Bits 23 - 12</td> </tr> <tr> <td style="padding-left: 40px;">Byte 3</td> <td style="text-align: center;">Bits 23 - 12</td> <td style="text-align: center;">Bits 35 - 24</td> </tr> <tr> <td style="padding-left: 40px;">Byte 4</td> <td style="text-align: center;">Bits 11 - 00</td> <td style="text-align: center;">Bits 47 - 36</td> </tr> </tbody> </table>		Normal	Reverse	Byte 1	Bits 47 - 36	Bits 11 - 00	Byte 2	Bits 35 - 24	Bits 23 - 12	Byte 3	Bits 23 - 12	Bits 35 - 24	Byte 4	Bits 11 - 00	Bits 47 - 36
	Normal	Reverse														
Byte 1	Bits 47 - 36	Bits 11 - 00														
Byte 2	Bits 35 - 24	Bits 23 - 12														
Byte 3	Bits 23 - 12	Bits 35 - 24														
Byte 4	Bits 11 - 00	Bits 47 - 36														
24-Bit Device Present & Connected	<p>Certain 3100, 3200, and 3300 computer data channels can communicate with both 12-bit and 24-bit I/O devices. The channels provide 3 receptacles for the 3 cables used by 24-bit devices; and a 12-bit device on this type of channel does not use the third cable.</p> <p>The 24-Bit Device Present &amp; Connected is a signal produced by 24-bit equipment enabling the data channel to check parity on the upper 12 bits which are on the third cable.</p>															

A 3606 type 12-bit channel communicates with external equipment using 2 bidirectional 29-pair cables. Each 48-bit word is transmitted in the form of four 12-bit bytes, each of which is accompanied by a parity bit. The sequence of operation is shown in figure 1. The Word Mark signal accompanies the final 12-bit byte.

TABLE 4  
Standard 12-bit Channel Interface

CABLE A  
Data I/O Cable, Signal and Pin Assignments

Pin (two used)	Signal
A1-2	Data Bit 00
A3-4	Data Bit 01
A5-6	Data Bit 02
A7-8	Data Bit 03
A9-10	Data Bit 04
B1-2	Data Bit 05
B3-4	Data Bit 06
B5-6	Data Bit 07
B7-8	Data Bit 08
B9-10	Data Bit 09
C1-2	Data Bit 10
C3-4	Data Bit 11
C5-6	Parity Bit
C7-8	Channel Busy
C9-10	Reverse Assembly
D1-2	Read
D3-4	Write
D5-6	Connect
D7-8	Function
D9-10	Data Signal
E1-2	Reply
E3-4	Reject
E5-6	End of Record
E7-8	Parity Error
E9-10	(Unused)
F1-2	Word Mark
F3-4	Master Clear
F5-6	(Unused)
F7-8	(Unused)
*F9-10 (not in cable)	Termination Power

\*NOTE: The 29-pair cables terminate in 61-pin connectors. Pins F9-10 of each connector are used to provide power to the terminator assembly and do not connect to lines in the I/O cable.

TABLE 4 (Cont'd)  
Standard 12-bit Channel Interface

CABLE B  
Control I/O Cable, Signal and Pin Assignments

Pin (two used)	Signal
A1-2	Status Bit 00
A3-4	Status Bit 01
A5-6	Status Bit 02
A7-8	Status Bit 03
A9-10	Status Bit 04
B1-2	Status Bit 05
B3-4	Status Bit 06
B5-6	Status Bit 07
B7-8	Status Bit 08
B9-10	Status Bit 09
C1-2	Status Bit 10
C3-4	Status Bit 11
C5-6	Computer Running
C7-8	Negate BCD Conversion
C9-10	Suppress Assy-Disassy
D1-2	Interrupt Line 0
D3-4	Interrupt Line 1
D5-6	Interrupt Line 2
D7-8	Interrupt Line 3
D9-10	Interrupt Line 4
E1-2	Interrupt Line 5
E3-4	Interrupt Line 6
E5-6	Interrupt Line 7
E7-8	Clear External Interrupt
E9-10	Negate Channel Interrupt Lockout
F1-2	(Unused)
F3-4	(Unused)
F5-6	(Unused)
F7-8	Reserved, Special Signal
*F9-10 (not in cable)	Termination Power

\* NOTE:

The 29-pair cables terminate in 61-pin connectors. Pins F9-10 of each connector are used to provide power to the terminator assembly and do not connect to lines in the I/O cable.

A 3607 type 24-bit channel communicates with external equipments using 3 bidirectional 29-pair cables. Each 48-bit data word is transmitted in the form of two 24-bit bytes. A parity bit accompanies each 12 bits of data; thus a 24-bit byte is accompanied by two parity bits. The sequence of operation is the same as the 12-bit channel interface, with the Word Mark signal accompanying the final 24-bit byte.

TABLE 5  
Special 24-bit Channel Interface  
CABLE A  
Signal and Pin Assignments

Pin (two used)	Signal
A1-2	Data Bit 00
A3-4	Data Bit 01
A5-6	Data Bit 02
A7-8	Data Bit 03
A9-10	Data Bit 04
B1-2	Data Bit 05
B3-4	Data Bit 06
B5-6	Data Bit 07
B7-8	Data Bit 08
B9-10	Data Bit 09
C1-2	Data Bit 10
C3-4	Data Bit 11
C5-6	Parity Bit 1 (bits 00-11)
C7-8	Channel Busy
C9-10	(Unused)
D1-2	Read
D3-4	Write
D5-6	Connect
D7-8	Function
D9-10	Data Signal
E1-2	Reply
E3-4	Reject
E5-6	End of Record
E7-8	Parity Error
E9-10	(Unused)
F1-2	Word Mark
F3-4	Master Clear
F5-6	(Unused)
F7-8	(Unused)
*F9-10 (not in cable)	Termination Power

**\*NOTE**

The 29-pair cables terminate in 61-pin connectors. Pins F9-10 of each connector are used to provide power to the terminator assembly and do not connect to lines in the I/O cable.

**TABLE 5 (Cont'd)**  
**Special 24-bit Channel Interface**

**CABLE B**  
**Signal and Pin Assignments**

Pin (two used)	Signal
A1-2	Status Bit 00
A3-4	Status Bit 01
A5-6	Status Bit 02
A7-8	Status Bit 03
A9-10	Status Bit 04
B1-2	Status Bit 05
B3-4	Status Bit 06
B5-6	Status Bit 07
B7-8	Status Bit 08
B9-10	Status Bit 09
C1-2	Status Bit 10
C3-4	Status Bit 11
C5-6	Computer Running
C7-8	Negate BCD Conversion
C9-10	Suppress Assembly/Disassembly
D1-2	Interrupt Line 0
D3-4	Interrupt Line 1
D5-6	Interrupt Line 2
D7-8	Interrupt Line 3
D9-10	Interrupt Line 4
E1-2	Interrupt Line 5
E3-4	Interrupt Line 6
E5-6	Interrupt Line 7
E7-8	Clear External Interrupt
E9-10	Negate Channel Interrupt Lockout
F1-2	(Unused)
F3-4	(Unused)
F5-6	(Unused)
F7-8	Reserved, Special Signal
*F9-10 (not in cable)	Termination Power

**\*NOTE**

The 29-pair cables terminate in 61-pin connectors. Pins F9-10 of each connector are used to provide power to the terminator assembly and do not connect to lines in the I/O cable.

**TABLE 5 (Cont'd)**  
**Special 24-bit Channel Interface**

**CABLE C**  
**Signal and Pin Assignments**

Pin (two used)	Signal
A1-2	Data Bit 12
A3-4	Data Bit 13
A5-6	Data Bit 14
A7-8	Data Bit 15
A9-10	Data Bit 16
B1-2	Data Bit 17
B3-4	Data Bit 18
B5-6	Data Bit 19
B7-8	Data Bit 20
B9-10	Data Bit 21
C1-2	Data Bit 22
C3-4	Data Bit 23
C5-6	Parity Bit 2 (Bits 12-23)
C7-8	24-Bit Device Present &
C9-10	(Unused) Connected
D1-2	(Unused)
D3-4	(Unused)
D5-6	(Unused)
D7-8	(Unused)
D9-10	(Unused)
E1-2	(Unused)
E3-4	(Unused)
E5-6	(Unused)
E7-8	(Unused)
E9-10	(Unused)
F1-2	(Unused)
F3-4	(Unused)
F5-6	(Unused)
F7-8	(Unused)
*F9-10 (not in cable)	Termination Power

**\*NOTE:**

The 29-pair cables terminate in 61-pin connectors. Pins F9-10 of each connector are used to provide power to the terminator assembly and do not connect to lines in the I/O cable.

A 3608 type 48-bit channel communicates with external equipment using 3 bidirectional 29-pair cables. Each 48-bit data word is transmitted in the form of one 48-bit byte. A parity bit accompanies each 12 bits of data; thus a 48-bit byte is accompanied by four parity bits. The sequence of operation is the same as the 12-bit channel interface, with the Word Mark signal accompanying the 48-bit byte.

TABLE 6  
Special 48-bit Channel Interface

CABLE A  
Signal and Pin Assignments

Pin (two used)	Signal
A1-2	Data Bit 00
A3-4	Data Bit 01
A5-6	Data Bit 02
A7-8	Data Bit 03
A9-10	Data Bit 04
B1-2	Data Bit 05
B3-4	Data Bit 06
B5-6	Data Bit 07
B7-8	Data Bit 08
B9-10	Data Bit 09
C1-2	Data Bit 10
C3-4	Data Bit 11
C5-6	Parity Bit 1 (Bits 00-11)
C7-8	Channel Busy
C9-10	(Unused)
D1-2	Read
D3-4	Write
D5-6	Connect
D7-8	Function
D9-10	Data Signal
E1-2	Reply
E3-4	Reject
E5-6	End of Record
E7-8	Parity Error
E9-10	Data Bit 39
F1-2	Word Mark
F3-4	Master Clear
F5-6	Data Bit 40
F7-8	Data Bit 41
*F9-10 (not in cable)	Termination Power

\*NOTE: The 29-pair cables terminate in 61-pin connectors. Pins F9-10 of each connector are used to provide power to the terminator assembly and do not connect to lines in the I/O cable.

TABLE 6 (Cont'd)  
Special 48-bit Channel Interface

CABLE B  
Signal and Pin Assignments

Pin (two used)	Signal
A1-2	Status Bit 00
A3-4	Status Bit 01
A5-6	Status Bit 02
A7-8	Status Bit 03
A9-10	Status Bit 04
B1-2	Status Bit 05
B3-4	Status Bit 06
B5-6	Status Bit 07
B7-8	Status Bit 08
B9-10	Status Bit 09
C1-2	Status Bit 10
C3-4	Status Bit 11
C5-6	Computer Running
C7-8	Negate BCD Conversion
C9-10	Data Bit 42
D1-2	Interrupt Line 0
D3-4	Interrupt Line 1
D5-6	Interrupt Line 2
D7-8	Interrupt Line 3
D9-10	Interrupt Line 4
E1-2	Interrupt Line 5
E3-4	Interrupt Line 6
E5-6	Interrupt Line 7
E7-8	Data Bit 43
E9-10	Data Bit 44
F1-2	Data Bit 45
F3-4	Data Bit 46
F5-6	Data Bit 47
F7-8	Parity Bit 4 (Bits 36-47)
*F9-10 (not in cable)	Termination Power

**\*NOTE:**

The 29-pair cables terminate in 61-pin connectors. Pins F9-10 of each connector are used to provide power to the terminator assembly and do not connect to lines in the I/O cable.

TABLE 6 (Cont'd)  
Special 48-bit Channel Interface

CABLE C  
Signal and Pin Assignments

Pin (two used)	Signal
A1-2	Data Bit 12
A3-4	Data Bit 13
A5-6	Data Bit 14
A7-8	Data Bit 15
A9-10	Data Bit 16
B1-2	Data Bit 17
B3-4	Data Bit 18
B5-6	Data Bit 19
B7-8	Data Bit 20
B9-10	Data Bit 21
C1-2	Data Bit 22
C3-4	Data Bit 23
C5-6	Parity Bit 2 (Bits 12-23)
C7-8	Data Bit 24
C9-10	Data Bit 25
D1-2	Data Bit 26
D3-4	Data Bit 27
D5-6	Data Bit 28
D7-8	Data Bit 29
D9-10	Data Bit 30
E1-2	Data Bit 31
E3-4	Data Bit 32
E5-6	Data Bit 33
E7-8	Data Bit 34
E9-10	Data Bit 35
F1-2	Parity Bit 3 (Bits 24-35)
F3-4	Data Bit 36
F5-6	Data Bit 37
F7-8	Data Bit 38
*F9-10 (not in cable)	Termination Power

**\*NOTE:** The 29-pair cables terminate in 61-pin connectors. Pins F9-10 of each connector are used to provide power to the terminator assembly and do not connect to lines in the I/O cable.

## **DATA TRANSFER RATES**

The following pages are the results of tests performed to determine maximum input/output rates of 3000 Series computers under various conditions. The rates were determined using a variable-speed channel exerciser equipped to indicate a Lost Data condition. (The Lost Data Condition occurs when the speed of the exerciser exceeds the speed of the channel. See status bit definitions in Table 3.)

### **DEFINITIONS**

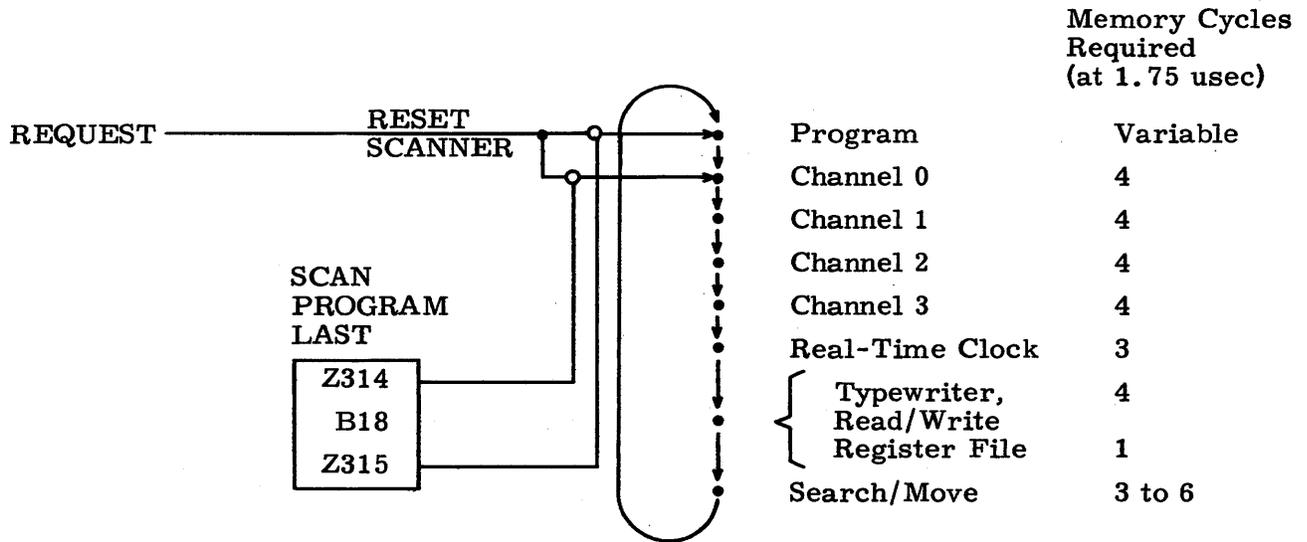
- 1) **Transfer Time** - the time in microseconds between the leading edges of successive Data Signals
- 2) **Maximum Rate** - a transfer time 10% greater than the time at which a Lost Data condition occurred

### **DATA FLOW ANALYSIS**

The following ground rules should be used in making data flow analysis calculations. (The figures contain a safety factor of approximately 10%).

- 1) The signal delay time along an I/O cable is 1.8 nanosec per foot.
- 2) The total circuit delay through a transmitter and receiver is 60 nanosec.
- 3) The total cable delay in a Ready/Resume signal exchange is 4 times 1.8 nanosec per foot, since the cable must be traversed by a total of 4 wavefronts.

3100 COMPUTER BLOCK CONTROL PRIORITY



All requests to Block Control are monitored by an eight-position scanner. When Block Control is not in use, the scanner is allowed to run free; however, when a request is received, the scanner is reset as follows:

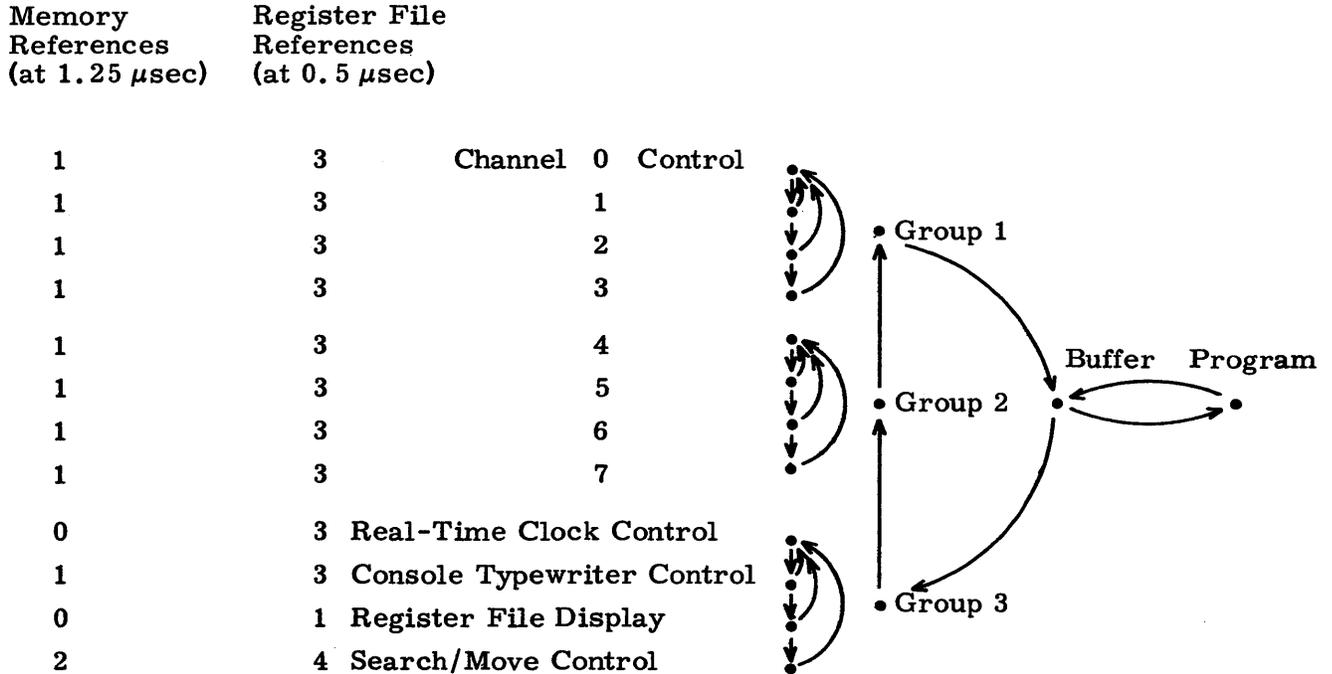
1. A request from any one of the I/O channels will reset the scanner to the Channel 0 position.
2. A request from any source except an I/O channel will reset the scanner to the Program position.
3. If a request from an I/O channel and a request from another source arrive simultaneously, the scanner will be reset to the Channel 0 position.

The technique of resetting the scanner with each request establishes definite priority in Block Control. It is therefore possible for fast I/O devices to monopolize the computer so that other sources including Program and Real-Time Clock cannot be serviced.

NOTE

The Pause instruction locks out Program requests for a 40 millisecond interval.

### 3200 COMPUTER BLOCK CONTROL PRIORITY



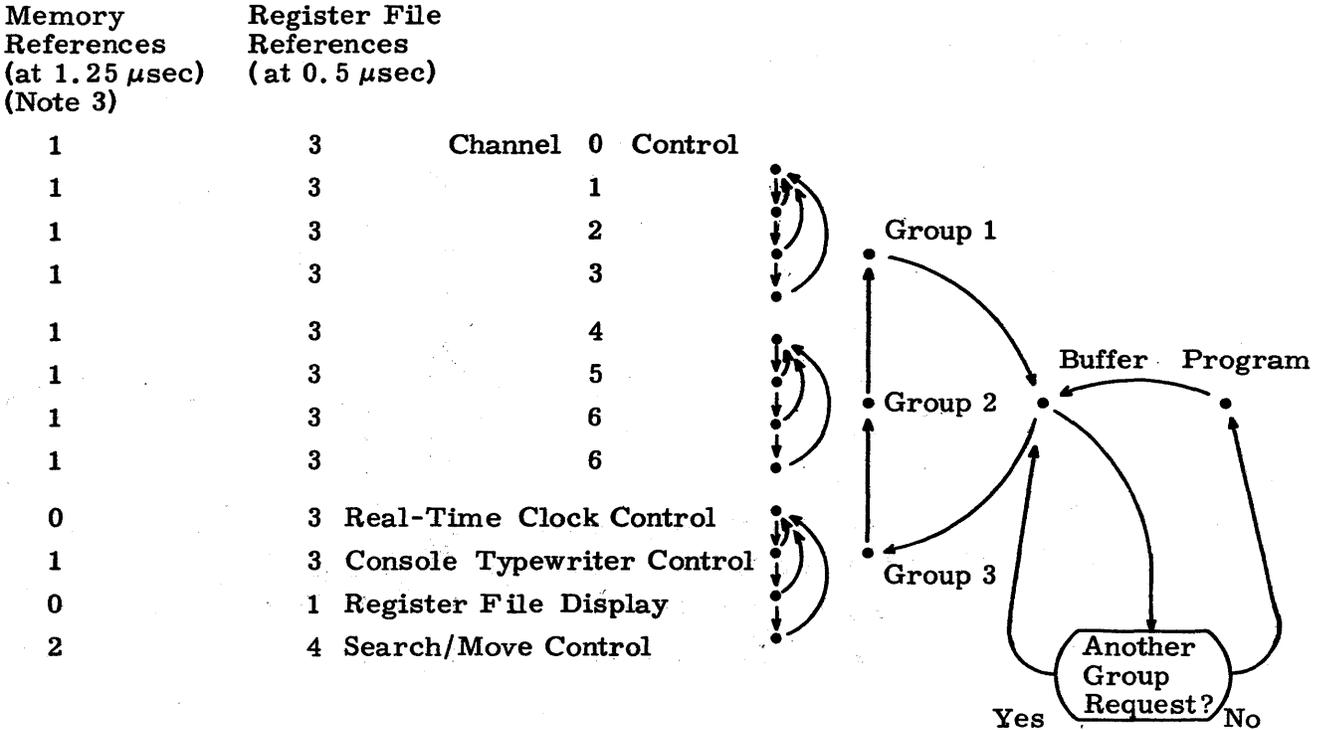
Requests to Block Control are monitored by a three-level scanner. Sequencing and priorities are as follows:

- 1) The Buffer/Program scanner alternately recognizes Buffer and Program requests on a one-for-one basis.
- 2) The Group scanner recognizes group requests sequentially in reverse order as shown.
- 3) The individual Group scanners monitor their sources in sequential order; however, at the conclusion of processing a request from any source in any group, all three Group scanners are reset to their starting positions.

Channels 0 and 4 and the Real-Time Clock have priority within the groups. Fast I/O devices on channels 0 and 4 are therefore able to monopolize the scanners so that devices on other channels cannot be recognized. The Real-Time Clock makes a request once each millisecond. It has the same priority as channels 0 and 4, and is recognized in turn.

NOTE: The Pause instruction locks out Program requests for a 40 millisecond interval.

### 3300 COMPUTER BLOCK CONTROL PRIORITY



Requests to Block Control are monitored by a three-level scanner. Sequencing and priorities are as follows:

- 1) The Buffer/Program scanner alternately recognizes Buffer and Program requests, but not necessarily on a one-for-one basis. Once the scanner stops in either the Buffer or Program position, it will be held until no more requests exist at that position. It is therefore possible for fast I/O devices generating overlapping requests to hold the scanner in the Buffer position indefinitely.
- 2) The Group scanner recognizes group requests sequentially in reverse order as shown.
- 3) The individual Group scanners monitor their sources in sequential order; however, at the conclusion of processing a request from any source in any group, all three Group scanners are reset to their starting positions.

Channels 0 and 4 and the Real-Time Clock have priority within the groups. Fast I/O devices on channels 0 and 4 are therefore able to monopolize the scanners so that devices on other channels cannot be recognized. The Real-Time Clock makes a request once each millisecond. It has the same priority as channels 0 and 4, and is recognized in turn.

- NOTES:
- 1) The Pause instruction locks out Program requests for a 40 millisecond interval.
  - 2) The Priority Pause instruction locks out both Program and Real-Time Clock requests for a 40 millisecond interval.
  - 3) Add 0.25  $\mu$ sec for relocation, if used.

### 3500 COMPUTER BLOCK CONTROL PRIORITY

Memory References (at 0.9 $\mu$ sec)*	Register File References (at 0.1 $\mu$ sec)	Request	Priority Order
0	0	MASTER CLEAR	1 (highest)
1	3	Channel 0	2
1	3	Channel 1	3
1	3	Channel 2	4
1	3	Channel 3	5
1	3	Channel 4	6
1	3	Channel 5	7
1	3	Channel 6	8
1	3	Channel 7	9
0	0/1/2**	PROGRAM REQUEST	10
0	3	REAL-TIME CLOCK	11
1	3	TYPEWRITER	12
1 Search 2 Move	3 Search 4 Move	SEARCH/MOVE	13 (lowest)

\*For an individual memory; overlapping of memory cycles or operation between memories will be less than 0.9  $\mu$ sec X No. of operations and/or cycles.

\*\*0, 1, or 2 references dependent upon the type of request.

#### Block Control

The Block Control section scans requests in the priority order shown above (except for the Special Scan conditions described below). With the exception of MASTER CLEAR, the priority network is I/O oriented and gives highest priority to the lowest numbered channel. Any lower numbered channel has priority over a higher numbered channel and therefore should be used to service the faster I/O devices in the system. Once a request is honored, the request scanning process is reset to Channel 0 and scanning recommences looking for the highest priority request that is active.

The main program requires access to Block Control to initiate I/O and Search/Move buffer operations. This initiation consists of storing modified forms of the instruction words in the Register File, hence providing available operating information (addresses, channel number, etc.) to Block Control. Once the desired I/O operation has been initiated, high priority is not given to further initiation. Table 7 lists the different buffer groups, in their normal order of priority, and also shows the priority within groups. Figure 2 is a flow diagram of the Priority Scheme.

TABLE 7. BUFFER GROUPS

GROUP 1	GROUP 2	GROUP 3
Channel 0 Channel 1 Channel 2 Channel 3	Channel 4 Channel 5 Channel 6 Channel 7	Program Real-time Clock Typewriter Search/Move

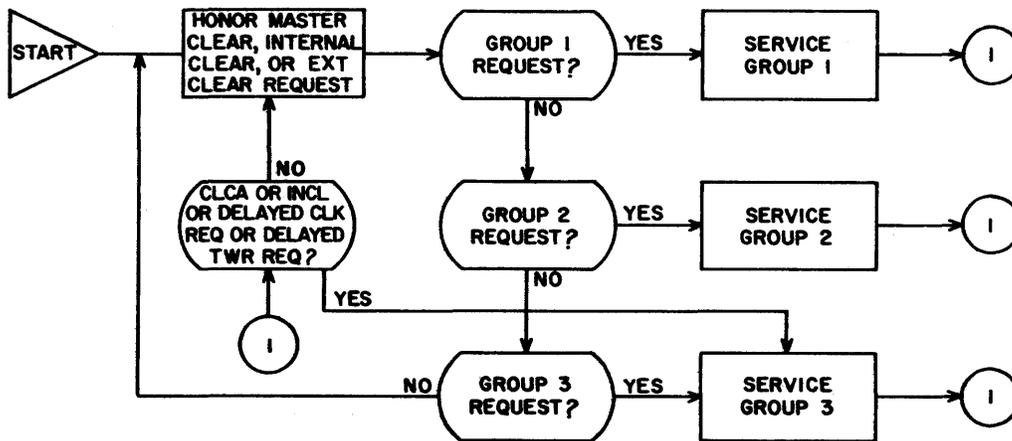


Figure 2. Block Control Priority Scheme

### Special Scan Logic

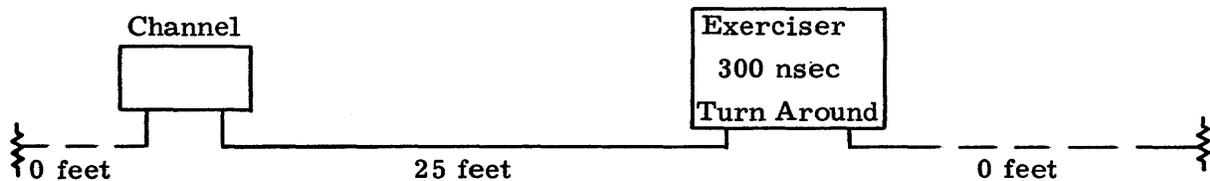
If the I/O system has not reached the maximum transfer rate, the requests in Group 3 are honored in their normal order of priority; however, since Block Control provides for maximum bursts of I/O without interruption, the honoring of a request to update the Real-time Clock, clear channels via program request instructions IOCL or CLCA, or service the typewriter, is delayed as long as possible so that the maximum burst rate may be achieved.

These delayed requests initiate the Special Scan logic which disables the normal scan logic. This prevents the Priority Network from resetting and results in the processing of all active requests even though of a lower priority. (It also prevents any new requests from being recognized until the existing requests have been honored.) Thus, any delayed requests are serviced with the highest priority after the delay. Figure 1-3 indicates the priority scheme; note that the Master Clear, Internal Clear, and External Clear requests are honored before any buffer requests.

The Real-time Clock must be updated once each millisecond; however, if a burst of I/O activity is occurring at the time the update is due, the clock will not be able to gain priority. In this case the Clock Request logic makes the request, and if it is not honored by the time the next Clock request is within 50  $\mu$ sec of being due, the Special Scan logic is triggered so the delayed request may gain priority.

The Type Load request from the console typewriter is also connected through the Special Scan logic to facilitate an I/O burst while ensuring that characters being typed in are not lost. The Special Scan logic is activated by the typewriter logic whenever a Type Load Request is waiting and it is mechanically possible for the next typewriter request to be generated.

I/O TRANSFER RATE TEST RESULTS: 3100 Computer System



Channel 0 - 3106

Channel 1 - 3106

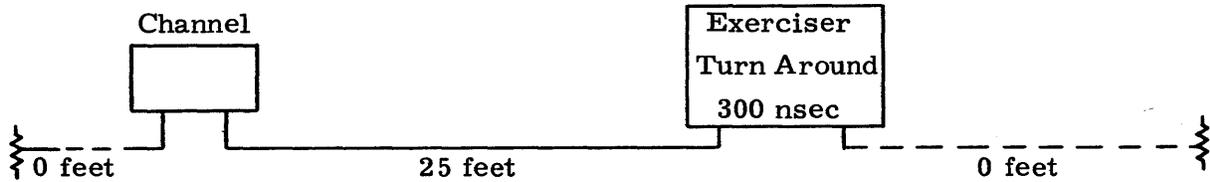
Maximum Rate  
(12-bit transfers)

- |      |                                                                                |                                                        |
|------|--------------------------------------------------------------------------------|--------------------------------------------------------|
| I.   | Best Case, I/O only. Pause used to lock out main control; clock disconnected.) |                                                        |
| A.   | Channel 0 active.<br>(Best case channel rate)                                  | 7.7 $\mu$ sec                                          |
| B.   | Channels 0 and 1 active.<br>(Best case block control rate)                     | Channel 0, 14.9 $\mu$ sec<br>Channel 1, 14.9 $\mu$ sec |
| II.  | I/O and Real-Time Clock. (Standard Pause used to lock out main control)        |                                                        |
| A.   | Channel 0 active.                                                              | 13.2 $\mu$ sec                                         |
| B.   | Channels 0 and 1 active.                                                       | Channel 0, 14.9 $\mu$ sec<br>Channel 1, 20.4 $\mu$ sec |
| III. | Standard Rate, with no inter-register transfers                                |                                                        |
| A.   | Channel 0 active.                                                              | 14.3 $\mu$ sec                                         |
| B.   | Channels 0 and 1 active.                                                       | Channel 0, 16.0 $\mu$ sec<br>Channel 1, 22.0 $\mu$ sec |
| IV.  | Standard Rate, no restrictions.<br>(Used Search instead of Move instruction)   |                                                        |
| A.   | Channel 0 active.                                                              | 15.4 $\mu$ sec                                         |
| B.   | Channels 0 and 1 active.                                                       | Channel 0, 18.0 $\mu$ sec<br>Channel 1, 23.1 $\mu$ sec |

REMARKS:

1. These figures are 10% above actual figures measured with the exerciser.
2. All times are average times and no buffering was done by the exerciser.

I/O TRANSFER RATE TEST RESULTS: 3200 Computer System



Channel 0 - 3206

Channel 1 - 3206

Maximum Rate  
(12-bit transfers)

- |      |                                                                                         |                                                        |
|------|-----------------------------------------------------------------------------------------|--------------------------------------------------------|
| I.   | Best Case, I/O only. (Priority Pause used to lock out main control and Real-Time clock) |                                                        |
| A.   | Channel 0 active.<br>(Best case channel rate)                                           | 2.8 $\mu$ sec                                          |
| B.   | Channels 0 and 1 active.<br>(Best case block control rate)                              | Channel 0, 4.5 $\mu$ sec<br>Channel 1, 4.5 $\mu$ sec   |
| II.  | I/O and Real-Time Clock. (Standard Pause used to lock out main control)                 |                                                        |
| A.   | Channel 0 active.                                                                       | 4.1 $\mu$ sec                                          |
| B.   | Channels 0 and 1 active.                                                                | Channel 0, 5.7 $\mu$ sec<br>Channel 1, 5.7 $\mu$ sec   |
| III. | Standard Rate, with no inter-register transfers.                                        |                                                        |
| A.   | Channel 0 active.                                                                       | 5.2 $\mu$ sec                                          |
| B.   | Channels 0 and 1 active.                                                                | Channel 0, 7.5 $\mu$ sec<br>Channel 1, 7.5 $\mu$ sec   |
| IV.  | Standard Rate, no restrictions.                                                         |                                                        |
| A.   | Channel 0 active.                                                                       | 9.4 $\mu$ sec                                          |
| B.   | Channels 0 and 1 active.                                                                | Channel 0, 12.1 $\mu$ sec<br>Channel 1, 15.4 $\mu$ sec |

REMARKS:

1. These figures are 10% above actual figures measured with the exerciser.
2. All times are average and no buffering was done by the exerciser.

WORST CASE - S/M CONTROL ACTIVE, REAL TIME CLOCK, IRT TRANSFERS, MAIN CONTROL

	CH. 0		CH. 1		CH. 2		CH. 3		CH. 4		CH. 5		CH. 6		CH. 7	
	3306	3307	3306	3306	3307	3306	3306	3307	3306	3306	3307	3306	3306	3307	3306	3306
A	12															
B	16		20													
C	16		23	40												
D	17		23	45		55										
E	16							16								
F	18		28					16								
G	19		28					19		28						
H		6														
I		7							8							
J		9			14				8							
K		10			15				10				15			
L		8	20													
M		10	25						9							
N		10	28						10	28						
O		8.5			10											
P		9	23		19											
Q		9	25		25	50										

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1. TRANSFER RATES ARE IN USEC FOR 12-BIT BYTES.
2. PRESENCE OF FIGURE INDICATES CHANNEL ACTIVE.
3. 3307 FIGURES ARE FOR 12→24 BIT ASSEMBLY.
4. TURN AROUND TIME OF EXERCISER IS 300 NSEC.
5. CABLE LENGTH BETWEEN CHANNEL AND EXERCISER IS 30 FT.
6. ADD 300 NSEC FOR RELOCATION.

RESTRICTED PROGRAMMING CASE- NO SEARCH/MOVE CONTROL BUSY  
 ALLOWS REAL TIME CLOCK, IRT TRANSFERS, MAIN CONTROL

	CH. 0		CH. 1		CH. 2		CH. 3		CH. 4		CH. 5		CH. 6		CH. 7	
	3306	3307	3306	3306	3307	3306	3306	3307	3306	3306	3307	3306	3306	3307	3306	3306
A	6.5															
B	9		9													
C	11		12	12												
D	11		13	14		15										
E	9						9									
F	12		12				10									
G	13		14				13		14							
H		3.3														
I		4.5						4.5								
J		6			6			5.5								
K		7			7			7					7			
L		5	9													
M		6	12					5.5								
N		7	14					7	14							
O		5			5											
P		5	12		6											
Q		5.3	13		7	16										

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SAME CONDITIONS HOLD FOR THIS CASE AS FOR  
 THE WORST CASE DATA.

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**I/O TRANSFER RATE TEST RESULTS**

The time necessary to transfer a 12-bit byte during an I/O operation is dependent upon the channel in use and the total number of channels active. The table indicates the time in microseconds to perform a 12-bit byte transfer (worst case) for the various channel active configurations. The restrictions under which the timing calculations were made are indicated below the table.

		CHANNEL NO.			
		0	1	2	3
No. of Channels Active	1	2.8	/	/	/
	2	3.7	3.7	/	/
	3	4.3	4.5	4.6	/
	4	4.3	5.1	5.3	5.4

**Restrictions:**

No Search/Move instructions

No "back door" access to memory

Maximum of 40' of cable to the peripherals

300 nanosecond turn-around time in the peripherals

3507 Channels operating in the 12-bit mode doing 24/12 bit disassembly

**APPENDIX A**  
**SIGNAL CABLE AND CONNECTOR**

## SIGNAL CABLE

A transmission line consists of two twisted-pair, 24 gauge conductors with Mylar insulation. A signal cable contains 29 transmission lines (58 conductors) combined into a cable approximately 5/8 inch in diameter with gray vinyl sheath. Each end of the cable is terminated in a 61-pin plug. Corresponding 61-socket receptacles are mounted in each cabinet. The weight of a signal cable is approximately 0.4 pound per foot. The signal cable does not carry terminator voltage or ground wires.

Signal cables can be made to order in any length to a maximum of 200 feet. Certain lengths which are carried in stock as standard items are listed below:

<u>Length</u>	<u>CDC Item Number</u>
30 inches	1285
36 inches	1286
10 feet	1287
14 feet	1294
20 feet	1288
25 feet	1289
30 feet	1290
40 feet	1291
50 feet	1292

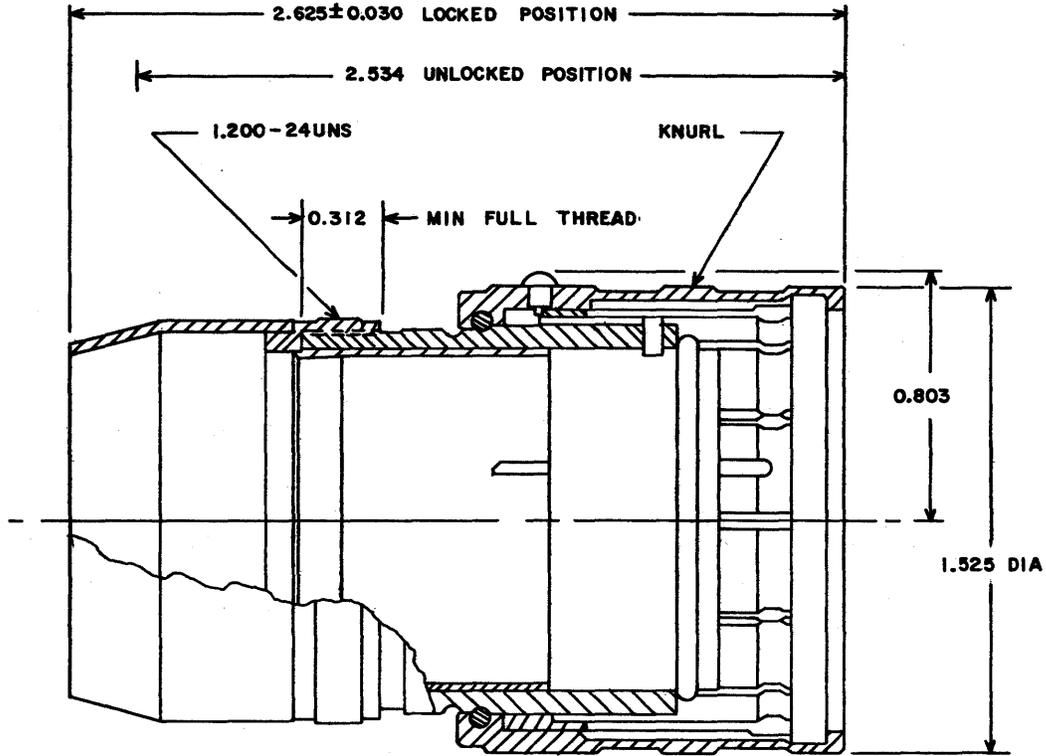
## 61-PIN CONNECTOR

Each end of the signal cable is equipped with a 61-pin male connector for attachment to a 61-socket cabinet receptacle. Dimensioned drawings of these items are shown on the following pages, which are excerpts from Control Data Specifications 300006 and 300009.

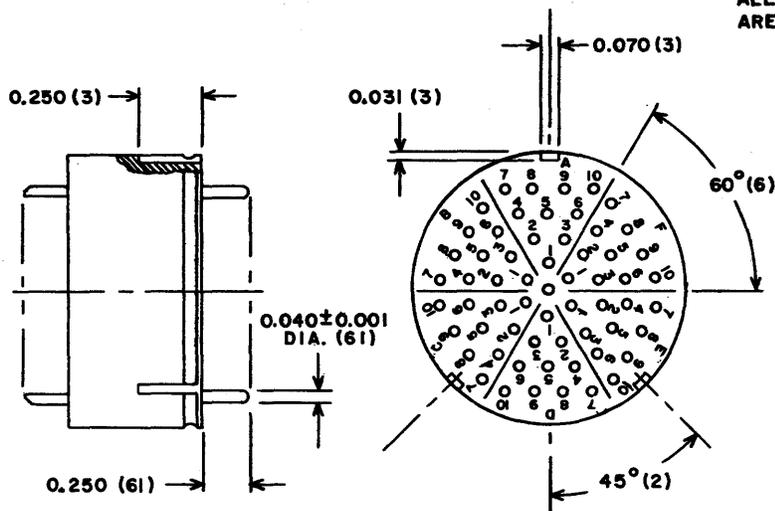
The connectors meet the following specifications:

Test Voltage	1000 volts RMS
Breakdown Voltage	1400 volts RMS
Current Rating	7.5 amperes

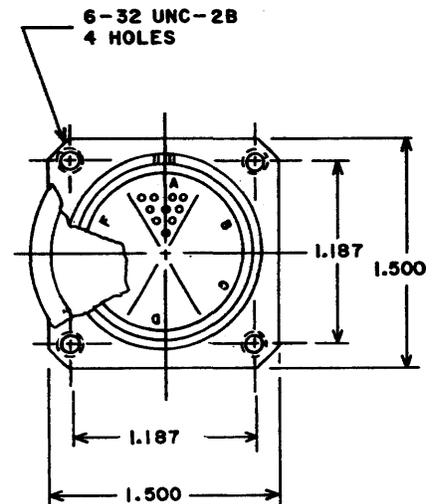
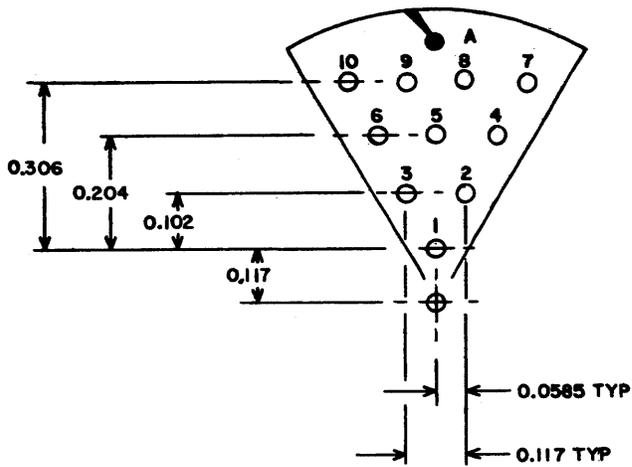
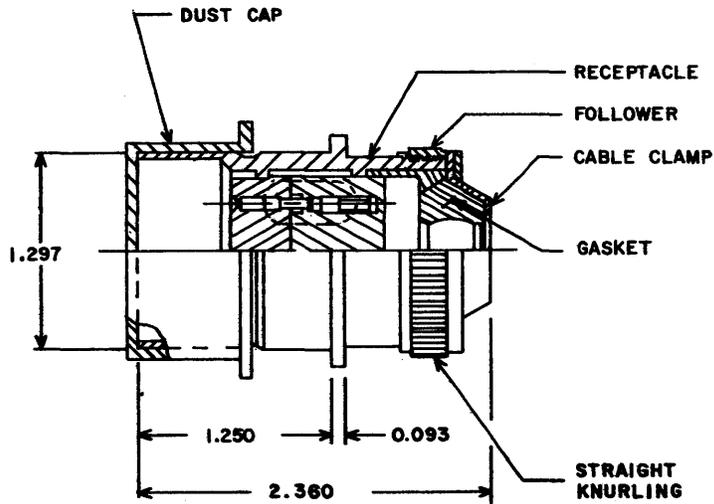
MALE CONNECTOR, 61 PIN  
 (both ends of cable)  
 CDC Part Number 300006



NOTE:  
 ALL MEASUREMENTS  
 ARE IN INCHES.



FEMALE CONNECTOR, 61 SOCKET  
 (Cabinet Chassis)  
 CDC Part Number 300009



NOTE:  
 ALL MEASUREMENTS ARE IN INCHES.



**APPENDIX B**  
**TRANSMITTER, RECEIVER, TRANSMISSION LINE**

## TERMINATOR POWER SUPPLY

In a 3000 series computing system, power for signal cable terminators is provided by a centrally located 40vdc supply. The terminators are connected in parallel to this supply, as shown in the accompanying diagram. The center ground of each terminator is a connection to the cabinet chassis. This provides an earth-ground reference for all terminators, since the cabinets in a 3000 series system have a common connection to earth ground.

The technique of using a common terminator power supply and earth grounds avoids problems of noise pickup that could otherwise occur because of differences in the reference levels of the transmitter and receiver. Decisions regarding the possible use of other terminator power and ground connections are the responsibility of the design engineer.

## SIGNAL CABLE TERMINATORS

Each cabinet receptacle for signal cables consists of two duplicate electrically parallel receptacles. In most cases, a signal cable will be plugged into one of the two receptacles, and a terminator (Control Data Part Number 300004) will be plugged into the other. The terminator contains a resistive network which terminates and establishes the logical "0" signal level for each of the 29 transmission lines in the cable. Power for the terminator assembly is provided by the 3 pins in the cabinet receptacle which do not have corresponding lines in the cable, as follows:

F9	+20 v
F10	-20 v
Center	Ground

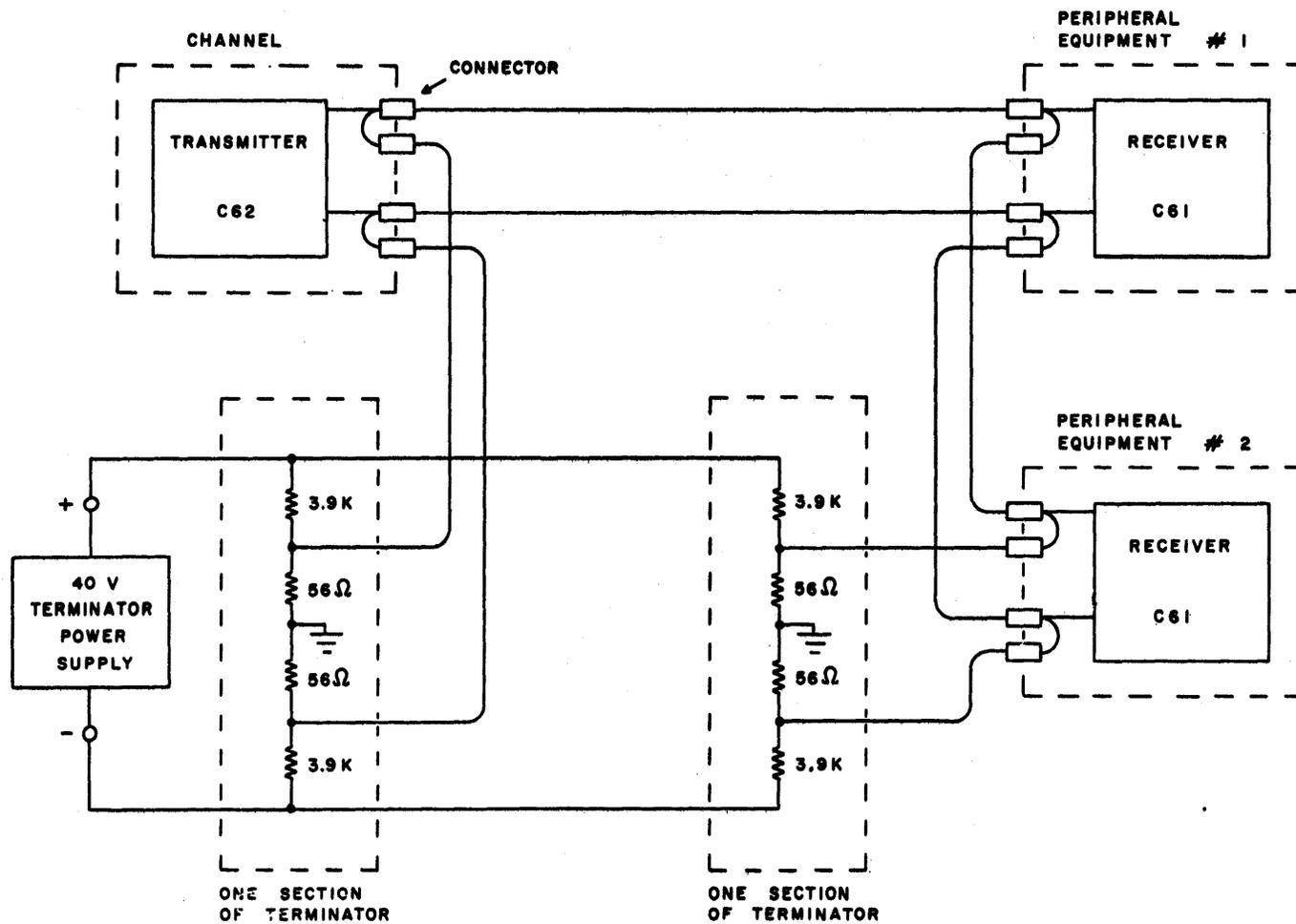


Figure B-1. Typical Transmission Line

TRANSMITTER AND RECEIVER  
Card Types C62A, C61, and C61B

GENERAL

The circuit configuration shown on page B-5 performs high speed transmission of digital information from one module to another. Inputs to the transmitter circuit are logical "1's" and "0's" of -5.8v and -1.1v, respectively. The transmitter converts these single-ended inputs to double-ended outputs suitable for transmission over a balanced transmission line. Tests using an 8-megacycle bit rate input have shown that 1 transmitter satisfactorily drives 20 receivers and 19 unused transmitters located at any point along a 200 foot transmission line.

The transmission line is twisted-pair having a characteristic surge impedance of approximately 110 ohms and is terminated at each end in its characteristic impedance. Transmission signal levels are approximately 0.5v measured differentially (line-to-line), and a "1" is distinguished from a "0" by a full voltage reversal.

The line voltage levels which represent a "0" are established by current flow from the +20v to the -20v source at the terminating resistors. Each of these currents is of the order of 5 ma, so that the total voltage developed across the terminating resistors is approximately 0.5v.

Transistor Q01 is turned on and current is shunted around the two constant current drivers Q02 and Q03 when the 3-way AND input to the transmitter is disabled by a "0". With the AND enabled by "1" inputs, Q01 is turned off, thus allowing Q02 and Q03 to drive a constant 20 ma into the transmission line. Originally, the bias networks on the line were producing a 5 ma current flow in one direction through the terminating resistors, but when the transmitter switches on, the direction of the net current flow through the terminating resistors effectively reverses. The current from the transmitter divides into two 10 ma currents which flow through each line termination. This current is in the opposite direction, producing a voltage drop equal and opposite to the original voltage. This results in a full voltage reversal for separating a "1" from a "0", although the signal level remains of the order of 0.5v line-to-line.

## TRANSMITTER, Card Type C62A

The printed circuit card contains two identical transmitter circuits designated A and B. A typical circuit is shown on page B-5.

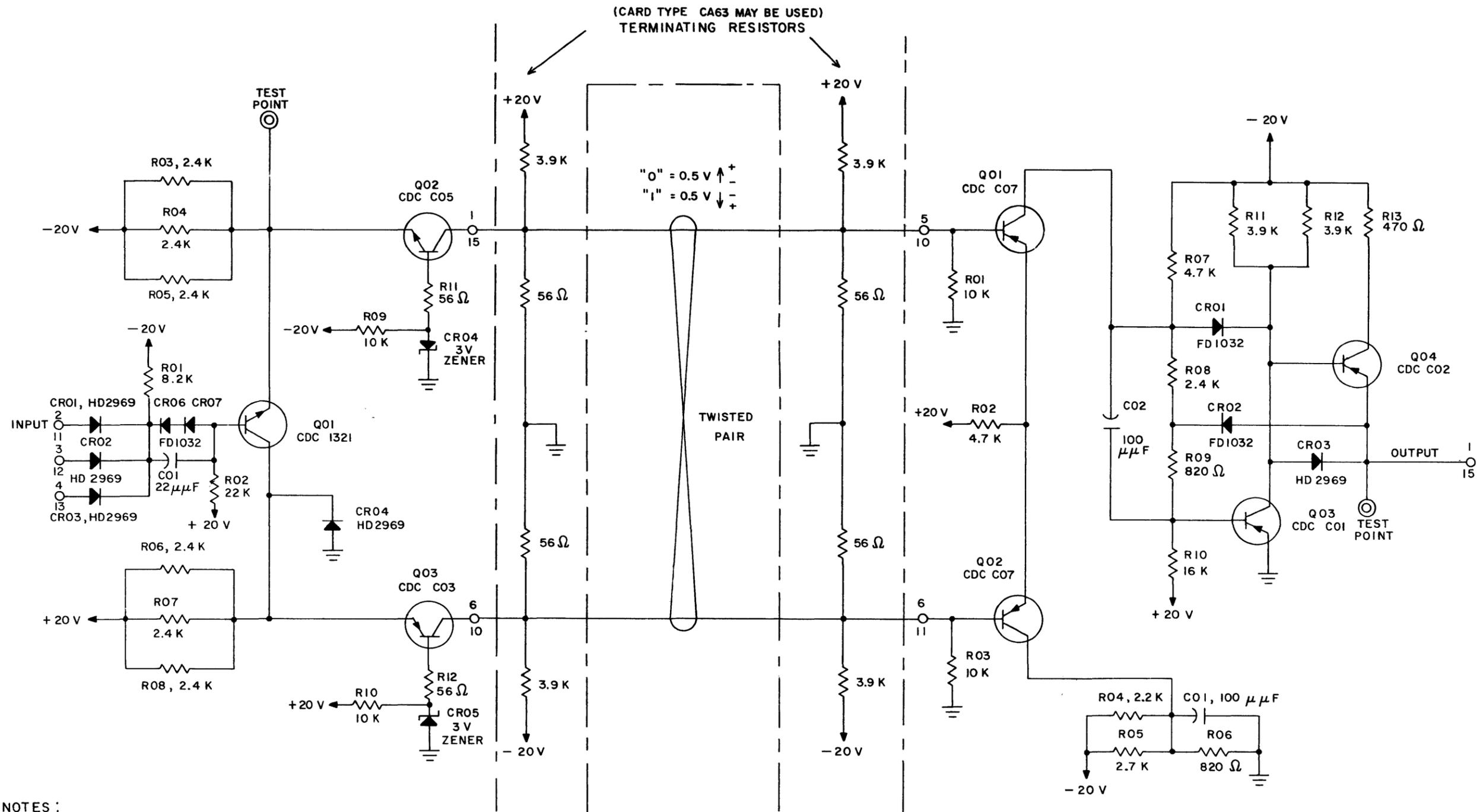
The logic input circuitry consists of a 3-way AND. The output of a standard logic card constitutes a proper input to a transmitter. A logical "1" input causes transistor Q01 to turn off and Q02 and Q03 to turn on, while a "0" input has the opposite effect.

A -1.1v "0" input causes the emitter-base junction of Q01 to be forward biased, fully turning on Q01. When Q01 is turned on, a shunt path for current is provided around Q02 and Q03. Since Q02 and Q03 no longer have a source of current, no current is injected into the transmission line.

When the AND input is satisfied, the base of Q01 is held at approximately -5 volts. This reverse biases the emitter-base junction by approximately 3 volts and causes Q01 to be turned off. Since the shunt path for current around Q02 and Q03 no longer exists, they become constant current generators of opposite polarities. Q03 injects a current of approximately 20 ma into the line and a like amount of current flows out of the line into Q02.

The base networks of Q02 and Q03 each contain a 3v zener diode which performs two functions. In the first case, the zener diode sets the voltage level at which the emitters of Q02 and Q03 reach their turned-on state. This, in turn, sets the threshold that must be overcome at the base of Q01, since its emitter is at the same potential as the emitter of Q02. In the second case, the zener diodes set the base voltages of Q02 and Q03 which determine how much noise voltage is allowed at the collectors before the collector-base junctions become forward biased. This value of noise voltage is something over 3 volts since the forward drop of the collector-base junctions adds to the zener diode voltage. This means that the transmitter operates satisfactorily with up to 3 volts of random noise on the transmission line.

The transmitter must be connected to the line in only one polarity, as shown on page B-5. This is necessary to provide current through the terminating resistors in a direction opposite the bias current.



NOTES :

1. THE CONNECTION SHOWN DOES NOT PROVIDE A LOGICAL INVERSION; A "1" INPUT RESULTS IN A "1" OUTPUT.
2. TO PRODUCE AN OVER-ALL LOGICAL INVERSION, THE TRANSMISSION LINE CONNECTION AT THE RECEIVER WOULD BE REVERSED.
3. THE TRANSMISSION LINE CONNECTION AT THE TRANSMITTER CAN NOT BE REVERSED, BECAUSE OF VOLTAGE POLARITIES.

Transmitter and Receiver C62 and C61

## TRANSMISSION LINE

A terminated balanced twisted-pair transmission line carries digital information from the transmitter to the receiver. This information is in the form of line-to-line, differential voltages of the order of 0.5v, with a complete voltage reversal distinguishing a "1" from a "0".

The surge impedance of the transmission line is 100 to 120 ohms. The line is terminated at each end with a 112-ohm resistive load, consisting of two 56-ohm resistors in series across the line with an optional center ground reference. This provides very good impedance matching and, as a result, reflections and standing waves are minimized.

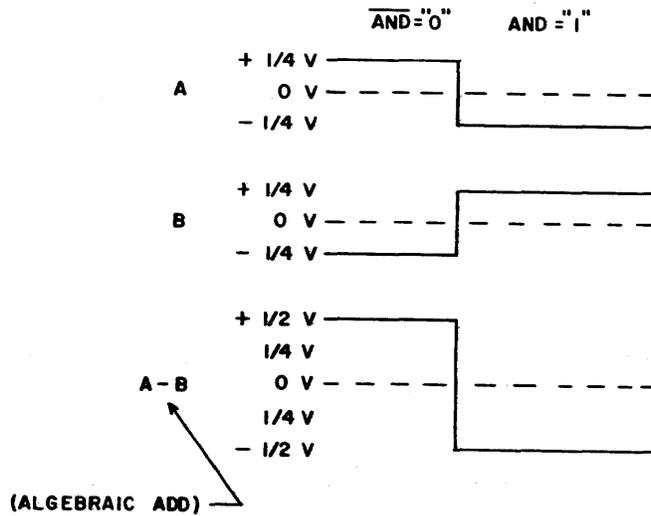
The line is biased at each end by means of 3.9k resistors to +20v and -20v to achieve a 5 ma bias current through the terminating resistors. This holds the "0" state signal level at 0.5v measured differentially.

## CURRENT FLOW

Refer to the diagram of the transmitter on page B-5. In the signal diagram accompanying this text the upper portion of the transmitter provides the readings for signal A (pin 1 or 15 on Q02); the lower portion provides the readings for signal B (Q03 pins 6 or 10).

When the AND to Q01 is not made, Q02 and Q03 are effectively open switches and the current on the line is 0. Approximately 5 ma flow from each of the 20 volt terminating networks sources, through the 3.9k and 56 ohm resistors on each side of the line to ground creating +0.25v at the collector of Q02 and -0.25v at the collector of Q03. Therefore when transmitting a "0" (AND gate not made) the live current is 0 and the differential voltage is 0.

When the AND to Q01 is made, Q02 and Q03 are closed switches and the current is then from the terminating networks through the respective set of three 2.4k resistors to the appropriate 20 volts. The current through each transistor (Q02 and Q03) is then 20 divided by 828 (28 ohms for the two 56 ohm resistors and 800 for the three 2.4k resistors.) or above 20 ma minimum. Half of this passes through the network at each end of the line. Thus when transmitting a "1" a current flow of at least 10 ma exists on each line.



#### NOTE

While a differential voltage measurement of either a "1" or a "0" is always 0v, a complete voltage reversal distinguishes a "1" from a "0" and can be observed on any oscilloscope equipped to perform an Algebraic Add as indicated in the lower signal pattern shown above when a "0" at +0.5v swings to -0.5v for a full 1v change.

#### GENERAL

The length of a transmission line may be up to 200 feet, with as many as 20 transmitters and 20 receivers placed in parallel along its length.

Bit rates of 8 mc or greater as possible on a 200 foot line. Low bit rates over longer distances are limited by the d-c line losses; however transmitters may be paralleled for longer distances to overcome these losses.

The velocity of signal propagation along the line is approximately 50 percent to 60 percent of the velocity of light. This results in a time delay per foot of the order of 1.6 to 1.8 nanoseconds.

The balanced system using differential receiving techniques allows a difference in noise levels up to 3v to be tolerated between the transmitter ground reference and the receiver ground reference.

## RECEIVER, Card Type C61B

The printed circuit card contains two identical receiver circuits designated A and B. A typical example is presented on page B-5. This portion of the circuits connected to the collector of Q01 is similar to a logical inverter, which is discussed elsewhere in this report.

This circuit functions as both a differential amplifier and a discriminator. It provides a logic output of either "1" or "0", according to the polarity of the differential 0.5v signal which the two input terminals receive from the transmission line.

The circuit inputs are connected directly into the bases of Q01 and Q02. The 0.5v differential input is centered about ground, so one input shifts approximately 0.25v positive while the other input shifts negative a similar amount. The two input transistors Q01 and Q02 are PNP type CDC C07's; thus the transistor which receives the negative input conducts less heavily.

The circuit is such that a negative input to the base of Q01 and a positive input to the base of Q02 results in a logical "1" at the receiver output. Under the opposite conditions of a positive input to Q01 and a negative input to Q02, the output is a logical "0". Thus, by reversing the connections at the receiver inputs, it is possible for a given set of conditions on the transmission line to produce either a "1" or a "0" at the receiver output.

The circuit shown on page B-5 does not produce an inversion between input to the transmitter and output from the receiver. A "1" input to the transmitter produces a transmission line signal of approximately 0.5v line-to-line with the polarity as shown. This allows transistor Q01 to apply approximately 5 ma of collector current to the junction of R07, R08, and the anode of CR01, which causes Q03 to switch off and Q04 to switch on, providing a "1" output. In this state, transistor Q04 can drive 8 OR loads. With opposite conditions at the receiver input, the output can drive 8 AND loads.

## GROUND RULES, using Receiver Card Type C61B

1. The output of a logic card constitutes a proper input to a transmitter.
2. The output of a receiver constitutes a proper input to a logic card.
3. A receiver may drive 8 OR loads, 8 AND loads, or any combination resulting in 8 loads total.

4. The transmission line is twisted-pair, having a surge impedance of 100 to 120 ohms.
5. The transmission line may be any length up to 200 feet.
6. The transmission line is terminated at each end in a resistive load approximately equal to its surge impedance.
7. A logical inversion between input to transmitter and output from receiver may or may not occur, depending upon the transmission line connections at the receiver.
8. The transmission line connections at the transmitter cannot be reversed, due to the polarity of the line bias voltage.
9. Up to 20 transmitters and 20 receivers may be connected along a transmission line.
10. A transmitter having an 8 megacycle bit rate input will drive 20 receivers at the end of a 200 foot transmission line, with 19 inactive transmitters also connected to the line.
11. Inactive transmitters and receivers do not load a transmission line and do not have to be disconnected from it.
12. No more than 8 transmitters should be driven by an inverter and no more than 7 should be driven by a flip-flop.

#### GROUND RULES, using Receiver Card Type C61

2. The output of a receiver constitutes a proper input to a logic card. However, when the output of the receiver is used with other terms to perform a logical function at the input of a logic circuit, the receiver output comes in on an AND input. This automatically implies that a receiver driving a flip-flop or control delay must feed an AND input. The above restriction may be violated when the output at the "1" level exceeds 0.6 usec duration.

All Ground Rules, other than number 2, for Card Type C61 are the same as for C61B.

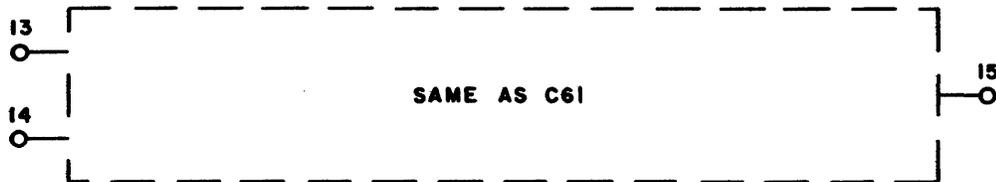
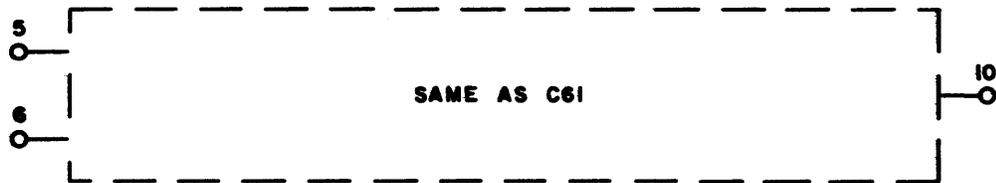
**RECEIVER**  
**Card Type HA11A**

This card contains three receiver circuits, having the pin connections shown in the accompanying diagram. The circuits operate the same as card type C61, which is discussed elsewhere.

The circuit functions as both a differential amplifier and a discriminator. It provides a logic output of either a  $-5.8\text{ v}$  "1" or a  $-1.1\text{ v}$  "0", according to the polarity of the differential  $0.5\text{ v}$  signal which the two input terminals receive from the transmission line.

The transmission line is balanced, terminated, twisted-pair, and the signals are centered about ground. As an example, if pin 2 goes to  $+0.25\text{ v}$  and pin 3 goes to  $-0.25\text{ v}$ , pin 1 will go to  $-1.1\text{ v}$  "0". If the inputs are reversed, the output will be  $-5.8\text{ v}$  "1".

The receiver circuit will drive 8 loads, and the ground rules are the same as for card type C61.

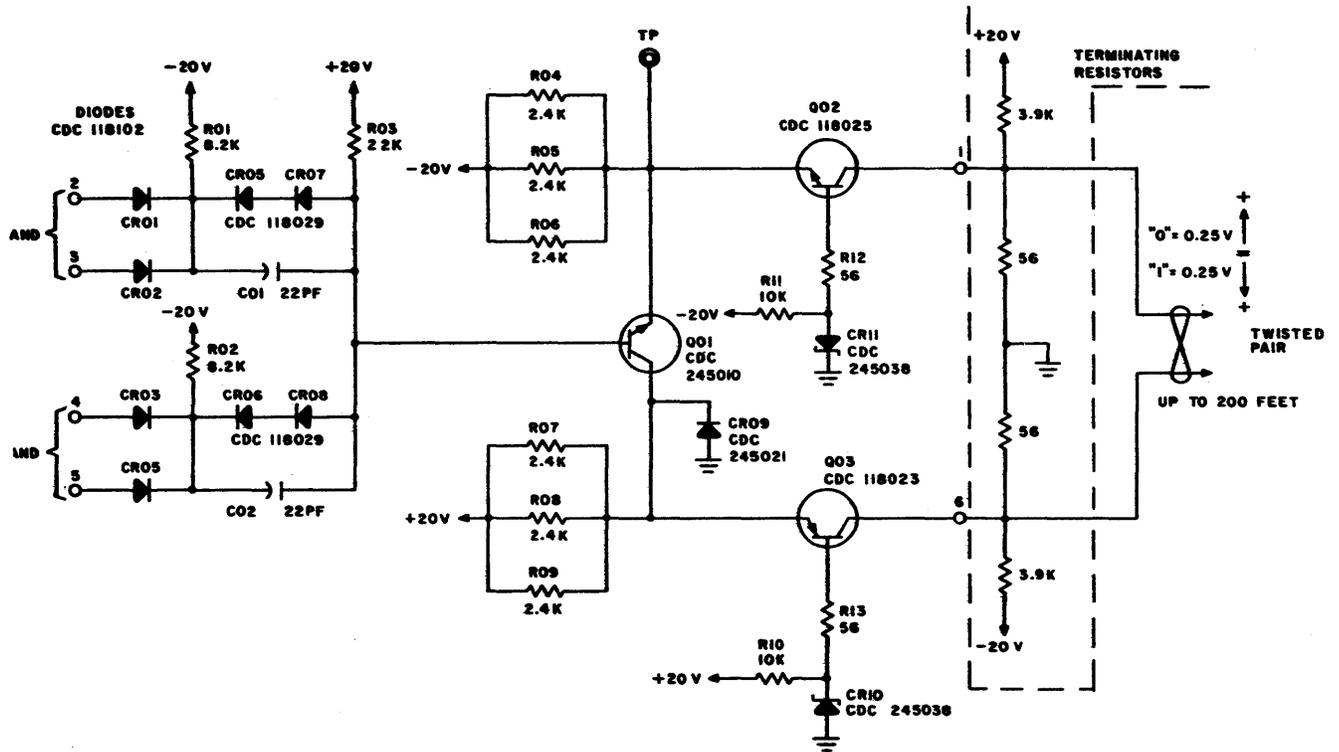


- NOTES: 1. CIRCUITS OPERATE SAME AS C61.  
2. 3 RECEIVER CIRCUITS PER CARD.

Receiver HA11A

**TRANSMITTER**  
**Card Type HA 19**

The function of the circuits on this card is to convert logic signals into outputs suitable for transmission over a balanced, terminated, twisted-pair transmission line up to 200 feet in length. Each circuit has two 2-way AND inputs. The remainder of the circuit is identical to card type C62 and the same ground rules apply.



NOTE: CIRCUIT OPERATES SAME AS CARD TYPE C62

### Transmitter HA19

**TRANSMITTER**  
**(1000-foot line)**  
**Card Types HA37 and HA43**

**GENERAL**

The purpose of the long-line transmitter circuits is to increase the distance over which signals may be sent on a 3600-type transmission line. The standard transmitter cards (C62 and HA19) are restricted to driving 200-foot lines; by substituting card types HA37 and HA43, the line length may be increased to 1000 feet. This feature will allow peripheral equipment to be installed in locations remote from the computer system.

The circuits on card types HA37 and HA43 are identical; the difference lies in their input configurations. The circuits on card type HA37 each have a 3-way AND input, the same as card type C62. The circuits on card type HA43 each have two 2-way AND inputs, the same as card type HA19.

The long-line system is d-c coupled, similar to the standard system. A limit of 1000 feet has been placed on the system to minimize changes required in standard hardware and because of limitations due to data transmission characteristics.

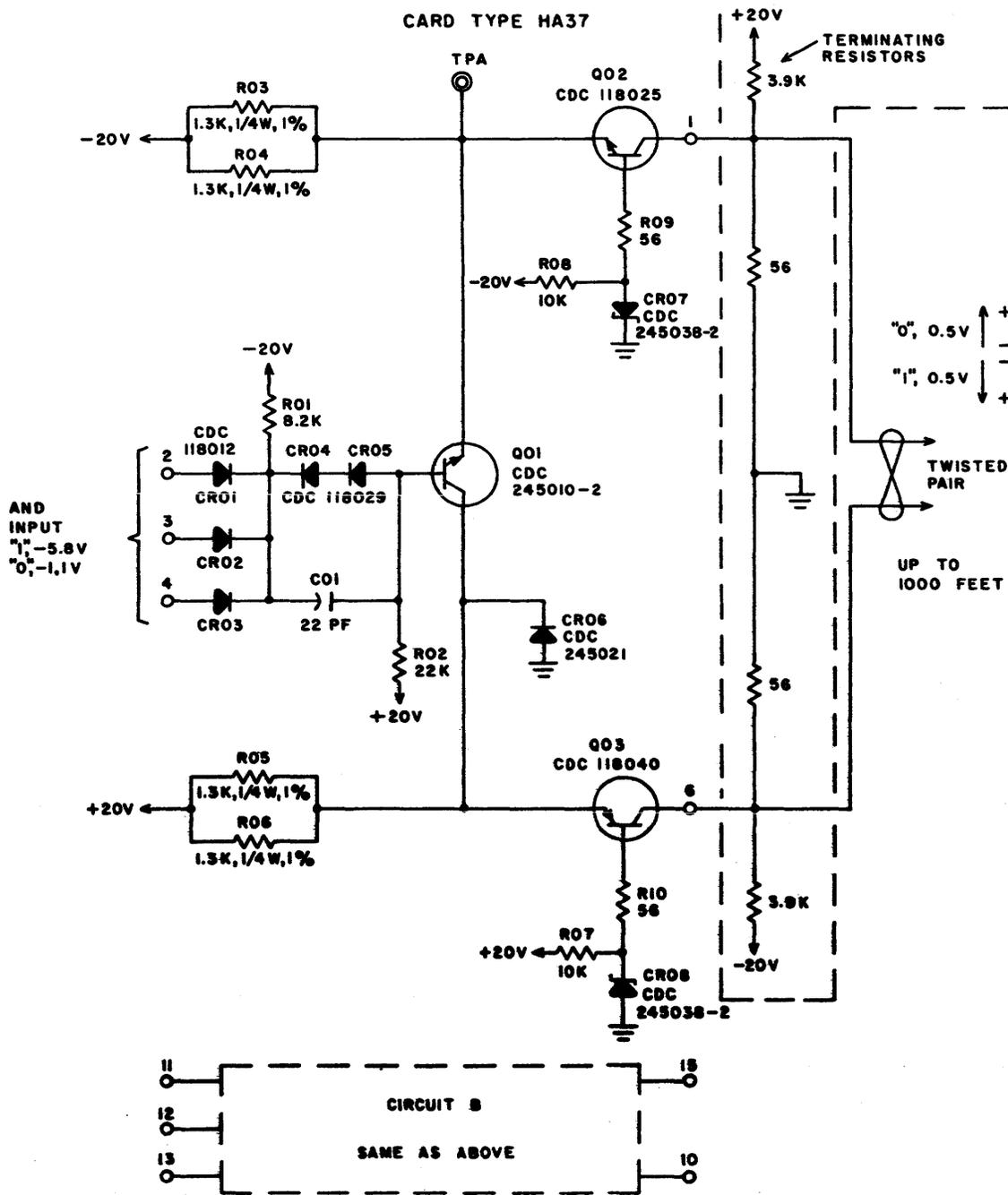
**OPERATION**

The long line transmitter circuit is identical in operation to the standard 3600-type transmitter. The major differences in the two circuits are the higher power capability of the HA37 and HA43 cards, and changes in specifications of some of the components.

Each circuit card contains two circuits designated A and B, as shown in the accompanying diagram. The input consists of a 3-way AND on HA37 cards, and two 2-way AND's on HA43 cards. The output of a standard logic card constitutes a proper input to a transmitter. A logical "1" input causes transistor Q01 to turn off and Q02 and Q03 to turn on, while a "0" input has the opposite effect.

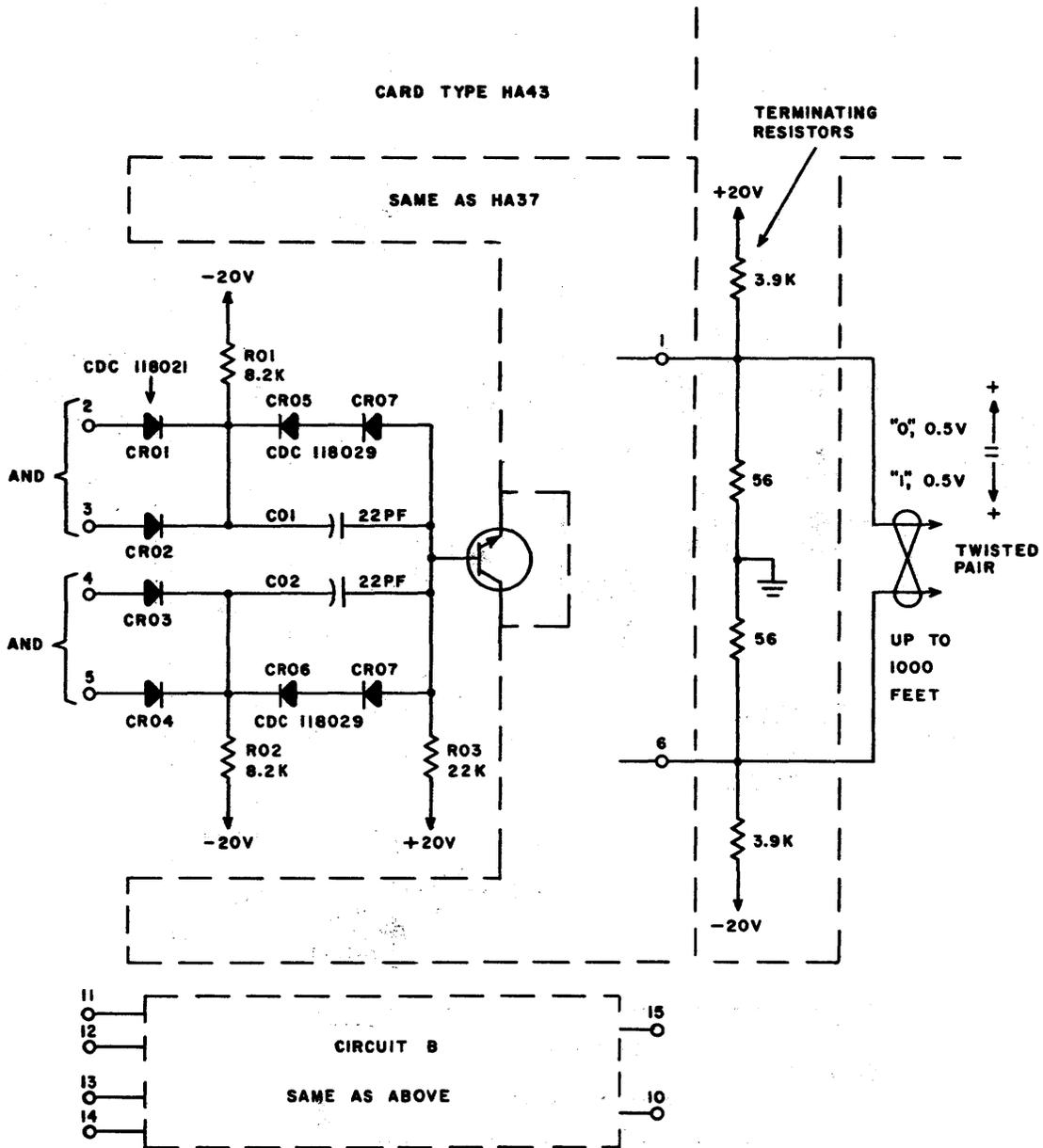
A -1.1v "0" input causes the emitter-base junction to Q01 to be forward biased, turning Q01 fully on. When Q01 is turned on, a shunt path for current is provided around Q02 and Q03. Since Q02 and Q03 no longer have a source of current, no current is injected into the transmission line.

When the "AND" input is satisfied, the base of Q01 will be held at approximately -5 volts. This reverse-biases the emitter-base junction by approximately 3 volts and causes Q01



NOTE: THIS CARD MAY BE SUBSTITUTED FOR THE C62 CARD, TO DRIVE LINES UP TO 1000 FEET.

**Transmitter HA37**



Transmitter HA43

to be turned off. Since the shunt path for current around Q02 and Q03 no longer exists, they become constant current generators of opposite polarities. Q03 injects a current of approximately 26 ma into the line and a like amount of current flows out of the line into Q02.

The base networks of Q02 and Q03 each contains a 3.45v zener diode which performs two functions. In the first case, the zener diode sets the voltage level at which the emitters of Q02 and Q03 will reach their turned-on state. This, in turn, sets the threshold that must be overcome at the base of Q01, since its emitter is at the same potential as the emitter of Q02. In the second case, the zener diodes set the base voltages of Q02 and Q03 which determine how much noise voltage will be allowed at the collectors before the collector-base junctions become forward biased. This value of noise voltage is something over 3.28 volts, since the forward drop of the collector-base junctions adds to the zener diode voltage. This means that the transmitter will operate satisfactorily with more than 3 volts of random noise on the transmission line.

#### RECEIVER CIRCUIT

The receiver is the standard type C61 or HA11, which are described elsewhere in this manual.

#### CABLE

The signal cable is standard 3600-type, containing 29 twisted-pair transmission lines. Each transmission line consists of two 24-gauge conductors. If required, a cable with a protective copper braid shield may be used to protect against extreme electrical noise and other environmental hazards.

#### LINE TERMINATIONS

Line terminations are standard 3600-type signal cable terminators.

#### GROUND RULES

##### 1. Installation:

- a. To convert an interface from a 200-foot cable length limitation to 1000-foot capability, all CA62B cards must be replaced with HA37 cards and all HA19 cards must be replaced with HA43 cards.
- b. Receiver cards remain unchanged.
- c. Transmission line terminations remain unchanged.

2. Each long line transmitter card requires approximately 1/3 watt more power than a standard transmitter card. The additional power is divided equally between the +20v and -20v supplies.
3. A maximum of 16 long line transmitters and 16 standard receivers may be distributed along a 1000-foot transmission line.
4. At a distance of 1000 feet, the output waveform of the receiver will be symmetrical for switching rates up to 500 kc. Switching rates in excess of 500 kc will result in degradation of symmetry. For distances of less than 200 feet, switching rates are similar to a standard transmitter-receiver system.
5. The balanced system using differential receiving techniques allows a difference in noise levels of up to 3 volts between the transmitter ground reference and the receiver ground reference. To avoid problems of noise pickup, it is recommended that the terminators on all remote equipments be energized from the common 40v supply, with an earth ground reference level. Decisions regarding the possible use of other terminator power and ground connections are the responsibility of the design engineer.
6. When driving signals through a 1000-foot cable, total delay time between input to the transmitter and output from the receiver will be approximately 2 micro-sec.
7. A signal de-skewing delay of 300 nanoseconds must be allowed for parallel transmission of 12 data bits over distances from 600 to 1000 feet.

#### DELAY AND SKEW ON A 1000-FOOT CABLE

When changing from a line driver system with a maximum distance of 200 feet to a system with a maximum distance of 1000 feet, the following changes must be made and new characteristics observed:

1. For distances from 600 to 1000 feet, the control signal (Data Signal, Reply, etc.) deskewing delay must be increased from 100 to 200 nanoseconds.

#### Data Channel - Peripheral Device Delays

##### Normal Operation

The data channel allows 100 nanoseconds for Data Signal deskewing. This is active during both Read and Write operations. During a Write operation, the peripheral device must allow Data Signal delay for parity checking.

During a Read operation, the peripheral device delays the Reply for 200 nanoseconds to allow for signal deskewing and data channel parity checking.

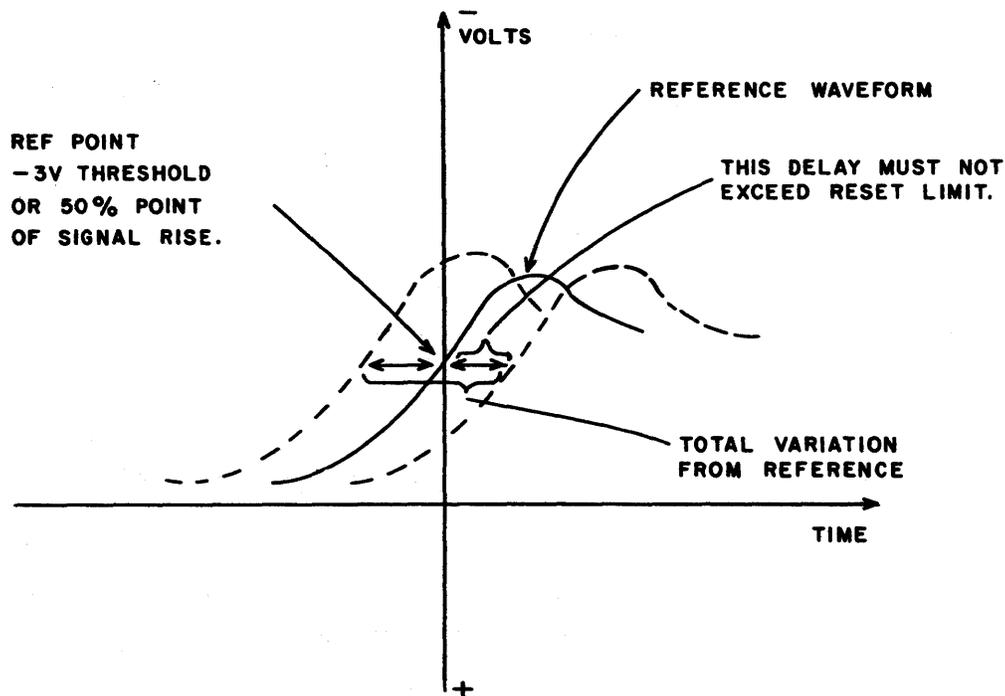
Recommended Modifications for 200 Nanosecond Deskewing Delay

Modification should be done at the peripheral device, which would normally be the remote site. During a Write operation, the Data Signal should be delayed 100 nanoseconds at the peripheral device in addition to the parity checking delay. During a Read operation, the Reply delay should be increased by 100 nanoseconds to 300 nanoseconds to allow for signal deskewing and data channel parity checking.

No attempt will be made to specify how the added delay should be inserted. The delay may be added in a manner most feasible for the device involved.

2. If normal operation does not occur, the following tests should be conducted:
  - A. Check for required signal outputs from the transmitters (H37 card output) and receiver circuits (C61 card output). If no signal is received, check transmitter and receiver circuits; check line termination and voltages. If no problem appears to exist at this point, proceed to step B.
  - B. From information on the logic of the connected equipment, find cases where the data or signal code lines are sampled within a certain period after the control signal is received. If the delay is preset, for example, at 100 nanoseconds, test if the delay period is at least 100 nanoseconds. Preset delay shall not be less than 100 nanoseconds. Synchronize an oscilloscope on the output of the control line receiver and observe the variation of the receiver outputs of the data or code lines with respect to the control line reference. The reference point may be considered as the -3 volt threshold point or 50% of the risetime point of 3600 logic.

In pictorial form, risetime variation may be sketched as follows:



The delay of the signal risetime of any data or code line must not exceed the preset 100 or 200 nanoseconds, whichever the case may be. Where required, fall time going from a "1" to a "0" signal may be tested in a similar manner. If the delay does not fall within the preset time, check for: (1) bad receiver card, bad components, etc. (2) bad wiring connection (3) improper line termination or termination voltages.

- C. Check the system logic for Data Signal-Reply operation. The propagation time becomes an important factor in this situation. For example, assume device A has a Data Signal up and the remote site responds with a Reply. Device A drops the Data Signal in response to the Reply. The Reply is dropped at the remote site. Device A cannot bring up the next Data Signal until the dropping of the Reply at the remote site is recognized at Device A. Otherwise, Device A may accept the Reply from the previous word transfer and the information will be lost.
- D. Connect and Disconnect Delay. For a system in which a data channel is communicating with peripheral equipments via 1000 feet of cable, the equipments must be modified so that the selected equipment will not return a Reply earlier than 3 usec after receiving the Connect signal.

## TIME VARIATIONS DUE TO CABLE DELAY

A significant amount of time is lost in transmission of signals through cables. The following is an itemized list of approximate time lag in a 3600 system over a 1000-foot cable.

- |                                                                                                        |                      |
|--------------------------------------------------------------------------------------------------------|----------------------|
| 1. Transmit Data Signal and data from data channel to peripheral device plus Data Signal delay         | 2, 100 nano.         |
| 2. Response time of peripheral device, i. e., examine parity, bring up Reply, and control signal delay | 400 nano.            |
| 3. Send Reply to data channel                                                                          | 2, 000 nano.         |
| 4. From dropping of Data Signal until data channel senses dropping of Reply.                           | 4, 000 nano.         |
| 5. Memory reference time between 48-bit words                                                          | <u>1, 500 nano.</u>  |
|                                                                                                        | <b>10, 000 nano.</b> |

$$\frac{1.0}{10.0 \times 10^{-6}} = .100 \times 10^6$$

100 KC word rate  
200 KC character rate

worst case with 60 usec. memory reference time

$$\begin{array}{r} 8.5 \text{ usec.} \\ + 60 \text{ usec.} \\ \hline 68.5 \text{ usec.} \end{array}$$

$$\frac{1.00}{68.5 \times 10^{-6}} = .0146 \times 10^6$$

14.6 KC word rate  
29.9 KC character rate

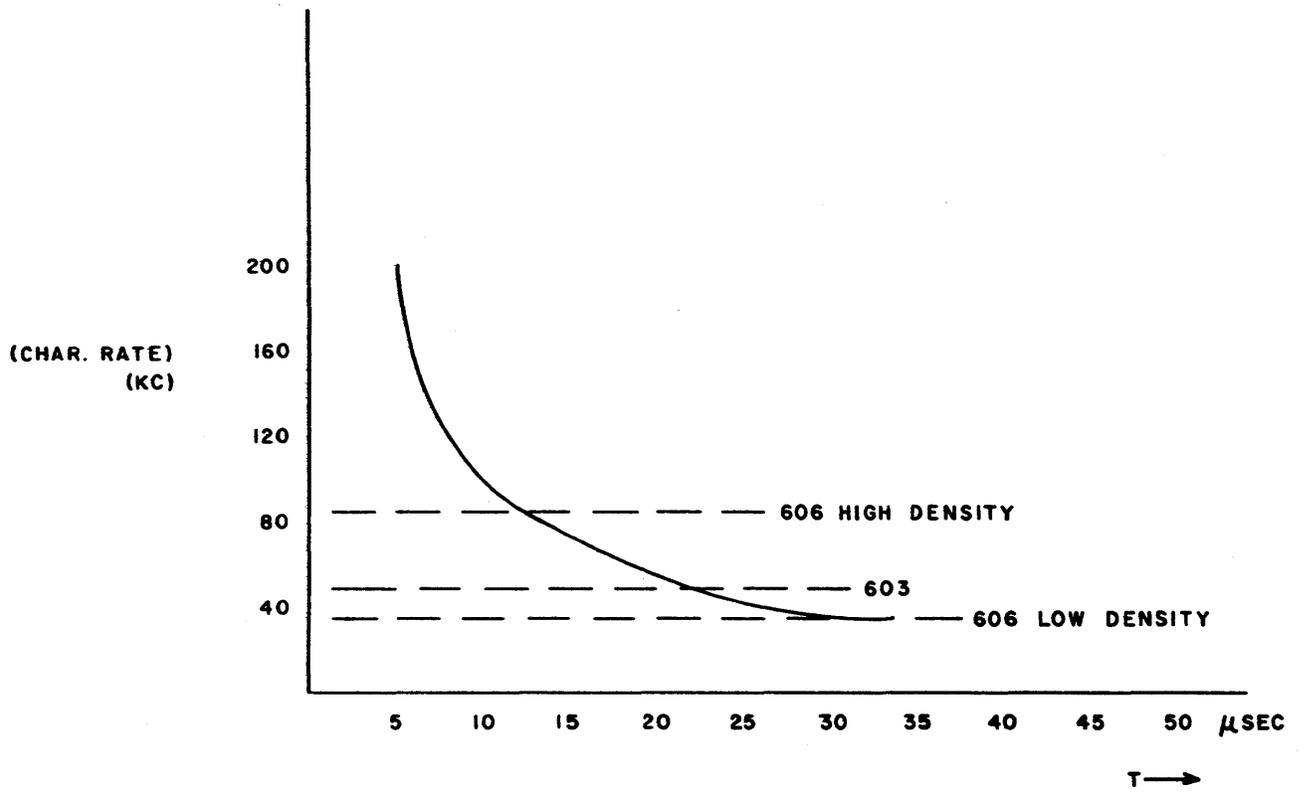
### Read Delay (See accompanying diagram)

1. Same as for write (1).
2. This time is dependent on peripheral device speed.
3. 200 nanoseconds required with 200 to 1000 foot cable.
4. 100 nanoseconds for parity generation and checking.
5. Same as (1).

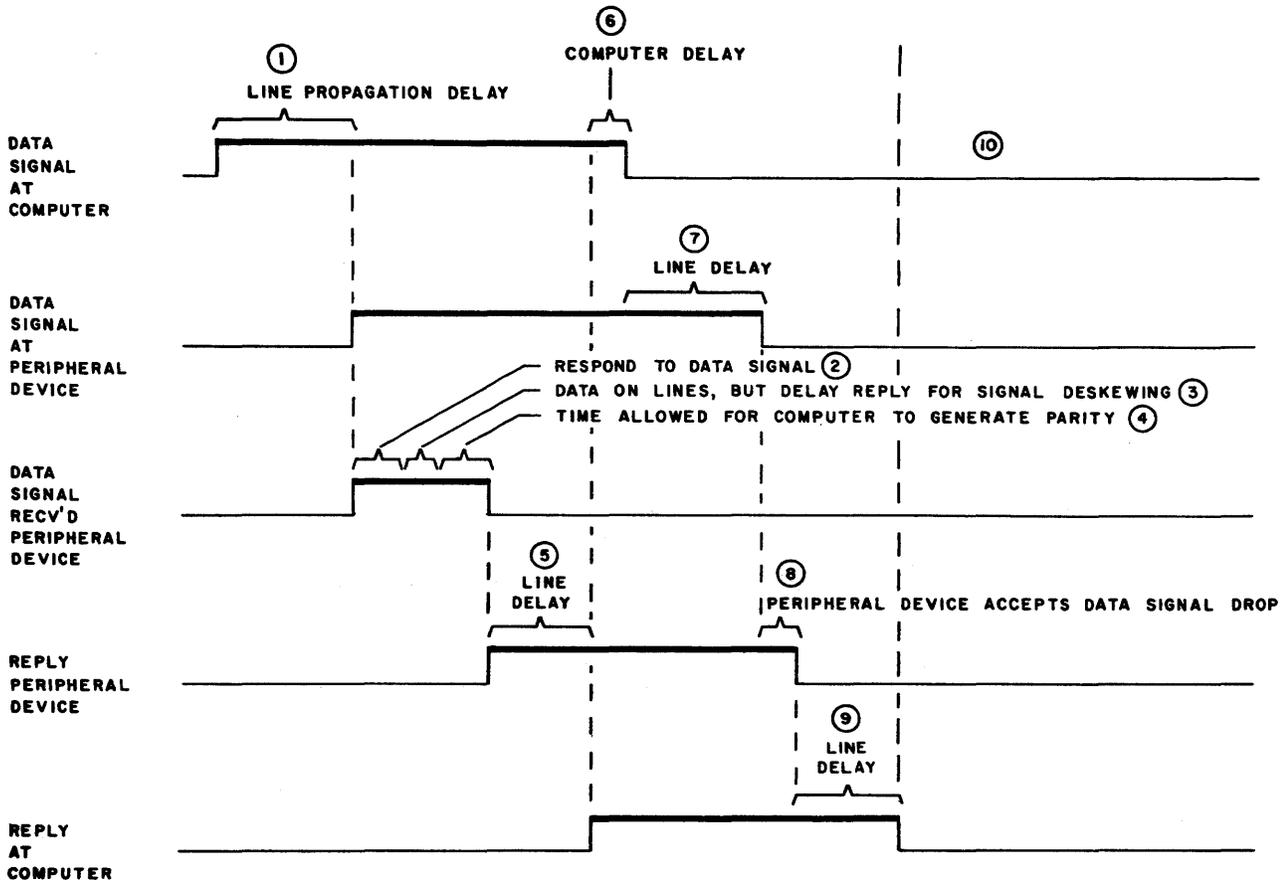
6. Computer responds to Reply, samples lines and drops Data Signal, (100 nanoseconds for 3606 data channel).
7. Same as (1).
8. Peripheral device responds to Data Signal drop and drops Reply.
9. Same as (1).
10. The next Data Signal can be transmitted and the computer can accept a Reply/Reject signal only after time (9) is completed.

Write Delay (See accompanying diagram)

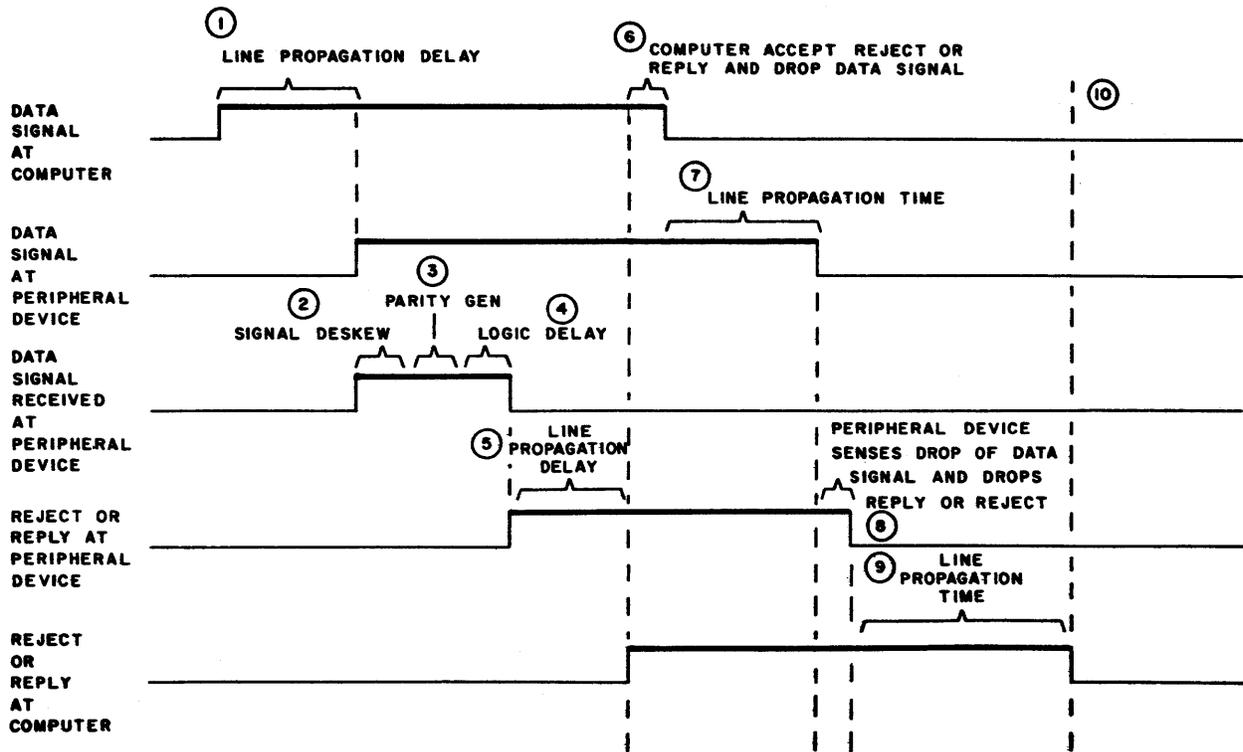
1. Line, transmitter and receiver card delay (approx. 2 usec. per 1000 feet).
2. Signal deskew allows the data lines to stabilize prior to sampling. (200 nanoseconds required for 1000 feet). The 3606 data channel inserts 100 nanoseconds of the required 200 nanoseconds.
3. Parity generated from data and checked against received parity bit.
4. Logic delay for decision making -- such as examine data and send Reply or Reject. This delay must be 3 usec. on a Connect operation to allow all peripheral devices to disconnect if the connect code does not pertain to that device.
5. Same as 1.
6. Computer accepts Reject or Reply and drops Data Signal. (The 3606 data channel allows 100 nanoseconds).
7. Same as 1.
8. Dependent on peripheral device.
9. Same as 1.
10. The next Data Signal can be transmitted and the computer can accept a Reject or Reply signal only after time (9) is completed.



Approximate Character Speed for 3600 Computer I/O Operations



Delays during Read Operation



**Delays during Write Operation**

## TRANSMITTER AND RECEIVER

### Card Types P14A and P16A

#### FUNCTION

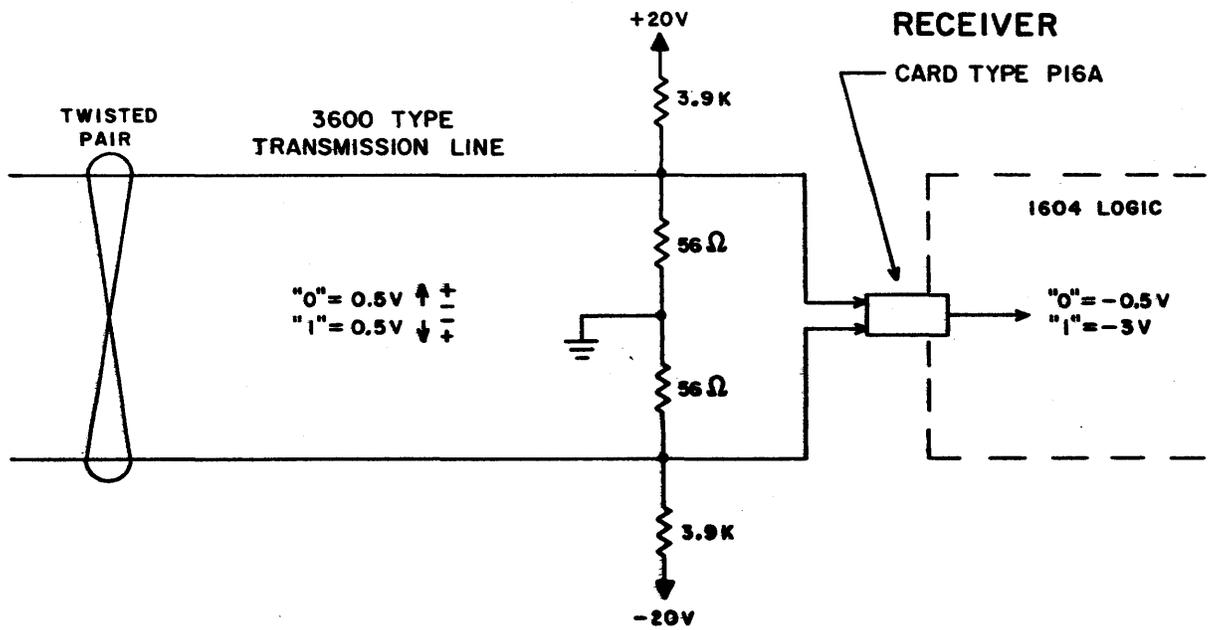
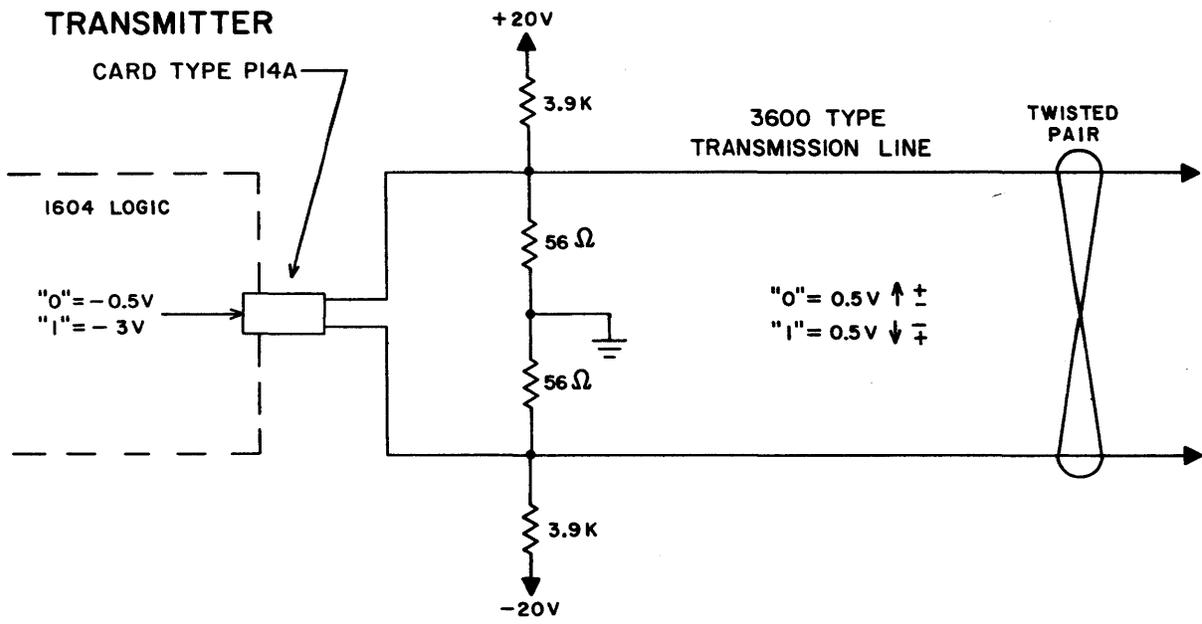
These circuits enable equipment containing 1604 logic to receive and transmit via a 3600 type I/O cable. This is accomplished by converting the 3600 transmission line signal levels of 0.5v line-to-line to the 1604 logic levels of "1" = -3v and "0" = -0.5v. Card types P14A and P16A have the same capabilities and impedance characteristics as 3600 type transmitters and receivers. Both types of transmitters and receivers may use the same transmission line.

#### OPERATION

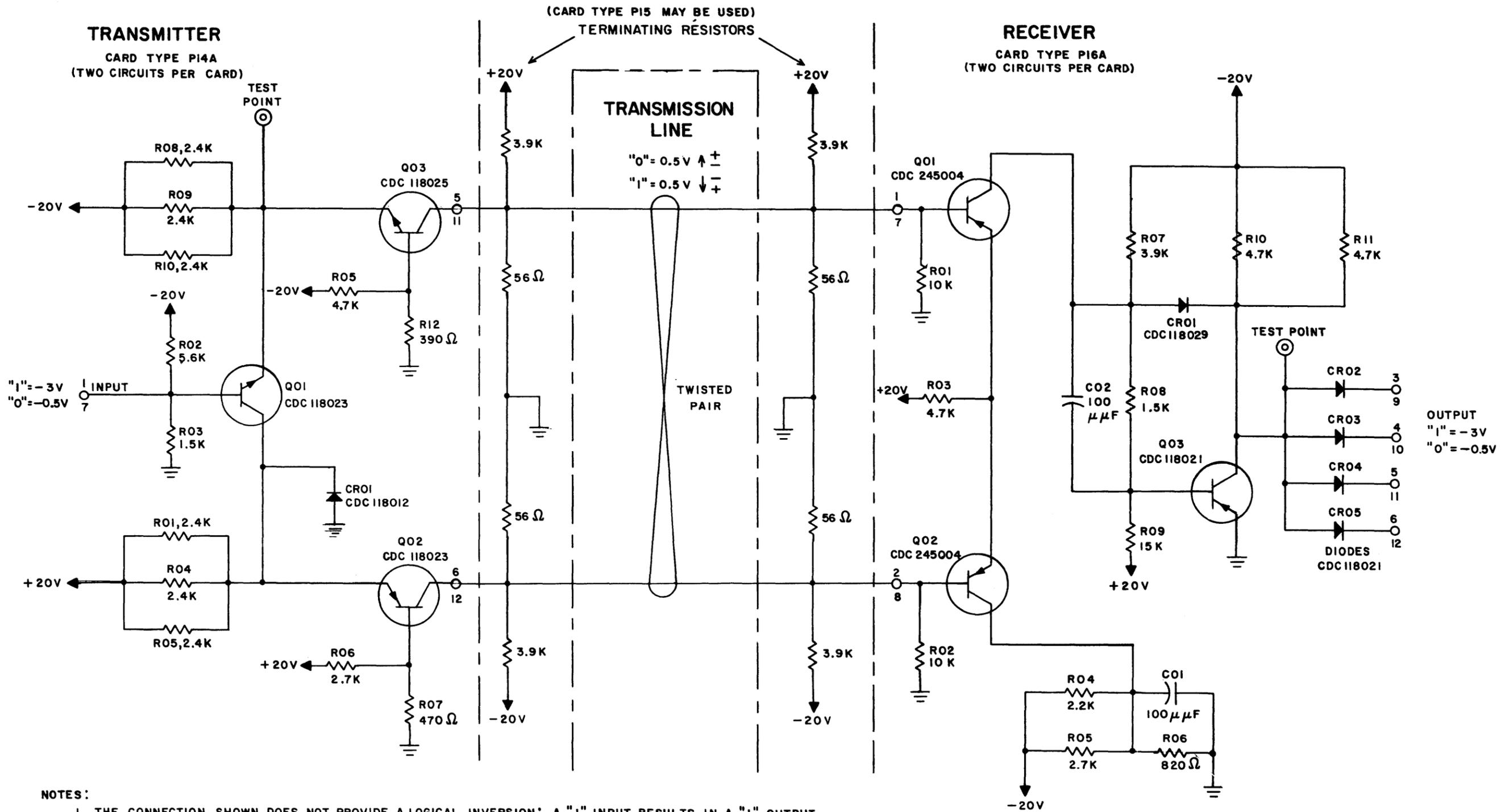
The transmitter, card type P14A, is similar to the C62A, which is discussed elsewhere. It converts single-ended inputs into double-ended outputs suitable for driving a balanced, terminated, twisted-pair transmission line. A -3v "1" input to transistor Q01 causes Q02 and Q03 to inject a current of about 20 ma into the transmission line. This results in a full line-to-line voltage reversal.

The "0" line signal level is established by the flow of bias current through the terminating resistors. In order to obtain proper voltage polarities, the transmitter must be connected to the line as shown.

The receiver, card type P16A, is similar to the C61B, which is discussed elsewhere. It functions both as a differential amplifier and as a discriminator, providing logic outputs of -3v "1" or -0.5v "0" according to the polarity of the 0.5v signal received from the transmission line. The transmitter and receiver combination can be made to provide a logical inversion by reversing the transmission line connections at the receiver.



Transmitter P14A and Receiver P16A

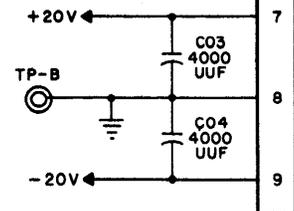
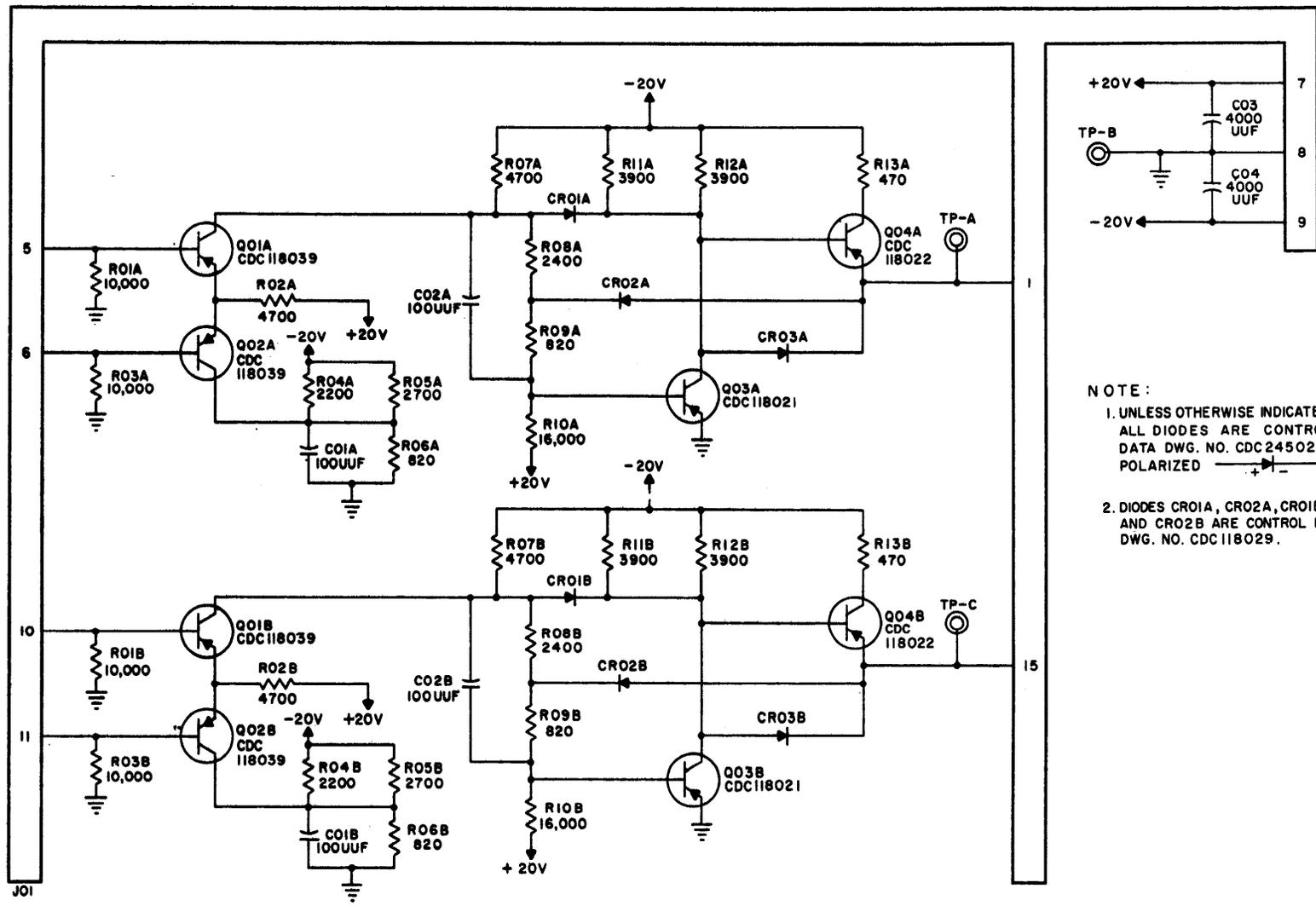


**NOTES:**

1. THE CONNECTION SHOWN DOES NOT PROVIDE A LOGICAL INVERSION; A "1" INPUT RESULTS IN A "1" OUTPUT.
2. TO PRODUCE AN OVER-ALL LOGICAL INVERSION, THE TRANSMISSION LINE CONNECTION AT THE RECEIVER WOULD BE REVERSED.
3. THE TRANSMISSION LINE CONNECTION AT THE TRANSMITTER CAN NOT BE REVERSED, BECAUSE OF VOLTAGE POLARITIES.

Transmitter P14A, Transmission Line and Receiver P16A.

**APPENDIX C**  
**SCHEMATIC DIAGRAMS**

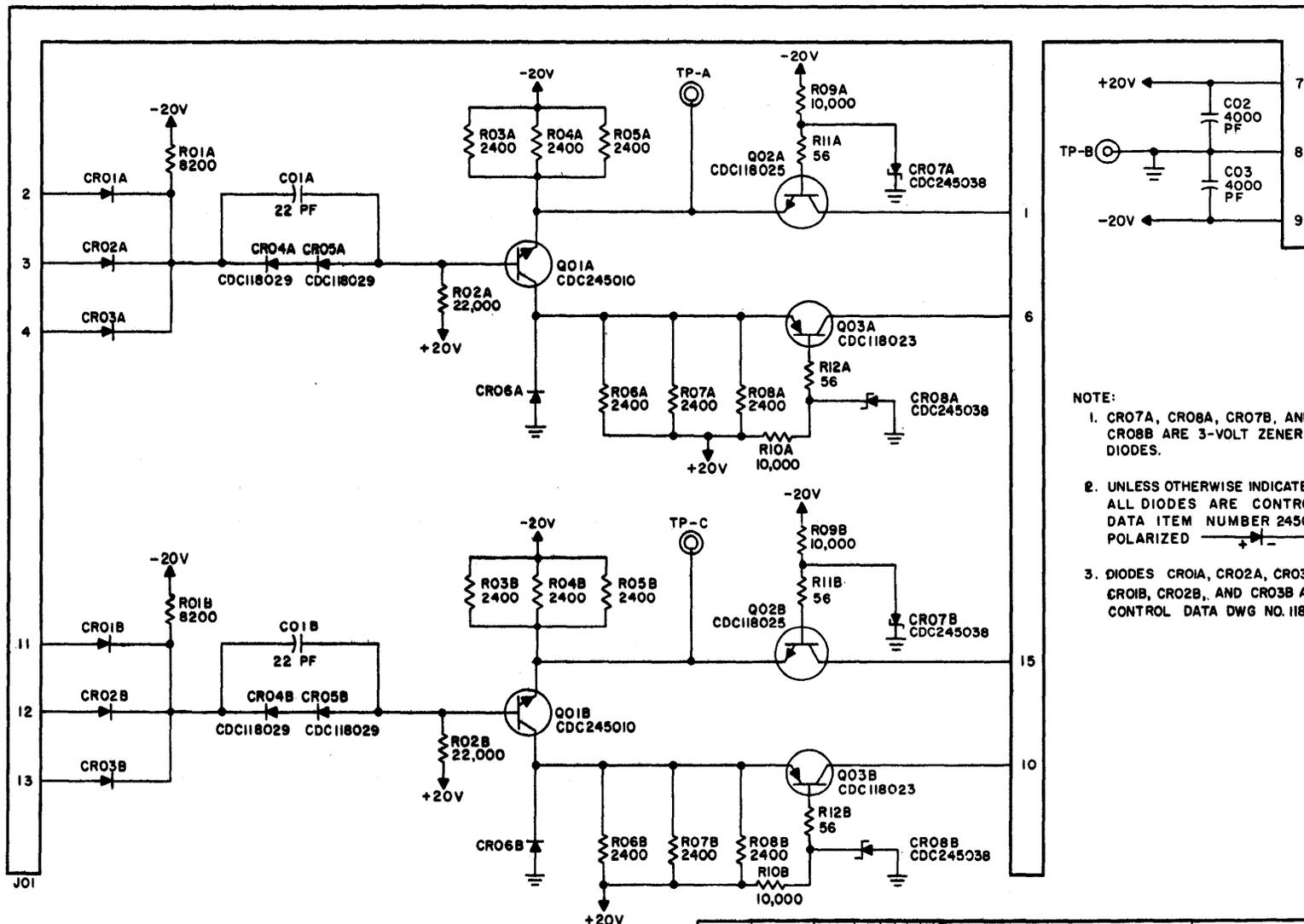


NOTE:

1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA DWG. NO. CDC 245021 POLARIZED
2. DIODES CRO1A, CRO2A, CRO1B, AND CRO2B ARE CONTROL DATA DWG. NO. CDC 118029.

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TO

C.D.H.		REFERENCE DRAWINGS		PRINTED CIRCUIT MASTER 309241		CONTROL DATA CORPORATION COMPUTER DIVISION 3600 (025)
309241		COMPONENT ASSEMBLY 309242		PROJECT OR PRODUCT		
A.A.B.		COMPONENTS (UNLESS OTHERWISE INDICATED)		TOLERANCE VALUE SIZE		DESIGN NUMBER Y C 309243
C.D.H.		RESISTORS ± 5% OHMS 1/4 WATT		CAPACITORS ± 20% UUF		
2-21-63		TITLE		RECEIVER -		REV A
3791		A		TYPE CA61, SCHEMATIC		



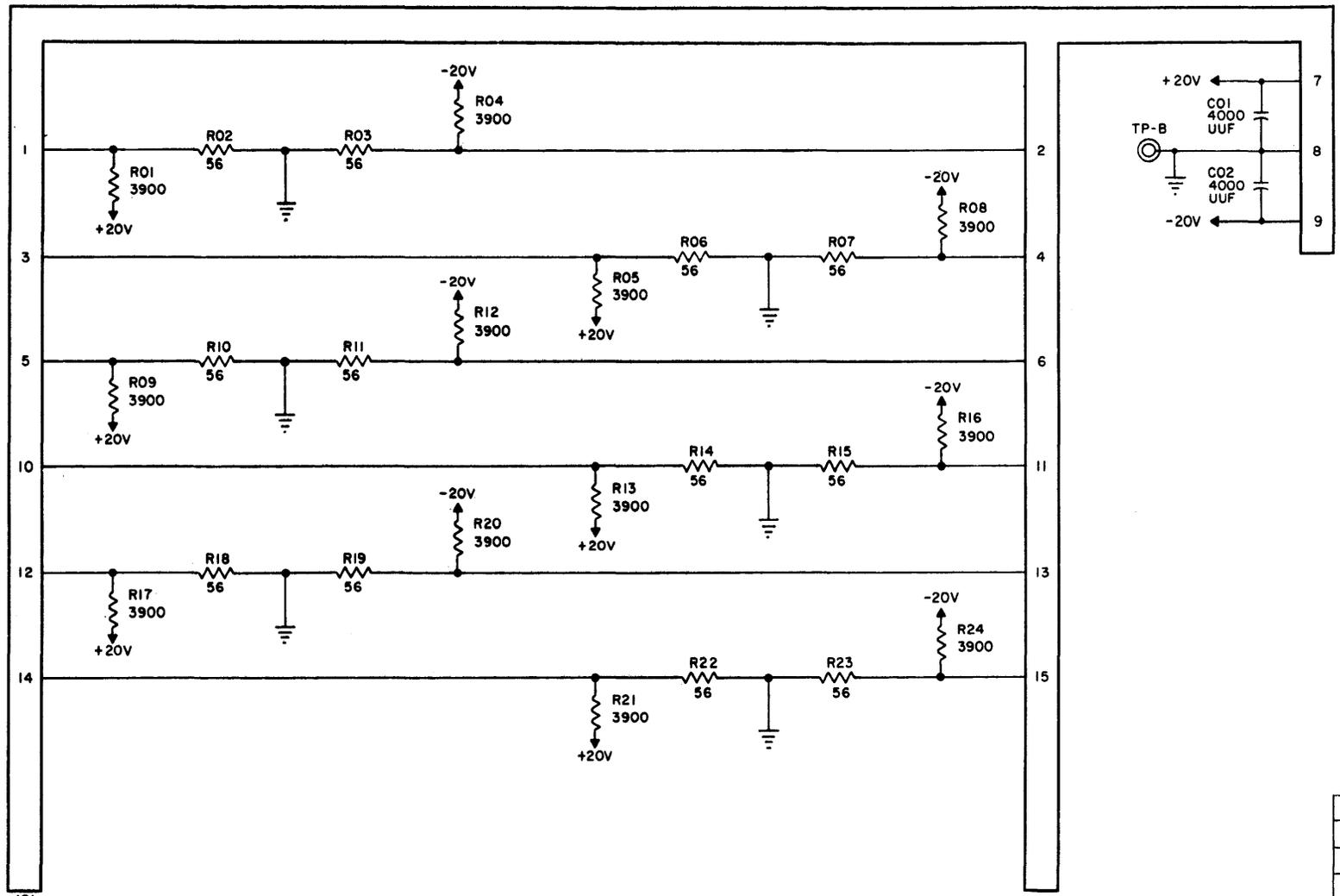
- NOTE:
1. CRO7A, CRO8A, CRO7B, AND CRO8B ARE 3-VOLT ZENER DIODES.
  2. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA ITEM NUMBER 245021 POLARIZED  $\begin{matrix} \text{+} \\ \text{+} \end{matrix}$
  3. DIODES CRO1A, CRO2A, CRO3A, CRO1B, CRO2B, AND CRO3B ARE CONTROL DATA DWG NO. 118012.

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GAS		H.N.F.		GAS	
300	<i>Neck</i>	300			
PN	R.A.P.	AAB			
GAS	H.N.F.	GAS			
3-20-63	2-20-63	1-18-63			
4160	4005	3799			
C	B	A			

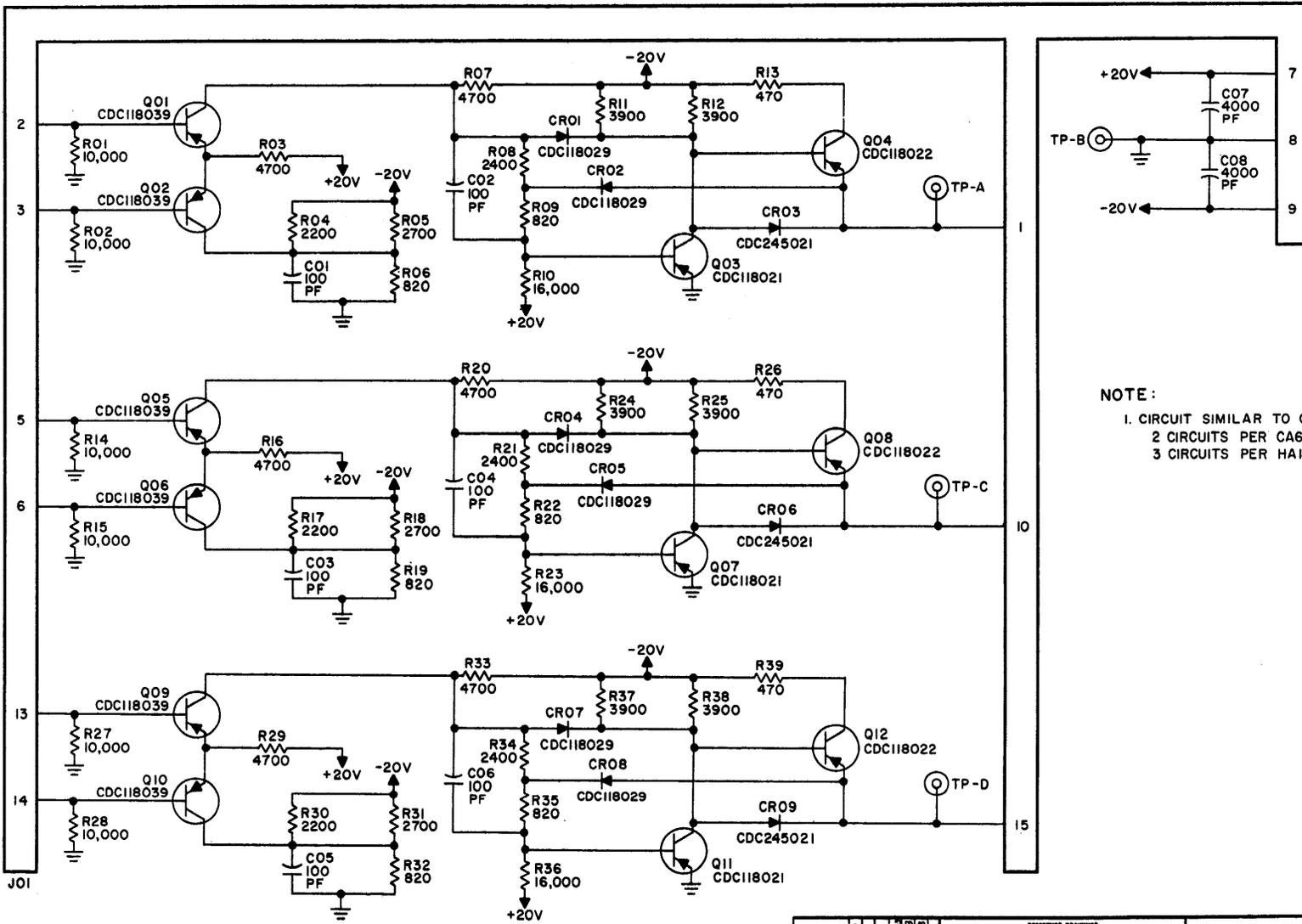
REFERENCE DRAWINGS	
PRINTED CIRCUIT MASTER	309245
COMPONENT LAYOUT	309246
COMPONENTS (UNLESS OTHERWISE INDICATED)	
RESISTORS	±5% OHMS 1/4 WATT
CAPACITORS	±20% PF
TITLE	
TRANSMITTER - TYPE CA62B, SCHEMATIC	

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COMPUTER DIVISION	
3600 (025)	
Y C 309247	REV C



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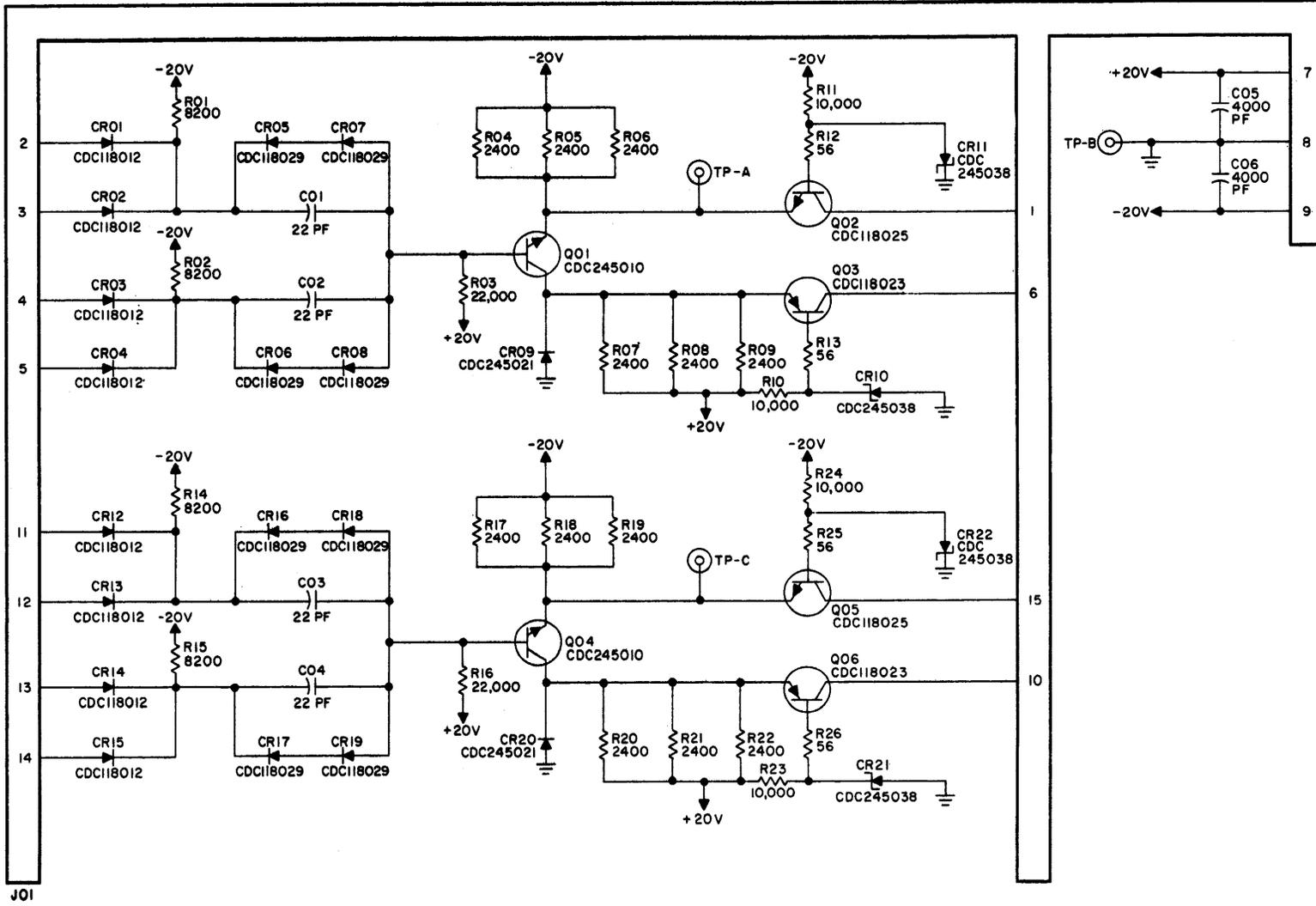
REFERENCE DRAWINGS		309249	
PRINTED CIRCUIT MASTER		309250	
COMPONENT ASSEMBLY			
COMPONENTS UNLESS OTHERWISE INDICATED			
RESISTORS	3.5%	OHMS	1/4 WATT
CAPACITORS	±20%	UUF	
TITLE		XMSM LINE TERM.-	
		TYPE CA63, SCHEMATIC	
CONTROL DATA CORPORATION		COMPUTER DIVISION	
PROJECT OR PRODUCT		3600 (025)	
DRAWING NUMBER		Y C 309251	
REV			



NOTE:  
 1. CIRCUIT SIMILAR TO CA61  
 2. CIRCUITS PER CA61  
 3. CIRCUITS PER HA11

D-12  
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DRN		309 445		PRINTED CIRCUIT MASTER		309 446	
LIB		309 446		COMPONENT ASSEMBLY		309 446	
DRN		309 446		COMPONENTS (UNLESS OTHERWISE INDICATED)		TOLERANCE	
10-2-63		309 446		RESISTORS		± 5% OHMS 1/4 WATT	
A		309 446		CAPACITORS		± 20% UUF	
A		309 446		TITLE		RECEIVER-TYPE HA11A, SCHEMATIC	
A		309 446		CONTROL DATA CORPORATION		COMPUTER DIVISION	
A		309 446		ZETA (074)		REV	
A		309 446		Y C 309 447 A		PAGE	



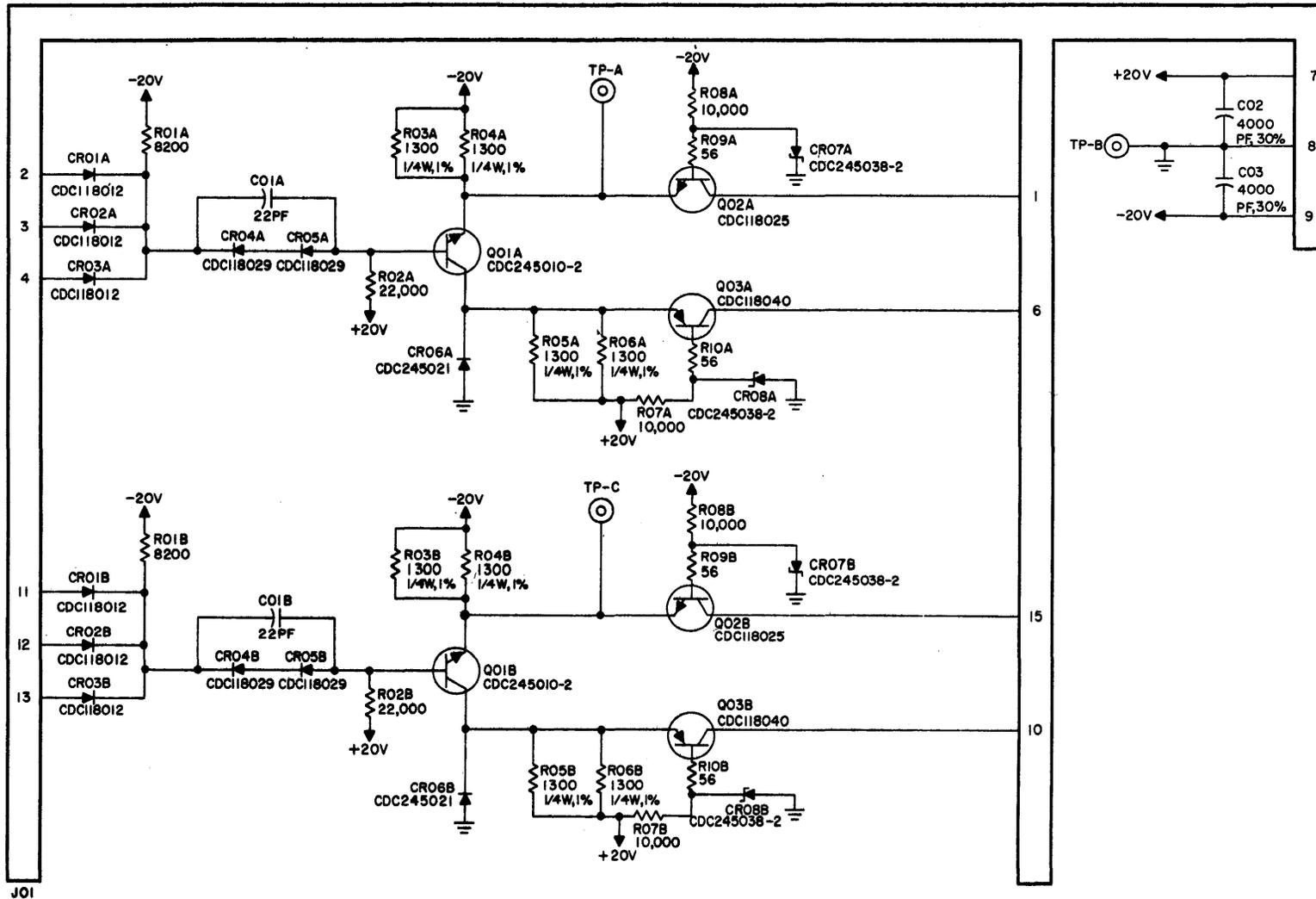
J01

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REFERENCE DRAWINGS		CONTROL DATA CORPORATION	
PRINTED CIRCUIT BOARD	309480	COMPUTER DIVISION	
COMPONENT ASSEMBLY	309478		
COMPONENTS (UNLESS OTHERWISE INDICATED)			
TOLERANCE	VALUE	DATE	PRODUCT OR PART NO.
RESISTORS	± 5 %	OHMS	1/4 WATT
CAPACITORS	± 20 %	PF	
TITLE		REVISION NUMBER	
TRANSMITTER - TYPE HA19, SCHEMATIC		Y C 309479	
		REV	



ZETA (074)



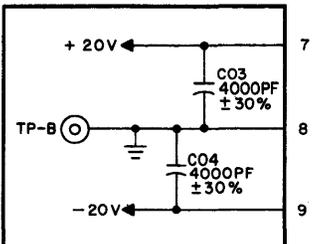
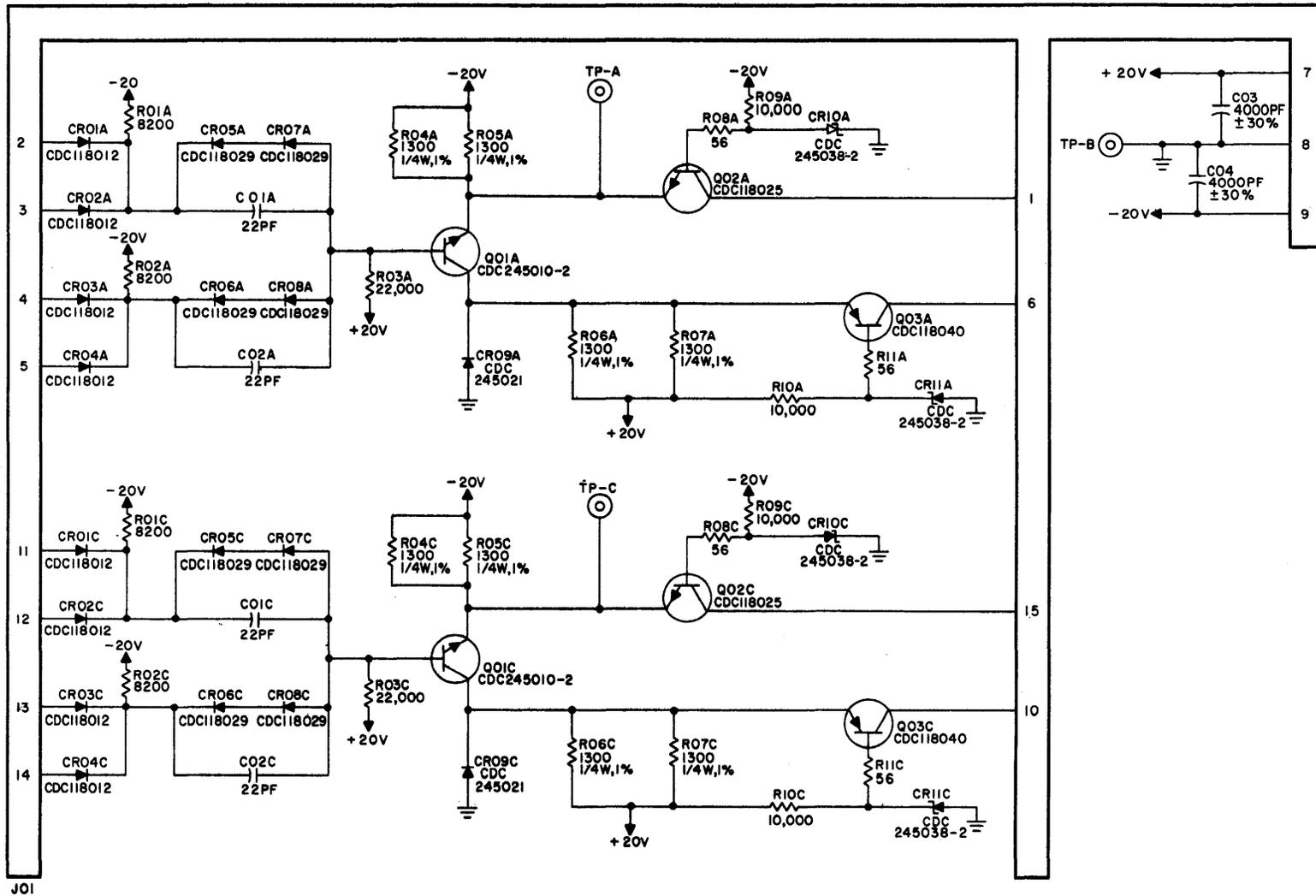
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REFERENCE DRAWINGS			
PRINTED CIRCUIT BOARD	309552		
COMPONENT ASSEMBLY	309550		
COMPONENTS UNLESS OTHERWISE INDICATED			
RESISTORS	TOLERANCE	VALUE	WATT
	± 5%	OHMS	1/4 WATT
CAPACITORS	TOLERANCE	VALUE	
	± 20%	PF	
TITLE		309551	
TRANSMITTER- TYPE HA37, SCHEMATIC		REV	



PROPERTY OF PRODUCT  
3600 (025)  
309551



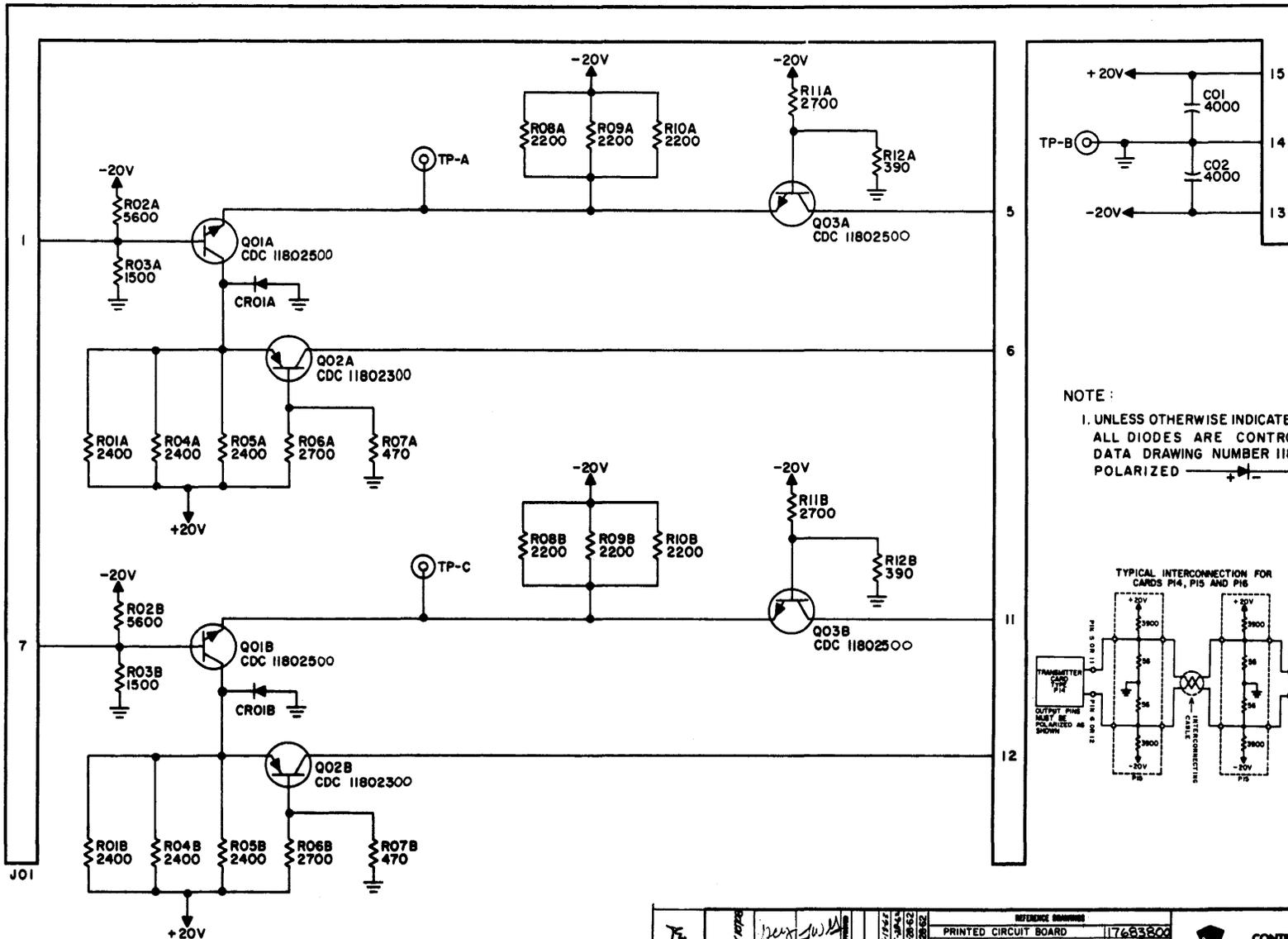
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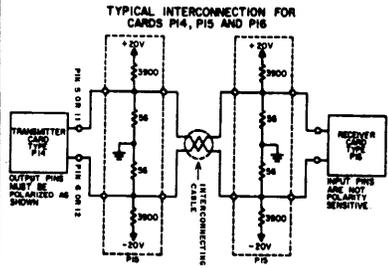
REFERENCE DRAWINGS		309592	
PRINTED CIRCUIT BOARD		309590	
COMPONENT ASSEMBLY		309590	
COMPONENTS UNLESS OTHERWISE INDICATED			
TOLERANCE	VALUE	SIZE	
RESISTORS	± 5 %	OHMS	1/4 WATT
CAPACITORS	± 20 %	PF	
TITLE		3600	REV
LINE DRIVER -		309591	
TYPE HA43, SCHEMATIC			

**CONTROL DATA CORPORATION**  
COMPUTER DIVISION

3600  
309591



NOTE:  
 1. UNLESS OTHERWISE INDICATED,  
 ALL DIODES ARE CONTROL  
 DATA DRAWING NUMBER 11801200  
 POLARIZED



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 TO

TE	VOIDED	SUPPLIES BY RTR	17683800
TE		RESIST	17683900
M.T.M.		SEM	
6-24-65	5-3-65	4-24-65	3-10-65
1070B	1042B	10344	RELEASED
E	D	C	B

REFERENCE DRAWINGS			
PRINTED CIRCUIT BOARD	17683800		
COMPONENT LAYOUT	17683900		
COMPONENTS (UNLESS OTHERWISE INDICATED)			
RESISTORS	± 5%	OHMS	1/4 W
CAPACITORS	± 20%	PF	
TITLE <b>TRANSMITTER-      TYPE P14C, SCHEMATIC</b>			

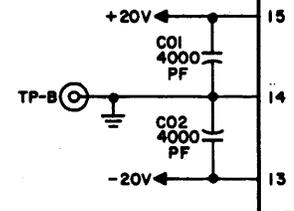
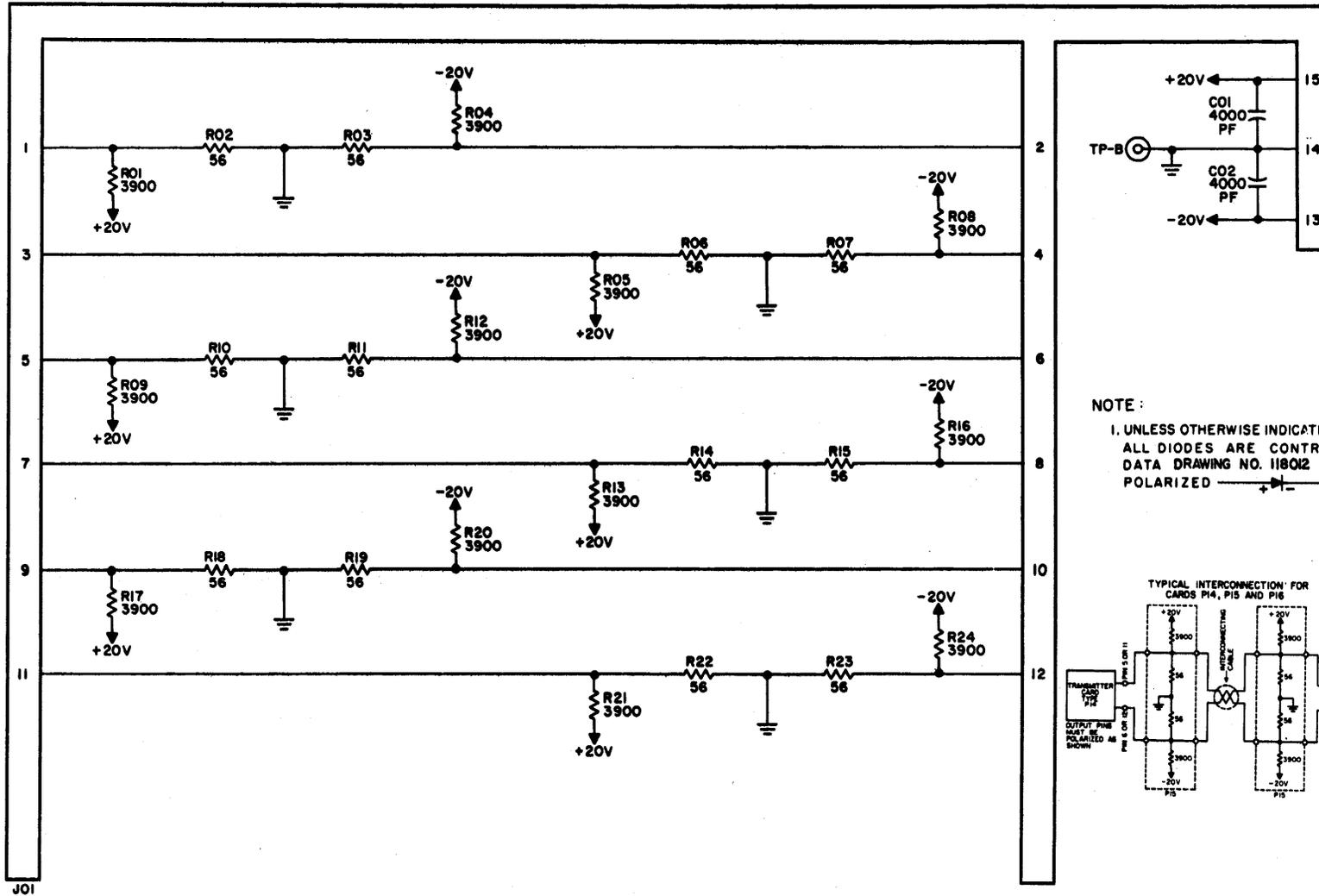
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 COMPUTER DIVISION

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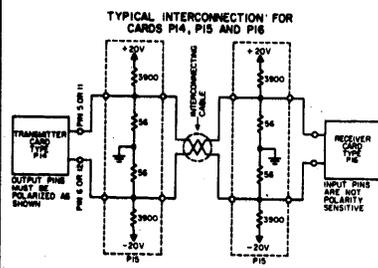
DRAWING NUMBER  
**YC 17684000**

REV  
**E**

1/14



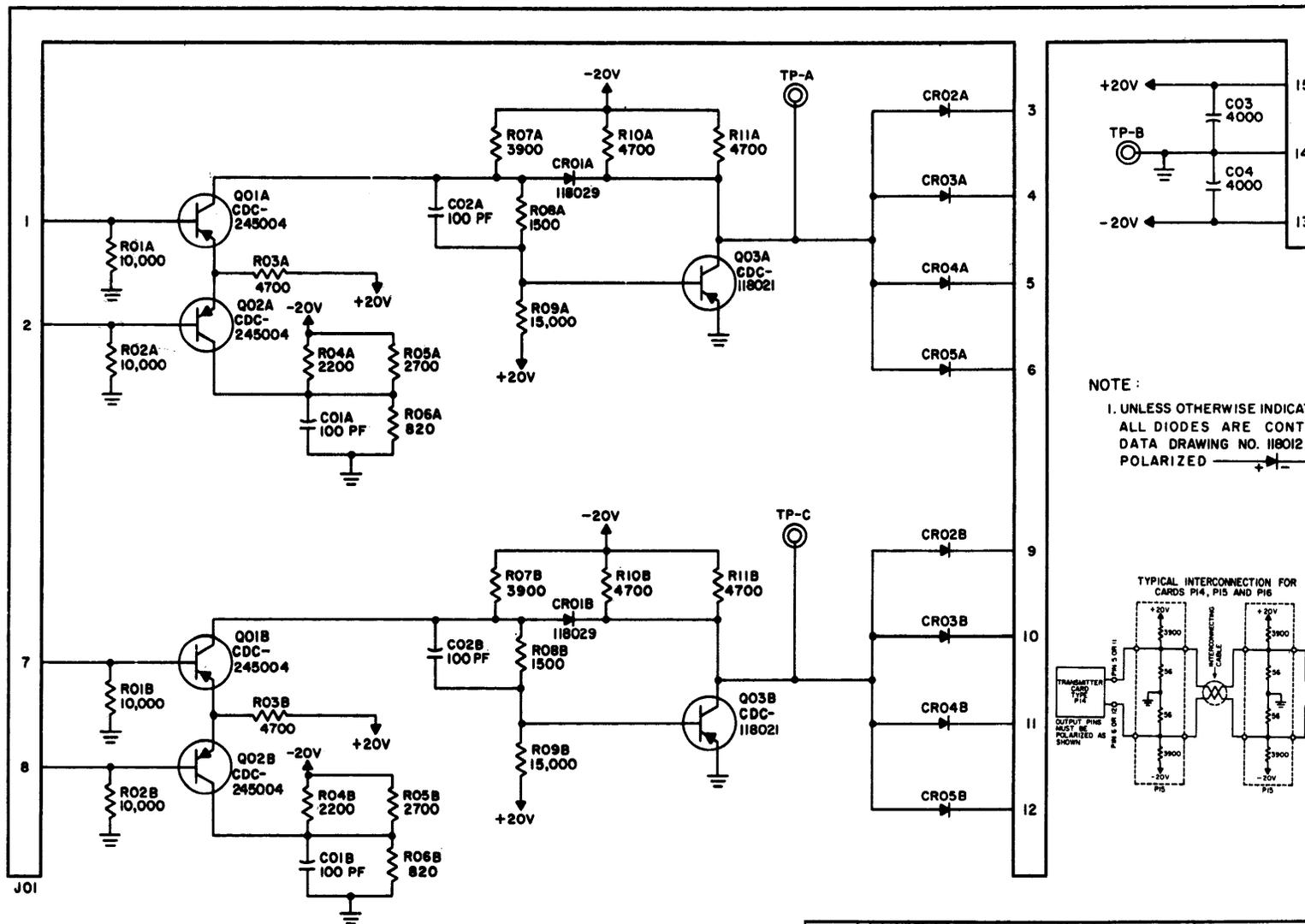
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 1. UNLESS OTHERWISE INDICATED,  
 ALL DIODES ARE CONTROL  
 DATA DRAWING NO. 118012  
 POLARIZED



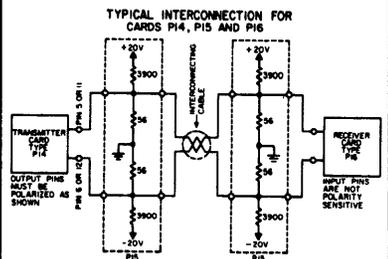
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REFERENCE NUMBERS		223101S	
PRINTED CIRCUIT BOARD		223111S	
COMPONENT ASSEMBLY			
COMPONENTS UNLESS OTHERWISE INDICATED			
RESISTORS	± 5 %	OHMS	1/4W
CAPACITORS	± 20 %	PF	
TITLE			
TRANSMISSION LINE TERM-		YC 2231215	
TYPE P15, SCHEMATIC		REV	

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 8952 (071)



NOTE:  
 1. UNLESS OTHERWISE INDICATED,  
 ALL DIODES ARE CONTROL  
 DATA DRAWING NO. 118012  
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H N		REVISED		REFERENCE DRAWINGS	
RAP		REVISED		PRINTED CIRCUIT BOARD 2231016	
H N		REVISED		COMPONENT ASSEMBLY 2231116	
8-63		REVISED		COMPONENTS (UNLESS OTHERWISE INDICATED)	
4726		REVISED		TOLERANCE VALUE SIZE	
A		REVISED		RESISTORS $\pm$ 5% OHMS 1/4 WATT	
		REVISED		CAPACITORS $\pm$ 20% P F	
TITLE				RECEIVER -	
				TYPE P16A, SCHEMATIC	
				PROJECT OR PRODUCT	
				8752 (071)	
				DRAWING NUMBER	
				YC 2231216	
				REV A	

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 COMPUTER DIVISION  
 8752 (071)  
 YC 2231216  
 REV A

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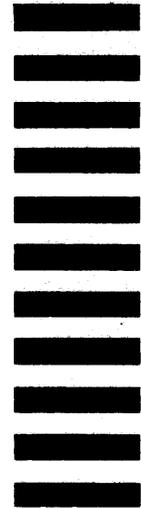
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