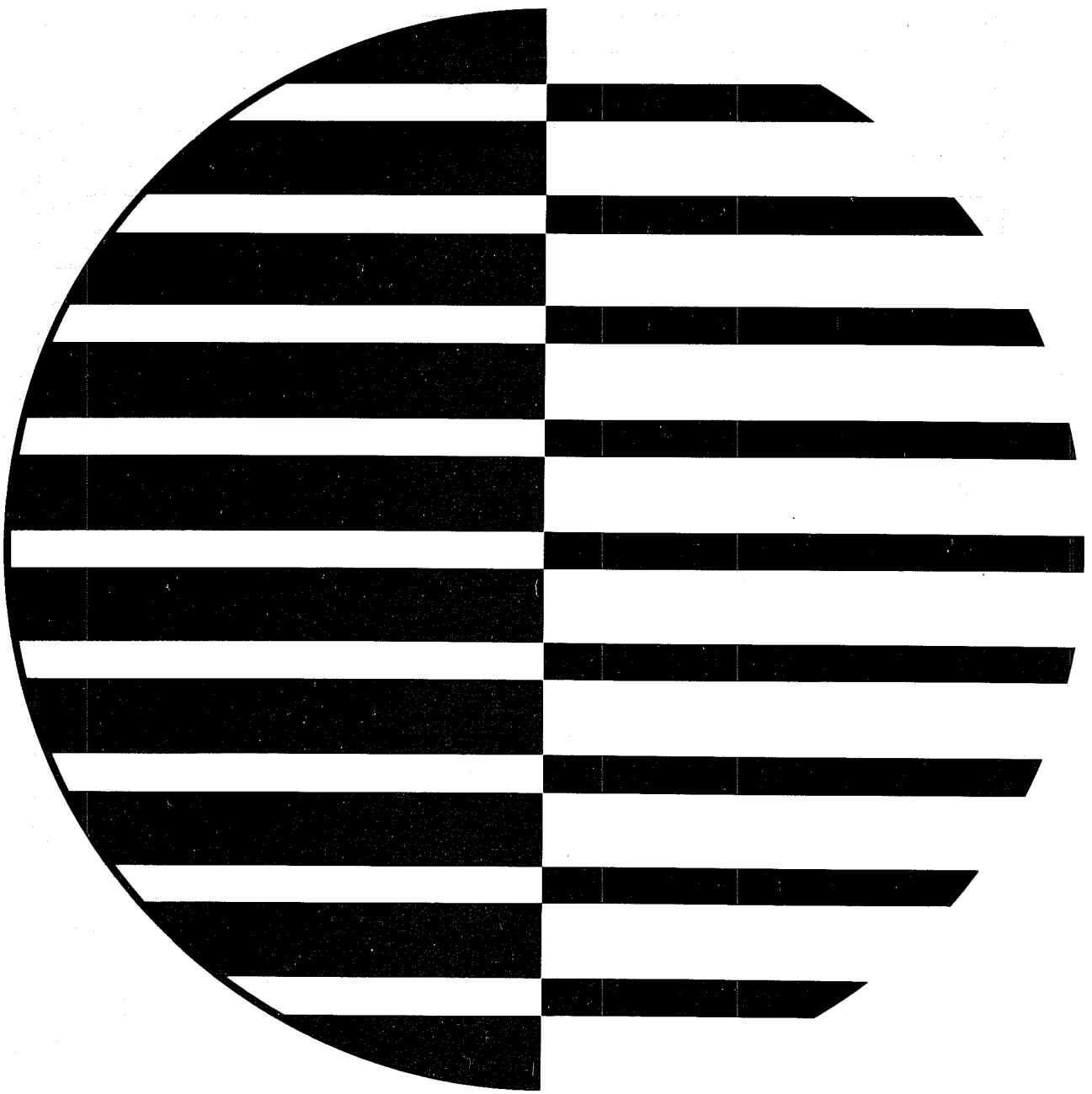
CONTROL DATA® 6000 SERIES COMPUTER SYSTEMS

Input/Output Specifications



60045100	**Record of Revisions**
REVISION	NOTES
A	Clarification of Text, pages v and 19 revised.
B	Change Order 11521 updated figures, changed cable specs
(9-24-65)	and removed appendix A. This manual obsoletes all
	previous editions.
C	Publications Change Order CA11922, miscellaneous
(11-9-65)	corrections on page 1-1.

Pub. No. 60045100
November, 1965

Address comments concerning this manual to:

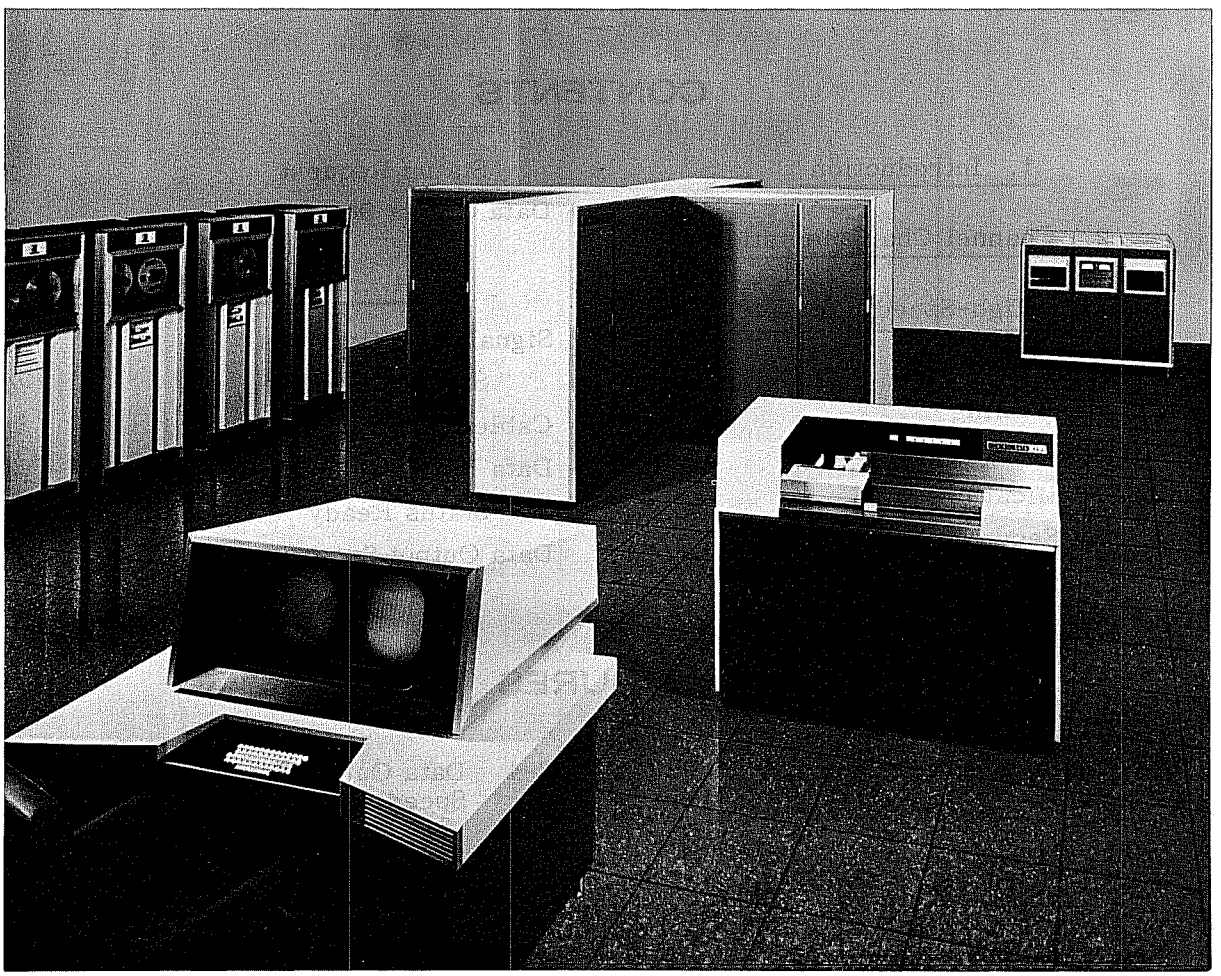
Control Data Corporation
Technical Publications Department
4201 North Lexington Avenue
St. Paul, Minnesota 55112

or use Comment Sheet in back of this manual.

CONTENTS

FIGURES

TABLES



1610

A CONTROL DATA 6000 SERIES COMPUTER SYSTEM

Display console (foreground) - includes a keyboard for manual input and operator control and two 10-inch display tubes for display of problem status and operator directives.

Main frame (center) - contains 10 Peripheral and Control Processors, Central Processor, Central Memory, some I/O synchronizers. The main frame in this photo is that of the 6600 Computer System; main frames for the 6400 or 6800 Systems vary in physical appearance, depending on options included in the system.

CONTROL DATA 607 Magnetic Tape Transport (left front) - 1/2-inch magnetic tape units for supplementary storage; binary or BCD data handled at 200, 556, or 800 bpi.

CONTROL DATA 626 Magnetic Tape Transport (left rear) - 1-inch magnetic tape units for supplementary storage; binary data handled at 800 bpi.

CONTROL DATA 405 Card Reader (right front) - reads binary or BCD cards at 1200 card per minute rate.

Disk file (right rear) - supplementary mass storage device; holds 500 million bits of information.

Rev. B

1. INTRODUCTION

This specification describes the CONTROL DATA* 6400/6600 Computer System Input/Output (I/O) characteristics and the I/O signals. The sequence of signals used to direct data exchange between the computer and external equipment is also given. This information will aid in successful connection and communication between the computer and printers, card equipment, displays, and other peripheral equipment.

The 6400/6600 Computer System includes 10 separate Peripheral and Control Processors, any one of which can exchange data with external equipment connected to 12 separate and identical Data Channels (Figure 1-1). Each external equipment communicates with the computer via a synchronizer. A synchronizer changes the one-shot pulse signals used by the computer into the signals required by the particular external equipment and vice versa. The synchronizers present two types of interface to external equipment: high-speed interface and low-speed interface. The high-speed interface uses one-shot pulse transmission on the I/O signal lines; the low-speed interface converts the high-speed interface signals to static d-c level signals and vice versa. The low-speed interface also accommodates a wide variety of data input only (e.g., card readers) or data output only (e.g., printers) type devices. An installation may include both interface types which may be connected to a common Data Channel. (See Figure 1-1.)

* Registered trademark of Control Data Corporation

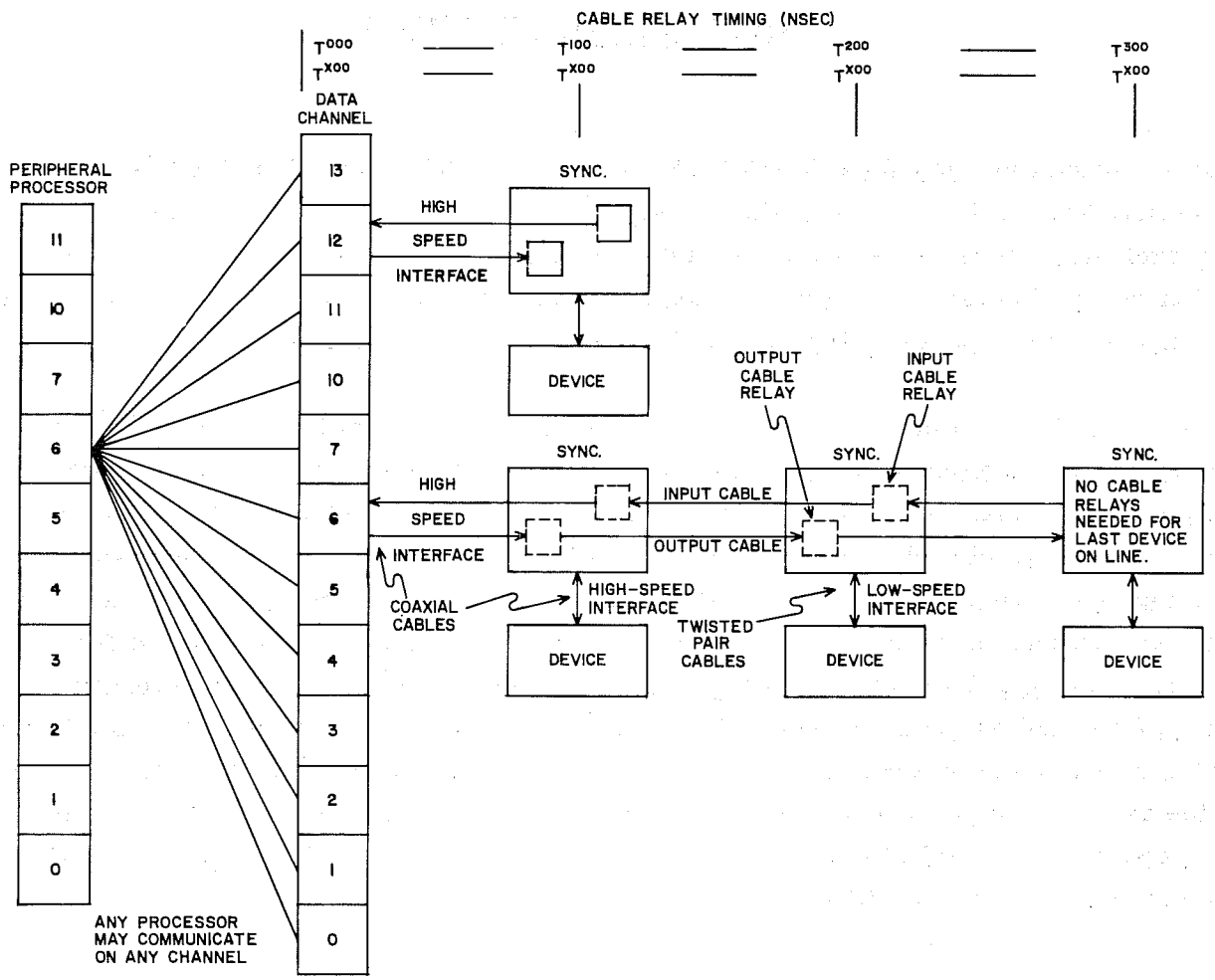


Figure 1-1. Interface Connections

2. CHANNEL CHARACTERISTICS

Each channel* handles 12-bit words at varying rates up to a maximum of one word every μsec, the equivalent of a one megacycle (mc) transfer rate. All channels may be in operation at the same time. Pulse communication is used on all the data and control lines of a channel, and all lines are synchronized to the Peripheral Processor clock system. Each channel has a 12-bit bidirectional register plus several bidirectional control designators which define the status of the register and the channel.

A Channel Active designator (flag) is set from an internal source to reserve a channel for communication between a processor* and synchronizer. A Channel Inactive signal from an internal or external source clears the Channel Active flag to terminate communication.

A Channel Full flag is set at the same time a word is entered in the channel register from an internal or external source. An internal or external Channel Empty signal clears the Full flag, which in turn statically clears the channel register.

The pulses on the data and control lines are one-shot, non-repeated type transmissions, and all synchronizers must provide for storing the information. Other control includes two Clock signals and one Master Clear signal for external devices. Clock signals are 10 mc (100 nsec period) and 1 mc (1 μsec period).

Channel data and control lines are grouped into two cables, input and output (Figure 2-1). The output cable carries processor signals to synchronizers; the input cable carries synchronizer signals to the processor and also carries the two processor Clock signals to

* All references to channel mean Data Channel; processor refers to Peripheral Processor.

synchronizers. All devices on a channel connect to the data and control lines in a series-parallel scheme (Figure 1-1). Each synchronizer samples the lines and unconditionally relays all signals to the next in-line synchronizer (which may be the processor). Each synchronizer times the signal relay on the 10 mc Clock signal from the processor so all synchronizers and the processor are synchronous and time-displaced from each other one or more clock periods. The scheme provides for orderly, high-speed data exchange.

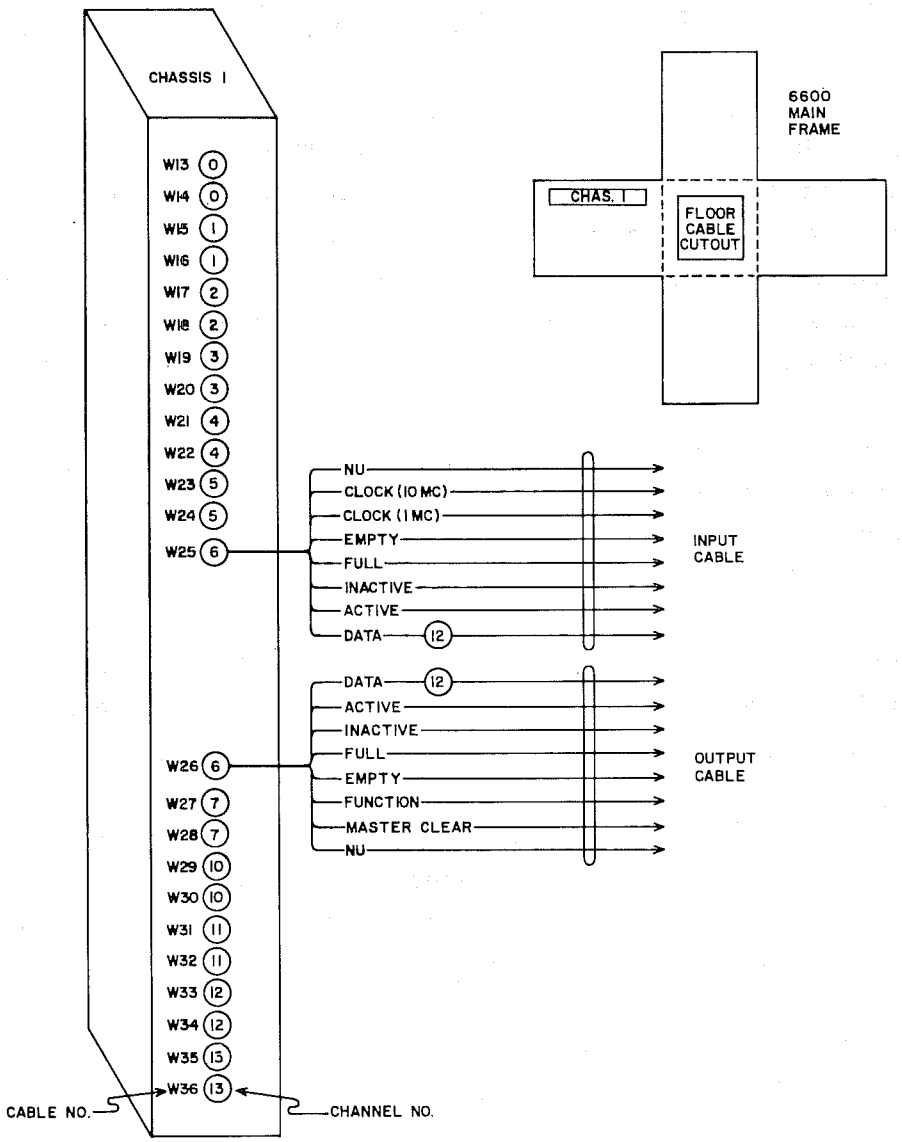


Figure 2-1. High-Speed Interface Signals

3. HIGH-SPEED INTERFACE

SIGNAL SPECIFICATIONS

The high-speed interface signals are listed in Table 3-1 and shown in Figure 3-1.

TABLE 3-1. COAXIAL CABLE LINES, HIGH-SPEED INTERFACE

INPUT CABLE	COLOR CODE	OUTPUT CABLE
Data 2^0	90	Data 2^0
Data 2^1	91	Data 2^1
Data 2^2	92	Data 2^2
Data 2^3	93	Data 2^3
Data 2^4	94	Data 2^4
Data 2^5	95	Data 2^5
Data 2^6	96	Data 2^6
Data 2^7	97	Data 2^7
Data 2^8	98	Data 2^8
Data 2^9	99	Data 2^9
Data 2^{10}	900	Data 2^{10}
Data 2^{11}	901	Data 2^{11}
Active	902	Active
Inactive	903	Inactive
Full	904	Full
Empty	905	Empty
Clock (10 mc)	906	Function
Clock (1 mc)	907	Master Clear
Not used	908	Not used

Binary one voltage is measured at the circuit terminals of the sending device as shown below. No voltage is impressed on the line for binary zero. Typical processor transmitter-receiver circuits and line voltage waveforms are shown in Figure 3-1.

Binary one	1.4v ± 0.1v
Pulse width	35 nsec ± 10 per cent
Pulse amplitude	1.4v peak at 19 ma into 73 ohm coaxial cable terminated in its approximate characteristic impedance
Rise time	5 nsec
Fall time	5 nsec

Input circuits in the external device synchronizer must terminate the line in its characteristic impedance to minimize standing waves.

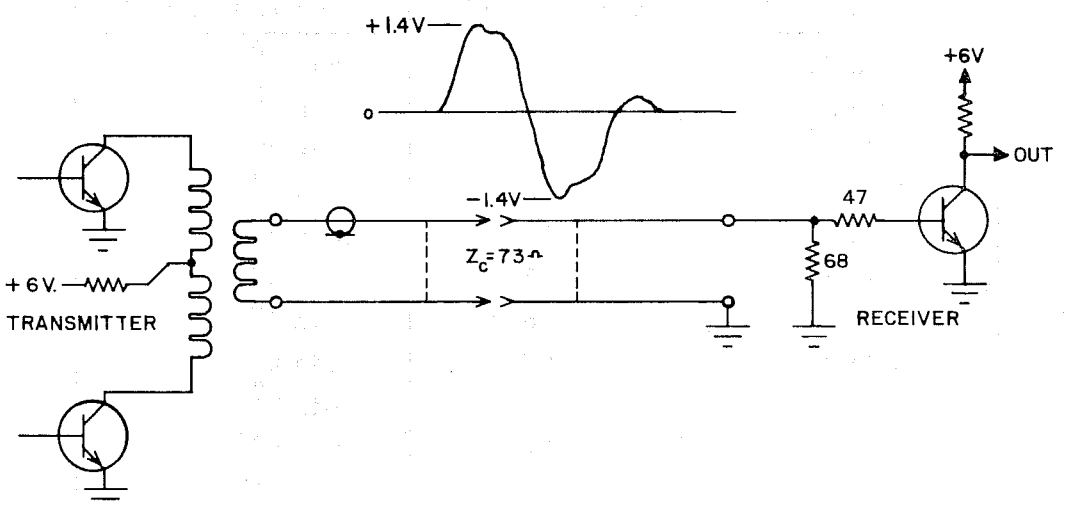


Figure 3-1. Transmitter-receiver Circuits and Line Voltage Waveform

Signal Timing

All lines connecting the processor and external device synchronizers are synchronized to the processor Clock signals. Signal delay on the lines and through synchronizer hardware must be taken into account to keep the data exchange synchronous. Coaxial cable delay is calculated at 1.5 nsec per foot.

The processor fills (and sends out on the line) or empties the channel register at one μsec intervals or multiples thereof. In a processor data output case, if the data is sent at processor time Y, then a synchronizer can sample the lines (Y + 1.5x) nsec later, where x = length of output cable in feet.

The acknowledging Synchronizer Empty signal (or Inactive signal) should arrive at the processor end of the input cable at an integral multiple of processor time Y (+0, -10 nsec) to avoid generating a runt pulse in the processor channel control. In a similar fashion, Data Input and Full signals from a synchronizer must arrive at the processor at an integral multiple of processor time Y (+0, -10 nsec). The Clock signals available externally provide a time reference point relative to the processor and can be used for signal clocking in the synchronizer.

The 10 mc Clock pulses lead data pulses by 25 nsec when a processor output word is on the lines. Processor data is identified by an accompanying Full pulse, function codes by a function pulse. Refer to Figure 3-2.

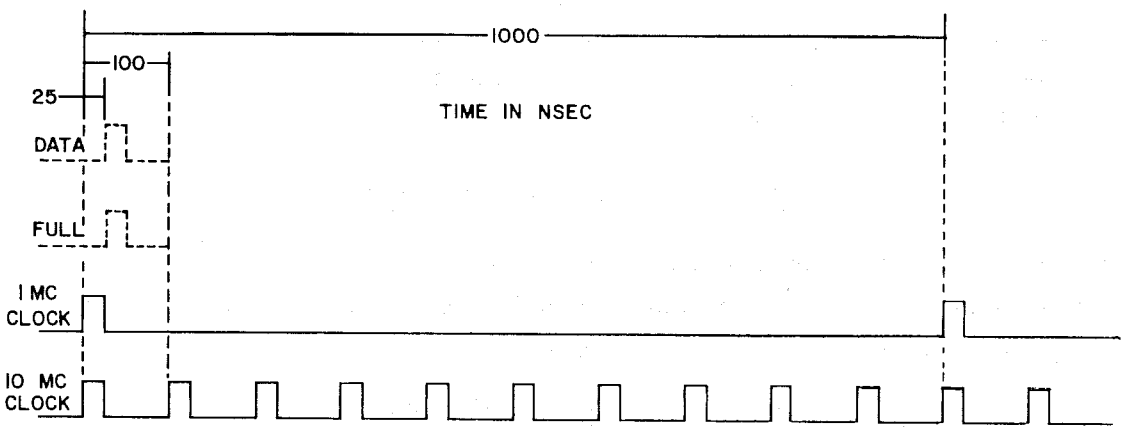


Figure 3-2. Clock Timing Sequence

Computation of cable time and signal delay time through internal hardware allows a synchronizer to place the signals on the lines for relay to the next in-line synchronizer at the same time relative to the processor, but later by an integral multiple of clock (10 mc) periods. Thus each synchronizer appears as the processor to the one next in line.

Depending on external requirements, the 10 mc clock pulses can be used to generate a multiple phase clock for incremental gating signals. The 1 mc clock pulses are synchronous with the 10 mc clock and are an alternate clocking signal for gating or other purposes.

The Master Clear line is pulsed at 4096 μsec periods as long as the DEAD START switch on the computer dead start panel is in ON position. The one μsec duration Master Clear establishes initial operating conditions.

Signal Relay

The signal relay is an integral part of each synchronizer. The relay is necessary in all synchronizers on a channel except in the one at the end of the line. Signal timing through the relay is at a 10 mc rate, and each synchronizer appears as the processor to the next in-line synchronizer. Each synchronizer samples and stores all output signal lines in addition to sending them on to the next in-line synchronizer.

Each synchronizer also transfers all input signal lines on to the next in-line synchronizer. In addition, the device must provide for entering its signals on the same lines. The network feeding the processor (or next-in-line synchronizer) is thus an OR combination of a synchronizer and the one feeding it.

CABLE SPECIFICATIONS

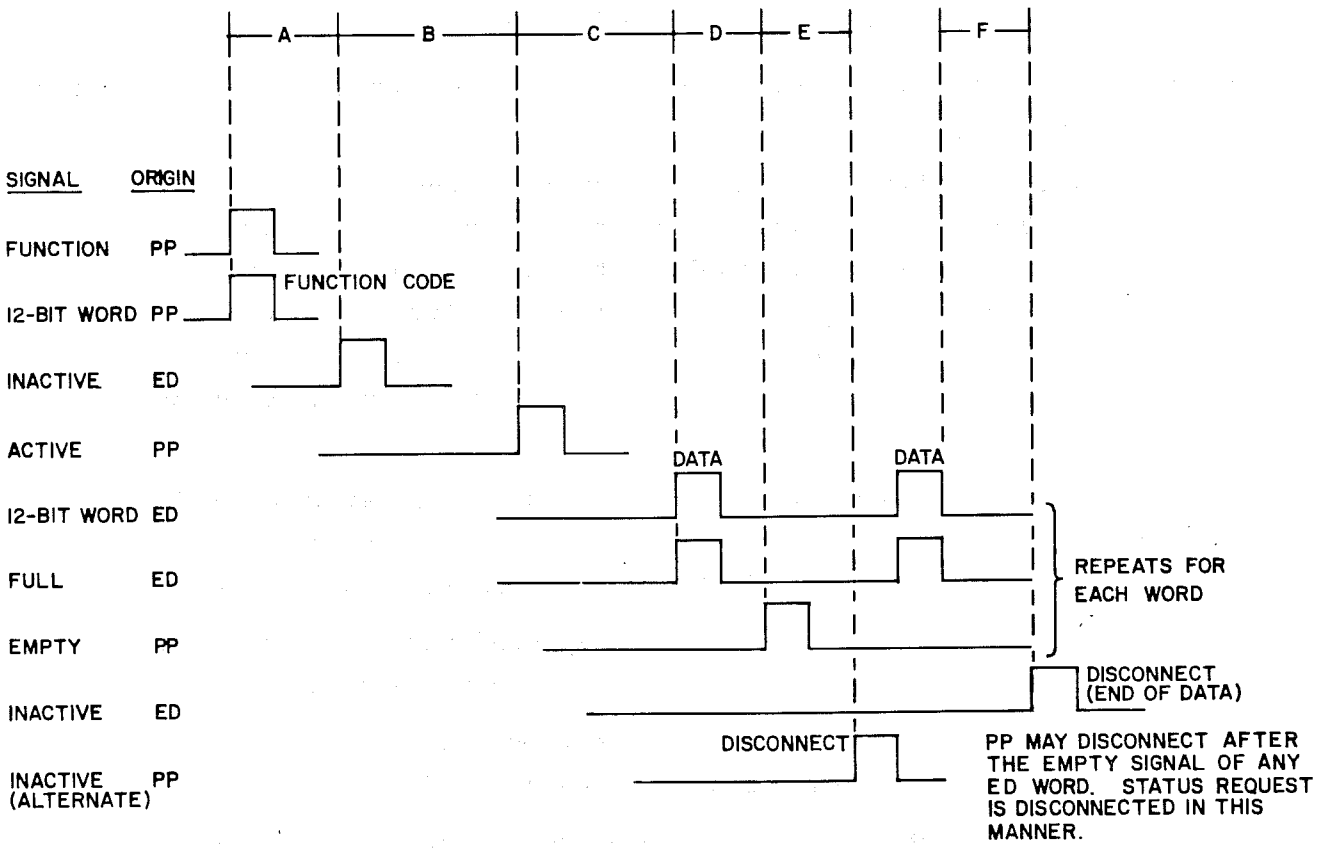
A 75-foot cable is used to connect each channel with external I/O equipment. The cable has 19 coaxial conductors, and each conductor and each shield is terminated with a taper pin. Specifications for this cable are listed below.

Cable (sheathed, coaxial)	Control Data Spec. No. 24567000
Length	75 feet
Number of coaxial conductors	19
Connectors	Taper Pins (22-24 AWG wire)
Impedance	70-73 ohms @ 1 mc
Line capacity	21.5 pf/foot maximum
Voltage rating	30 volt maximum

DATA INPUT SEQUENCE

An external device sends data to the processor by way of the synchronizer in the following manner (Figure 3-3):

1. The processor places a function word in the channel register and sets the Full flag and the Channel Active flag. Coincidently, it sends the word and a function signal to all synchronizers. The function signal tells all synchronizers to sample the word and identifies the word as a function code rather than a data word. The code selects a synchronizer and a mode of operation. Non-selected synchronizers clear, leaving only the selected one turned on.
2. The synchronizer sends an Inactive signal to the processor indicating acceptance of the function code. The signal drops the Channel Active flag which in turn drops the Full flag and clears the channel register.
3. The processor sets the Channel Active flag and sends an Active signal to the synchronizer which signals the device to start sending data.
4. The device reads a word and then sends the word to the channel register with a Full signal which sets the Channel Full flag.
5. The processor stores the word, drops the Full flag, and returns an Empty signal indicating acceptance of the word. The device clears its data register and prepares to send the next word.
6. Steps 4 and 5 repeat for each word transferred.
7. At the end of the transfer, the synchronizer clears its Active condition and sends an Inactive signal to the processor to indicate end of data. The signal clears the Channel Active flag to disconnect the synchronizer and the processor from the channel.
8. As an alternative, the processor may choose to disconnect from the channel before the device has sent all of its data. The processor does this by dropping the Active flag and sending an Inactive signal to the synchronizer which immediately clears its Active condition and sends no more data, although the device may continue to the end of its record or cycle (e.g., a magnetic tape unit would continue to end-of-record and stop in the record gap).



PP = Peripheral and Control Processor; ED = External Device

A. Time is a function of ED - PP recognizes inactive 1 μsec after function or at an integral multiple thereafter

B. Time is a function of PP - Minimum time 2 μsec, maximum time an integral multiple of 1 μsec intervals thereafter

C. Time is a function of ED

D. Time is a function of PP - Minimum time 100 nsec, maximum time an integral multiple of 100 nsec intervals thereafter

E. Time is a function of PP - Minimum time 3 μsec, maximum time an integral multiple of 1 μsec intervals thereafter

F. Time is a function of ED

Figure 3-3. Data Input Sequence, High-Speed Interface

Status Request

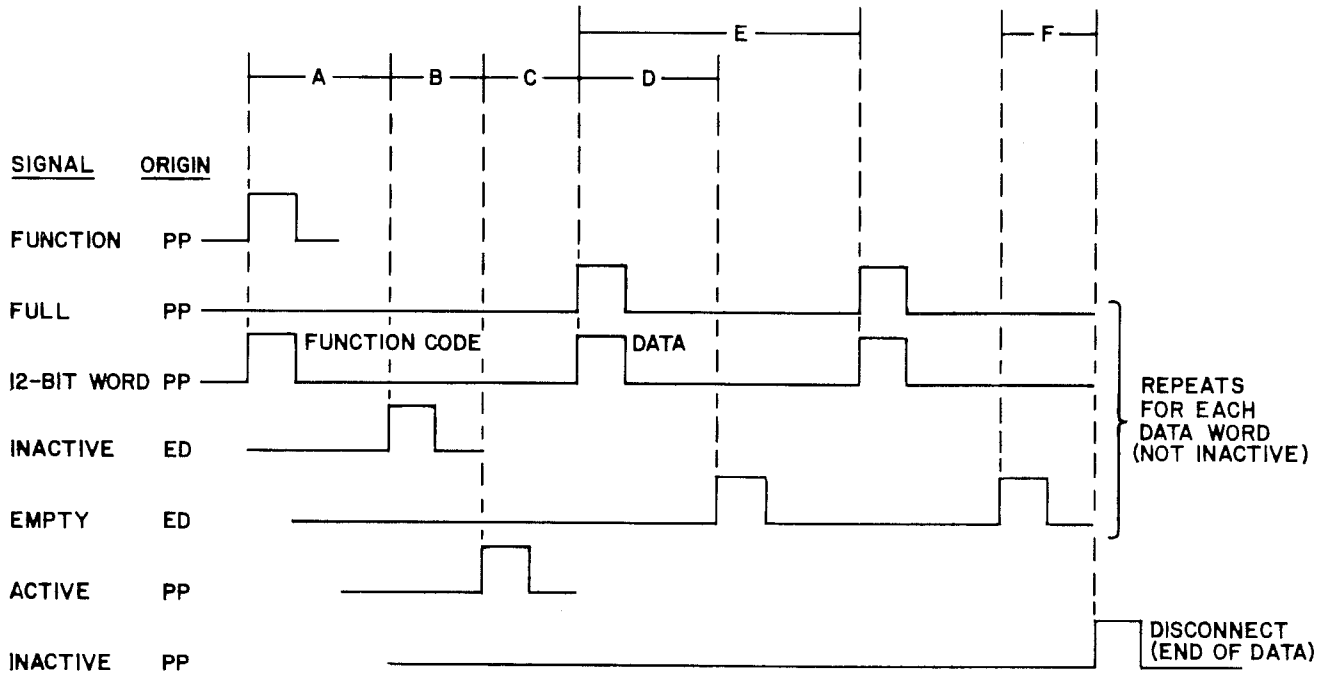
A Status Request is a special one word data input transfer in which an external device indicates a Ready or Error condition to a processor (Figure 3-3).

1. The processor places a function word in the channel register and sets the Full flag and the Channel Active flag. Coincidently, it sends the word and a function signal to all synchronizers. The function signal tells all synchronizers to sample the word and defines the word as a function code rather than a data word. The code selects a synchronizer and places it in Status Mode. Non-selected synchronizers clear, leaving only the selected one turned on.
2. The synchronizer sends an Inactive signal to the processor indicating acceptance of the Status Function code. The signal drops the Channel Active flag which in turn drops the Full flag and clears the channel register.
3. The processor sets the Channel Active flag and sends an Active signal to the synchronizer which signals the device to send the Status word.
4. The synchronizer sends the Status word to the channel register with a Full signal which sets the Channel Full flag.
5. The processor stores the word, drops the Full flag, and returns an Empty signal indicating acceptance of the word.
6. The processor drops the Channel Active flag to disconnect the channel and sends an Inactive signal to the synchronizer to disconnect it.

DATA OUTPUT SEQUENCE

The processor sends data to an external device in the following manner (Figure 3-4):

1. The processor places a function word in the channel register and sets the Full flag and the Channel Active flag. Coincidently, it sends the word and a function signal to all devices. The function signal tells all synchronizers to sample the word and identifies the word as a function code rather than a data word. The code selects a synchronizer and a mode of operation. Non-selected synchronizers clear, leaving only the selected one turned on.
2. The synchronizer sends an Inactive signal to the processor, indicating acceptance of the function code. The signal drops the Channel Active flag which in turn drops the Full flag and clears the channel register.
3. The processor sets the Channel Active flag and sends an Active signal to the synchronizer which signals the device that data flow is starting.
4. The processor places a data word in the channel register and sets the Full flag. Coincidently, it sends the word and a Full signal to the synchronizer.
5. The synchronizer accepts the word and sends an Empty signal to the processor where it clears the channel register and drops the Full flag.
6. Steps 4 and 5 repeat for each processor word.
7. After the last word is transferred and acknowledged by the Synchronizer Empty signal, the processor drops the Channel Active flag and sends an Inactive signal to the synchronizer to turn it off.



PP = Peripheral and Control Processor; ED = External Device

A. Time is a function of ED - PP recognizes inactive 1 μsec after function or at an integral multiple thereafter

B. Time is a function of PP - Minimum time 2 μsec, maximum time an integral multiple of 1 μsec intervals thereafter

C. Time is a function of PP - Minimum time 2 μsec or 4 μsec depending on instruction

D. Time is a function of ED

E. Time is a function of ED - Minimum PP time is 1 μsec

F. Time is a function of PP - Minimum time 2 μsec after empty from ED

Figure 3-4. Data Output Sequence, High-Speed Interface

4. LOW-SPEED INTERFACE

The low-speed interface converts static d-c level signals to high-speed interface pulse signals and vice versa. Twisted-pair lines connect the external device to the low-speed interface, and the latter connects to the high-speed interface via coaxial cable (Figure 4-1).

SIGNAL SPECIFICATIONS

Low-speed interface signals are listed in Table 4-1 and described below.

Binary one and zero voltages are measured at the output terminals of the sending device and are as follows:

Binary one	-0.5v (+0.5v, -2.5v)
Binary zero	-16v (-2.5v)
Current supply	10 ma
Rise time:	2 μsec minimum, 4 μsec maximum
Line capacity	0 to 2000 pf maximum

Signal Timing

The low-speed interface uses a ready-resume scheme for data exchange. The data transmitter sends a Ready signal with data, and the receiver acknowledges receipt of data with a Resume signal. The Resume turns off the Ready, and this action turns off the Resume.

The output data lines also carry the function code. Data is accompanied by an Information Ready signal and a function code by a function Ready signal.

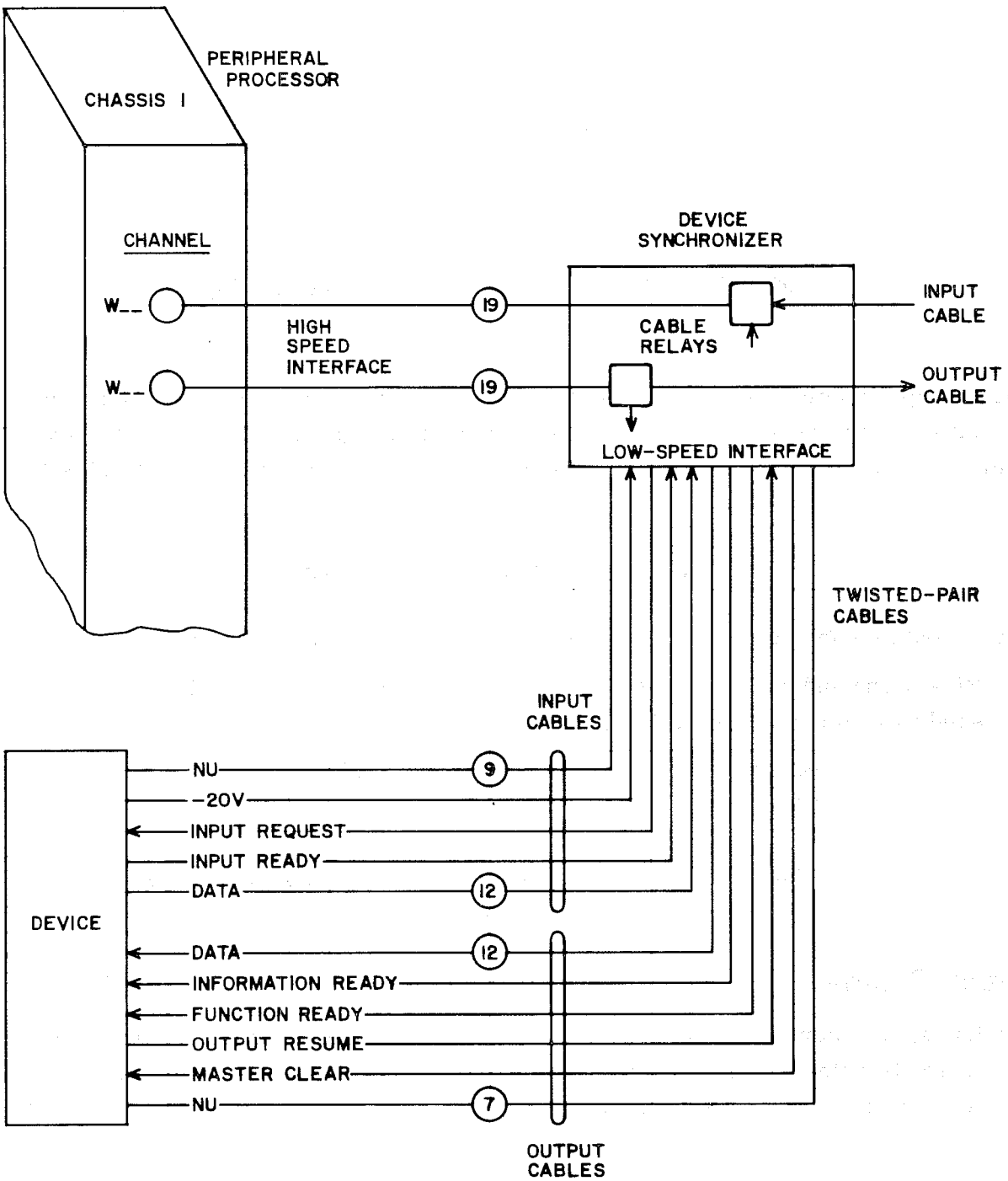


Figure 4-1. Low-Speed Interface Signals

TABLE 4-1. TWISTED PAIR LINES, LOW-SPEED INTERFACE

INPUT CABLE	PIN	COLOR	OUTPUT CABLE
Data 2^0	A	0	Data 2^0
Data 2^1	B	2	Data 2^1
Data 2^2	C	4	Data 2^2
Data 2^3	D	5	Data 2^3
Data 2^4	E	6	Data 2^4
Data 2^5	F	90	Data 2^5
Data 2^6	H	91	Data 2^6
Data 2^7	J	92	Data 2^7
Data 2^8	K	93	Data 2^8
Data 2^9	L	94	Data 2^9
Data 2^{10}	M	95	Data 2^{10}
Data 2^{11}	N	96	Data 2^{11}
	P	97	
Input Ready	R	98	Information Ready
Input Request	S	900	Output Resume
	T	910	Function Ready
	U	920	Master Clear
	V	930	
	W	940	
	X	950	
	Y	960	
	Z	970	
-20v	a	980	
	b	Grd	

The input data lines carry data and also carry the Status Request code but use a common input ready control line. The processor program distinguishes data and status information.

The Master Clear line is switched to a binary one level every 4096 μsec as long as the DEAD START switch on the computer dead start panel is in ON position. This signal establishes initial operating conditions.

CABLE SPECIFICATIONS

Low-speed interface signals are carried in two cables, input and output, and are terminated at one end in customer specified connectors. The interface connection is fitted with Amphenol connectors.

Cable (sheathed, 24 twisted-pair conductors)	Brand-Rex Turbo Type No. 4545
Length	50 feet maximum
Number of twisted-pair conductors	24 (No. 24 stranded)
Connectors	Amphenol 67-06P20-37P
Cable ground return d-c resistance	0.5 ohm

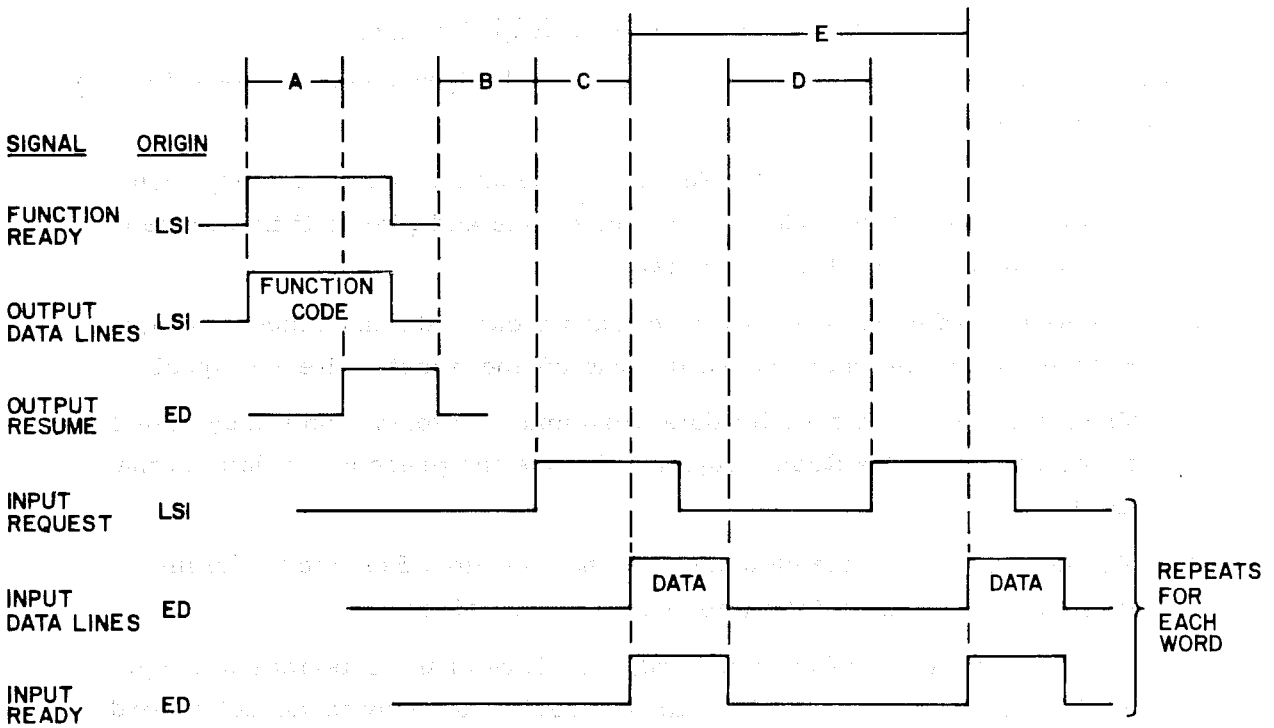
DATA INPUT SEQUENCE

An external device sends data to the processor through the low-speed interface in the following way (Figure 4-2). This sequence is related to low-speed interface signals only.

1. The interface sends a 12-bit function code and a function Ready signal to its devices. The code selects one device and places it in a mode of operation and de-selects all others.
2. The selected device accepts the code at its own rate and sends an Output Resume to the interface where it turns off the function Ready signal.
3. The interface sends an Input Request signal to the device indicating it is ready to accept data.
4. The device places a word on the data lines and sends an Input Ready to the interface where it turns off the Input Request.
5. Steps 3 and 4 repeat for each input word requested by the processor. Failure of the interface to supply the Input Request at the time the device is ready to send data indicates end of operation.

Status Request

A Status Request is a coded one-word input transfer in which an external device indicates a Ready or Error condition to a processor (Figure 4-2). The transfer is identical with the data input sequence.



LSI = Low-Speed Interface; ED = External Device

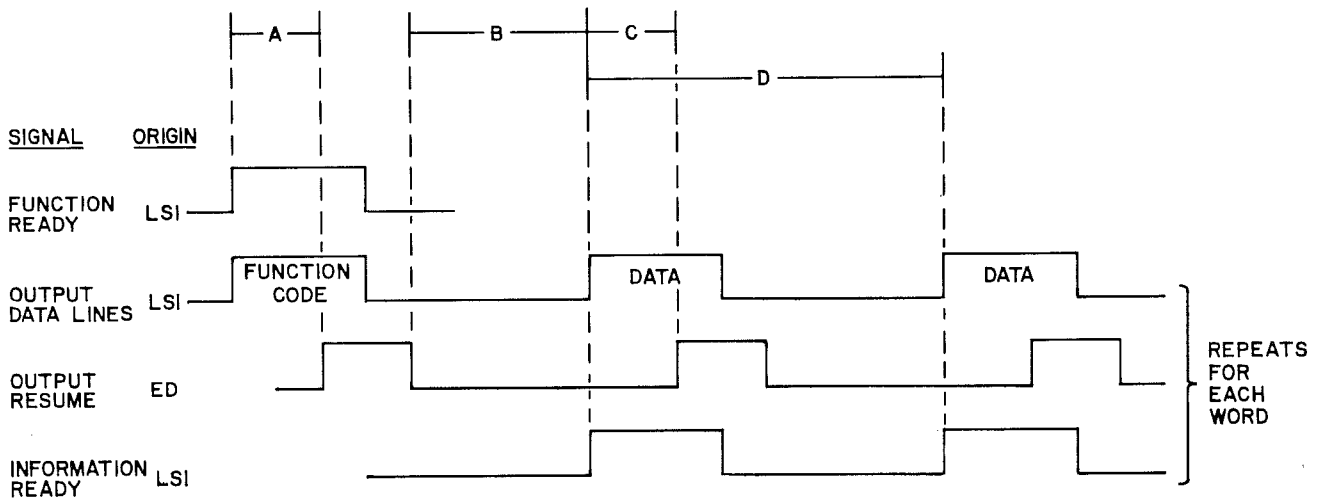
A. Time is a function of ED
B. 2 μsec minimum
C. Time is a function of ED
D. 2 μsec minimum
E. Time is a function of ED

Figure 4-2. Data Input Sequence, Low-Speed Interface

DATA OUTPUT SEQUENCE

The processor sends data to an external device via the low-speed interface in the following manner (Figure 4-3).

1. The interface sends a 12-bit function code and a function Ready signal to its devices. The code selects one device and places it in a mode of operation, and de-selects all others.
2. The selected device accepts the code at its own rate and sends an Output Resume to the interface where it turns off the function Ready signal.
3. The interface sends a 12-bit data word and an Information Ready signal to the device. The Ready signal indicates the presence of data on the lines.
4. The device accepts the data and returns an Output Resume to the interface where it turns off the Information Ready signal.
5. Steps 3 and 4 repeat for each word. Failure of the interface to supply an Information Ready at the time the device is ready to accept a word indicates end of data.



LSI = Low-Speed Interface; ED = External Device

A. Time is a function of ED
B. 2 μsec minimum
C. Time is a function of ED
D. Time is a function of ED

Figure 4-3. Data Output Sequence, Low-Speed Interface

CUT ALONG LINE

COMMENT SHEET

6000 Series Computer Systems
Input/Output Specifications

Pub. No. 60045100

FROM NAME : _____

BUSINESS ADDRESS : _____

COMMENTS: (DESCRIBE ERRORS, SUGGESTED ADDITION OR DELETION AND INCLUDE PAGE NUMBER, ETC.)

NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

FOLD ON DOTTED LINES AND STAPLE

STAPLE

STAPLE

FOLD

FOLD

FIRST CLASS
PERMIT NO. 8241

MINNEAPOLIS, MINN.

BUSINESS REPLY MAIL

NO POSTAGE STAMP NECESSARY IF MAILED IN U.S.A.

POSTAGE WILL BE PAID BY

CONTROL DATA CORPORATION
8100 34TH AVENUE SOUTH
MINNEAPOLIS 20, MINNESOTA

ATTN: TECHNICAL PUBLICATIONS DEPT.
COMPUTER DIVISION
PLANT TWO

FOLD

FOLD

CUT ALONG LINE