60437300

CONTROL DATA CORPORATION

CDC®
7639-1/21
7639-2/22
MASS STORAGE CONTROLLERS
STANDARD OPTION 10339-1/10424-1
MASS STORAGE CONTROLLERS
STANDARD OPTION 10423-1/2
DOUBLE TRACK DENSITY

HARDWARE REFERENCE MANUAL

New features, as well as changes, deletions, and additions to information in this manual are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

REVISION RECORD

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or use Comment Sheet in the back of this manual.

PREFACE

This manual provides basic operating information for the CDC® 7639-1/2/21/22 Mass Storage Controllers. The 7639-1/21, 7639-2/22, and CDC® Standard Option 10339-1/10424-1 Mass Storage Controllers can be a part of a CDC® 7600, CDC® CYBER 70 Model 76, or CDC® CYBER 170 Model 176 Computer System. The CDC® Standard Option 10423-1/2 allows the controller to interface double track density disk storage units. For more information describing the controller, disk storage unit, and 7600 interface, refer to the following manuals. Refer to the Literature Distribution Services Catalog for ordering information.

Control Data Publication	Publication No.
7600/CYBER 70 Model 76 Computer Systems Input/Output Specifications	60408700
FA202-A/B/C/D/E and FA103-A/B Mass Storage Controllers Hardware Maintenance Manual	60427600
BR304 Disk Storage Unit Hardware Maintenance Manual	70627900
BR304 Disk Storage Unit Hardware Reference Manual	70628000
BR319 Disk Storage Unit Hardware Maintenance Manual	83322770
BR319 Disk Storage Unit Hardware Reference Manual	83322780
BR319 Parts Data Manual	83322950

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SYSTEM DESCRIPTION 1

The 7639-1/21, 7639-2/22, and Standard Option 10339-1/**10424-1** Mass Storage Controllers provide a hardware interface between a CDC® 7000 type peripheral processing unit (PPU) and a CDC® Model 819 Disk Storage Unit (DSU). The PPU is part of a CDC CYBER 170 Model 176, CDC CYBER 70 Model 76, or 7600 Computer System. The 7639-1/21 consists of one controller housed in a cabinet containing power supplies and blowers. The 7639-2/22 consists of two controllers housed in one cabinet with the power supplies and blowers. Standard Option 10339-1/10424-1 consists of one controller without a cabinet, power supply, or blower. The standard option is added to the 7639-1/21 to expand the configuration. This is a field installable option, which is placed in the 7639-1/21 cabinet. The combination of the 7639-1 and the 10339-1 option is identical to the 7639-2. The 10424-1 option converts the 7639-21 to a 7639-22.

The 7639-21, 7639-22, and Standard Option 10424-1 controllers have double track density capability allowing them to handle double density DSUs. The controllers can handle a mixture of single and double track density DSUs. The double track density DSUs have twice the storage capacity of the single track density DSUs.

The CDC® Double Track Density Option 10423-1 converts the 7639-1 controller to the 7639-21 controller. The 10423-2 option converts the 7639-2 controllers to the 7639-22 controllers.

NOTE

In all subsequent descriptions, the term controller refers to an independent logical entity. Where two controllers are present in a cabinet, as in the 7639-2, the descriptions that follow apply to the controllers equally.

Each controller contains four PPU and four DSU accesses. A maximum of two PPUs from the same mainframe can be attached to the controller. In a maximum configured 7639-1, the controller would be attached to four PPUs, two from mainframe A and two from mainframe B, and to four DSUs. In a maximum configured 7639-2 this would be true of both controllers. Figure 1-1 illustrates a typical configuration for a 7639-1/21.

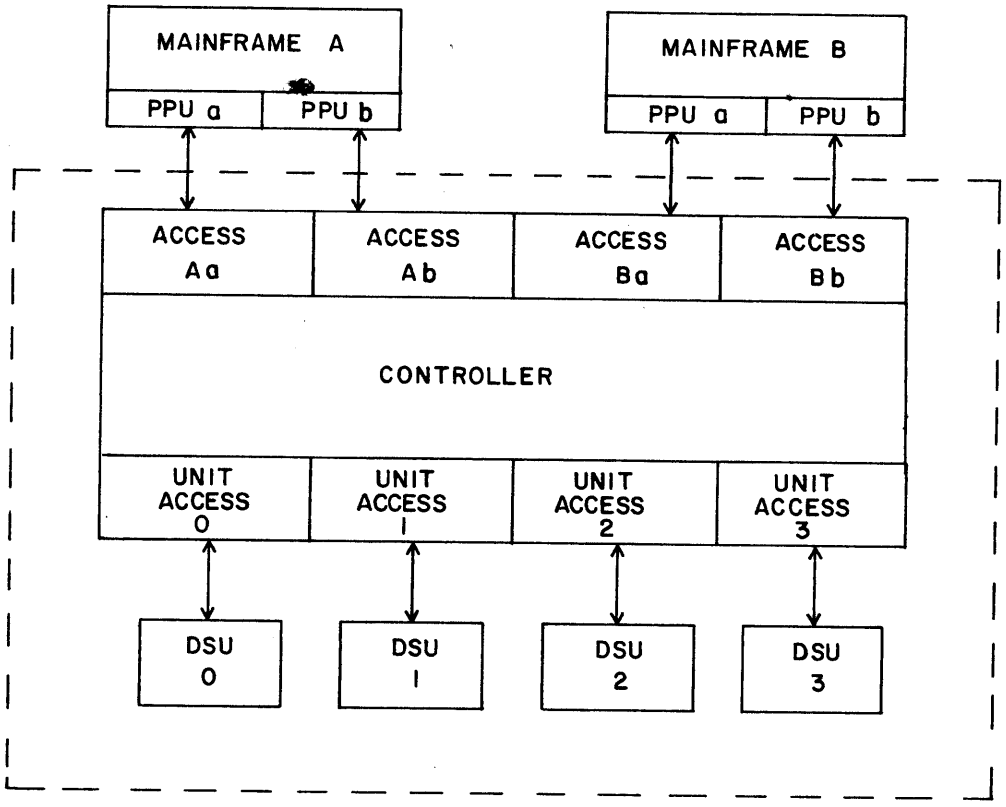


Figure 1-1. Typical Configuration

CONTROLLER

Each PPU is connected to the controller by two bidirectional 12-bit channels (a data and control channel). Four-bit data paths connect the controller to each DSU. The controller assembles and disassembles data, detects and corrects errors, deskews data read from a DSU, and performs the other control function necessary to transfer data between a PPU and DSU.

DISK STORAGE UNIT

Each DSU has two controller interfaces. If a DSU is attached to two controllers, it can communicate with only one controller at a time. Data is written on the disk in 4-bit parallel bytes. The DSU has the following recording characteristics.

Mode	Modified frequency modulation
Density (inner track)	6000 bits per inch nominal
Number of disks	22
Number of servo surfaces	1
Total recording surfaces	40
Number of tracks per surface	411 (823 for double track density units)
Total disk diameter	14 inches
Track spacing	192 tracks per inch (5.2 mils, center to center)
Track spacing (double track density units)	384 tracks per inch (2.6 mils, center to center)
Track width	4.4 mils (2.2 mils for double track density units)
Number of servo heads	1
Number of recording heads	40
Number of heads parallel	4
Spindle speed	3600 revolutions per minute (± 72)

PHYSICAL DESCRIPTION

One controller in a cabinet consists of a 2-row logic chassis, TTL 25-paks, a +5-volt 100-ampere dc power supply, a 5-volt 50-ampere dc power supply, a power distribution box, and a blower housed in the cabinet. Two controllers in a cabinet add another 2-row logic chassis and additional 25-paks. Each DSU consists of a cabinet containing a disk pack spindle with an associated drive motor, voice coil positioning mechanism, disk pack, power supply, and logic chassis.

CABLING

	Quantity	Length (maximum)
PPU access	4 per access	60 feet (18.3 metres)
DSU access	2 per access	75 feet (22.9 metres)
DSU	1 per unit	100 feet (30.5 metres)

ELECTRICAL REQUIREMENTS

Controller	120 volts, 50/60 Hz, 1Ø, 0.9 amperes per phase
	208 volts, 400 Hz, 3Ø, 1.7 amperes per phase
DSU	208 volts, 60 Hz, 3Ø, 9.5 amperes per phase (maximum)

ENVIRONMENTAL REQUIREMENTS

		Controller	DSU
Temperature	Operating	60°F to 90°F	60°F to 90°F
	Nonoperating	-30°F to 150°F	-30°F to 150°F
	Maximum gradient	20°F per hour	12°F per hour
	Recommended operating temperature	75°F	75°F
Relative Humidity	Operating	10% to 90%	30% to 80% (with no condensation)
	Nonoperating	5% to 95%	5% to 95%
Altitude	Maximum operating	6000 feet	6000 feet
Cooling	Internal fans	500 CFM	325 CFM

FUNCTIONAL DESCRIPTION

A PPU must reserve the controller before any communication can occur. A PPU does this by sending a function to the controller. The controller can maintain a 3.1 MHz transfer rate.

The controller performs the following major tasks.

1. Converts logic levels so that the data channel and controller are compatible. This is necessary because the controller uses TTL and the data channel uses 7000 logic levels.
2. Assembles and disassembles data. Each 12-bit byte from the PPU must be disassembled into three 4-bit bytes. Each 4-bit byte from the DSU must be assembled into a 12-bit byte.
3. Removes skew from data read from a DSU.
4. Executes functions from the PPU. This allows the controller to check DSU status, connect a DSU, address a DSU, or establish any other conditions necessary to transfer data.

5. Generates a preamble and sync byte which precedes each data sector.
6. Generates a 32-bit checkword for each channel.
7. Detects and corrects errors during data transfers.

DATA ORGANIZATION

Data blocks are a fixed length in the subsystem. All data transfers between the controller and PPU go to or come from the PPU memory.

DATA CAPACITY

	Number of 4-Bit Words (Decimal)	
Preamble	300	
Sync-byte	2	
Data	7692	(2564 12-bit words)
Checkword	32	
Postamble	6	
Sector gap	20	
Total per sector	8052	
Index gap	240	
Cells per revolution	161,280	(Based on 20 sectors)†

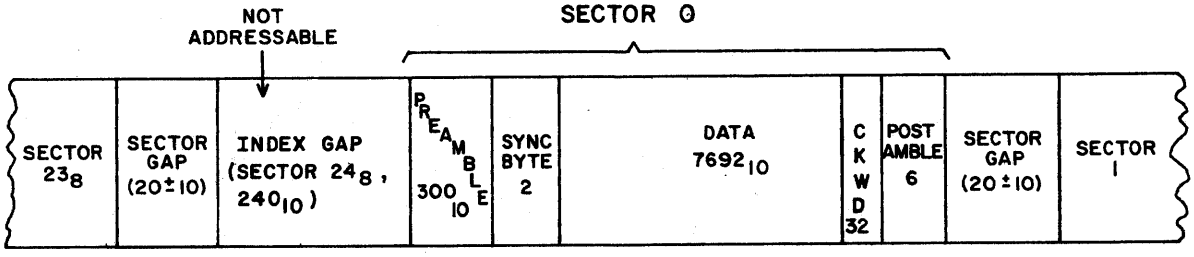


Figure 1-2. Track and Sector Format

† The 20 data sectors are designated and addressed as sectors 0 through 23_8. An additional sector, 24_8, is present at the end of the revolution. This short sector is not addressable. Head changes can occur at this time during full tracking.

DSU DATA TRACK FORMAT

The 40 recording heads are divided into ten groups of four each (figure 1-3). Each is dedicated to one of the bits in a 4-bit byte. Forty disk surfaces are used for data, one (in the middle of the pack) is the servo surface and three are not used (both sides of the top disks and the bottom disk).

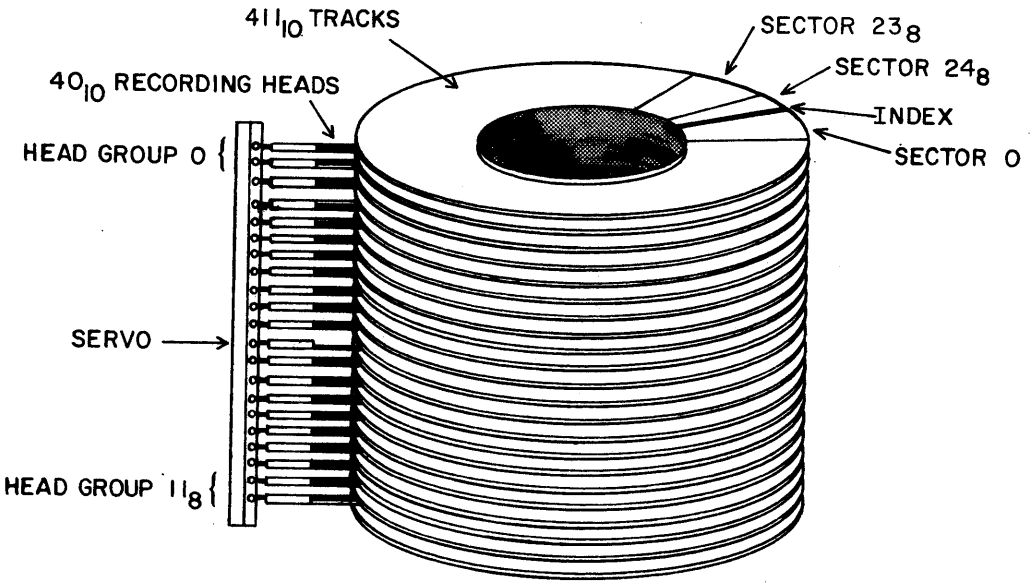


Figure 1-3. Pack Organization

DSU TIMING

The servo track on the DSU generates 13,440 pulses per revolution. Each servo pulse is 1240 (±125) nanoseconds wide. From each servo pulse, the DSU generates 12 clock pulses which are 103 (±5) nanoseconds wide. The controller uses the servo pulses to generate sector marks, and clock pulses to synchronize write data. Other related timing information is given below.

Disk speed	3600 rpm (± 2%)	Nominal data transfer rate is 9.677 MHz per head (38.7 MHz per four heads).
Average latency	8.33 milliseconds	
Maximum latency	17.00 milliseconds	
Head stabilization	5.0 microseconds	
Read initialization	20.0 microseconds	
Read to write recovery	1.0 microseconds	

OPERATION AND PROGRAMMING 2

CONTROLLER RESERVATION

A controller can be accessed by four PPUs on a one-at-a-time basis. The four accesses are divided into two sections: one section consists of two accesses for mainframe A; the other section consists of two accesses for mainframe B. If only two PPUs are attached to the controller, and both come from the same mainframe, one may be attached to an access on one section, and the other may be attached to an access on the other section.

A PPU reserves the controller by sending a function code. The reservation applies to the section and not to the specific PPU that sent the function. Therefore, in a four PPU configuration, if PPU Aa sent a function and reserved the controller, then PPU Ab would have equal access. PPUs Aa and Ab must coordinate their communications with the controller by using an external data channel. The reservation prevents the controller from responding to any function from the other section. PPUs Ba and Bb cannot communicate with the controller until the reservation is cleared.

Any PPU can master clear the controller and also clear the reservation. An output data record flag from any PPU master clears the controller. However, this does not clear the reserve. The reserve is cleared only when the controller receives an output control record flag within 1 microsecond of a data record flag. A reserved controller responds only to these two signals from a PPU on the unreserved access.

The reservation can also be cleared by a power on master clear and by pushing the MASTER CLEAR switch on chassis location A01.

UNIT SELECT AND UNIT RESERVE

Before the controller can communicate with a specific DSU, the DSU must be selected in the controller. Execution of any function in the controller selects the DSU designated in the unit number parameter of the function. The controller has only one DSU selected.

In addition to DSU selection in the controller, the DSU must be connected and reserved by the controller before it responds. A DSU can be attached to two controllers. If it is attached, either controller can attempt to reserve it. (Either controller access can, however, be disabled with the DISABLE CHAN 0 or DISABLE CHAN 1 switch in the back of the DSU.) An unreserved DSU becomes reserved by a controller whenever it receives a unit reserve and head select function. It remains reserved and connected until it receives a unit disconnect function from the reserving controller. (The reserve may also be cleared by toggling one of the DISABLE switches on the back of the DSU.) When a DSU is reserved by the other access, bit 5 (DSU busy) of the subsystem status word sets. When a DSU becomes connected and reserved, bit 5 (unit connected) of the head status word sets. The controller can reserve up to four DSUs at a time.

FUNCTION CODES

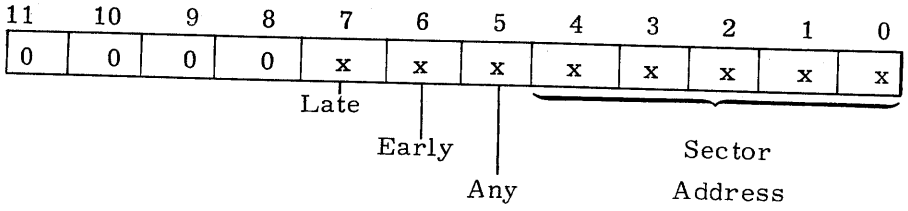
The controller responds to the following 12-bit function codes from the PPU. Function codes are sent on the output control channel and are accompanied by a control word flag. The controller responds with a control resume when the function has been executed. Table 2-1 lists all functions.

TABLE 2-1. FUNCTION CODES

	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	Late	Early	Any	← Sector →				
Read Serial	0	0	0	1	Channel		Any	← Sector →				
Write	0	0	1	-	-	Long	Last	← Sector →				
Unit Reserve and Head Select	0	1	0	0	Unit	Unit	-	-	← Head →			
Unit Disconnect	0	1	0	1	Unit	Unit	-	-	-	-	-	-
Unit Clear/ Return to Zero	0	1	1	0	-	-	-	-	-	-	-	R.T.Z.
Echo Check	**0**	**1**	**1**	**1**	**1PP**	-	-	-	-	-	-	-
Position Select	1	0	- †	← Cylinder Address →								
Margin Select	1	1	0	0	-	-	Direction	← Servo Offset →				
									Channel			
Error Correct	1	1	0	1	-	-	-	-	3	2	1	0
Status Select	1	1	1	0	Error Code Word		Controller	Interlock	Offset	Head	Cylinder	Unit Fault
DSU Status Enable	1	1	1	1	Unit	Unit	-	-	-	-	-	-

†Bit 9 is used in equipments with the double track density option installed.

READ



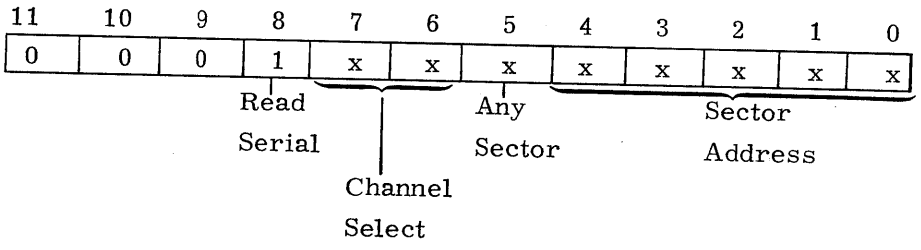
The PPU must issue a read function to read a sector of data. To read a stream of consecutive sectors, the PPU must send a read function within 30 microseconds of the last data word received from the preceding sector. If the function is not sent within the specified time, a lost revolution results but no controller errors occur.

A read function must have 0's in bits 8 through 11. Bits 0 through 4 contain the address of the sector to be read. Setting bit 5 of the function causes the DSU to ignore the sector address and to read the next sector that comes under the read heads.

Bits 6 and 7 are used for error recovery. Setting bit 6 of the function causes the read strobe of all four channels in a connected DSU to be shifted early. Setting bit 7 causes the read strobe to shift late. If both bits 6 and 7 are set, a fault condition results.

The maximum sector address is 23_8.

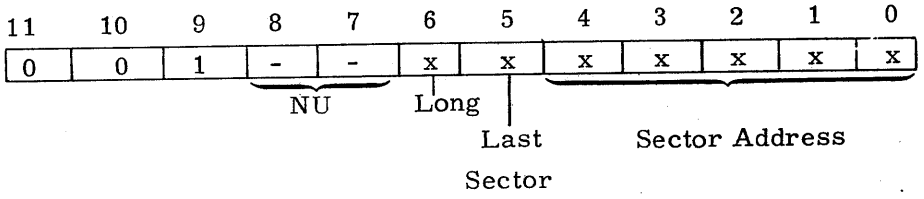
READ SERIAL



To read data serially from one channel of a connected DSU, the PPU sends a read serial function to the controller. Bits 9 through 11 are 0's and bit 8 is set. Bits 0 through 4 contain the sector address. If bit 5 is set, the DSU ignores the sector address and reads the next sector that comes under the read head. Bits 6 and 7 select the following channels.

Bit 7	Bit 6	Channel
0	0	0
0	1	1
1	0	2
1	1	3

WRITE

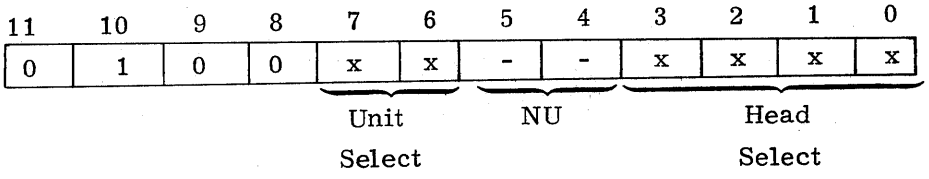


The PPU must issue a write function for each sector to be written. Bit 5 should be set when writing the last sector of a stream of sectors or when writing a single sector. If it is not set during these conditions, the data previously written on the sector following the current write data is destroyed. Data blocks are a fixed length. The controller must receive a write function and three data words within 36 microseconds of the last data word of the preceding sector.

A 1 in bit 6 indicates that a long write is to be performed. The data block continues until the end of the sector and creates a sector length error. This bit is to be used for diagnostic purposes in order to simulate checkword errors and check error correction.

In a write function bits 11 and 10 are 0's and bit 9 is a 1. Bits 0 through 4 contain the sector address. Sector addresses cannot exceed 23_8.

UNIT RESERVE AND HEAD SELECT



In this function, bits 8, 9, and 11 are clear and bit 10 is set. Bits 0 through 3 contain the head group address. Bits 6 and 7 contain the following unit number.

Bit 7	Bit 6	Unit Number
0	0	0
0	1	1
1	0	2
1	1	3

If a DSU is busy (that is, connected to a controller) when the unconnected controller executes the function, bit 5 of subsystem status is set and the function has no effect on the DSU.

The PPU must issue a unit reserve and head select function before any other operation can be performed on a DSU. When the controller executes this function, the PPU can receive the subsystem status of the selected DSU.

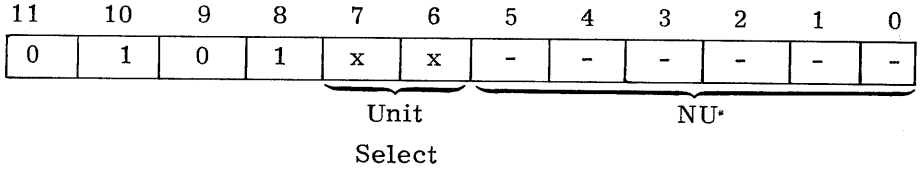
Because the DSU can be cabled to two controllers, the DSU has reservation logic in it. A successfully executed unit reserve and head select function reserves the DSU for a controller and sets busy status in the other access (indicating that the DSU is not available for the other controller).

Execution of the function accomplishes three things.

1. Reserves the DSU for the controller.
2. Selects the DSU in the controller, enabling a communication path between the controller and the reserved DSU.
3. Selects a head group in the selected DSU.

The controller can have all or none of the four DSUs reserved. It always has one and only one DSU selected.

UNIT DISCONNECT

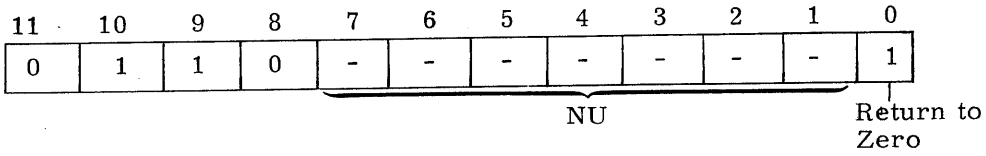


In this function, bits 8 and 10 are set and bits 9 and 11 are clear. Bits 6 and 7 contain the unit number.

This function clears the connect between the controller and the selected DSU by clearing the DSU reserve condition.

If the DSU is not reserved by this controller, the function has no effect on the DSU, but selects the DSU in the controller.

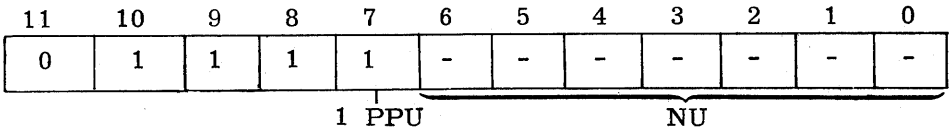
UNIT CLEAR/RETURN TO ZERO



In this function, bits 8 and 11 are clear and bits 9 and 10 are set. Execution of this function clears the fault register, except for bit 7 (seek error), in the DSU selected by the controller and clears the on cylinder interrupt for that DSU.

If bit 0 is set, the DSU moves its read/write heads to the outer edge of the disk surface (end of travel), then to position zero. This allows the DSU to reestablish a reference point for cylinder position and clears bit 7 (seek error) of the fault register. This function should only be issued during the time the DSU is on cylinder or a seek error status is present. A data channel record pulse should be issued when the return to zero seek is complete (unit on cylinder). This clears a possible controller error due to missing servo clock pulses at the end of travel area.

ECHO CHECK



This function is intended for maintenance and hardware error detection. Controllers can be exercised with this function by using either one or two PPUs. Bit 7 should be set if only one PPU is used. A DSU does not have to be connected to the controller to use this function.

Using one PPU, the procedure is to:

1. Issue the echo check function from the PPU.
2. Send five 12-bit words from the PPU to the controller.
3. Input 16 12-bit words from the controller to the PPU. This includes the five words sent (in step 2) from the PPU, plus the 11-word checkword generated by the controller.
4. Compare the input with the output in the PPU, and check the checkword polynomial for each of the four read channels. The polynomial is:

$$g(X) = X^{32} + X^{23} + X^{21} + X^{11} + X^{2} + 1$$

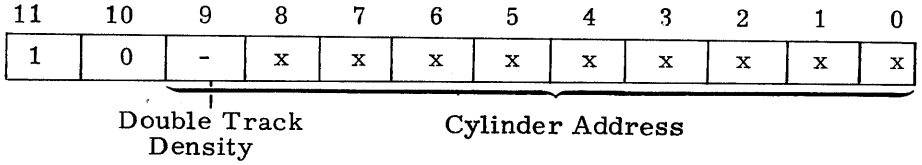
The function causes the controller to gate the five words through its data path in a loop and to generate a checkword on the data.

The procedure, using two PPUs, follows.

1. Issue the echo check function.
2. Do an output of one sector on the same PPU which issued the function. Do an input of one sector on the other PPU. The controller loops the data through its data path and generates the checkword.
3. Compare the output with the input, and check the checkword polynomial for each of the four read channels. The polynomial is the following.

$$g(X) = X^{32} + X^{23} + X^{21} + X^{11} + X^{2} + 1$$

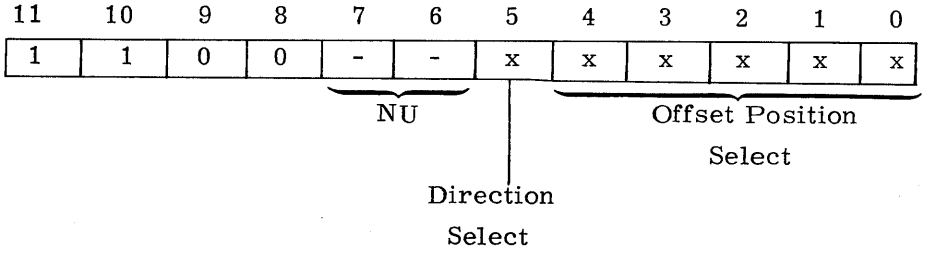
POSITION SELECT



In this function, bit 11 is set, bit 10 is clear, and bit 9 is used only in double track density equipment. Bits 0 through 8 contain the address of the position on the disk surface. If bit 9 is used, it is part of the cylinder address.

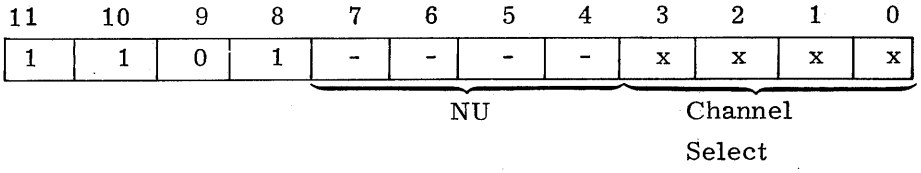
This function causes the DSU to move the read/write heads to the selected position on the surface of the disk. The not on cylinder bit in the subsystem status word sets during the move. The programmer must know that the proper DSU is selected in the controller.

MARGIN SELECT



Execution of this function causes the positioning arm to move to one of 31 positions determined by bits 0 through 5. If bit 5 is set, the arm moves in the forward direction. If bit 5 is clear, the arm moves in the backward direction. If bits 0 through 4 are clear, the arm moves to or remains in the nominal position. The 31 positions in each direction correspond to the binary equivalent of bits 0 to 4. Each position (in ascending order) is 0.00005 inch more offset from the nominal position. Any position select or a unit clear/return to zero resets the margins to the nominal position. The programmer must delay 10 milliseconds after issuing a margin select function before issuing a read function.

ERROR CORRECT

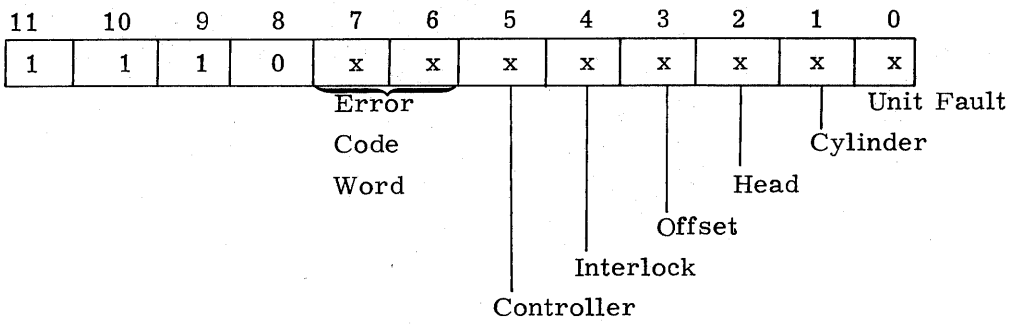


The PPU issues this function when the controller reports a read channel checkword error in bits 0 through 3 of the controller status response. The status response indicates which channel had an error. The function must select this channel in bits 0 through 3. Only one channel can be selected at a time. When the controller executes this function, it provides status responses (error code words 1, 2, and 3). These words contain information necessary to correct the error.

After the controller executes the function, the PPU must check error code word 1 to determine if the information is available and if the error can be corrected. If both these conditions are met, the PPU software can use the information provided in the error code words to correct the error.

The error correct function can correct single burst errors 11 bits long.

STATUS SELECT



Execution of this function gates one of seven types of status responses to the PPU control channel. The requested status response is specified in bits 0 through 7. Only one type of status can be requested each time the function is issued. If the function is issued with bits 0 through 7 all clear, an eighth type of status (subsystem status) is made available. The types of status are defined as follows (the type specified if the bit is set).

Bit 0 Contents of the DSU fault register
Bit 1 Contents of the DSU cylinder register
Bit 2 Contents of the DSU head register
Bit 3 Contents of the DSU difference register
Bit 4 Contents of the DSU interlock register
Bit 5 Controller status

Bit 6	Bit 7		
0	1	Error code word 1
1	0	Error code word 2
1	1	Error code word 3

DSU STATUS ENABLE

11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	x	x	-	-	-	-	-	-
				Unit		NU					

Execution of this function allows the PPU to check subsystem status on a DSU specified in bits 6 and 7 without reserving the DSU. This function selects the DSU in the controller. Contrast this with the unit reserve and head select function which selects the DSU in the controller and reserves the DSU.

STATUS RESPONSES

To check status, the PPU must reserve the controller. Subsystem status is available at any time the other seven status responses are not on the control channel. The PPU must issue a status select function to check any status response except subsystem status. (If the status select function is issued without specifying one of the other status words, subsystem status is enabled.) Table 2-2 lists all status responses.

TABLE 2-2. STATUS RESPONSES

	11	10	9	8	7	6	5	4	3	2	1	0
Subsystem (CDC CYBER)	Sub-system Busy	← Sector Count →					DSU Busy	Not Used	On Cylinder Inter-rupt	Not on Cylinder	Control Error	Not Ready
Unit Fault	-	-	-	← Refer to Text →								
Cylinder	-	-	-†	← Cylinder Address →								
Head	-	-	-	-	-	-††	Unit Connect-ed	-	← Head Address →			
Offset	-	-	-†	← Difference Register →								
Interlock	-	-	-	-	← Refer to Text →							
Controller	-	Unit	Unit	Index Error	Sync Error	Stream Error	Length Error	Skew Error Lost Data	← Read Channel Checkword Error →			
Error Code 1	-	-	-	-	-	-	Not correct-able	-	-	Correc-tion Infor-mation Avail-able	Parcel	Parcel
Error Code 2	← Correction Address →											
Error Code 3	-	← Correction Vector →										

†Bit 9 is used in equipments with the double track density option installed.
††Bit 6 is added in equipments with the double track density option installed. Bit 6 is a 1 if the connected DSU is a double track density unit.

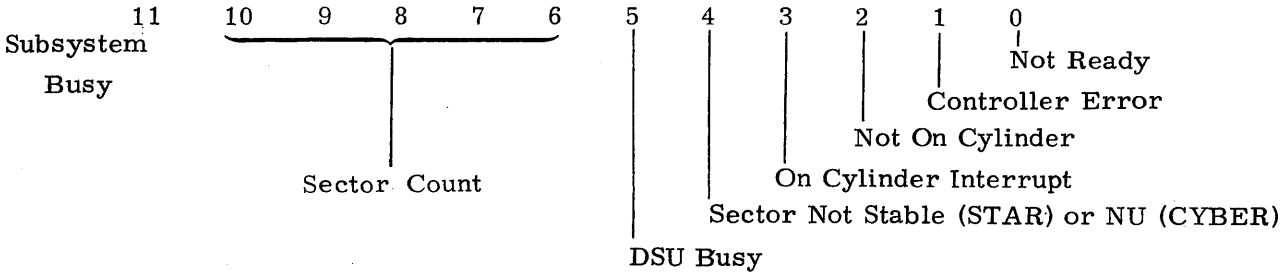
SUBSYSTEM STATUS

Subsystem status is always present on the input control channel unless a PPU on a mainframe which has reserved the controller has issued a status select function last. In this case, one of the other status responses is present on the input channel.

Bit 11 of subsystem status indicates that the subsystem is busy, that is, reserved by the other PPU. A reserved controller ignores all channel activity from a PPU on an unreserved access except control channel record pulse which clears the controller reservation, and data channel record pulse which clears everything else in the controller. A data record pulse must precede the control record pulse by a maximum of 1 microsecond to clear the reservation.

Subsystem status contains the ready status for the selected unit. If the selected unit is nonexistent, bit 0 (not ready) of subsystem status is set.

If a connect and head select is sent to a nonexistent unit (despite not ready status), the controller responds as though conditions were normal.



If bit 0 is set, it indicates that the selected DSU is not ready. The PPU must request unit fault or interlock status response to determine the reason the DSU is not ready.

If bit 1 is set, it indicates that the controller detected an error. The PPU must check the controller status response (by issuing the status select function with bit 5 set) to determine the specific error. A data channel record pulse clears this bit if the cause of the error has been corrected. This error bit lights the indicator.

If bit 2 is set, it indicates that the selected DSU is positioning its read/write heads.

If bit 3 is set, it indicates that the selected DSU has completed a seek operation and is on cylinder. The on cylinder interrupt can be cleared on an individual unit basis with a unit clear function, or for all four units with a data channel record pulse.

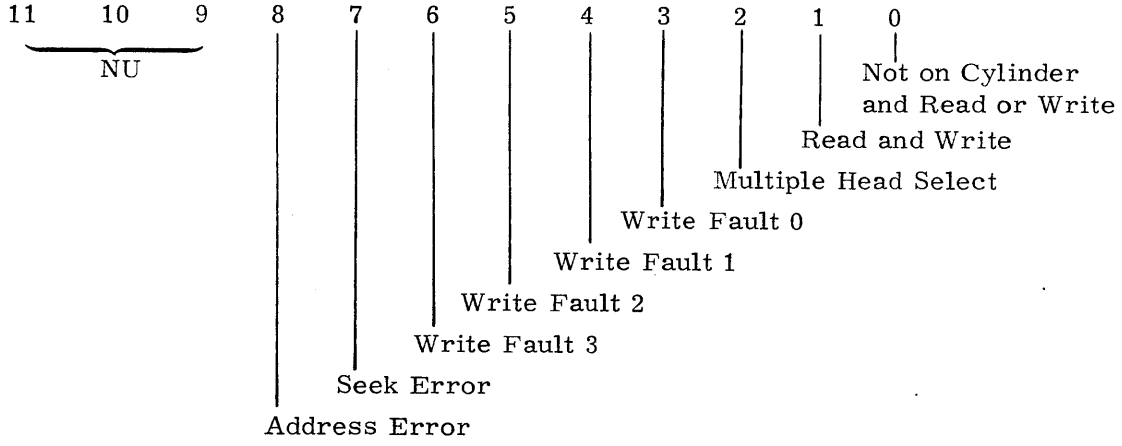
Bit 4 is not used in CYBER mode. If bit 4 is set in STAR mode, it indicates that the sector count changes within 90 microseconds.

If bit 5 is set, it indicates that the selected DSU is connected to a different controller.

Bits 6 through 10 contain the address of the sector currently under the read/write heads (for the selected DSU).

Bit 11 indicates that the controller has been reserved by a PPU on another controller access. The PPU, which does not have the reservation, gets no response if it attempts to communicate with the controller by issuing any function. If bit 11 is set, all other bits should be ignored.

UNIT FAULT



Bit 0 indicates that the DSU received a read or write signal from the controller when the DSU was positioning read/write heads.

Bit 1 indicates that the DSU received a write signal when the read gate was true.

Bit 2 indicates that more than four read/write heads have been selected for more than 7.5 microseconds.

Bits 3 through 6 indicate that one or more of the following fault conditions occurred on the indicated channel.

1. Incorrect output from the write driver.
2. The selected head is open or shorted.
3. Write gate enabled without write data.

NOTE

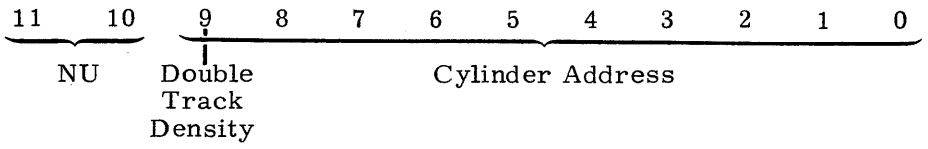
The fault must exist for 600 nanoseconds before the DSU detects it.

Bit 7 indicates that a seek error has occurred.

Bit 8 indicates that one or more of the following conditions occurred.

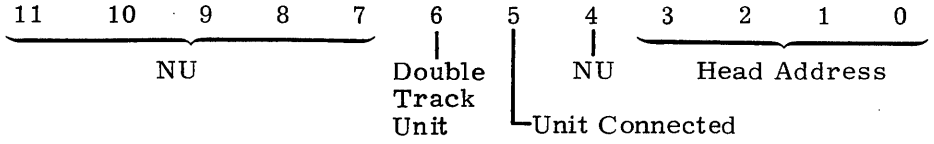
1. DSU received a cylinder address greater than 632_8 (1466_8 for double track density units).
2. DSU received a head address greater than 11_8.
3. DSU received a margin select signal or cylinder select when not on cylinder.

CYLINDER ADDRESS



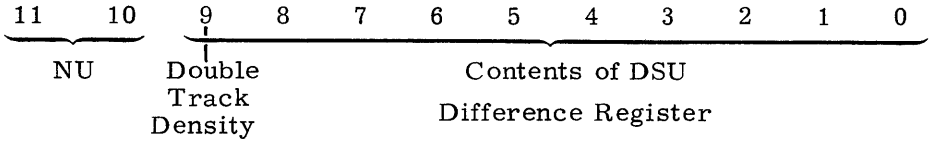
Bits 0 through 8 of this status response contain the contents of the selected DSU read cylinder register (bits 0 through 9 for double track density equipment). This address indicates the position of the read/write heads on the surface of the disk pack. Bit 0 is the least significant bit of the address.

HEAD ADDRESS



If the selected DSU is connected to the controller, bit 5 is set and this status response contains the head address in bits 0 through 3. If the selected DSU is not connected, the response is all zeros. Bit 6 is used in double track density equipment. Bit 6 is set if the connected DSU is a double track density unit.

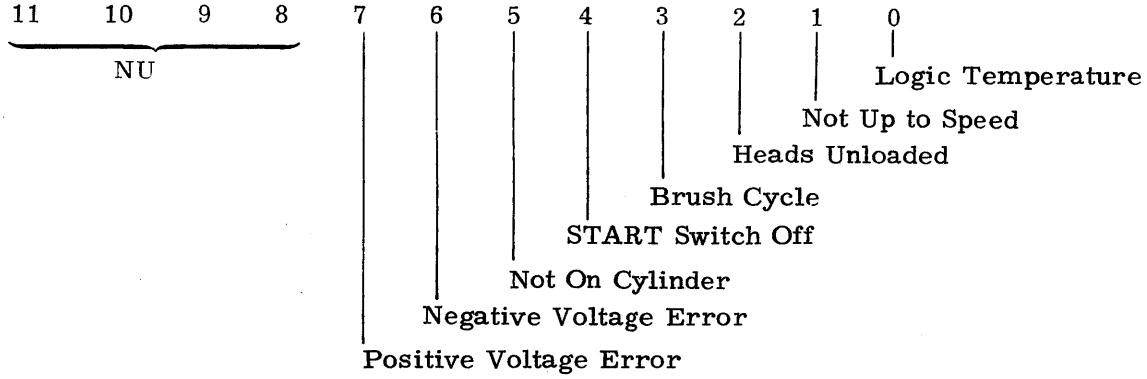
OFFSET



This status response contains the contents of the DSU difference register in bits 0 through 8 (bits 0 through 9 for double track density equipment). The PPU can interpret this information in two ways.

1. If the DSU is not on cylinder, the contents reflect the relative position of the read/write heads during a head positioning operation. During this operation, the difference register is incrementing the complement of the difference between the last and the next position. When the positioning is complete, the register contains 777_8 (1777_8 for double track density), and the head arms are on cylinder.
2. If the DSU executes a margin select function, bits 0 through 5 reflect the complement of the quantity placed in bits 0 through 5 of the margin select function.

INTERLOCK



This status response reflects an abnormal condition in the DSU. Setting any one of these bits causes the DSU to set bit 0 (not ready) of the subsystem status response. Each condition is defined at a 1 (true) level.

Bit 0 indicates that the temperature in the logic chassis is above normal.

Bit 1 indicates that the DSU is not up to speed.

Bit 2 indicates that the heads are not loaded on the disk pack.

Bit 3 indicates that the DSU brush cycle is in progress.

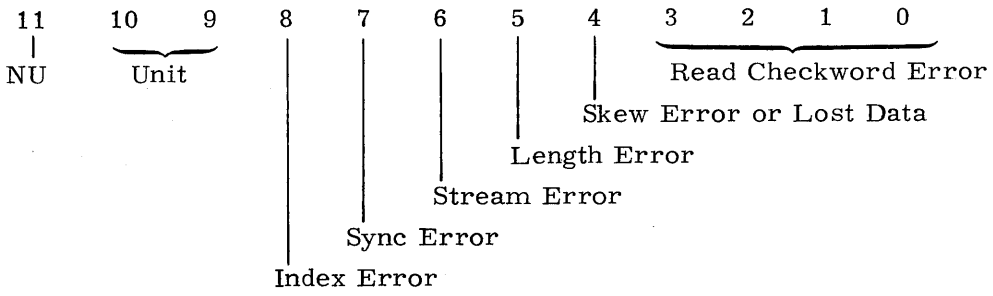
Bit 4 indicates that the DSU START switch is off.

Bit 5 indicates that the DSU is positioning its read/write heads.

Bit 6 indicates that the DSU negative voltages are in a below normal condition.

Bit 7 indicates that the DSU positive voltages are in a below normal condition.

CONTROLLER



This response reflects error(s) in the selected DSU or in the controller. The errors are defined at a 1 (true) level. Setting any one of these bits causes bit 1 (controller error) of the subsystem status word to set.

Bits 0 through 3 indicate that the controller detected a read channel checkword error in channels 0, 1, 2, or 3, respectively.

Bit 4 indicates lost data due to more skew than the controller can tolerate during a read. It also indicates a lost data condition during a write.

Bit 5 indicates an attempt to read or write data during a sector mark. It usually indicates that the controller stopped during a read or write function.

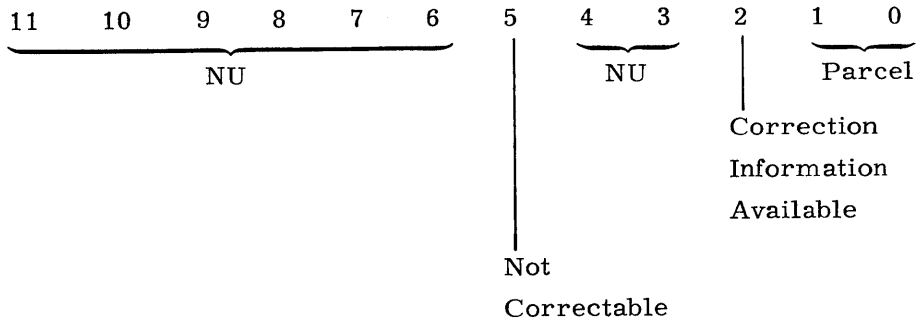
Bit 6 indicates that the controller did not receive three words of data within 30 microseconds after responding to a write function or did not receive a write function and three words of data within 36 microseconds of the last data word in the previous sector when writing consecutive sectors. This bit sets if the last write function does not have bit 5 set (write terminate).

Bit 7 indicates that the controller did not detect a sync byte when it should have.

Bit 8 indicates an extra or missing index mark or servo clock pulse.

Bits 9 and 10 contain the binary code number of the DSU selected in the controller.

ERROR CODE 1



If the controller detects a read channel checkword error, the PPU can attempt to correct the error using error code words 1, 2, and 3, which are generated as the result of an error correction function. Code word 1 bits are defined for a 1 (true) level.

Bits 0 and 1 form a binary code which indicates on which of three bits of a data buffer word to start implementing the correction vector. The parcel code, channel, and word/bit relationship is as follows.

	Parcel Code		
Channel	10	01	00
0	2^0	2^1	2^2
1	2^3	2^4	2^5
2	2^6	2^7	2^8
3	2^9	2^{10}	2^{11}

Bit 2 indicates that error code word 1, 2, and 3 are available (that is, may be used to do the error correction). The controller takes 4.4 milliseconds (maximum) to process the error correction algorithm following an error correction function.

Bit 5 indicates that the error cannot be corrected. (Error code words 2 and 3 are invalid.)

ERROR CODE 2

11	10	9	8	7	6	5	4	3	2	1	0
Correction Address											

The correction address is the displacement from the end of sector of the incorrect word.

ERROR CODE 3

11	10	9	8	7	6	5	4	3	2	1	0
NU	Correction Vector										

This response contains the correction vector. The PPU performs an exclusive OR with the vector and the data to be corrected. The first bit of data to be corrected is indicated by the channel bit parcel and correction address. The PPU must perform an exclusive OR with this bit and bit 10 of error code word 3. An exclusive OR is performed on the remaining nine bits in memory with those in the vector. The correction vector is 11 bits long and is applied to four or five data words, depending on the parcel count.

The word assembly/disassembly format follows (the most significant bit and byte are written on the pack first).

	11	10	9	8	7	6	5	4	3	2	1	0
Channel	3			2			1			0		

ERROR RECOVERY AND CORRECTION

DATA RECOVERY

The following techniques are available to recover data lost due to subsystem errors and/or to correct the error.

- If the controller detects a unit fault, the PPU can attempt to clear this condition by sending a unit clear function to the faulty DSU.
- If the software detects a position error, the PPU must send a unit clear and return to zero function before repositioning. It must do this to reestablish the reference point for positioning because positioning is done relatively and not absolutely.
- To recover misaligned data, the margin select function causes the positioner to move forward or backward from the nominal position.
- To recover data with poor clock-data synchronization, bit 6 and 7 of a read function can be coded to cause the read strobe of all four channels in a connected unit to be shifted early or late. If both bits 6 and 7 are set, a drive fault results.

DATA RECONSTRUCTION

After a head change in the device, data must first be reconstructed if it is to be used in the PPU. If data cannot be recovered normally, then this may be accomplished by using the read serial function to read data on each of the four read channels and assemble the four data blocks on a bit basis to form a record.

Checkword errors may be ignored on read channels that are not being read during one of the four reads. Error or offset recovery may be used if there is a checkword error on the channel being read.

During a read serial operation, data from one channel is read by the controller. These bits are arranged in 3-bit groups sequentially through the entire sector. Each 3-bit group (for example, 0, 1, 2 for channel 0) is assembled in the controller in its normal position of a 12-bit word and sent to the PPU. The PPU must ignore the other nine bits on the channel.

The PPU must read a sector of data from each channel and assemble the three bits into the original 12-bit bytes.

After the record is formed, it should not be rewritten on that sector until the previous and following sector have also been formed.

CHECKWORD ERROR CORRECTION

Following a PPU read operation, the PPU must delay 3.2 microseconds and check subsystem status to determine if a controller error occurred (bit 1 set). If an error occurred, the PPU must check controller status to determine which type of error occurred. If a read channel check word error occurred, bit 0, 1, 2, or 3 of controller status sets indicating which of four DSU channels contained the error.

The PPU can then attempt to correct the error by issuing an error correction function, designating the channel to be corrected in the function. It takes a maximum of 4.4 milliseconds from the time the controller executes the function until the controller has generated information for error code words 1, 2, and 3. The PPU can loop on error code word 1, checking bit 2. When this bit is set, the controller hardware has completed generating the information for the error correction. If bit 5 of EC 1 is set, the error cannot be corrected (with this procedure) and the PPU should discontinue the error correction operation.

If bit 5 is not set and bit 2 is set (of EC 1), the PPU should also read status error code words 2 and 3. The PPU uses the information in these words to correct the error in memory (the error is not corrected on the disk). Errors from 1 bit to a burst of 11 bits can be corrected on a single channel. If more than one channel has an error, each channel must be corrected separately. A data record flag destroys the data residue needed to do error correction so it should not be issued until error correction has been tried on all channels to be corrected. If more than two channels have errors, error correction is not the most efficient method of recovering data. In this case reread the sector to recover data.

The PPU reads data in 12-bit bytes from four DSU channels (three bits per channel). Since error correction is executed on only one channel at a time, only three bits of a 12-bit byte is subject to the correction vector. The PPU must use the parcel code (bits 0 and 1 of error code 1) to determine on which of the three bits to begin applying the correction vector. The parcel code, channel, and word-bit relationship are as follows.

	Channel 3			Channel 2			Channel 1			Channel 0		
Word bits	11	10	9	8	7	6	5	4	3	2	1	0
Parcel	0	1	2	0	1	2	0	1	2	0	1	2

To determine the byte address at which to start applying the correction vector, the PPU must subtract the correction address (EC2) from the sector length. For example, if the data sector length is 5300_8 and EC2 were equal to 2000_8, the result of the subtraction would be 3300_8. This indicates the displacement from the first word of the sector. (It may be a negative number.) The result 3300_8 is added to the address of the first word in the sector. If this were 1000, the vector (EC3) would be applied beginning at location 4300_8.

To apply the correction vector, 11 bits, beginning with bit 2^{10}, are exclusive ORed with 11 consecutive bits in memory associated with the selected DSU channel. If channel 0 were selected and the parcel count were 0, bit 2^{10} of the correction vector would be applied at location 4300_8, beginning with bit 2^2. Bit 2^0 of the correction vector would be applied at bit 2^1 of word 4303_8.

Example 1:

Last bit of a sector (on a specified channel) is incorrect.

Channel 0 is selected (bit 0 of controller status word is set)

Error code word 1 = 000 000 000 101 (parcel count 01)

Error code word 2 = 000 000 000 100 (address displacement)

Error code word 3 = -00 000 000 001 (vector)

Starting sector address = 1000_8

Sector length = 5300_8

1. PPU subtracts EC2 from sector length.

$$\begin{array}{r} 5300_8 \\ -\quad 4 \\ \hline 5274_8 \end{array}$$

2. Add starting address to the result.

$$\begin{array}{r} 5274_8 \\ +1000_8 \\ \hline 6274_8 \end{array}$$

3. Apply vector to the 11 successive bits from channel 0, starting with bit 2^1 at memory location 6274_8.

Address	Channel 3	2	1	0	Vector		
6274	2^{11}	2^8	2^5	2^2			
	2^{10}	2^7	2^4	2^1	0	Bit 2^{10}	Parcel code 01
	2^9	2^6	2^3	2^0	0		indicates that bit 2^{10}
6275				2^2	0		of the vector be applied
				2^1	0		at data bit 2^1.
				2^0	0		
6276				2^2	0		
				2^1	0		
				2^0	0		
6277				2^2	0		
				2^1	0		
				2^0	1	Bit 2^0	

The PPU performs an exclusive OR with the 11 vector bits and 11 data bits to correct the error.

Example 2:

First bit of a sector (on a specified channel) is incorrect.

Channel 1 selected (bit 1 of controller status word is set)

Error code word 1 = 000 000 000 110

Error code word 2 = 101 011 000 100

Error code word 3 = -00 000 000 001

Starting address = 1000_8

Sector length = 5300_8

1. PPU subtracts EC2 from sector length.

$$\begin{array}{r} 5300_8 \\ -5304 \\ \hline -\quad 4 \end{array}$$

2. Add starting address to the result.

$$\begin{array}{r} -4 \\ +1000_8 \\ \hline 774_8 \end{array}$$

3. Apply vector to the 10 successive bits from channel 1, starting with bit 2^3 at location 774_8.

NOTE

The address in this example is out of the boundaries of the data sector to be corrected. In this example, the error can still be corrected as follows. However, in some rare cases, the address of the error is completely out of the boundary and the error correction is not possible.

Address	Channel 3	2	1	0	Vector	
774	2^{11}	2^8	2^5	2^2		
	2^{10}	2^7	2^4	2^1		
	2^9	2^6	2^3	2^0	0	Bit 2^{10}
775			2^5		0	
			2^4		0	
			2^3		0	
776			2^5		0	
			2^4		0	
			2^3		0	
777			2^5		0	
			2^4		0	
			2^3		0	
1000			2^5		1	Bit 2^0

PROGRAMMING CONSIDERATIONS

1. Because the controller has four accesses (Aa, Ab, Ba, and Bb) to allow accessing by two mainframes, the controller contains reservation logic. A function from one mainframe reserves the controller for that mainframe.

   The reservation is cleared by the following.

   - Power on master clear
   - Maintenance panel MASTER CLEAR switch (chassis location A01).
   - Data record flag followed within 1 microsecond by a control record flag from any PPU.

   NOTE

   A data record flag by itself from any PPU master clears the controller regardless of reservation but does not clear the reservation.

2. Because each DSU has two accesses to allow accessing by two controllers, each DSU contains reservation logic. A DSU is reserved when a controller issues a reserve and head select function provided that accessing by that controller is not locked out by a switch on the DSU. The reservation is cleared by the following.

   - A disconnect function issued by the controller to which the DSU is reserved
   - Toggling LOCKOUT CHAN 0 or LOCKOUT CHAN 1 switch on the DSU

   NOTE

   Clearing of the controller PPU access reservation does not clear any DSU reservations to the controller.

3. After a power-up sequence or system deadstart, the controller should be cleared with a data record flag.

4. A data record flag clears a channel that is stopped waiting for a data or control word flag. It also causes the error correction status to be set to the following values.

   EC1 = 0002
   EC2 = 7777
   EC3 = 0000

5. The subsystem requires fixed length sectors for normal operation. If the number of the data bytes written on a sector is incorrect, a lost data error occurs. Correct sector length is 2564_{10} 12-bit words.

6. During every read operation, the controller issues extra input data word flags to allow the PPU to read the checkwords (this is primarily for diagnostic purposes). Therefore, before issuing a read function, the PPU must sense and clear any input data word flags from a preceding read operation. A one-word input on the data channel should accomplish this. In addition, a program delay of 3.2 microseconds is required after each read operation to allow time for a valid checkword status to be generated in the controller.

7. Any of the following causes indeterminate hardware conditions (may disable the PPU channel).

   - Reading or writing at a sector address larger than 23_8
   - Attempting to read, write, or position a unit that is not connected (The controller does not send a control resume to the PPU in this case)

8. The margin function can be used to recover data from marginally bad areas of the disk surface. It can also be used to identify these areas more quickly during bad spot mapping. The margin function must be executed after each change of position. Each time the margin function is issued, the PPU must delay for 10 milliseconds to allow time for the positioner to move. The positioner is returned to the nominal position by the following.

   - Return-to-zero function
   - Margin function to nominal

   The position function also returns the head to the nominal position. However, the position function should not be used to return the head to nominal because an error in the cylinder address can occur (occassionally, not always) if the position function is executed when the heads are offset.

   The margin function can be used in conjunction with read strobe shifts to enhance data recoverability. A minimum of three read operations should be attempted at each offset selected before moving to another offset. If data cannot be recovered at any offset, the positioner should be returned to nominal offset and the data recovery† aborted.

† Suggested order of offsets to be tried for data recovery (octal): -37, +37, -20, +20, -10, +10, -4, +4, -2, +2.

9. A single PPU can read and write data on alternate sectors of a DSU, reserving it for exclusive use. However, a second method can be used to transfer large blocks of data at a faster speed: two PPUs can transfer data to a DSU if one PPU transfers data to even numbered sectors and the other PPU transfers data to odd numbered sectors. This method doubles the transfer rate.

10. The controller contains no hardware to verify head positions; the verification must be done by the PPU. The position, head, and sector addresses are to be written in the first part of the data field of every sector by the PPU. Position verification is accomplished by reading the first four bytes of any sector with a read any sector operation. A comparison of the actual and requested position and head addresses is then made by the PPU. A checksum word for the address field (one 12-bit byte) can be generated and checked by the PPU on an output/input operation. The time cost for verification during a write operation (position, read first sector, compare address, output to requested sector) is one sector (800 microseconds). To verify the address, the programmer can read only the address portion of the sector. Verification takes no additional time during a read operation since the address information is contained in the data field.

    The address format follows.

Word 0	SINGLE DENSITY	
	BITS 8-0	POSITION
	BITS 11-9	UNIT NUMBER
	DOUBLE DENSITY	
	BITS 9-0	POSITION
	BITS 11-10	UNIT NUMBER
Word 1	BITS 5-0	SECTOR
	BITS 9-6	HEAD GROUP
Word 2	BITS 11-0	ZERO
Word 3	BITS 11-0	CHECKSUM RESULTING FROM SUBTRACTING THE CONTENTS OF WORDS 0 AND 1 FROM WORD 2

OPERATION

The subsystem requires little operator intervention during execution. The operator should be aware of the following switches and indicators.

CONTROLLER INDICATORS AND SWITCHES

POWER ON	This indicator lights when the controller has power applied to it. The indicator is located on the top, right, front of the cabinet.
Mini-Maintenance Indicators and Switches	These switches/indicators are located inside the controller cabinet on the printed circuit board at chassis location A01.
ERR/MC	This switch, when pushed, master clears the controller including the PPU access reservation. When the indicator lights, it indicates that a controller error (bit 1 of subsystem status) has been detected.
CYBER/STAR	This switch must be in the CYBER position.
A RESERVED	This indicator lights when the PPU attached to controller access Aa or Ab has reserved the controller.
B RESERVED	This indicator lights when the PPU attached to controller access Ba or Bb has reserved the controller.
UNIT BIT 0/UNIT 1	These two indicators form a binary code which indicates which DSU is selected in the controller.

DSU INDICATORS AND SWITCHES

The DSU has six switches/indicators on the top of the unit.

START	Push this alternate action switch to start the spindle rotating and to load heads, or to stop the spindle rotation and unload the heads. The indicator lights when the switch is in the START position.
READY	This indicator lights when the DSU is ready for operation.
FAULT	This indicator lights when the DSU detects a unit fault.
MAINTENANCE	This indicator lights when the DSU is in maintenance mode (off line).
TEMP	This indicator lights when the temperature exceeds a level safe for operation.
1/0	The 1 lights when the DSU is reserved by the controller on access 1. The 0 lights when the DSU is reserved by the controller on access 0.

In addition to these switches and indicators, the operator should be aware of the following toggle switches located on the lower right inside of the rear door.

LOCKOUT CHAN 0	When in the up position, this switch disables the controller/DSU interface designated 0.
LOCKOUT CHAN 1	When in the up position, this switch disables the controller/DSU interface designated 1. By toggling these switches the controller/DSU reservation can be cleared.

819 MEDIA FLAW DOCUMENTATION A

This appendix contains information on disk flaw documentation. It includes examples and explanations of each of the two types of documentation which accompanies disk packs: the Flaw Strip and the Media Flaw Map.

Each of the two types of documentation list areas on the disk pack that should not be used. This flaw information must be added to the diagnostic flaw table. To do this, the flaw information must be properly interpreted. Typical format of each type of documentation and the meaning of each is explained below.

819 FLAW STRIP CONVERSION

Flaw Strip Entry (in decimal)	Diagnostic Flaw Table Entry
N	
C REC 018	22_8
N	
REC 222	Not Used
HD 14	3_8
TRK 083	123_8

N — This indicates a noise error. An R in this position indicates a ratio error.

C REC — This is the number (0-19) of the sector that contains a bad spot. This decimal number must be converted to octal ($0-23_8$) before being entered into the diagnostic.

N — Same as above.

REC — This entry does not pertain to units on a CDC CYBER system.

HD — This entry is the decimal listing (0-39) of the actual surface containing the flaw. Because the controller reads and writes with four heads in parallel, the diagnostic requires inputs of head

groups 00-11, octal. To convert the HD number to head group, divide by 4 and convert the quotient to octal. This number is the head group. The remainder of this divide operation indicates which head group will be affected by the flaw. The head number is necessary to correlate flaws to errors on the subsystem but is not necessary for diagnostic input.

TRK — This entry is the decimal listing of the cylinder or track of the flaw. This number must be converted to octal before entering it in the diagnostic flaw table. Octal limits are $0\text{-}632_8$ single density, and $0\text{-}14466_8$ double density.

MEDIA FLAW MAP CONVERSION

PACK S/N - 400172
DATE - 111178
MEDIA FLAW MAP

				SECTOR MODES		
CYL	HDGR	CHAN	DIFF	(16)	(18)	(20)
octal	octal	octal	octal	hex	hex	octal
1466						
0037	07	2	03	0C	0E	20
0040	02	2	01	04	05	06
0043	02	2	37	04	05	06
0073	05	2	03	08	09	12
0105	10	3	14	02	02	02
0117	05	2	01	0A	0B	14
0154	05	2	01	0C	0D	17
0255	07	1	04	09	0A	13
0353	03	0	01	08	09	12
0366	05	2	25	01	02	02
0503	00	0	02	00	00	01
0534	01	3	14	02	02	02
0605	02	3	20	06	07	10
0627	05	1	37	04	04	05
0632	06	3	32	04	04	05
0712	03	3	25	02	02	02
0772	10	3	01	00	00	00
1035	00	3	01	02	02	02

TEST END

CYL	This entry is the octal listing of the cylinder or track of the flaw and is to be entered into the flaw table. At the top of the flaw map, the 1466 indicates that there are 1466_8 or 822_{10} cylinders to the disk pack.
HDGR	This entry is an octal listing of the headgroup affected by the flaw, and is to be entered into the flaw table. The headgroups are numbered 00-11 octal. For CDC CYBER 200 series systems, this value must be converted to hexadecimal.
CHAN	This entry indicates which head within the headgroup is detecting the flaw. Combined with the HDGR entry, the flaw is isolated to one of the 40 recording surfaces of the faulting cylinder.
DIFF	This entry is an octal quantity indicating the number of bad bits contained in the flaw.
SECTOR MODES	These entries list the sector of the cylinder which contains the bad spot. Sector mode 20 is listed in octal and is used on SCOPE, NOS, and NOS/BE operating systems. Sector modes 16 and 18 are listed in hexadecimal for CDC CYBER 200 series systems. The appropriate sector is also entered into the flaw table.

As an example, using the given Media Flaw Map, the flaw table entry on a CDC CYBER 170 series system would be:

Sector:	20_8
Headgroup:	07_8
Cylinder:	37_8
Unit:	X

For a CDC CYBER 200 series system formatted in 16 sectors, the flaw table entry would be:

Sector:	$0C_{16}$
Headgroup:	07_{16}
Cylinder:	$1F_{16}$

COMMENT SHEET

MANUAL TITLE CDC 7639-1/21, 7639-2/22, and Standard Option 10339-1/
10424-1 Mass Storage Controllers Hardware Reference Manual

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