Printed Circuit Manual

VOLUME 2

CONTROL DATA

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or use Comment Sheet in back of this manual.

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Record of Revisions

REVISION	NOTES
A	Corrections
B	1604 Inverter Ground Rules and Hammer Storage Card
	91 pages added.
C	Long Line Driver and Receiver Cards CA98 and HA26
	pages added.
D	Corrections to card type C64 and C65.
E	Add index tabs, chapter headings, new Table of Contents
	addition to Appendix, type "E" and 1604 cards; and
	Delay Card P13A.
F	Replace the following pages: 3-HA18-1 and 2; 4-C62 and
	C-61-5 and 6; Appendix pages 5 thru 10. Add pages 4-60,
	60A, 62 and 67-1 thru 3; 4-79A-1, 5-97-1 and 2, 5-E10-1.
	Replace page 4-E12-1.
G	6600 Info and Circuit Module Schematics added as Vol. 3.
H	Vol. 1, addition of revised Record of Rev. Vol. 2 add.
	of Record of Rev. Replace the following revised pages;
	Chapter 4 contents page, 4-C62 and C61-1, 4-C62 and
	C61-2, 4-C62 and C61-3, 4-C62 and C61-5, 4-C62 and
	C61-6, 4-C62 and C61-7, 4-P14A & P16A-3, 5-C94-3.
J	Vol. 1, page 2-3600 Inv-3 revised. Vol. 2, Chapter 5,
	second page of contents revised, removed pages 5-PED-1
	thru 5-PED-22. Chapter 6 added and Appendix 1, pages
	16, 17 and 18 removed and new pages added.
K	Publications Change Order 11170. Record of Rev. for
	Vol's. 1 and 2 revised. Removed pages 15 thru 31 of vol.
	2, Appendix 1 and replaced with revised pages.
L	Change Orders 10344 and 10708. Pages v, vi, vii, viii of
(10-5-65)	volume 1 revised. Chapter 4 contents page, 4-HA19-3,
	4-HA37 & HA43-10, 4-P14C & P16A-1, 4-P14C & P16A-2,
	4-P14C & P16A-3, chapter 5 contents pages, 5-C84-1,
	5-C84-2, 5-C84-3 (new page), 3, 4, 7 & 8 (appendix)

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Record of Revisions

REVISION	NOTES
L (Cont'd)	revised. Pages 5-C60-1, 5-C60-2, 5-C60-3, 5-C97-1,
(10-5-65)	5-C97-2, and 5-C97-3 added. Pages 5-HA27 & 5-HA28-1
	and 5-HA27 & 5-HA28-2 revised.
M	Change Order 12131. Appendix 1: pages 16 through 31
(12-13-65)	revised and pages 32 through 47 added.
N	Publication Change Order 12940. New Peripheral
(5-13-66)	Equipment cards added to Chapter 6: ADH, ITA/ITB/ITC,
	ITD, IYA, OJB, OYA and UJB. Revised text for page:
	6-OHA-1. Revised schematic for page 6-IAA, IAB-2.
	Appendix 1 revised. This revision obsoletes all editions
	of Pin Assignments - 1604 & 3600 - Printed Circuit
	Cards, Pub. No. 60106200, which is now included in
	this revision.
P	Publication Change Order 13632. Pages 6-ISC-1 of
(5-13-66)	chapter 6 is revised. The following new cards are
	added to chapter 6: ALA, AMF, AMG, AMH, AMI,
	ANB, ANC, AND, AUA, EUA, EUC, EVB, FCA, FCB,
	FDA, FGA, FHA, FIA, FJA, FKA, FLA, FLB, FMA,
	FNA, FPA, FRA, FSA, FTA, FUA, FVA, FWA, FYA,
	JBA, JCA, JDA, and OTA.
R	Publications Change Order 15800. The following new
(2-13-67)	cards added to Chapter 6: AIB, AKA, AOA, ATA, ATB,
	AVA, AYA, BAA, BAB, BBA, BCA, EEG, EEH, EWA,
	EWB, EZA, FAB, FOA, FOB, FRB, FRC, FRD, FSB,
	FUB, FWB, FXB, GAA, GBA, GCA, GCB, GCC, GCD,
	IOB, IOC, IOD, JEB, JEC, ONA, OUA, OVA, UEA,
	UHB, UIA, UJC, UKA, and UKB.

CHAPTER 4. I/O CARDS

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Modified L--- Output	C76, C76A
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Line Receiver	E13
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OUTPUT CARDS (L)

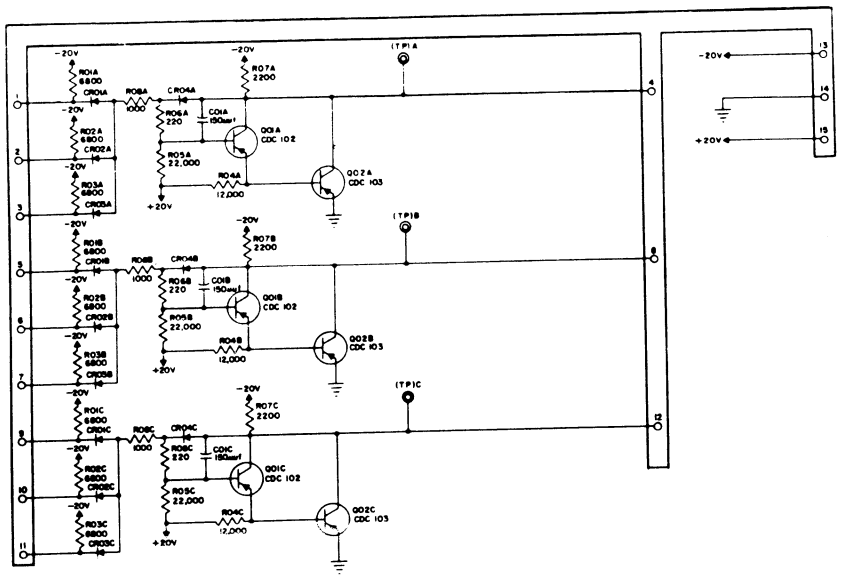
Card Types 60, 60A, 62 and 67

The circuits contained on these cards adapt the relatively low level 1604 logic voltages to the relatively high level voltages necessary for transmission over a 1604-type I/O cable. Each card contains three separate circuits designated A, B, and C.

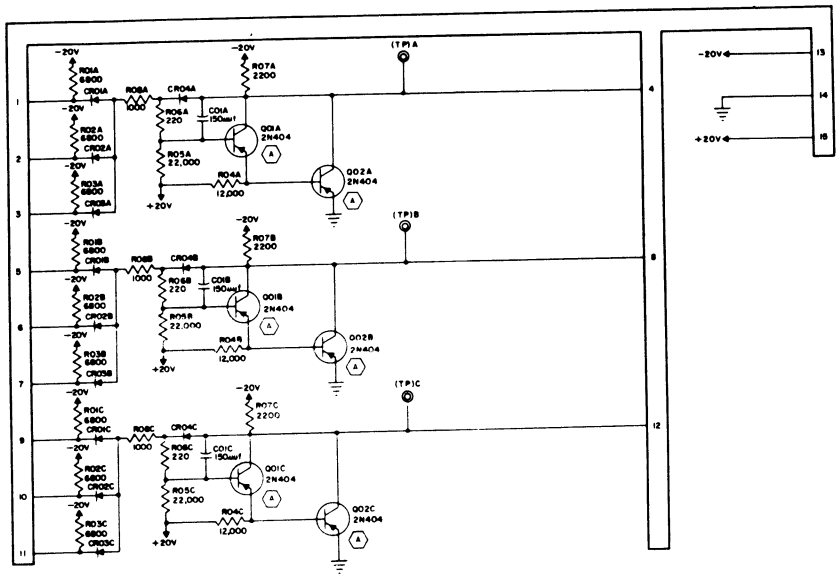
These circuits are similar to 1604-type inverters, in that they contain a common emitter transistor circuit producing a 180^{o} electrical phase shift

The switching speed of the circuit is limited by the 150 uuf of Miller feedback capacitance, and the feedback network allows a -0.5v "0" input to drive the circuit to cutoff. Input and output levels are as follows:

Input	Output
-3v "1"	-0.5v
-0.5v "0"	-18v



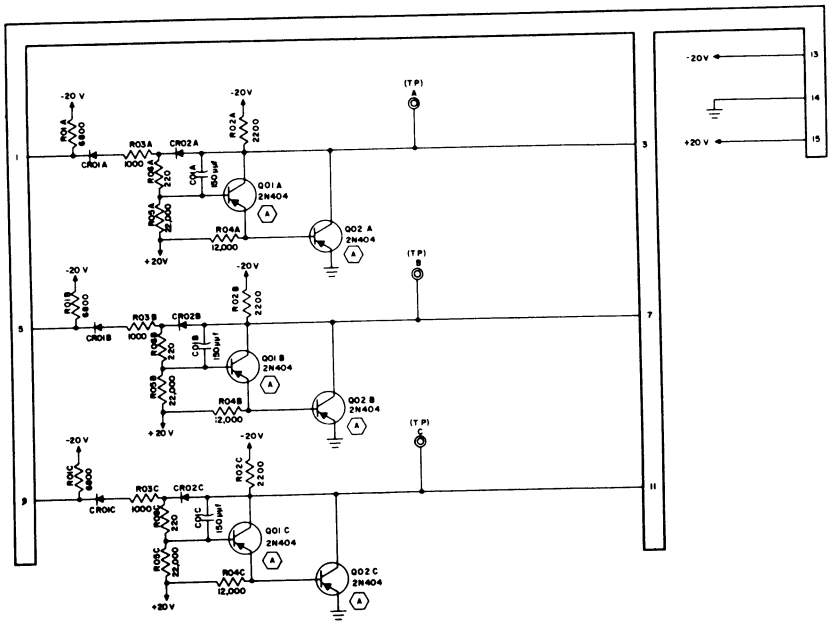
Output 60



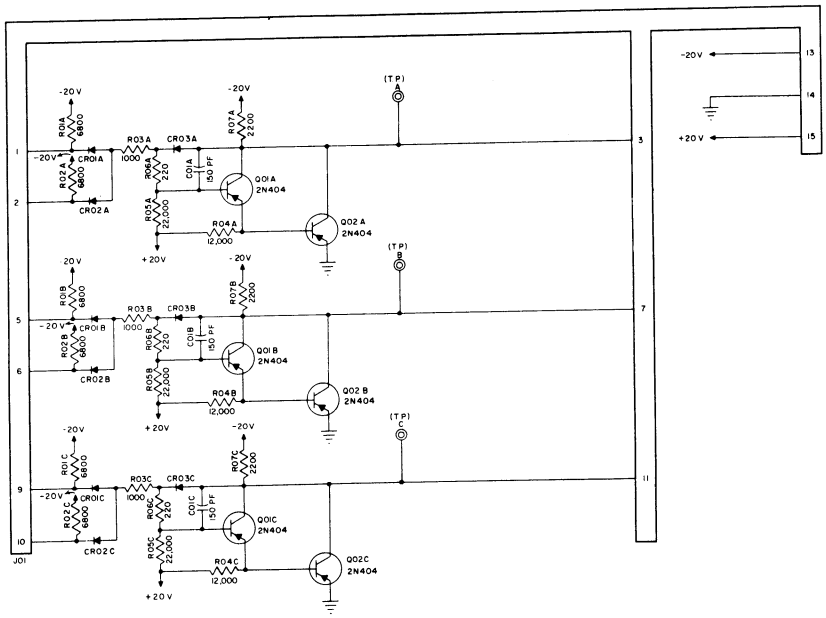
Output 60A

4-60, 60A, 62, & 67-2

Rev. F



Output 62



Output 67

INPUT CARDS (M)

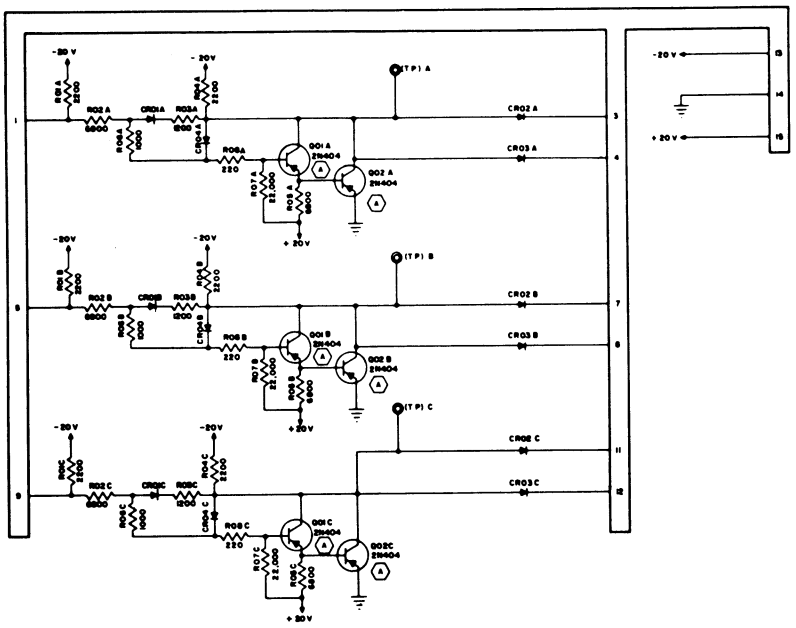
Card Types 61 and 87

The circuits contained on these cards adapt relatively high line voltage used for 1604-type cable transmission to the relatively low-level voltage used for logical functions. Each card contains three separate circuits designated A, B, and C.

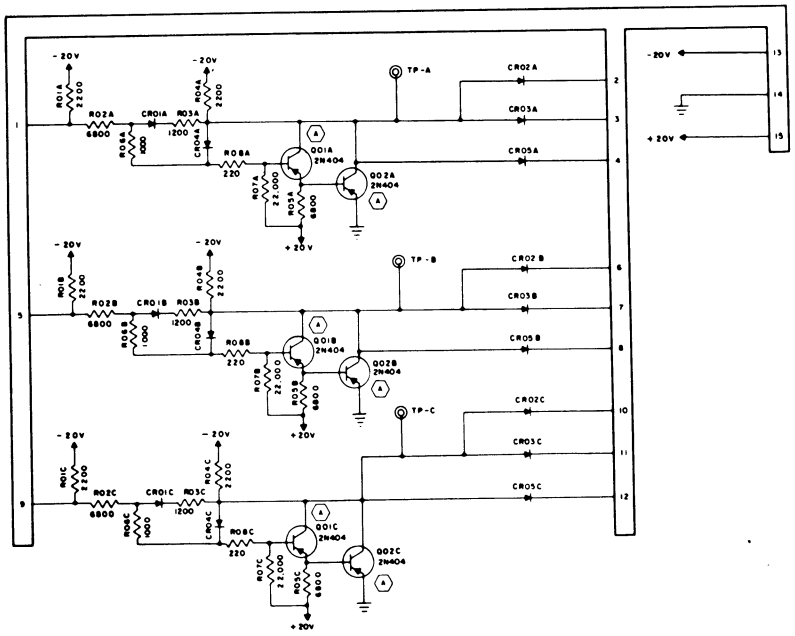
These circuits are similar to the 1604-type inverter, except that the modified input allows the circuit to accept higher voltage signals.

Inputs and outputs are as follows:

Input	Output
-0.5v (or ground)	-3v "1"
-18v (or open)	-0.5v "0"



Input 61

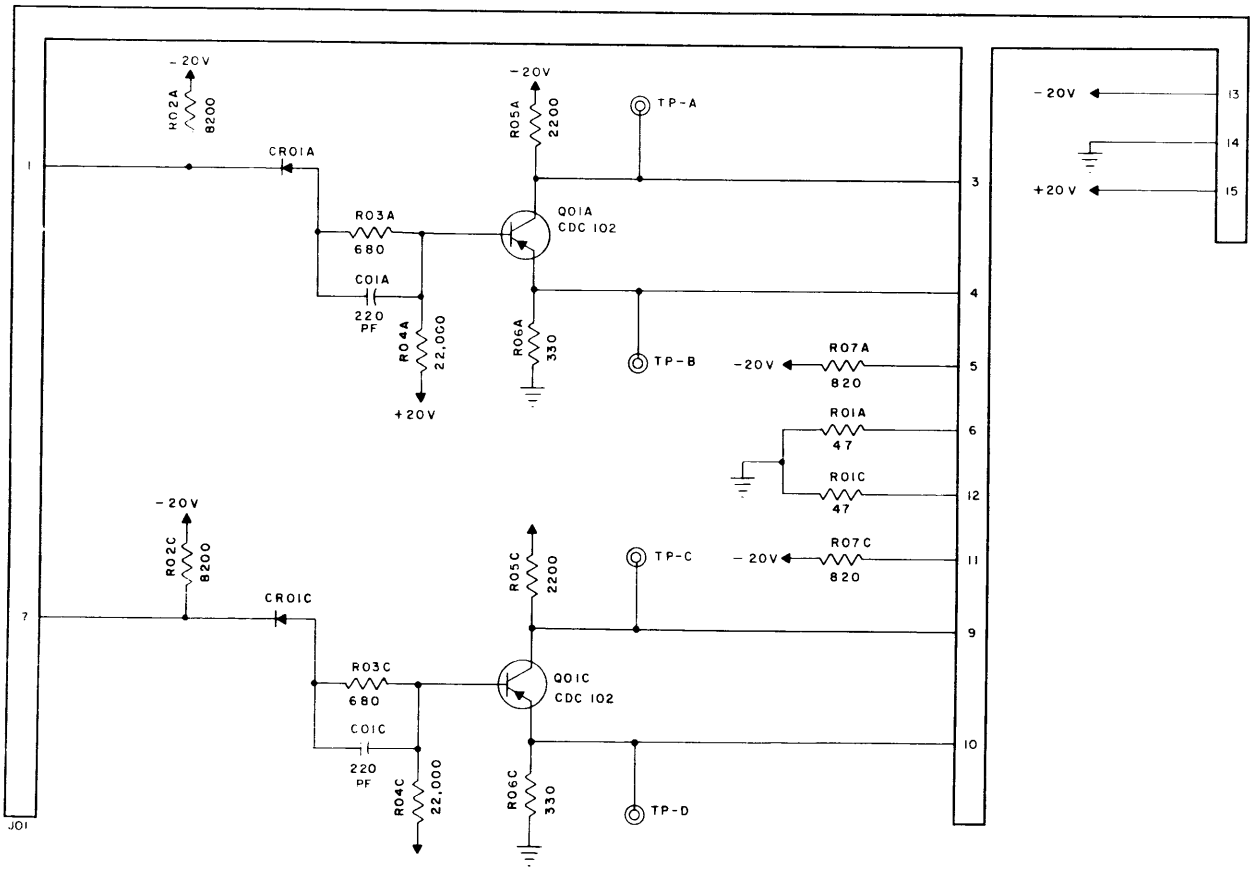


Input 87

OUTPUT

Card Type 79A

The function of the circuits on this card is to enable 1604-type logic to interface with IBM equipment. The card contains a biasing network, and both "P" and "N" signal levels may be produced as shown in the accompanying diagram.



Output 79A

TRANSMITTER AND RECEIVER
Card Types C62B and C61

GENERAL

The circuit configuration shown on page 4-C62-3 performs high speed transmission of digital information from one module to another. Inputs to the transmitter circuit are logical "1's" and "0's" of -5.8v and -1.1v respectively. The transmitter converts these single-ended inputs to double-ended outputs suitable for transmission over a balanced transmission line. Tests using an 8-megacycle bit rate input have shown that 1 transmitter satisfactorily drives 20 receivers and 19 unused transmitters located at any point along a 200 foot transmission line.

The transmission line is twisted-pair having a characteristic surge impedance of approximately 110 ohms and is terminated at each end in its characteristic impedance. Transmission signal levels are approximately 0.5v line-to-line, and a "1" is distinguished from a "0" by a full voltage reversal.

The line voltage levels which represent a "0" are established by current flow from the +20v to the -20v source at the terminating resistors. Each of these currents is of the order of 5 ma, so that the total voltage developed across the terminating resistors is approximately 0.5v.

When the 3-way AND input to the transmitter is disabled by a "0", transistor Q01 is turned on and current is shunted around the two constant current drivers Q02 and Q03. With the AND enabled by "1" inputs, Q01 is turned off, thus allowing Q02 and Q03 to drive a constant 20 ma into the transmission line. Originally, the bias networks on the line were producing a 5 ma current flow in one direction through the terminating resistors, but when the transmitter switches on, the direction of net current flow through the terminating resistors effectively reverses. The current from the transmitter divides into two 10 ma currents which flow through each line termination. This current is in the opposite direction to the 5 ma bias current; thus the net current flow is 5 ma in the opposite direction, producing a voltage drop equal and opposite to the original voltage. This results in a full voltage reversal for separating a "1" from a "0", although the signal level remains of the order of 0.5v line-to-line.

TRANSMITTER, Card Type C62

The printed circuit card contains two identical transmitter circuits designated A and B. A typical circuit is shown on page 4-C62-3.

The logic input circuitry consists of a 3-way AND. The output of a standard logic card constitutes a proper input to a transmitter. A logical "1" input causes transistor Q01 to turn off and Q02 and Q03 to turn on, while a "0" input has the opposite effect.

A -1.1v "0" input causes the emitter-base junction of Q01 to be forward biased, fully turning on Q01. When Q01 is turned on, a shunt path for current is provided around Q02 and Q03. Since Q02 and Q03 no longer have a source of current, no current is injected into the transmission line.

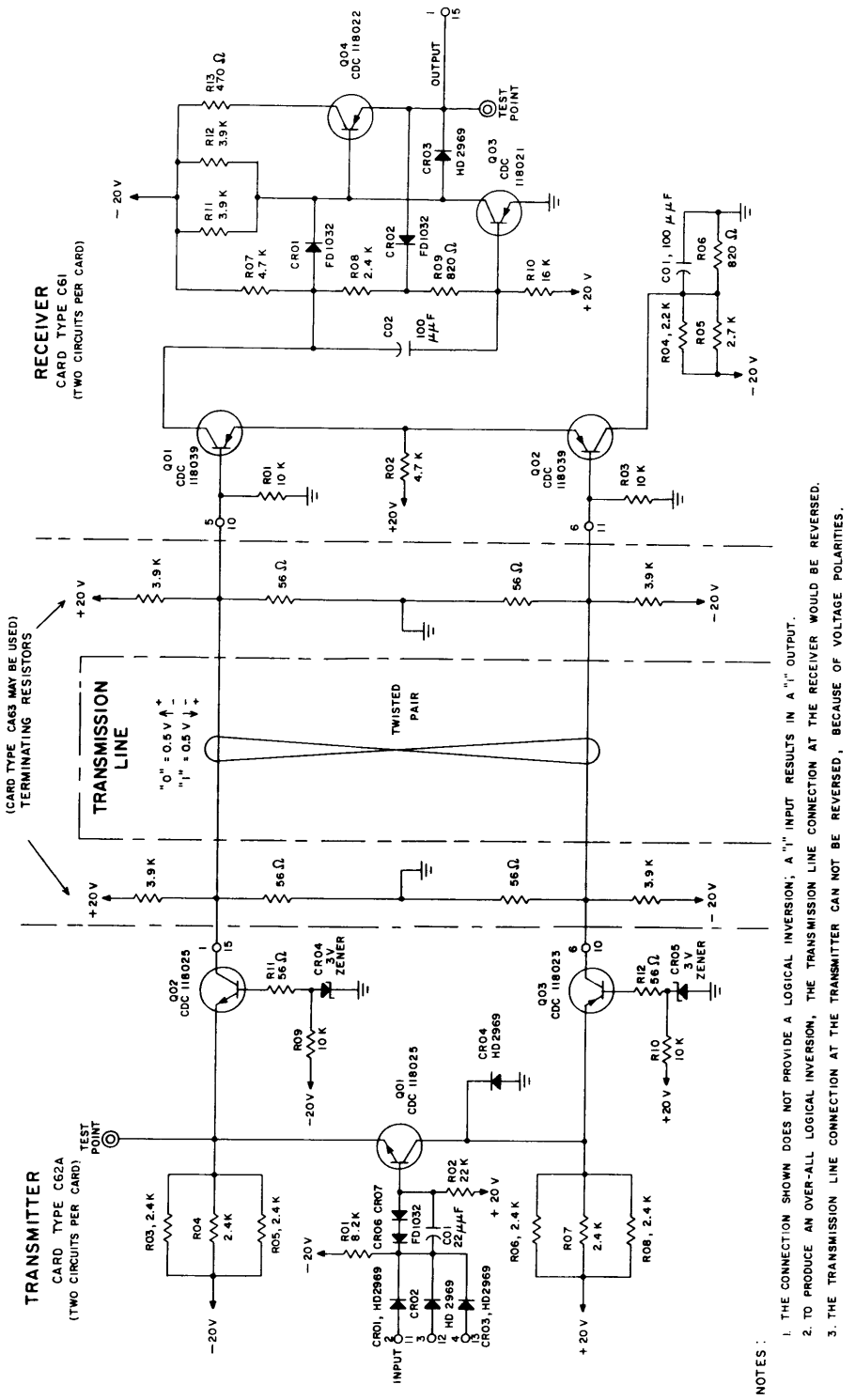
When the AND input is satisfied, the base of Q01 is held at approximately -5 volts. This reverse biases the emitter-base junction by approximately 3 volts and causes Q01 to be turned off. Since the shunt path for current around Q02 and Q03 no longer exists, they become constant current generators of opposite polarities. Q03 injects a current of approximately 20 ma into the line and a like amount of current flows out of the line into Q02.

The base networks of Q02 and Q03 each contain a 3v zener diode which performs two functions. In the first case, the zener diode sets the voltage level at which the emitters of Q02 and Q03 reach their turned-on state. This, in turn, sets the threshold that must be overcome at the base of Q01, since its emitter is at the same potential as the emitter of Q02. In the second case, the zener diodes set the base voltages of Q02 and Q03 which determine how much noise voltage is allowed at the collectors before the collector-base junctions become forward biased. This value of noise voltage is something over 3 volts since the forward drop of the collector-base junctions adds to the zener diode voltage. This means that the transmitter operates satisfactorily with up to 3 volts of random noise on the transmission line.

The transmitter must be connected to the line in only one polarity, as shown on page 4-C62-3. This is necessary to provide current through the terminating resistors in a direction opposite the bias current.

TRANSMISSION LINE

A terminated balanced twisted-pair transmission line carries digital information from the transmitter to the receiver. This information is in the form of line-to-line



Transmitter and Receiver C62 and C61

differential voltages of the order of 0.5v, with a complete voltage reversal distinguishing a "1" from a "0".

The surge impedance of the transmission line is 100 to 120 ohms. The line is terminated at each end with a 112-ohm resistive load, consisting of two 56-ohm resistors in series across the line with an optional center ground reference. This provides very good impedance matching and, as a result, reflections and standing waves are minimized.

The line is biased at each end by means of 3.9k resistors to +20v and -20v to achieve a 5 ma bias current through the terminating resistors. This holds the "0" state signal level at 0.5v line-to-line.

The length of a transmission line may be up to 200 feet, with as many as 20 transmitters and 20 receivers placed in parallel along its length.

Bit rates of 8 mc or greater are possible on a 200 foot line. Low bit rates over longer distances are limited by the d-c line losses; however transmitters may be paralleled for longer distances to overcome these losses.

The velocity of signal propagation along the line is approximately 50 percent to 60 percent of the velocity of light. This results in a time delay per foot of the order of 1.6 to 1.8 nanoseconds.

The balanced system using differential receiving techniques allows a difference in noise levels up to 3v to be tolerated between the transmitter ground reference and the receiver ground reference.

RECEIVER, Card Type C61

The printed circuit card contains two identical receiver circuits designated A and B. A Typical example is presented on page 4-C62-3. This portion of the circuit connected to the collector of Q01 is similar to a logical inverter, which is discussed elsewhere in this report.

This circuit functions as both a differential amplifier and a discriminator. It provides a logic output of either "1" or "0", according to the polarity of the differential 0.5v signal which the two input terminals receive from the transmission line.

The circuit inputs are connected directly into the bases of Q01 and Q02. The 0.5v differential input is centered about ground, so one input shifts approximately 0.25v positive while the other input shifts negative a similar amount. The two input transistors Q01 and Q02 are PNP type CDC C07's; thus the transistor which receives the negative input conducts more heavily while the one receiving the positive input conducts less heavily.

The circuit is such that a negative input to the base of Q01 and a positive input to the base of Q02 results in a logical "1" at the receiver output. Under the opposite conditions of a positive input to Q01 and a negative input to Q02, the output is a logical "0". Thus, by reversing the connections at the receiver inputs, it is possible for a given set of conditions on the transmission line to produce either a "1" or a "0" at the receiver output.

The circuit shown on page 4-C62-3 does not produce an inversion between input to the transmitter and output from the receiver. A "1" input to the transmitter produces a transmission line signal of approximately 0.5v line-to-line with the polarity as shown. This allows transistor Q01 to apply approximately 5 ma of collector current to the junction of R07, R08, and the anode of CR01, which causes Q03 to switch off and Q04 to switch on, providing a "1" output. In this state, transistor Q04 can drive 8 OR loads. With opposite conditions at the receiver input, the output can drive 8 AND loads.

GROUND RULES

1. The output of a logic card constitutes a proper input to a transmitter.
2. The output of a receiver constitutes a proper input to a logic card.
3. A receiver may drive 8 OR loads, 8 AND loads, or any combination resulting in 8 loads total.
4. The transmission line is twisted-pair, having a surge impedance of 100 to 120 ohms.
5. The transmission line may be any length up to 200 feet.
6. The transmission line is terminated at each end in a resistive load approximately equal to its surge impedance.
7. A logical inversion between input to transmitter and output from receiver may or may not occur, depending upon the transmission line connections at the receiver.
8. The transmission line connections at the transmitter can not be reversed, due to the polarity of the line bias voltage.

9. Up to 20 transmitters and 20 receivers may be connected along a transmission line.
10. A transmitter having an 8 megacycle bit rate input will drive 20 receivers at the end of a 200 foot transmission line, with 19 inactive transmitters also connected to the line.
11. Inactive transmitters and receivers do not load a transmission line and do not have to be disconnected from it.
12. No more than 8 transmitters should be driven by an inverter and no more than 7 should be driven by a flip-flop.

MODIFIED M^{---} INPUT
Card Types C75* and C75B

FUNCTION

This card contains two identical circuits. Its function is to enable the 3600 computer system to receive information from a 1604 type input/output cable. This is done by converting the "1" and "0" signal levels from -0.7v and -18v to -5.8v and -1.1v, respectively.

OPERATION

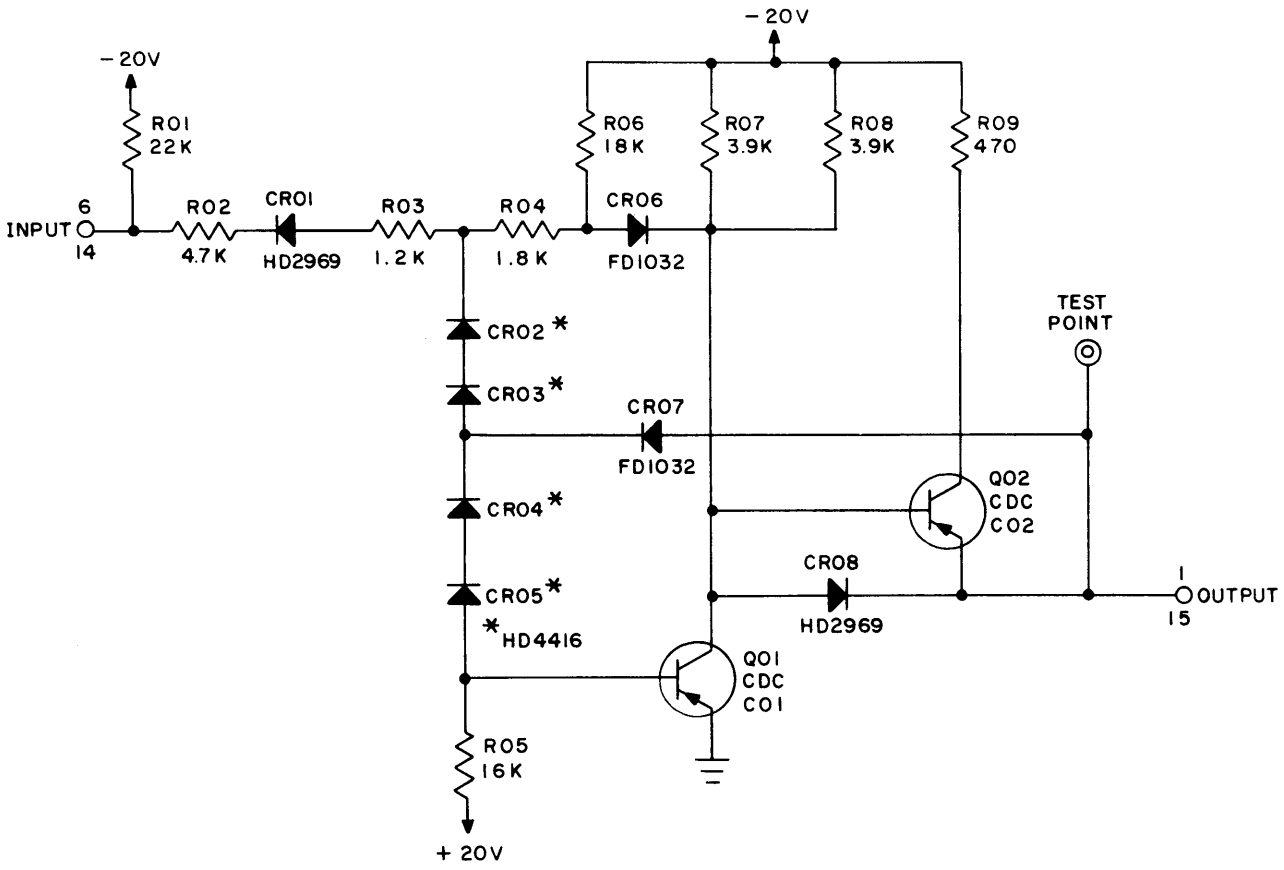
This circuit is essentially a single inverter having one OR input which has been modified by the deletion of the input coupling capacitor and the addition of resistors R01 and R02. These provide a voltage dividing effect, so a -18v input results in approximately -6v at the cathode of CR01. Similarly, a -0.7v input results in -0.7v at that point.

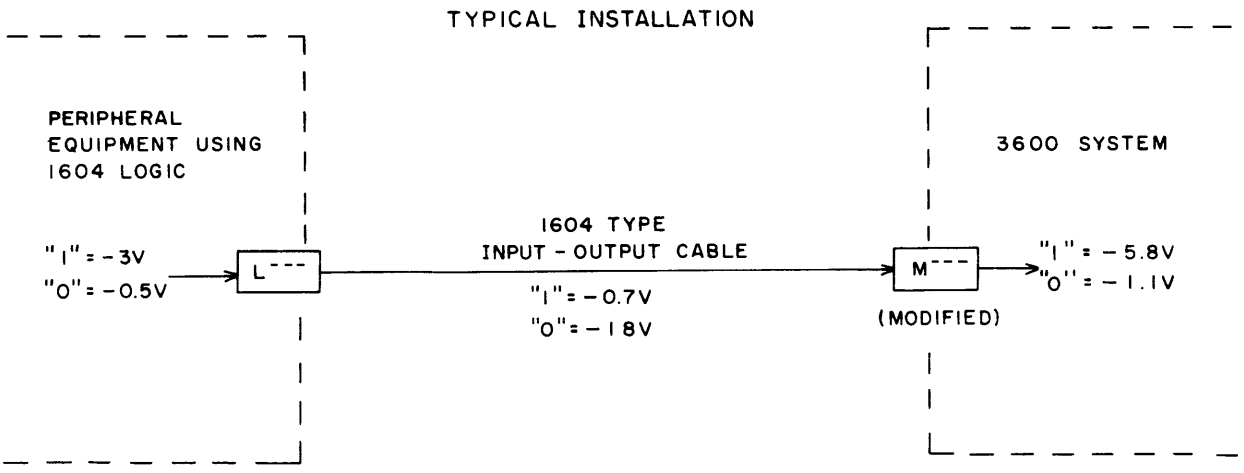
The remainder of the circuit is identical to a single inverter, which is discussed elsewhere.

The C75B is capable of driving 8 OR loads, 8 AND loads, or any combination resulting in 8 loads total.

The C75 is capable of driving 3 OR loads, 8 AND loads, or any combination resulting in 8 loads total, but not to exceed a total of 3 OR loads.

*All future cards of this type are C75B





Modified M--- Input C75
(Two circuits per card)

MODIFIED L--- OUTPUT
Card Types C76* and C76A

GENERAL

This card contains two identical circuits. Its function is to enable the 3600 computer system to transmit information to peripheral equipment containing 1604 type logic. This is done by converting "1" and "0" levels from -5.8v and -1.1v to approximately -0.7v and -18v, which are the signal levels transmitted over a 1604 input/output cable. An M--- card in the peripheral equipment converts these signals to -3v and -0.5v, which respectively represent "1" and "0" in the 1604 type logic.

MODIFICATIONS

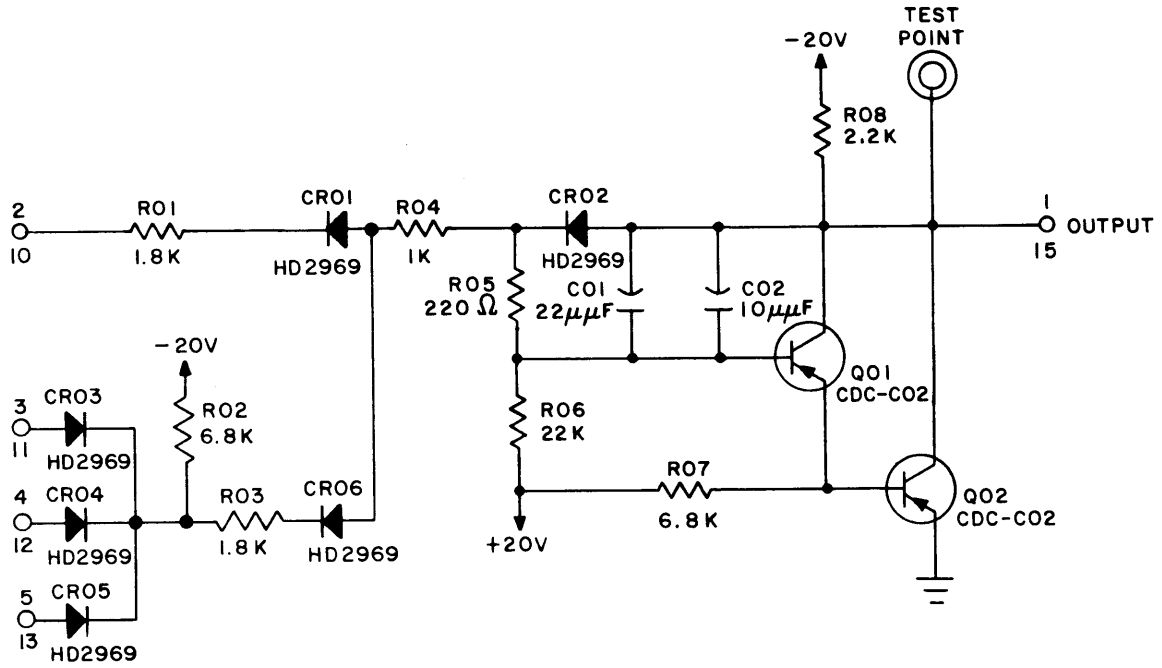
The modified L--- circuit shown on page 4-C76-2 is similar to one of the circuits contained on the 1604 card type 62. It has been modified through the use of CDC C02 transistors, reduction of the Miller feedback capacitance to 32 uuf, and the addition of 1.8 k resistors in the input networks. This enables the circuit to accept 3600 logic level inputs, and results in a switching time of approximately 0.8 usec.

OPERATION

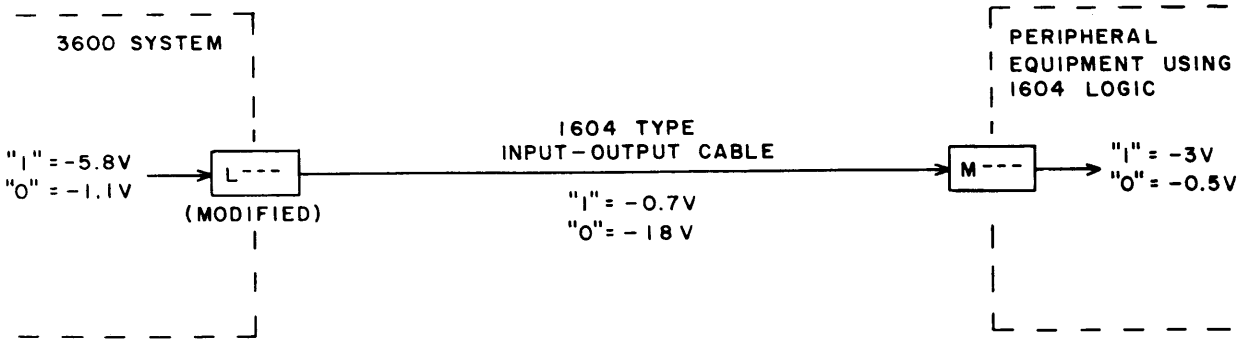
The circuit inputs are a three-way AND and an OR. The threshold level at the cathodes of CR01 and CR06 is approximately -1.5v. Thus as the circuit input becomes more negative, conduction increases from the +20v source through the resistor network. When the circuit input reaches the -3v level, the resulting voltage drop at the base of Q01 provides sufficient forward bias to the base-emitter junction of transistor Q01, so that it starts to switch to its conduction state.

The voltage at the base of Q01 is clamped at the sum of the base-emitter junction drops of Q01 and Q02, which is approximately -0.6v. Thus, as the input goes negative, the voltage across R06 is clamped at approximately 20.6v so that the current through it does not increase beyond approximately 0.9 ma. Therefore, as the input becomes more negative, turn-on current is drawn through transistors Q01 and Q02. This action begins when the input reaches approximately -3v, and as the input continues moving negative to the -5.8v "1" level, Q01 and Q02 switch to a state of heavy conduction.

*All future cards of this type are C76A.



TYPICAL INSTALLATION



Modified L--- Output C76
(Two circuits per card)

Transistor Q01 is connected as an emitter follower and Q02 as a grounded emitter stage. Thus when Q01 switches on, Q02 conducts heavily, providing a low impedance path from ground to the circuit output. The transistors are clamped out of saturation by diode CR02, but their collector potential is approximately -0.7v when both are in the conduction state.

A positive-going input causes transistor drive current to decrease, and when the input becomes more positive than -3v, transistor Q02 switches off, and the circuit output approaches -18v.

The switching time of the circuit is approximately 0.8 usec. The limiting factor is the 32 uuf of Miller feedback capacitance, which effectively slows the response of Q01.

LONG LINE DRIVER AND RECEIVER
Card Types CA98 and HA26

GENERAL

This circuit configuration performs high-speed transmission of digital information from one module to another over distances to 1000 feet. The driver card converts system logic levels into voltages suitable for output over an unbalanced transmission line. The receiver card converts the transmission line voltages into system logic levels capable of operating subsequent logical stages.

Transmitted carrier levels are -0.15v for a logic "1" and -2.1v for a logic "0". These levels are established by current flow through the termination networks. When the transmitter is turned off, the terminating network biases the line at 2.1v while turning on the long line driver forces the line to the -0.15v level.

LONG LINE DRIVER, Card Type CA98

The printed circuit card shown in the illustration contains two identical transmitter circuits which are designated A and B.

The logic input circuitry consists of a 3-way AND and an OR input. A -1.1v logic "0" results in the application of a positive potential to the base of Q01. Consequent emitter follower action causes a positive voltage to be coupled to the base of Q02. The resultant reverse bias condition at the emitter/base junction turns off Q02.

When Q02 is turned off, the transmission line will be biased at -2.1v. A -5.8v logic "1" signal causes a negative potential to be applied to the base of Q01. The resultant current increase in Q01 allows the base current of Q02 to increase to the saturation level. The saturation of Q02 forces the transmission line to the -0.15v level.

TRANSMISSION LINE

A terminated unbalanced transmission line conveys digital information between the driver and receiver cards. A -2.1v input to the receiver card signifies a logic "0" while a -0.15v level signifies a logic "1".

The line is terminated at each end in approximately 110 ohms. A normal -2.1v line level is established by the terminating network, while turning on the driver forces the line to -0.15v.

Separate power supplies may be used with each terminating network. The two power supplies are interconnected by means of the illustrated diode network. This arrangement gives either or both power supplies the ability to bias the line.

The transmission line, which is limited to 1000 feet, can service combinations of up to eight long line drivers and eight long line receivers.

Two electrically paralleled connectors connect a given piece of equipment to the transmission line. Equipment located at the extremities of the line must have one of its connectors directed to a termination network.

The velocity of signal propagation along the line is approximately 50 to 60 percent of the velocity of light. The resultant time delay per foot is of the order of 1.6 to 2.0 nanoseconds.

The long line driver/receiver will tolerate typical noise levels to 0.75v.

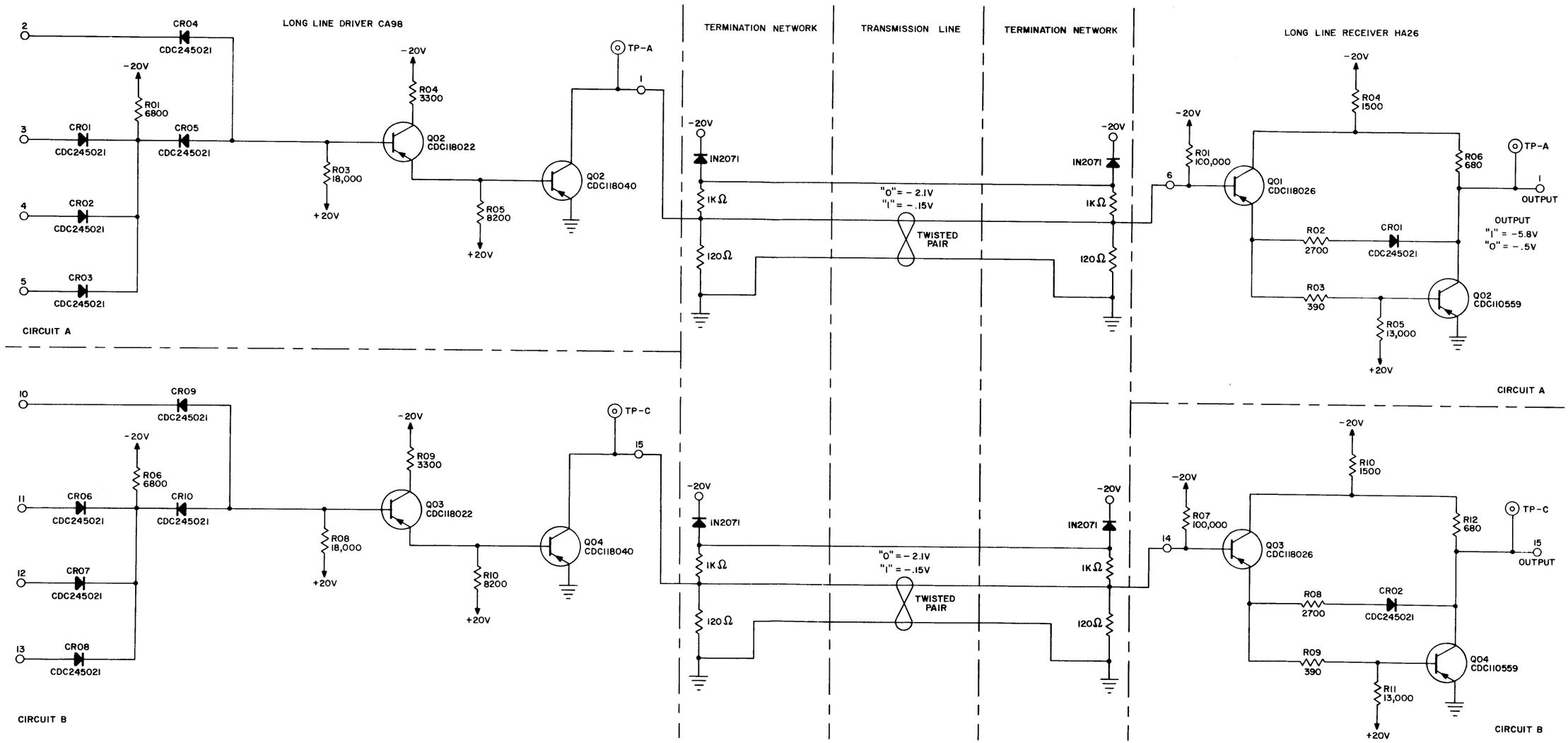
LONG LINE RECEIVER, Card Type HA26

This card contains two identical long line receiver circuits designated A and B. The receiver card responds to transmission line inputs of -2.1v and -0.15v which signify logic "0" and logic "1" inputs respectively. A -2.1v signal at the receiver input is applied to the base of Q01. The resultant forward bias condition allows conduction through Q01. Emitter follower action forward biases Q02. The resultant saturation of Q02 forces the collector potential to 0.2v.

A -0.15 signal at the receiver input turns Q01 off. This allows diode CR01 to become forward biased permitting feedback between the base and collector. This feedback stabilizes the collector voltage at -5.8v.

GROUND RULES

1) The output of a logic card constitutes a proper input to a long line driver.
2) The output of a long line receiver constitutes a proper input to a logic card.
3) A long line receiver may drive up to eight "AND" loads or up to three "OR" loads.
4) The transmission line may be of any length to 1000 feet. Transmission lines over 500 feet in length use 20-gauge wire, whereas lines less than 500 feet may use 24-gauge wire.
5) Any combination of up to eight long line drivers and eight long line receivers may be connected to one transmission line.



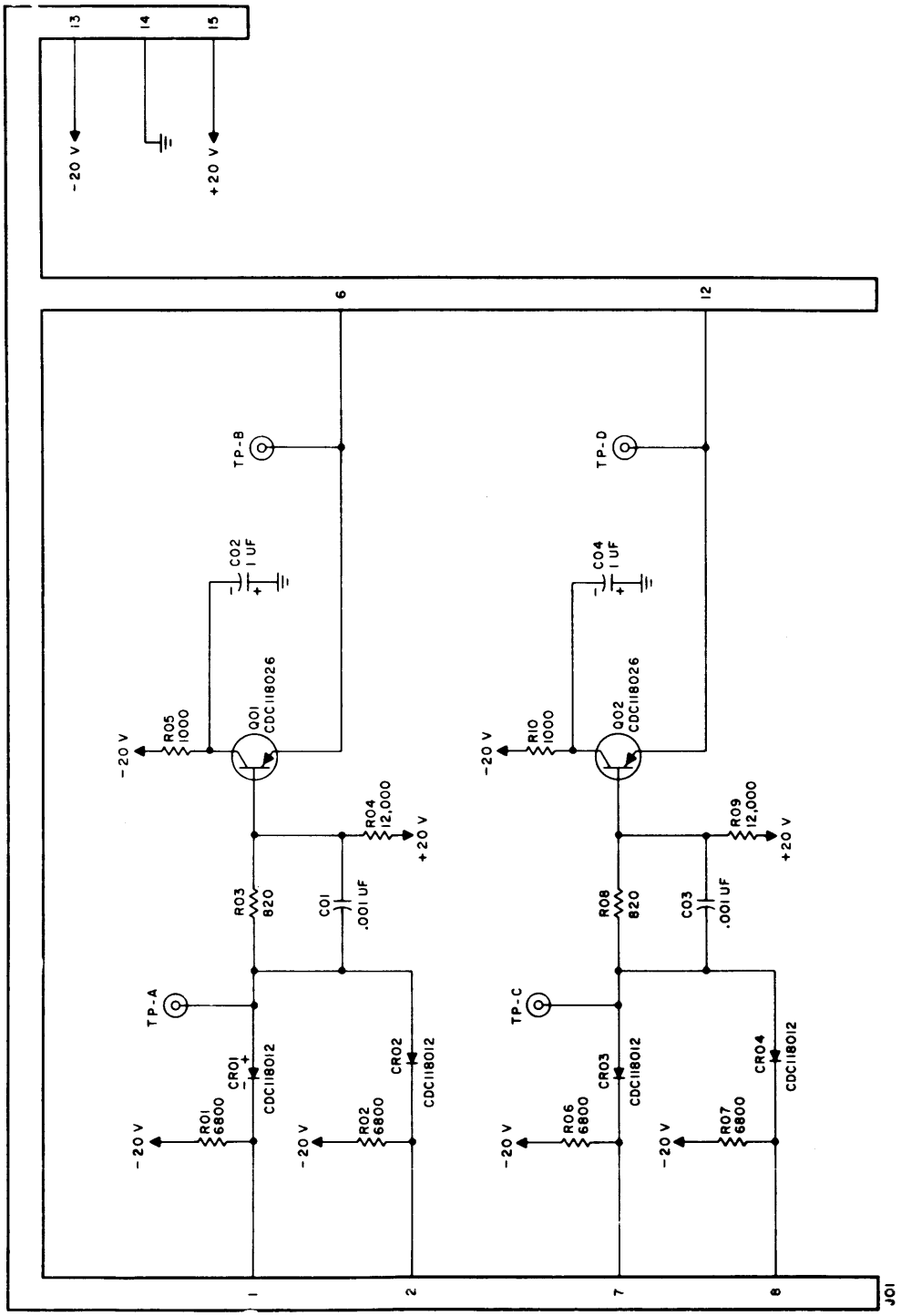
Long Line Driver CA98 Transmission Line and Long Line Receiver HA26

LINE DRIVER

Card Type E12

Card Type E12 is a ±1.0v (C Type, IBM) Line Driver. This card can be used to interface Control Data equipment using 1604-type logic with IBM equipment which uses C-line voltage levels. The card has two inputs and one output. An output of ±1.0v is obtained when a -3v "1" or -0.5v "0" is applied at the input.

The card has two identical emitter follower circuits. Since transistor Q01 is connected in an emitter-follower configuration, there is no phase reversal between the input and output. As the input signal becomes less negative, -0.5v, the forward bias is reduced and the output is +1v. When the input signal is -3.v, the forward bias is increased and the output is -1v.



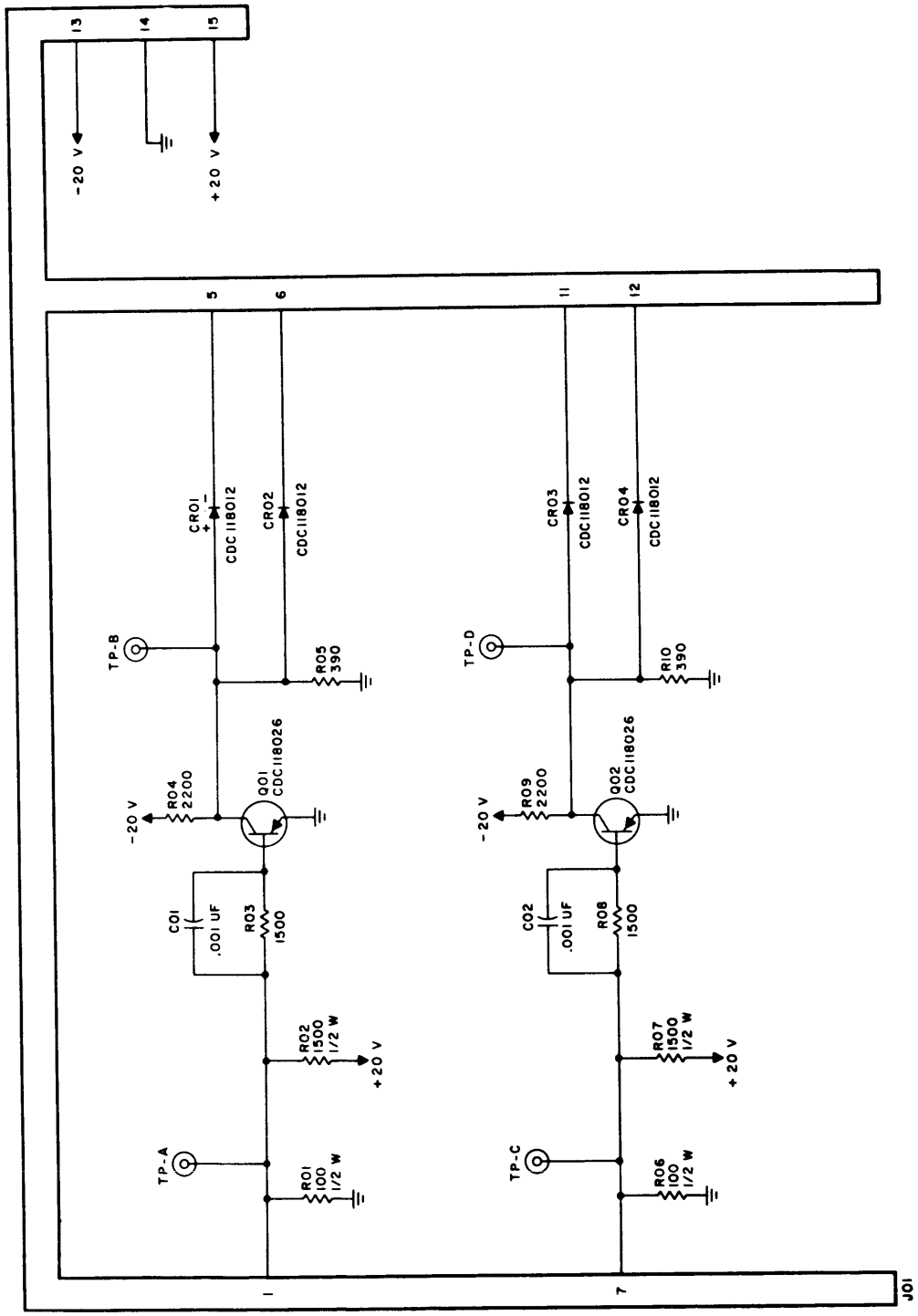
Line Driver E12

LINE RECEIVER

Card Type E13

Card type E13 is a ±1.0v (C-type), IBM Line Receiver and is a counterpart of E12. The card enables 1604-type logic to receive signals from IBM equipment which uses C-line logic levels.

The card has two identical common inverter circuits Pins 1 and 7 are used as input pins; and pins 5, 6, 11, and 12 as output pins. An input of -1.0v gives an output of -0.5v "0". An input of +1.0v gives an output of -3.0v "1". Resistors R01, R02, and R05 are voltage dividers and C01 is a by-pass capacitor.



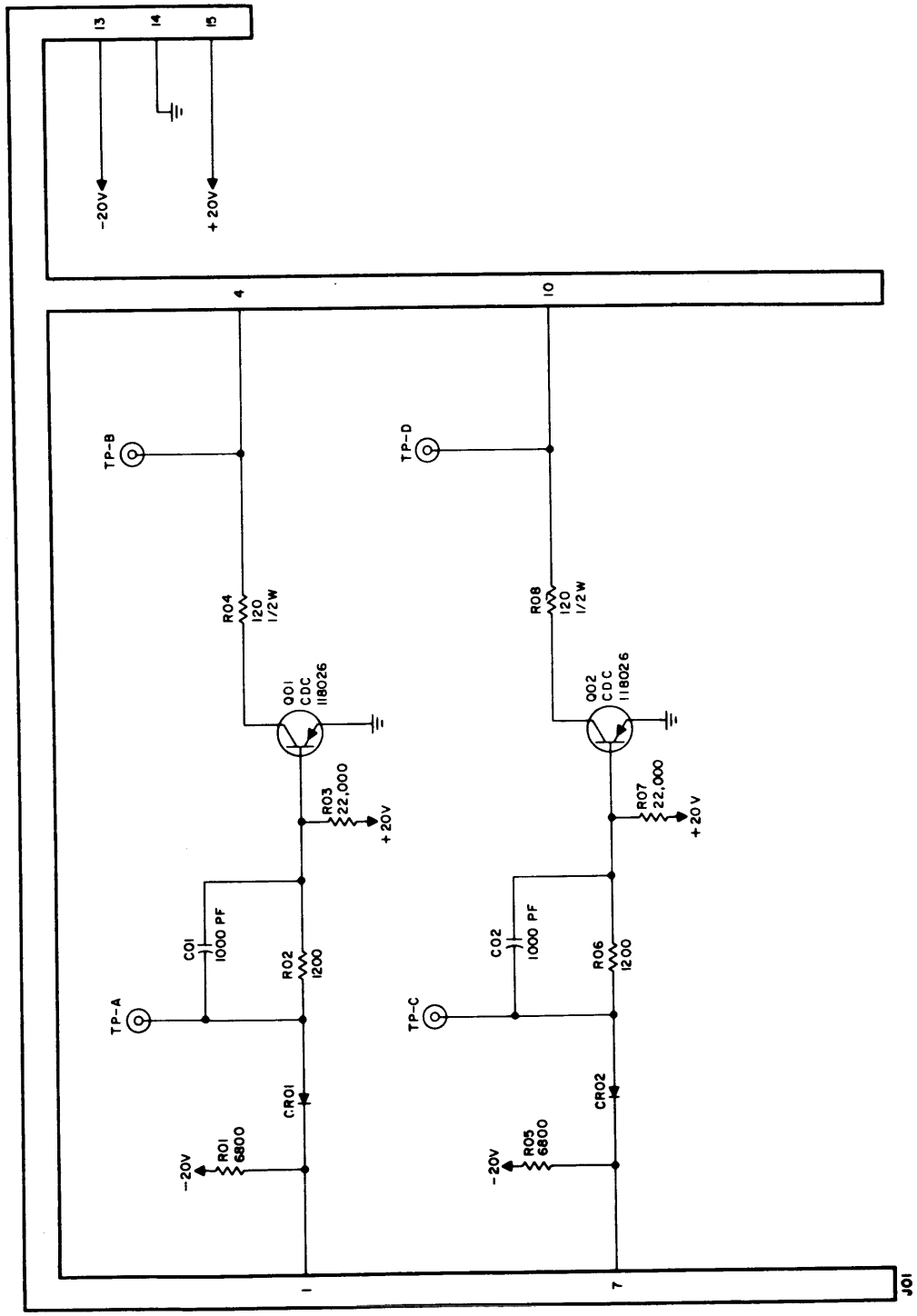
Line Receiver E13

LINE DRIVER

Card Type E15

Card E15 has been designed to convert 1604-type logic levels to IBM P-line logic levels (-6 ± 1v).

The card has two identical circuits, each having one input and one output. The circuit consists of a single stage simple inverter (common-emitter). Capacitor C01 is a bypass capacitor. An output of -6 ± 1v is obtained when a -3.0v "1" or -0.5v "0" is fed as an input.



Line Driver E15

LINE RECEIVER

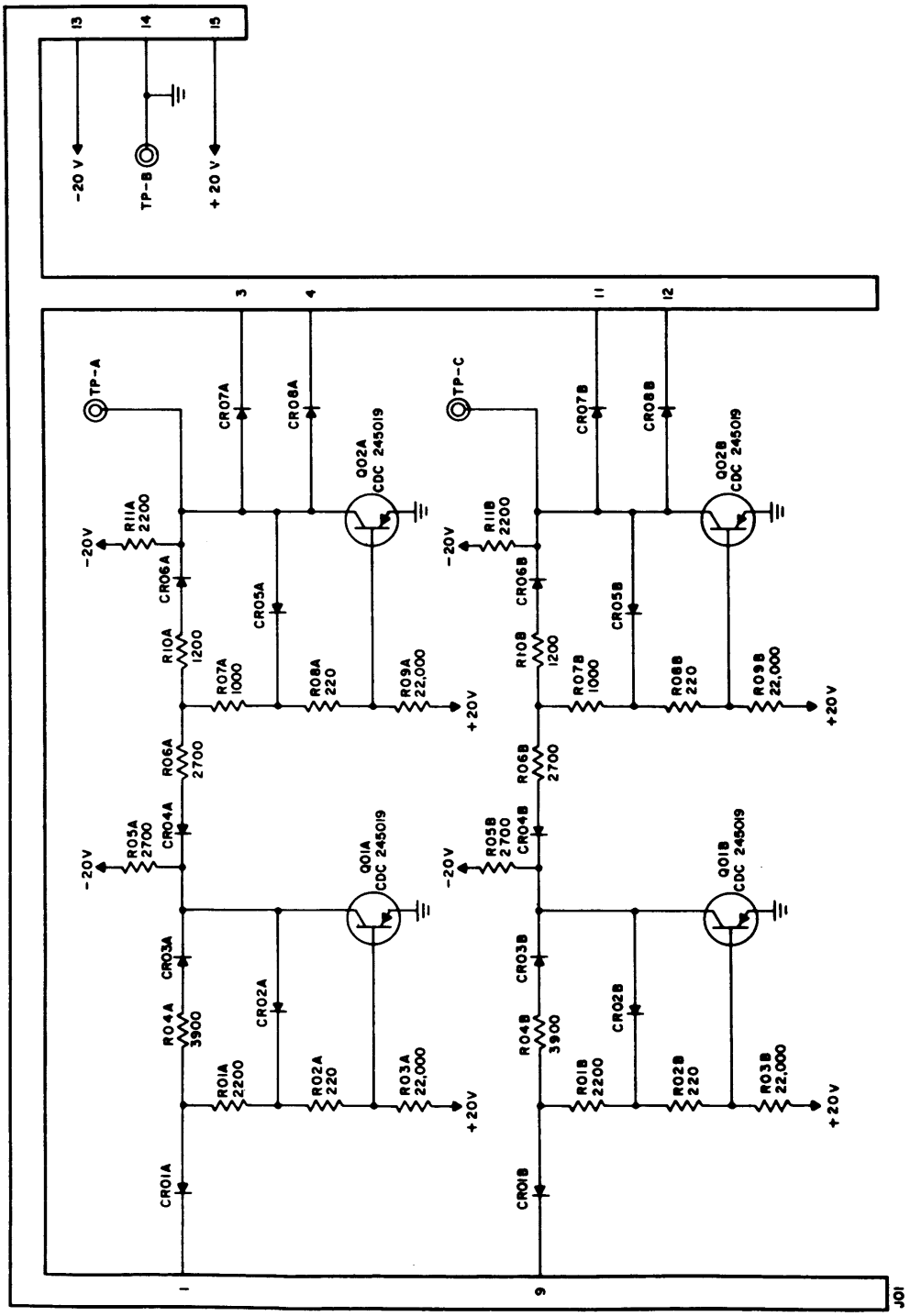
Card Type E61-A

Card type E61A is a receiver card which converts a -6v input to -3v "1" output and a 0v input to a -0.5v "0" output.

The card has two identical circuits, each containing one input and providing two outputs. A circuit consists of two common emitter inverter sections. The component values of the two circuits are such that an input of approximately 0 volts causes Q01 to approach cutoff and Q02 to approach saturation. When Q02 is near saturation, output diodes CR07 and CR08 provide a -0.5v output. An input of -6v causes Q01 to approach saturation and Q02 to approach cutoff. When Q02 is near cutoff, output diodes CR07 and CR08 provide a -3.0v output.

Feedback diodes CR02, CR03, CR04, CR05, and CR06 speed the switching time of the transistors by preventing complete cutoff or saturation.

Line driver counterparts of the E61A receiver are E62B and E67A.



Line Receiver E61A

LINE DRIVER

Card Types E62B and E67A

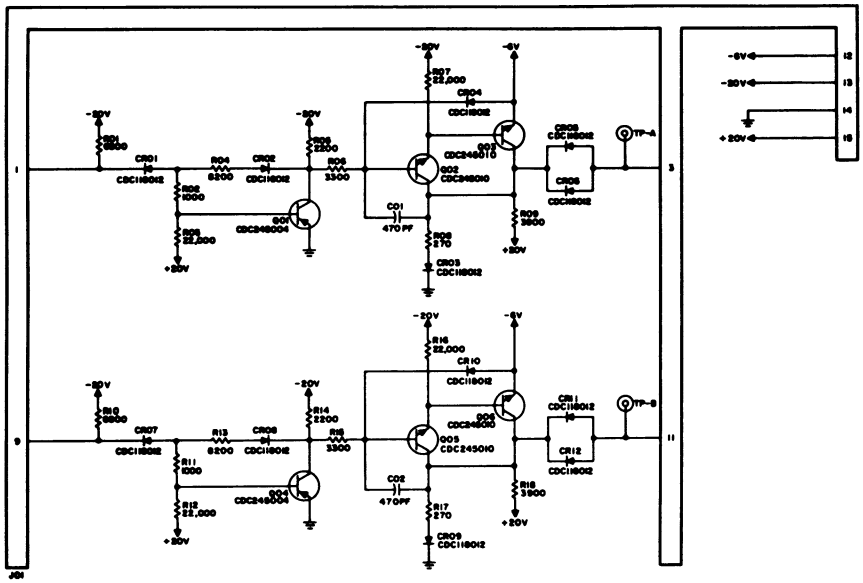
Card types E62B and E67A provide a 0v output for a -0.5v "0" input and a -6v output for a -3v "1" input. The only difference between the two cards is that E67A has an additional OR input.

Card circuits have three sections: input, amplifier, and output. The input section consists of a PNP transistor inverter. The amplifier section consists of two NPN transistor amplifiers. The output section consists of two parallel isolating diodes.

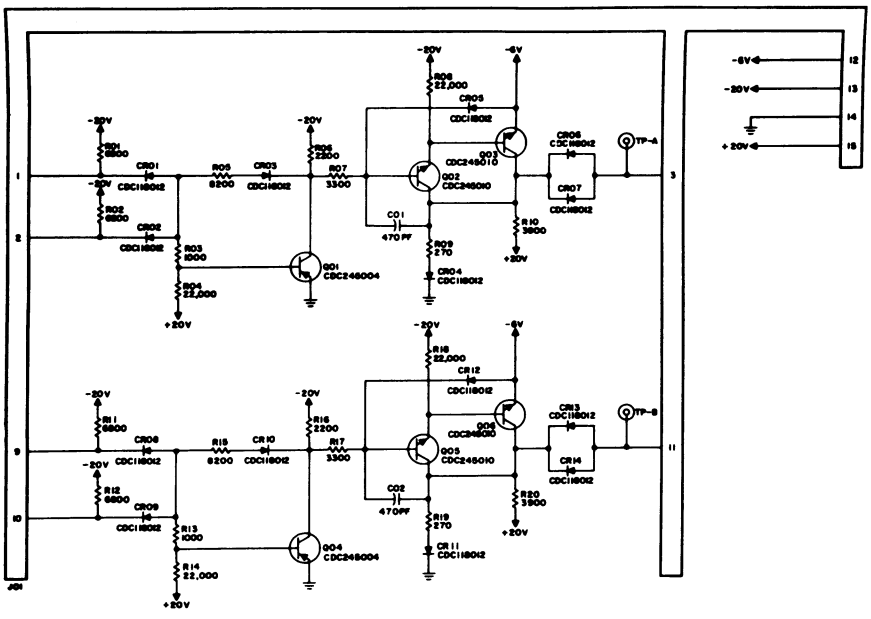
An input of logical "0" (-0.5v) at pin 1 (pin 2 for E67A) places a small positive voltage (approximately .8v) on the base of transistor Q01, causing it to approach cutoff. When Q01 is near cutoff, its collector is at approximately -10v, and the base of Q02 approaches -6v as C01 charges through R06, causing transistors Q02 and Q03 to approach cutoff. When Q03 is near cutoff, diodes CR05 and CR06 are reverse biased and have a small positive voltage (effectively 0v).

An input of "1" (-3.0v) at pin 1 (pin 2 of E67A) places a negative voltage of approximately -0.5v on the base of transistor Q01, causing it to approach saturation. When Q01 is near saturation, the voltage on its collector approaches 0v, and the base of Q02 becomes more positive as C01 discharges through R06. As the base of Q02 becomes more positive, conduction increases, and Q02 approaches saturation. As the conduction of Q02 increases, the base of Q03 becomes more positive, and it approaches saturation. When Q03 is near saturation, the -6v supply is impressed across the output diodes CR05 and CR06.

The switching time of the Q02-Q03 amplifier circuit is dependent upon the charge-discharge time of C01 through R06. In order to speed the switching time of the transistors, feedback is provided through CR02 and CR04 to prevent the transistors from being driven to complete saturation.



Line Driver E62B



Line Driver E67A

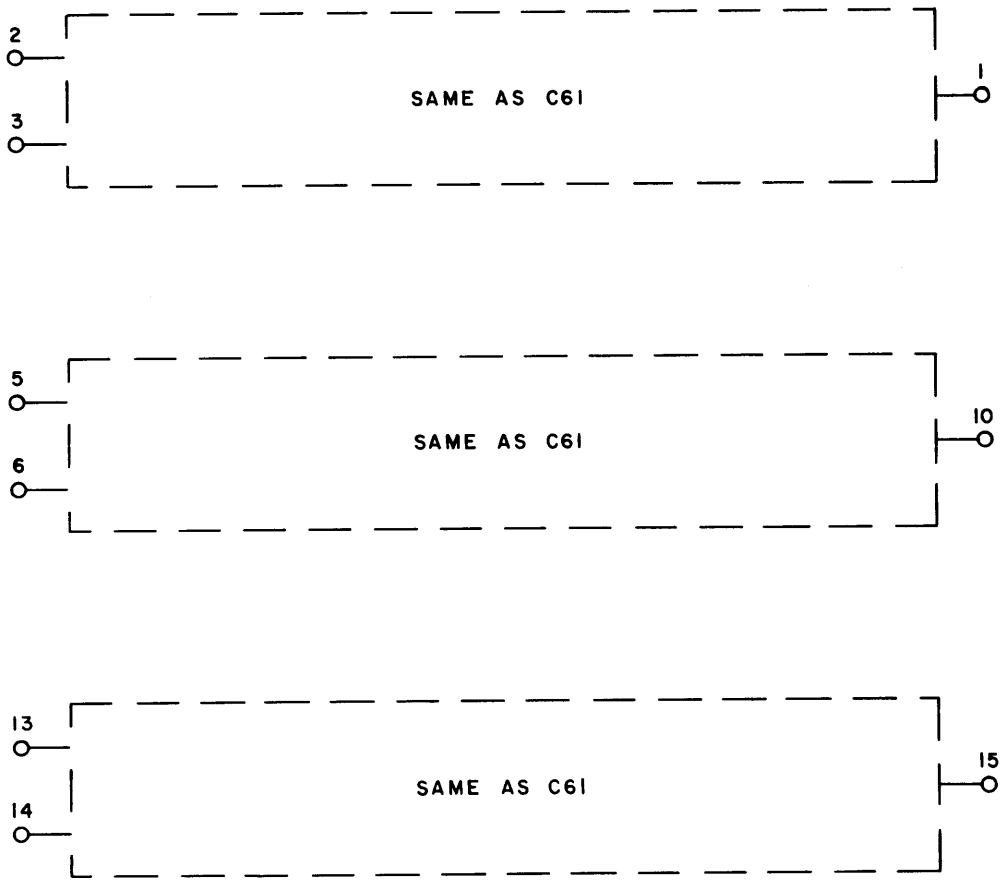
RECEIVER
Card Type HA11A

This card contains three receiver circuits, having the pin connections shown in the accompanying diagram. The circuits operate the same as card type C61, which is discussed elsewhere.

The circuit functions as both a differential amplifier and a discriminator. It provides a logic output of either a -5.8 v "1" or a -1.1 v "0", according to the polarity of the differential 0.5 v signal which the two input terminals receive from the transmission line.

The transmission line is balanced, terminated, twisted-pair, and the signals are centered about ground. As an example, if pin 2 goes to +0.25 v and pin 3 goes to -0.25 v, pin 1 will go to -1.1 v "0". If the inputs are reversed, the output will be -5.8 v "1".

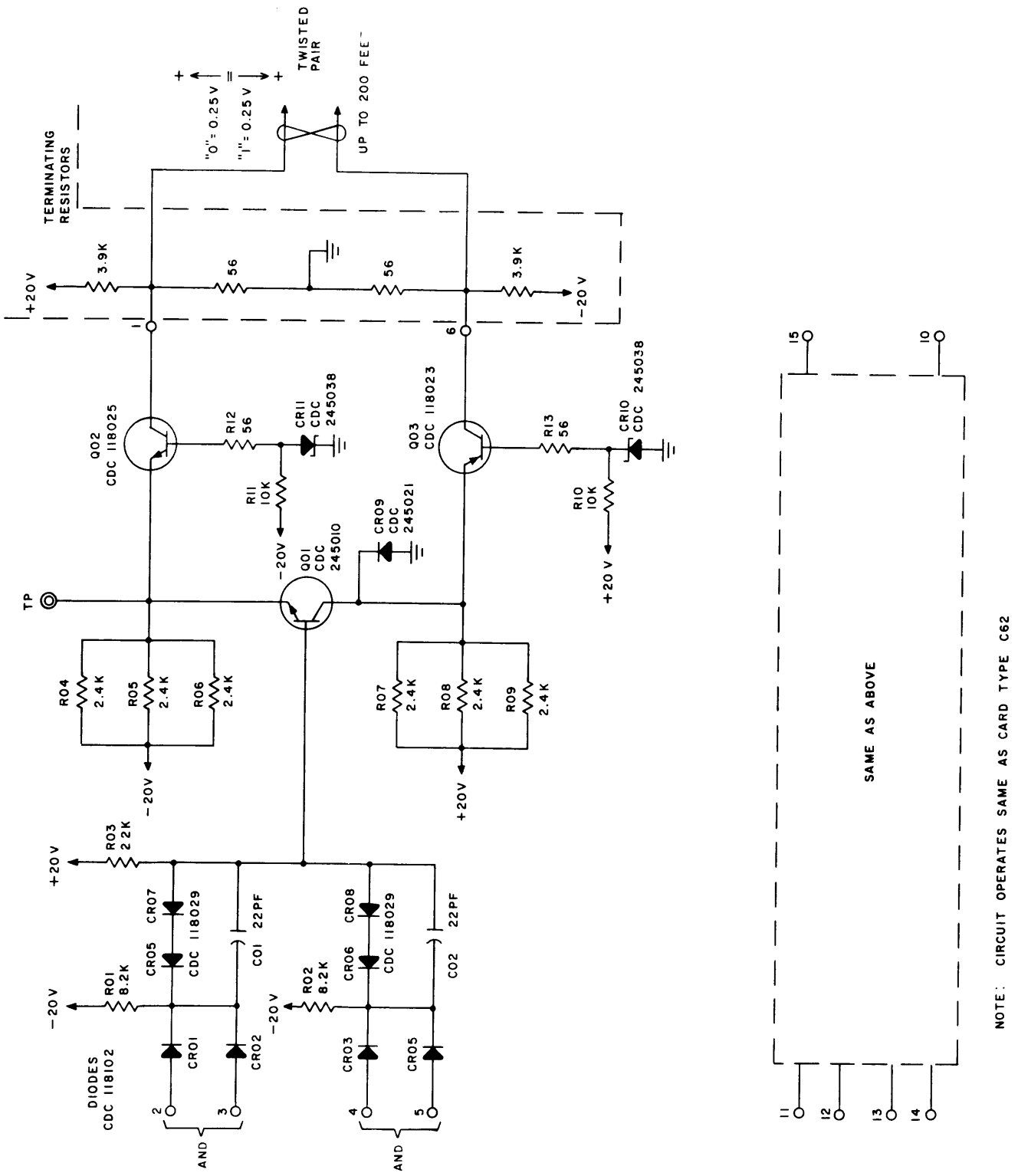
The receiver circuit will drive 8 loads, and the ground rules are the same as for card type C61.



NOTES: 1. CIRCUITS OPERATE SAME AS C61.
2. 3 RECEIVER CIRCUITS PER CARD.

TRANSMITTER
Card Type HA19

The function of the circuits on this card is to convert logic signals into outputs suitable for transmission over a balanced, terminated, twisted-pair transmission line up to 200 feet in length. Each circuit has two 2-way AND inputs. The remainder of the circuit is identical to card type C62 and the same ground rules apply.



Transmitter HA19

LEVEL TRANSLATOR
Card Type HA31

FUNCTION

The function of the circuits on this card is to perform a level-shifting action so that a 3600 receiver circuit can receive inputs from a 75-ohm coaxial line. A typical application is shown in the accompanying diagram.

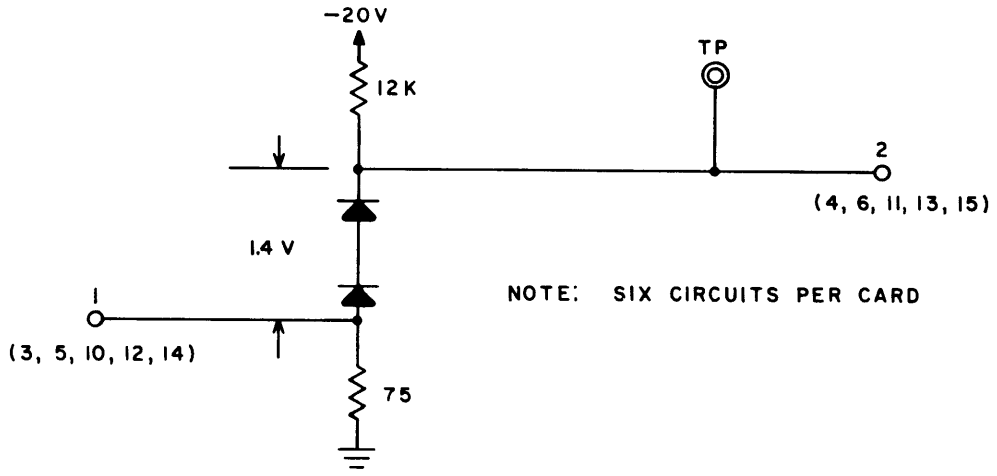
OPERATION

The card contains six identical circuits, as shown. The output of each circuit is held approximately 1.4 v negative with respect to the input.

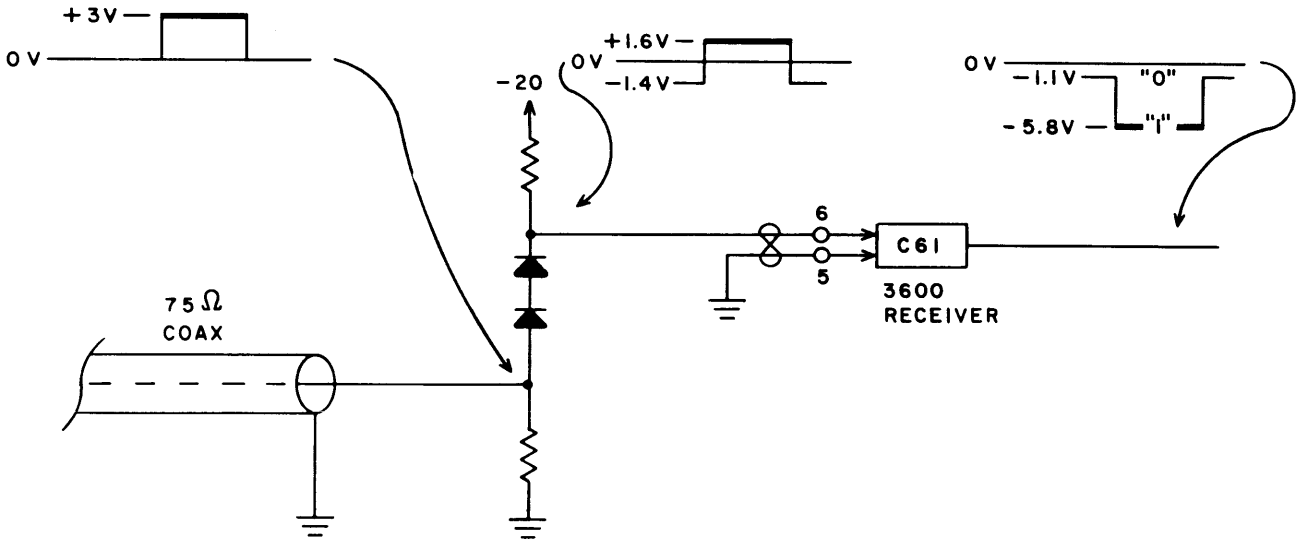
The level-shifting action is performed by two silicon diodes, each having a forward drop of approximately 0.7 v. These diodes also have a low dynamic impedance which will cause little attenuation of input signal current.

The purpose of the 75-ohm resistor is to provide impedance matching for the 75-ohm coaxial cable input.

SCHEMATIC



TYPICAL APPLICATION



Level Translator HA31

LINE DRIVER
Card Type HA32A

FUNCTION

The function of this card is to enable 3600 logic to interface with a disc file, as described in specification 118086. The circuit is designed so that, in the quiescent state with -1.1 v "0" inputs, all transistors are cut off and the circuit draws very little power. Upon receipt of a -5.8 v "1" input, all transistors switch to their conduction state and the circuit produces a positive going output.

The circuit will drive a signal a distance of 50 feet. The output from pin 2 can feed either a twisted pair with one line grounded or a 75-ohm coaxial line. By jumpering pins 1 and 2, approximately 70 ma of current may be provided for activating a reed relay.

OPERATION

The logic input to the circuit consists of two 4-way ANDs and two single-way ANDs. The circuit will be turned off only when all AND groups receive -1.1 v "0" inputs or are grounded. An open AND group or a -5.8 v "1" which satisfies the AND will activate the circuit.

Diodes CR16 and CR17 are silicon forward-drop devices, each of which has a constant forward drop of 0.7 v. They have a low dynamic impedance and are used to obtain an input level shift for transistor Q01.

A -1.1 v "0" input on each AND group results in all transistors being cut off. The level-shifting action of CR16 and CR17 attempts to bias Q01 well into the cut off region, however, the base of Q01 is clamped at about +0.7 v by diode CR18.

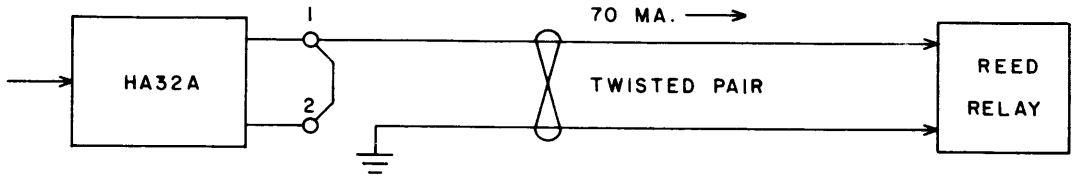
The collector voltage of Q01 rises to approximately -5.4 v, due to the voltage-divider action of R08, R09, R10, R11, and R12. The input at the base of Q02 will be about -3.4 v so that it is well into the cut off region. The input at the base of Q03 rises toward +20 v, however, its emitter is held at +19.3 v by the forward drop across CR20 so that Q03 is also cut off. In this state, the output impedance of the circuit is approximately 5,000 ohms, established by R17 and the output resistors.

A -5.8 v "1" input which satisfy one of the AND groups will cause all of the transistors to switch to their conduction state. This input voltage causes diodes CR16 and CR17 to place a strong forward bias on the base of Q01, causing it to conduct heavily. However, Q01 is held out of saturation by diode CR15 and its collector voltage stabilizes near -0.7 v.

The voltage-dividing action of R09, R11, and R12 provides forward drive for Q02. It is prevented from saturating by CR19. Transistor Q02 in its conduction state causes current flow through R16 to increase. The voltage drop across R16 is limited by the sum of the drops across CR20 and the emitter-base junction drop of Q03. A further increase in the collector current of Q02 will draw turn-on current through Q03, causing it to switch on and conduct heavily. This allows the -20 v source through CR20 and Q03 to produce an output at pins 1 and 2.

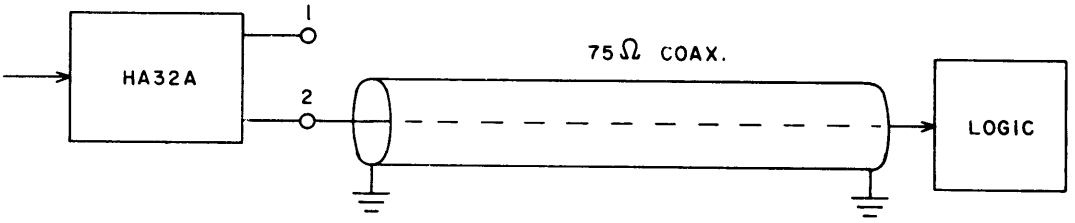
The 1000-ohm resistor R25 will prevent damage to Q03 and CR20 if the circuit test point is accidentally grounded.

TYPICAL APPLICATIONS



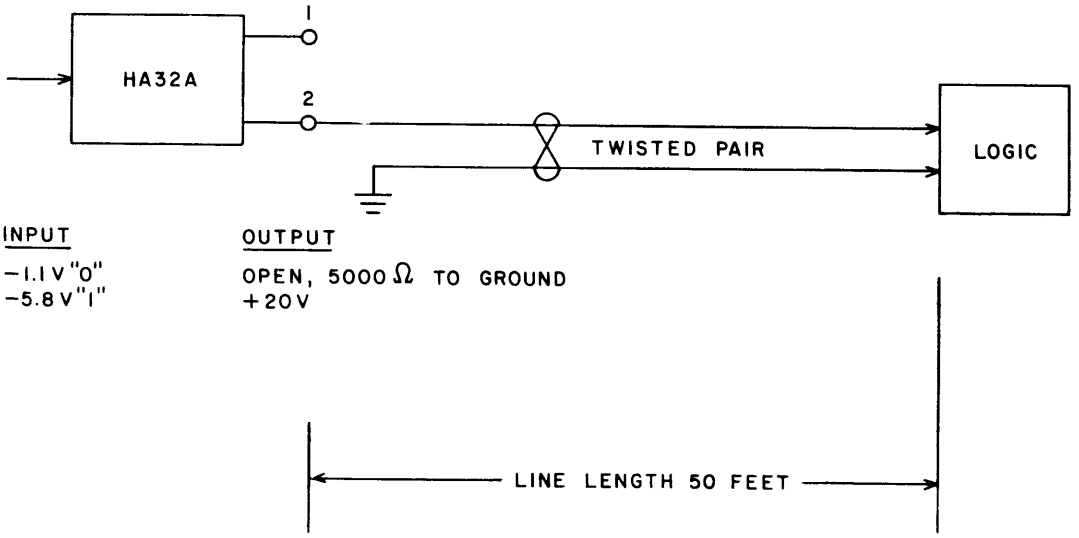
INPUT
−1.1 V "0"
−5.8 V "1"

OUTPUT
OPEN, 5000 Ω TO GROUND
70 MA. ≈ +9V



INPUT
−1.1 V "0"
−5.8 V "1"

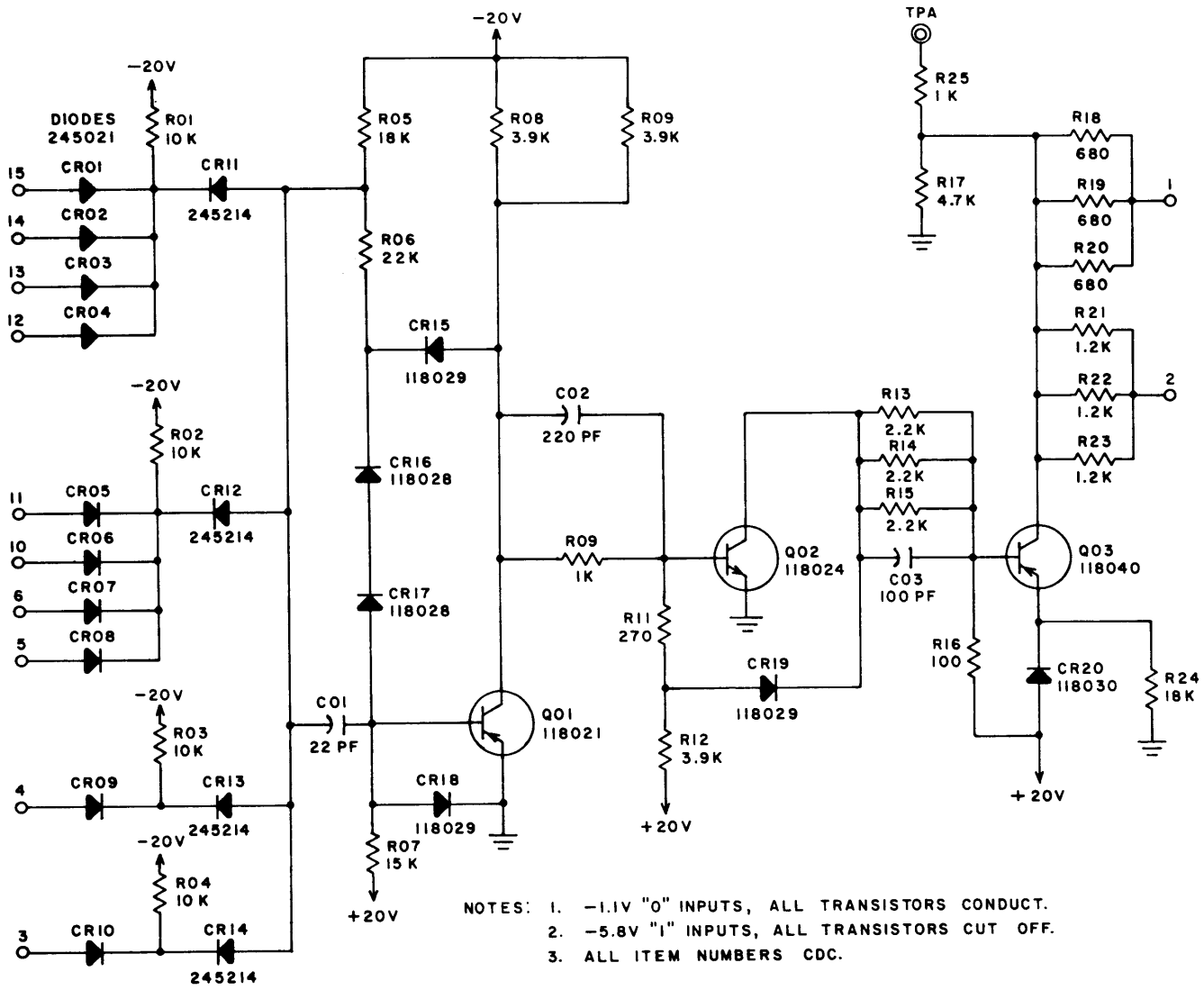
OUTPUT
OPEN, 5000 Ω TO GROUND
+20 V



INPUT
−1.1 V "0"
−5.8 V "1"

OUTPUT
OPEN, 5000 Ω TO GROUND
+20 V

Typical Applications



Line Driver HA32A

TRANSMITTER
(1000-foot line)
Card Types HA37 and HA43

GENERAL

The purpose of the long-line transmitter circuits is to increase the distance over which signals may be sent on a 3600-type transmission line. The standard transmitter cards (C62 and HA19) are restricted to driving 200-foot lines; by substituting card types HA37 and HA43, the line length may be increased to 1000 feet. This feature will allow peripheral equipment to be installed in locations remote from the computer system.

The circuits on card types HA37 and HA43 are identical; the difference lies in their input configurations. The circuits on card type HA37 each have a 3-way AND input, the same as card type C62. The circuits on card type HA43 each have two 2-way AND inputs, the same as card type HA19.

The long-line system is d-c coupled, similar to the standard system. A limit of 1000 feet has been placed on the system to minimize changes required in standard hardware and because of limitations due to data transmission characteristics.

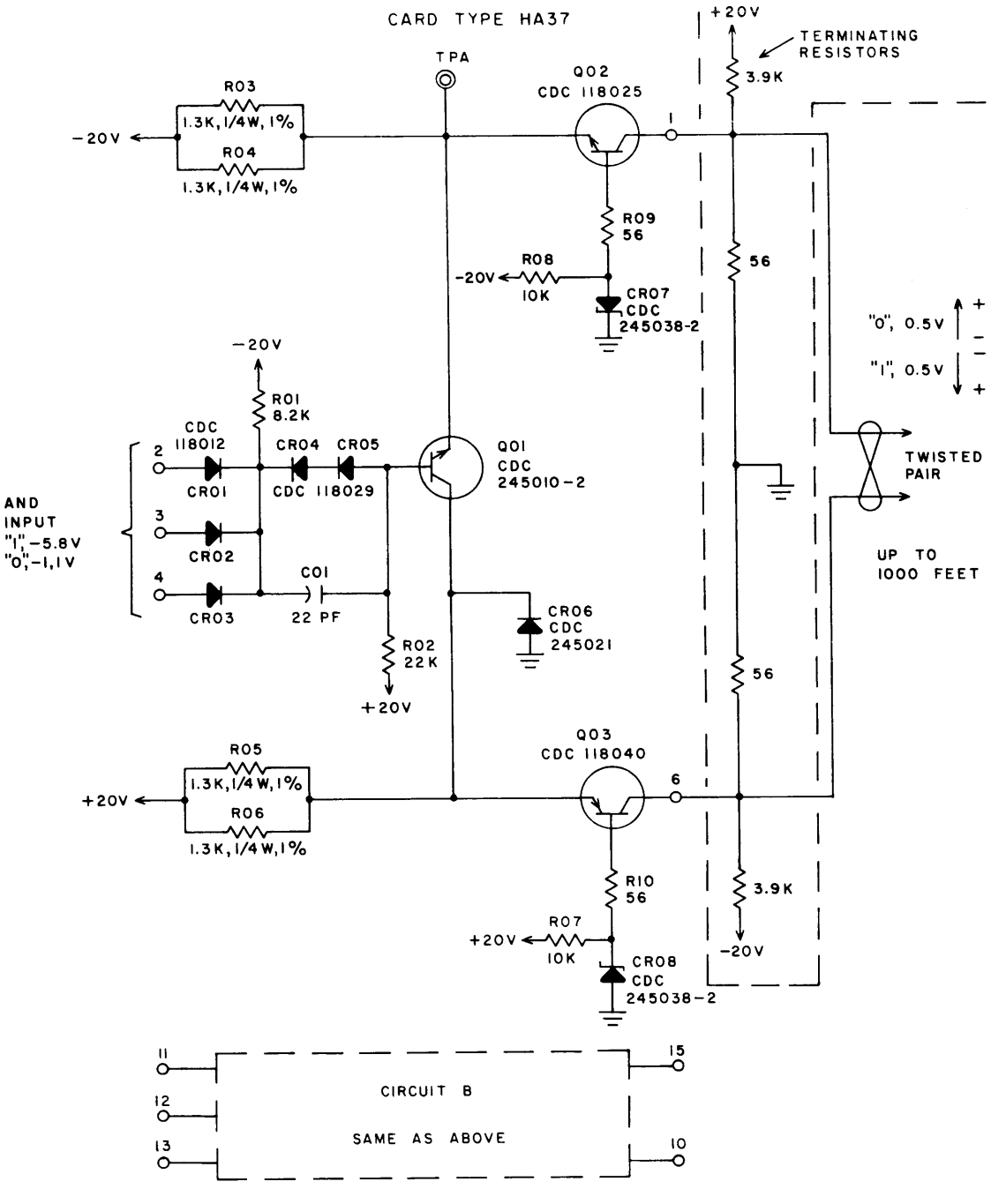
OPERATION

The long line transmitter circuit is identical in operation to the standard 3600-type transmitter. The major differences in the two circuits are the higher power capability of the HA37 and HA43 cards, and changes in specifications of some of the components.

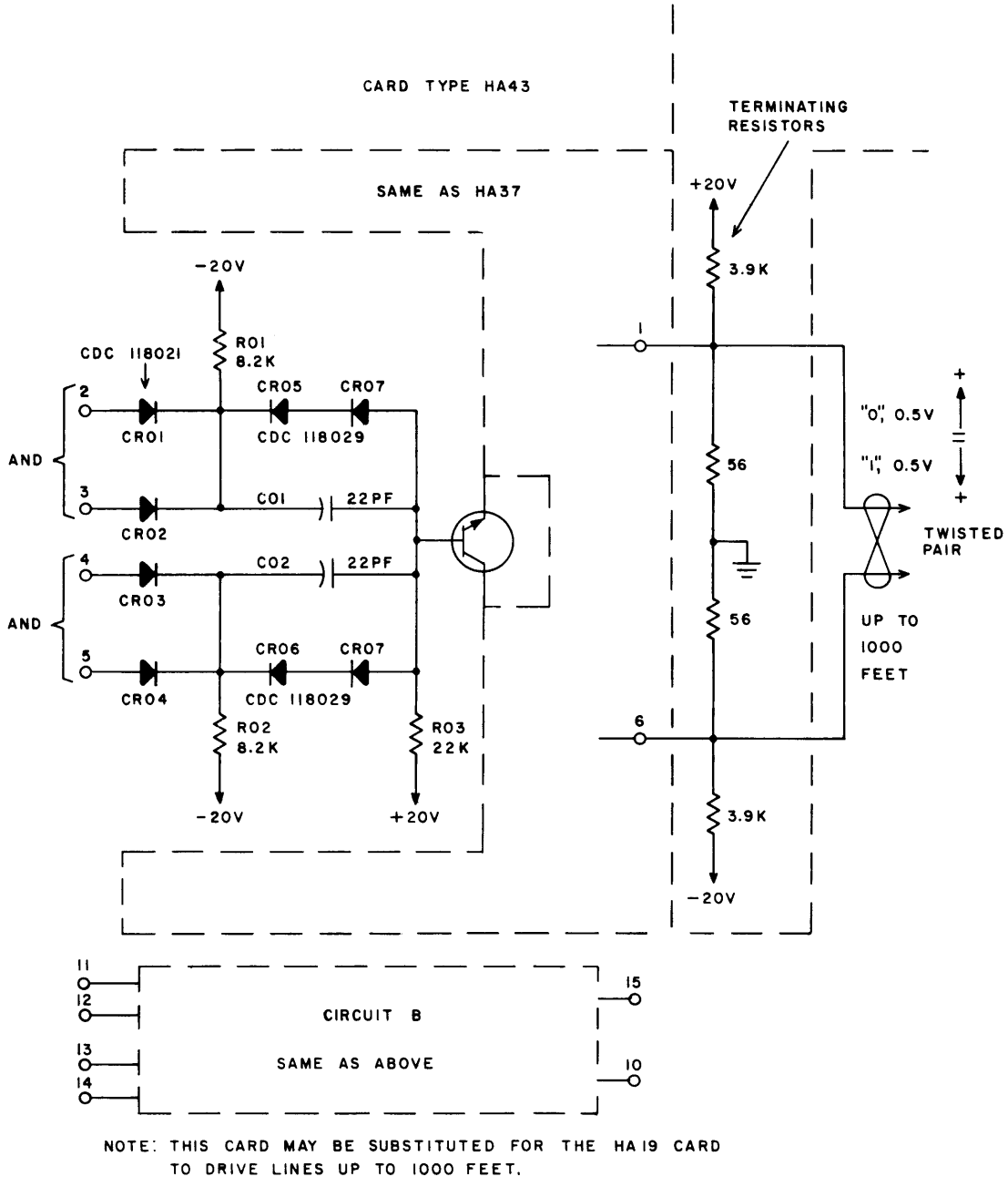
Each circuit card contains two circuits designated A and B, as shown in the accompanying diagram. The input consists of a 3-way AND on HA37 cards, and two 2-way AND's on HA43 cards. The output of a standard logic logic card constitutes a proper input to a transmitter. A logical "1" input causes transistor Q01 to turn off and Q02 and Q03 to turn on, while a "0" input has the opposite effect.

A -1.1v "0" input causes the emitter-base junction to Q01 to be forward biased, turning Q01 fully on. When Q01 is turned on, a shunt path for current is provided around Q02 and Q03. Since Q02 and Q03 no longer have a source of current, no current is injected into the transmission line.

When the "AND" input is satisifed, the base of Q01 will be held at approximately -5 volts. This reverse-biases the emitter-base junction by approximately 3 volts and causes Q01



NOTE: THIS CARD MAY BE SUBSTITUTED FOR THE C62 CARD, TO DRIVE LINES UP TO 1000 FEET.



NOTE: THIS CARD MAY BE SUBSTITUTED FOR THE HA19 CARD TO DRIVE LINES UP TO 1000 FEET.

Transmitter HA43

to be turned off. Since the shunt path for current around Q02 and Q03 no longer exists, they become constant current generators of opposite polarities. Q03 injects a current of approximately 26 ma into the line and a like amount of current flows out of the line into Q02.

The base networks of Q02 and Q03 each contains a 3.45v zener diode which performs two functions. In the first case, the zener diode sets the voltage level at which the emitters of Q02 and Q03 will reach their turned-on state. This, in turn, sets the threshold that must be overcome at the base of Q01, since its emitter is at the same potential as the emitter of Q02. In the second case, the zener diodes set the base voltages of Q02 and Q03 which determine how much noise voltage will be allowed at the collectors before the collector-base junctions become forward biased. This value of noise voltage is something over 3.28 volts, since the forward drop of the collector-base junctions adds to the zener diode voltage. This means that the transmitter will operate satisfactorily with more than 3 volts of random noise on the transmission line.

RECEIVER CIRCUIT

The receiver is the standard type C61 or HA11, which are described elsewhere in this manual.

CABLE

The signal cable is standard 3600-type, containing 29 twisted-pair transmission lines. Each transmission line consists of two 24-gauge conductors. If required, a cable with a protective copper braid shield may be used to protect against extreme electrical noise and other environmental hazards.

LINE TERMINATIONS

Line terminations are standard 3600-type signal cable terminators.

GROUND RULES

1. Installation:
   a. To convert an interface from a 200-foot cable length limitation to 1000-foot capability, all CA62B cards must be replaced with HA37 cards and all HA19 cards must be replaced with HA43 cards.
   b. Receiver cards remain unchanged.
   c. Transmission line terminations remain unchanged.

2. Each long line transmitter card requires approximately 1/3 watt more power than a standard transmitter card. The additional power is divided equally between the +20v and -20v supplies.

3. A maximum of 16 long line transmitters and 16 standard receivers may be distributed along a 1000-foot transmission line.

4. At a distance of 1000 feet, the output waveform of the receiver will be symmetrical for switching rates up to 500 kc. Switching rates in excess of 500 kc will result in degradation of symmetry. For distances of less than 200 feet, switching rates are similar to a standard transmitter-receiver system.

5. The balanced system using differential receiving techniques allows a difference in noise levels of up to 3 volts between the transmitter ground reference and the receiver ground reference. To avoid problems of noise pickup, it is recommended that the terminators on all remote equipments be energized from the common 40v supply, with an earth ground reference level. Decisions regarding the possible use of other terminator power and ground connections are the responsibility of the design engineer.

6. When driving signals through a 1000-foot cable, total delay time between input to the transmitter and output from the receiver will be approximately 2 micro-sec.

7. A signal de-skewing delay of 300 nanoseconds must be allowed for parallel transmission of 12 data bits over distances from 600 to 1000 feet.

DELAY AND SKEW ON A 1000-FOOT CABLE

When changing from a line driver system with a maximum distance of 200 feet to a system with a maximum distance of 1000 feet, the following changes must be made and new characteristics observed:

1. For distances from 600 to 1000 feet, the control signal (Data Signal, Reply, etc.) deskewing delay must be increased from 100 to 200 nanoseconds.

Data Channel - Peripheral Device Delays

Normal Operation

The data channel allows 100 nanoseconds for Data Signal deskewing. This is active during both Read and Write operations. During a Write operation, the peripheral device must allow Data Signal delay for parity checking.

During a Read operation, the peripheral device delays the Reply for 200 nanoseconds to allow for signal deskewing and data channel parity checking.

Recommended Modifications for 200 Nanosecond Deskewing Delay

Modification should be done at the peripheral device, which would normally be the remote site. During a Write operation, the Data Signal should be delayed 100 nanoseconds at the peripheral device in addition to the parity checking delay. During a Read operation, the Reply delay should be increased by 100 nanoseconds to 300 nanoseconds to allow for signal deskewing and data channel parity checking.

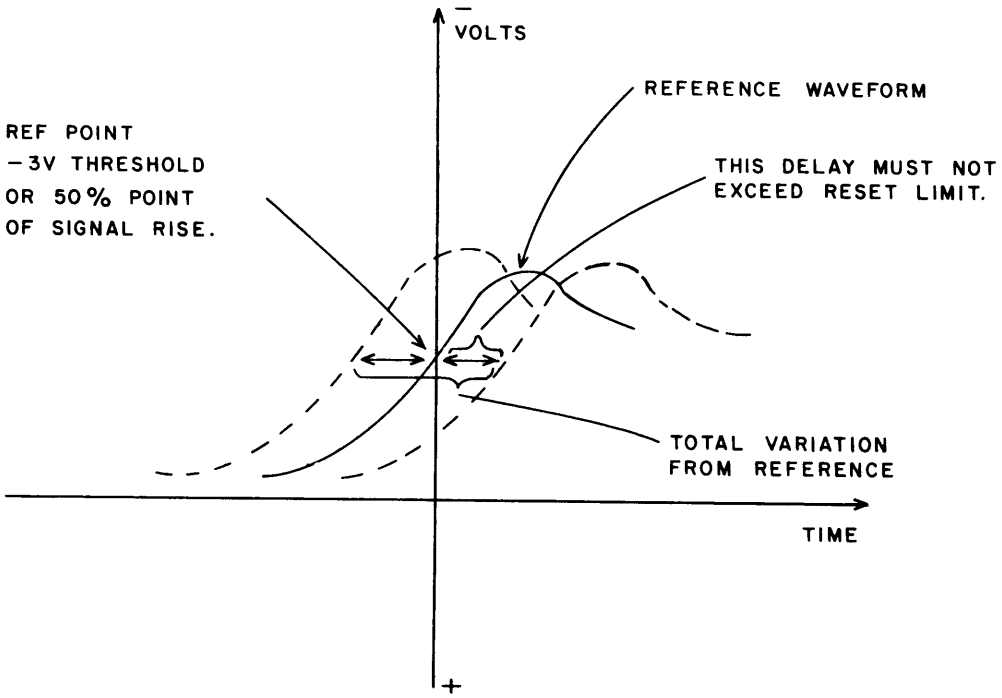
No attempt will be made to specify how the added delay should be inserted. The delay may be added in a manner most feasible for the device involved.

2. If normal operation does not occur, the following tests should be conducted:

   A. Check for required signal outputs from the transmitters (H37 card output) and receiver circuits (C61 card output). If no signal is received, check transmitter and receiver circuits; check line termination and voltages. If no problem appears to exist at this point, proceed to step B.

   B. From information on the logic of the connected equipment, find cases where the data or signal code lines are sampled within a certain period after the control signal is received. If the delay is preset, for example, at 100 nanoseconds, test if the delay period is at least 100 nanoseconds. Preset delay shall not be less than 100 nanoseconds. Synchronize an oscilloscope on the output of the control line receiver and observe the variation of the receiver outputs of the data or code lines with respect to the control line reference. The reference point may be considered as the -3 volt threshold point or 50% of the risetime point of 3600 logic.

In pictorial form, risetime variation may be sketched as follows:



The delay of the signal risetime of any data or code line must not exceed the preset 100 or 200 nanoseconds, whichever the case may be. Where required, fall time going from a "1" to a "0" signal may be tested in a similar manner. If the delay does not fall within the preset time, check for: (1) bad receiver card, bad components, etc. (2) bad wiring connection (3) improper line termination or termination voltages.

C. Check the system logic for Data Signal-Reply operation. The propagation time becomes an important factor in this situation. For example, assume device A has a Data Signal up and the remote site responds with a Reply. Device A drops the Data Signal in response to the Reply. The Reply is dropped at the remote site. Device A cannot bring up the next Data Signal until the dropping of the Reply at the remote site is recognized at Device A. Otherwise, Device A may accept the Reply from the previous word transfer and the information will be lost.

D. Connect and Disconnect Delay. For a system in which a data channel is communicating with peripheral equipments via 1000 feet of cable, the equipments must be modified so that the selected equipment will not return a Reply earlier than 3 usec after receiving the Connect signal.

TIME VARIATIONS DUE TO CABLE DELAY

A significant amount of time is lost in transmission of signals through cables. The following is an itemized list of approximate time lag in a 3600 system over a 1000-foot cable.

1.	Transmit Data Signal and data from data channel to peripheral device plus Data Signal delay	2,100 nano.
2.	Response time of peripheral device, i.e., examine parity, bring up Reply, and control signal delay	400 nano.
3.	Send Reply to data channel	2,000 nano.
4.	From dropping of Data Signal until data channel senses dropping of Reply.	4,000 nano.
5.	Memory reference time between 48-bit words	1,500 nano.
		10,000 nano.

$$\frac{1.0}{10.0 \times 10^{-6}} = .100 \times 10^{6}$$

100 KC word rate

200 KC character rate

worst case with 60 usec. memory reference time

$$\begin{array}{r} 8.5 \text{ usec.} \\ +\ 60 \text{ usec.} \\ \hline 68.5 \text{ usec.} \end{array}$$

$$\frac{1.00}{68.5 \times 10^{-6}} = .0146 \times 10^{6}$$

14.6 KC word rate

29.9 KC character rate

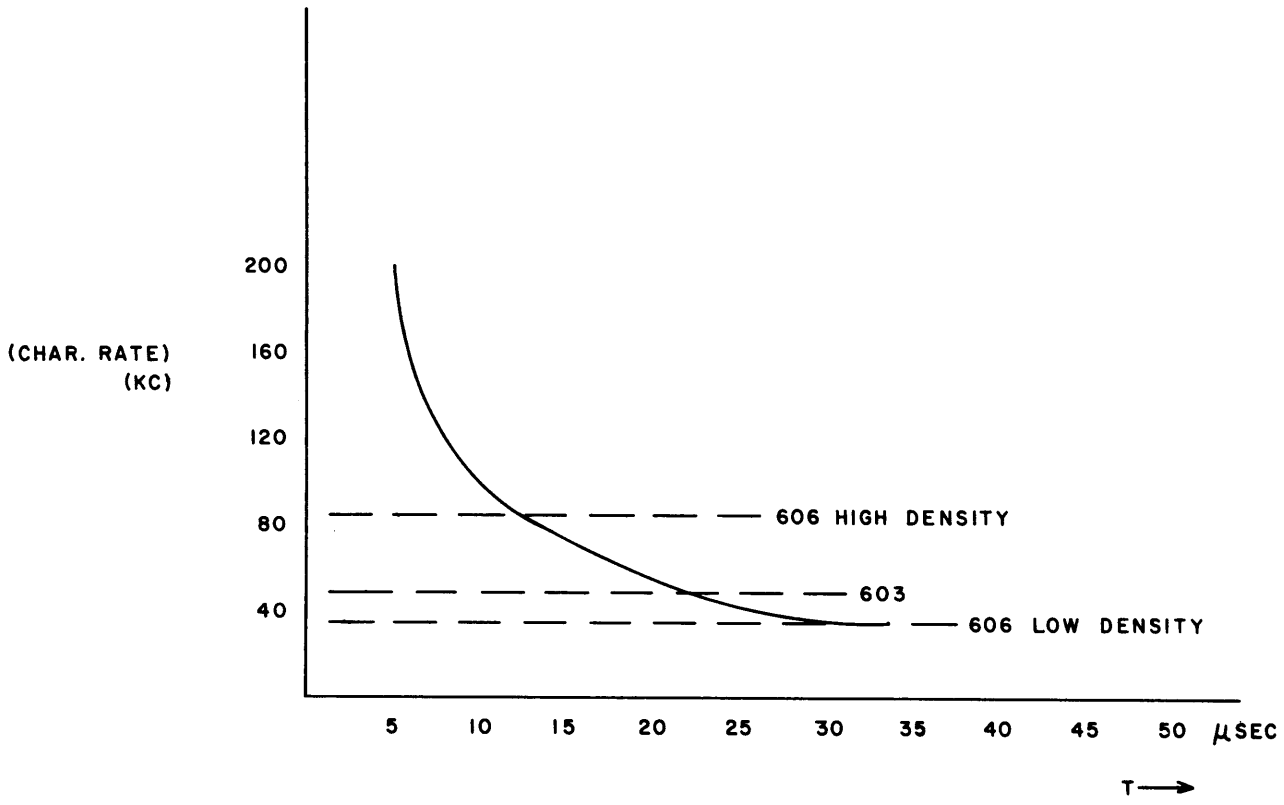
Read Delay (See accompanying diagram)

1. Same as for write (1).
2. This time is dependent on peripheral device speed.
3. 200 nanoseconds required with 200 to 1000 foot cable.
4. 100 nanoseconds for parity generation and checking.
5. Same as (1).

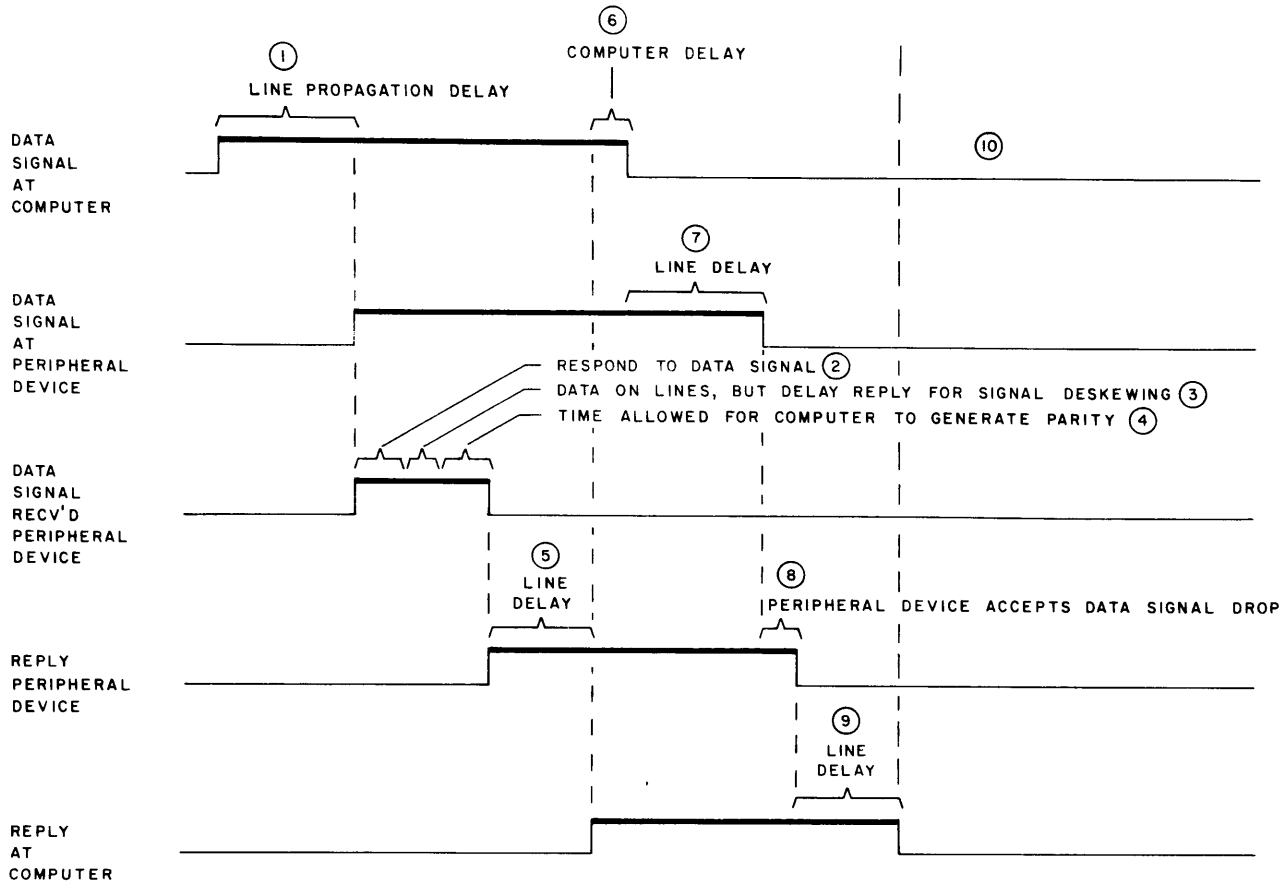
6. Computer responds to Reply, samples lines and drops Data Signal, (100 nanoseconds for 3606 data channel).
7. Same as (1).
8. Peripheral device responds to Data Signal drop and drops Reply.
9. Same as (1).
10. The next Data Signal can be transmitted and the computer can accept a Reply/ Reject signal only after time (9) is completed.

Write Delay (See accompanying diagram)

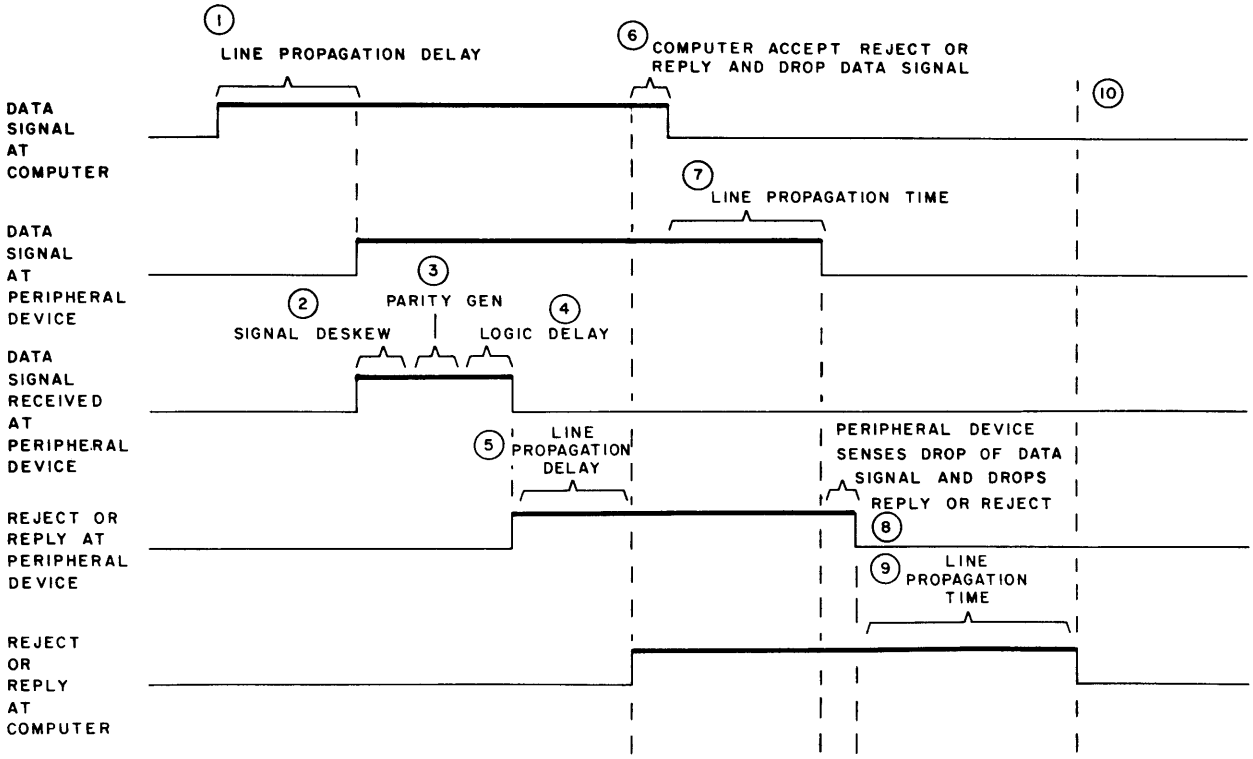
1. Line, transmitter and receiver card delay (approx. 2 usec. per 1000 feet).
2. Signal deskew allows the data lines to stabilize prior to sampling. (200 nanoseconds required for 1000 feet). The 3606 data channel inserts 100 nanoseconds of the required 200 nanoseconds.
3. Parity generated from data and checked against received parity bit.
4. Logic delay for decision making -- such as examine data and send Reply or Reject. This delay must be 3 usec. on a Connect operation to allow all peripheral devices to disconnect if the connect code does not pertain to that device.
5. Same as 1.
6. Computer accepts Reject or Reply and drops Data Signal. (The 3606 data channel allows 100 nanoseconds).
7. Same as 1.
8. Dependent on peripheral device.
9. Same as 1.
10. The next Data Signal can be transmitted and the computer can accept a Reject or Reply signal only after time (9) is completed.



APPROXIMATE CHARACTER SPEED FOR
3600 COMPUTER I/O OPERATIONS



DELAYS DURING READ OPERATION



DELAY DURING WRITE OPERATION

TRANSMITTER AND RECEIVER
Card Types P14C and P16A

FUNCTION

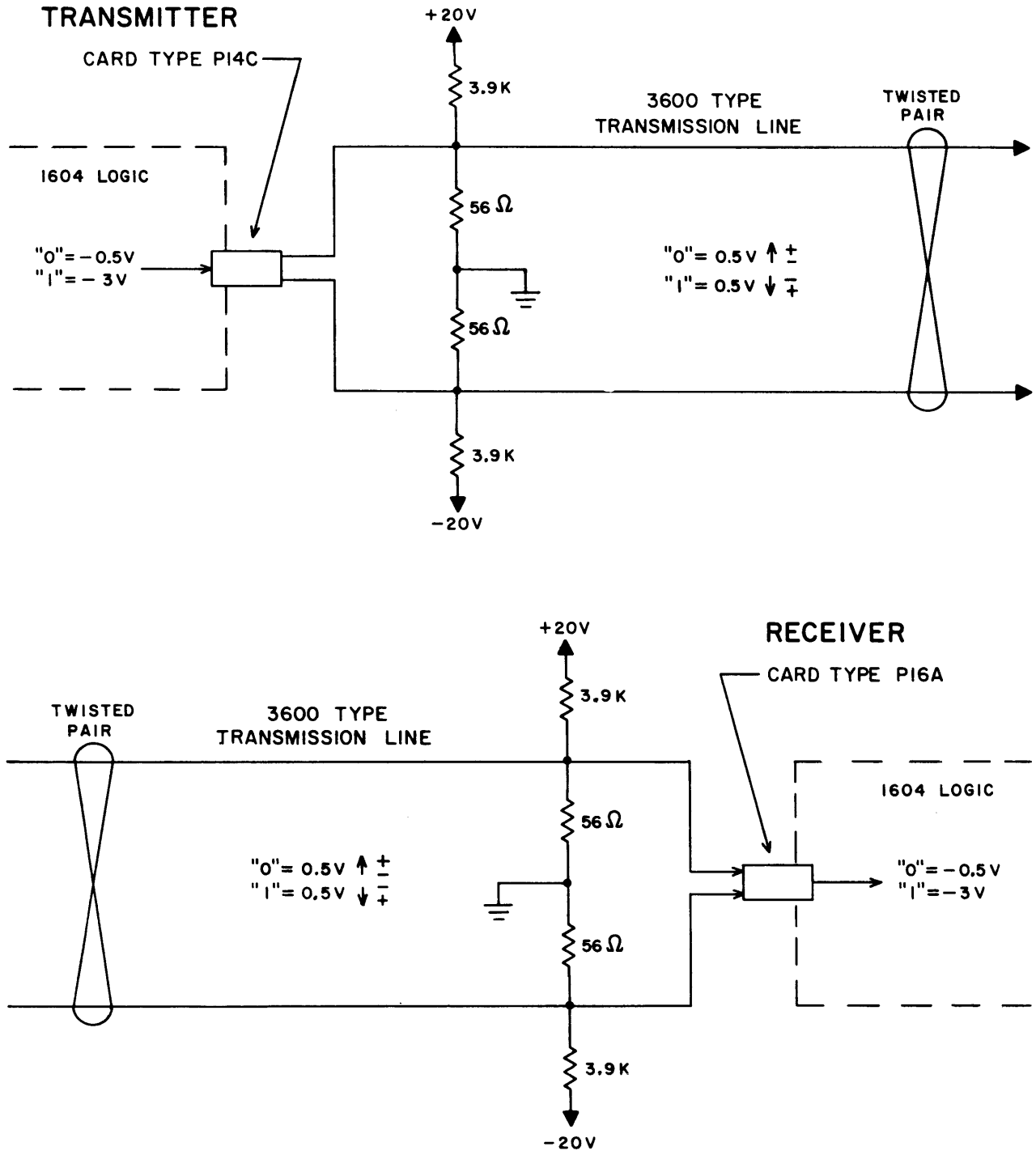
These circuits enable equipment containing 1604 logic to receive and transmit via a 3600 type I/O cable. This is accomplished by converting the 3600 transmission line signal levels of 0.5v line-to-line to the 1604 logic levels of "1" = -3v and "0" = -0.5v. Card types P14C and P16A have the same capabilities and impedance characteristics as 3600 type transmitters and receivers. Both types of transmitters and receivers may use the same transmission line.

OPERATION

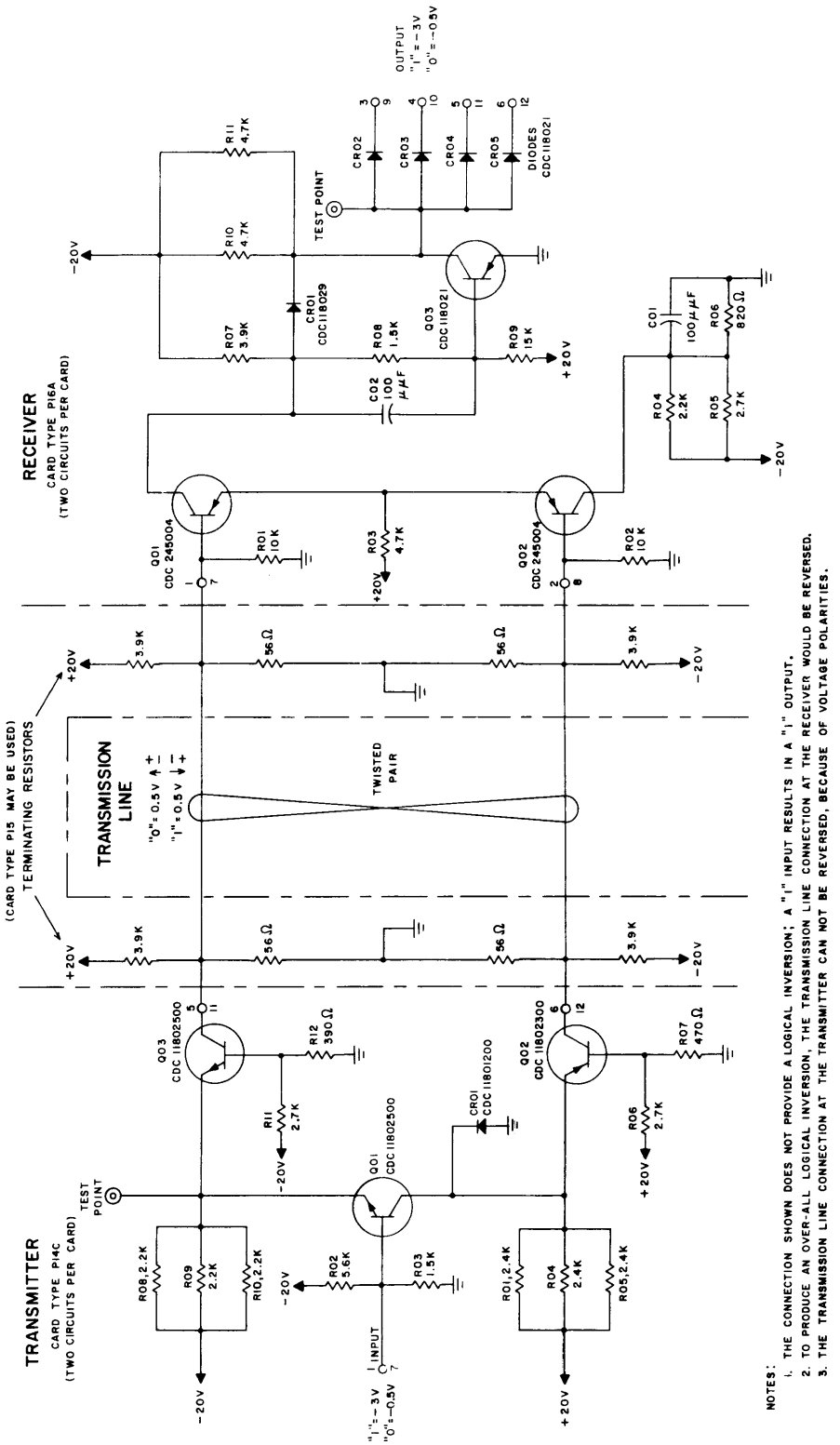
The transmitter, card type P14C, is similar to the C62A, which is discussed elsewhere. It converts single-ended inputs into double-ended outputs suitable for driving a balanced, terminated, twisted-pair transmission line. A -3v "1" input to transistor Q01 causes Q02 and Q03 to inject a current of about 20 ma into the transmission line. This results in a full line-to-line voltage reversal.

The "0" line signal level is established by the flow of bias current through the terminating resistors. In order to obtain proper voltage polarities, the transmitter must be connected to the line as shown.

The receiver, card type P16A, is similar to the C61B, which is discussed elsewhere. It functions both as a differential amplifier and as a discriminator, providing logic outputs of -3v "1" or -0.5v "0" according to the polarity of the 0.5v signal received from the transmission line. The transmitter and receiver combination can be made to provide a logical inversion by reversing the transmission line connections at the receiver.



Transmitter P14C and
Receiver P16A

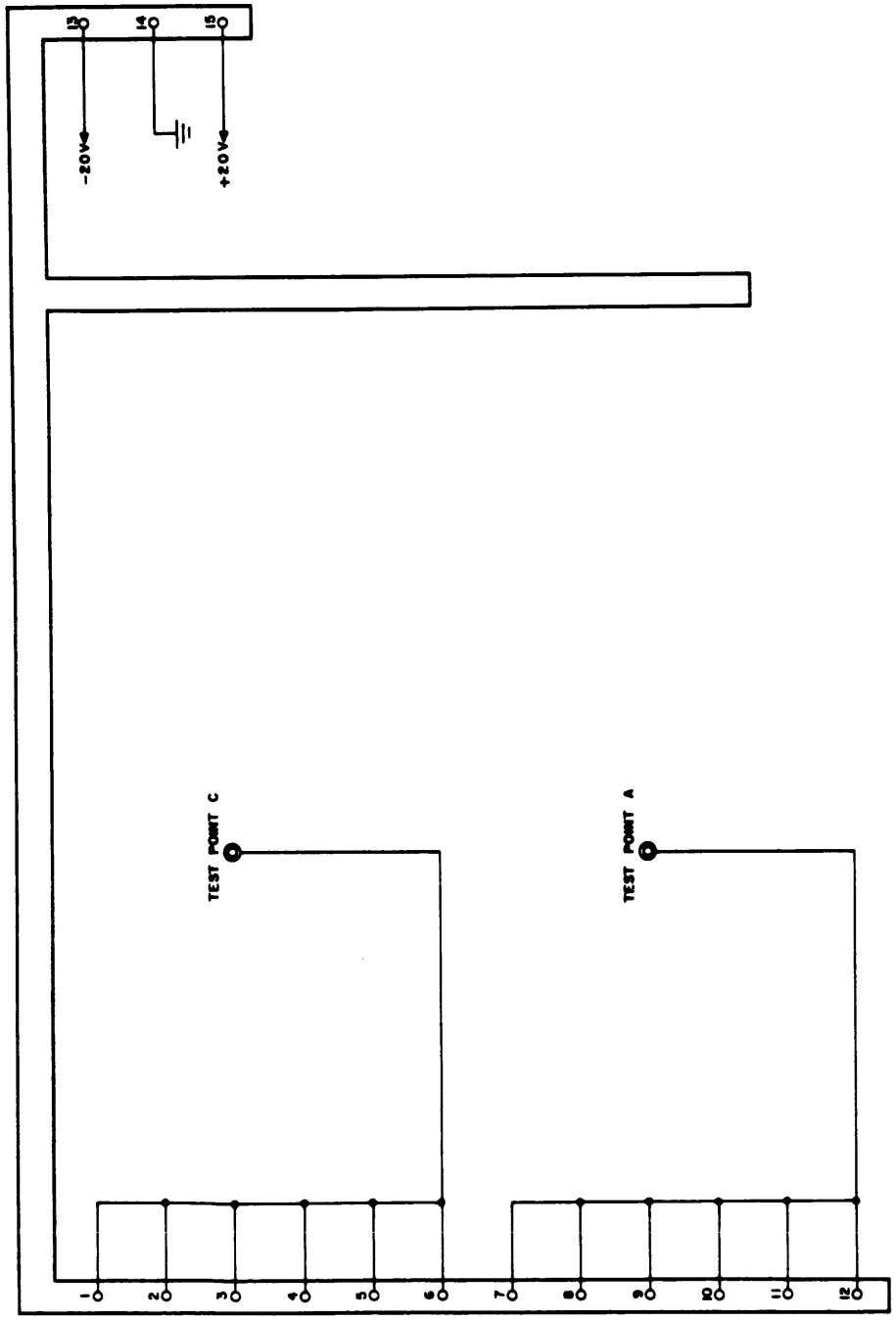


Transmitter P14C
Transmission Line and Receiver P16A

CLOCK DISCONNECT

Card Type 00

The clock disconnect is a jumper type card which synchronizes pulses from three 1604-type clock cards by connecting their tanks in parallel. It has no active components. This card should be removed when clock cards are being tested in order that they may be tested individually.

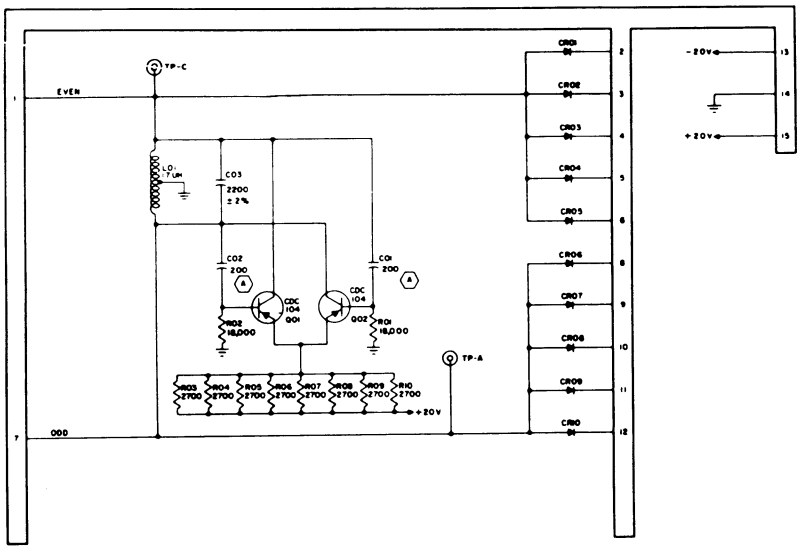


Clock Disconnect 00

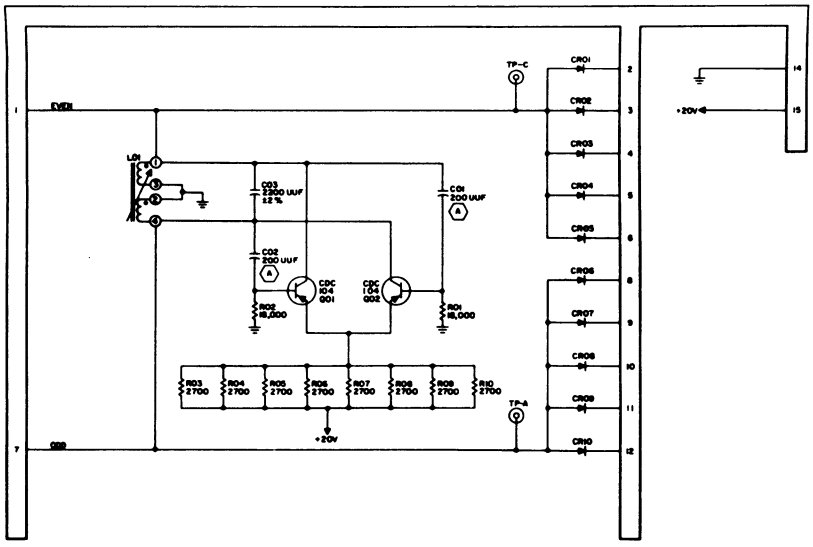
CHAPTER 5. SPECIAL PURPOSE CARDS

Clock Disconnect	00
Oscillator	01, 01A, 02A
Oscillator Amplifier	06
Capacitor	50
Speaker Driver	65
Punch Puller	66
Read Amplifier	70B
Delay Capacitors	73, 73A, 77, 82
Reader Level Amplifier	75, 75A
Reader Brake-Clutch Driver	76A
Punch Puller	86
Hammer Storage	91
Delay	97A
Clock Oscillator-Amplifier	C01
Clamp	C02
Emitter Follower	C07C
Delay Line Driver	C08
Switch	C60A
Resync Circuit	C64A, C65A, C66A
Capacitive Delay	C67, K67, C68, C69, C70C, C71, K71
Priority Circuit	C77, C78B, C79A
Delay Line, 1 usec	C80
Crystal Oscillator	C81, C82, C83
Relay Driver	C84
Strobe Shaper	C85
Amplifier-Shaper	C89
Reader Level Amplifier	C91
Overload Protector	C94
Channel Disable	C97
Jumper	E00
Crosspoint Module	E01A, E02A
Crosspoint Crosspoint Module	E03A, E04A
Decoder	E05
Terminator	E06, E07

Single Pulser	E08
Integrator	E10
Delay	E11
Variable Clock	E14
Terminator	E19
Resistor Assembly	E20
Console Interface	H10A
Delay Line Amplifier	H12
Filter	H17
Light Driver	H20
Keyboard Translator	H27, H28
Delay Line, 0.1 usec	H35
Diode	H38
Line Terminator	H39
Delay, Inductive, 0.15 usec	P13A
Power Supply Filter & Jumper	P54
Power Supply Filter & Jumper	P55
Hammer Driver	P91, P92
Pulse Shaper	P93
Ribbon Advance	P94
Brake-Clutch One-Shot	P95, P99
Ribbon Drive and Hold	P96
Hammer Driver One-Shot	P97



Oscillator 01A



Oscillator 02A

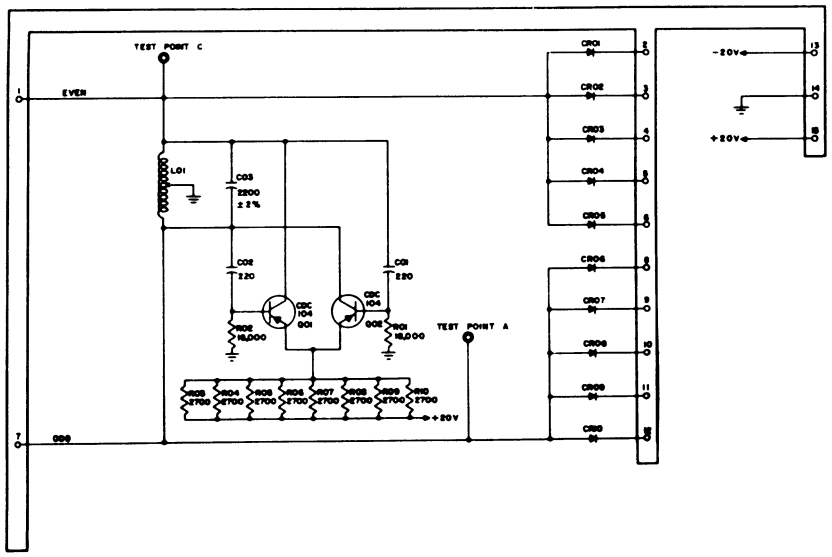
OSCILLATOR

Card Types 01, 01A, and 02A

Oscillator cards provide odd and even clock pulses, which provide timing for certain operations, at a nominal frequency of 2.5 megacycles. The circuits of the three cards are similar.

These oscillator cards contain a tank circuit which feeds the multivibrator, consisting of transistors Q01 and Q02. To provide odd and even pulses, the collector of one transistor is tied to the base of the other. When transistor Q01 is conducting, transistor Q02 is cut off; and when Q02 is conducting, Q01 is cut off.

02A differs slightly from 01 and 01A in that it has an adjustable inductor (L01).

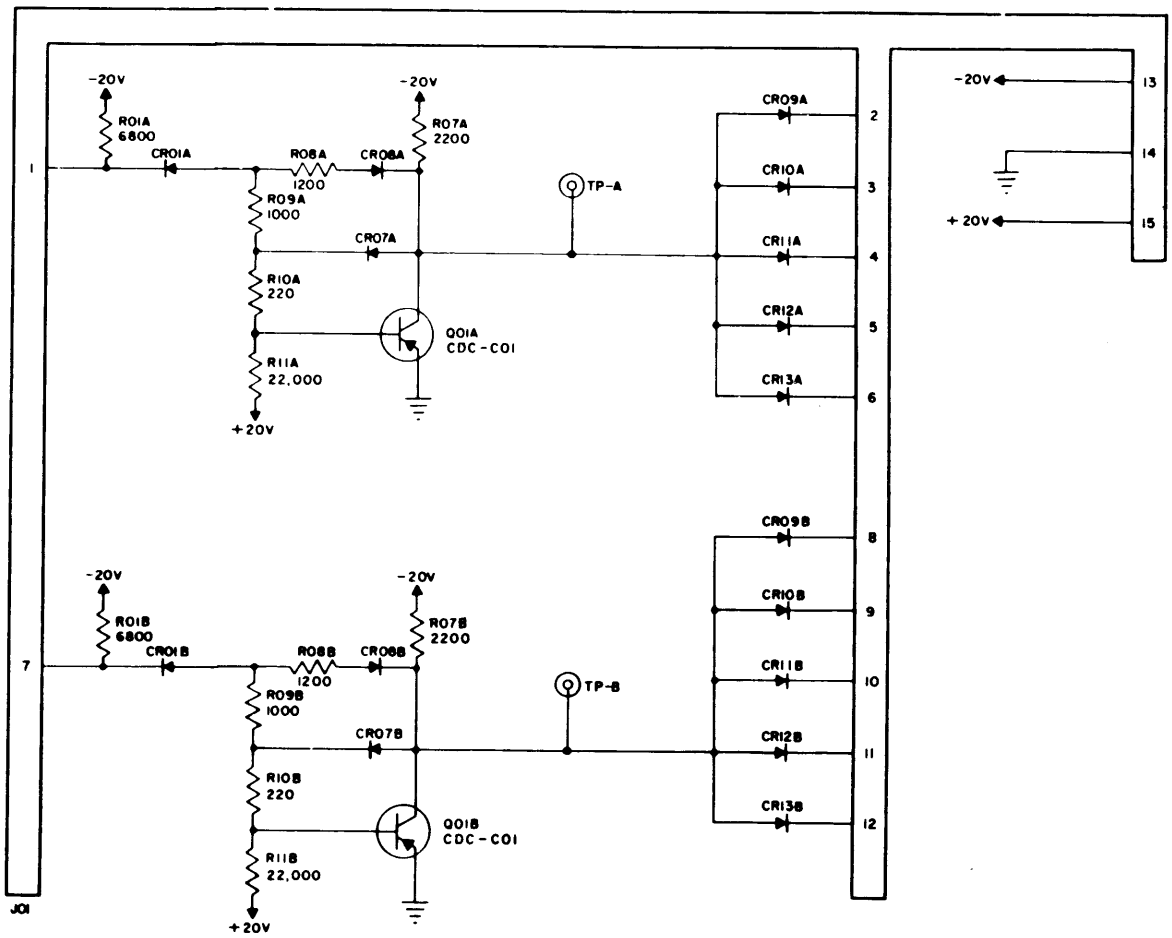


Oscillator 01

OSCILLATOR AMPLIFIER

Card Type 06

An oscillator amplifier consists of two 1604-type inverter circuits. Except for the type of transistors, it is identical to card type 21A.

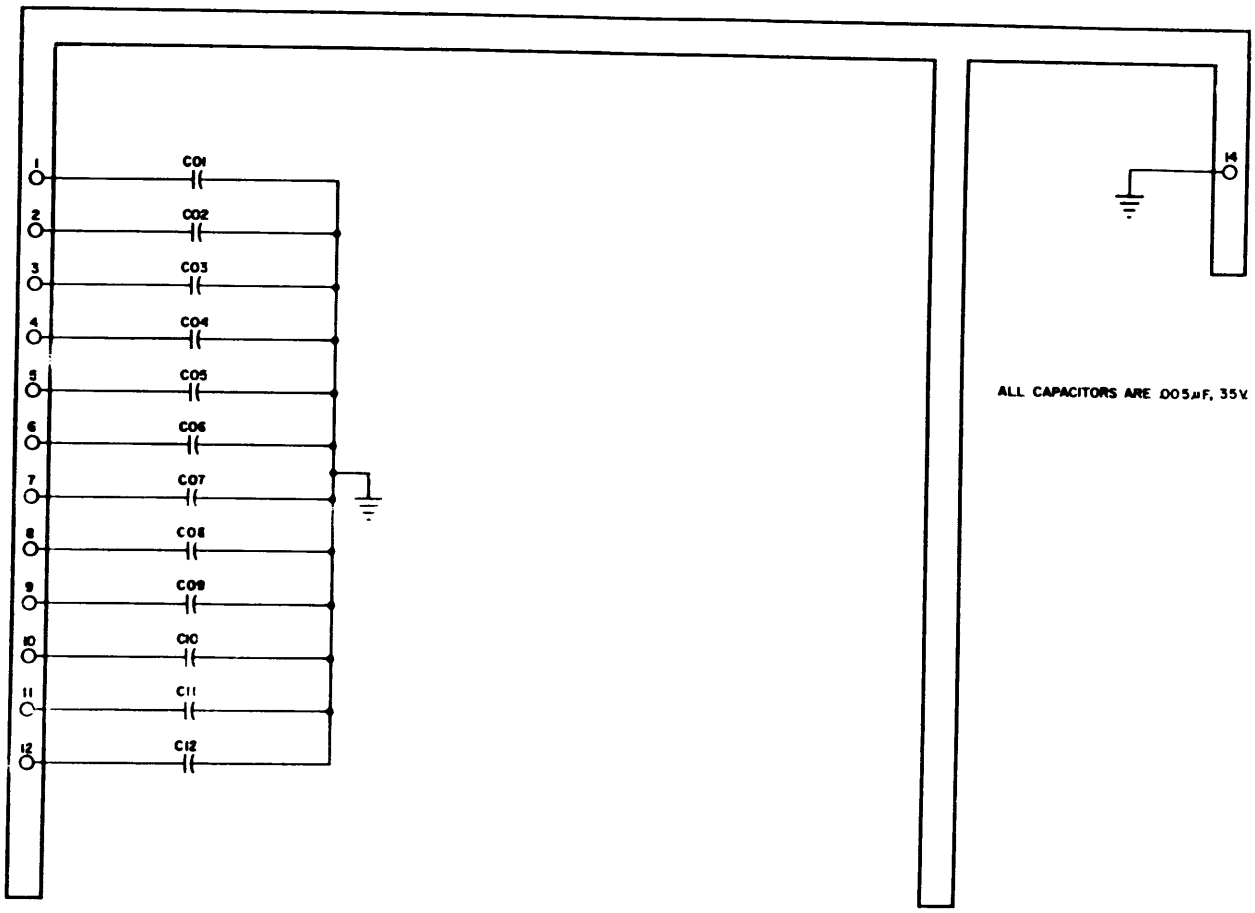


Oscillator Amplifier 06

CAPACITOR

Card Type 50

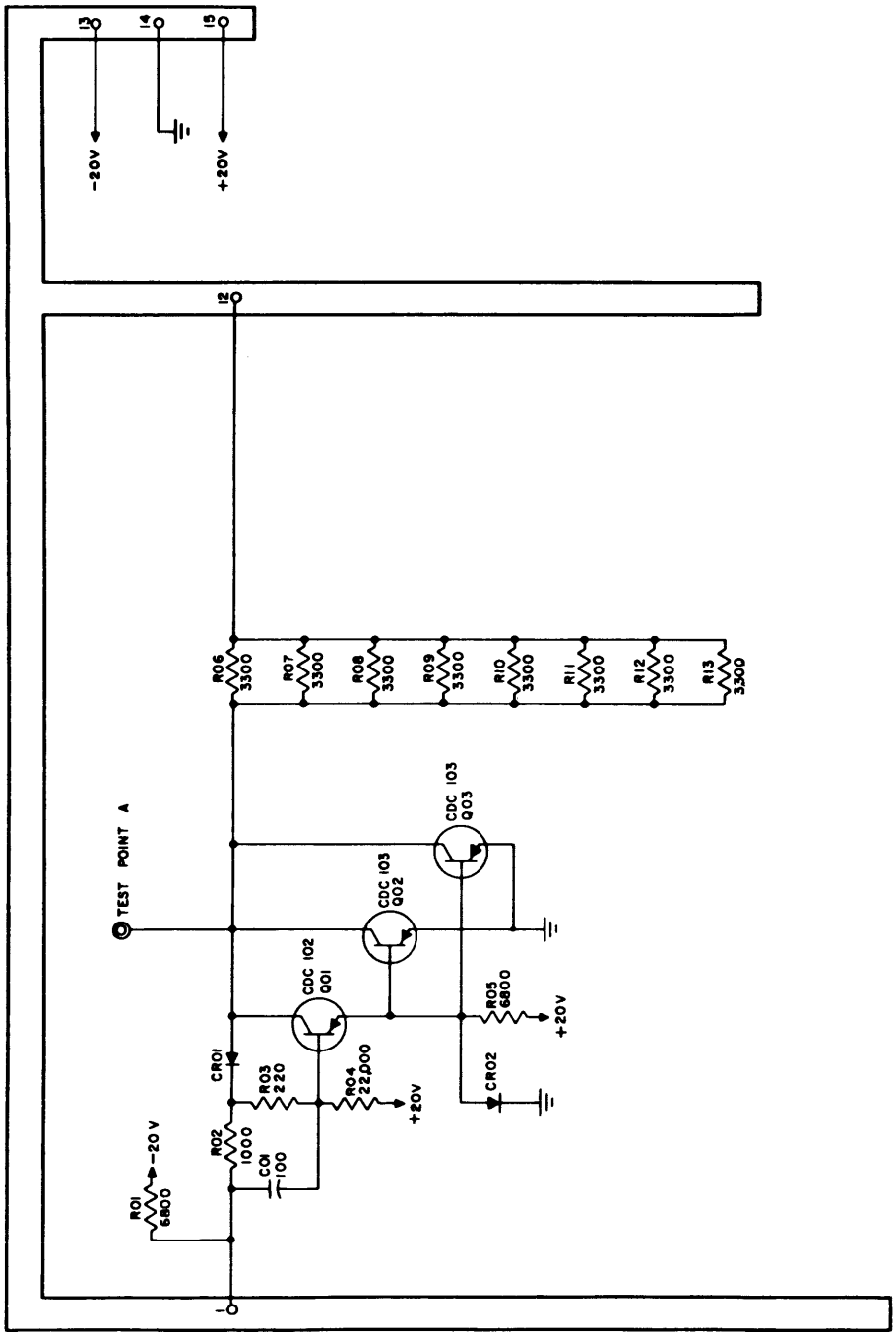
This card contains twelve 0.005 uf, 35v capacitors. It may be used as a delay or as a filter.



SPEAKER DRIVER
Card Type 65

Card type 65 is used to drive a speaker with a low-impedance coil.

The speaker driver has a two stage circuit, input and output. The input stage consists of an inverter which feeds the output stage. The output stage consists of two transistors (Q02 and Q03) which are operated in parallel to protect the transistors and minimize power dissipation. The resultant resistance of the input of the speaker and the resistor bank (consisting of R06, R07, R08, R09, R10, R11, R12, R13) is approximately 400 to 500 ohms. An input of -3v "1" at pin 1 causes sufficient current generation to activate the speaker.



Speaker Driver 65

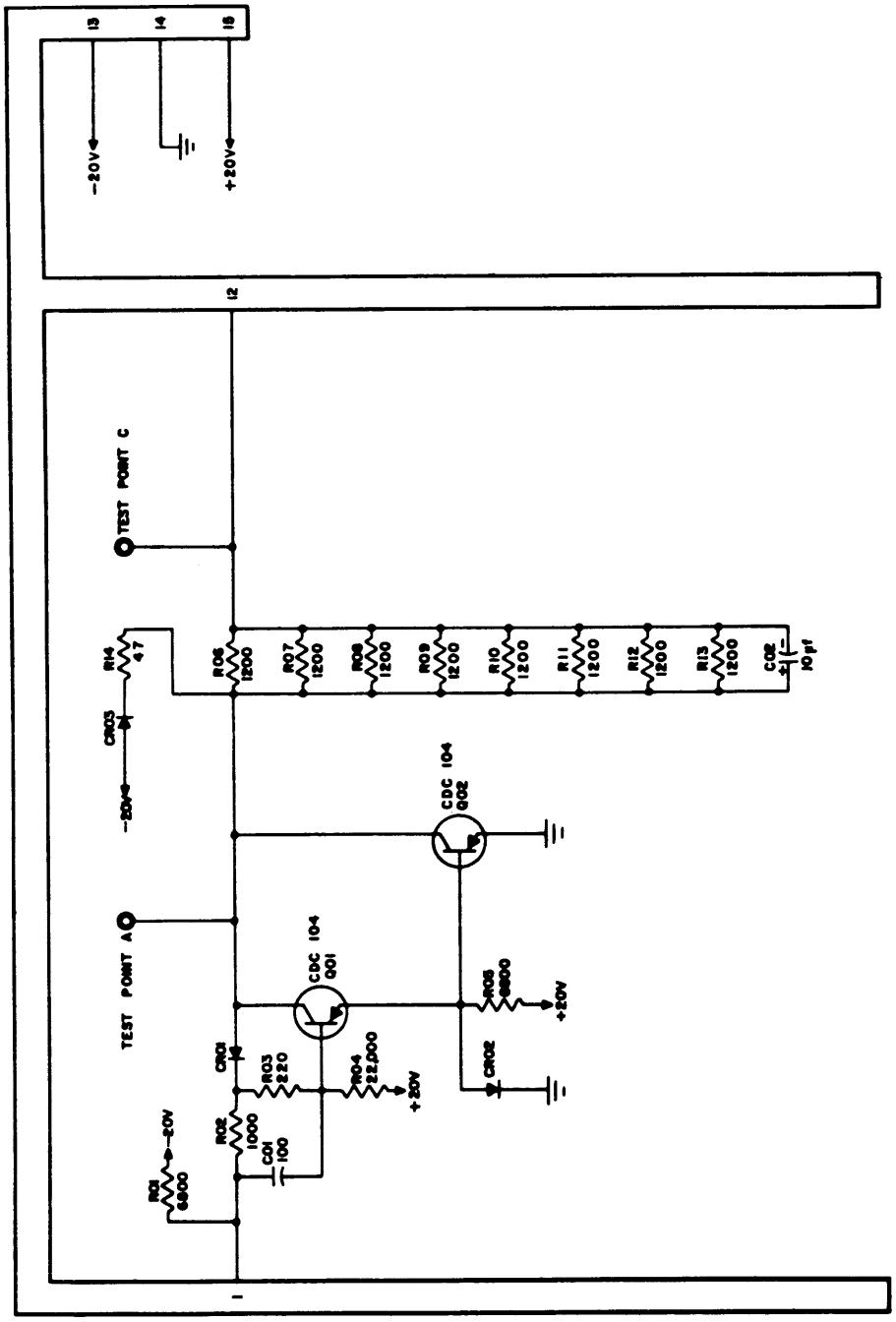
PUNCH PULLER

Card Type 66

This card is designed to handle a current of the order of 100 ma in an inductive load. The circuit is similar to an L^{---} card.

The circuit consists of an emitter follower driving a grounded emitter amplifier. A -0.5v "0" (or ground) input raises the emitter of Q01 to a sufficiently positive potential so that the forward drop across CR02 will cause Q02 to be cut off. A -3.v "1" (or open) input will cause both transistors to conduct heavily, and if pin 12 is fed from -20v, current flow through the resistor network will be about 130 ma.

The connection of diode CR03 clamps the collectors at approximately -20.3v when the circuit switches off.


13
14
15
-20V
+20V
12
TEST POINT C
R04
47
R05
1200
R07
1200
R08
1200
R09
1200
R10
1200
R11
1200
R12
1200
R13
1200
C02
.1 μf
CR03
-20V
CDC 104
Q02
TEST POINT A
CDC 104
Q01
R06
6800
+20V
CR01
R03
220
R04
22,000
+20V
CR02
R02
1000
C01
100
-20V
R01
6800
-

READ AMPLIFIER

Card Type 70B

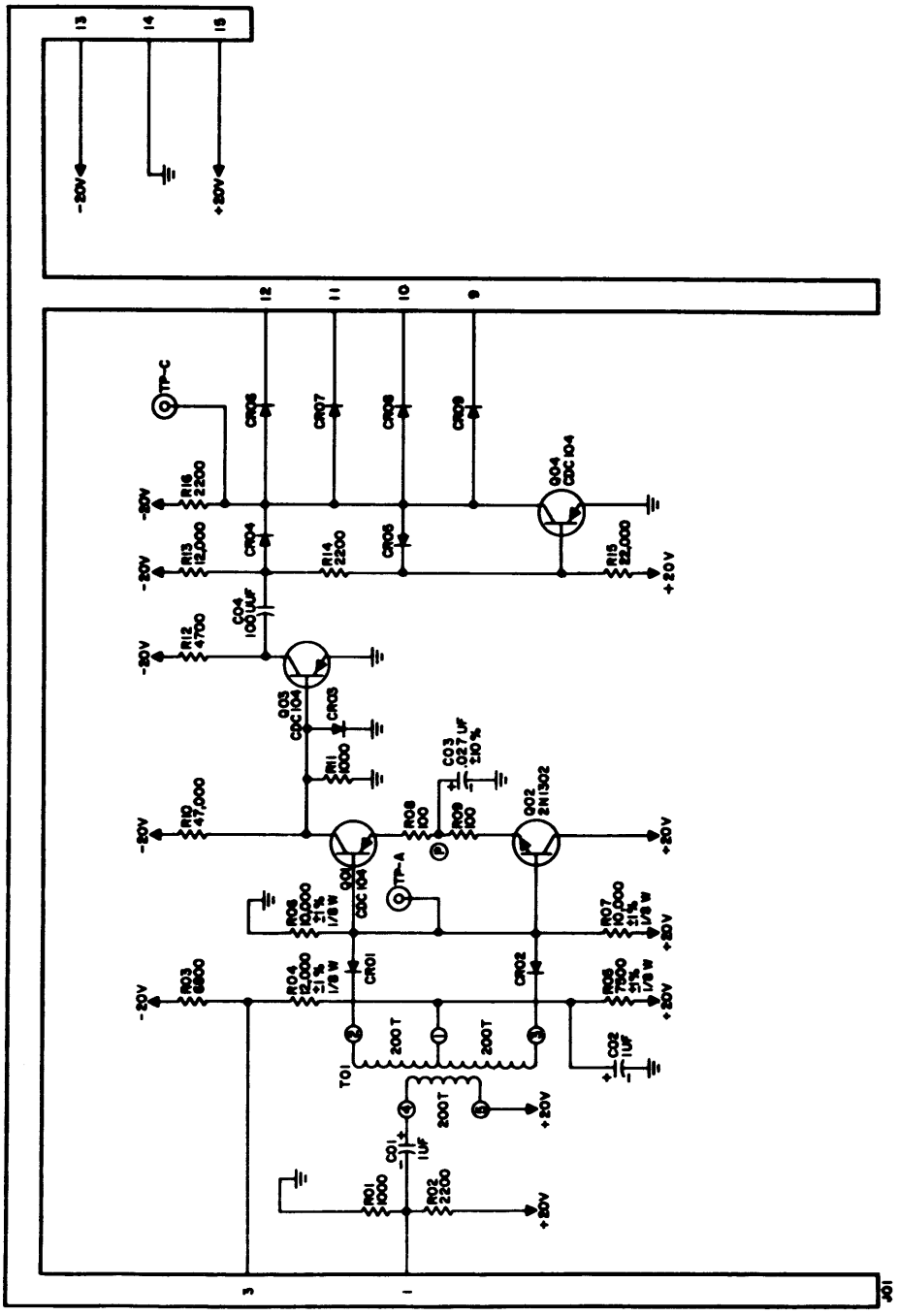
The 70B card detects sinusoidal signals and provides outputs of -3v "1". The input at pin 1 ranges from 6-8 volts (peak to peak) during a read-write mode and from 4-8 volts (peak to peak) during a normal read mode. To insure writing during a read-write mode, the write pulse should be fed to pin 3.

This circuit consists of three stages: the threshold detecting stage, the peak detecting stage, and the output stage. Essentially, the peak detecting stage and the output stage are a standard type of inverter; the only difference is that they are a-c coupled by the capacitor C04.

In the quiescent state, transistors Q01 and Q02 are cut off. As the input signal goes negative, Q01 starts to conduct, drawing its current from the charge on C03 since Q02 is still cut off. The point common to resistors R08 and R09 (point P) follows the negative signal by 2 usec. When the voltage at point P is equal to the input voltage, Q01 is cut off. As the input voltage goes positive, Q02 starts to conduct; it conducts until the input and output voltages at point P are equal. Thus transistors Q01 and Q02 provide pulses of negative polarity from either input polarity which are of greater magnitude than the bias supply voltage which acts as a threshold of detection level.

The peak detecting stage is a common emitter amplifier. When Q03 is cut off, a sharp negative transient is produced across R12. A small capacitor (C04) and a diode couple the peak detector stage and the output stage. The diode clips any positive signals and passes any negative signals. The time constant of C04 and the backward resistance of the diode are chosen to provide a negative spike for approximately 2 usec. This spike turns on transistor Q04, providing an output of "1" for a duration of 2 usec.

The voltages for an input of 4.0 volts (peak to peak) 30 KC should be about -2.0 v/cm and 0.5 v/cm at test points A and C.



Read Amplifier 70B

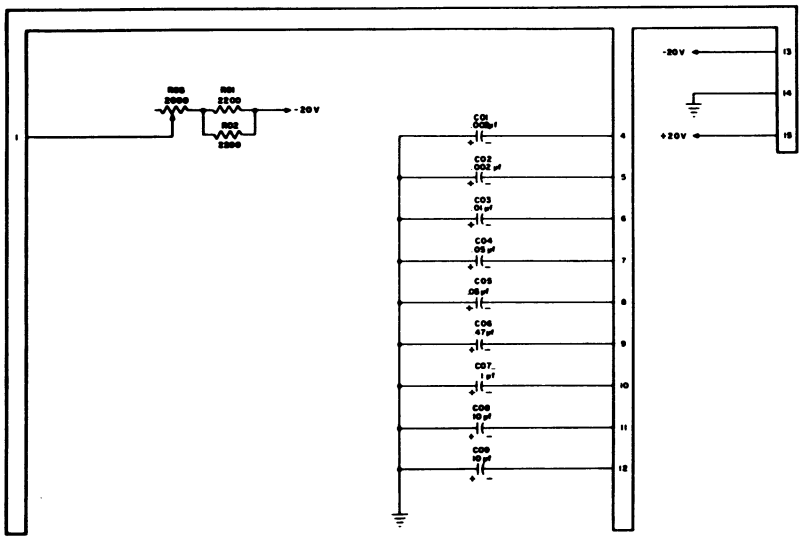
DELAY CAPACITORS

Card Types 73, 73A, 77, 82

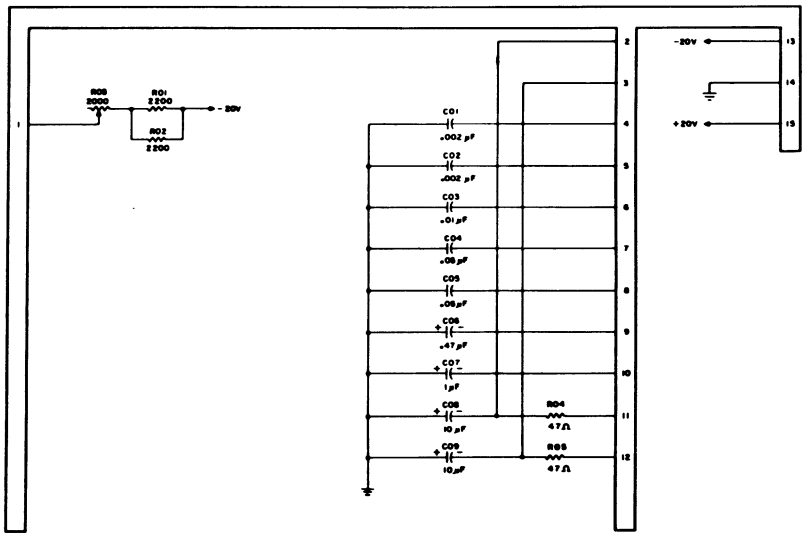
The purpose of a delay circuit is to provide an interval of time between successive logical operations. This is achieved by connecting a capacitor from the signal line to ground. The time elapsing between the input and output of a pulse, the time required to charge the capacitor, is known as delay time. The delay time is a function of the size of the capacitor and the rate at which it receives current. Other things being equal, the larger the capacitor, the longer the delay time; the smaller the capacitor, the shorter the delay time.

In the adjustable delay circuit, the delay time can be altered by varying the resistance in series with the capacitor. Varying the resistance increases or decreases the current flow to the capacitor, thereby increasing or decreasing the delay time. In the non-adjustable delay circuit, the delay time is fixed; it is a function of the size of the capacitor only.

The circuits contained on these cards may be used alone to provide short delays. To obtain long delays (greater than 10 usec) with greater stability, they may be used in conjunction with card type 97.



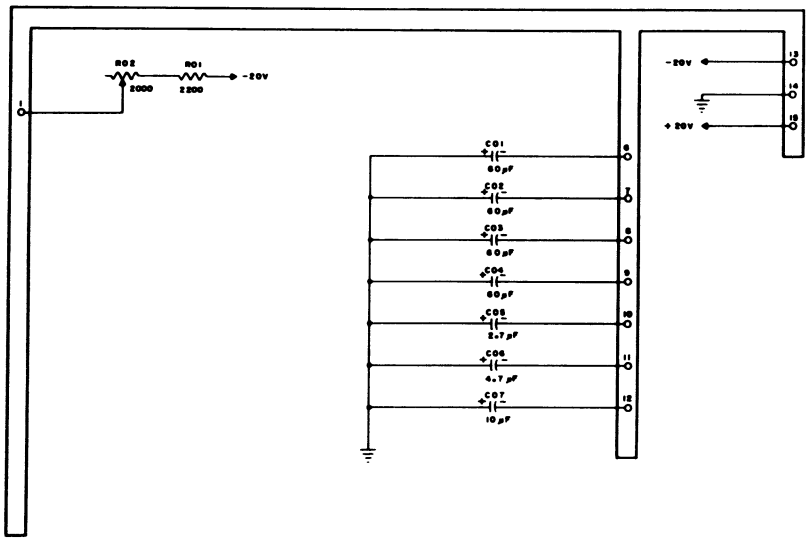
Delay 73



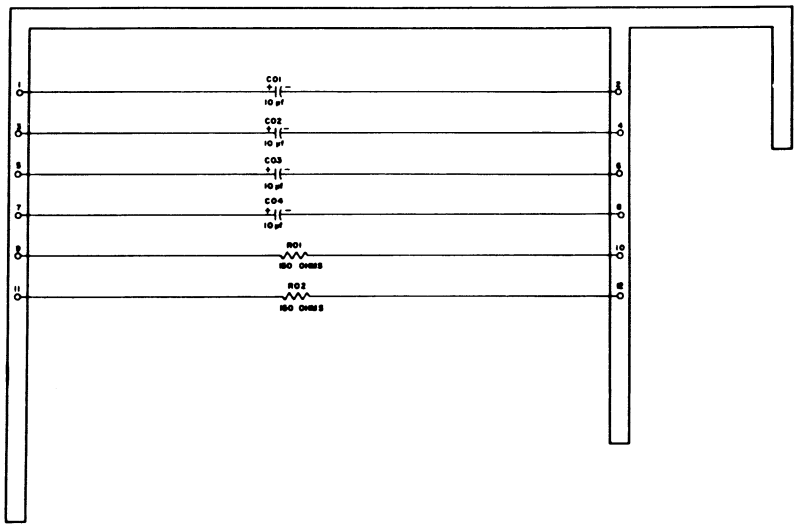
Delay 73A

5-73, 77, 82-2

Rev. E



Delay 77



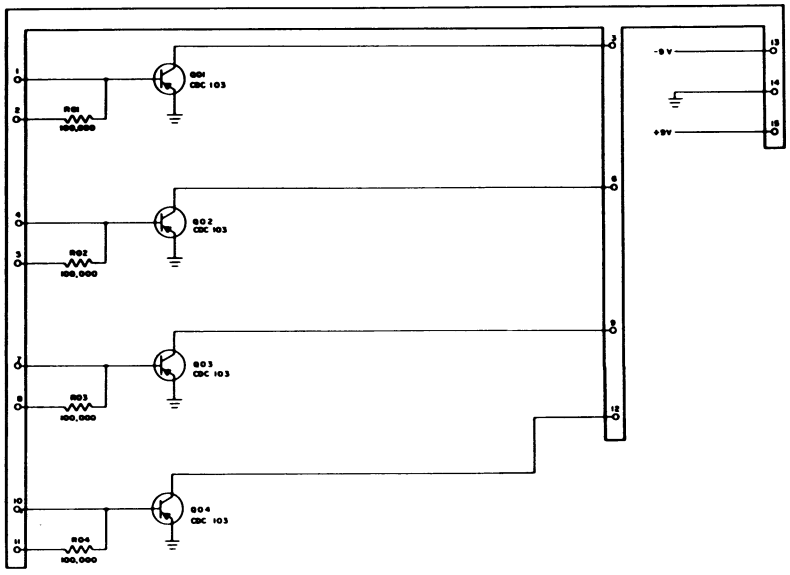
Delay 82

READER LEVEL AMPLIFIER

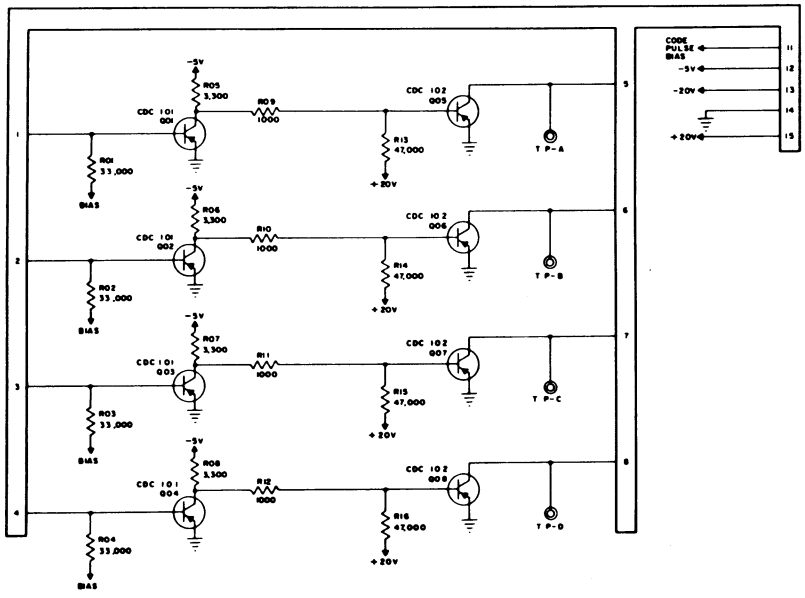
Card Types 75 & 75A

The circuits on card type 75 each consist of a single transistor connected as a grounded-emitter amplifier. A positive-going input causes the transistor to be cut off, while a negative-going input causes it to conduct. The transistor has a biasing resistor connected to its base, so that the sensitivity of the amplifier may be adjusted.

Card type 75A is designed to convert solar cell outputs from a paper tape reader into -0.5v outputs, representing a "0" in 1604-type logic. If no hole is sensed, the output transistor will be cut off. When light strikes the solar cell, the circuit input will be approximately +0.4v. This causes the input transistor to cut off and the output transistor to conduct. At other times, the input will be approximately an open circuit and the bias must be such that the input transistor is in its conduction state.



Reader Level Amplifier 75



Reader Level Amplifier 75A

READER BRAKE-CLUTCH DRIVER

Card Type 76A

FUNCTION

This card controls the starting and stopping of tape in a paper tape reader by alternately energizing the clutch and brake coils.

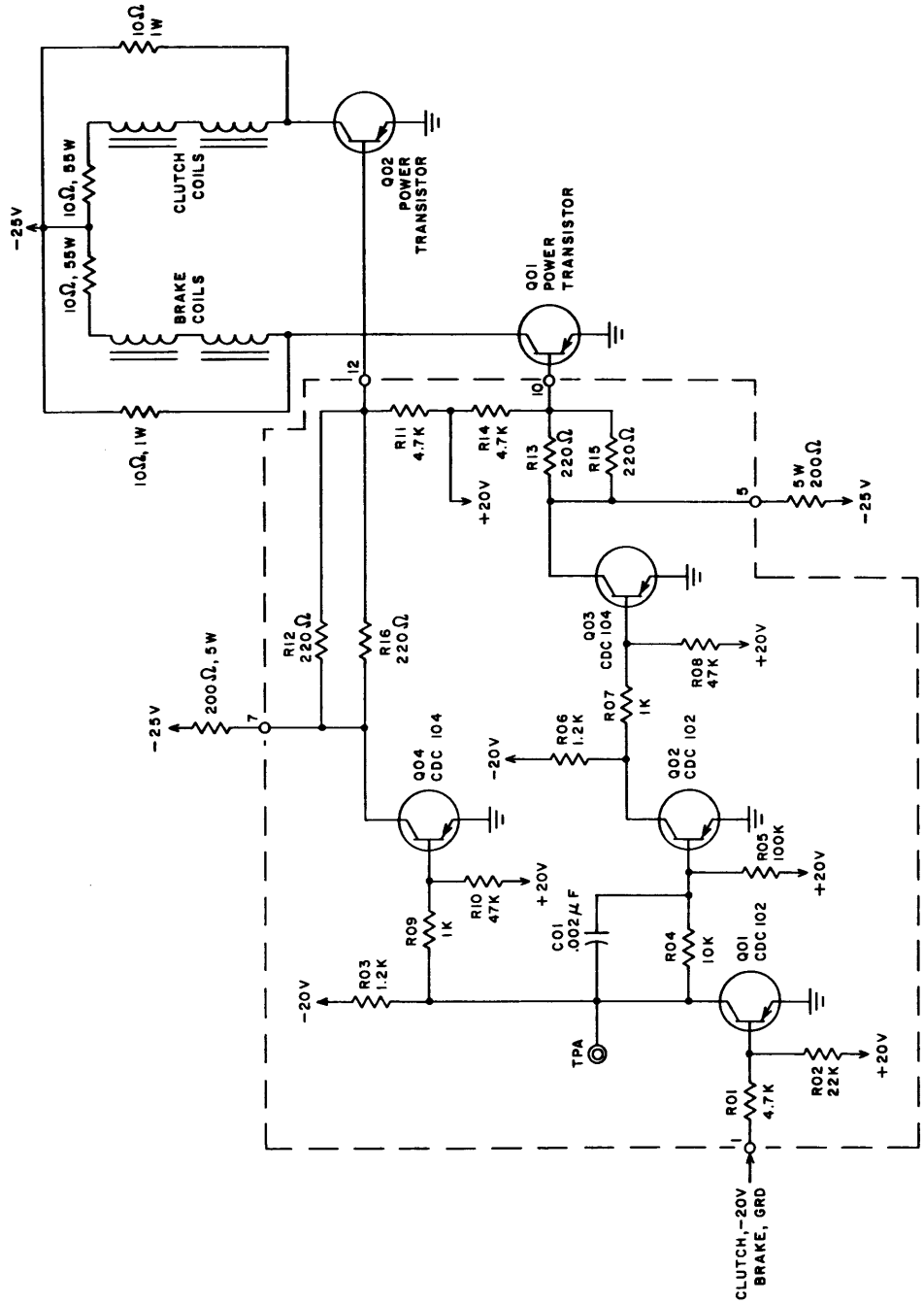
OPERATION

The clutch signal, a -20 volt potential applied to the base of Q01, energizes the clutch coils and starts the tape. The bias is determined by the voltage dividing network. The collector of Q01 drives transistors Q02 and Q04 to cut off. This forces the base of Q03 negative and Q03 conducts. A voltage dividing network supplies a positive base drive to power transistor Q01 and a negative base drive to power transistor Q02. The clutch coils are energized and the tape is advanced.

When the external equipment drops the clutch signal to ground, the brake coil is energized and the tape stops. Q02 and Q04 conduct because Q01 is cut off. The base of Q03 goes positive and power transistor Q01 receives the negative base drive necessary to energize the brake coils.

Diodes are used in conjunction with the brake and clutch coils. These diodes prevent back EMF induced by the coils when the transistors switch off from driving the collectors of the power transistors too far above the supply voltage.

The two brake electromagnets are identical coils connected in series. The clutch electromagnets are connected in similar fashion.



Reader Brake-Clutch Driver 76A

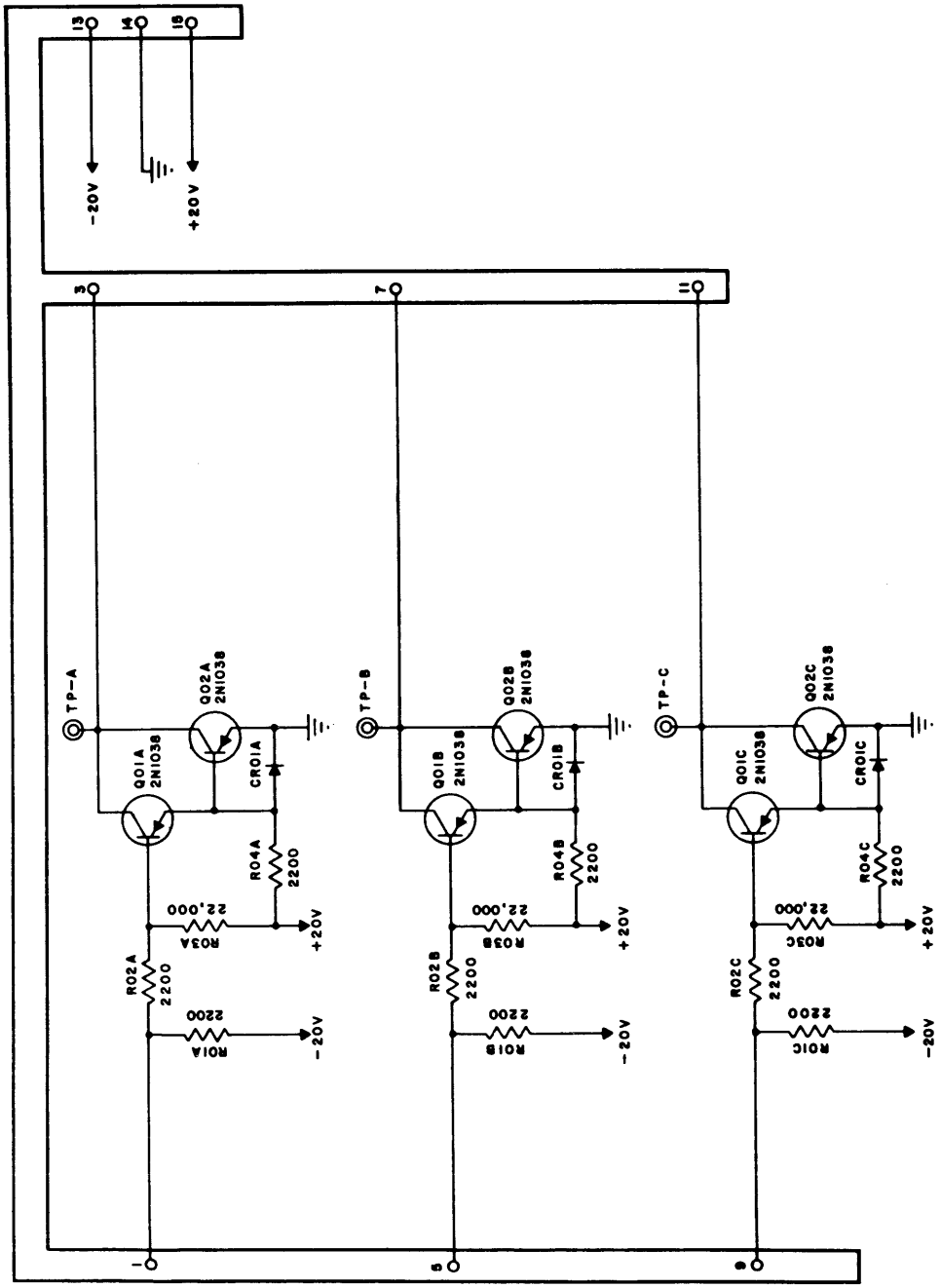
PUNCH PULLER

Card Type 86

(Note: Card Type 86A is identical except different transistors)

This circuit is designed to activate the magnets in a paper tape punch. It can switch a current of the order of 1.25 amperes at - 28V.

The circuit is driven by an L--- card. A - 18V input causes both transistors to switch to the conduction state. A - 0.5V input causes conduction through Q01 to decrease and the forward drop across CR01 cuts off Q02.



Punch Puller 86

HAMMER STORAGE
CARD TYPE 91

The design of the 91 card combines a binary storage location with an inverter of high current-switching ability.

SWITCH

The inverter-switch portion of the 91 card is capable of conducting 400 milliamperes continuously. A "1" input to Q03 from Q02 causes conduction. Output diode CR18 allows the card to drive one standard inverter or flip-flop. Another 91 card in the "0" state, connected to pin 10, acts as a block and prevents Q04 from conducting.

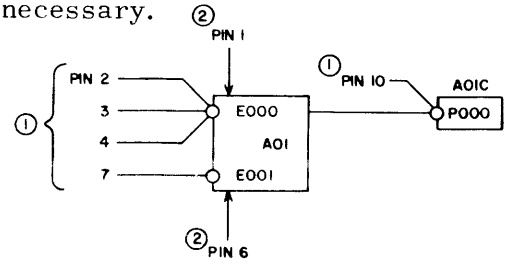
STORAGE

The storage flip-flop, a simplified version of the 1604 flip-flop series, contains two transistors, Q01 and Q02. A "1" input to Q01 (pins 1-4) sets the flip-flop and causes Q04 to conduct if a "1" is present at pin 10. A "1" input to Q02 (pins 6-7) clears the flip-flop.

The 1604 series of inverters and flip-flops used by Control Data have isolation diodes placed at their output and none at their input. A 1604 card may therefore drive only as many cards as it has output diodes (a maximum of eight). The 91 card, which has three isolation diodes on the set side of its input and one on the clear side, may be driven directly by Q04 of other 91 cards. Because of the high switching current property of Q04, it is possible to drive up to 120 91 cards with only one 91 driver. The result is elimination of the slave inverter pyramid usually required to drive so many cards. In addition to the isolated inputs, the 91 card has a standard input on the set and on the clear side for inputs from the 1604 series of logic cards. The isolated and non-isolated inputs are ANDed together within the 91 card.

SYMBOL

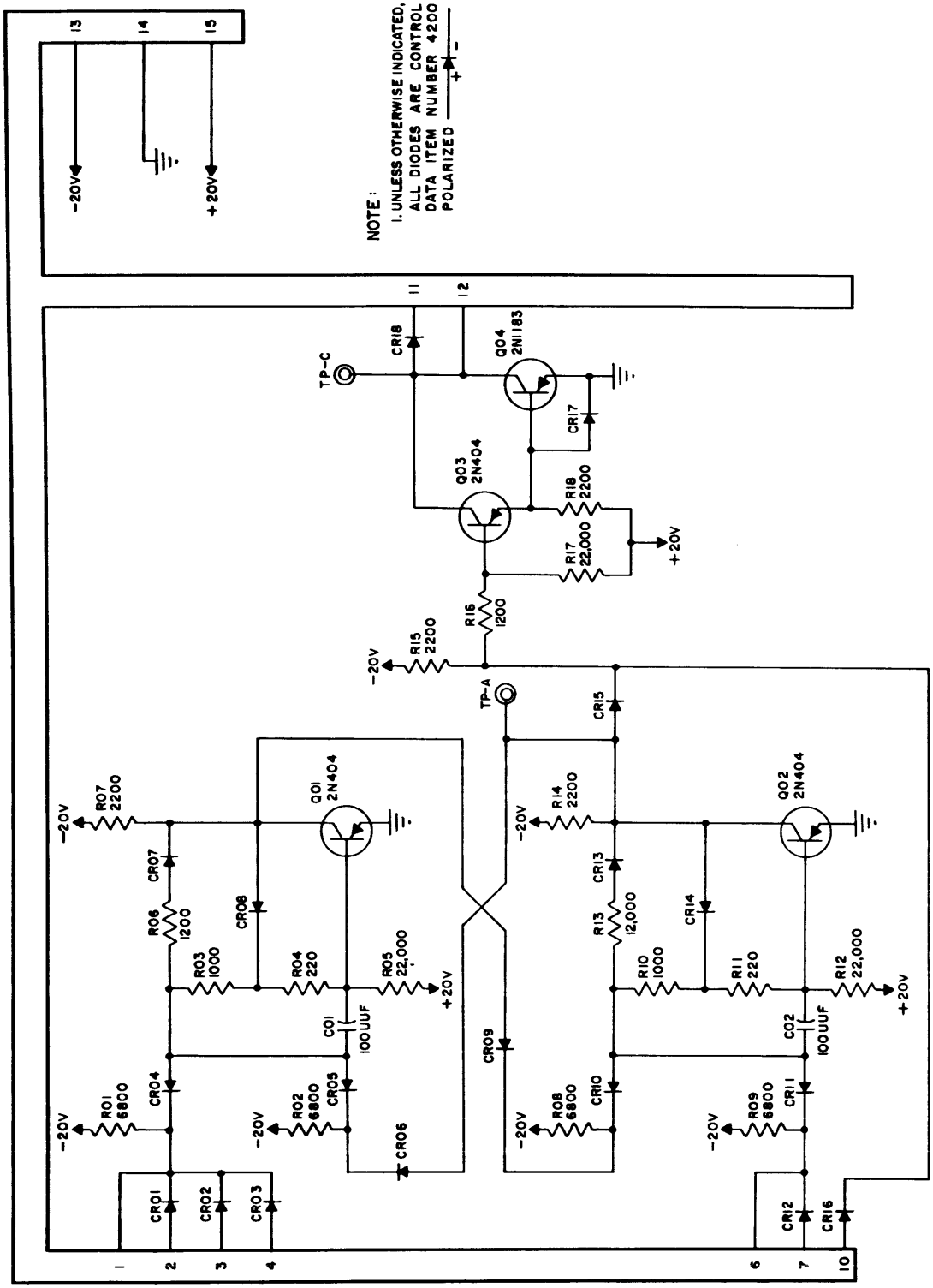
The combination of isolated and non-isolated inputs on the 91 card made a new logic symbol necessary.



Logic Symbol, Card Type 91

Notes:

1. Feed from pin 12 of other 91 cards.
2. Treat as standard 1604 input.



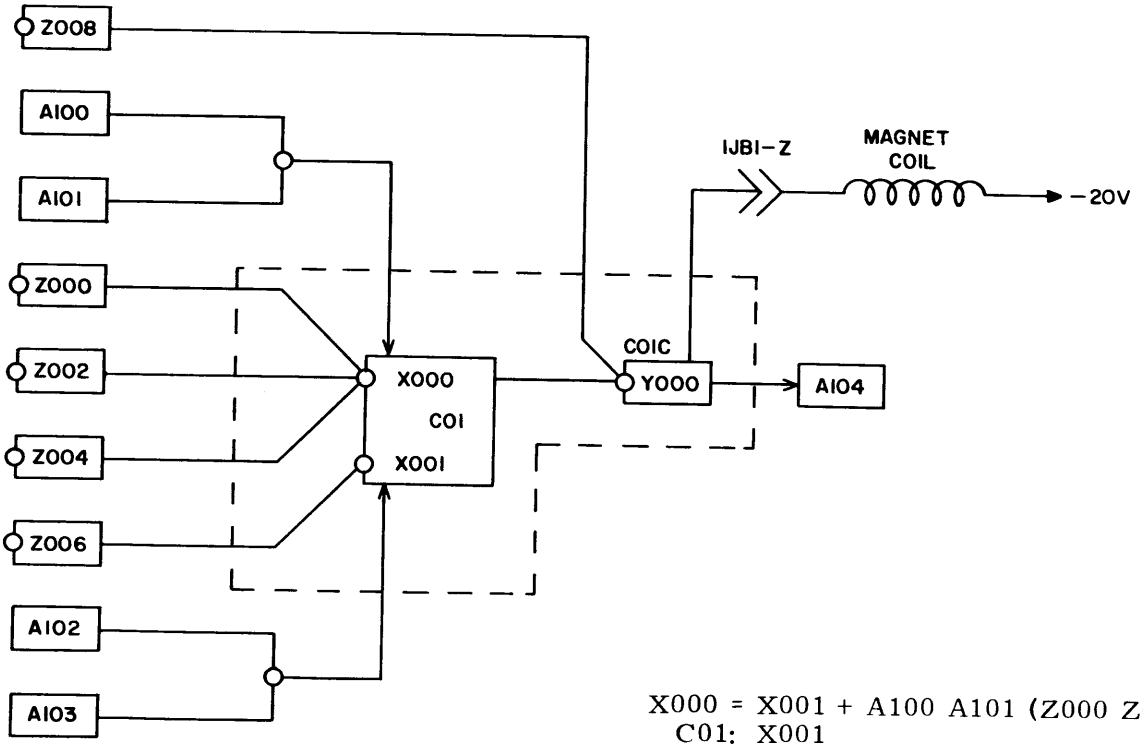
Schematic Diagram, Card Type 91

TESTPOINTS

There are two testpoints located on the 91 card, TP-A and TP-C. TP-A registers a "1" when the flip-flop is set. TP-C registers a "0" when the inverter-switch is conducting.

EQUATIONS

91 card equations are similar to those for standard 1604 logic cards. An exception is the use of parenthesis around terms connected to isolated inputs. A sample circuit and its associated equations is shown below.



X000 = X001 + A100 A101 (Z000 Z002 Z004)
C01: X001

X001 = X000 + A102 A103 (Z006)
C01A: X000: Y000

Y000 = X001 (Z008)
C01C: A104: 1JB1-Z

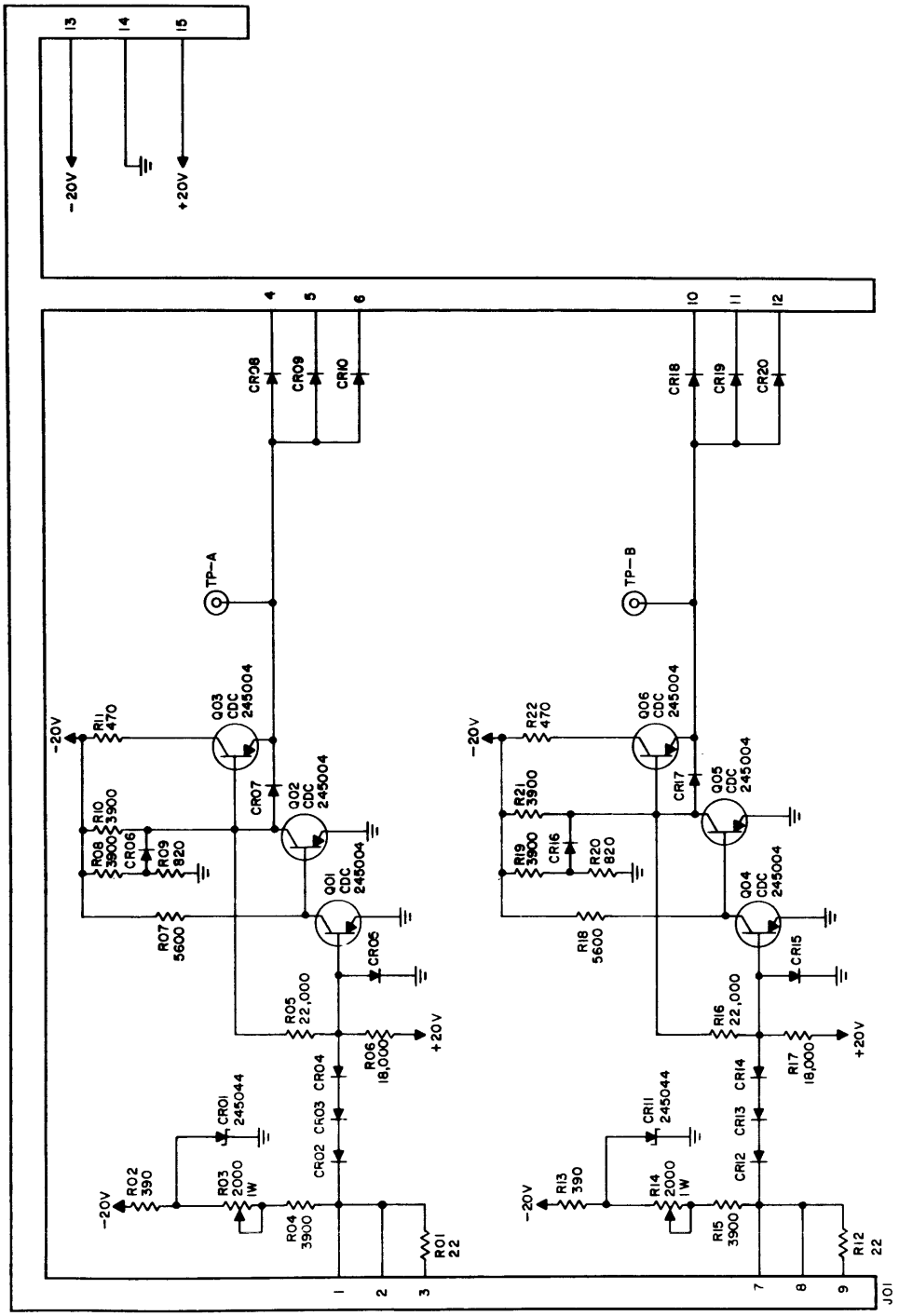
Sample Logic Diagram With Equations

DELAY
Card Type 97A

This circuit is designed to provide stable delay times of relatively long duration in 1604-type logic. It consists of a double inverting network such that the dircuit does not produce an overall logical inversion. The input to the circuit must be connected to an external capacitor. The delay time obtained can be adjusted approximately ± 15% by means of the variable resistor R03.

The circuit is similar to card types C68 and C69, which are discussed elsewhere in this manual. The principal differences are the addition of AND diodes on the output, and a slightly different method of shifting the input level. The input level is shifted approximately 2.1v positive by diodes CR02, CR03, and CR04. These are silicon diodes having a constant forward drop of 0.7v. (On card types C68 and C69, this level shifting is done by a 3.5v zener diode.)

The external delay capacitor can be connected to either pin 2 or pin 3. Pin 3 contains a series 22-ohm resistor to protect against damage from peak currents when using large capacitors.


13
14
15
-20V
+20V
4
5
6
10
11
12
CR08
CR09
CR10
CR18
CR19
CR20
TP-A
TP-B
Q03 CDC 245004
Q06 CDC 245004
Q02 CDC 245004
Q05 CDC 245004
Q01 CDC 245004
Q04 CDC 245004
R11 470
R22 470
R10 3900
R21 3900
R08 3900
R19 3900
CR06
CR16
R09 820
R20 820
R07 5600
R18 5600
CR07
CR17
CR05
CR15
R05 22,000
R16 22,000
R06 18,000
R17 18,000
+20V
CR04
CR14
CR01 245044
CR11 245044
CR03
CR13
CR02
CR12
R02 390
R13 390
R03 2000 1W
R14 2000 1W
R04 3900
R15 3900
R01 22
R12 22
1
2
3
7
8
9
J01

Delay 97A

CLOCK OSCILLATOR-AMPLIFIER
Card Type C01

GENERAL

The clock oscillator-amplifier shown on page 5-C01-2 is essentially a tank circuit which may be tuned through a small range around 8 megacycles, with drive provided to the tank by two transistor amplifiers. The transistors are connected in a push-pull configuration, with the two circuit inputs directly connected to their bases. When the transistor inputs are provided with cross-coupled feedback from the oscillator transformer secondary, a continuous self-oscillation is maintained.

The circuit is designed so that, if external drive is provided to the inputs, the two transistors will operate as sine wave amplifiers, providing a two-phase output at the tank frequency.

PYRAMID CONNECTION

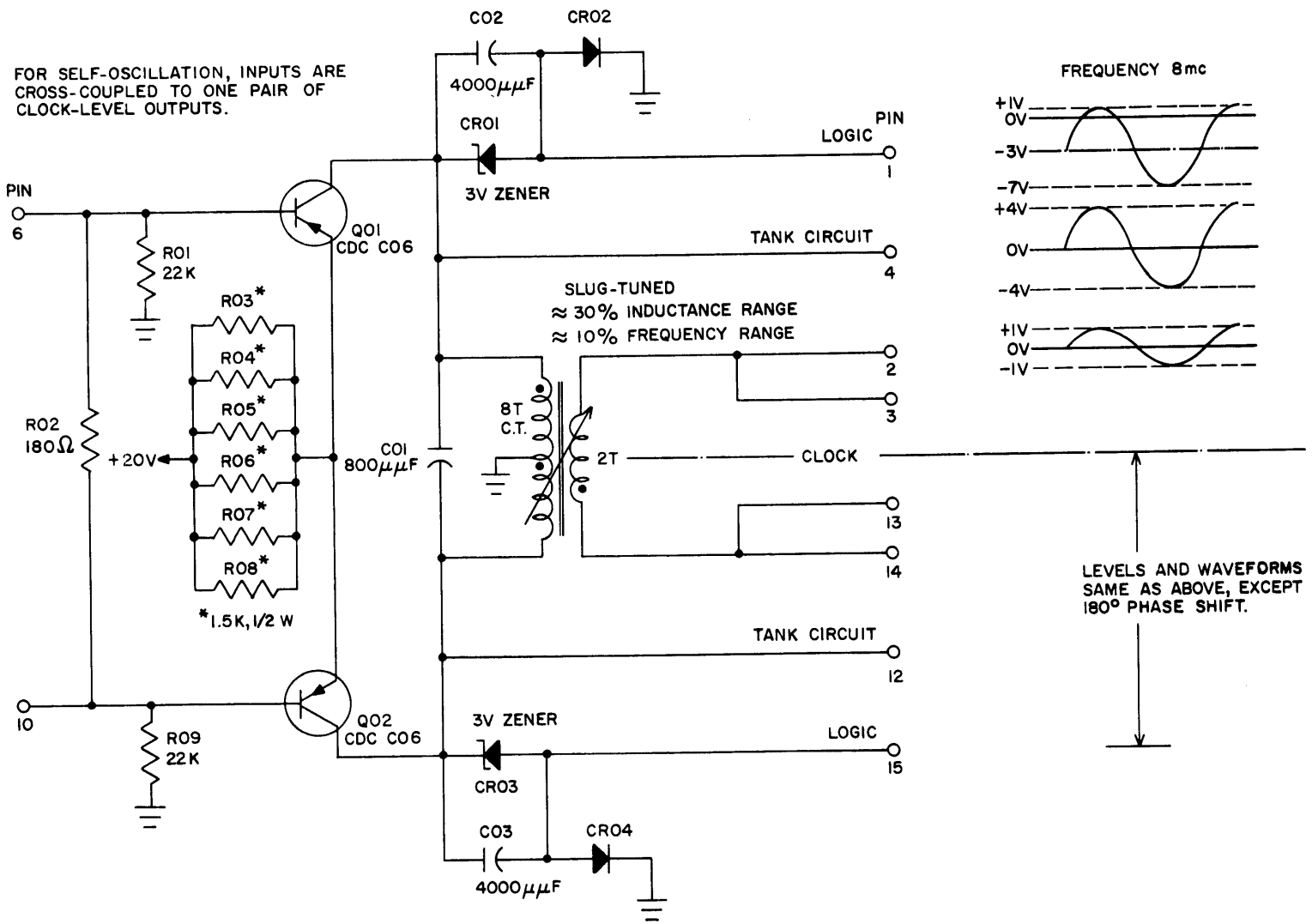
The computer timing configuration for which this circuit is designed is an oscillator-amplifier pyramid, as shown on page 5-C01-3. The master oscillator is a clock circuit connected as a feedback oscillator. To avoid undue loading effects, the master oscillator is permitted to drive only 2 amplifiers.

The ranks of amplifiers are clock circuits which receive external inputs and function as push-pull sine wave amplifiers. Each amplifier is capable of driving 4 others; thus, the pyramid effect is produced. Each amplifier in a rank must be in phase with every other amplifier in that same rank, although it is not necessary for the ranks to be in phase with each other or with the master oscillator. Outputs to the logic are taken only from the final rank of amplifiers.

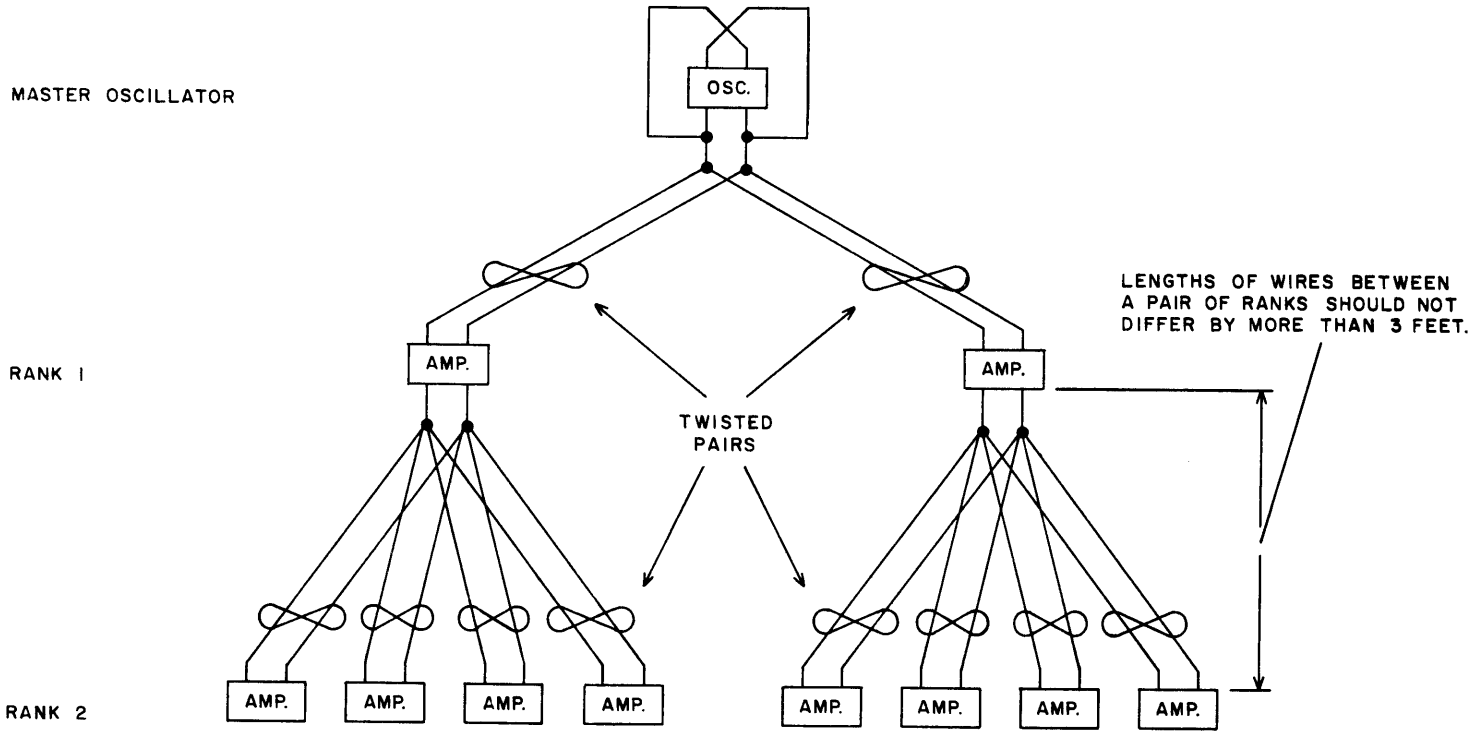
CIRCUIT OPERATION

The driving transistors Q01 and Q02 are CDC C06's and are connected in a push-pull configuration. Only one transistor is necessary to sustain oscillation; however, two transistors greatly increase the ability of the circuit to drive an unsymmetrical load.

Clock amplifier logic outputs are restricted to driving AND loads only. Through jumpered connections, an amplifier may drive up to 10 loads. Ideally, this is distributed


FOR SELF-OSCILLATION, INPUTS ARE CROSS-COUPLED TO ONE PAIR OF CLOCK-LEVEL OUTPUTS.
C02
CR02
4000μμF
CR01
PIN
LOGIC
1
3V ZENER
PIN
6
Q01
CDC C06
TANK CIRCUIT
4
R01
22K
R03*
R04*
R05*
R06*
R07*
R08*
*1.5K, 1/2 W
SLUG-TUNED
≈ 30% INDUCTANCE RANGE
≈ 10% FREQUENCY RANGE
2
3
8T
C.T.
2T
CLOCK
R02
180Ω
+20V
C01
800μμF
13
14
TANK CIRCUIT
12
10
Q02
CDC C06
3V ZENER
LOGIC
15
R09
22K
CR03
C03
CR04
4000μμF
FREQUENCY 8mc
+1V
0V
-3V
-7V
+4V
0V
-4V
+1V
0V
-1V
LEVELS AND WAVEFORMS SAME AS ABOVE, EXCEPT 180° PHASE SHIFT.

Clock Pyramid C01



NOTE:

1. MASTER OSCILLATOR MAY DRIVE 2 AMPLIFIERS.
2. EACH AMPLIFIER MAY DRIVE 4 FOLLOWING AMPLIFIERS.
3. ALL AMPLIFIERS IN THF SAME RANK ARE IN PHASE WITH EACH OTHER, BUT NOT NECESSARILY IN PHASE WITH ANY OTHER RANK OR WITH THE MASTER OSCILLATOR.

with 5 loads on each output phase; however, the loading may be unbalanced to 8 and 2, if necessary.

The characteristics of transistors Q01 and Q02 are such that they have a power handling capability of 150 mw at 25°C ambient. The average transistor dissipation in an oscillator circuit is of the order of 60 mw.

An 800 uuf silver-mica capacitor C01 having a low temperature coefficient and good stability is used in the tank circuit to resonate with the transformer inductance at a center frequency of 8 megacycles. The transformer inductance may be tuned through a range of approximately 30 percent by means of a low permeability ferrite slug. This has the effect of shifting the tank frequency through a range of approximately 10 percent.

The peak-to-peak signal develped across the tank is restricted to approximately 8v by the clamp diodes CR01 and CR04. The printed circuit card provides outputs at pins 4 and 12 at which this sine wave appears. If necessary, all tanks in a rank of amplifiers may be locked in phase with one another by connecting these outputs in parallel.

A logic-level signal is a sine wave about -3v, with peaks at +1v and -7v. It is produced by using a zener diode to shift the d-c reference level of the tank output. Logic-level outputs are taken only from the last rank of the clock pyramid and are available at pins 1 and 15.

The circuit on page 5-C01-2 provides a clock-level output at pins 2, 3, 13, and 14, which is taken from the secondary of the tank transformer. The secondary winding consists of 2 turns, while the primary winding is 8 turns, center-tapped; therefore the clock-level output is a sine wave about ground with a peak-to-peak amplitude of approximately 2v.

The clock-level signals are used as drive signals throughout the clock pyramid, as shown on page 5-C01-3. All wires used to transmit clock-level signals must be twisted pair, and the distance over which the signal is transmitted should be less than 15 feet. In addition, there should be less than a 3 foot variation in the lengths of wire used to transmit drive signals between a given pair of ranks.

PROCEDURE FOR TUNING A CLOCK PYRAMID

A scope equipped with a differential or dual-trace preamplifier, such as a Tektronix type CA, may be used for tuning the pyramid. The probe leads should be equal in length and must be grounded at the cards. The scope should be externally synchronized during step 3. Use the master oscillator for this.

Step 1.

Adjust the transformer of the master oscillator to the correct computer frequency. This may be done by setting the horizontal sweep at 0. 1 usec/ cm and adjusting until 8 peaks are seen across the 10 cm scope grid, if the desired frequency is 8 megacycles.

Step 2.

With the scope on a sensitive range, adjust one of the amplifiers in Rank 1 for maximum amplitude.

Step 3.

Using external sync, adjust the remaining amplifiers in Rank 1 to be in phase with the reference amplifier tuned in step 2. This may be done with a differential preamplifier, by inverting one signal and adding algebraically, and adjusting for minimum deflection with the scope on a sensitive range.

Other ranks are tuned according to steps 2 and 3.

GROUND RULES

A. Clock-level outputs.

1. The oscillator may drive 2 amplifiers in addition to providing its own feedback.
2. Each amplifier may drive 4 other amplifiers.
3. Interconnecting wires between ranks of amplifiers and from the master oscillator to rank 1 must be twisted pair.
4. Signals may be transmitted up to 15 feet.
5. There should be no more than a 3-foot difference in the lengths of interconnecting wires between a given pair of ranks.

B. Tank circuit output.

1. This is used only to phase-lock the tanks within a single rank of amplifiers, if necessary.

C. Logic-level outputs.

1. Clock outputs must always connect to logic card AND inputs.
2. A maximum of 10 loads may be driven.
3. A maximum of 8 loads may be driven by any single output; with 8 loads on one output, the opposite-phase output of that amplifier may drive only 2 loads, so that the total number does not exceed 10.

CLAMP

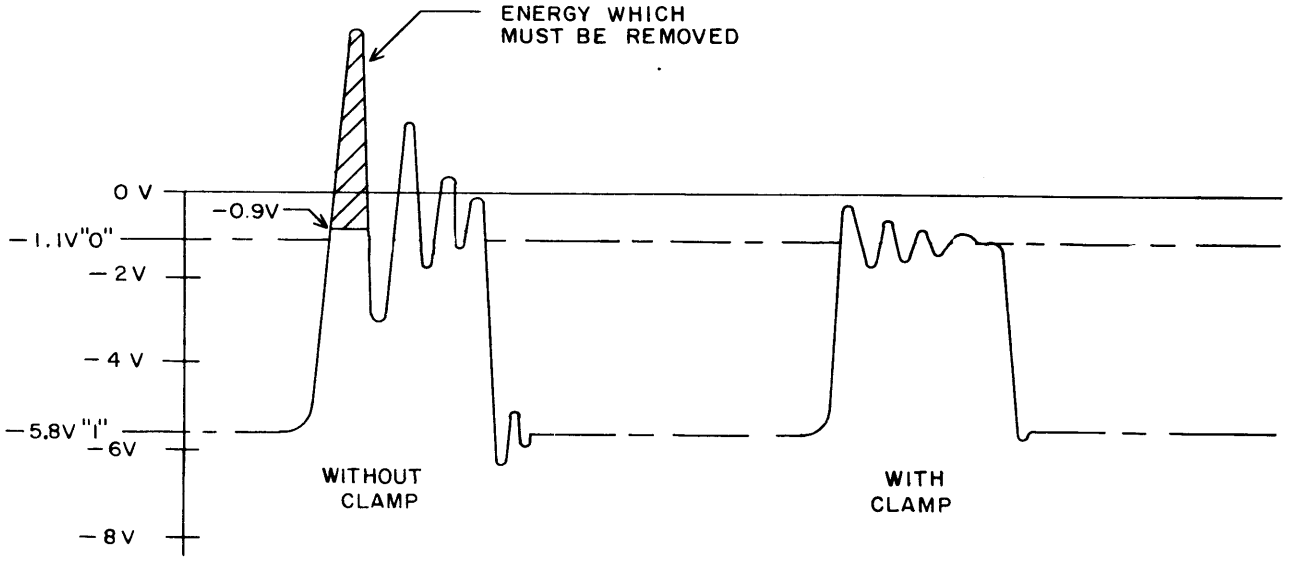
Card Type C02

This circuit provides a clamp for logic circuit connecting lines, so that ringing is minimized. If sufficient energy is removed from the first overshoot, the remainder of the ringing has an amplitude less than the logic circuit threshold. A schematic of the clamp circuit is presented on page 5-C02-2, with typical waveforms showing its effect on a line having excessive ringing.

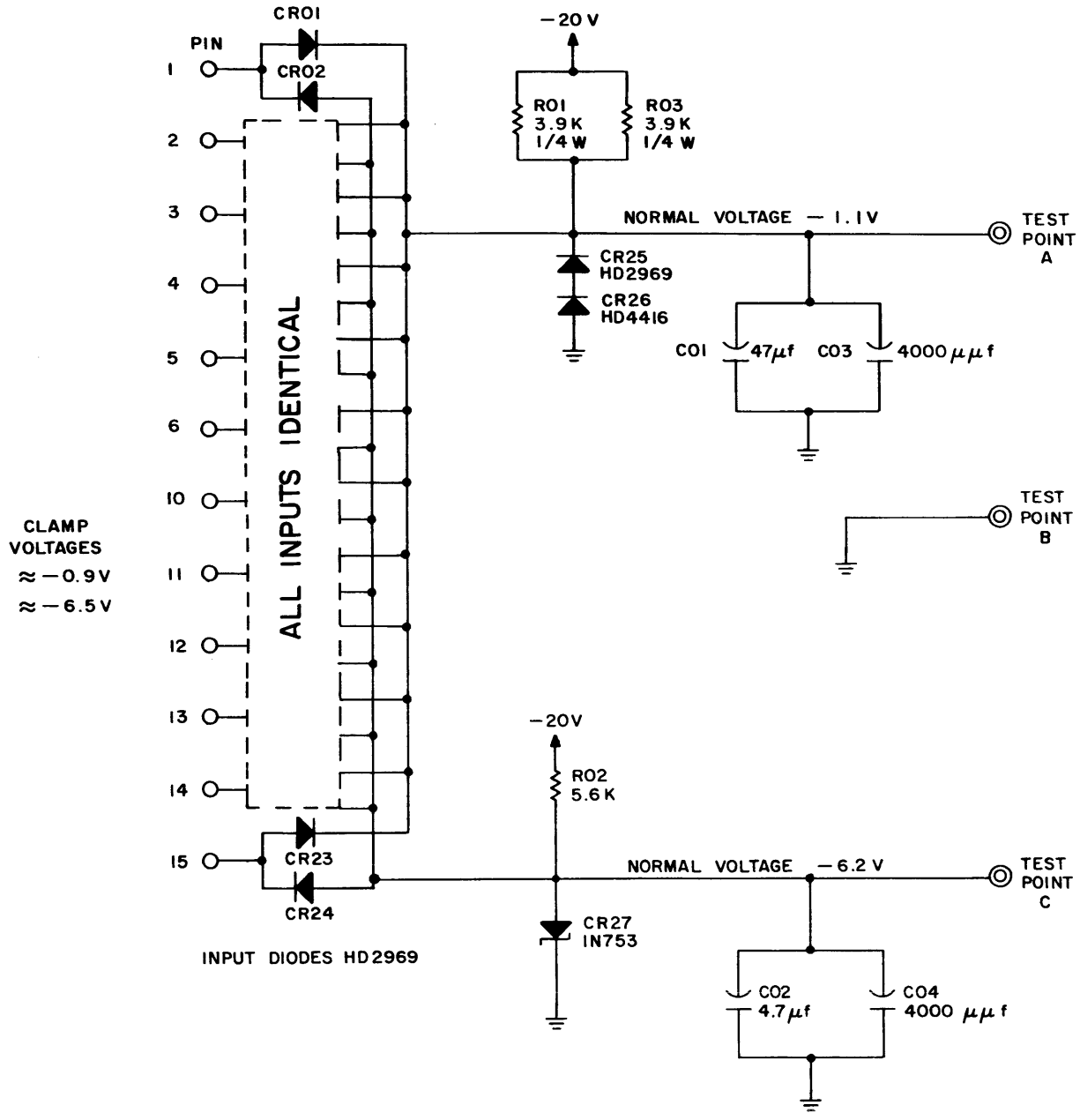
The clamp voltage in the positive direction is the sum of the forward drops across diodes CR25 and CR26, less the drop across the input diodes. It is approximately -0.9v.

The clamp voltage in the negative direction is the sum of the drop across zener diode CR27 plus the drop across the input diodes. It is approximately -6.5v.

Filtering is provided by capacitors C01, C02, C03, and C04. Due to their large area C01 and C02 present an appreciable amount of inductive reactance. It is therefore necessary to include the small capacitors C03 and C04 in order to filter out high-frequency spikes.



Typical Logic Line Voltage, 3600


CR01
PIN
1
CR02
2
3
4
5
6
10
11
12
13
14
15
CR23
CR24
ALL INPUTS IDENTICAL
INPUT DIODES HD2969
CLAMP VOLTAGES
≈ −0.9 V
≈ −6.5 V
−20 V
R01 3.9 K 1/4 W
R03 3.9 K 1/4 W
NORMAL VOLTAGE — 1.1 V
TEST POINT A
CR25 HD2969
CR26 HD4416
C01 47μf
C03 4000 μμf
TEST POINT B
−20V
R02 5.6 K
NORMAL VOLTAGE −6.2 V
TEST POINT C
CR27 IN753
C02 4.7μf
C04 4000 μμf

Clamp C02

EMITTER FOLLOWER
Card Type C07C

FUNCTION

The function of this circuit is to convert inputs received from a terminated 200-ohm delay line into outputs suitable for driving a logic card load. This circuit provides a high impedance load for the delay line, avoiding excessive current drain which affects its operating characteristics.

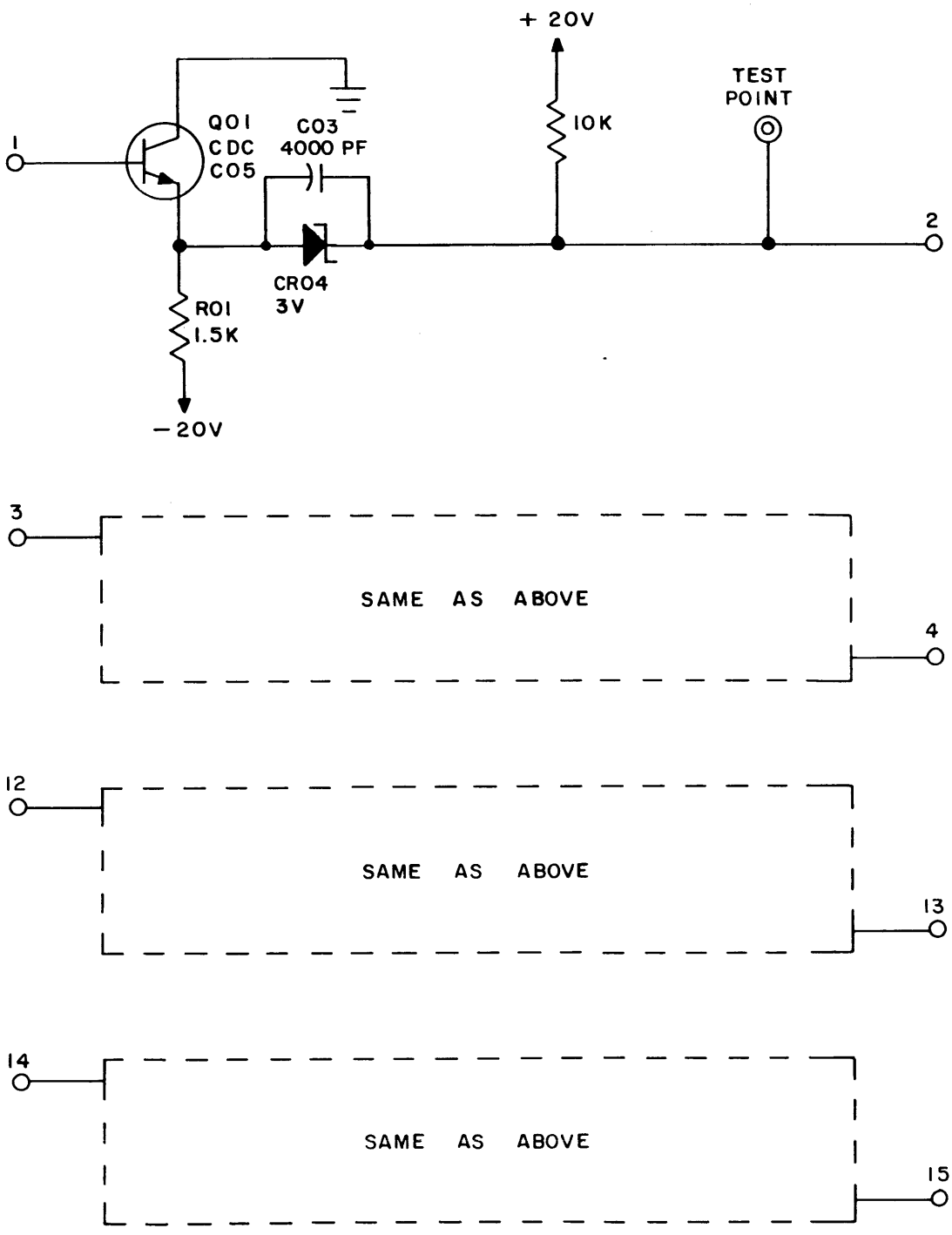
OPERATION

The delay line is driven by the circuit on card type C08; thus its input signal levels are approximately -0. 3v and -10v. However, due to integrating characteristics and attenuation, the peak voltage levels tend to diminish slightly as the signal travels down the delay line. The input signal levels of the emitter follower circuit are therefore of the order of -0 3v and -10v, depending upon the point of the delay line from which the signal is taken.

A -0. 3v input results in an output near ground which is interpreted as a logical "0". A -10v input results in an output of approximately -9. 3v which is interpreted as a logical "1".

Transistor Q01 is an NPN silicon type CDC C05. It is connected as an emitter follower; thus its emitter voltage is always approximately 0. 7v more negative than the circuit input.

CR04 is a zener diode having a voltage drop of approximately 3v. This holds the circuit output 3v more positive than the emitter of Q01.



Emitter Follower C07C

DELAY LINE DRIVER
Card Type C08

FUNCTION

The function of this circuit is to provide an output suitable for driving a terminated 200-ohm delay line. With a 200-ohm load at pin 1 and the circuit in its quiescent state, the output voltage level is approximately -10v. Upon receipt of a -5.8v "1" input, both transistors switch to a state of heavy conduction and the output voltage becomes approximately -0.3v.

OPERATION

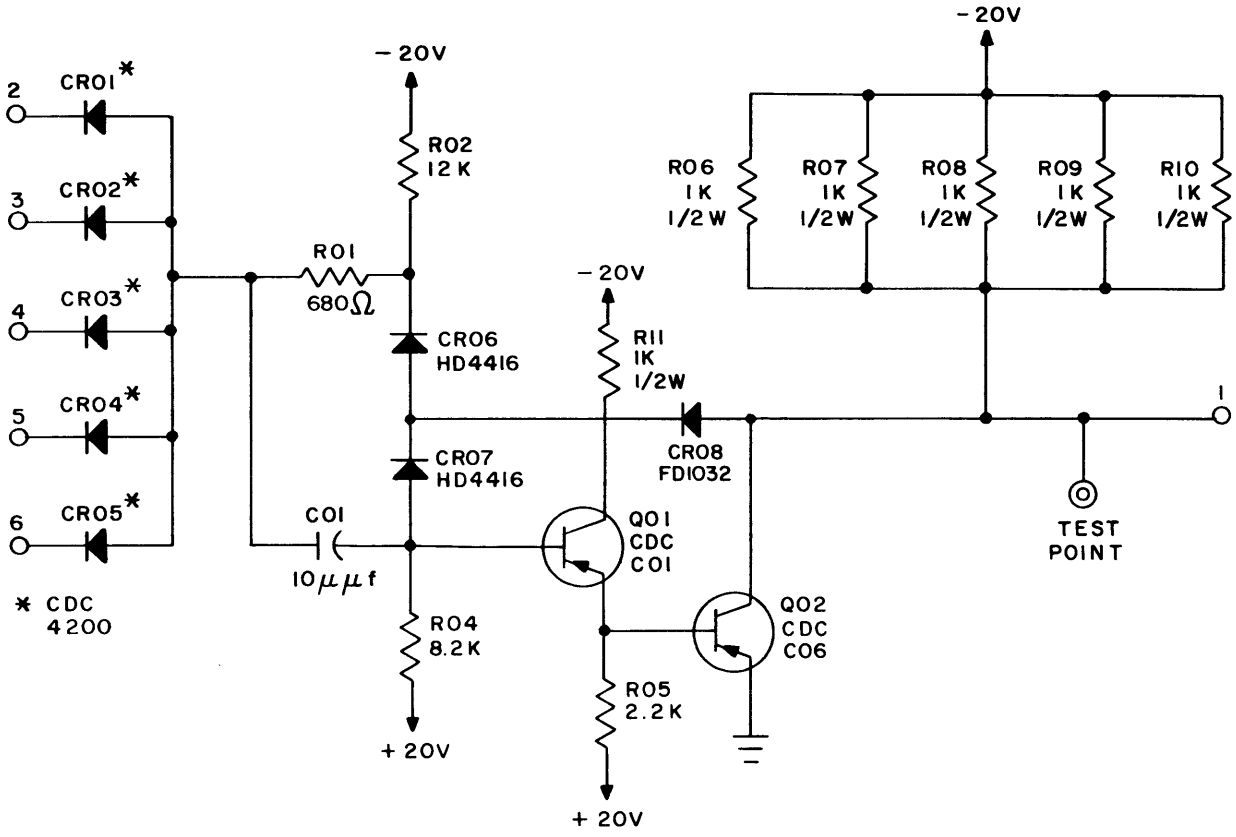
The circuit has 5 logical OR inputs; thus a -5.8v "1" on any input activates the circuit. An unused input is effectively a steady "0", regardless whether it is grounded or left open.

An input level-shifting action is provided by the two forward-drop diodes CR06 and CR07. These are silicon diodes having a forward voltage drop of approximately 0.7v. The two diodes in series provide a voltage shift of +1.4v from the cathode of CR06 to the anode of CR07.

With -1.1v "0" inputs, the base of Q01 is held at approximately +1.3v by the level-shifting diodes. Transistor Q01 is connected as an emitter follower; thus its emitter voltage is equal to the base voltage plus the base-emitter junction drop, and is approximately +1.6v. This provides sufficient forward bias so that minimum conduction is maintained through Q01. The emitter voltage of Q01 drives the base of Q02, which is a grounded emitter stage. The base-emitter junction of Q02 is therefore back-biased by the +1.6v input, and Q02 is cut off.

A -5.8v "1" input holds the base of Q01 at approximately -0.6v causing Q01 to conduct heavily. The emitter voltage of Q01 goes to approximately -0.3v, which causes Q02 to switch on and conduct heavily. In this state, the circuit output is clamped at approximately -0.6v by CR08.

With Q02 in the cut off state, its collector voltage tends to rise toward -20v. However, the 200-ohm load acts as a voltage divider with the equivalent 200-ohm resistance of the five 1000-ohm resistors, and the output stabilizes at -10v.



NOTES:

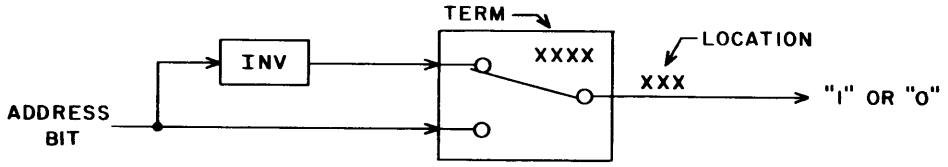
1. CIRCUIT HAS 5 "OR" INPUTS.
2. A -5.8V "1" INPUT CAUSES TRANSISTORS TO CONDUCT.

Delay Line Driver C08

COMPUTER DIVISION
PRINTED CIRCUIT DESCRIPTION
SWITCH
Card Type CA60A

FUNCTION AND OPERATION

This card contains four single-pole, double-throw toggle switches. The card was originally disigned as a memory selection switch to translate four bits of a storage address. The two positions of each switch correspond to the "1" and "0" values of the address bit.

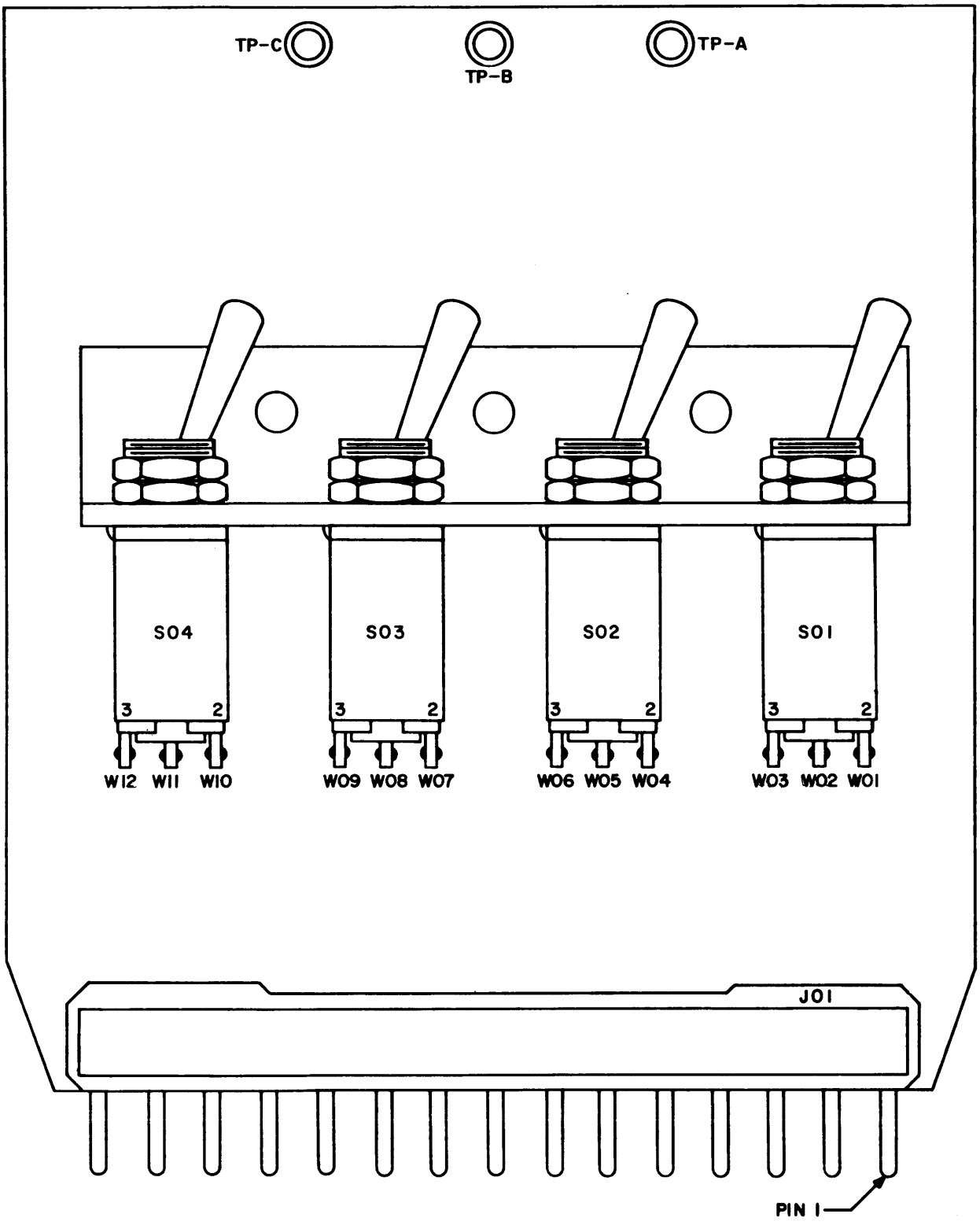


LOGIC DIAGRAM SYMBOL

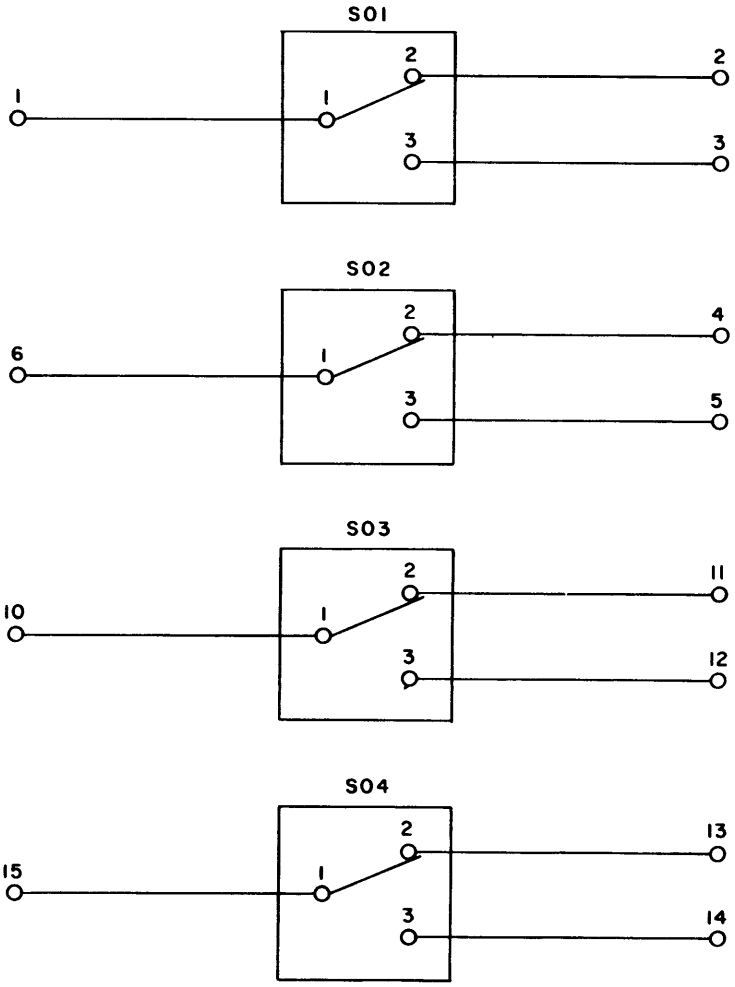
RELATED DOCUMENTS	NUMBER
Parts List	30923800
Assembly Drawing	30923800
Schematic Drawing	30923900
Engineering Specification	None

GROUND RULES

1. Because of the size of the switches, the card location adjacent to the component side of the CA60A card cannot be used.



COMPONENT LAYOUT



Switch CA60A

RESYNC CIRCUIT
Card Types C64A, C65A, C66A

GENERAL

The resync circuit shown on page 5-C64-3, is contained on three printed circuit cards, the type numbers being C64, C65, and C66. The logical operation of this circuit is presented on page 5-C64-2, and a timing diagram is shown on page 5-C64-5.

The function of a resync circuit is to synchronize an asynchronous signal of random length with the computer clock. Upon receipt of a logical "1" input signal, the resync circuit produces a "1" output during a clock phase. This output is 62.5 nanoseconds long and is not repeated, regardless of the duration of the input.

The delay time through the resync circuit is approximately 40 nanoseconds. The clock which drives the resync circuit must be phase-shifted so that the resync output coincides with the computer clock.

The average time required for resynchronization is 2 clock phase times, taking into account the 40-nanosecond circuit delay. It is possible, however, for this to occur during 1 phase time, and it never requires more than 3. A simplified timing diagram of the resync circuit is shown on page 5-C64-5. The best case and worst case conditions refer to the length of time required for synchronization.

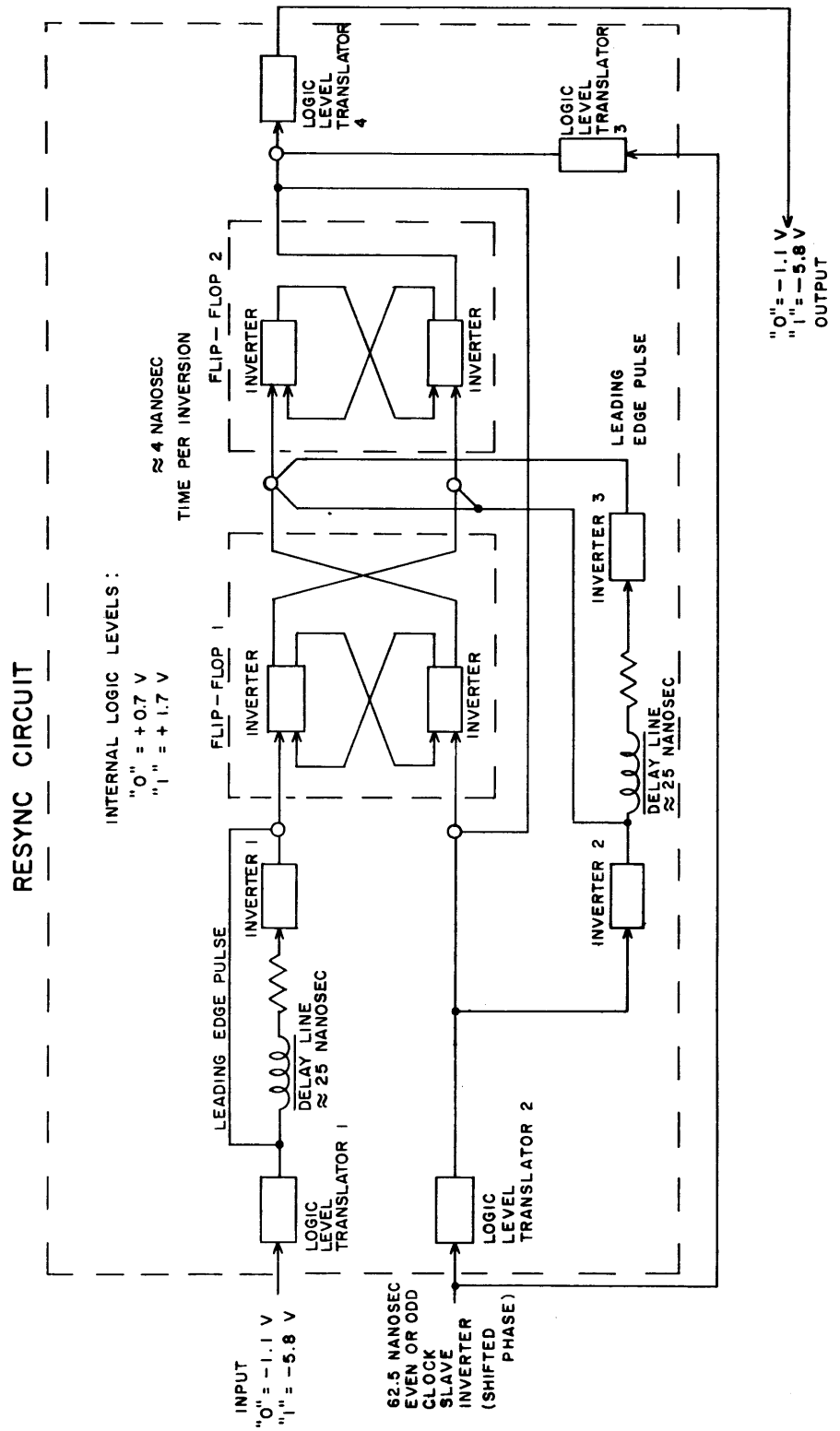
Logic levels within the resync circuit are in the positive voltage domain. A "0" is represented by +0.7v and a "1" by +1.7v.

LOGICAL FUNCTIONING

With initial conditions prevailing, the input to the circuit is a steady "0" and the output of inverter 1 is a steady "1". When a "1" input is received by the circuit, the delay line allows the output of inverter 1 to remain a "1" for approximately 25 nanoseconds. During this time FF 1 is set.

Next, FF 2 is set by the ANDed outputs of inverters 2 and 3. When the clock input goes to "0", the output of inverter 2 goes to "1". The delay line allows the output of inverter 3 to remain a "1" for 25 nanoseconds, setting FF 2.

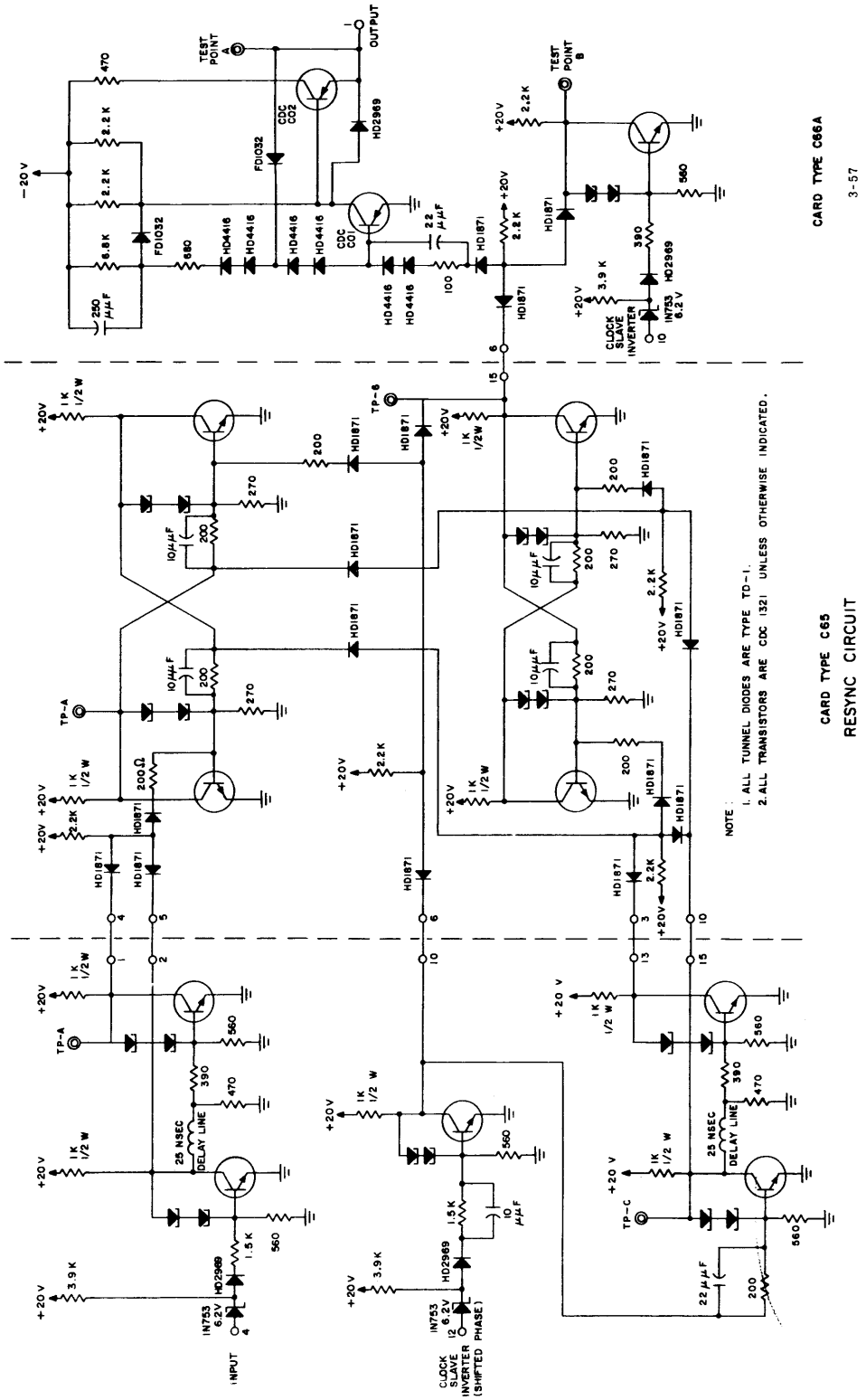
With FF 2 set, the "1" is gated out of the circuit by a full 62.5 nanosecond clock phase, which also clears FF 1. Following this, the clock input clears FF 2, and initial conditions prevail.



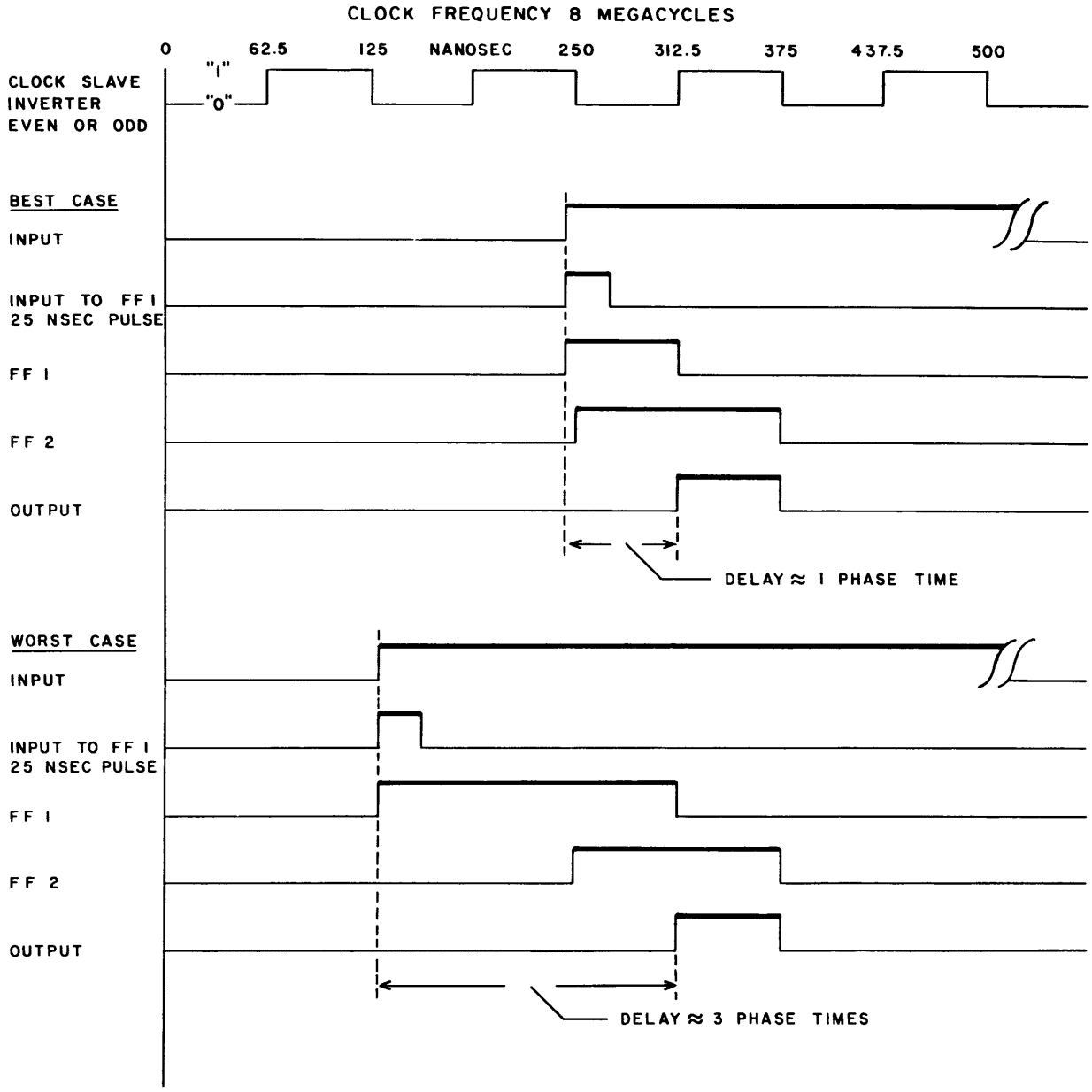
Resync Circuit

5-C64, C65 and C66-2

REV. D



Resync Circuit C64A, C65A, and C66A



NOTES:

1. BEST CASE — INPUT RECEIVED JUST BEFORE CLOCK PHASE GOES TO "0".
2. WORST CASE — INPUT RECEIVED JUST AFTER CLOCK PHASE GOES TO "0".

Resync Circuit Timing Diagram

5-C64, C65 and C66-5

REV. D

CIRCUIT OPERATION

As shown on page 5-C64-3, except for the transistors in the output logic level translator, all of the resync circuit transistors are CDC 1321. This is a high speed silicon NPN type, having a gain-bandwidth of 1 kmc, which provides a time per inversion of approximately 4 nanoseconds, as used in this circuit. All of the CDC 1321 transistors have a base-to-collector tunnel diode network. This network establishes an input threshold level and holds the output voltage at the sum of the tunnel diode drops and the base-emitter junction drop.

The tunnel diodes are type TD-1. This is an axial tunnel diode having an I_p = 1 ma and a V_{fp} = 500 mv. Assuming an ideal case, two tunnel diodes in series would switch at 1 ma with a composite V_{fp} = 1v. Due to slight individual differences, no two tunnel diodes switch at exactly the same point, but the difference is negligible in this high speed circuit.

Logic level translators 1, 2, and 3 perform the function of changing a -5.8v "1" to a +1.7v "1", and a -1.1v "0" to a +0.7v "0". Upon receipt of a -1.1v "0" input, the tunnel diodes are back biased and they are in the low voltage state. Thus the collector potential is held at the potential of the base, which is approximately +0.7v, being a grounded emitter silicon transistor. However, upon receipt of a -5.8v "1" input, the 6.2v drop across the zener diode causes tunnel diode current to increase to approximately 1.2 ma, so they switch to the high voltage state. This causes transistor conduction to decrease, and the collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter voltage, a total of +1.7v.

The inverter circuits change a +1.7v "1" input to a +0.7v "0" output, and vice versa. Again, the output levels are taken from the collector, and the collector potential is equal to the sum of the tunnel diode voltages plus the base-emitter voltage of the silicon transistor. The time required for a transition from one state to the other is approximately 4 nanoseconds.

As shown on page 5-C64-3, the two flip-flops are each constructed of two inverter circuits provided with cross-coupled feedback from collector to base. These flip-flops are bistable circuits and are therefore capable of storing information.

The output logic level translator is quite similar to a logical inverter circuit, which is discussed elsewhere. This circuit converts a +0.7v "0" into a -1.1v "0", and a

+1.7v "1" into a -5.8v "1". It is capable of driving up to 8 logic cards, all of which may be either AND or OR, or any combination resulting in 8 loads total. The input to this translator consists of the set output of FF 2, ANDed with the output of logic level translator 3. This produces an output pulse width of 62.5 nanoseconds, since the input from the clock slave inverter is a -5.8v "1" for this length of time. There is a delay of approximately 40 nanoseconds from this input to the resync circuit output.

The grounded emitter transistor is a PNP type CDC C01. The base bias is such that a +0.7v "0" allows it to switch on, producing a -1.1v "0" output, while a +1.7v "1" input causes it to switch off, producing a -5.8v "1" output.

GROUND RULES

1. The clock slave inverter input to pin 12 of the C64 card and pin 10 of the C66 card should be phaseshifted so that the resync output coincides with the computer clock.
2. There is a delay of approximately 40 nanoseconds from the clock slave inverter input at pin 10 of the C66 card to the resync circuit output.
3. The resync circuit may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.

PRIORITY CIRCUIT

Card Types C77, C78B, C79A

(See Pub No. 60042000 3609 Diagrams, drawing number 311518)

GENERAL

The priority circuit shown on page 5-C77-3 is contained on three printed circuit cards, the type numbers being C77, C78, and C79. The logical operation of this circuit is presented on page 5-C77-2, and a timing diagram is shown on page 5-C77-5.

The function of the priority circuit is to enable a storage module to honor its five access channels on a first-come, first-serve basis, without interference from any other access channel. Priority circuits are contained in the input logic of each of the five access channels, and when one of them receives a "1" input, it disables the priority circuits in the remaining four channels. Thus a request on any of the remaining channels is not honored until the first channel is released.

The priority circuits differentiate between access channel requests spaced down to approximately 7 to 8 nanoseconds. Requests arriving more closely than this are considered to have arrived simultaneously, and factors such as supply voltage and wire length determine which channel is honored. If two requests arrive simultaneously and all other factors are equal, then neither is honored.

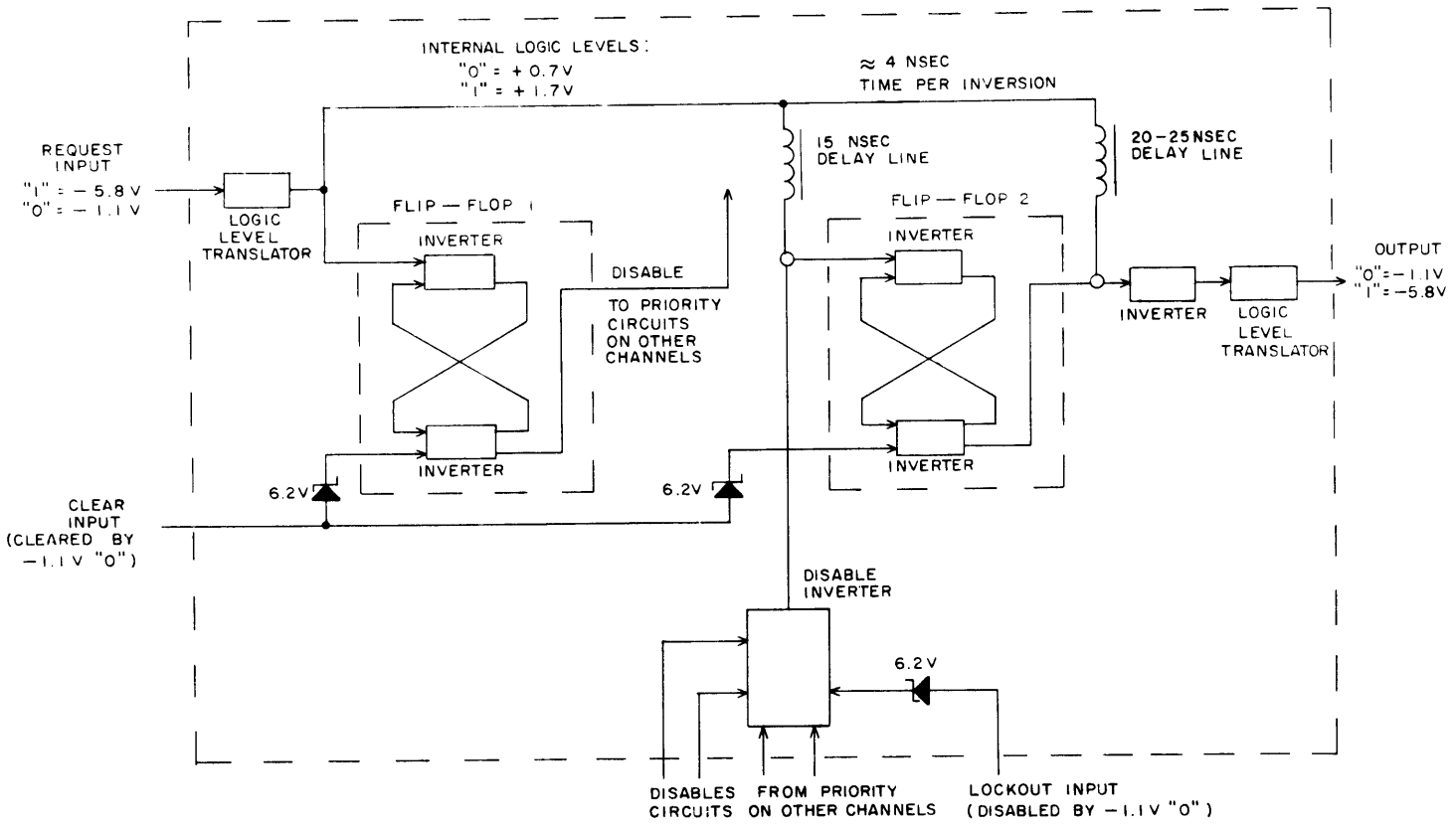
With card type C79A, the delay time through a priority circuit is 30 to 40 nanoseconds. The 20-nanosecond delay line accounts for the majority of this, since the transistor and tunnel diode logic provides a time per inversion of approximately 3 to 4 nanoseconds. A priority circuit timing diagram is presented on page 5-C77, C78 and C79-5.

Logic levels within the priority circuit are in the positive voltage domain. A "0" is represented by +0.7v and a "1" by +1.7v. The disable signal sent from one priority circuit to the other four is the set output of FF1, and is a +1.7v "1".

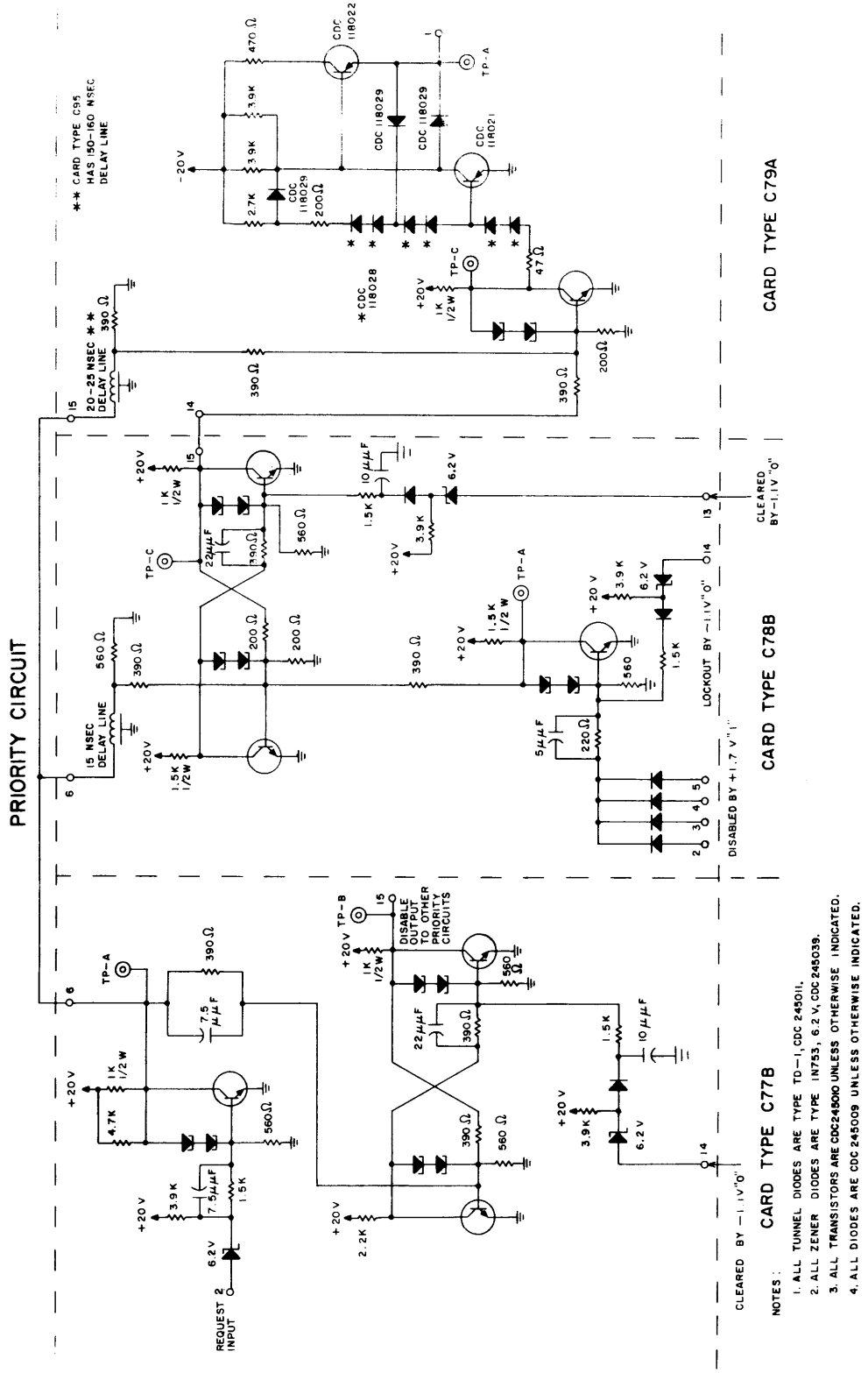
NOTE

Card type C95 is similar to C79A, except that the delay line is 150-160 nanoseconds.

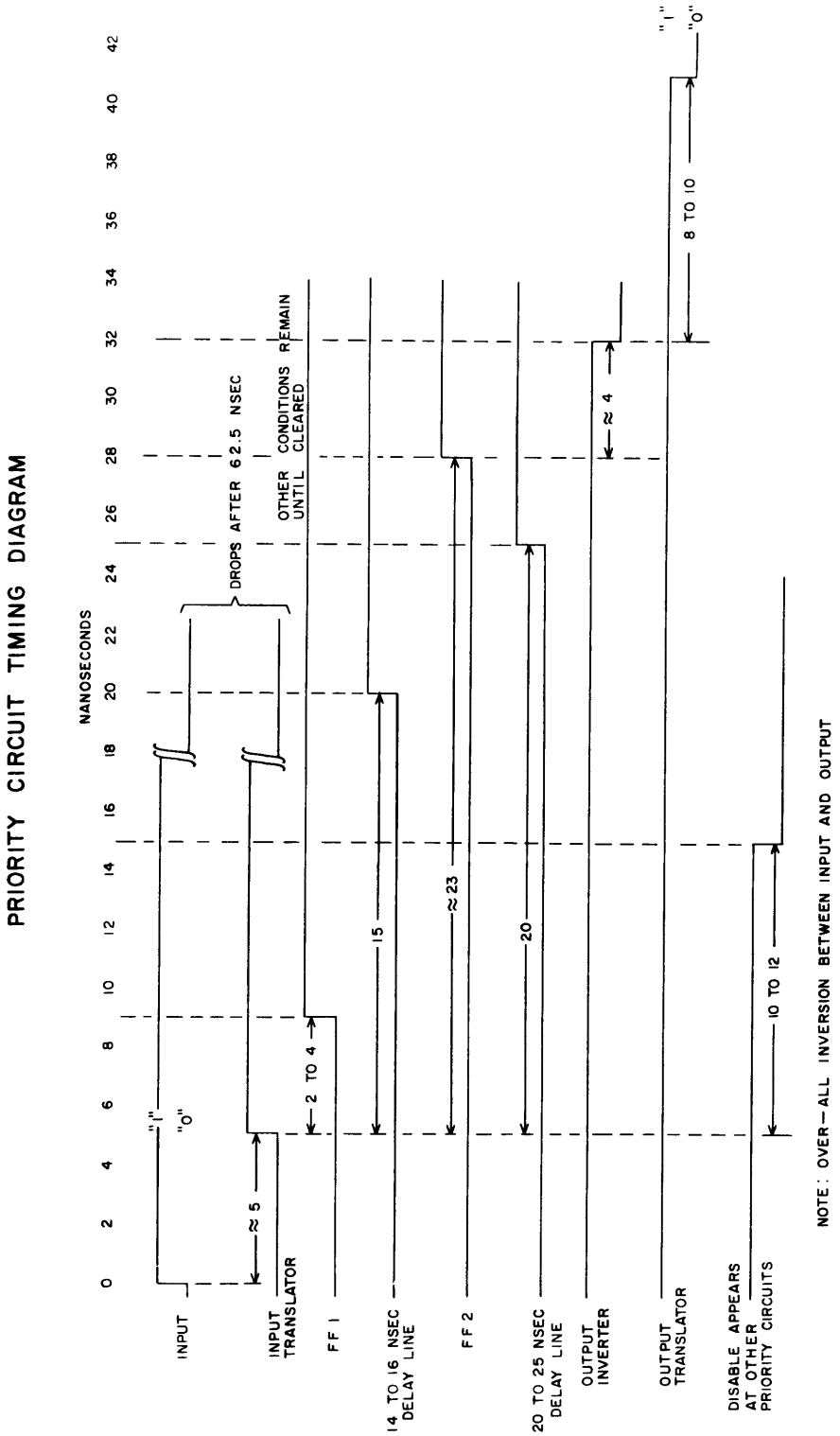
Priority Circuit



NOTE:
CIRCUIT PRODUCES A LOGICAL INVERSION BETWEEN INPUT AND OUTPUT.



Priority Circuit C77B, C78B and C79A



Priority Circuit Timing Diagram

LOGICAL FUNCTIONING

As shown on page 5-C77-2, the portions of the priority circuit are: an input logic level translator; flip-flop 1 which produces the signal disabling the other priority circuits; an inverter which disables flip-flop 2 if another access channel has priority; flip-flop 2; an output inverter; and an output logic level translator.

In addition, the priority circuit contains four 6.2v zener diodes, three of which function both as logic level translators and inverters. A -5.8v "1" input to a zener diode becomes a +0.4v output, and a -1.1v "0" input becomes a +5.1v output. These outputs act as "0" and "1", respectively, in the priority circuit logic. The remaining zener diode performs a level-shifting action in the input logic level translator.

A Request signal on an access channel results in a -5.8v "1" input, which is converted by the input logic level translator to a +1.7v "1". This sets FF1, which, in turn, disables the other priority circuits.

After a delay of 15 nanoseconds, the "1" reaches the AND into FF2. If a disable input is not being received, the output of the disable inverter is also a "1", so that FF2 is set. Then, after an additional 5-nanosecond delay, the "1" is ANDed with the set output of FF2 into the output inverter, where it becomes a +0.7v "0". This is converted by the output logic level translator to a -1.1v "0". The priority circuit therefore produces a logical inversion between input and output.

As soon as the access channel has been honored, the priority circuit is cleared by a -1.1v "0" input, which is converted by zener diodes to +5.1v, and is applied to the clear inputs of FF1 and FF2. This removes the disable from the other priority circuits so that a request on another channel may be honored.

CIRCUIT OPERATION

As shown on page 5-C77-3, except for the transistors in the output logic level translator, all of the priority circuit transistors are CDC 245010. This is a high speed silicon NPN type, having a typical gain bandwidth of 1 kmc, which provides a time per inversion of approximately 2 to 4 nanoseconds, depending upon the loading.

All of the CDC 245010 transistors have a base-to-collector tunnel diode network. This establishes an input current threshold level and holds the output voltages at the sum of the tunnel diode drops and the base-emitter junction drop.

The tunnel diodes used are CDC 245011. This is an axial tunnel diode having an I_p = 1 ma and a V_{fp} = 500 mv. Assuming an ideal case, two tunnel diodes in series would switch at 1 ma with a composite V_{fp} = 1v. Due to slight individual differences, no two tunnel diodes ever switch at exactly the same point, but the difference is negligible in this high speed circuit.

The input logic level translator performs the function of changing a -5.8v "1" into a +1.7v "1", and a -1.1v "0" to a +0.7v "0". Upon receipt of a -1.1v "0" input, the tunnel diodes are back biased and they are in the low voltage state. Thus the collector potential is held at the potential of the base, which is approximately +0.7v, being a grounded emitter silicon transistor. However, a -5.8v "1" input causes tunnel diode current to increase to a value in excess of 1 ma, so that they switch to the high voltage state. This causes transistor conduction to decrease, and the collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter voltage, a total of +1.7v.

The disable inverter and the output inverter circuits are for changing a +1.7v "1" to a +0.7v "0", and vice versa. In addition, the disable inverter also changes the +5.1v signal received through the zener diode to a +0.7v "0". Again, the output levels are taken from the collector, and the collector potential equals the sum of the tunnel diode voltages plus the base-emitter voltage of the silicon transistor. The time required for a transition from one state to the other is approximately 4 nanoseconds.

The amount of speed-up capacitance used on inverters of this type is dependent upon the particular input. A single OR input may have a fairly large speed-up capacitor; however, the speed-up capacitance on the OR inputs to the disable inverter must be kept small. This is because FF 1 on each priority circuit must drive four disable inverter inputs and is loaded too heavily if too much speed-up capacitance is used. Also, the speed-up capacitance on AND inputs must be small in order to prevent runt pulses and partial enables from satisfying the AND.

As shown on page 5-C77-3, the two flip-flops are each constructed of two inverter circuits provided with cross-coupled feedback from collector to base. These flip-flops are bi-stable circuits and are therefore capable of storing information.

The output logic level translator is quite similar to a logical inverter circuit, which is

discussed elsewhere. This circuit converts a +0.7v "0" to a -1.1v "0", and a +1.7v "1" to a -5.8v "1". It is capable of driving up to 8 logic cards, all of which may be either AND or OR, or any combination resulting in 8 loads total. The grounded emitter transistor is a PNP type CDC118021.The base bias is such that a +0.7v input allows it to switch on, producing a -1.1v "0" output, while a +1.7v input causes it to switch off, producing a -5.8v "1" output.

GROUND RULES

1. The priority circuit may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.
2. Lead length from FF 1 to the disable inverters on the other priority circuits must be less than 5 inches.
3. Only one priority circuit may be cleared by any one inverter, because a priority circuit requires approximately 15 ma of current for clearing.
4. One inverter may drive the lockout inputs of 4 priority circuits, because a lockout input requires approximately 4 ma.

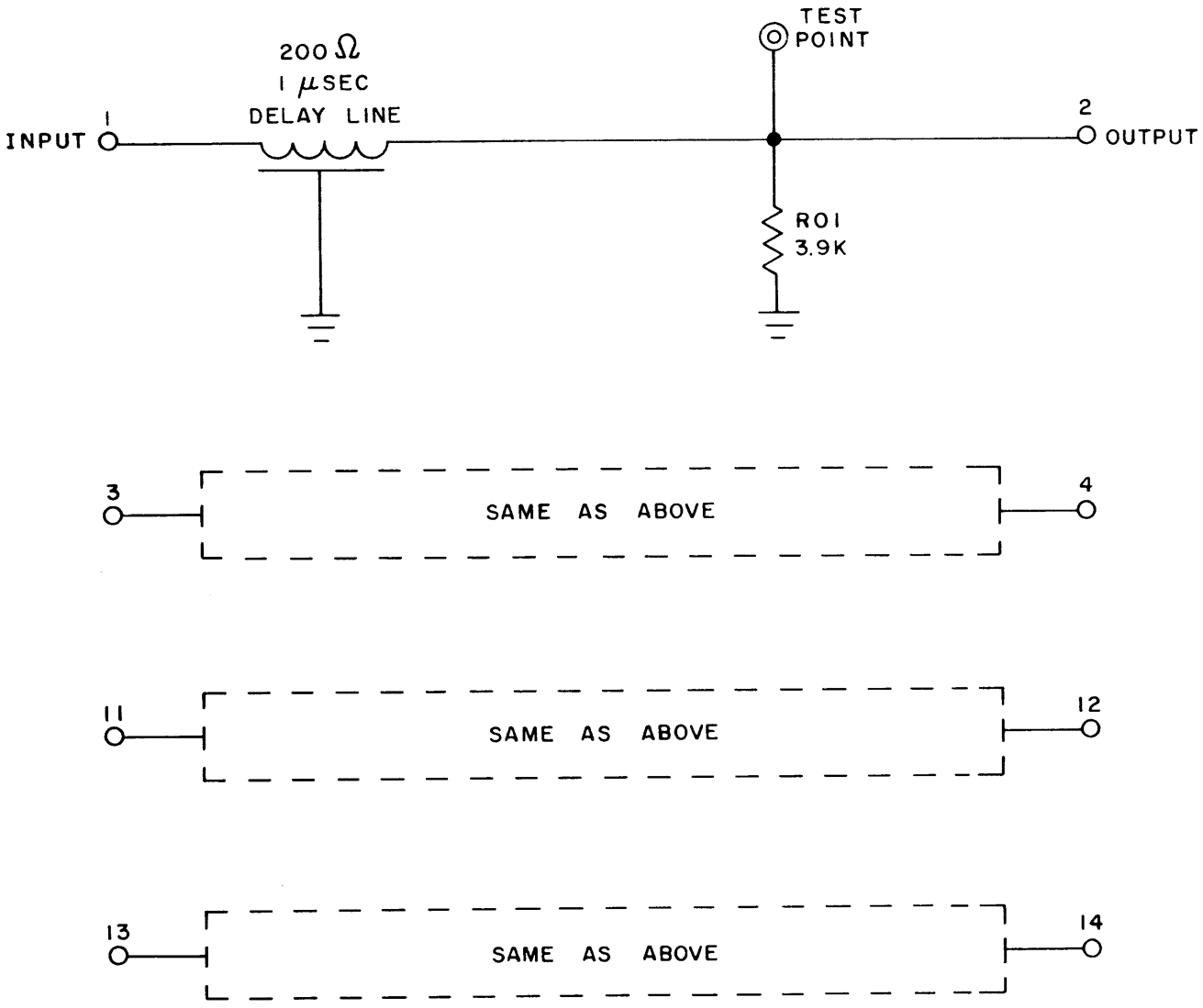
DELAY LINE, 1 USEC

Card Type C80

The function of this circuit is to provide an interval of time delay between successive logical operations. It is designed for use in applications requiring greater stability than may be obtained from capacitive delays.

The nominal 1 usec delay time applies to both "1's" and "0's", and the delay may be used to drive either an AND or an OR input. Attenuation through the delay line is negligible.

The characteristic impedance of the delay line is 200 ohms. The purpose of resistor R01 is to provide better impedance matching between the logic circuit input and the delay line output.



NOTE:

1. EACH DELAY MAY DRIVE ONE LOGIC CIRCUIT USING EITHER AN "AND" OR AN "OR" INPUT.

Delay Line, 1 usec C80

CRYSTAL OSCILLATOR

Card Type C81, 30 kc
Card Type C82, 83.4 kc
Card Type C83, 120 kc

FUNCTION

The function of these circuits is to produce accurately timed signals for controlling the Write operation in magnetic tape equipment. Information may be written on tape at rates of either 30,000, 83,400, or 120,000 frames per second. A single-phase sine wave output is taken from the oscillator tank and is converted by the circuit contained on card type C89 into a chain of square pulses at logic voltage levels.

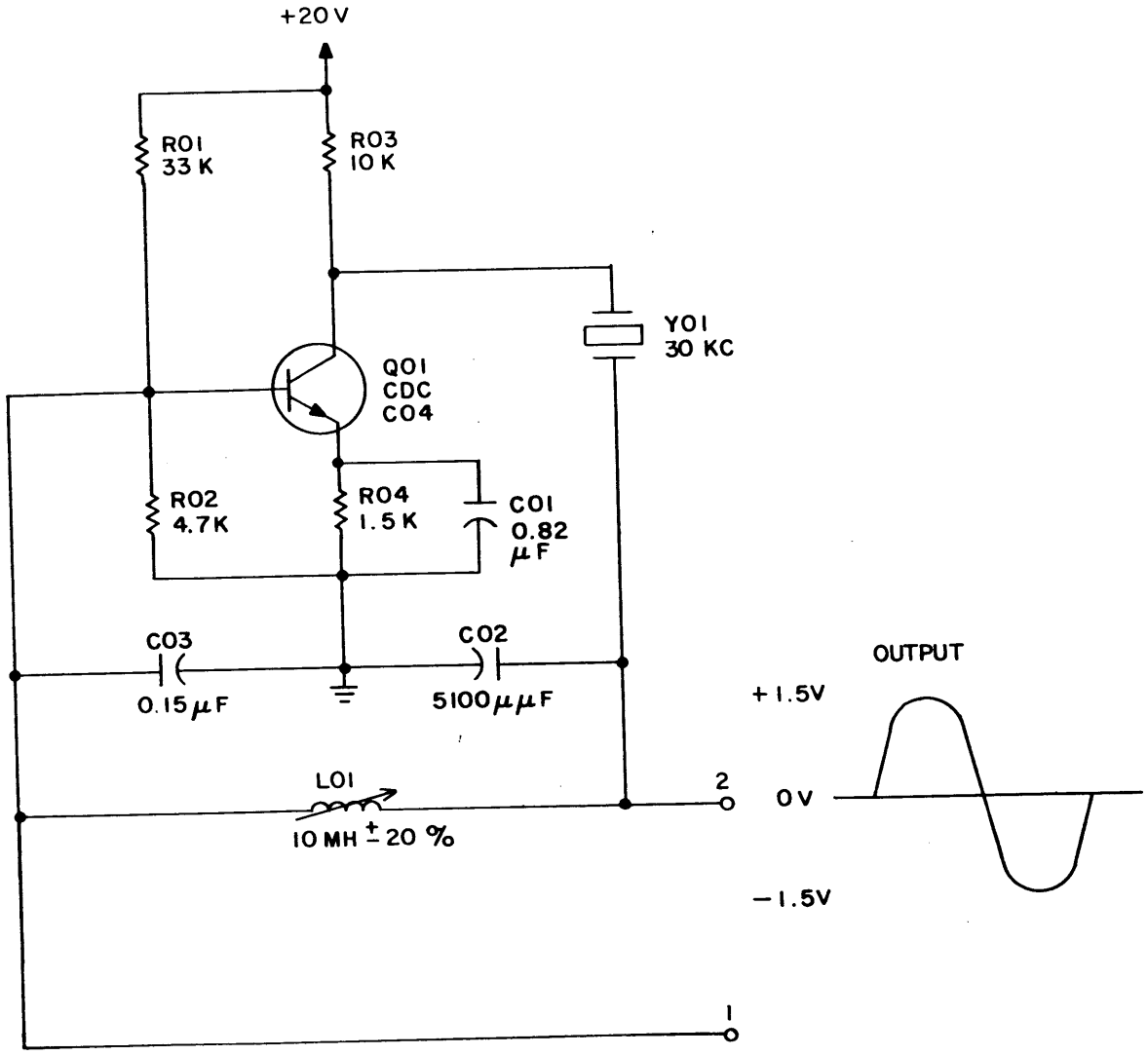
OPERATION

The circuit is essentially a Colpitts oscillator having a crystal filtered power amplifier. Opposite-phase outputs are taken from the oscillator tank and are available at pins 1 and 2 of the printed circuit card. Each output is a sine wave about ground; however, the peak-to-peak amplitude of the output at pin 2 is approximately 3 volts while that at pin 1 is approximately 0.5v.

Sufficient gain to maintain oscillation is provided by transistor Q01, which is connected as a Class C power amplifier. Q01 is an NPN silicon transistor capable of providing a current gain greater than 25 with a collector current of 400 ma. Transistor Q01 is driven both into saturation and cut off, so that its collector voltage is approximately a square wave.

The square wave signal from the collector of Q01 is filtered by the crystal filter Y01 into a sine wave at the fundamental frequency. Y01 is a high impedance quartz crystal having a Q value of the order of 10^5. It exhibits a frequency stability of 0.005 percent over the range $25^{\circ}C \pm 35^{\circ}C$, and a long-term stability with time of 1 ppm per week.

The oscillator tank consists of capacitors C02, C03, and the inductance L01. The values of these components are shown in the accompanying diagrams. Inductance L01 is adjustable through a range of approximately ± 20 percent, so that the tank may be tuned to the center frequency of the crystal.

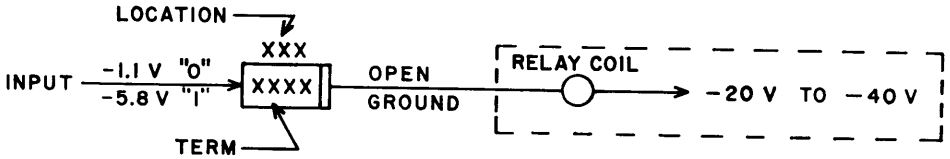


Crystal Oscillator, 30KC C81
(Others are similar)

COMPUTER DIVISION
PRINTED CIRCUIT DESCRIPTION
RELAY DRIVER
Card Type CA84A

FUNCTION

The function of this circuit is to enable a low impedance path from ground to the circuit output, upon receipt of a -5.8v "1" input. The circuit is designed to switch a current of the order of 1 ampere flowing in a highly inductive load such as a relay coil. A diode clamp connection is provided at the collector of Q02, so that a high-voltage inductive transient induced when current is interrupted does not damage the transistor.



LOGIC DIAGRAM SYMBOL

RELATED DOCUMENTS	NUMBER
Parts List	30933400
Assembly Drawing	30933400
Schematic Drawing	30933500
Engineering Specification	None

OPERATION

The two circuits on the card are identical and are labeled A and B. The following discussion applies to either circuit, but the component numbers mentioned are those appearing in circuit A.

The circuit has one logical OR input, and a 3-way AND. An unused OR input has no effect on the circuit, while an unused AND input, if left open, acts as a steady "1." Thus if the entire AND group is unused, at least one pin must be grounded.

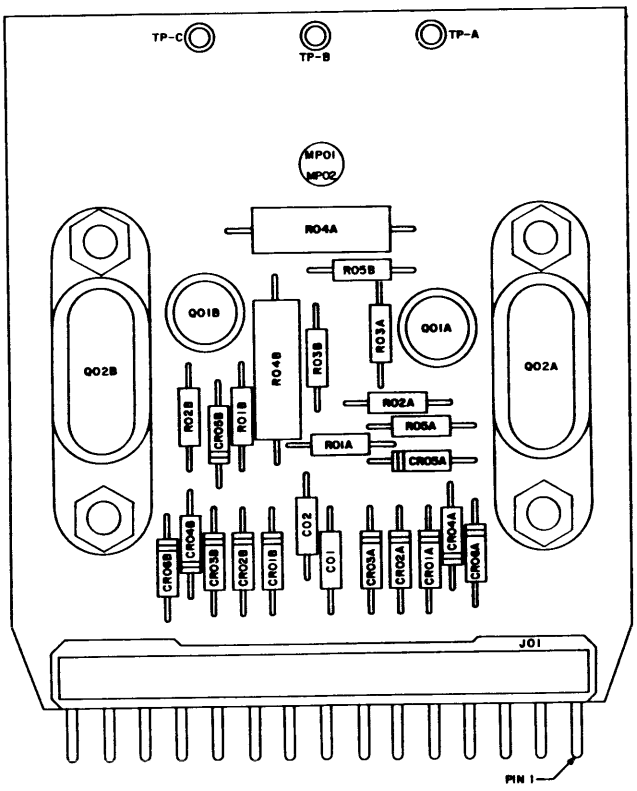
A -1.1v "0" input holds the base of Q01 at a low negative voltage with respect to the emitter, so that Q01 conducts relatively little. However, a -5.8v "1" input

results in a base current sufficiently large so that Q01 conducts heavily.

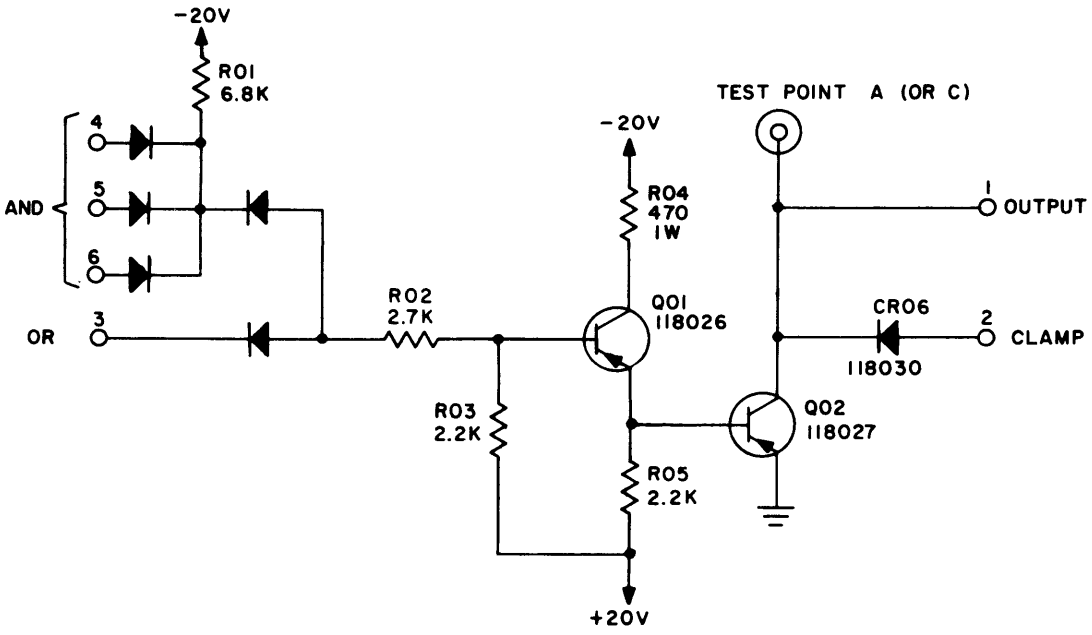
Transistor Q02 is a grounded emitter stage driven by the emitter follower Q01. When Q01 switches on, it attempts to bias the base of Q02 well into the negative voltage region, so that Q02 also switches on the conducts heavily. Likewise, when Q01 switches off, Q02 switches off and the positive voltage source applies a reverse bias to the base-emitter junction of Q02 so that it is well into the cut off region.

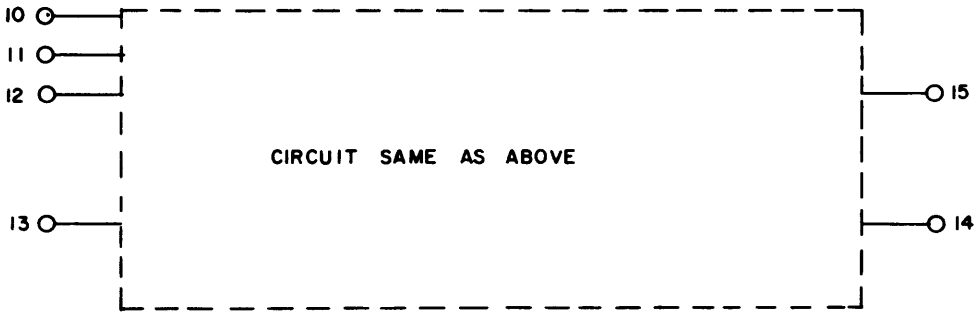
GROUND RULES

1. Any inductive load must be by-passed by the clamp diode.
2. The power supply voltage which drives the load must not exceed 40 volts.
3. With a 40v supply, load current cannot exceed 0.5 ampere; with a 20v supply, load current cannot exceed 1 ampere.
4. In case an entire AND group is unused, at least one of the inputs must be grounded.



COMPONENT LAYOUT





NOTE:

1. A -5.8V "1" INPUT CAUSES TRANSISTORS TO SWITCH TO CONDUCTION STATE.
2. LOGIC DIODES ARE 245021.

Relay Driver C84

STROBE SHAPER
Card Type C85

FUNCTION

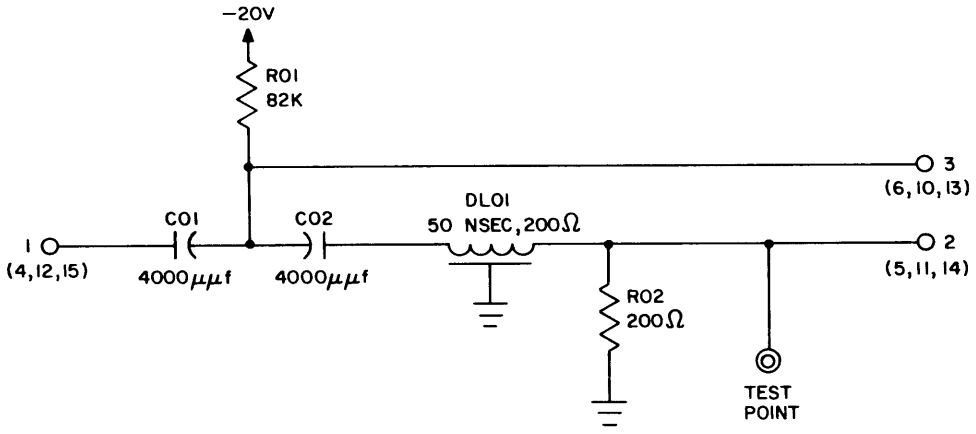
This circuit operates with a Receiver circuit contained on card type C61. Their function is to convert a delay line output (received via an Emitter Follower circuit on card type C07) into a -1.1v "0" pulse 50 nanoseconds in length.

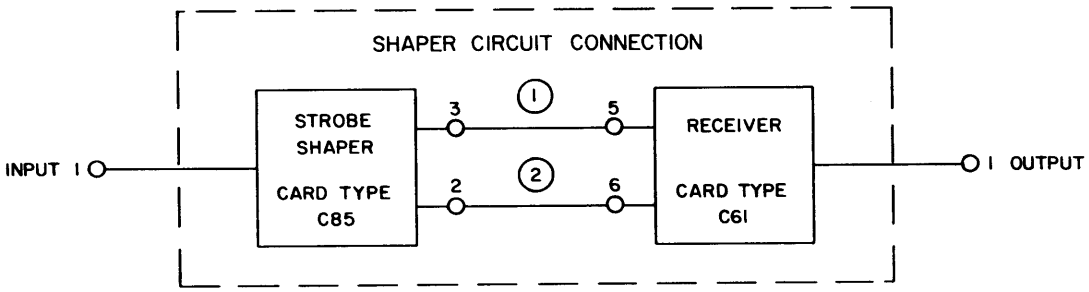
OPERATION

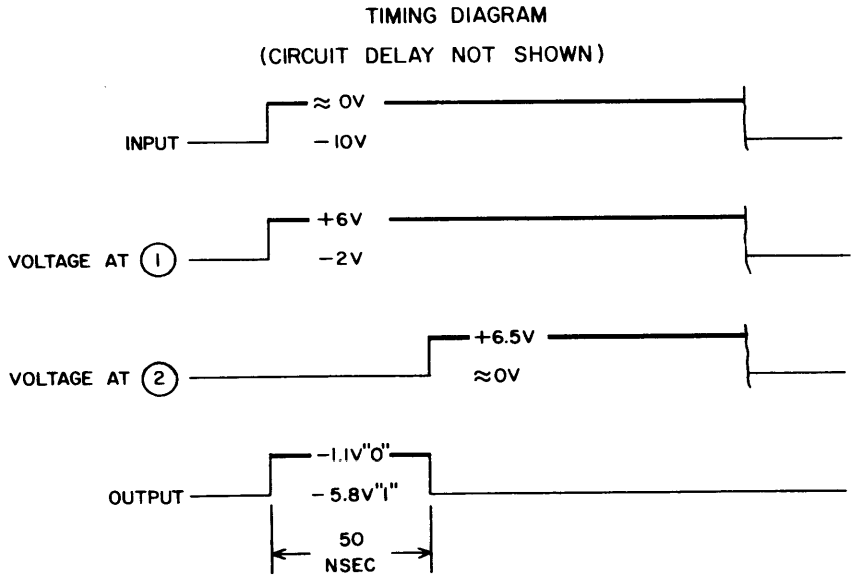
As shown on the accompanying diagram, the input from the Emitter Follower circuit is a positive-going pulse with a swing from -10v to ground, approximately. This input is received by the Strobe Shaper circuit and immediately appears on one of the outputs, causing the Receiver output to switch to -1.1v "0". After a delay of 50 nanoseconds, the input signal appears on the other output, causing the Receiver output to return to -5.8v "1". When the input signal drops, the bias from -20v through R01 holds the Receiver output at -5.8v "1".

Capacitors C01 and C02 isolate the input and the delay line output from the -20v bias voltage. The d-c levels of the input and output are approximately the values shown in the timing diagram.

The delay line is 50 nanoseconds, with a 200-ohm characteristic impedance. The 200 ohm resistor R02 provides impedance matching between the delay line and the Receiver input.







Strobe Shaper C85
(Four Circuits per card)

AMPLIFIER - SHAPER
Card Type C89

FUNCTION

The function of this circuit is to convert the sine wave output of a crystal oscillator into a chain of -5.8v "1" pulses of approximately 0.2 us duration. The input is a sine wave about ground with a peak-to-peak amplitude of approximately 3v. The -5.8v "1" pulse output is produced immediately after the input crosses the zero axis in the positive-going direction.

OPERATION

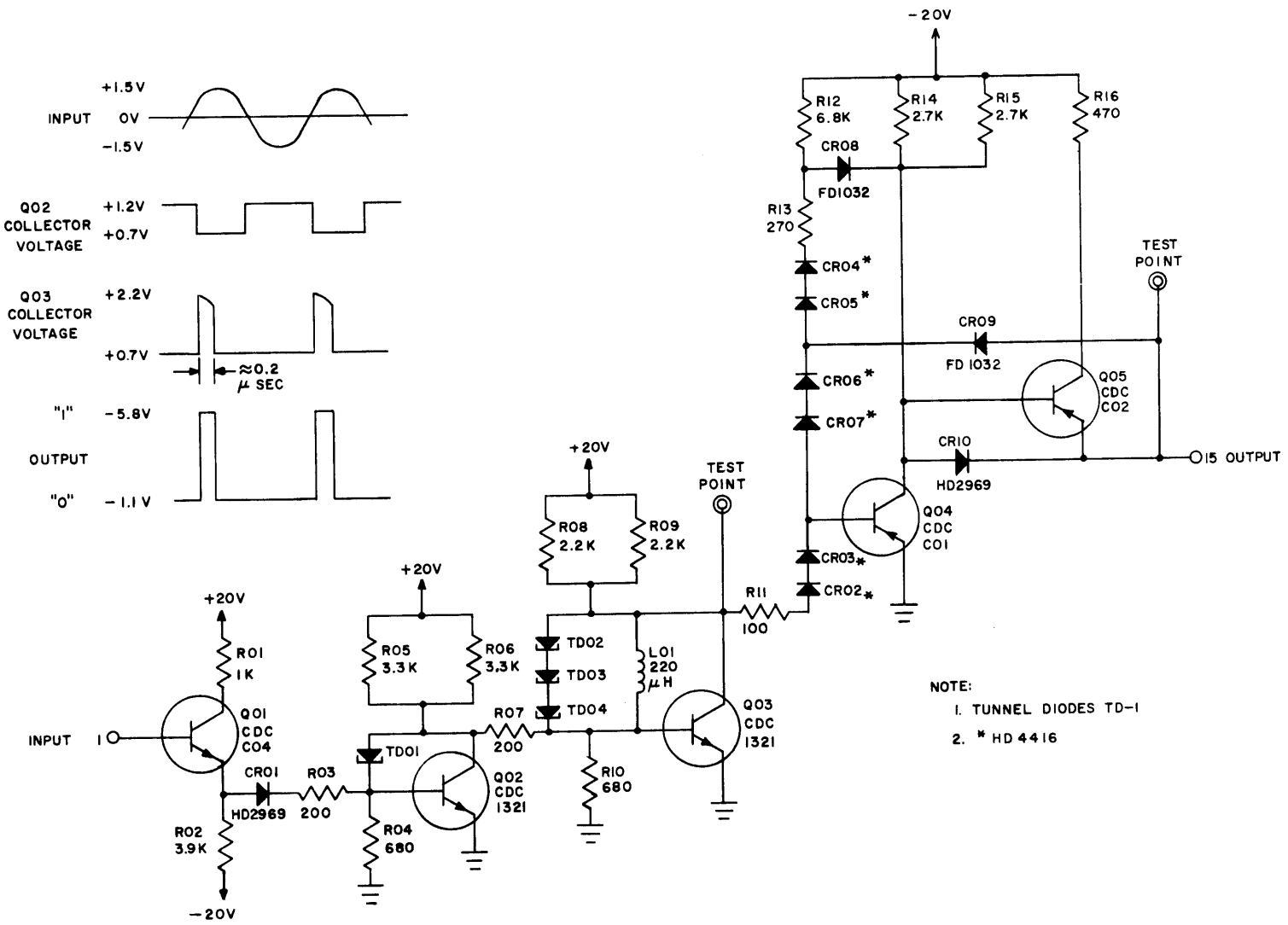
The width of the output pulse is approximately 0.2 us and is determined by the 200 uh inductance L01. The repetition rate of the output is determined by the frequency of the input signal.

The input signal is applied to the base of transistor Q01, which is an NPN silicon type CDC C04. In this application, it is used as an emitter follower current amplifier providing drive current for transistor Q02.

Transistors Q02 and Q03 are CDC 1321, which is a high speed NPN silicon type having a gain-bandwidth of 1 kmc. Each of these transistors has a base to collector tunnel diode network which produces an essentially square waveform and establishes its voltage level.

The tunnel diodes used are type TD-1. This is an axial tunnel diode having an I_p = 1 ma and a V_{fp} = 500 mv. Assuming an ideal case, the three tunnel diodes connected to Q03 would switch at 1 ma with a composite V_{fp} = 1.5v. Due to slight individual differences, no two tunnel diodes ever switch at exactly the same point, but the difference is negligible in this high speed application.

As shown in the accompanying diagram, a positive-going input results in a -5.8v "1" output of approximately 0.2 us duration. As the input goes positive, Q01 provides drive current to Q02 so that it switches to a state of heavy conduction. This results in minimum current flow through TD01 so that it switches to its low voltage state. The collector voltage of Q02 is therefore approximately equal to its base-emitter junction drop of +0.7v, being a grounded emitter silicon transistor. Transistor Q02 in its conduction state allows current flow to increase through TD02, TD03, and TD04, so that they switch to their high voltage states. This causes conduction through Q03 to


INPUT
+1.5V
0V
-1.5V
Q02 COLLECTOR VOLTAGE
+1.2V
+0.7V
Q03 COLLECTOR VOLTAGE
+2.2V
+0.7V
≈0.2 μ SEC
"1"
-5.8V
OUTPUT
"0"
-1.1V
-20V
R12 6.8K
R14 2.7K
R15 2.7K
R16 470
CR08
FD1032
R13 270
CR04*
CR05*
CR06*
CR07*
CR09
FD 1032
TEST POINT
Q05 CDC C02
CR10
HD2969
15 OUTPUT
Q04 CDC C01
CR03*
CR02*
R11 100
+20V
R08 2.2K
R09 2.2K
TD02
TD03
TD04
L01 220 μH
Q03 CDC 1321
R10 680
R07 200
R05 3.3K
R06 3.3K
TD01
Q02 CDC 1321
R04 680
R01 1K
Q01 CDC C04
INPUT 1
CR01
HD2969
R03 200
R02 3.9K
NOTE:
1. TUNNEL DIODES TD-1
2. * HD 4416

decrease, and its collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter junction drop, a total of +2.2v. This voltage level causes Q04 to switch to a state of minimum conduction and the circuit output becomes a -5.8v "1".

The length of the -5.8v "1" output pulse is determined by the 220 uh inductance L01. The tunnel diodes are able to switch state almost instantaneously while current through the inductance increases exponentially. After a time of approximately 0.2 us, current through the inductance has increased to the point that the tunnel diodes are effectively by-passed and they return to their low voltage states. This reduces the collector voltage of Q03 to approximately +0.7v, which causes Q04 to conduct heavily and returns the circuit output to a -1.1v "0".

A negative-going circuit input prevents Q01 from providing drive current to Q02. This allows current through TD01 to increase, causing it to switch to its high voltage state. Conduction through Q02 decreases and its collector voltage becomes equal to the sum of the tunnel diode voltage and the base-emitter junction drop, a total of +1.2v. This provides forward drive to the base of Q03, holding the circuit in the quiescent state.

The portion of the circuit consisting of Q04, Q05, and their associated biasing network is similar to a logical inverter, which is discussed elsewhere. It is capable of driving 8 AND loads, 8 OR loads, or any combination resulting in 8 loads total.

READER LEVEL AMPLIFIER
Card Type C91

FUNCTION

This card contains two identical circuits, the function of which is to convert solar cell outputs from a punched card reader into logical "0" signals of -1.1v. The circuit input is driven by one of the solar cells at a card reading station. When the solar cell senses a hole in the card, the circuit output switches to a -1.1v "0". If no hole is sensed, the output remains a -5.8v "1".

OPERATION

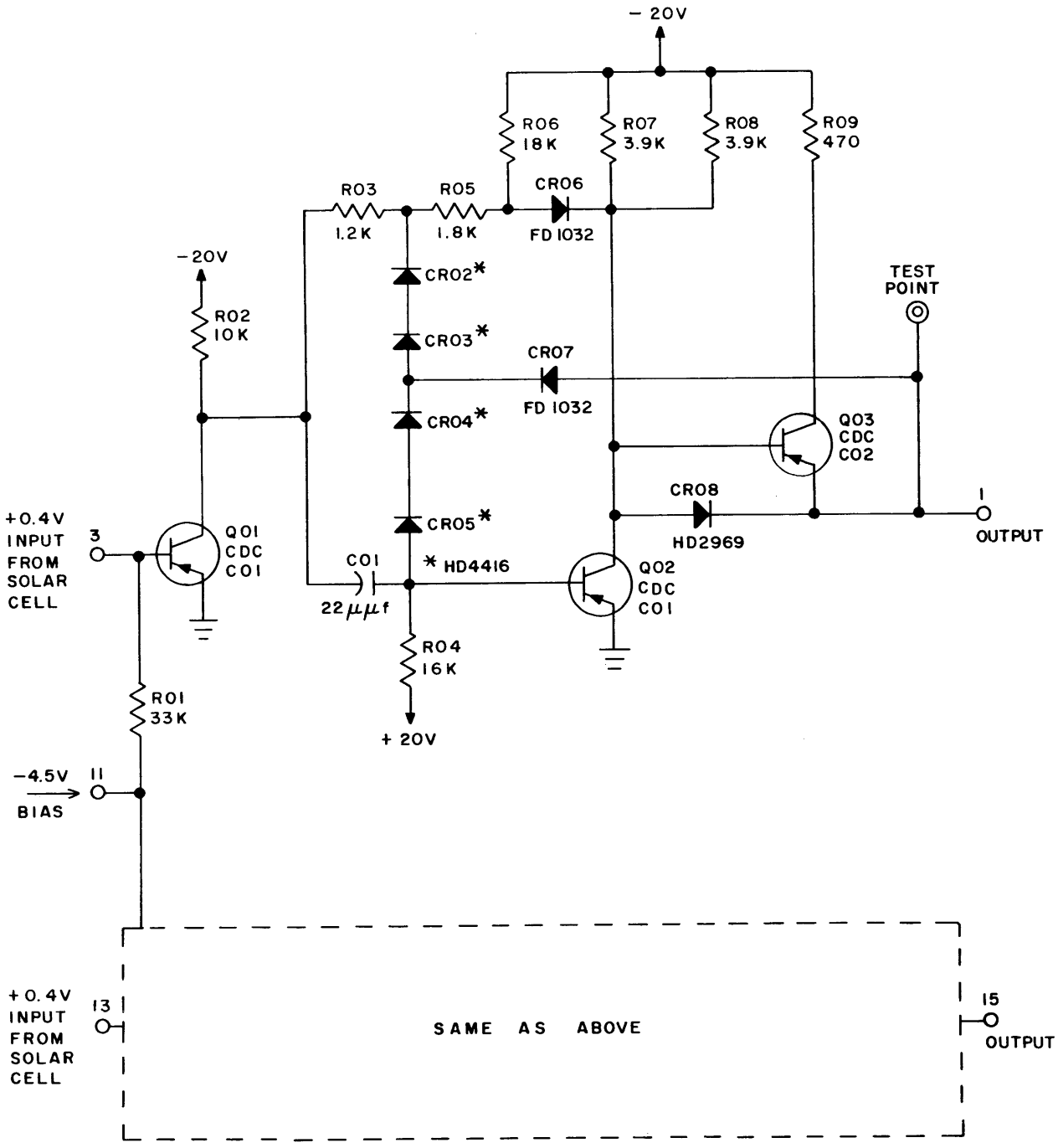
Inputs to the circuit are provided by a solar cell at the card reading station, and the signal levels are +0.4v and open circuit. The +0.4v signal results when light shining through a hole in the punched card activates the solar cell. If a hole is not present, light is prevented from striking the solar cell and its high impedance produces essentially an open circuit. Any leakage current is not more than a few ua.

The two circuits on this card are single inverters having one OR input which is fed by the network consisting of resistors R01, R02, and transistor Q01. In both circuits, the base of transistor Q01 is biased through resistor R01 to the -4.5v supply at pin 11.

An open circuit input allows the -4.5v supply at pin 11 to apply a strong forward bias to the base of Q01. This causes Q01 to conduct heavily and its collector potential becomes approximately -0.5v. The low collector voltage of Q01 is applied to the cathode of input diode CR01 and causes the inverter to provide a -5.8v "1" output.

A +0.4v input reverse biases the base-emitter junction of Q01 so that Q01 is cut off. Its collector potential rises toward -20v, but is clamped at approximately -6v by the input impedance of the inverter and the drop across R02. The -6v collector potential of Q01 is applied as an input to the inverter and causes its output to switch to a -1.1v "0".

The remainder of the circuit is identical to a logical inverter which is discussed elsewhere. It is capable of driving 8 AND loads, 8 OR loads, or any combination resulting in 8 loads total.



Reader Level Amplifier C91

OVERLOAD PROTECTOR
Card Type C94

FUNCTION

This circuit provides protection from excessive current flow in the memory drive lines (labeled X and Y in the 3600 system). In addition, it monitors the drive and inhibit voltages and disables the logic if any of these voltages fall below operating level. As shown in the accompanying diagram, the circuit contained on card type C94 operates in conjunction with other power supply components which are mounted elsewhere. The memory drive power supply system is disconnected if the type C94 card is removed from its connector.

Typical external connections to a C94 card are shown on page 5-C94-3. For the actual wiring of the Overload Protector circuit in the 3609 Storage Module, see the 3609 Diagrams manual, Pub. No. 60042000.

OPERATION, Over-Current Protectors

The card contains two identical circuits for dropping power if a current overload occurs in the X or Y drive scheme. This is shown with the principal current paths indicated by heavy lines. Normal current flow to the X or Y gate circuits is of the order of 900 ma. If this should increase to approximately 1.4 amperes, the voltage drop across the 18-ohm resistor causes the transistor to switch to its conduction state, firing the silicon controlled rectifier.

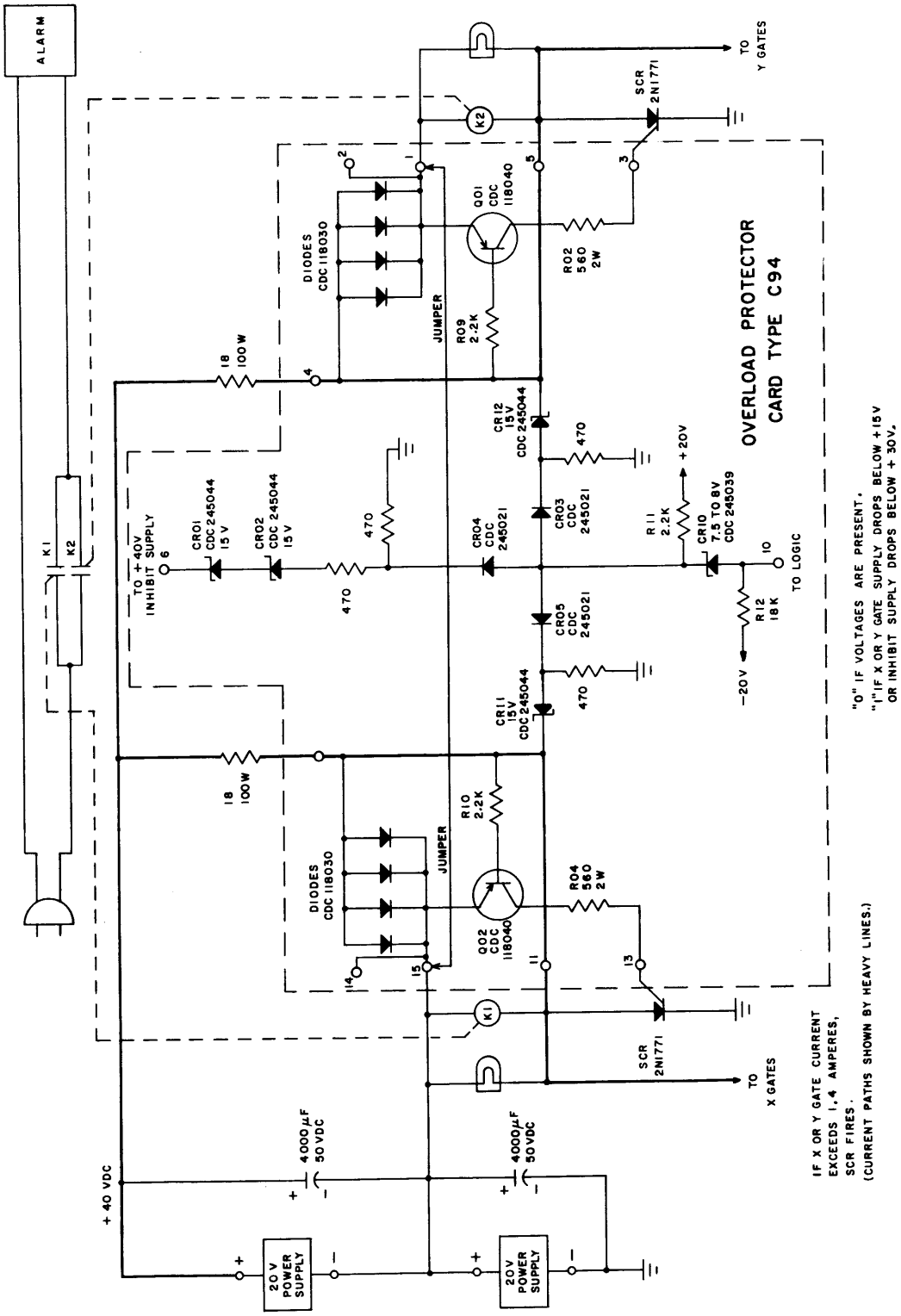
During normal operation, the rank of four CDC 118030 diodes are in a state of heavy forward conduction and the drop across the 18-ohm resistor is very close to 19.3v. The output supplied to the gate circuits is the voltage at the anodes of the diodes and is around 20.7 volts (20v plus 0.7v forward diode drop). A heavier output current results in a greater drop across the 18-ohm resistor, and when the current reaches approximately 1.4 amperes, the diodes cut off. A further increase in current draws turn-on current through the transistor causing it to switch on, which fires the silicon controlled rectifier (SCR).

As shown in the diagram, the SCR in its high conduction state grounds the output to the gate circuits, lights an indicator, and closes a relay to sound an alarm. The SCR may be returned to its OFF state by lowering the power supply voltages to zero.

OPERATION, Voltage Monitor

This portion of the circuit monitors the +20v gate supplies and the +40v inhibit supply. If these three voltages are present, a "0" output of approximately -0.7v appears at pin 10. If the inhibit supply falls below +30v, or if either gate supply falls below +15v, this output switches to a "1" of approximately -6.5v, disabling the operation of the memory logic.

A 3-way AND connection is provided by diodes CR03, CR04, and CR05, so that a low input voltage to any diode results in a "1" output. A level-shifting action is provided by the zener diode CR10. This diode is back biased sufficiently so that the voltage across it is a constant 7.5 to 8v.



Overload Protector C94

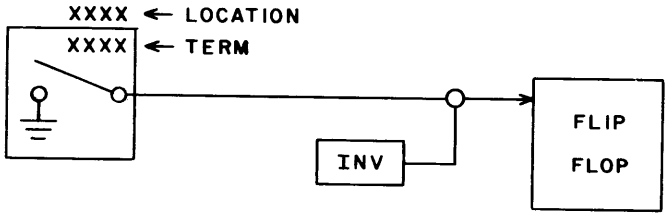
COMPUTER DIVISION

PRINTED CIRCUIT DESCRIPTION

CHANNEL DISABLE
Card Type CA97

FUNCTION AND OPERATION

This card contains a single-pole, double-throw toggle switch and a biasing network by which the output pins may be held at either -6.8 volts or ground, representing a logical "1" or "0". The card is designed to be used as a controlling input to an AND gate, providing a means of manually disabling the input.

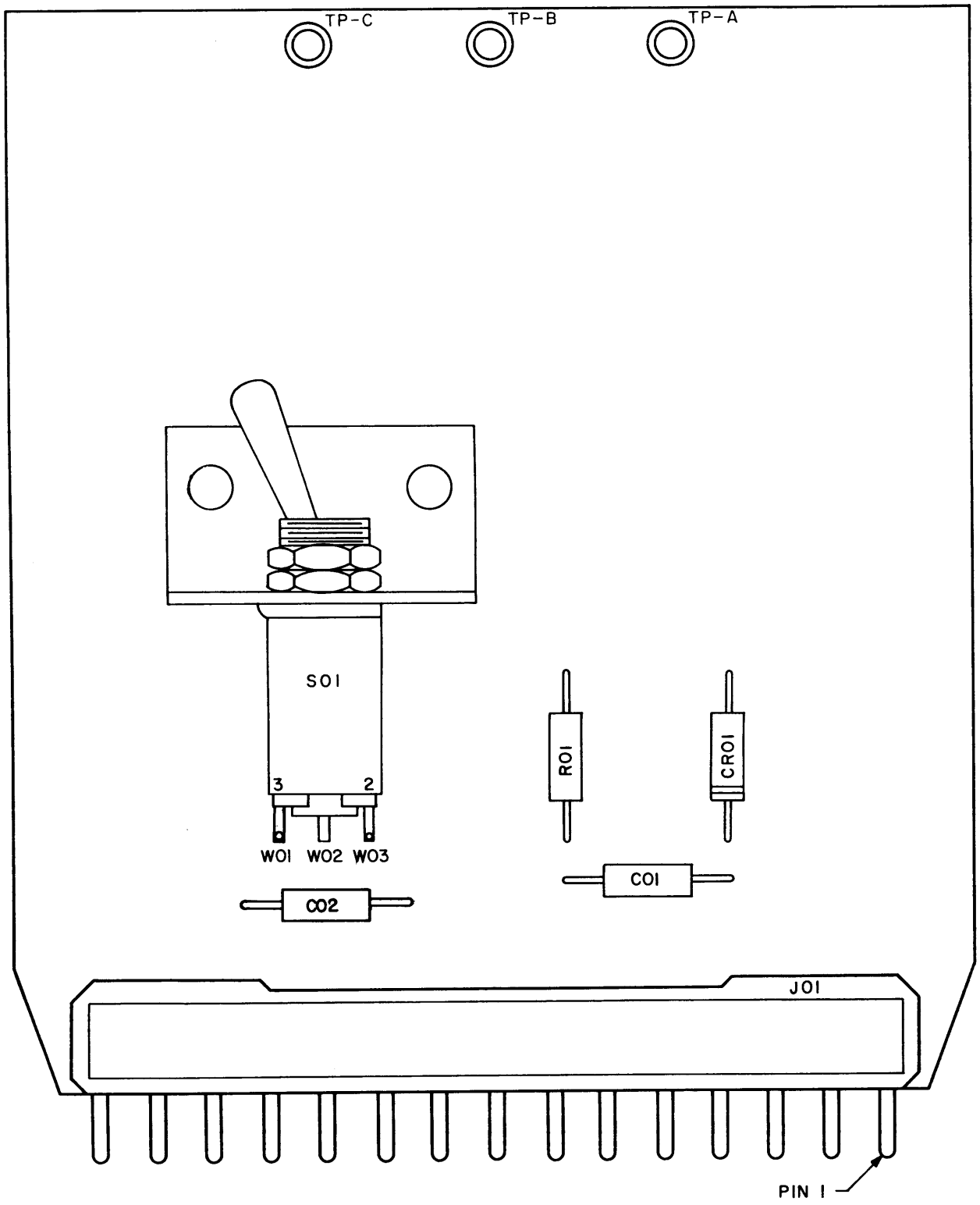


LOGIC DIAGRAM SYMBOL

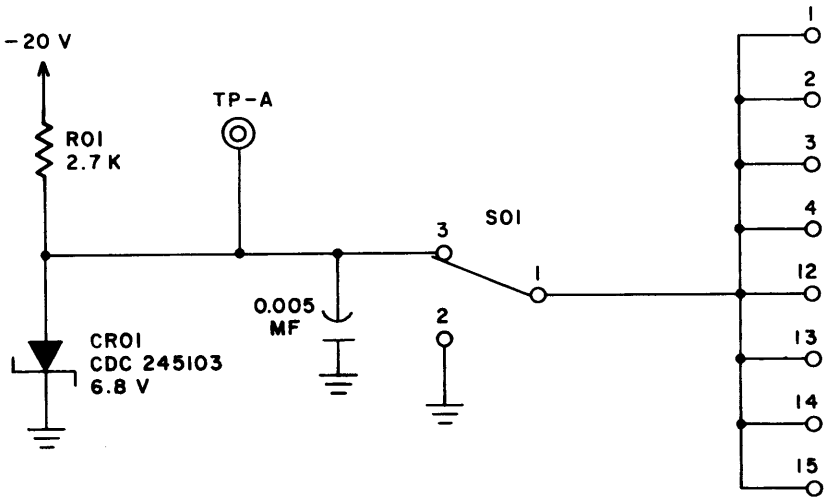
RELATED DOCUMENTS	NUMBER
Parts List	30938600
Assembly Drawing	30938600
Schematic Drawing	30938700
Engineering Specification	None

GROUND RULES

1. Each output can control 12 AND gates.
2. Because of the size of the switch, the card location adjacent to the component side of the CA97 card cannot be used.



COMPONENT LAYOUT



Channel Disable CA97

CAPACITIVE DELAY
Card Types C67, K67, C68, C69, C70, C71, K71

FUNCTION

The function of a capacitive delay is to provide an interval of time delay between successive logical operations. This is done by regulating the length of time required for a logical "1" to pass through the delay circuit. The delay time for a logical "0" is approximately one-tenth of the delay time for a logical "1".

The circuits contained on card types C67, C68, C69, C70, and C71 provide delay times ranging from 20 nanoseconds to 40 ms, and are shown on pages 5-C67-5 through 5-C67-10. In addition, the delays on card types C68 and C69 may be varied through a range of approximately ±15 percent by means of the variable resistor R02.

OPERATION, Card Types C67, C71, and K71

A delay circuit configuration is shown on page 5-C67-5, with typical waveforms. It consists of a capacitor from the signal line to ground, having a source of charging current through a series resistance with the voltage regulated by a 15v zener diode. The delay time from A to B is the time required to charge the capacitor to the input threshold level of inverter B when the output of inverter A switches to a -5.8v "1".

The charging voltage is stabilized at a constant 15 volts by a zener diode. The delay time is therefore proportional only to the RC time constant of the series resistance and the capacitance, and is not affected by small line voltage variations. On card types K67, C68, and C69, the series resistance is variable by means of a 2k potentiometer. This provides a close adjustment of the delay times through a range of approximately ±15%.

The AND input contains FD 1032 silicon diodes having a voltage drop of approximately 0.6v; thus point ① on page 5-C67-5 is always 0.6v more negative than the logic-level input. The voltage across the capacitor is controlled by the level of the input signal. With a -1.1v "0" input, this voltage is approximately -1.7v. When the input from A switches to a -5.8v "1", the voltage at point ① approaches -6.4v in an exponential curve according to the rate at which charging current flows into the capacitor. At the threshold level of approximately -3v, inverter B switches state.

OPERATION, Card Types K67, C68, and C69

The circuit contained on these cards is designed to provide stable delay times of relatively long duration. It consists of a capacitive delay followed by a double inverting network such that the circuit does not produce an over-all logical inversion.

The circuit output characteristics are similar to those of a logic card, and it drives a maximum of 8 logic card loads. These may be 8 AND loads, 8 OR loads, or any combination up to 8 loads total.

As discussed in the previous section, the delay time is the time required to charge the capacitor to the threshold level of the following inverter when the circuit input switches to the -5.8v "1" level. The threshold level at which the inverter switches state is approximately -3v, but often varies slightly from card to card. From an examination of the exponential charge curve of the capacitor, it is seen that a small variation of the threshold level makes an appreciable difference in the delay time. This variation can be eliminated by always using the same inverter with a given capacitive delay. Mounting the inverter on the same card ensures that the capacitive delay always drives the same inverter and the threshold remains essentially constant.

As discussed previously, the input logic diodes are high speed devices having a voltage drop of approximately 0.6v. This holds the anode of zener diode CR05 at a potential 0.6v more negative than the logic-level input.

Zener diode CR05 functions as a threshold-setting device. The breakdown voltage of CR05 is approximately 4.9v; thus with its anode held at -6.4v by "1" inputs, CR05 applies approximately 1.3v of forward drive to the base of Q01. As the circuit input goes negative, conduction increases through CR05 and resistor R05. When current flow through R05 reaches approximately 0.36 ma, the negative-going input starts to draw turn-on current from transistor Q01. The input continues moving negative to the -5.8v "1" level, causing Q01 to conduct heavily.

A -1.1v "0" input holds the anode of CR05 at approximately -1.7v. In this state, CR05 does not have sufficient bias to hold it in the zener breakdown region. The base of Q01 is therefore held at a low positive voltage by resistors R05 and R06, and Q01 is cut off.

Base drive for transistor Q02 is taken from the collector of Q01. When -5.8v "1" inputs cause Q01 to conduct heavily, its collector holds the base of Q02 at approximately -0.5v, so that Q02 is in a state of minimum conduction. The collector voltage of Q02 is clamped

at approximately -6v by resistors R07, R08, and diode CR06.

The -6v level is applied to the base of Q03 and its emitter is isolated by CR07. Transistor Q03 is connected as an emitter follower, and in this state, it can supply OR current for 8 logic card loads.

A -1.1v "0" input causes Q01 to cut off and its collector voltage rises toward -20v, causing transistor Q02 to conduct heavily. The collector voltage of Q02 approaches -0.5v, and the circuit output becomes a logical "0". In this state, transistor Q03 is cut off and Q02 can supply AND current for 8 logic card loads.

Positive feedback is provided from the collector of Q02 to the base of Q01 by resistors R05, R06, and capacitor C09. This produces a regenerative effect which speeds the switching action.

OPERATION, Card Type C70C

This circuit is designed to provide an approximate linear delay, requiring 120 to 150 nanoseconds for the output to change from "0" to "1", and requiring 60 to 75 nanoseconds to change from "0" to the -3v threshold. The delay time from "1" to "0" is approximately one-tenth as long, or 10 to 15 nanoseconds.

With a -1.1v "0" input, the cathode of CR01 is near -1.3v. The two forward-drop diodes CR02 and CR04 hold the base of Q03 near ground. Transistor Q03 is connected as an emitter follower; thus the circuit output is equal to the base voltage less the base-emitter junction drop and in this state is approximately -0.8v.

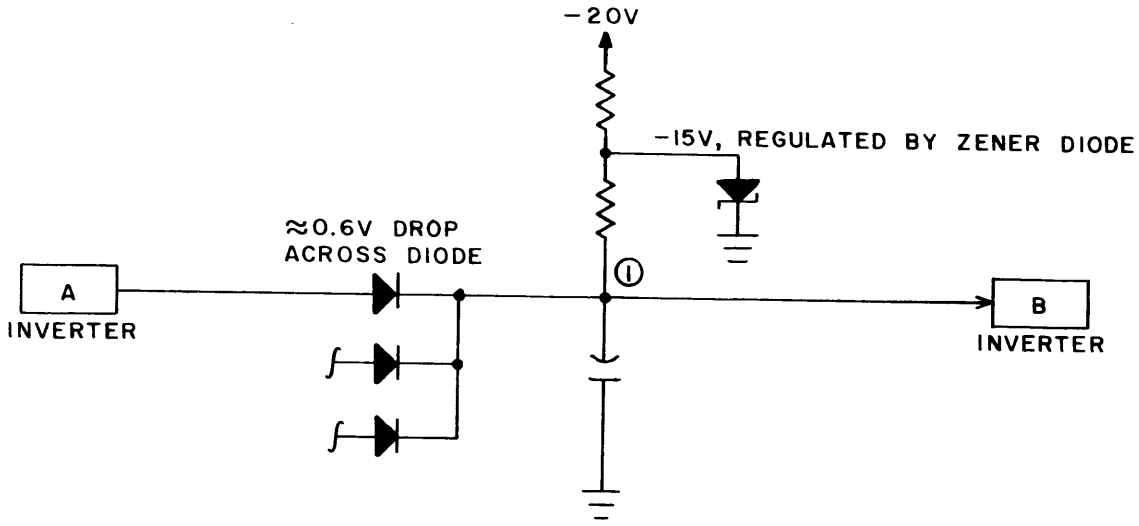
When the input switches to a -5.8v "1", capacitor C01 begins charging toward -6v. This causes conduction through Q01 to decrease so that the circuit output moves negative. However, the negative-going output is coupled back by the "bootstrap" connection of CR03, which is a 3v zener diode. This results in a nearly constant current of about 3.5 ma through resistor R02. Capacitor C03 is therefore charged at a nearly constant rate, resulting in a highly linear output.

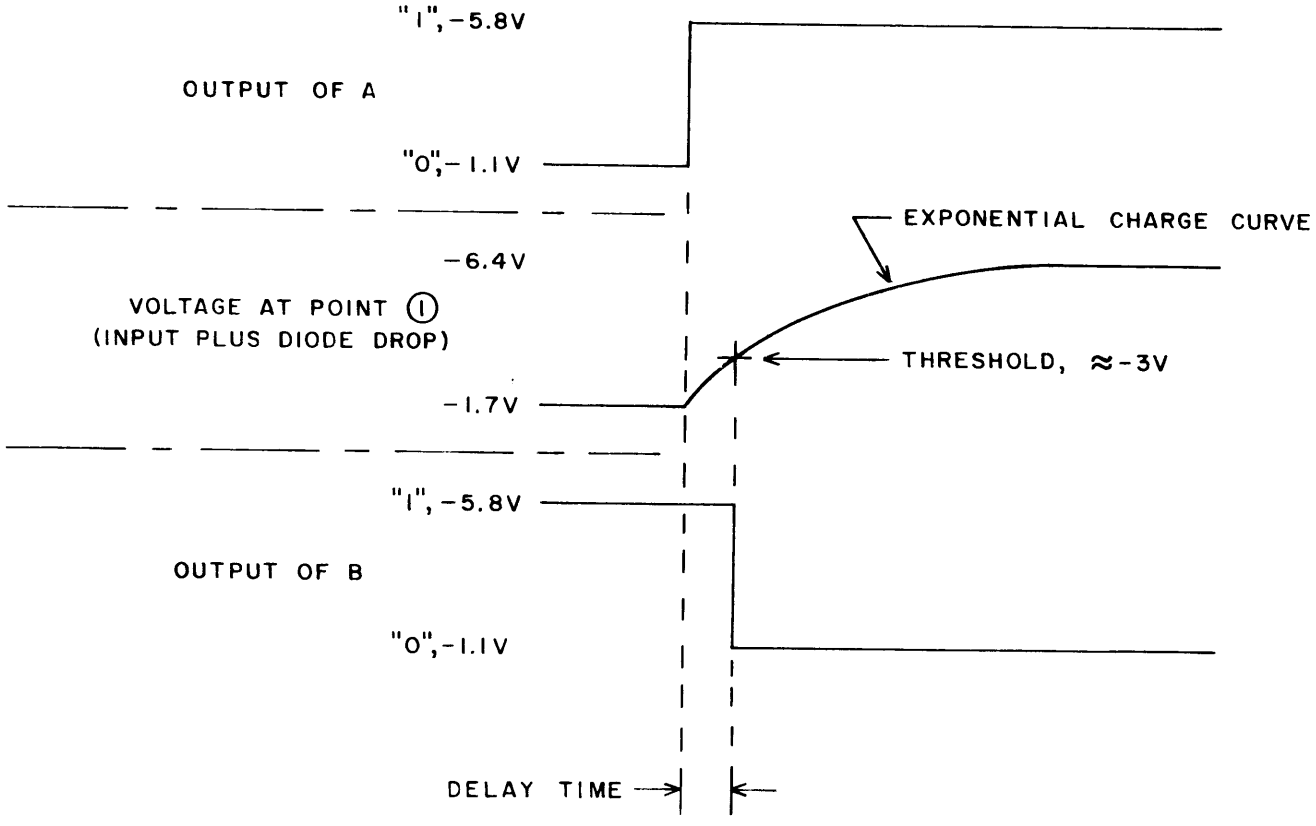
GROUND RULES

1. Each delay circuit contained on card types C67 and C71 may drive only one logic circuit.
2. The outputs of delay circuits contained on card types C67 and C71 must always connect to logic circuit OR inputs, while the circuit on Card Type K71

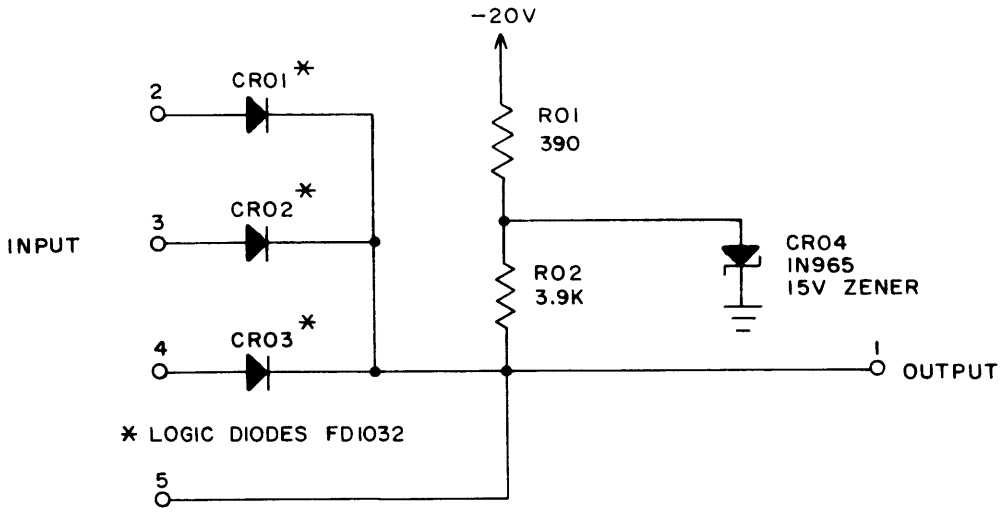
must drive AND inputs.

3. The delay circuits contained on card types K67, C68, and C69 may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.
4. The nominal delay times pertain to a logical "1".
5. The delay time for a logical "0" is approximately one-tenth of the corresponding delay time for a logical "1".

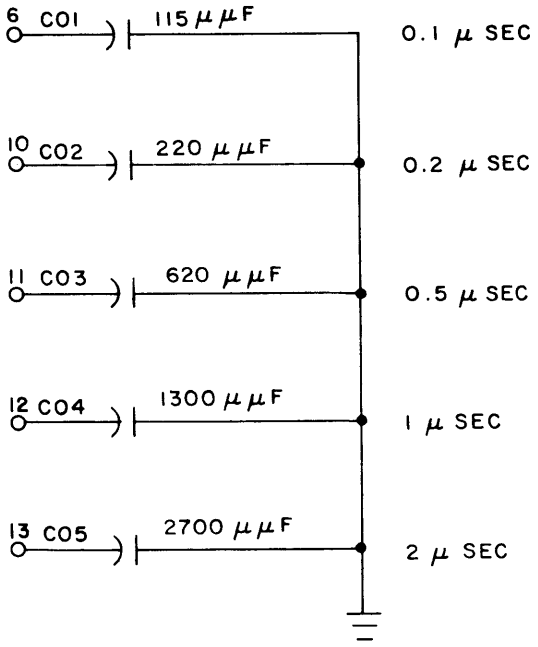




Typical Circuit Configuration



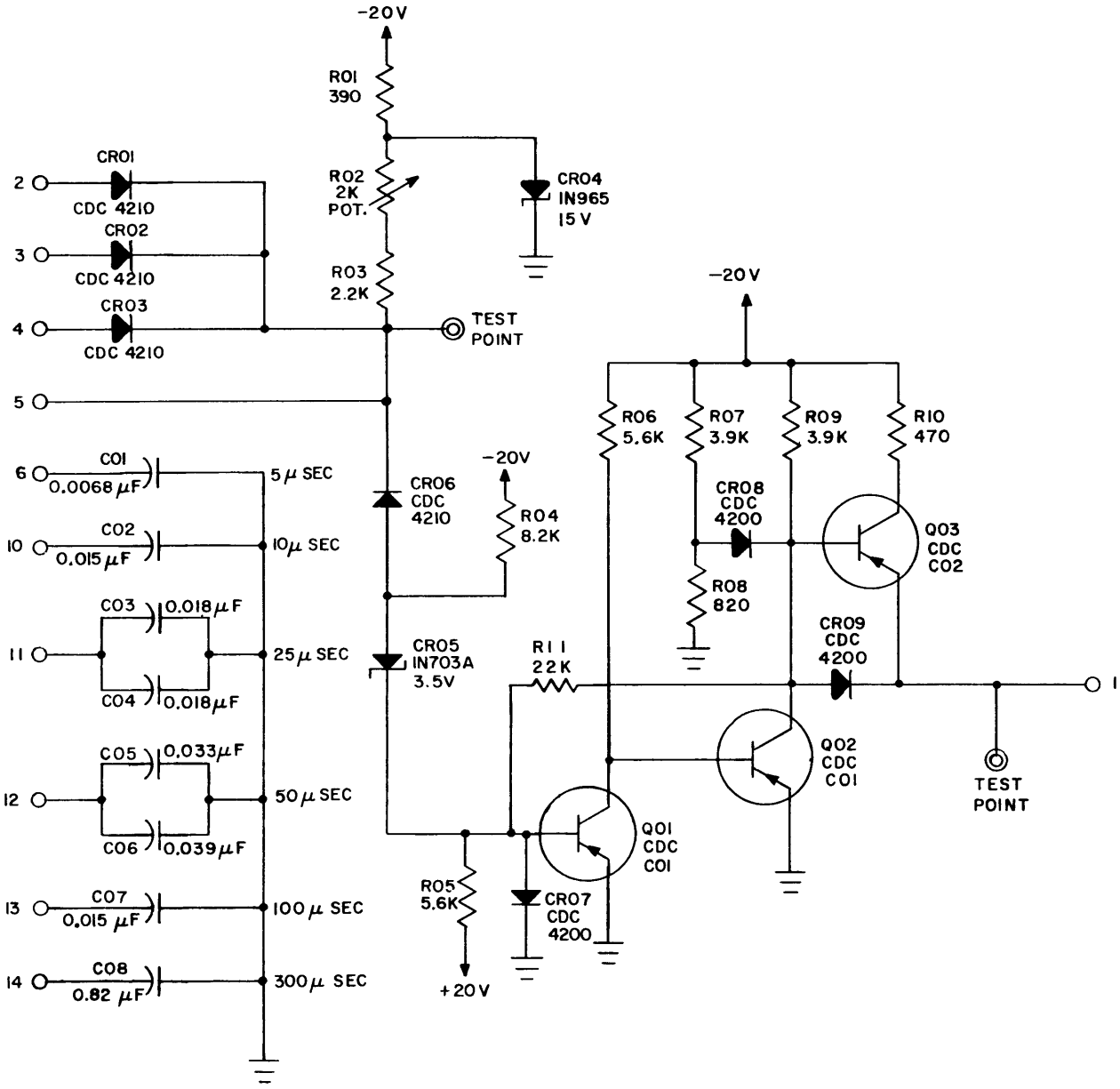
NOMINAL DELAY TIMES



NOTE:

1. AN EXTERNAL JUMPER CONNECTS PIN 5 TO THE DESIRED DELAY.
2. CARD TYPE K67 GIVES SAME DELAY TIMES, BUT CIRCUIT IS SIMILAR TO C68 AND C69.

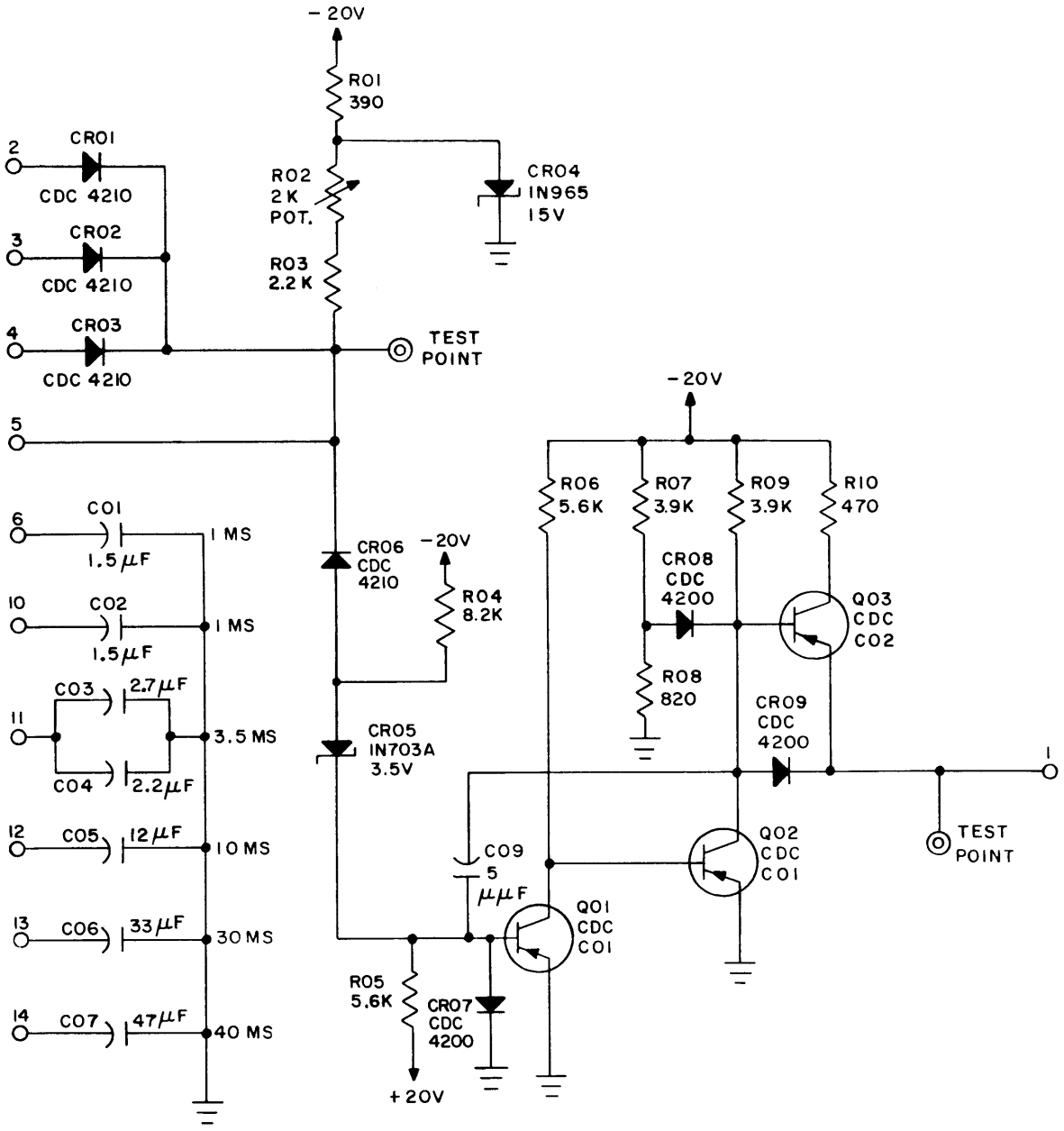
Capacitive Delay, Fixed C67



NOTES:

1. EXTERNAL JUMPER CONNECTS PIN 5 TO DESIRED DELAY.
2. NOMINAL DELAY TIMES VARIABLE ± 15% BY ADJUSTING R02.
3. THE CIRCUIT DOES NOT PRODUCE AN OVER-ALL INVERSION.

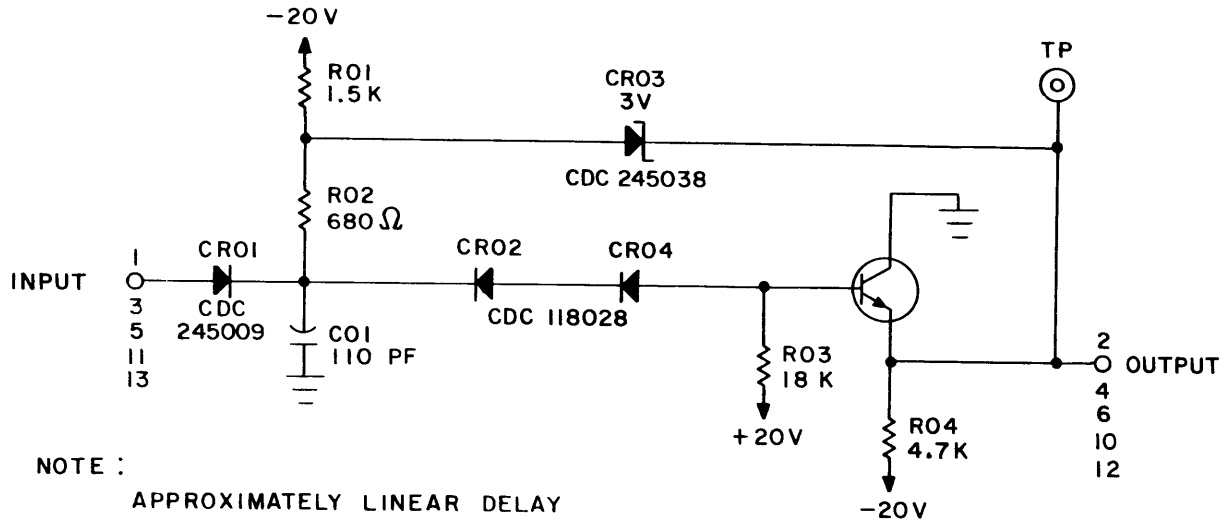
Capacitive Delay, Variable C68

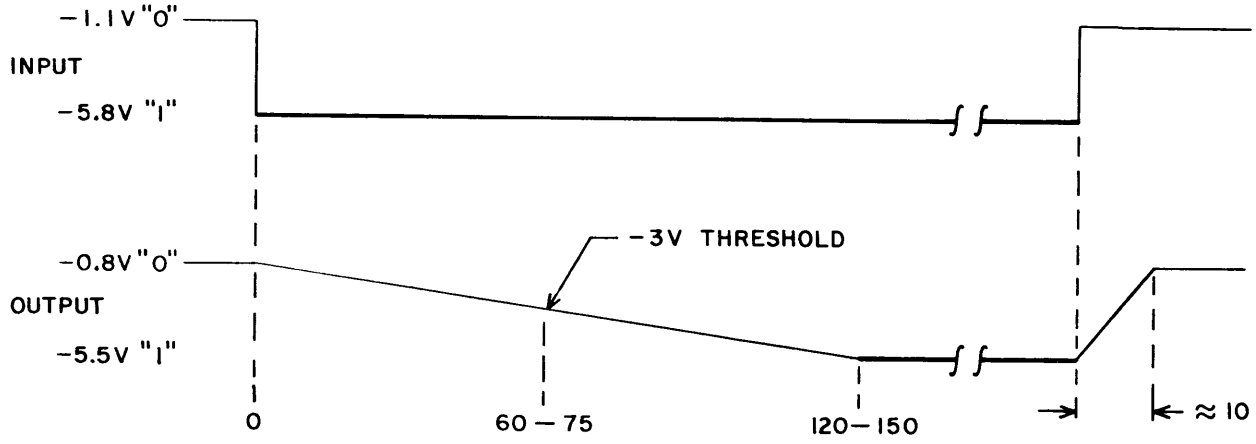


NOTES:

1. EXTERNAL JUMPER CONNECTS PIN 5 TO DESIRED DELAY.
2. NOMINAL DELAY TIMES VARIABLE ± 15 % BY ADJUSTING R02.
3. THE CIRCUIT DOES NOT PRODUCE AN OVER-ALL INVERSION.

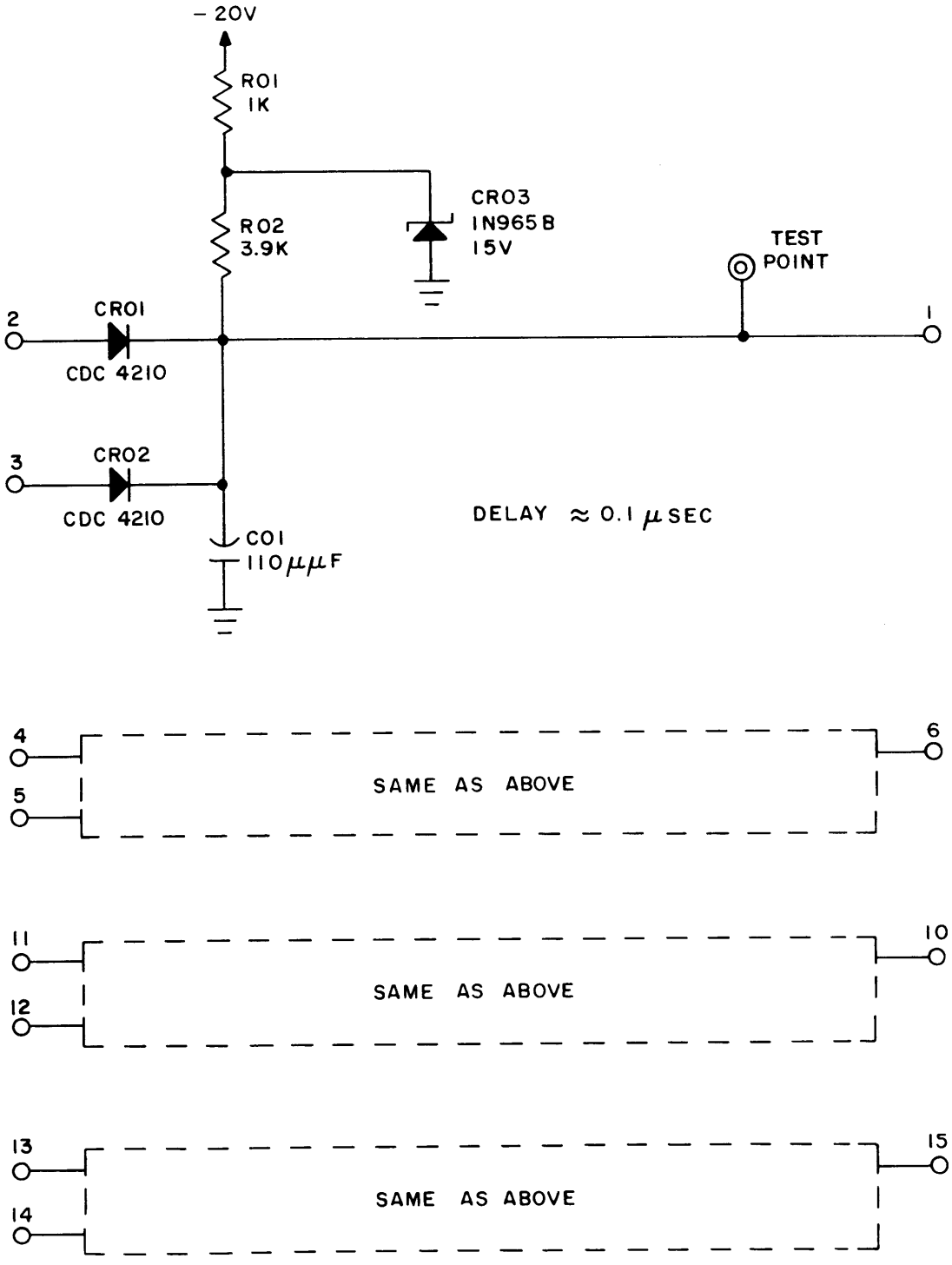
Capacitive Delay, Variable C69





NOTE :

ALL TIMES ARE IN NANOSECONDS.



Capacitive Delay, 0.1 usec C71

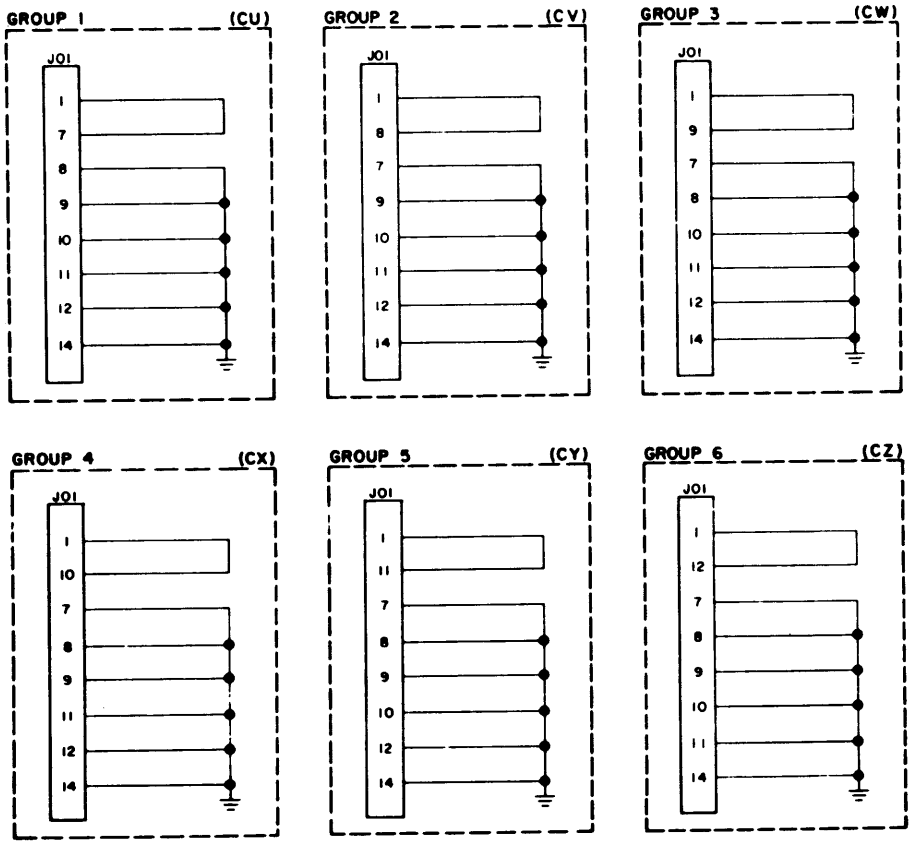
JUMPER
Card Type E00

E00 cards were developed by OPCONCTR for use in select identify circuits. These circuits enable each 160-A computer to identify itself, via program control, with respect to other 160-A computers in the system. Each of the six groups of jumper cards is wired to transmit one specific output pulse. Depending upon the bit location of the logical "1" in a Select Identify EXF code (1100), a particular jumper card will receive a pulse and transmit the pulse to its computer. Jumper cards have no active components.

E00 does not use pins 2, 3, 4, 5, 6, 13 and 15. Pin 14 is grounded. Pin 1 is the only input pin used. Pins 7, 8, 9, 10, 11 and 12 are output pins. The output of the card is dependent upon which output pin is connected to pin 1; the remaining pins are grounded. A logical "1" input to pin 1 from the set side of the select identify flip-flop produces a "1" on the output pin that is connected to pin 1. The logical "1" is fed through an L card to a 160-A computer.

"1" bit locations and the unit symbols of the computers they select:

Group 1 - CU - bit 6	Group 2 - CV - bit 7	Group 3 - CW - bit 8
Group 4 - CX - bit 9	Group 5 - CY - bit 10	Group 6 - CZ - bit 11


GROUP 1
(CU)
J01
1
7
8
9
10
11
12
14
GROUP 2
(CV)
J01
1
8
7
9
10
11
12
14
GROUP 3
(CW)
J01
1
9
7
8
10
11
12
14
GROUP 4
(CX)
J01
1
10
7
8
9
11
12
14
GROUP 5
(CY)
J01
1
11
7
8
9
10
12
14
GROUP 6
(CZ)
J01
1
12
7
8
9
10
11
14

Jumper E00

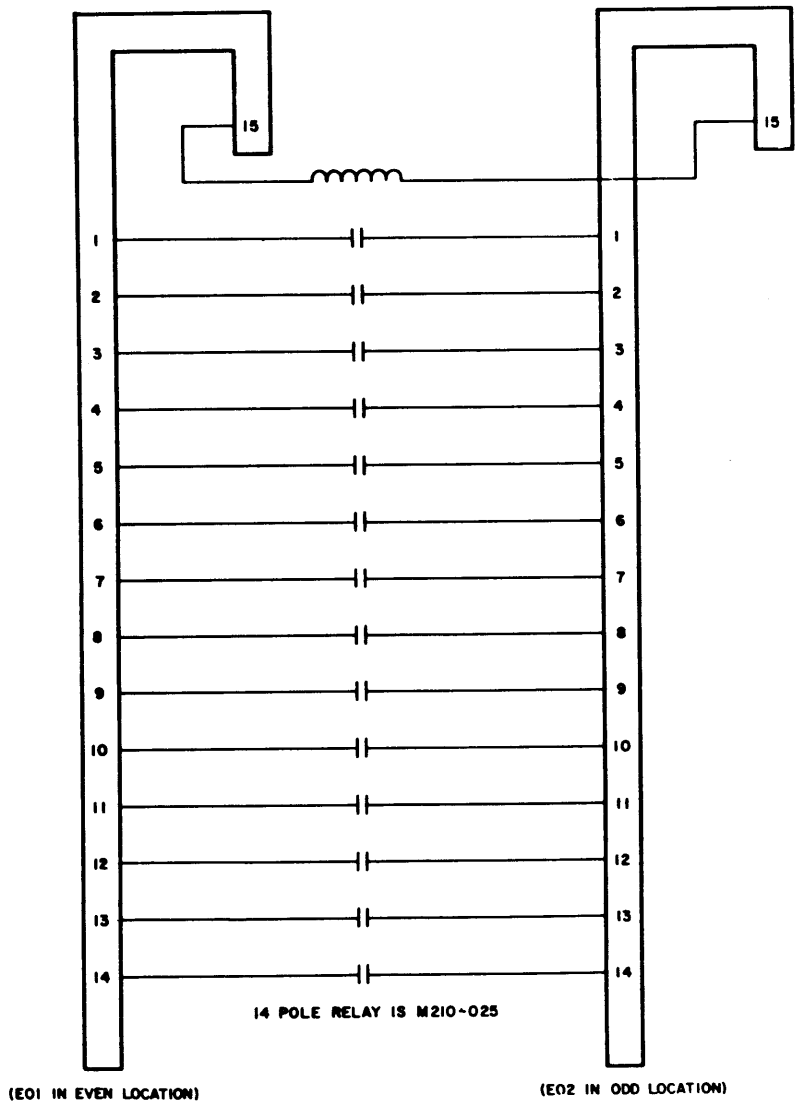
CROSSPOINT MODULE

Card Types E01A and E02A

Crosspoint Module (CM) is an assembly of a 14-pole relay. The 14-pole relay, encapsulated and enclosed in an aluminum box, is between two printed circuit cards, E01A and E02A. The module has a 30 pin connector.

The relay consists of 14 miniature dry-reed switches. The simultaneous opening and closing of the 14 switch contacts is controlled by a single d-c operating coil. The coil-resistance is about 250 ohms and dissipates about 16 watts when energized with 20 volts, giving an operating current of about 80 ma. The operating and release time is about 5 usec. The life expectancy of a single reed is about 100,000 cycles.

Each reed switch is hermetically sealed in a glass capsule containing approximately one atmosphere of nitrogen. The switch consists of two nickel-iron alloy reed elements with contacts of diffused gold. The reed switch contacts are Form A, normally open. They close when a magnetic field of the required strength is applied.



Crosspoint Module E01A & E02A

CROSSPOINT CONTROL MODULE
Card Type E03A and E04A

The Crosspoint Control module consists of selection and latching relays and an Override switch. The two relays, (housed in separate cans), the override switch, and two diodes are mounted between two printed circuit cards E03A and E04A. The module has a 20 pin connector. The two diodes are used for inductive suppression. All the odd numbered pins are on E03A;, even numbered pins on E04A. Of 30 pins, only pin numbers 4, 6, 8, 12, 14, 16, 26, 28, and 30 are used; the remainder are open.

SELECTION RELAY

The selection relay consists of a Form A type reed switch and two magnetic coils excited separately. In order to close the reed switch in the relay, both coils must be energized simultaneously. However, to keep the switch closed only one coil need be energized. Since the coils are slow to magnetize, they are slow to damp out after the excitation pulse has been removed. This limits the rate at which the relay can be selected. A rate of 400 cycles per second is normal.

LATCHING RELAY

The latching relay is a Form C bi-stable device with two coils of reversible polarity. It switches the relay from one state to the other. The coil operates at a power of 300 mw with an operate time of 3 ms. A supply of 20v is needed to energize the relay.

The form C dry-reed switch has 3 contacts. The center contact (or movable reed) is located between the other two contacts. Biasing is accomplished by positioning permanent magnets adjacent to the reed leads. One reed is induced with the "N" polarity and the other with the "S" polarity.

If the release coil is excited, the center reed switches to the normally closed (NC) reed. If the operate coil is excited, the center reed switches to the normally open (NO) reed. If both coils are energized at the same time, the latching relay does not change its state.

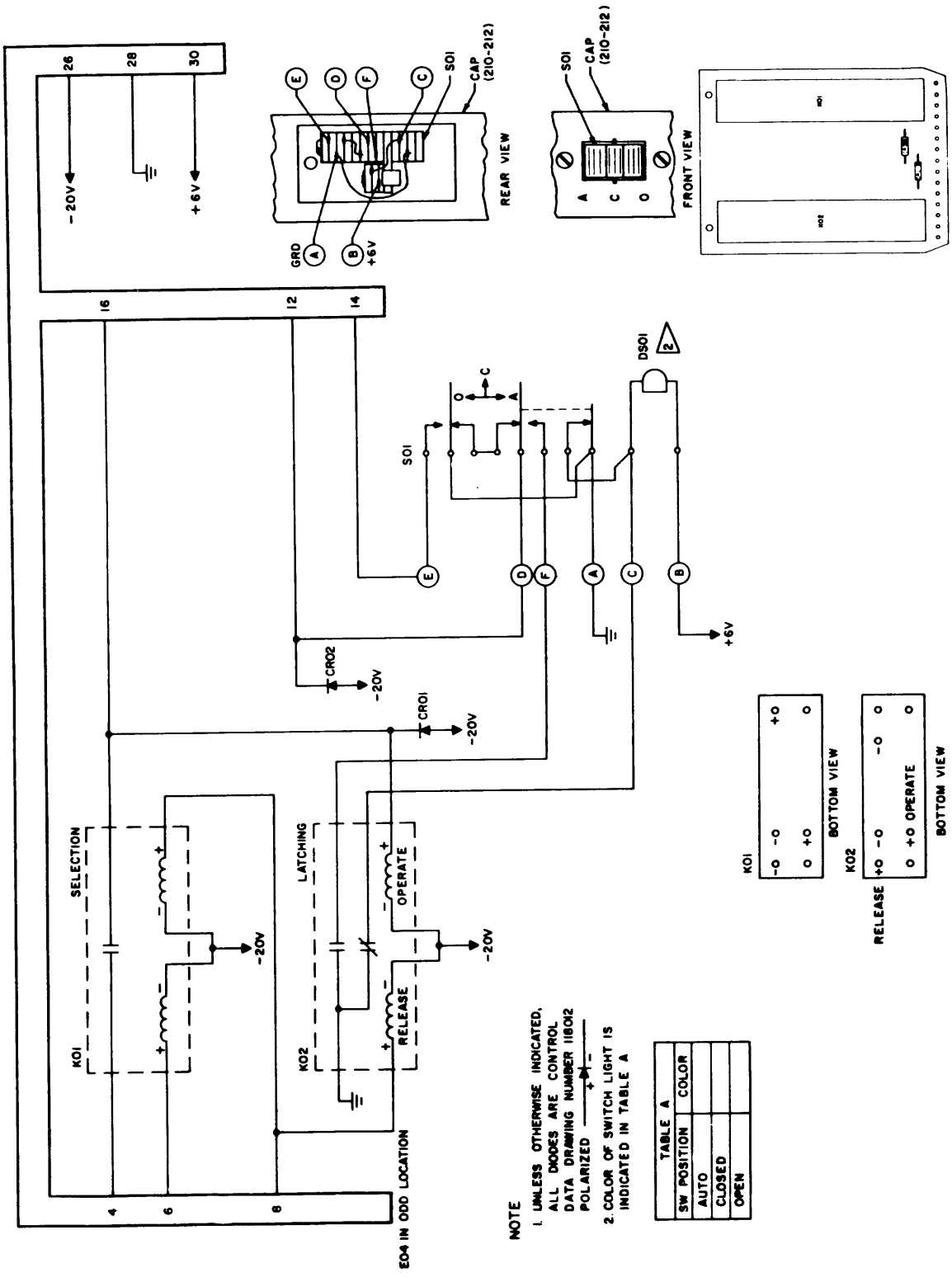
OVERRIDE SWITCH

The Override switch has three positions: Automatic (A); Closed (C), and Open (O). Each position of the Override switch is indicated by a lighted colored background.

In the A position, the circuit to the 14-pole relay coils may be either Open or Closed. In the A position, the selection or deselection of a crosspoint is automatic. The amber light is off if the latch relay is closed to the 14-pole relay (crosspoint made). The light is on if the contact is open.

In the C position, the circuit to the 14-pole relay coils is always closed.

In the O position, the circuit to the 14-pole relay coils is always open.



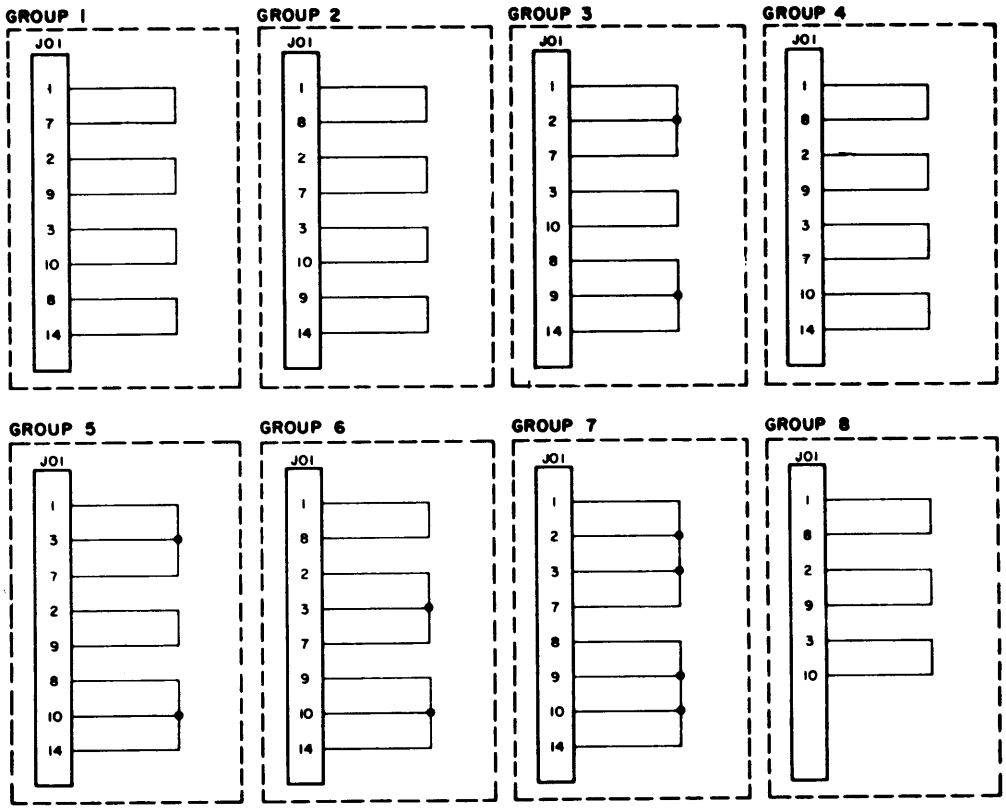
Crosspoint Control Module E03A & E04A

DECODER

Card Type E05

Function decoders are primarily used in the selection of equipment and peripheral device controllers. The cards receive function codes from computers and decode them, providing proper address bits for the selection of devices. The decoder cards are similar to other printed circuit cards in appearance, but have no active components. If the required pins are connected, the cards can decode any octal digit (0-7). Groups 1-7 decode octal digits 1-7 respectively; group 8 decodes 0.

Card E05 does not use pins 4, 5, 6, 11, 12, 13 and 15. Pin 14 is grounded. The outputs from function translators are fed to pins 1, 2 and 3. Decoding is accomplished by interconnecting various combinations of pins 1, 2 and 3 with pin 7. Logical "1" inputs ANDed with pin 7 produce logical "1" outputs. Logical "0" outputs are produced by ANDing inputs with some pin other than pin 7. Logical "0" outputs are fed through an inverter to a gate where they are ANDed with the "1" output from pin 7.

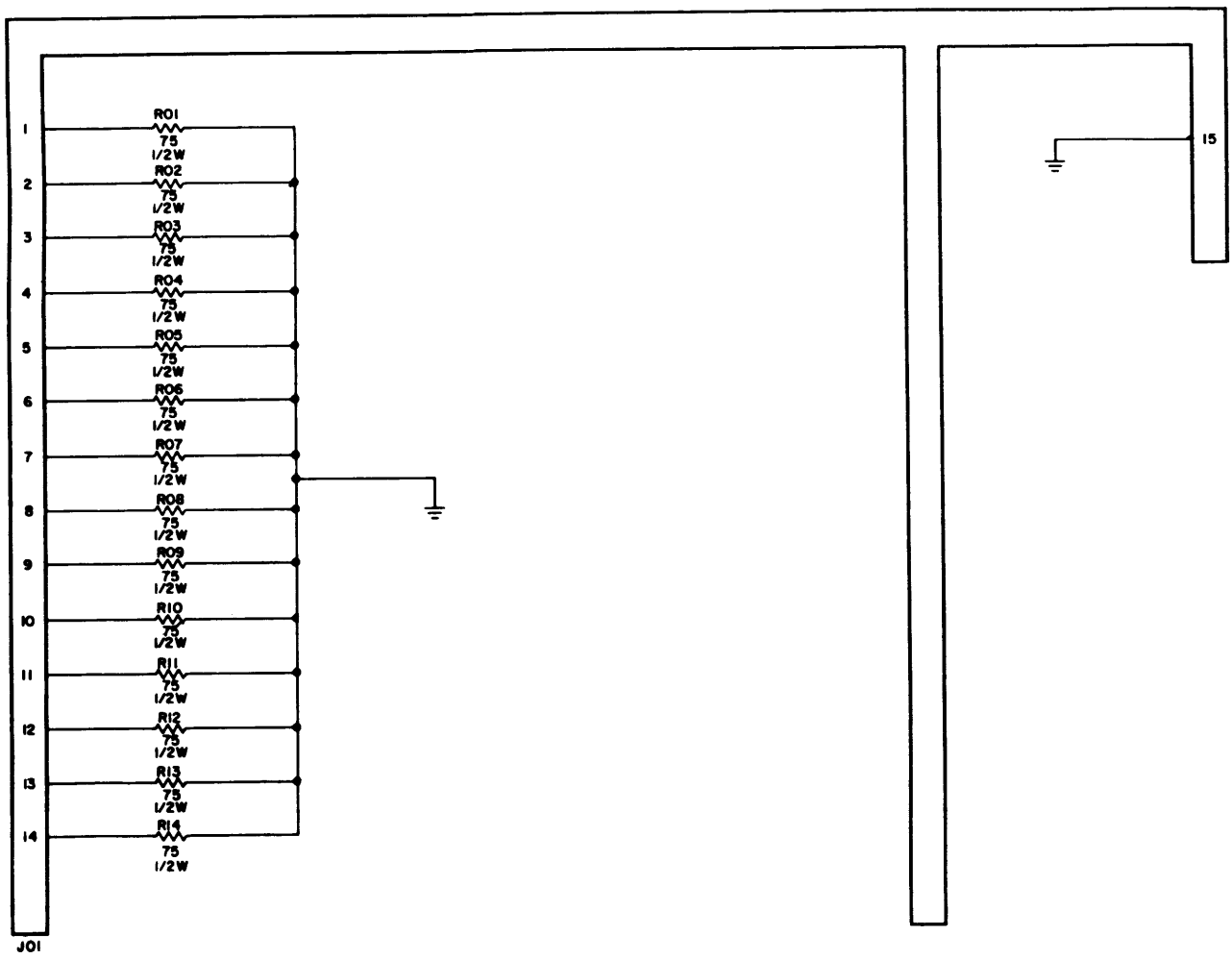

GROUP 1
J01
1
7
2
9
3
10
8
14
GROUP 2
J01
1
8
2
7
3
10
9
14
GROUP 3
J01
1
2
7
3
10
8
9
14
GROUP 4
J01
1
8
2
9
3
7
10
14
GROUP 5
J01
1
3
7
2
9
8
10
14
GROUP 6
J01
1
8
2
3
7
9
10
14
GROUP 7
J01
1
2
3
7
8
9
10
14
GROUP 8
J01
1
8
2
9
3
10

Decoder E05

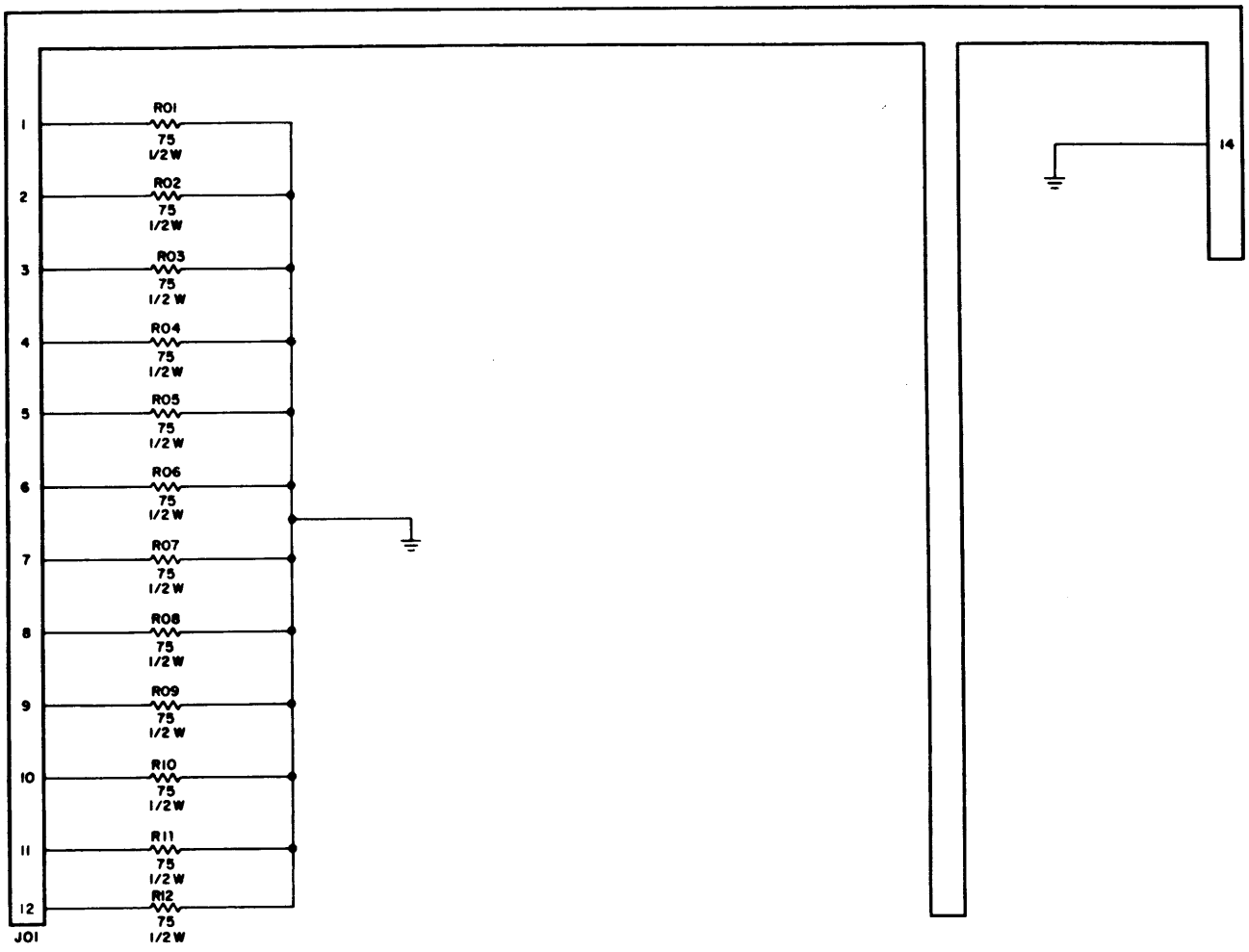
TERMINATOR

Card Types E06 and E07

Card types E06 and E07, which are used for impedance matching on inter-device cables, contain 75-ohm, 1/2-watt resistors. E06 is a 14 resistor assembly; E07 is a 12 resistor assembly.



Terminator E06



Terminator E07

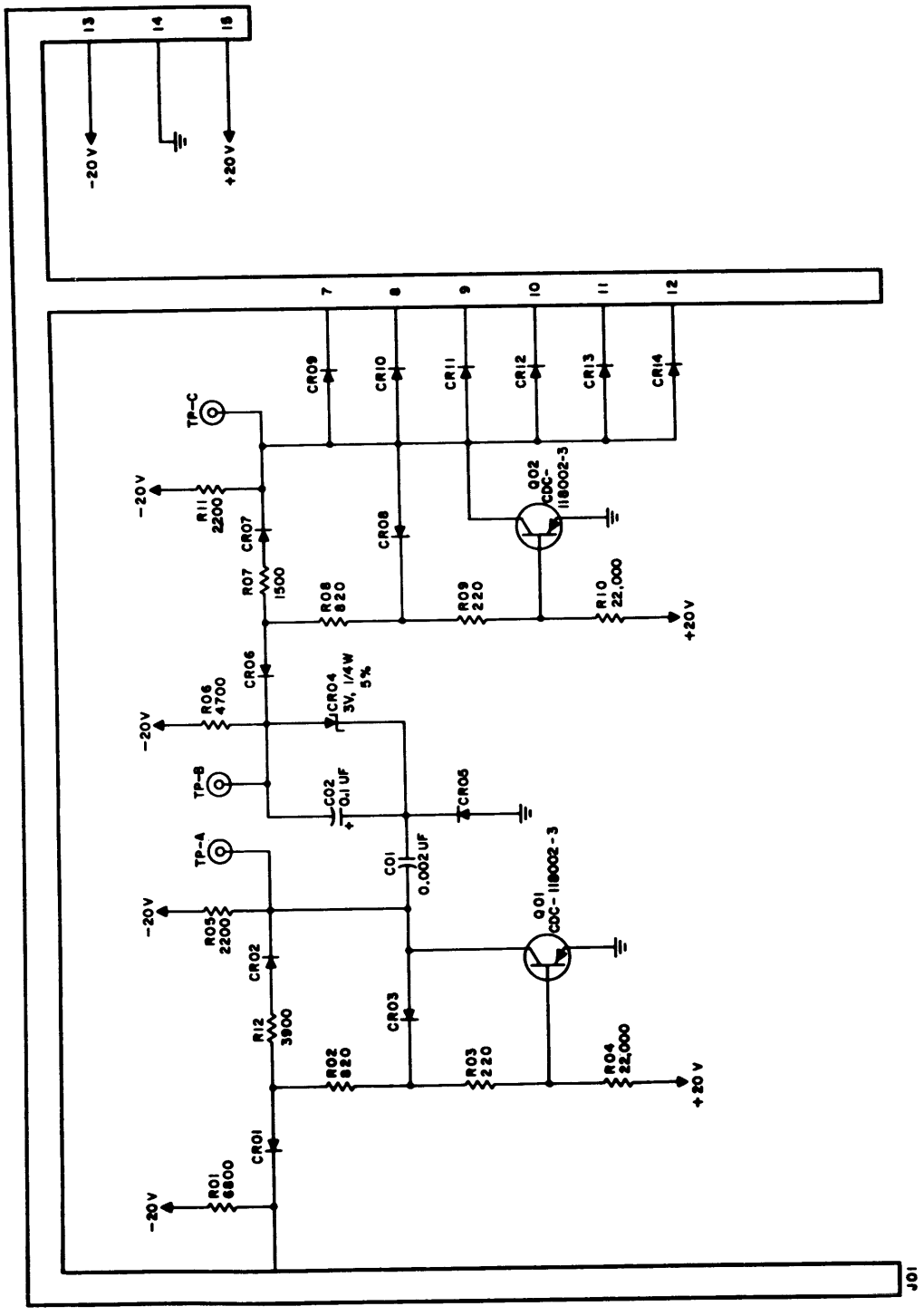
5-E06 & E07-2

Rev. E

SINGLE PULSER
Card Type E08

Card type E08 consists of two common-emitter inverters. The card has one input and six outputs. The main function of the card is to provide 6 outputs for one input of the same voltage level and phase.

An input of -0.5v "0" at pin 1 provides 3.0v across diode CR04. This 3.0v fed through the inverter, consisting of transistor Q03, gives an output of -0.5v "0" at pins 7-12. Similarly, an input of a -3v "1" at pin 1 provides an output of -3.v "1" at pins 7-12. An input of -3v "1" at pin 1 grounds capacitor C01 and provides +1.0v as an input to the second stage of the circuit. This will decay to -3.0v as C01 discharges. Capacitor C01 cannot recharge until the input to pin 1 again returns to 0.5v "0".

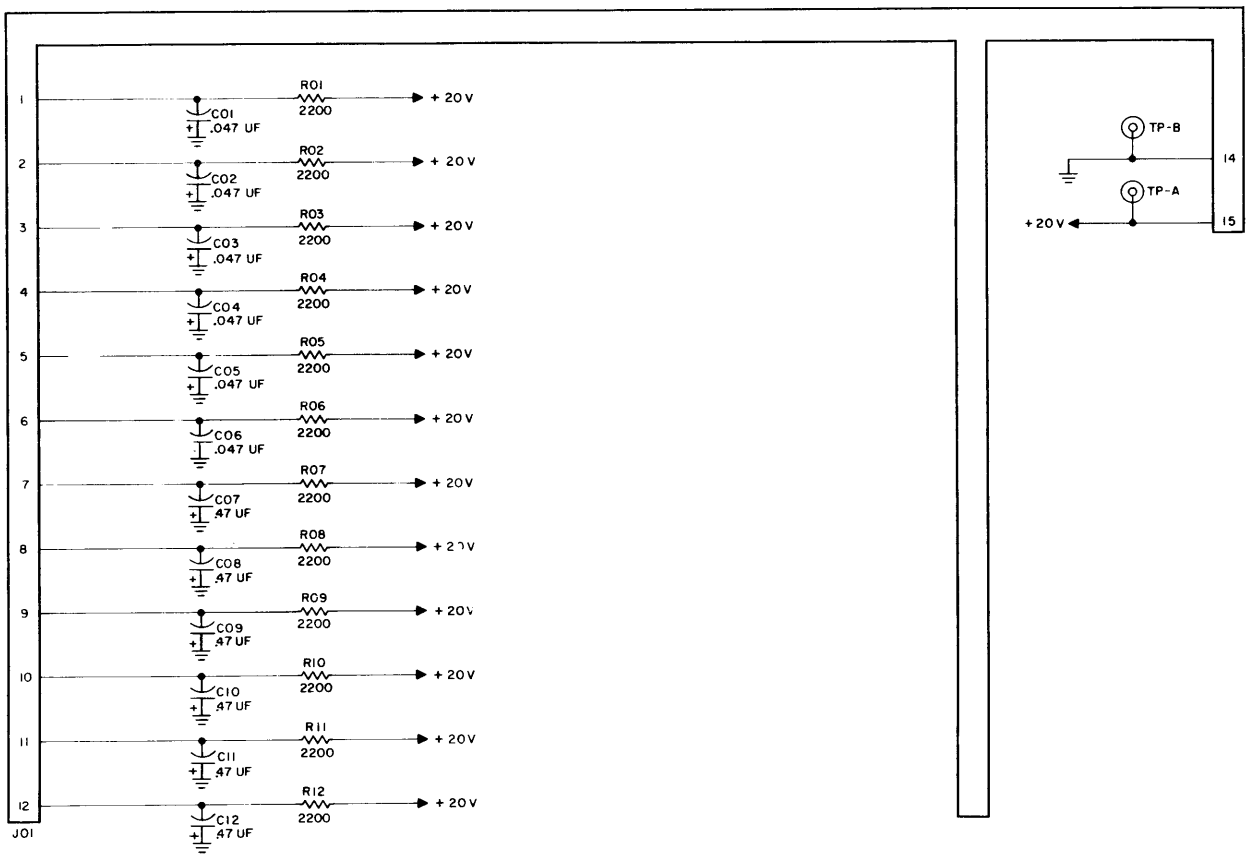


Single Pulser E08

INTEGRATOR

Card Type E10

Card Type E10 is a simple filter to remove unwanted signals or noises from the mechanical devices (e.g., a card reader or card punch). Card E10 can also be used as a delay.

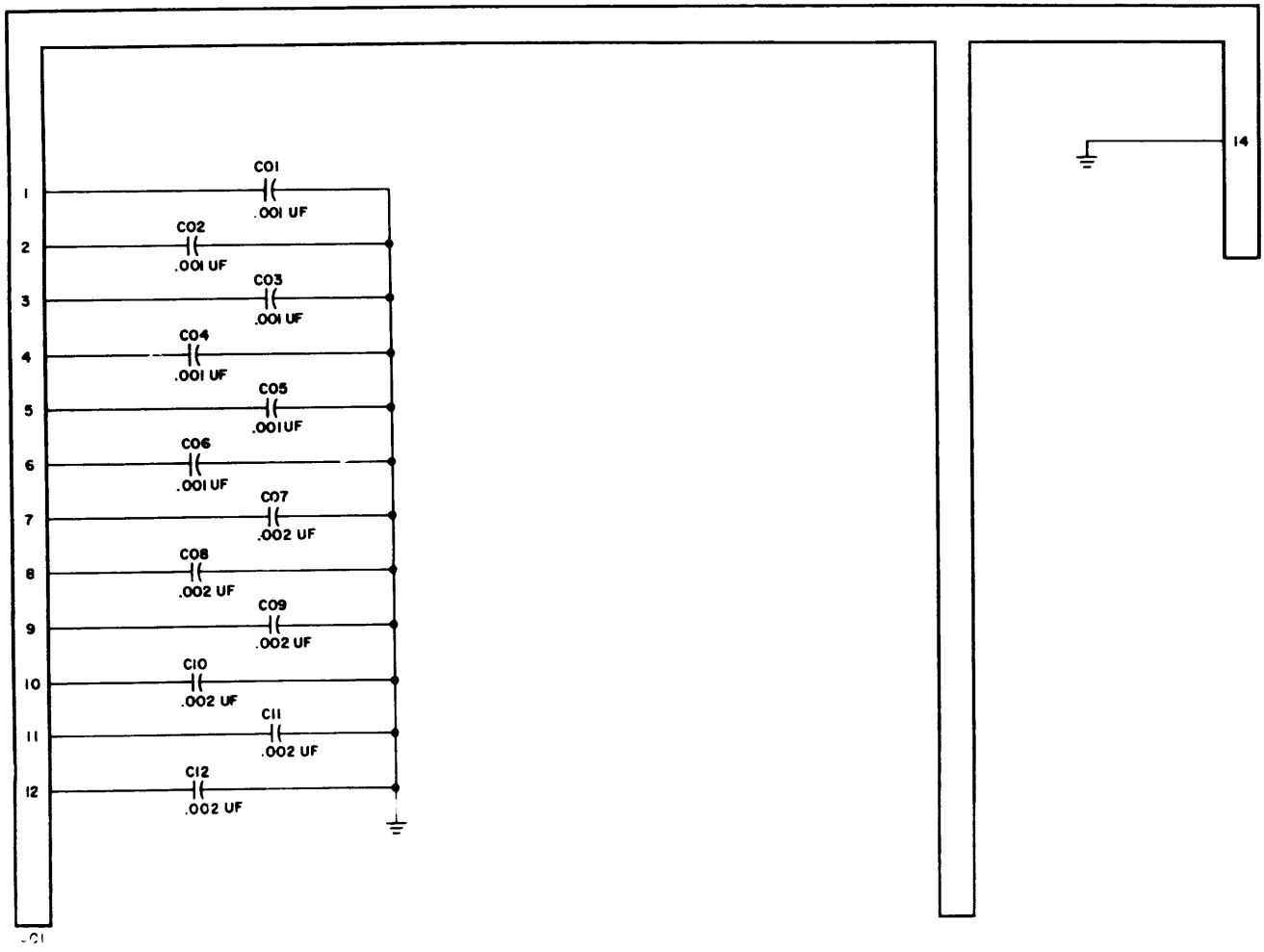


Integrator E10

DELAY

Card Type E11

Card type E11 is a bank of two types of capacitive delays: .001 uf and .002 uf. A .001 uf capacitor causes a delay in 1604-type logic of half a usec, and a .002 uf capacitor causes a delay of 1 usec to the incoming signal. .001 capacitors are connected to pins 1-6; .002 capacitors are connected to pins 7-12. Pin 14 is grounded, and pins 13 and 15 are not used.



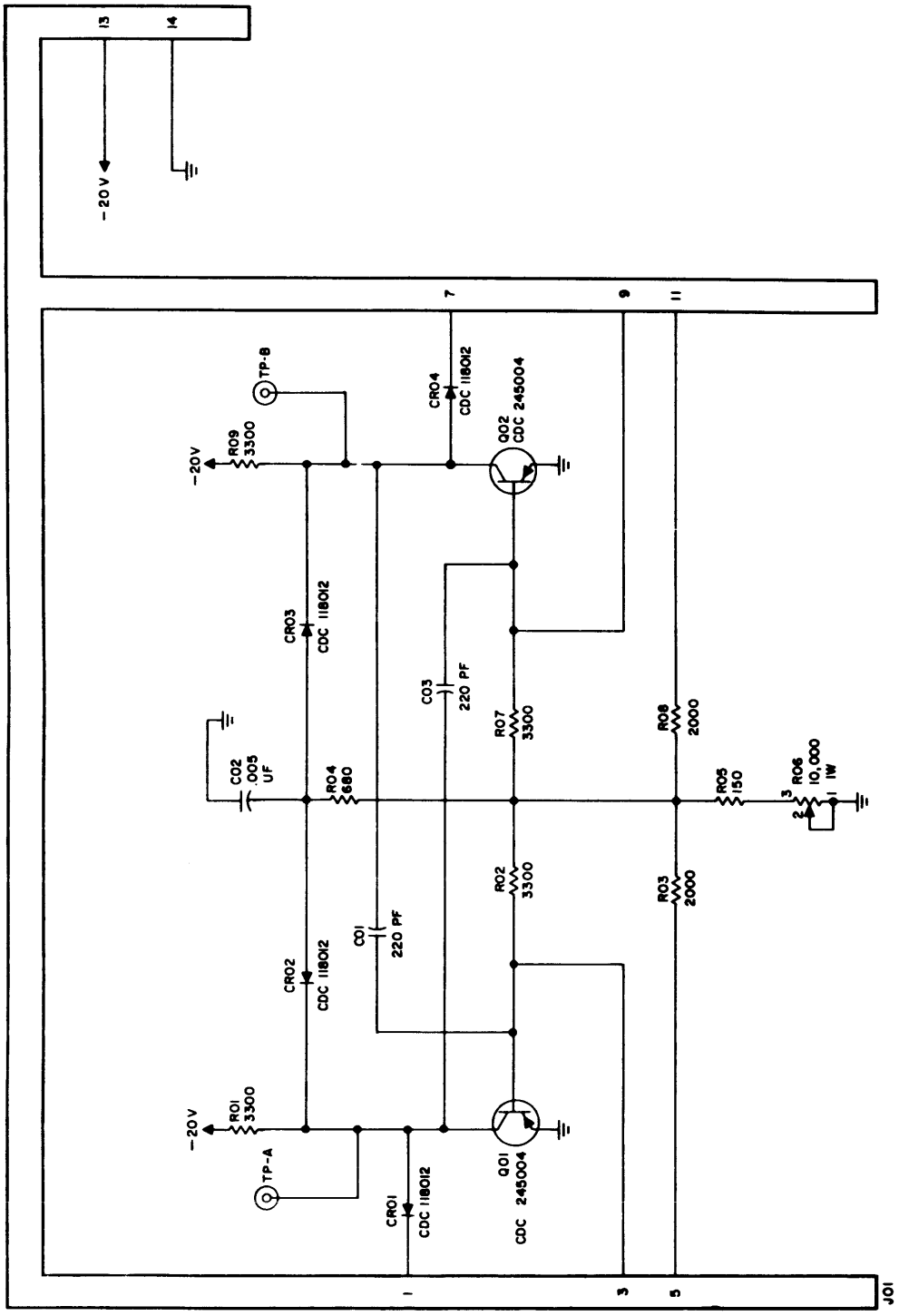
Delay E11

VARIABLE CLOCK
Card Type E14

Card type E14 is a variable clock or a free-running multivibrator with a frequency range of 4kc to 1.5 megacycles. The frequency is changed by varying the time-constant of the circuits, i.e., by jumper pins 3 and 5 or by the variable resistance R06.

The charge on a capacitor and the voltage across its plates cannot change instantly; these factors affect operation. Capacitor C01 connects the base of transistor Q01 with the collector of Q02, and capacitor C03 connects the base of Q02 with the collector of Q01. When supply voltage (-20v) is initially applied, currents flow in the various circuit branches and the capacitor builds up charge. Because the two halves of the circuit are alike, currents are alike at first, but even the slightest imbalance results in a cumulative difference in the two collector currents, saturating one of the transistors and cutting off the other. Outputs are obtained from pins 1 and 7. Diodes CR02 and CR03 switch the two transistors from one state to the other.

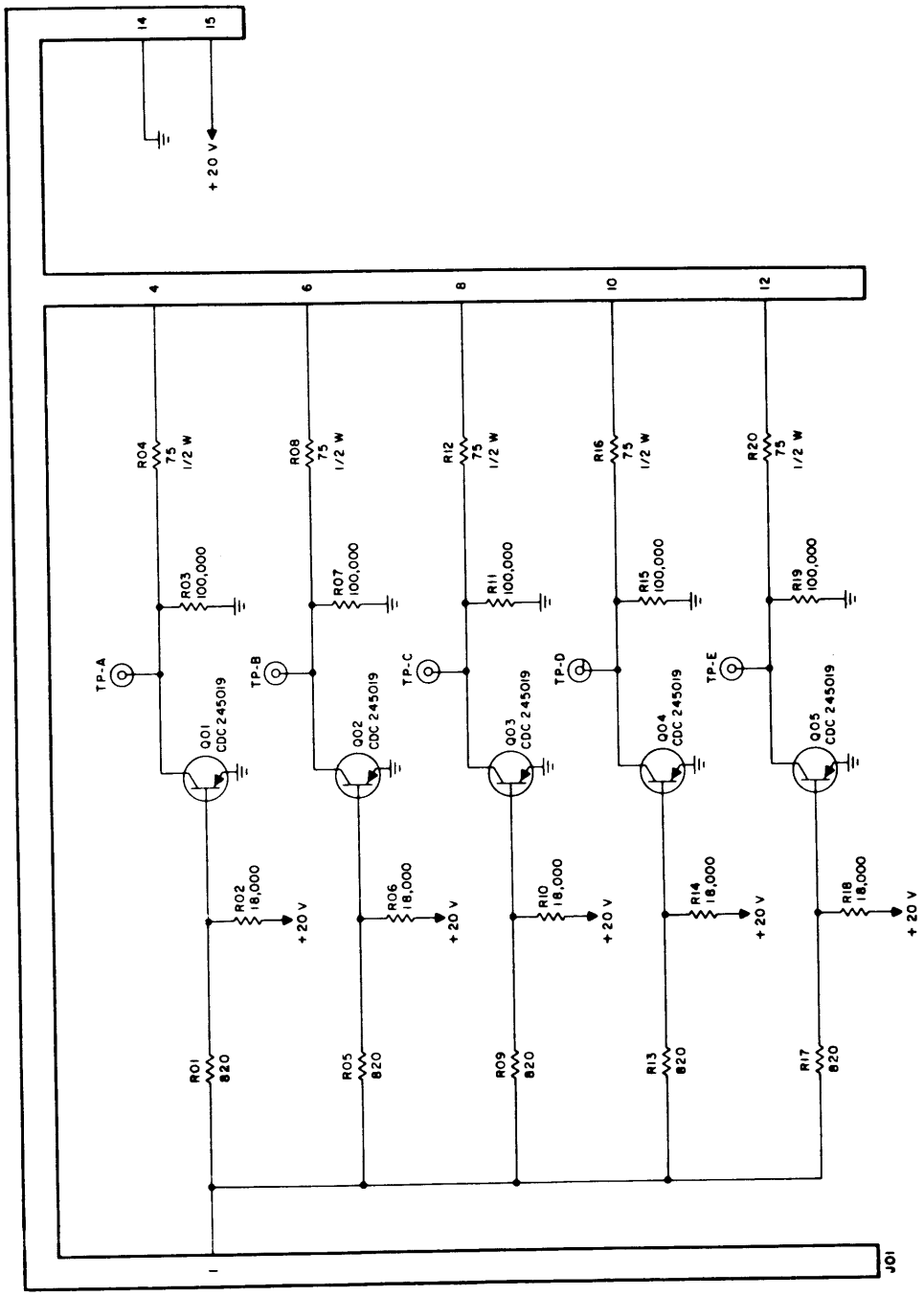
Once the circuit is triggered, it continues to provide an output at the desired frequency, as long as the supply voltage is maintained.



Variable Clock E14

TERMINATOR
Card Type E19

Card type E19 contains five terminator circuits that are switched by transistors. When the transistors are conducting, the circuits serve as impedance matchers; when the transistors are not conducting, the circuits serve as bleeders. E19 has a single input at pin one and outputs at pins 4, 6, 8, 10 and 12. When the voltage level at pin 1 is at or near -6v potential, the transistors conduct, providing 75 ohms resistance from the output pins to ground. An input of 0 volts at pin 1 cuts off the transistors, providing 100K ohms resistance from the output pins to ground.

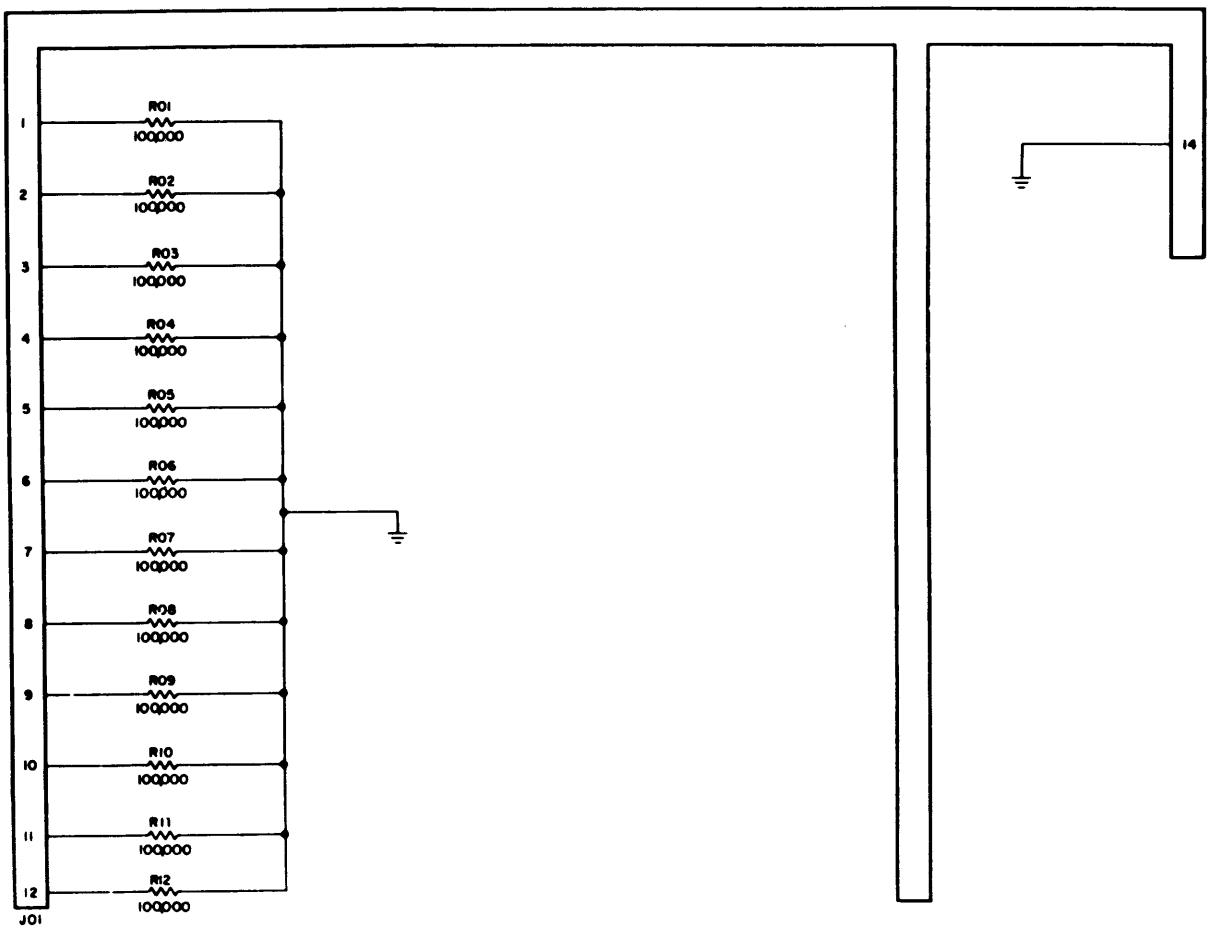


Terminator E19

RESISTOR ASSEMBLY

Card Type E20

Card type E20 contains twelve 100K, 1/2 watt resistors. It is designed to be used in a bleeder network.



Resistor Assembly E20

CONSOLE INTERFACE

Card Type HA10A

FUNCTION

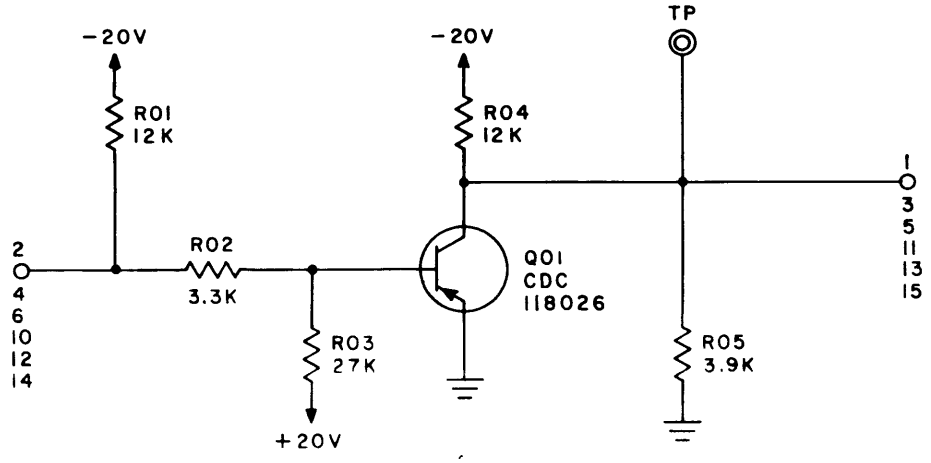
This circuit converts the signals received from either logical inverters or manual switches into outputs suitable for driving a high-current load such as a 5v light. This circuit can also function as a logical inverter since its output voltages are approximately those required for "1's" and "0's".

OPERATION

Transistor Q01 is capable of handling a current of the order of 200 ma. A -5.8 v "1" (or open) input causes Q01 to conduct, while a -1.1 v "0" (or ground) input causes Q01 to cut off.

A -1.1 v "0" or ground input allows the +20 v through resistor R03 to reverse-bias the emitter-base junction of Q01, so that Q01 is cut off. In this state, the test point voltage will be approximately -5.6 v. This is produced by the voltage divider action of R04 and R05.

A -5.8 v "1" or an open input will cause Q01 to switch on and conduct heavily. A negative-going input causes current flow to increase through R02. Initially this current is supplied by the +20 v source through R03, however the voltage drop across R03 is limited by the base-emitter junction drop of Q01. A further increase in current flow will draw turn-on current through Q01, causing it to switch to its conduction state.



NOTE: SIX CIRCUITS PER CARD.

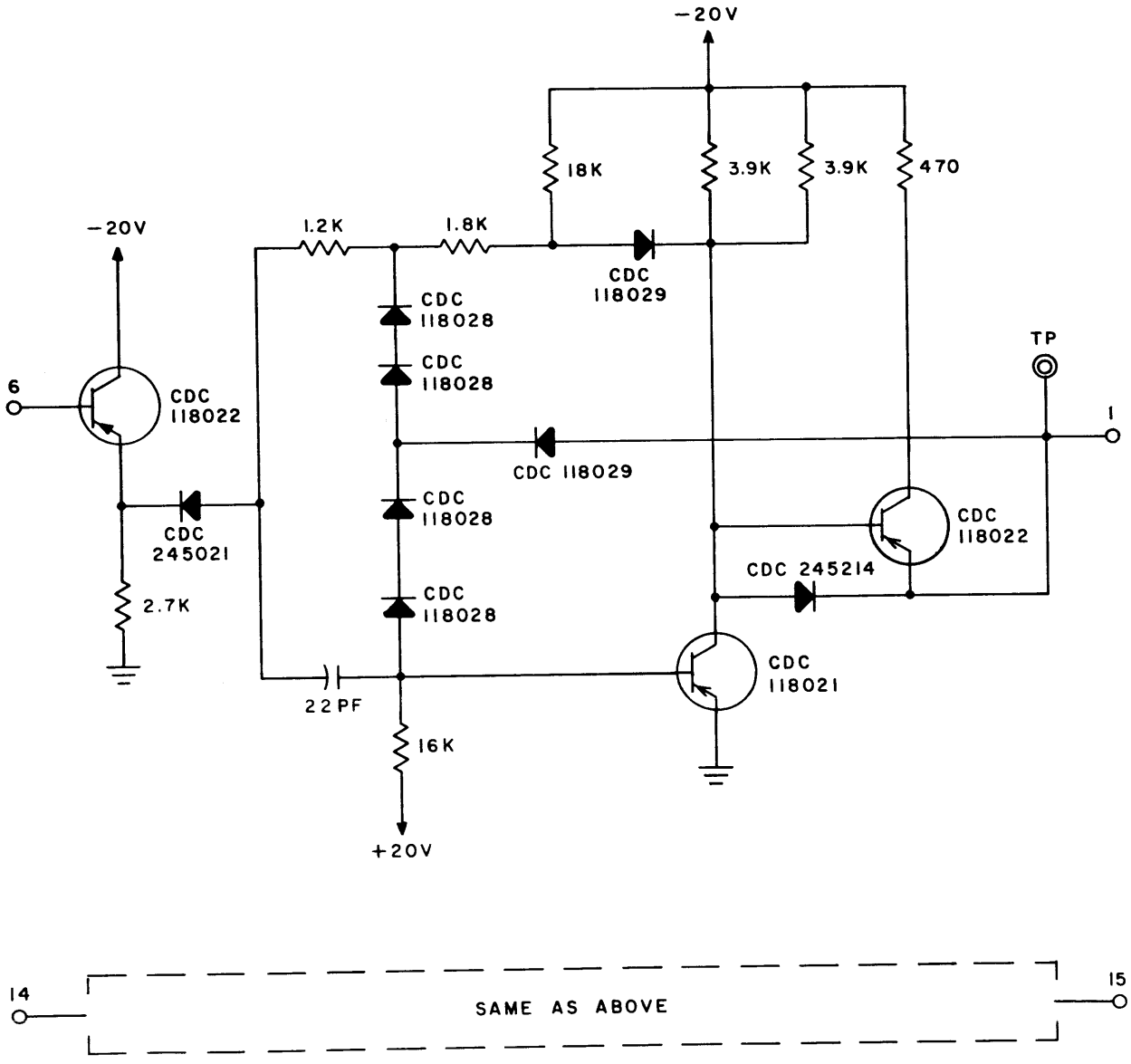
DELAY LINE AMPLIFIER
Card Type HA12

FUNCTION
The function of this circuit is to convert inputs received from a terminated, 200-ohm delay line into logic outputs. The circuit provides a high-impedance load for the delay line, avoiding excessive current drain. The circuit output is a -1.1 v "0" which goes to -5.8 v "1" upon receipt of a positive-going pulse from the delay line. It is capable of driving eight loads, and its output characteristics are identical to a logical inverter.

OPERATION
The circuit consists of an emitter follower feeding an inverter through an OR diode. Inputs are received by tapping from the delay line. The quiescent value of the input signal is about -10 v, with pulses going to ground.

The input transistor is an emitter follower current amplifier, which provides a high impedance load with little current drain for the delay line. It is coupled directly into the inverter by means of an OR diode. With a -10 v input, the emitter of the input transistor is held at approximately -9.3 v. This holds the output of the inverter at -1.1 v "0". A positive-going input is effectively the same as a logical "0" and will cause the inverter to have a -5.8 v "1" output.

The inverter portion of the circuit is similar to a logical inverter, which is discussed elsewhere.

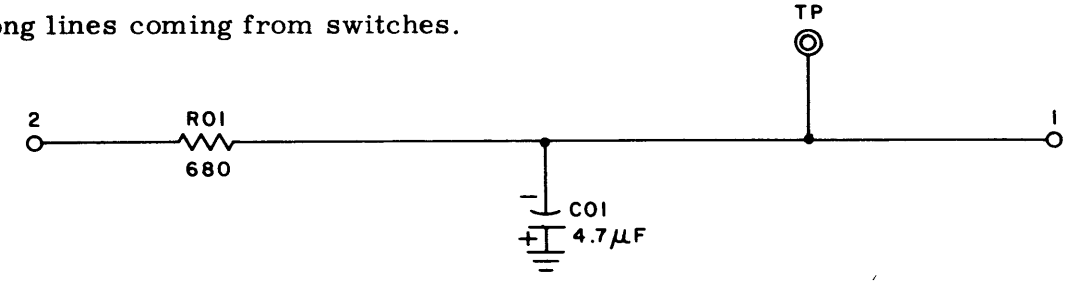


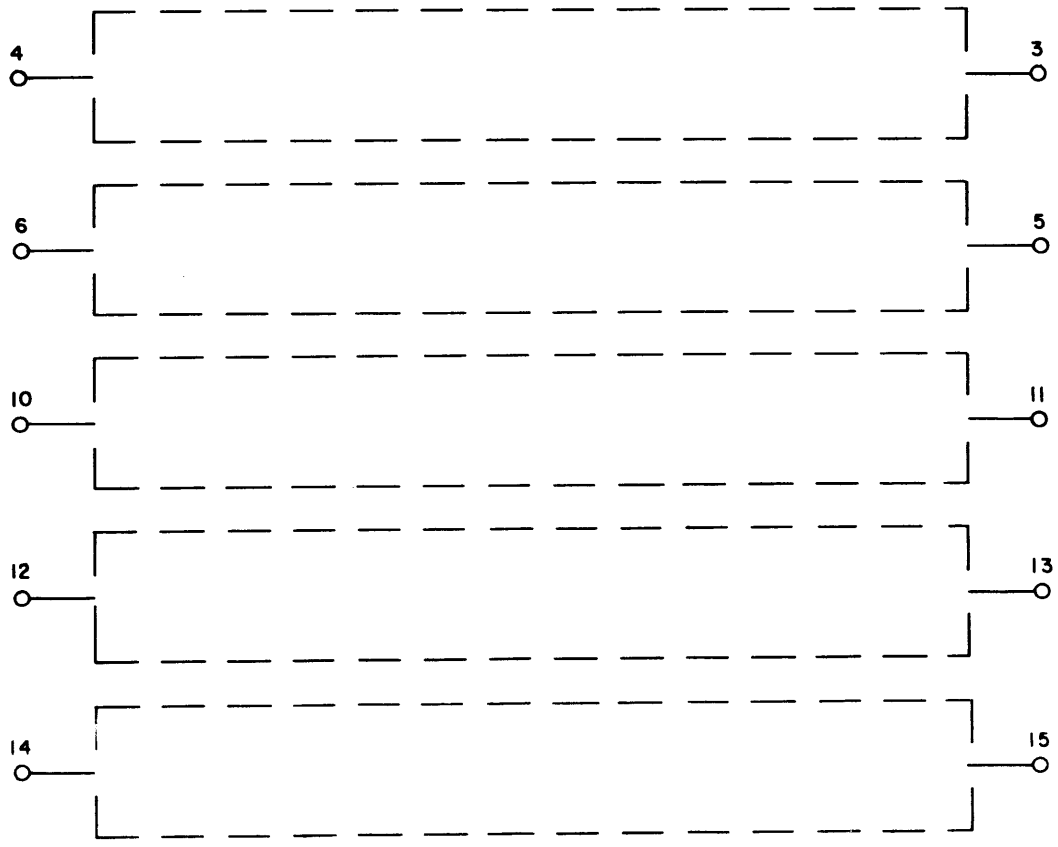
Delay Line Amplifier HA12

FILTER

Card Type HA17

This card contains six identical RC filters, each consisting of a series resistor followed by a capacitor to ground, as shown on the accompanying diagram. It is designed to be used in conjunction with card type HA10 on long lines coming from switches.





NOTE: ALL CIRCUITS IDENTICAL

LIGHT DRIVER

Card Type HA20

FUNCTION

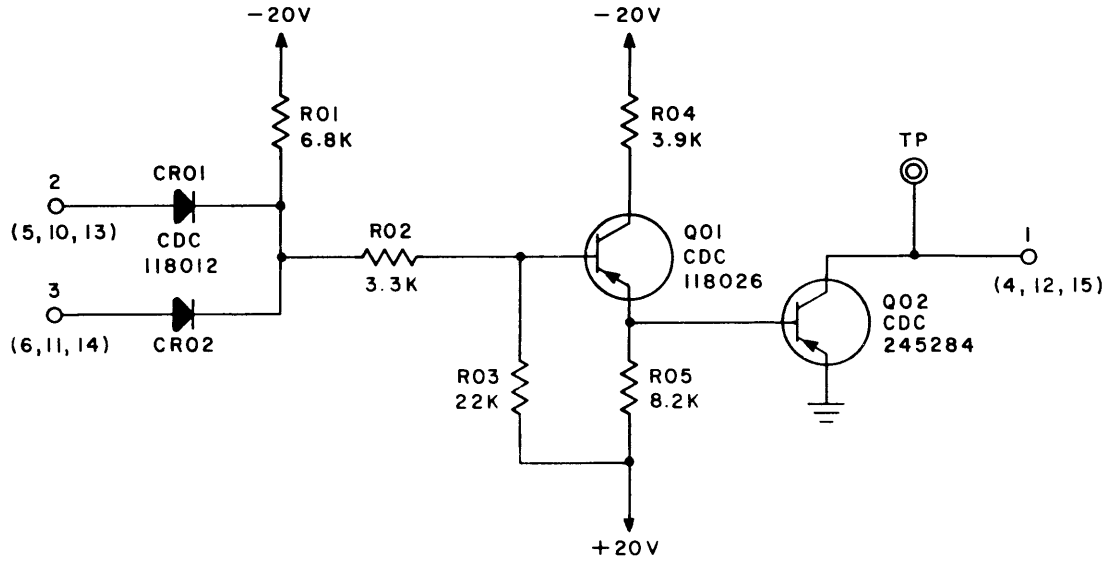
This card contains four identical circuits, the function of which is to provide a low impedance path from ground to the circuit output upon receipt of a -5.8v "1" input. The output transistor can handle a collector current of 500 ma at -18v, and is therefore well suited for driving an indicator light.

OPERATION

Transistor Q01 operates as an emitter follower and Q02 as a grounded emitter amplifier. The input to Q02 therefore follows the input to Q01 and is increased by the gain of Q01.

Each circuit has a 2-way AND input. Open inputs have the same effect as -5.8v "1's". If both inputs are open, the -20v through R01 will switch the transistors to the conduction state.

The base of Q02 is held approximately 0.5v more positive than the base of Q01 by the base-emitter junction drop of Q01. If the circuit inputs are -5.8v "1", the input to Q01 will be approximately -3.4v. This puts a strong forward bias on the base of Q02, enabling it to conduct. A -1.1v "0" circuit input holds the base of Q01 at about +2.7v. This applies a reverse bias of around +3v to Q02 so that it is cut off.



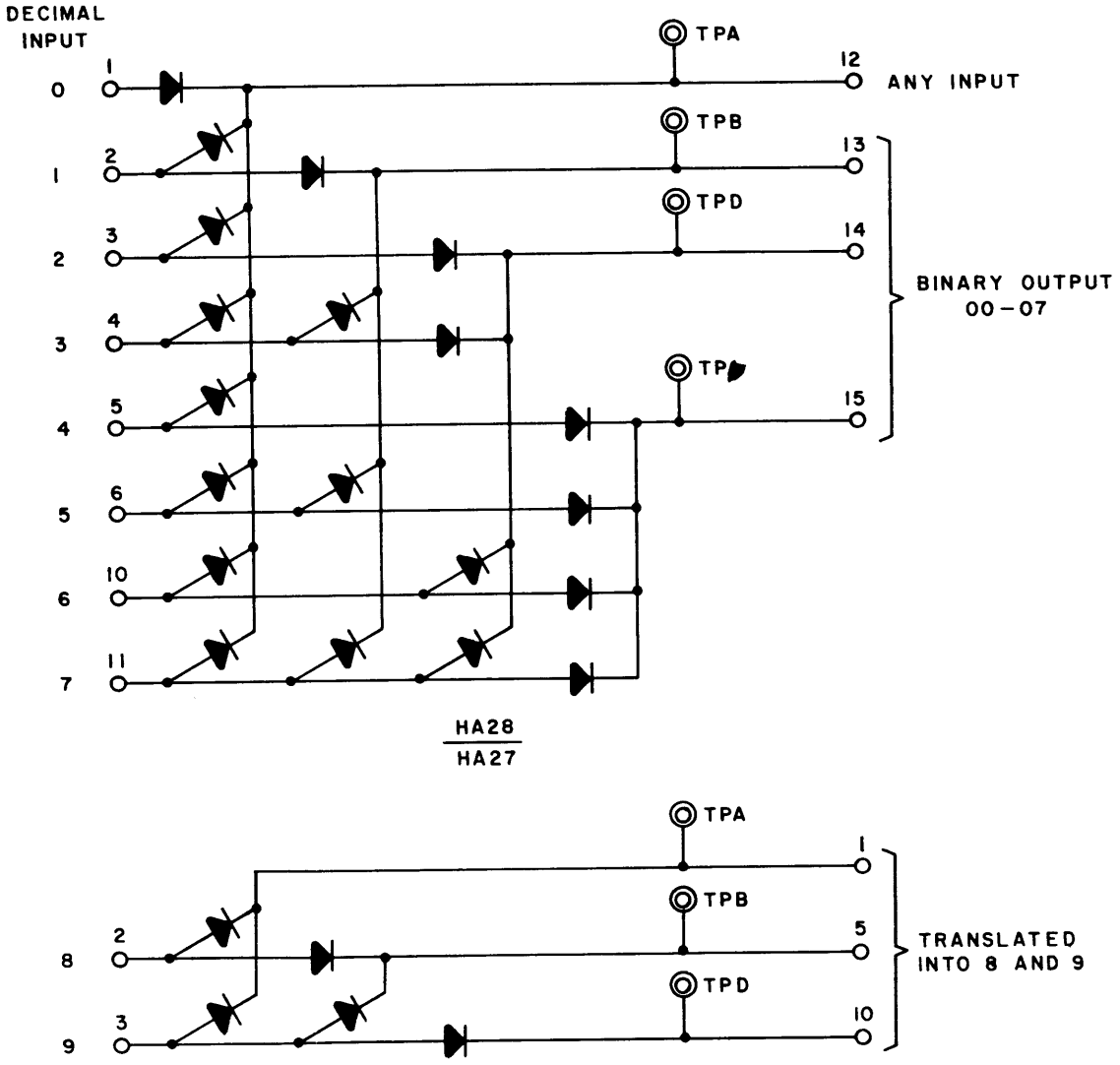
NOTE: 4 CIRCUITS PER CARD

KEYBOARD TRANSLATOR
Card Types HA27 and HA28

The function of these cards is to perform a decimal to binary conversion. Card type HA28 converts the numbers 0 through 7 and HA27 converts 8 and 9.

The circuits consist of AND diodes, and when one of the input pins is grounded, the output pins at which the ground appears will represent a binary number. The input pins are connected to a set of decimal push-buttons on a keyboard. As the buttons are pressed, the diode translator network converts the number to binary.

Note that pin 12 on card type HA28 will be at ground if any input pin is grounded. Similarly, pins 1 and 5 on card type HA27 will indicate a ground at either input.



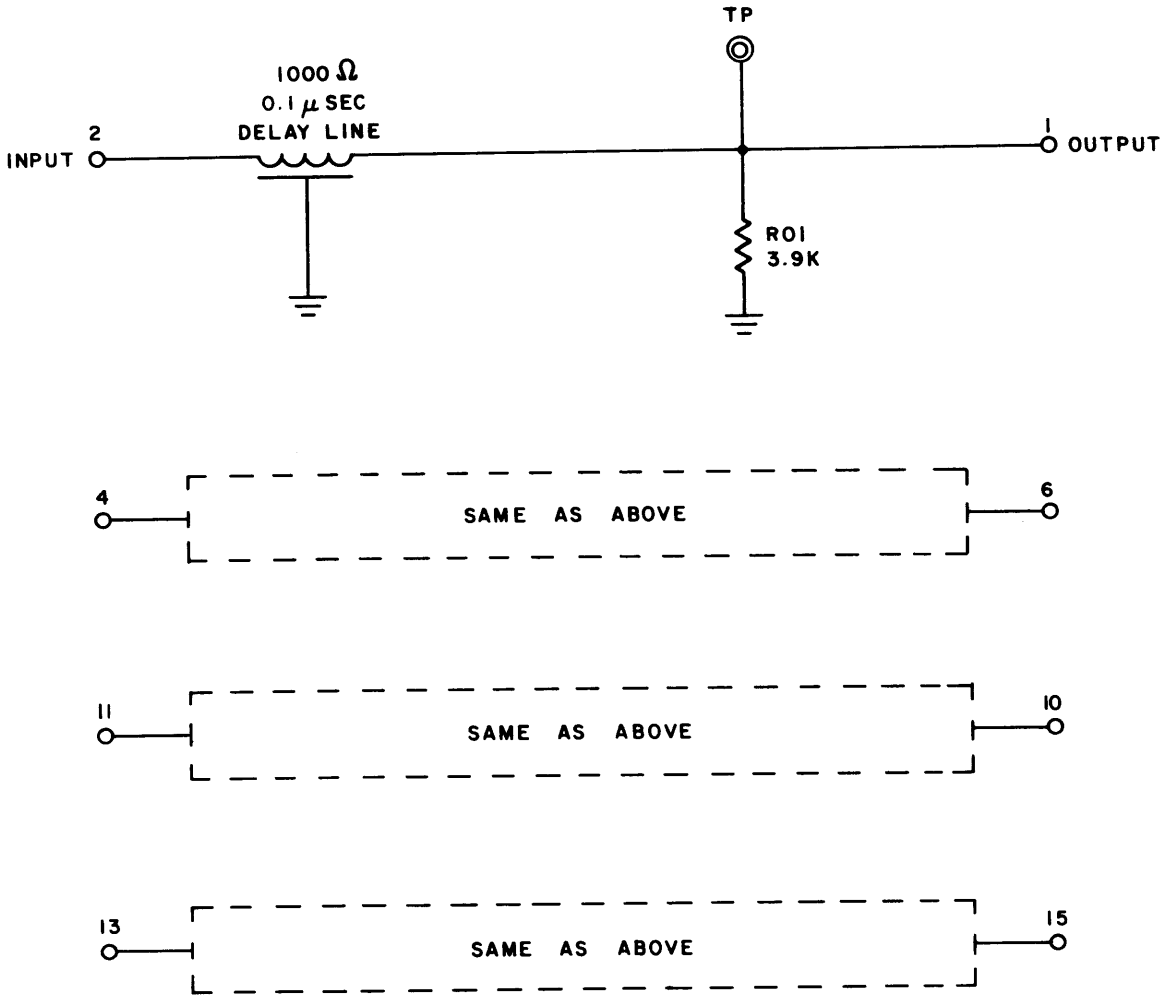
Keyboard Translator HA27 & HA28

DELAY LINE, 0.1 USEC
Card Type HA35

The function of this circuit is to provide an interval of time delay between successive logical operations. It is designed for use in applications requiring greater stability than may be obtained from capacitive delays.

The nominal 0.1 usec delay time applies to both "1's" and "0's", and the delay may be used to drive either an AND or an OR input. Attenuation through the delay line is negligible.

The characteristic impedance of the delay line is 1000 ohms. The purpose of resistor R01 is to provide better impedance matching between the logic circuit input and the delay line output.



NOTE:

1. EACH DELAY MAY DRIVE ONE LOGIC CIRCUIT USING EITHER AN "AND" OR AN "OR" INPUT.

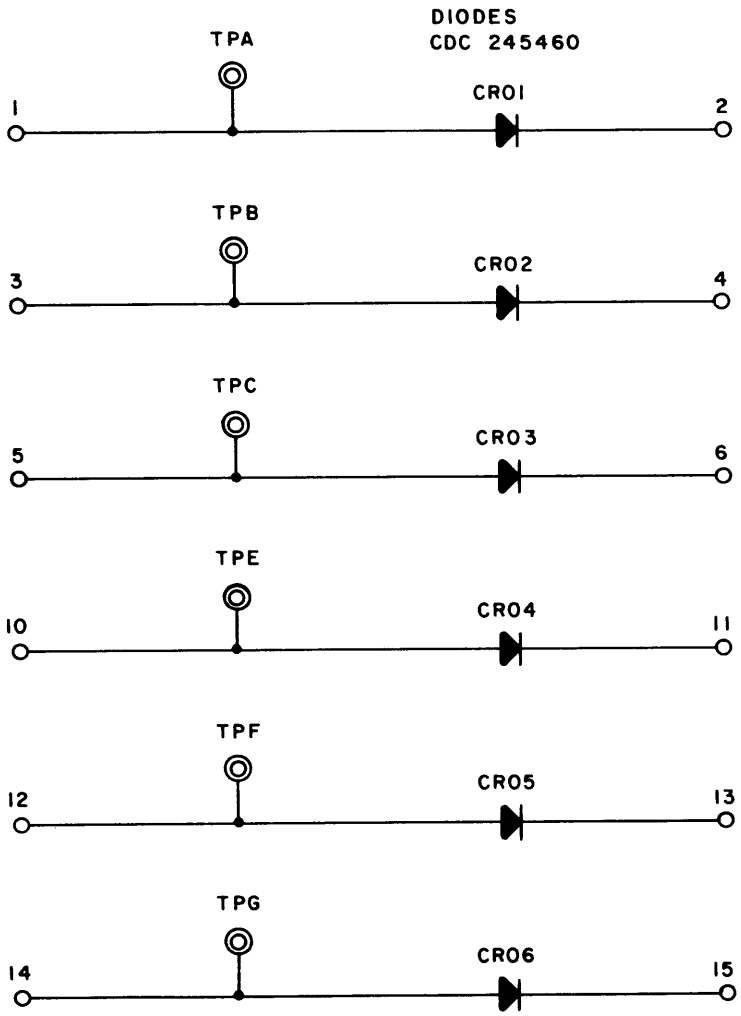
Delay Line, 0.1 usec HA35

DIODE

Card Type HA38

This card contains six diodes, as shown in the accompanying diagram. These diodes are high-current silicon devices, and a summary of their characteristics is as follows:

A. Average rectified forward current, 25°C; 750 ma.
B. Peak forward current; 6 amperes.
C. Peak reverse voltage; 600 volts.

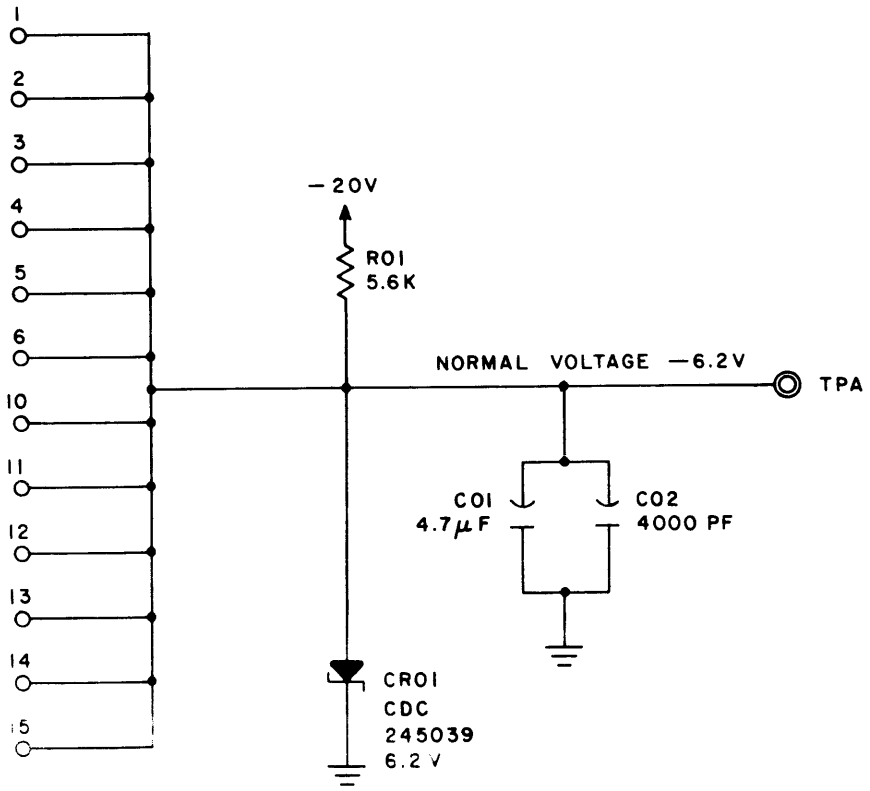


NOTE: DIODES RATED 750 MA.

LINE TERMINATOR
Card Type HA39

This circuit provides a clamp for logic lines, so that ringing is minimized. Any negative-going overshoot will be clamped at approximately -6.2 v. As shown in the accompanying diagram, the clamp voltage is the drop across the 6.2 v zener diode CR01.

Filtering is provided by capacitors C01 and C02. Due to its large area, C01 presents an appreciable amount of inductive reactance. It is therefore necessary to include the small capacitor C02 to filter out high-frequency spikes.



DELAY
(Inductive, 0.15 usec)
Card Type P13A

FUNCTION

The function of this circuit is to provide an interval of time delay between successive inversions in 1604-type logic. It is designed for use in application requiring greater stability than may be obtained with capacitive delays.

The normal 0.15 usec delay time applies to both "1's" and "0's". The delay will drive one load, which may be either an AND or an OR.

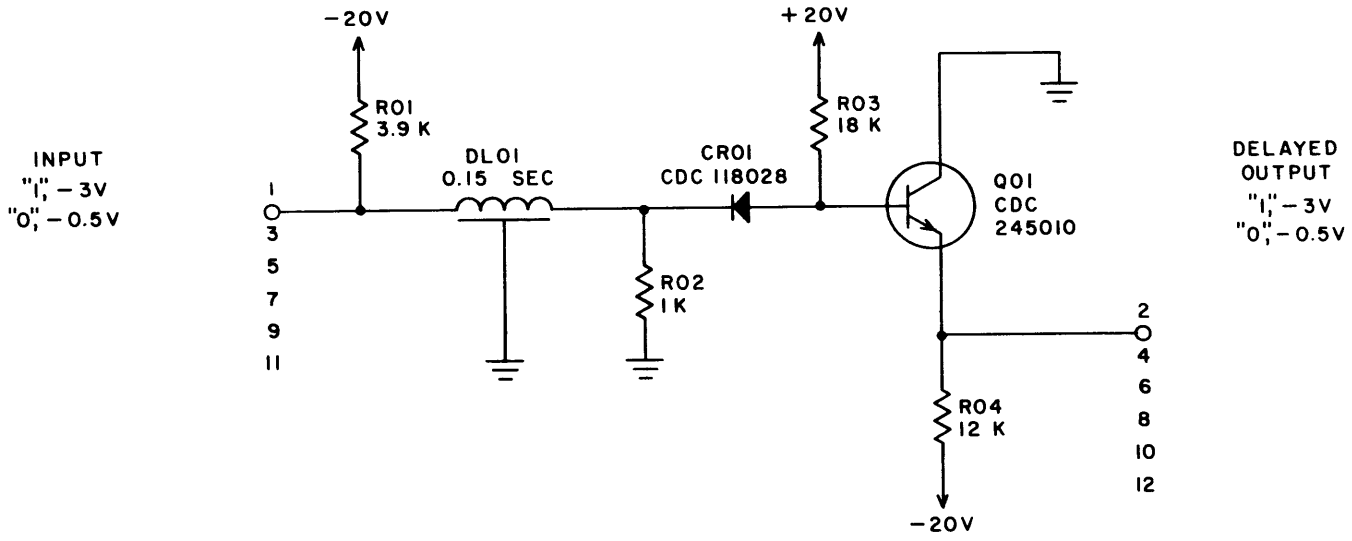
OPERATION

The delaying action is performed by the 0.15 usec inductive delay line DL01. The characteristic impedance of DL01 is about 1000 ohms. Resistor R02 provides impedance matching for the delay line output. Transistor Q01 operates as an emitter-follower current amplifier.

Resistors R02, R03, and diode CR01 perform a level-shifting function between the delay line and the base of Q01. CR01 is a silicon forward-drop diode having a differential of 0.7v between anode and cathode.

A -0.5v "0" input results in about +0.2v at the base of Q01. The output voltage is equal to the base voltage of Q01, less the base-emitter junction drop and is approximately -0.5v.

A -3v "1" input holds the base of Q01 at about -2.3v. However, the base-emitter junction drop of Q01 is approximately equal and opposite to the drop across CR01, so that the circuit output is about -3v.



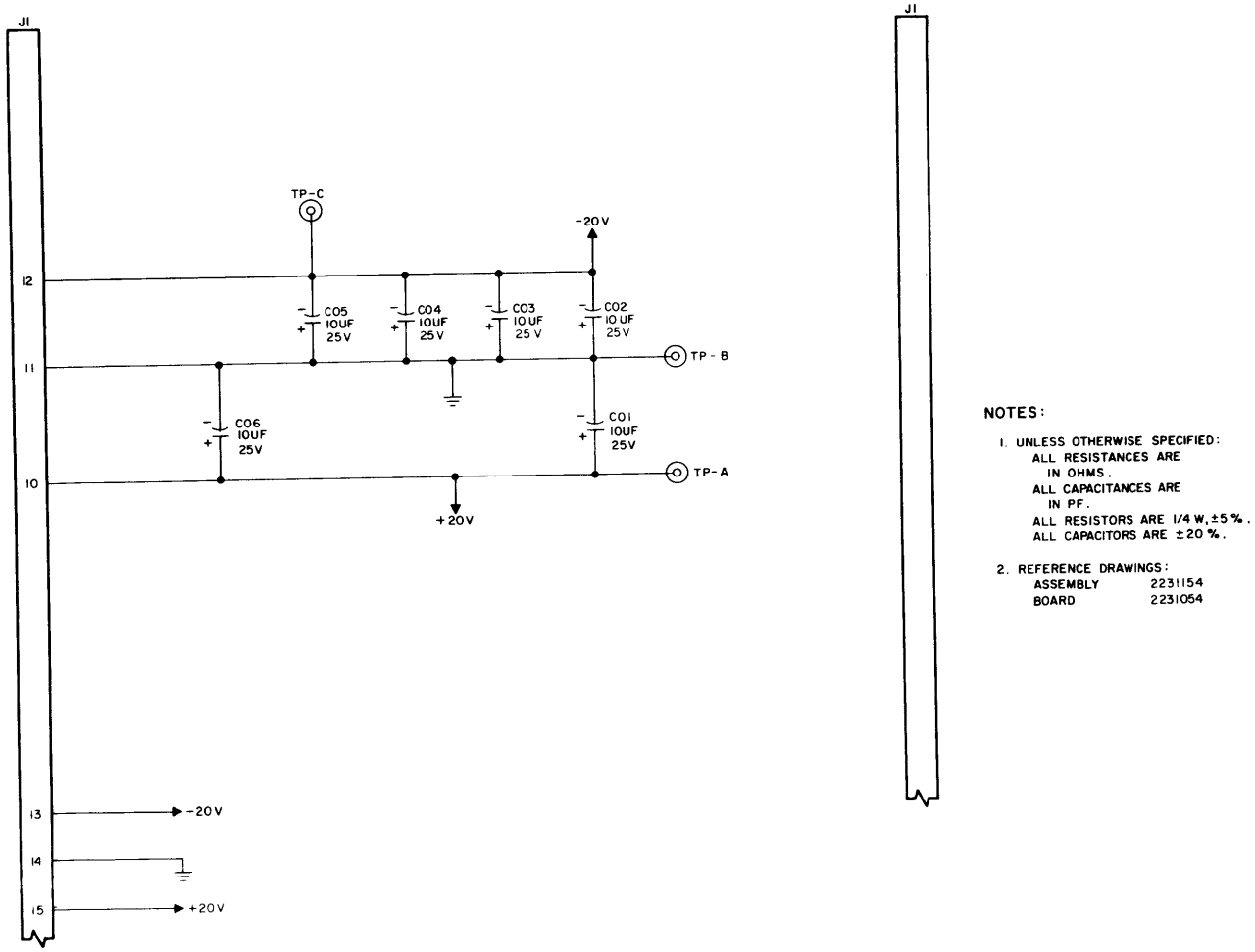
NOTES:

1. 6 CIRCUITS PER CARD.
2. APPROXIMATELY EQUAL DELAY FOR "1" AND "0".

POWER SUPPLY FILTER AND JUMPER
Card Type P54

Card P54 provides multiple connections to -20v, ground, and +20v. Pins 13, 14, and 15 are connected in the usual sequence to -20v, ground, and +20v. So that other connections can be taken from this card, pin 12 is held at -20v, pin 11 is held at ground, and pin 10 is held at +20v.

P54 also contains six filter capacitors rated uf at 25v. Four are connected between -20v and ground and two are connected between +20v and ground, to diminish any ripple in the supply voltage.

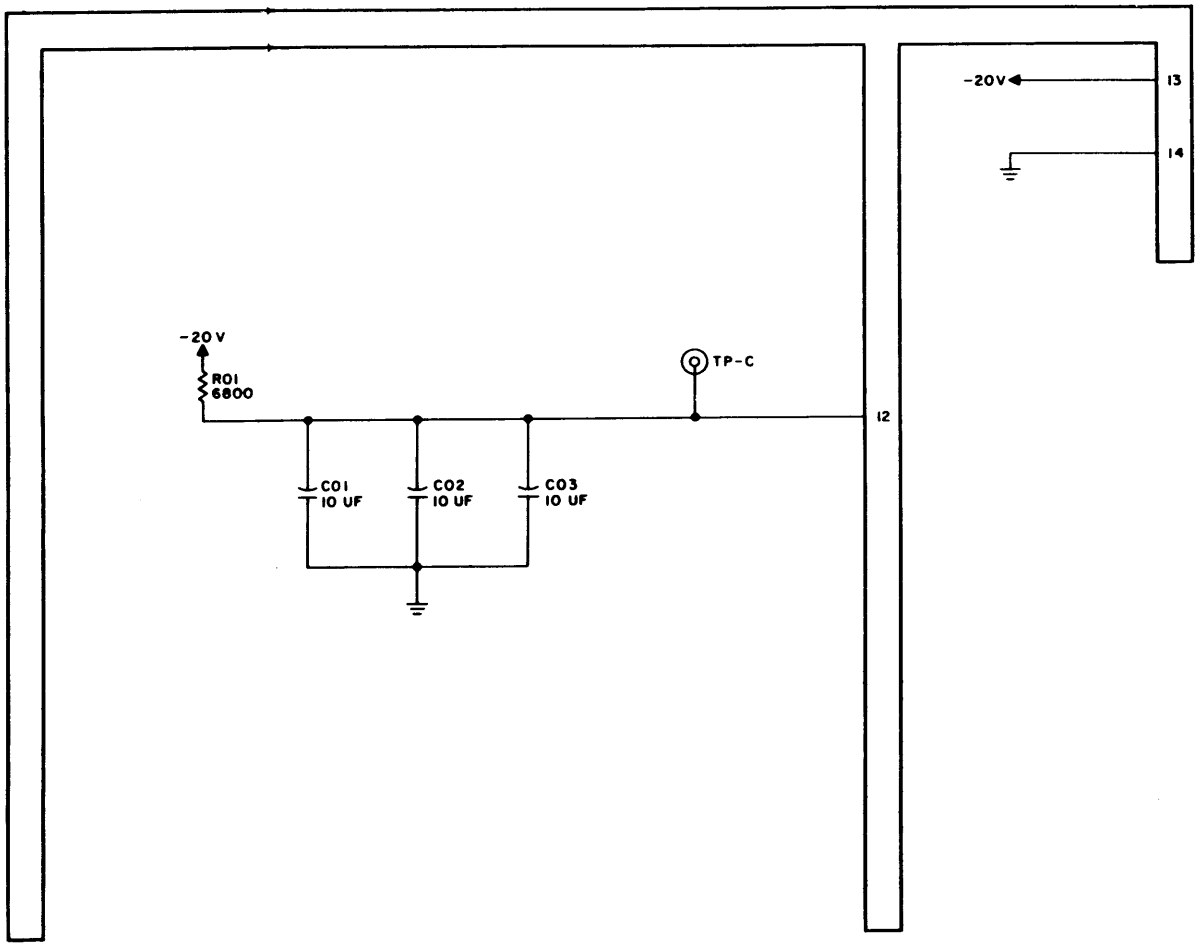


Power Supply Filter and Jumper P54

POWER SUPPLY FILTER & JUMPER

Card Type P55

This card contains a total of 30 uf of capacitance to ground, with a source of charging current through a 6800-ohm resistor to -20v, as shown on the accompanying diagram. The circuit may be used in various ways, such is to produce a power-on Master Clear pulse by connecting pin 12 to the input of an M^{---} card. When power is first applied, the uncharged capacitors on the P55 card will cause the M^{---} card to have a "1" output which may be used to drive the Master Clear inputs. When the capacitors obtain sufficient negative charge, the output of the M^{---} card will go to "0".



Power Supply Filter & Jumper P55

HAMMER DRIVER
Card Types P91 and P92

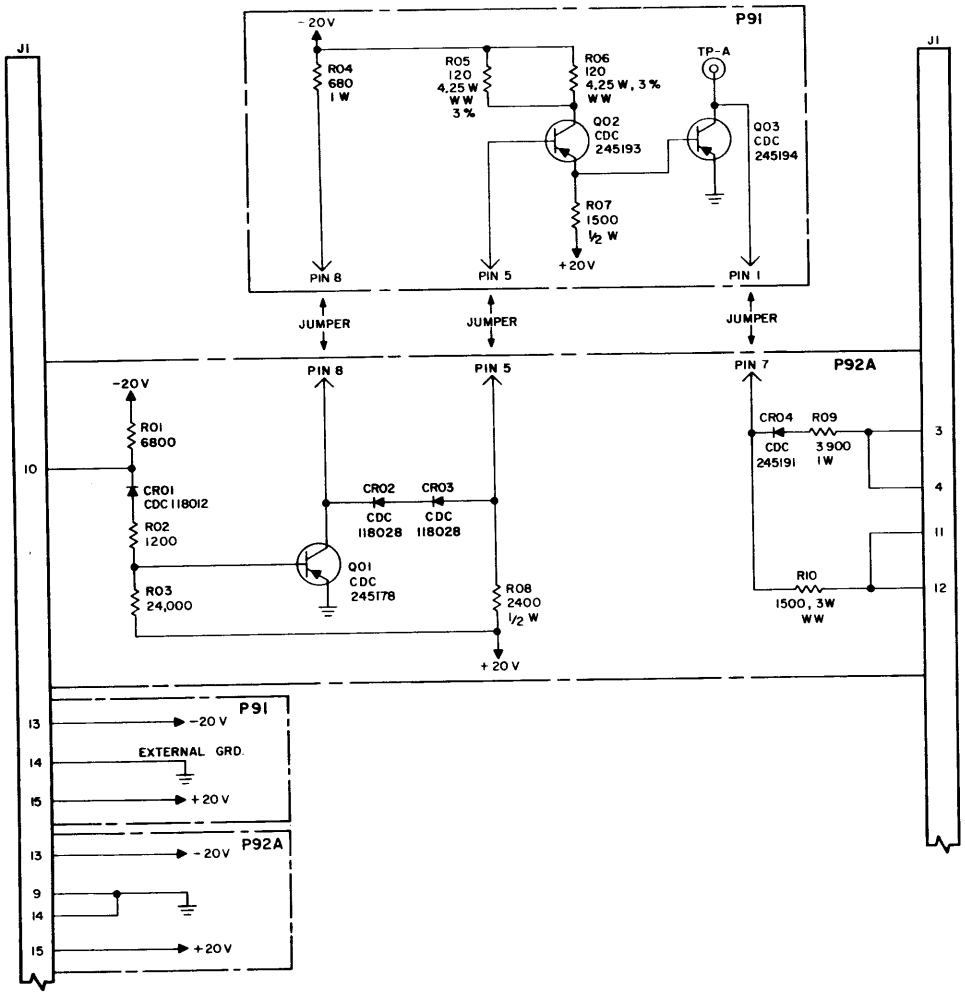
(Normal Test Point Voltages: -36v, or ground)
Card types P91 - P92 share circuitry. The 30-pin connector into which they are inserted is wired so the complete circuit is as shown.

The circuit is designed to switch a current of 7 amp from a -36v source. It is used as a hammer driver in which it provides 1.3 ms pulses to the hammer solenoids, and in the paper feed circuit, where it provides 4 ms starting pulses to the clutch and brake coils.

The circuit receives logic inputs from One-Shot card P95 or P97. These cards provide logical "0" input pulses of 4 ms and 1.3 ms.

Upon receipt of a "0" input (-0.5v), the base of Q01 is at a positive potential and it is cut off. The base of Q02 is biased somewhat negative and conducts. Transistor Q03 also conducts being connected to Q02 as an emitter follower, and the circuit is completed from pins 11 and 12 to ground. Upon receipt of a logical "1" (-3v) this circuit is cut off.

Provision is made to handle the high-voltage transient induced in the inductive coil when Q03 is cut off, by use of the diode CR04 and the connection at pins 3 and 4. A series circuit is provided through the diode with the coil as a source of EMF, so that the transient is dissipated harmlessly.



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.

2. REFERENCE DRAWINGS:
   ASSEMBLY 2231191, 2231192
   BOARD 2231091, 223109
   FINAL ASSEMBLY 2231402

Hammer Driver P91 and P92

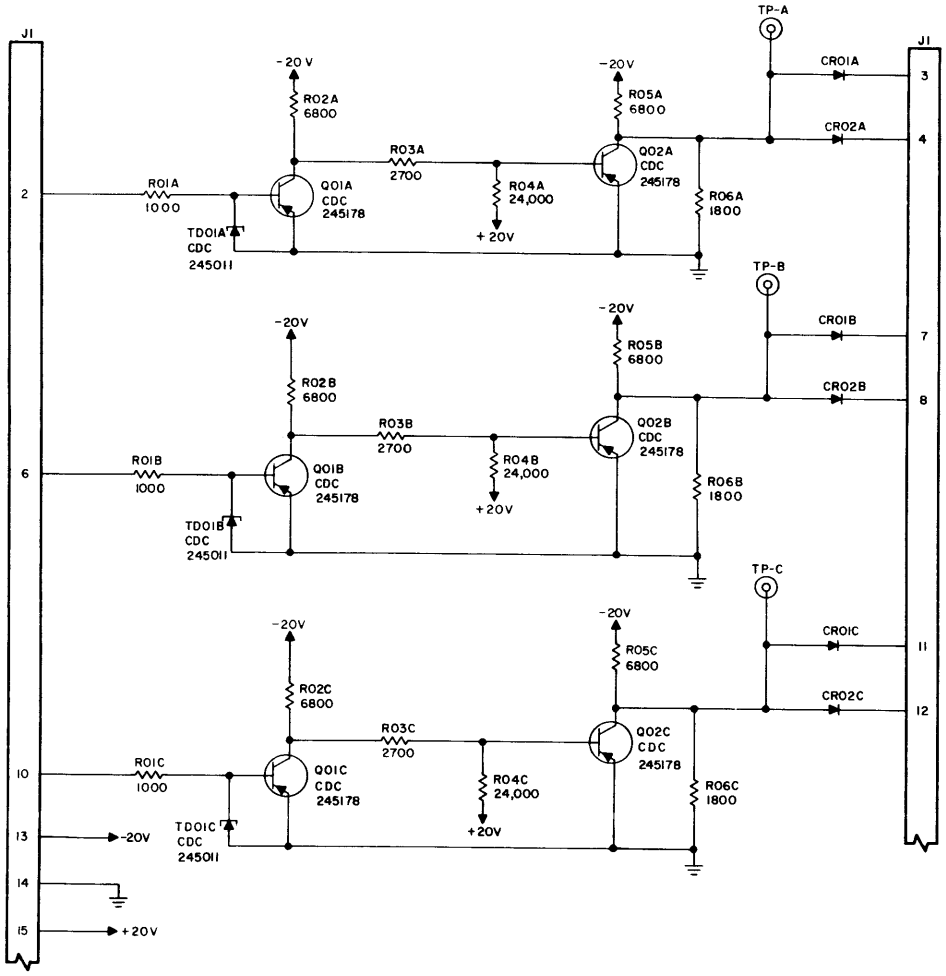
PULSE SHAPER
Card Type P93

(Normal Test Point Voltage: -4v, or ground)
Card type P93 contains three identical circuits, the function of which is to convert the irregular character, index, and paper strobe pulses into square wave, logic level outputs. Thus, a negative pulse is converted to a logical "1" (-3v), and a positive pulse is converted to a logical "0" (-0.5v).

A threshold level of discrimination is provided by the tunnel diode connected between base and emitter of transistor Q01 on each of the circuits. The tunnel diode exhibits two stable states. The voltage across it is quite low or relatively high, and it switches from one state to the other almost instantaneously.

As an example of card operation, assume that one of the circuits is receiving a positive-going input. This cuts off Q01. The base of Q02 is biased negative, and it conducts providing a steady -0.5v "0" output during the time that the circuit receives a positive input.

A low negative voltage also results in a zero output, if tunnel diode current is not sufficient to make it switch to its high voltage state. As the input signal approaches -2.7v, so that tunnel diode current is approximately 1 ma, the tunnel diode switches to its high voltage state and Q01 conducts. This causes Q02 to be cut off, so that the circuit output is held at -3v.



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5 %.
   ALL CAPACITORS ARE ±20 %.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231193
   BOARD 2231093
3. UNLESS OTHERWISE SPECIFIED
   ALL DIODES ARE CONTROL
   DATA DRAWING NUMBER 118012
   POLARIZED

Pulse Shaper P93

RIBBON ADVANCE

Card Type P94

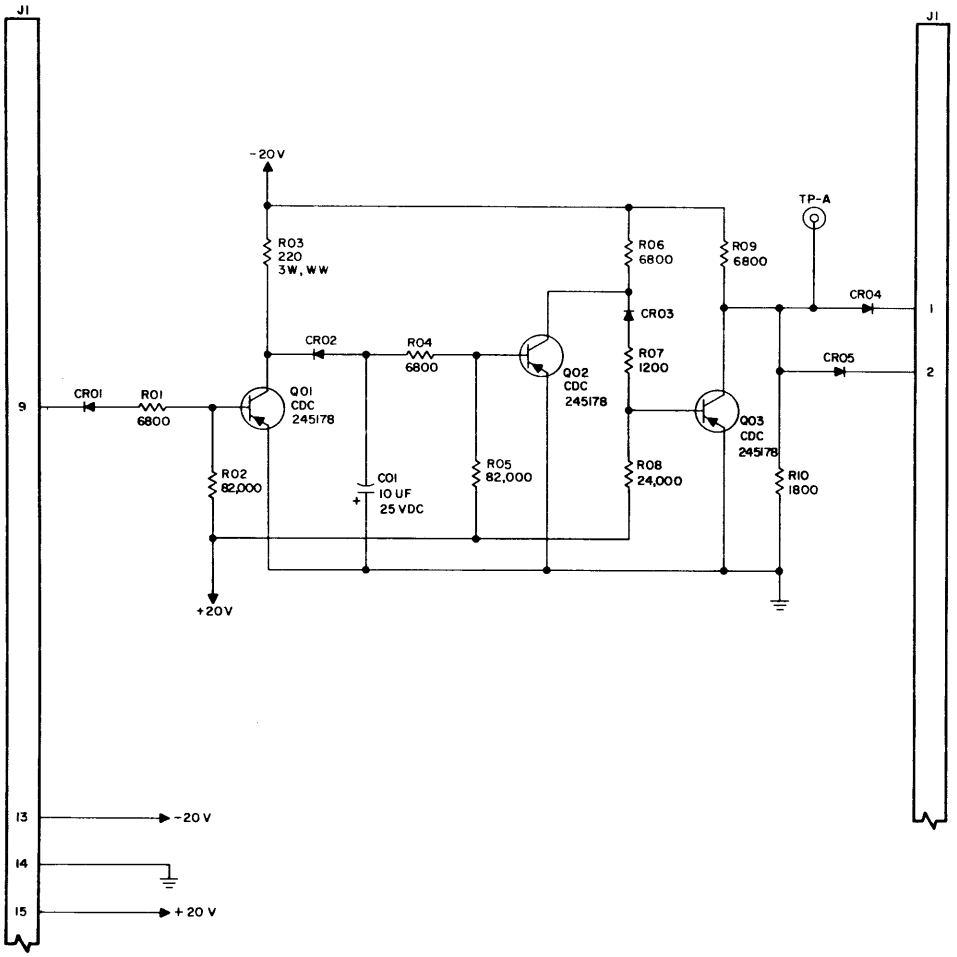
(Normal Test Point Voltage: -4v, or ground)

P94 enables the ribbon motion to continue for approximately 250 ms after paper motion has stopped. Inputs are received from pin 2 of the P96 card in the paper clutch circuit. The input levels are -0.5v and -36v, and the corresponding card outputs are -3v and -0.5v. Upon receipt of the -36v input, the -3v "1" output continues for approximately 250 ms before switching to the -0.5v "0" level.

As an example of card operation, assume that a -0.5v "0" input signal is being received on pin 9. The base of Q01 is at a positive voltage and is cut off. The base of Q02 is at a negative potential and conducts cutting off Q03, so that the output is a -3v "1". During the time that Q01 is cut off, the anode of CR02 is at approximately -15v, so that capacitor C01 obtains a negative charge.

A -36v signal causes Q01 to conduct; its collector goes to approximately ground potential. CR02 forces the charge on C01 to decay through R04 and R05. Q02 remains in its previous conduction state and the -3v output continues. When the negative charge on C01 has decayed sufficiently, Q02 is cut off. A negative potential then appears on the base of Q03, causing it to conduct, and the card output drops to -0.5v, which is a logical "0".

The time during which the charge on C01 causes Q02 to remain in its conducting state is not critical; it is designed to be approximately 250 ms.



NOTES:

1. UNLESS OTHERWISE SPECIFIED.
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5 %.
   ALL CAPACITORS ARE ±20 %.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231194
   BOARD 2231094
3. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE CONTROL DATA DRAWING NUMBER 118012, POLARIZED +▶|–

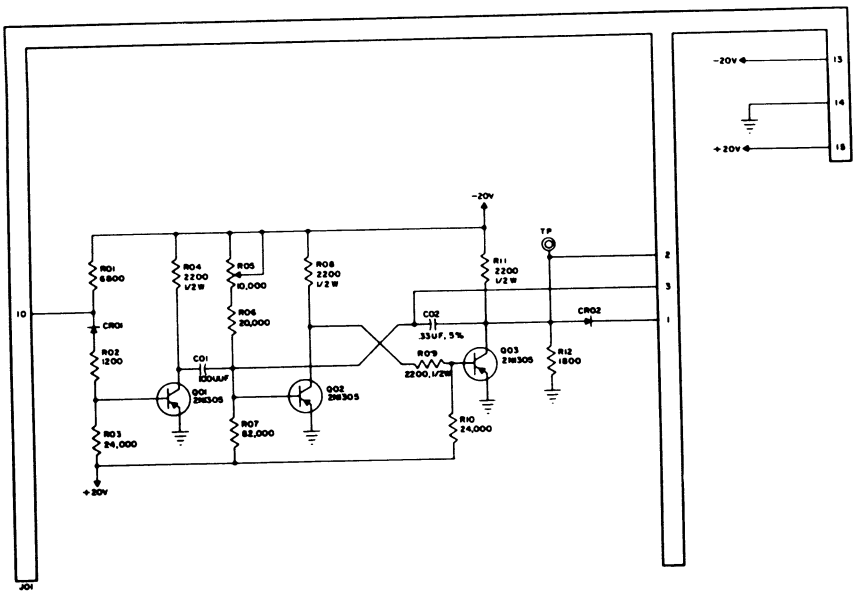
Ribbon Advance P94

BRAKE-CLUTCH ONE-SHOT
Card Types P95 and P99

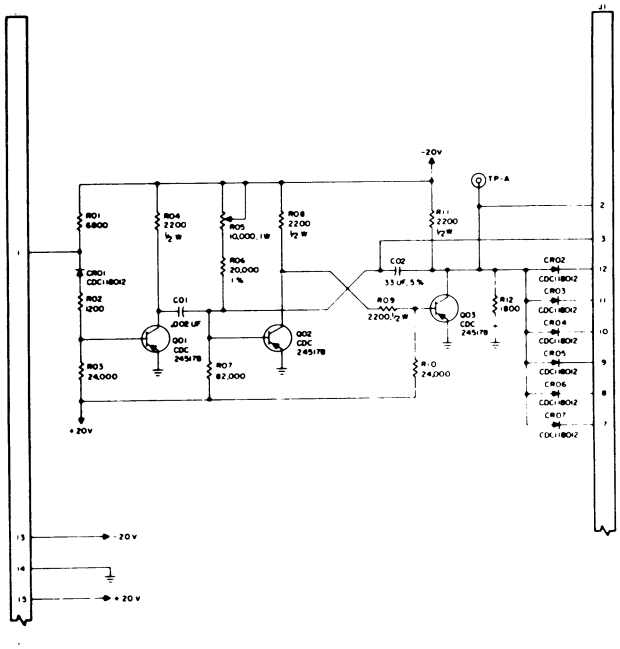
(Normal test point voltages: -9v, or ground)
These cards provide -0.5v "0" pulses of exactly 4 ms duration to the paper feed brake and clutch circuitry. For the major portion of its duty cycle, the card receives a "0" input and provides a steady "1" output. Upon receipt of a "1" input, the card output switches to "0" where it remains for 4 ms and then returns to a steady "1".

Assume that a "0" input is being received on pin 10. This puts a positive potential on the base of Q01 so that it is cut off. Due to the voltage-dividing action of R05, R06, and R07, the base of Q02 is at a negative potential and conducts. Q03 is therefore cut off, and the card output is a steady "1". The potential across capacitor C02 is approximately zero and the capacitor is uncharged.

A "1" signal causes Q01 to conduct; Q02 is cut off, and Q03 conducts. The card output goes to "0". The potential across C02 is no longer zero; it obtains a charge at a rate determined by the setting of R05. Thus, after a time of 4 ms, C02 has obtained a sufficiently negative charge so that Q02 conducts, Q03 is cut off, and the card output returns to a steady "1".



Brake-Clutch One-Shot P95



Brake-Clutch One-Shot P99

RIBBON DRIVE AND HOLD
Card Type P96

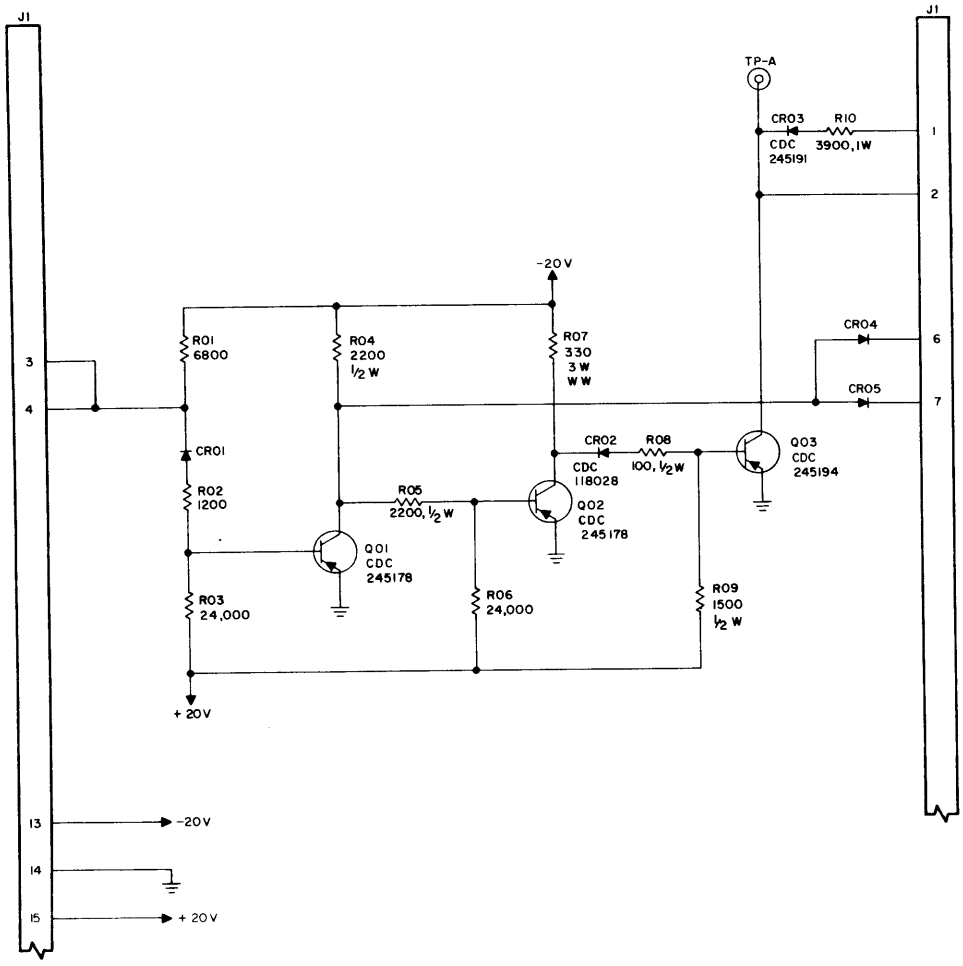
(Normal Test Point Voltages: -36v, or ground)
Card type P96 functions: as a logical inverter, in providing interlock signals to paper and ribbon feed circuitry; and as a switch, controlling the 200 ma ribbon drive current and the hold current of the paper clutch and brake.

The card receives logic inputs on pins 3 and 4. A logical "1" (-3v) input results in a logical "0" (-0.5v) output from pins 6 and 7, and enables Q03 so that 200 ma of negative current flows from pin 2 to ground. Upon receipt of a logical "0" input, the output from pins 6 and 7 changes to a "1" and the circuit from pin 2 to ground is opened.

As an example of card operation, assume that a -3v "1" signal is received on pins 3 and 4. This results in a potential of about -1v on the base of Q01, so that it conducts. The collector of Q01 therefore goes to approximately ground potential, placing a logical "0" signal on pins 6 and 7, and placing a positive voltage on the base of Q02. Thus Q02 is cut off, which places a negative voltage on the base of Q03 and causes it to conduct, closing the circuit from pin 2 to ground.

Similarly, upon receipt of a "0" input signal, Q01 is cut off and a "1" appears on pins 6 and 7. Q02 conducts, cutting off Q03, so that the circuit is broken from pin 2 to ground.

The connection at pin 1 and the diode CR03 provide a means of dissipating the high-voltage transient induced when the 200 ma of current flowing through the inductive coil is switched off. A connection is made at pin 1, producing a series circuit with the coil as the source of EMF. This prevents the inductive transient from damaging Q03 when the transistor is cut off.



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231196
   BOARD 2231096
3. UNLESS OTHERWISE SPECIFIED
   ALL DIODES ARE CONTROL DATA
   DRAWING NUMBER 118012
   POLARIZED

Ribbon Drive and Hold P96

HAMMER DRIVER ONE-SHOT

Card Type P97

(Normal Test Point Voltage: -9v, or ground)

Card type P97 provides a 0.5v "0" pulse of 1.3 ms duration to a print hammer driving circuit, upon receipt of a "0" pulse. This "0" input is received from a sense amplifying circuit, and is caused by a memory core switching during the read operation.

During the major portion of its duty cycle, this card produces a steady "1" output. A "0" input switches the output to "0" where it remains for 1.3 ms, and then automatically returns to a steady "1".

There are two OR inputs to the circuit used to gate the action, since both of these inputs must simultaneously be at -0.5v ("0") for the circuit to produce a "0" output pulse. If either input is at -3v ("1"), a "0" on the other input is not sensed, and the circuit produces a steady "1" output.

As an example of card operation, assume that a "1" input is being received. Thus, transistor Q01 has a base potential sufficiently negative for conduction, while Q02 has a positive base voltage and is cut off. This biases CR04 in the reverse direction, so that the output is sensed as a logical "1", and also applies a negative voltage to the base of Q03 causing it to conduct. Since Q02 is not conducting and the base of Q03 is at a small negative voltage during this time, there is a potential difference across C02 and it obtains a charge.

If the circuit receives a "0" input, Q01 is cut off and Q02 conducts, providing a "0" output signal and cutting off Q03. The potential of approximately -8v across C02 discharges at a rate set by R12 and R13. The value of R12 is adjusted so that, after 1.3 ms, C02 has gained a sufficient negative charge to cause Q03 to conduct. This places a positive voltage on the base of Q02, cutting it off, and the circuit output returns to a steady "1".

CHAPTER 6. PERIPHERAL EQUIPMENT CARDS

Relay Puller	ABA
Photo-Diode Bias and Preamplifier	ACA
Hammer Driver	ADA, ADB
Hammer Driver	ADC, ADD, ADE
Clutch-Brake Driver	ADH
Output Driver	AEB
Multiple Time Delay	AFA, AFB
Enable Amplifier	AGA
Flip-Flop Driver	AHA
Shift Driver	AIA, AIB
Photocell Amplifier	AKA
Power Supply	ALA
Write/Erase Driver	AMF, AMG, AMH, AMI
Head Select and Write Error Checker	ANB, ANC, AND
Exclusive OR Circuit	AOA
Gated Amplifier	ATA, ATB
Power Supply Regulator	AUA
Write Resistor Diode	AVA
Voltage Checker	AYA
Voltage Checker	BAA, BAB, BBA, BCA
Read Level Detector	EDA
Resistor Termination	EEA
Capacitor Termination	EEB
Capacitor Termination	EEC
Resistor Termination	EED
Capacitor Termination	EEE
Resistor Termination	EEF
Resistor Termination	EEG
Resistor Termination	EEH
Clock Amplifier	EFA
Read Level Detector	EGA
Read Preamplifier	EHA, EHB, EHC
Read Level Detector	EIA, EIB, EID, EIE
Potentiometer	EPA

Solenoid Driver	ERA
Delay Control Potentiometers	ESA
Differential Amplifier	EUA, EUC
Receiver Flip-Flop	EVB
Zero-Crossing Detector	EWA
Peak Detector	EWB
AGC Attenuator	EZA
Shaper Flip-Flop	FAB
Inner and Outer Track Select and Summing Networks	FCA, FCB
Oscillator	FDA
Clamp and Summing	FGA
Valve Amplifier	FHA
Power Amplifier	FIA
Servo Cycling Generator	FJA
Demodulator	FKA
Bridge Rectifier	FLA, FLB
Power Amplifier Output Stage	FMA
Retract Inverter and Current Source	FNA
Function Generator	FOA, FOB
Reference Amplifier	FPA
Velocity, Acceleration Summing Network	FRA, FRB, FRC, FRD
Operational Amplifier	FSA, FSB
Velocity Summing Network	FTA
Position, Velocity, and Acceleration Summing Network	FUA, FUB
Position and Acceleration Network	FVA
Temperature Servo Amplifier	FWA
Gated Amplifier	FXB
AGC Rectifier	FYA
Diode Card	GAA
Brake/Clutch Driver	GBA
500 Cycle Twin "T" Notch Network	GCA, GCB
Notch Networks	GCC
Relay Puller	IAA, IAB
Power Emitter Follower	IBA
Dual Driver	ICA
Write Driver	IIA

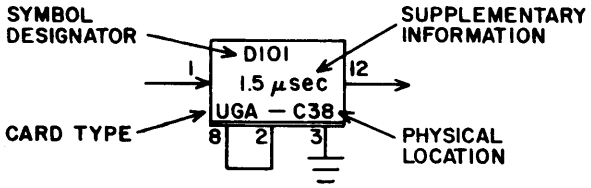
Flip-Flop Write Driver	IJA
Output Amplifier	IKA
Voice Coil Driver	ILA
Output Amplifier	INA
Head Selector	IOB, IOC, IOD
Output Amplifier	IPA
Output Amplifier	IQA
Output Amplifier	ISC
Pulse Delay and Output Amplifier	ITA, ITB, ITC, ITD
Output Amplifier	IYA
Positive Voltage Reference Switch	JBA
Negative Voltage Reference Switch	JCA
Long Stroke and Short Stroke Switch	JDA
Tuned Amplifier	JEB
Photocell Amplifier	OAA
Dual Photocell Amplifier	OCA
Read Peak Detector	ODA
Input Amplifier	OFA
Peak Detector	OGA, OGB, OBC
Peak Detector	OHA
Input Amplifier	OIA
Long Term Delay	OJB
Input Amplifier	OKA
Flyback Verify Flip-Flop	OLA
Input Amplifier, High Fan-Out	OMA
Photocell Amplifier	ONA
Input Amplifier	OPA
Input Amplifier	OQA
Comparator and Readout	ORA
Input Amplifier	OSA, OSB
Level Switch	OTA
Schmitt Trigger	OUA
Gated Pulse Shaper	OVA
Input Amplifier	OYA
Adjustable Delay	UAA, UAB

Double Inverter	UBA
Adjustable Pulse Delay	UCB
Oscillator Calibrator	UEA
Voltage Controlled Delay	UFA, UFB
Voltage Controlled Pulse Delay	UGA
Adjustable Short Term Delay	UHB
Pulse Shaper	UIA
Adjustable Long Term Delay	UJB, UJC
Gated Toggle Flip-Flop	UKA
Gated Toggle Flip-Flop	UKB
Pulse Shaper	XKA, XKC

LOGIC SYMBOLS

All special modules (including delays*) are represented by rectangles. Inputs are shown with arrows normally from the left, and outputs normally extend out to the right. Other connections to the card such as jumpers and grounds, except disabled OR inputs, are shown without arrowheads. The double bar on one or more sides of the symbol is used to indicate a non-logic voltage level.

EXAMPLE



* Passive delays such as capacitors mounted on a card are represented by an oval symbol (see section 2).

MODULE DESIGNATION

Five general categories are used for classifying special purpose circuits for peripheral equipment:

1. A-D (AA-, AB-, ····· DY-, DZ-)
2. E-H (EA-, EB-, ····· HY-, HZ-)
3. I-N (IA-, IB-, ····· NY-, NZ-)
4. O-T (OA-, OB-, ····· TY-, TZ-)
5. U-Z (UA-, UB-, ····· ZY-, ZZ-)

The two most significant letters (IA-, for example) define the basic circuit. The least signficant letter defines slight variations with the possibility of interchange in some but not all applications. Standard power supply connections are -20v on pin 13, ground on pin 14, +20v on pin 15, and no low impedance voltage sources on other pins. Standard voltage levels on input and output are -0.5v and -3v and match internal logic of standard cards such as flip-flops and inverters (including the 10, 20, and 30 series). Nonstandard input (or output) signals indicate one or more inputs (or outputs) that may be analog or digital, but cannot generally interface with standard cards such as flip-flops and inverters.

Category	Designation	Power Supply	Input	Output
A	AAA to DZZ	Nonstandard	Standard or Nonstandard	Standard or Nonstandard
E	EAA to HZZ	Standard	Nonstandard	Nonstandard
I	IAA to NZZ	Standard	Standard	Nonstandard
O	OAA to TZZ	Standard	Nonstandard	Standard
U	UAA to ZZZ	Standard	Standard	Standard

601 DAISY CHAIN LINE TRANSMISSION SYSTEM

The term "601 Daisy Chain Line Transmission System" is derived from its initial application as a digital-signal connection on a time-shared line between several (8 max.) 601 Tape Transports and a 3127 Controller. The following description contains background and ground rules for this system and presents information for other possible applications.

Design criteria included the following:

1. Three output amplifier circuits and three input amplifier circuits, 1604-type cards with pin assignments compatible with existing 69-and 87-type cards.
2. Provision for paralleling multiple output amplifiers (transmitters) and input amplifiers (receivers) at any point on the same line, with or without power supply voltage available.
3. Ability to transmit 1-usec logical "1" pulses from any output amplifier through any input amplifier to set a 1604-series flip-flop (500 kc maximum transmission rate).
4. Ability to operate with standard 24-pin I/0 cables (23 twisted pairs with one side of each pair grounded) over a length of 100 feet or more.
5. Simplification of terminators and bias voltages for terminators and output amplifiers.
6. Circuits capable of operating in 25°C to 50°C ambient air.

With the above basic design objectives, the approach was taken to simplify special output amplifier and terminator biasing requirements by employing line signals that drive away from ground. Thus both shorts and opens on a line result in a logical "0" at a receiver. Output amplifiers cannot drive a "1" on a line without power supply voltages, and both input and output amplifiers have disconnect features built in to prevent unwanted loading of the time-shared line when power supply voltages are off in some units.

The twisted-pair cable is satisfactory from an attenuation standpoint over 100-foot lengths but does present crosstalk problems unless rise and fall times are limited in volts per microsecond. A controlled rise and fall time of ½ usec for the 2-volt swing is used as a compromise

with speed. Crosstalk can be further reduced by using coax. However, unless bulky coax cables are used, attenuation increases and the characteristic impedance decreases; this requires greater line current (higher power levels) or lower voltage excursions, or results in reflections and ringing from improper terminations. The connector used with the 24-pin I/O cables permits the mounting of 23 terminating resistors directly to 23 pins (with one end of the resistors grounded to the remaining pin). Power in each termination is low (1/30 w for 120 ohms) for a logical "1" and essentially zero for a logical "0" on the line. This provides a terminator that can fit in the same space as a 24-pin I/O cable and still be reasonable in cost. Where module flexibility of extending cables is not required, input amplifiers with built-in terminating resistors are available; and the jumper option on the output amplifier may be employed without requiring external terminator resistors.

The voltage excursion of the output amplifier was selected to have a basic excursion that would be about five times the tolerance of the expected input amplifier switching threshold and twice the nominal switching threshold value of the input amplifier. A 2-volt excursion allows realistic tolerances in parts employed in the output and input amplifiers and a margin of safety for ringing, crosstalk, attenuation, and external interference for both logical "0" and logical "1" signals on the line. The positive excursion of the line connecting the output and input amplifiers was selected from a standpoint of circuit simplicity and cost. It is also more compatible with the newer positive logic computer circuits employing silicon components. In each circuit, two transistors are required. One transistor is used for inversion to standardize the voltage excursion over a small input threshold, and the other transistor provides current amplification.

The output amplifier, which receives its input from standard logic, was also designed to have a switching threshold tolerance that permits some noise on its input whether in the "0" or "1" state. Both stages of the output amplifier and one stage of the input amplifier use high-frequency npn silicon transistors. These provide a good compromise in voltage breakdown, power capability, and switching uniformity at moderate cost.

This system may not be ideal in <u>each</u> of the performance criteria,

but it does provide a useful application region within the following ground rules:

1. OS..series input amplifiers are designed to switch at $+1.0 \pm 0.2$v. System application should provide a minimum "1" line signal of +1.6v and a maximum "0" line signal of +0.3v. This allows a reserve for seldom-encountered signal interference and variable factors not usually predictable or easily measured, such as:
   a. Crosstalk from outside interference.
   b. Partial drive leakage from parallel output amplifiers not remaining completely off because of power supply coupling, for example. (This could produce an erroneous "1".)
   c. Slight changes in input amplifier switching because of aging, ambient temperature changes, or small errors in initial card testing measurements.
   d. Imperfections in ground reference points.

   The minimum "1" line signal of +1.6v and the maximum "0" line signal of +0.3v shall be attainable under <u>any</u> combination of the following worst-case conditions:
   a.* +20v power supply of IS..series or equivalent output amplifier at lowest expected value (minimum IS..series output voltage into a 60-ohm load is +2.0v with a +20v power supply and proportionably less as +20v is decreased).
   b.* Maximum line attenuation calculated on the basis of cable type and maximum distance between any output amplifier and input amplifier.
   c.* Maximum number of OS..or equivalent input amplifiers to be connected to a signal line. (With power on, each OS..causes a 0.03v maximum negative bias to a line terminated in 120 ohms at both ends.
   d. Maximum crosstalk from other signals in the cable. (Worst case is usually when other signals are closely in phase; position of worst-case crosstalk varies much over a cable length with cables.)

e. Maximum ringing because of reflections of non-ideal cable and termination conditions.

* These conditions (a, b, and c) tend to reduce the "1" line signal margins. It may be the best compromise to increase cable termination to 150 ohms where "1" signal margins are used up before the "0" signal margins. The following 24-pin terminators are documented for production. (Pin b is the ground reference in all units.)

Part No.	Ohms ±5%
45948500	56
45948501	68
45948502	82
45948503	100
45948504	120
45948505	150
45948506	180
45948507	220

2. If the rules of paragraph 1 are satisfied, up to 8 output and 8 input amplifiers may be paralleled on any signal line. They may be grouped or located at different locations. Lines should not "Y" out to several ends, although short stubs may be used to wire to input or output amplifiers. Terminators shall be placed within 3 feet of the end of each cable.

3. Time-shared lines are subject to a "1" coming from any output amplifier on the line. While the system is designed to work with either power on or off on inactive output amplifiers (no external bias required), power sequencing of equipment should provide one of the following during the turning on or turning off of power of any unit with an output amplifier:

   a. Disconnecting +20v from pin 15 of IS.. series cards during time any input can approach a logical "1" threshold.

   b. Clamping the input of the amplifier at ground and

assuring that the +20v supply does not exceed the -20v supply by more than 20 percent.

c. Disabling the AND gates at the output of all input amplifiers (receivers).

d. Providing a program that can repeat an operation when errors are received because of erroneous "1" signals coming from power sequencing operations.

4. The following card types are the present family of cards using this transmission system:

a. ISA Output Amplifier (3 circuits) -- preproduction version of the ISC, but with less predictable turnoff time from "1" to "0".

b. ISC Output Amplifier (3 circuits) -- 0.5 $\pm$0.15 usec rise and fall times. Optional 120-ohm termination to ground for each of the three circuits by using external jumpers. For best results, use caution on loading test point.

c. ITA Pulse Delay and Output Amplifier (1 circuit) -- pins 1 - 8 perform delay function of UGA. Pins 11 and 12 are output and optional 120-ohm termination respectively.

d. ASA Quantizer and Output Amplifier (3 circuits) -- Quantizing point is designed for about -6v but usable above and below this value with variations in fall time. Circuit is generally less uniform in output waveform than ISC. A 120-ohm terminating resistor is permanently wired to the output. Therefore, the circuit is designed to be located only at one of two ends of a line.

e. OSA Input Amplifier (3 circuits) -- No input termination resistor available. Input is single-ended to ground and output of each circuit has 3 AND diodes to match standard logic.

f. OSB Input Amplifier (3 circuits) -- Like the OSA except with 120-ohm input termination to ground. Therefore, the circuit is designed to be located only at one of the

two ends of a line. The OSB does not include all the line-loading disconnect features of the OSA when power is turned off.

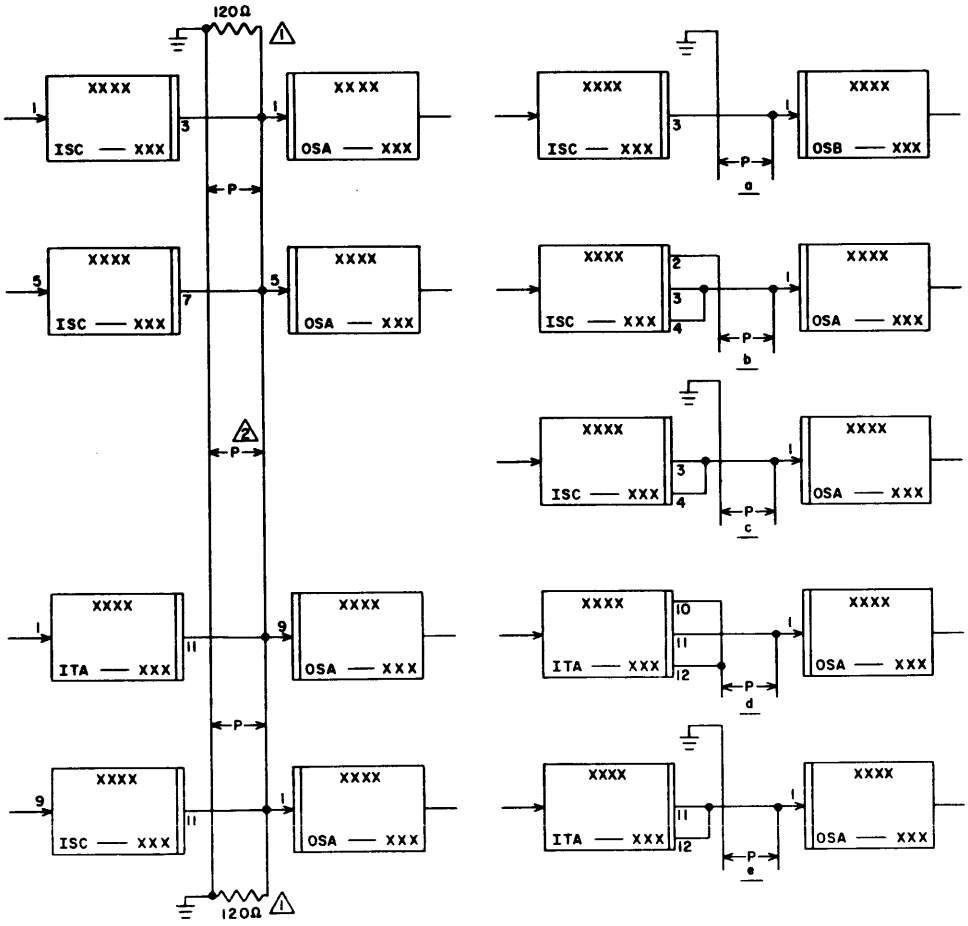
As required in future systems, the family of cards may be expanded to include the following:

a. Output amplifier with fast rise and fall times.

b. Output amplifier with 2 or 3 OR inputs but with only 2 circuits.

c. Input amplifier with differential input stage for common-mode interference rejection on twisted-pair lines.

d. Input amplifier with 0.7v nominal switching point for longer impedance terminations.



601 DAISY CHAIN WIRING SHOWING 4 OUTPUT AND 4 INPUT AMPLIFIERS ON A TIME — SHARED LINE

NOTE:
⚠1 ALTERNATE WAYS OF TERMINATING A LINE ARE SHOWN IN a, b, c, d, and e.
⚠2 TWISTED PAIR

RELAY PULLER
ABA

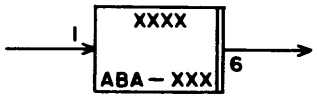
This circuit is used to drive high surge current loads such as lamps or the discharge of capacitors, or inductive loads such as relays and solenoids. It is particularly useful in driving loads up to 0.6 amp which are terminated at negative voltages between -5v and -36v.

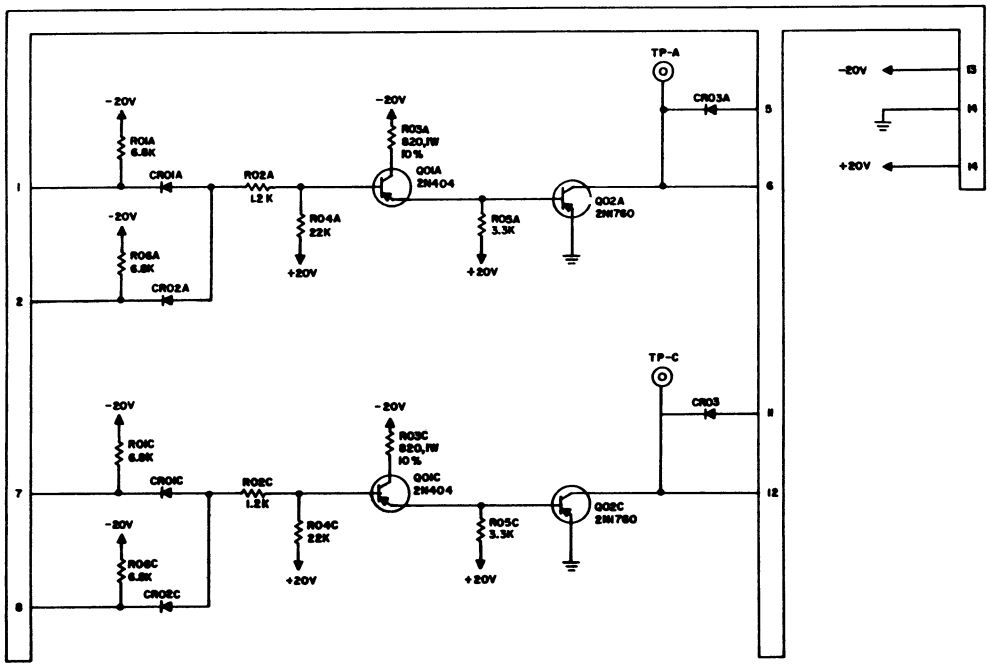
The relay puller circuit can also be used as a slow speed L--- card. The input-output voltage levels are the same for both cards.

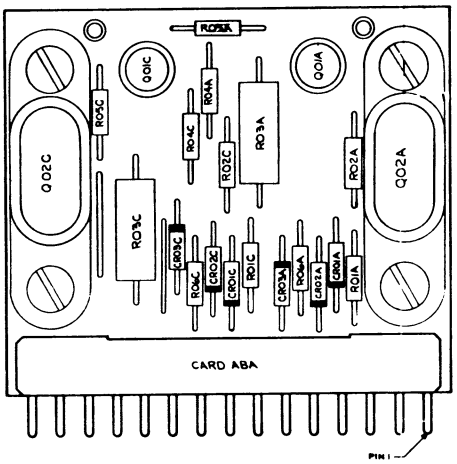
This circuit is similar to the IAA relay puller, but has an added "OR" input on each of the two circuits as well as a clamping diode available on pins 5 and 11 to limit the negative excursion when inductive loads are switched off.

The input stage of the relay puller circuit has its transistor connected as an emitter follower with the collector returned to -20v through a limiting resistor, R03. The first stage emitter follower current does not flow through the load as it does in circuits such as the 55 card, thereby limiting collector voltage on Q01 to -20v; Q02 may have excursions to -50v. The only current flowing to the load in the turnoff condition is the leakage current of the output transistor. Turnon time is 5 usec maximum and turnoff switching is 25 usec maximum.

SYMBOL




TP-A
TP-C
-20V
+20V
R01A
6.8K
CR01A
R02A
1.2K
R03A
820,1W
10%
Q01A
2N404
Q02A
2N760
R04A
22K
R05A
3.3K
CR02A
R06A
6.8K
CR03A
CR03
R01C
6.8K
CR01C
R02C
1.2K
R03C
820,1W
10%
Q01C
2N404
Q02C
2N760
R04C
22K
R05C
3.3K
CR02C
R06C
6.8K
CR03C
1
2
5
6
7
8
11
12
13
14
15

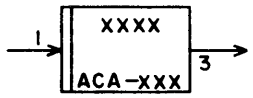

R05A
Q01C
Q01A
R04A
R05C
R04C
R03A
R02C
R02A
Q02C
Q02A
R03C
CR03C
R04C
CR02C
CR01C
R01C
CR03A
R04A
CR02A
CR01A
R01A
CARD ABA
PIN 1

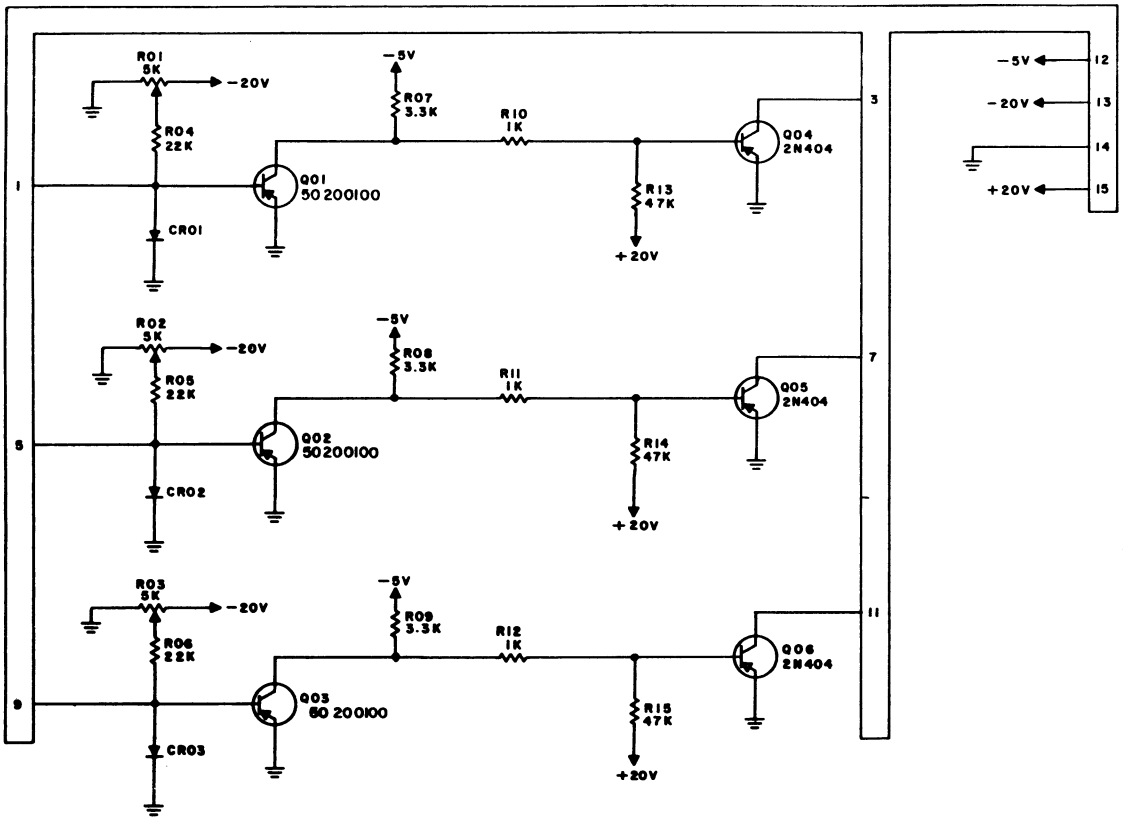
PHOTODIODE BIAS AND PREAMPLIFIER
ACA

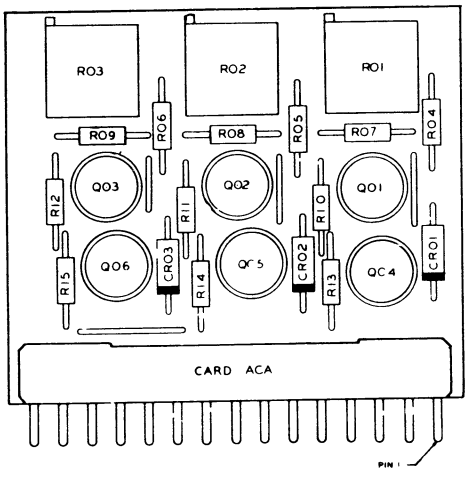
The photocell amplifier is designed to receive inputs from photodiodes or silicon solar cells. The output of the amplifier may be terminated by the input of a standard inverter or an "M" card. The output from the standard inverter or "M" card is a "1" when the photocell is illuminated and a "0" when unlighted. A potentiometer is provided because of the low level signals normally available from the solar cells and the wide range of sensitivity of photodiodes. This allows optimum centering of the switching point of the amplifier to compensate for the overall photocell excitation, sensitivity, and amplifier tolerance.

The first stage of amplifier A consists of an inverting amplifier, Q01. This transistor is turned on by drive current flowing through R04 from potentiometer R01. One lead of the photodiode is connected to pin 1 and the other lead is connected to a positive voltage source. Light on the photodiode causes its conductivity to increase and the photodiode current counteracts the turnon current of R01. CR01 limits the base to emitter voltage of Q01. When using solar cells, the positive terminal is normally connected to pin 1, and the output current of the solar cell counteracts the turnon current of R01.

SYMBOL




R01
5K
-20V
R04
22K
CR01
Q01
50200100
-5V
R07
3.3K
R10
1K
R13
47K
+20V
Q04
2N404
R02
5K
-20V
R05
22K
CR02
Q02
50200100
-5V
R08
3.3K
R11
1K
R14
47K
+20V
Q05
2N404
R03
5K
-20V
R06
22K
CR03
Q03
50200100
-5V
R09
3.3K
R12
1K
R15
47K
+20V
Q06
2N404
1
5
9
3
7
11
-5V
-20V
+20V
12
13
14
15


R03
R02
R01
R09
R06
R08
R05
R07
R04
Q03
Q02
Q01
R12
R11
R10
CR03
CR02
CR01
Q06
QC5
QC4
R15
R14
R13
CARD ACA
PIN 1

HAMMER DRIVER CARD
ADA, ADB

These cards are intended for low-speed switching of high current pulses of 1.5 to 4.5 msec duration into an inductive load such as the hammers, clutch, or brake in a 501 Printer. An open circuit on pin 1 or -3 volts will keep the circuit off. Driving pin 1 to within -0.5 volt of ground allows a current pulse to flow up to 10 amp for the ADA and 7 amp for the ADB. The duty cycle should be no greater than 12 percent, to avoid excessive heating. The minimum input pulse width needed to reach 2 percent of the maximum current level with an inductive load should be about 4 times the L/R time constant of the load. The total collector circuit resistance should be sufficient to limit the load current to 10 amp maximum for the ADA. The ADB has a 4-ohm resistor mounted on the card in the collector circuit of Q03. With a purely resistive load, the current rises to the 10 amp level in 20 usec typically.

For normal operation of the circuit, the following connections are made (see circuit schematic). One side of the load plus the limiting resistor (for the ADA) is connected to pin 10 or 11. The other side is connected to the high current negative supply which can have a maximum value of -38 volts but is nominally -36 volts. Pin 8 is also connected to the -36v supply. This returns a suppression circuit consisting of CR05 and R07 to the emitter of Q03 via the power supply (-36v) common at pins 5 and 6. For good inductive spike supression, it is evident that the -36 volt lines and power supply impedance must be low. The suppressed pulse is about 10v greater than the power supply voltage. The usual + and -20 volt supplies must also be furnished to the circuit. Normally, the logic ground and high current ground are tied together at the card connector. This is done to minimize the tendency for the circuit to oscillate.

Referring to the schematic, the circuit operates as follows. Transistors Q02 and Q03 comprise a Darlington pair in a collector-loaded switch circuit. This pair is normally off with pin 1 at -3 volts. Transistor Q01 conducts when pin 1 is -3v; its collector is

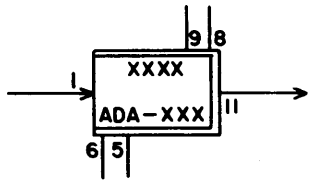
then at ground. This establishes +1.2 volts on the base of Q02 due to current flow from the +20 supply through R05 and silicon diodes CR02 and CR03 to ground. The emitter of Q02 and hence the base of Q03 is at +0.5 volt due to current from +20 volt through R06 and CR04 to ground. Both Q02 and Q03 are therefore off because of the reverse base voltages.

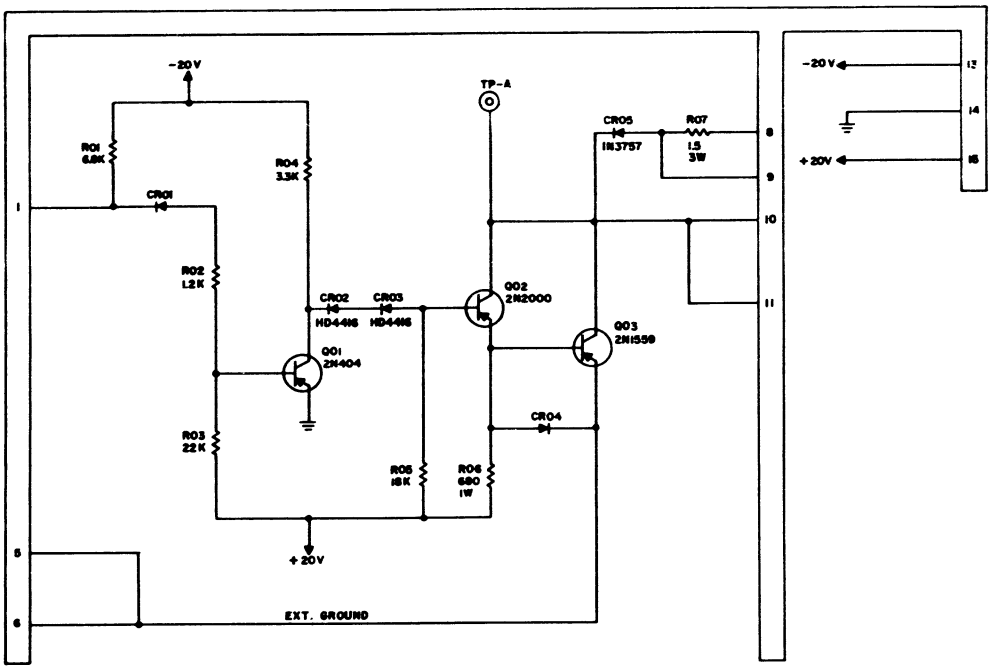
When the input goes to within -0.5 volt of ground, transistor Q01 goes off due to the divider action of R02, R03, and CR01, i.e., the base becomes positive. With Q01 collector unclamped, base current begins to flow in Q02 and Q03 from ground to the -20v supply by way of the collector load resistor R04. This turns on the Darlington circuit and lets load current flow.

In the on state and with a 10 amp load on the ADA card, the collector to emitter voltage of Q03 is about 0.5 volt. With a 12 percent duty cycle the power dissipated in Q03 is about 0.75 watt. In free air (i.e., natural convection) this dissipation causes Q03 to attain 135°F case temperature in 80°F ambient.

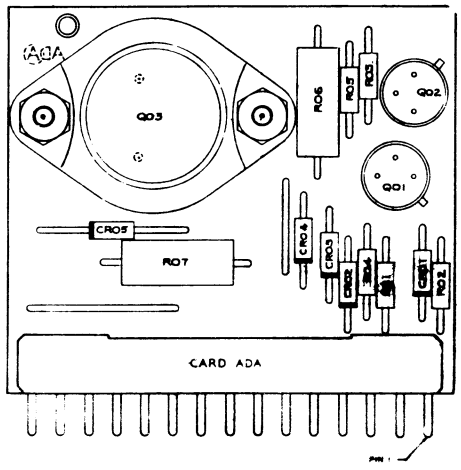
It is recommended that these cards be placed in moving air and away from any temperature sensitive circuits.

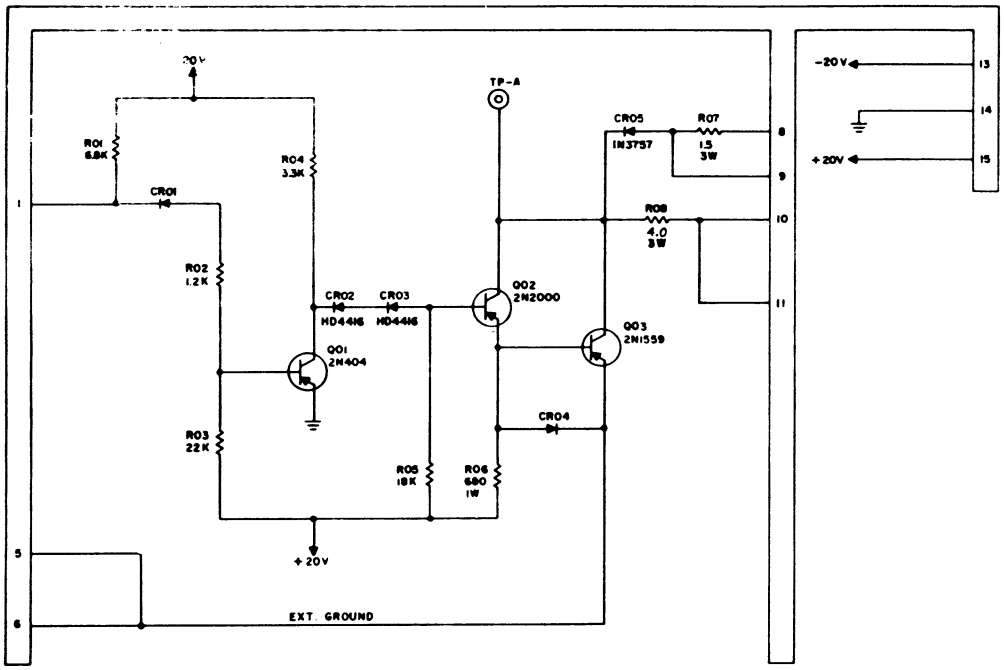
SYMBOL



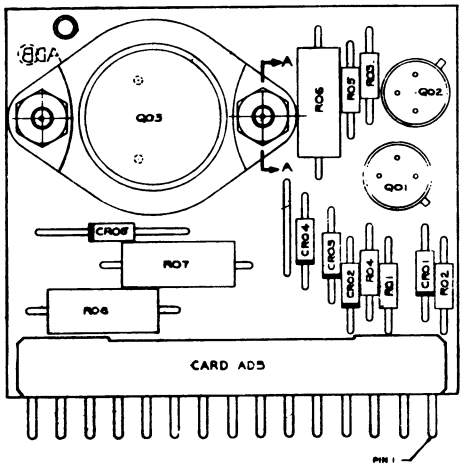

-20 V
TP-A
R01
6.8K
R04
3.3K
CR01
R02
1.2K
CR02
HD4416
CR03
HD4416
Q02
2N2000
Q03
2N1559
Q01
2N404
CR04
R03
22K
R05
18K
R06
680
1W
CR05
1N3757
R07
1.5
3W
+ 20V
EXT. GROUND
-20 V
+ 20V
1
5
6
8
9
10
11
12
14
15

ADA


ADA
Q03
R06
R03
R01
Q02
Q01
CR05
R07
CR04
CR03
CR02
CR01
R02
CARD ADA


20V
TP-A
R01
6.8K
R04
3.3K
CR01
R02
1.2K
CR02
HD4416
CR03
HD4416
Q02
2N2000
Q01
2N404
Q03
2N1559
CR04
R03
22K
R05
18K
R06
680
1W
+20V
EXT. GROUND
CR05
1N3757
R07
1.5
3W
R08
4.0
3W
-20V
+20V
1
5
6
8
9
10
11
13
14
15

ADB


Q03
R06
R05
R08
Q02
Q01
CR05
R07
R04
CR04
CR03
CR02
R01
CR01
R02
R08
CARD ADB
PIN 1

HAMMER DRIVER
ADC, ADD, ADE

The ADC, ADD, and ADE cards are used in the 501 Printer to supply 5 amp (ADC) and 7 amp (ADD, ADE) current pulses of 1.3 msec duration to the basically inductive hammer coils. An open circuit on pin 1 or -3 volts will keep the circuit off. Driving pin 1 to within -0.5 volt of ground lets the load current rise to its 5 or 7 amp levels. The maximum duty cycle of 3 percent must not be exceeded in order to keep the average transistor dissipation to a safe level.

For normal operation of the circuit, the following connections are made (see circuit schematic). One side of the hammer coil is connected at pin 10 or 11 and the other side is connected to the high-current negative power supply. The negative supply voltage is nominally -29 volts for the ADC and -36 volts for the ADD and ADE. Pin 7 or 8 is also connected to this negative supply for suppression of the inductive kick pulse. Since the suppression circuit is returned to the circuit common via the line and supply impedances, these must be kept low to insure reduction of the voltage spike across Q03. The suppressed pulse across Q03 on the hammer driver cards is limited to about 10 volts. The inductive kick pulse is brought out to pin 9. This may be used in conjunction with the OLA card in error checking systems. The pulse is about 100 usec wide with the ADC and 1 msec with the ADD and ADE cards.

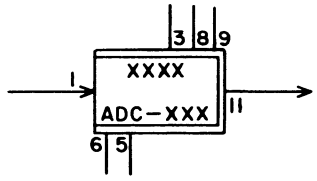
Referring to the schematic, the circuit operates as follows. Transistor pair Q02 and Q03 make up a Darlington switching circuit. The pair is normally off when pin 1 is at -3 volts on the base of Q02 due to current flow from the +20 supply through R06 and silicon diodes CR02 and CR03 to ground. The emitter of Q02 and hence base of Q03 is at +0.5 volt due to current flow from +20 volts through R07 and CR04 to ground. Both Q02 and Q03 are therefore off because of the reverse base voltage.

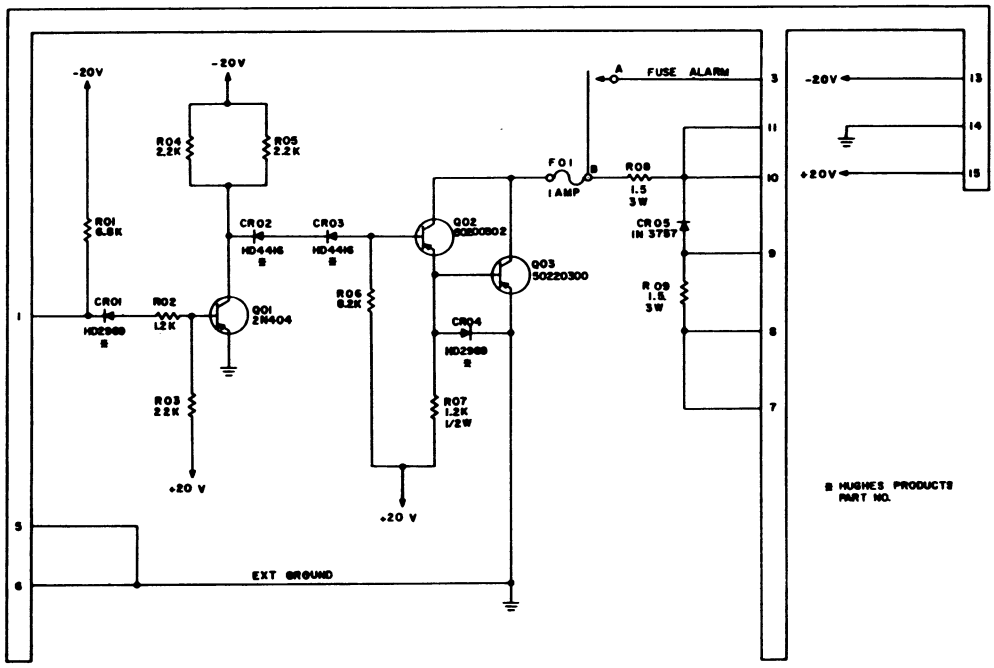
When the input goes to within -0.5 volt of ground, transistor Q01 goes off due to the divider action of R02, R03, and CR01, i.e., the base becomes positive. With Q01 collector unclamped, base current begins to flow in Q02 and Q03, from ground to the -20v supply by way of collector load resistors R04 and R05 in parallel. This turns on the

Darlington pair and allows the load current to flow.

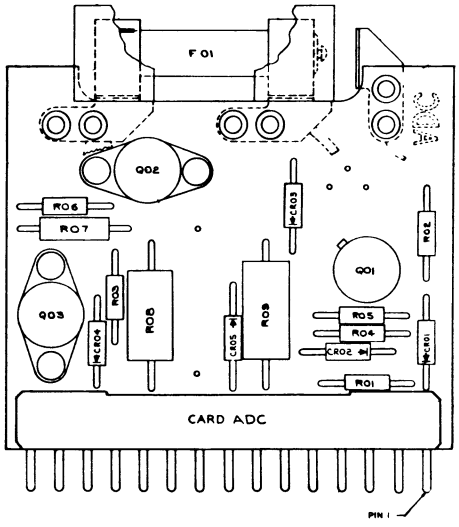
In the on state and with a 3 percent duty cycle, the average dissipation in the collector load resistor with 7 amp and 3 percent duty cycle is about 2 watts. This gives a temperature on the resistor of about 180° F. This necessitates placing the card in moving air to eliminate damage to the card.

SYMBOL

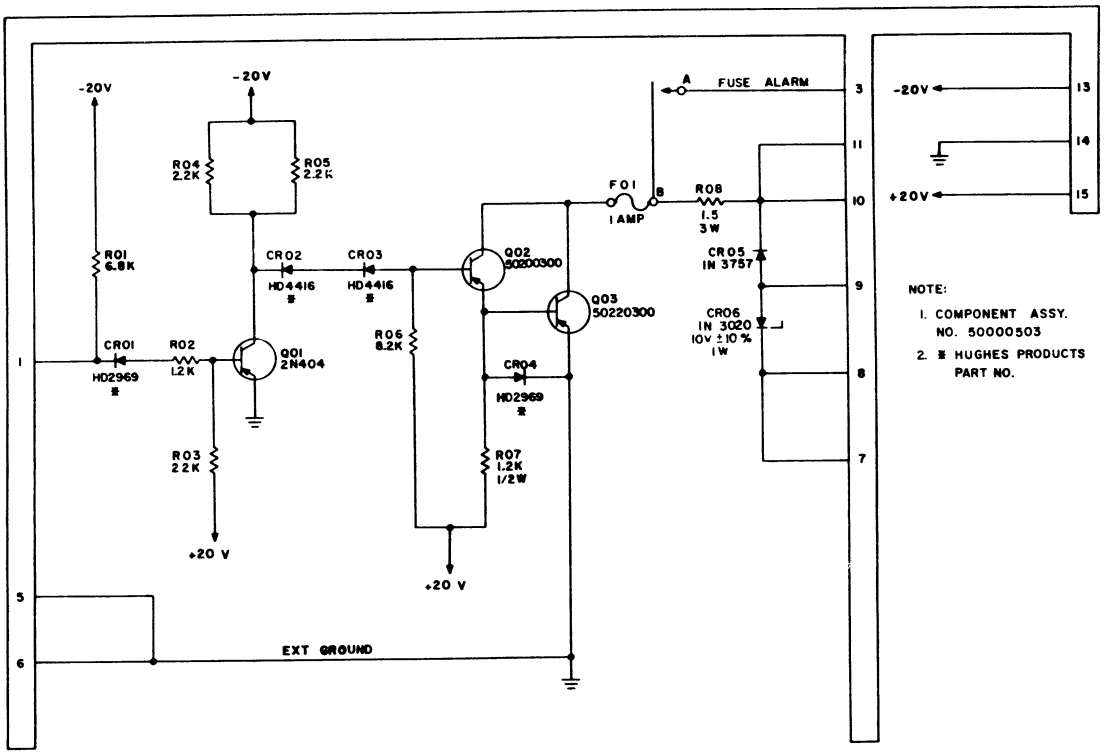




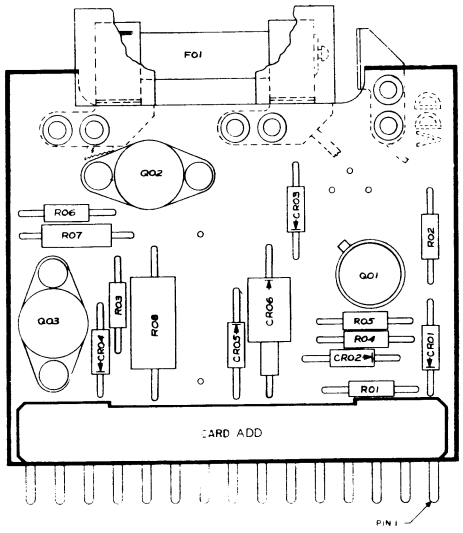
ADC

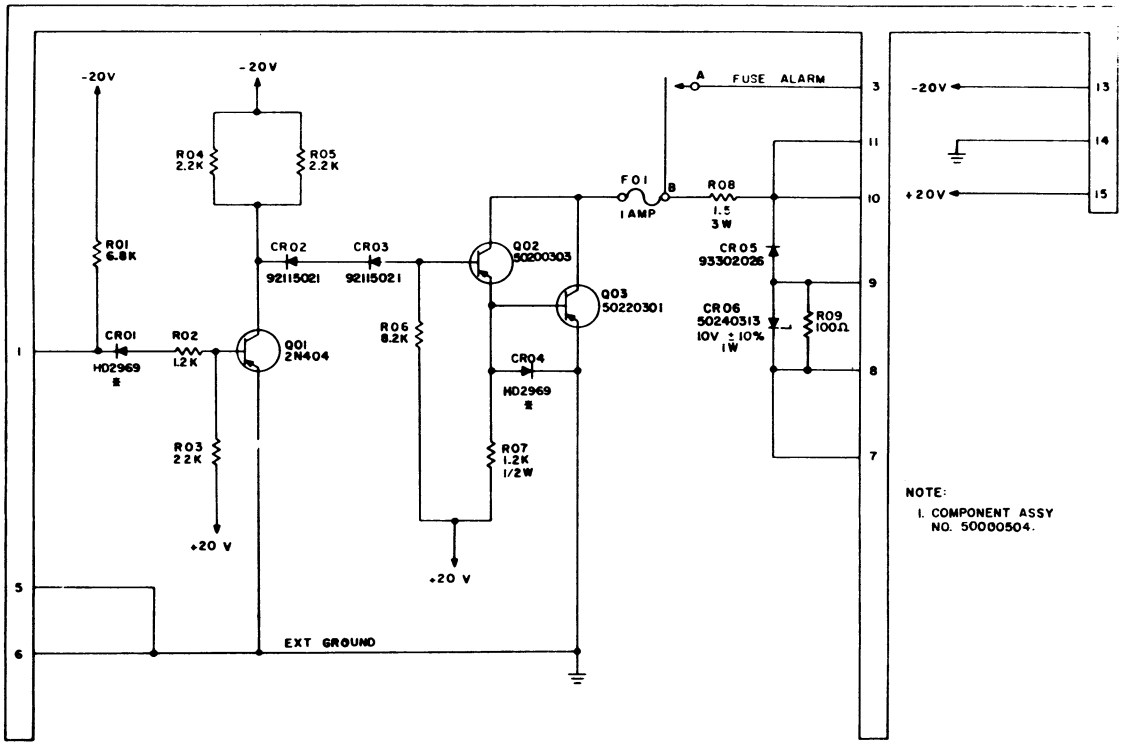


6-ADC, ADD, ADE-2

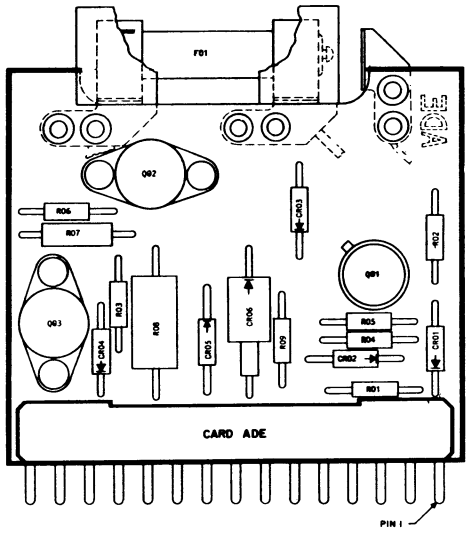

-20V
-20V
R04 2.2K
R05 2.2K
R01 6.8K
CR02
HD4416 #
CR03
HD4416 #
Q02 50200300
Q03 50220300
F01 1AMP
R08 1.5 3W
A FUSE ALARM
CR05 IN 3757
CR06 IN 3020 10V ±10% 1W
CR01 HD2969 #
R02 1.2K
Q01 2N404
R06 8.2K
CR04 HD2969 #
R07 1.2K 1/2W
R03 2.2K
+20 V
+20 V
EXT GROUND
-20V
+20V
NOTE:
1. COMPONENT ASSY. NO. 50000503
2. # HUGHES PRODUCTS PART NO.

ADD


F01
Q02
R06
R07
CR03
R02
Q01
Q03
R03
R08
CR04
CR05
CR06
R05
R04
CR02
R01
CR01
CARD ADD
PIN 1


-20V
-20V
R04 2.2K
R05 2.2K
R01 6.8K
CR01 HD2969
R02 1.2K
Q01 2N404
R03 2.2K
+20 V
CR02 92115021
CR03 92115021
Q02 50200303
Q03 50220301
R06 8.2K
CR04 HD2969
R07 1.2K 1/2W
+20 V
EXT GROUND
A FUSE ALARM
F01 1 AMP
B
R08 1.5 3W
CR05 93302026
CR06 50240313 10V ± 10% 1W
R09 100Ω
-20V
+20V
NOTE:
1. COMPONENT ASSY NO. 50000504.

ADE


F01
Q02
R06
R07
CR03
R02
Q01
Q03
R03
R08
CR04
CR05
CR06
R09
R05
R04
CR02
CR01
R01
CARD ADE
PIN 1

CLUTCH-BRAKE DRIVER
ADH

This card is used for low-speed switching of high current pulses of 4.5 msec duration into an inductive load such as the clutch or brake in a 501 printer. An open circuit on pin 1 or -3 volts will keep the circuit off. Driving pin 1 to within -0.5 volts of ground allows a current pulse up to 15 amperes to flow. The duty cycle should be no greater than 12 percent. The minimum input pulse width needed to get 15 amperes into an inductive load should be about 4 times the L/R time constant of the load. An external resistor has to be added to limit the current to 15 amperes maximum. With a resistive load, the minimum input pulse width should be as great as the rise time of the circuit - in this case, 50 usec.

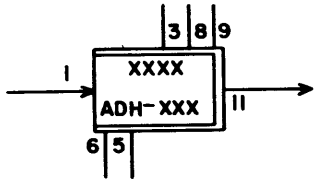
For normal operation of the circuit the following connections are made (see circuit schematic). One side of the load plus the limiting resistor is connected to pin 10 or 11. The other side is connected to the high current negative supply, which can have a maximum value of -38 volts but is nominally -36 volts. Pin 8 is also connected to the -36v supply. This returns a suppression circuit consisting of CR05 and R07 to the emitter of Q03 via the power supply (-36v) common at pins 5 and 6. For good inductive spike suppression, it is evident that the -36 volt lines and power supply impedances must be low. The suppressed pulse is about 10v greater than the power supply voltage. The usual + and -20 volt supplies must also be furnished to the circuit. Normally the logic ground and high current ground are tied together at the card connector, (i.e., jumper pins 5 and 14).

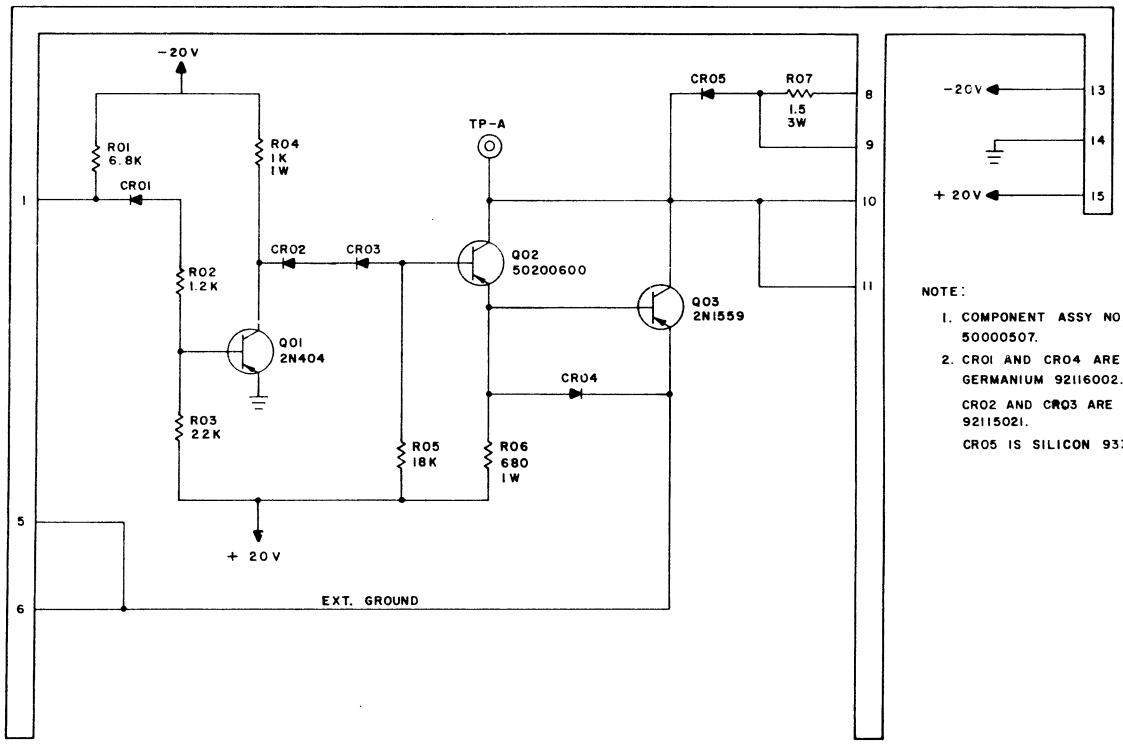
Referring to the schematic, the circuit operates as follows. Transistors Q02 and Q03 comprise a Darlington pair in a collector-loaded switch circuit. This pair is normally off with pin 1 at -3 volts. Transistor Q01 conducts when pin 1 is -3v; its collector is then at ground. This establishes +1.2 volts on the base of Q02 due to current flow from the +20 supply through R05 and silicon diodes CR02 and CR03 to ground. The emitter of Q02 and hence the base of Q03 is at +0.5 volts due to current from +20v through R06 and CR04 to ground. Both Q02 and Q03 are therefore off because of the reverse base voltages.

When the input goes to within -0.5 volts of ground, transistor Q01 goes off due to the divider action of R02, R03, and CR01, i.e., the base becomes positive. With Q01 collector unclamped, base current begins to flow in Q02 and Q03 from ground to the -20v supply by way of the collector load resistor R04. This turns on the Darlington circuit and lets load current flow.

In the on state and with a 15-ampere load, the collector to emitter voltage of Q03 is about 1.2 volts. With a 12 percent duty cycle, the average power dissipated in Q03 is about 2 watts. In free air (i.e., natural convection) at room temperature of 80°F, this dissipation causes Q03 to attain 175°F case temperature. With this high temperature on the card, it is suggested that the card be located in moving air and away from any temperature sensitive circuits.

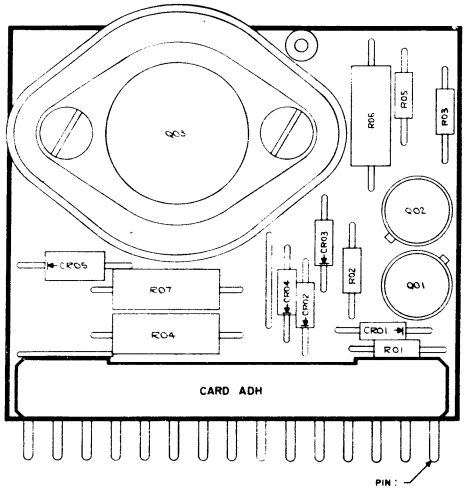
SYMBOL





NOTE:

1. COMPONENT ASSY NO 50000507.
2. CR01 AND CR04 ARE GERMANIUM 92116002.
   CR02 AND CR03 ARE SILICON 92115021.
   CR05 IS SILICON 93302026.



OUTPUT DRIVER
AEB

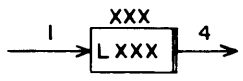
This output driver is used to operate on a common line with other equipment having similar output drivers attached to the same common line. The driver meets the common line requirement that it disconnect itself from signals on the common line whether power is on or off. This power off requirement is satisfied only if a positive voltage of 5 volts or more remains on pin 15. For these particular circuits the internal machine plus 20v is "ORed" with a plus 15v bus from the controller.

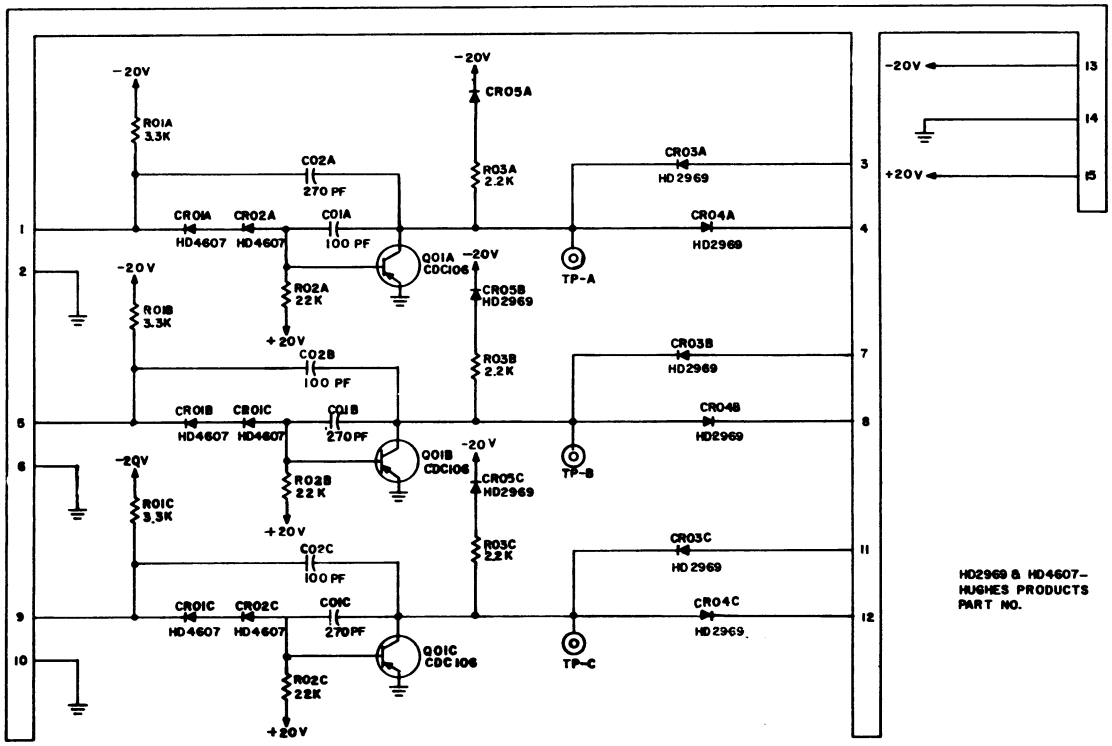
The circuit is designed around the type and length of interconnecting cable (100 ft. max) to provide optimum rise (0.35 to 1.0 use) and fall time (0.30 to 0.65 usec).

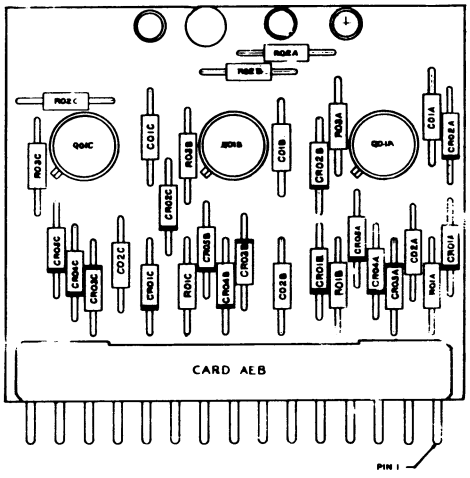
The circuit is a switching type inverter with certain variations. R01 reflects twice the usual load to the previous circuit. CR01 and CR02 are forward biased silicon diodes to improve the efficiency of the base divider of Q01. Capacitors C01 and C02 provide the proper combination of feedback to achieve the desired rise and fall times. Diode CR03 is connected to a minus 8-volt clamp to obtain the desired negative excursion of 8 volts. Diode CR04 prevents loading of this circuit in a negative direction when another signal is on the common line. Diode CR05 prevents loading of this circuit in a positive direction when another signal is on the common line.

A total of 85 ma output current is available for the receiver load, for charging the line capacity, and for driving small shunt leakages in parallel drivers on the same common line.

SYMBOL




-20V
R01A 3.3K
C02A 270 PF
CR01A HD4607
CR02A HD4607
C01A 100 PF
Q01A CDC106
R02A 22K
+20V
R01B 3.3K
C02B 100 PF
CR01B HD4607
CR01C HD4607
C01B 270PF
Q01B CDC106
R02B 22K
R01C 3.3K
C02C 100 PF
CR01C HD4607
CR02C HD4607
C01C 270PF
Q01C CDC106
R02C 22K
CR05A
R03A 2.2K
CR05B HD2969
R03B 2.2K
CR05C HD2969
R03C 2.2K
CR03A HD2969
CR04A HD2969
TP-A
CR03B HD2969
CR04B HD2969
TP-B
CR03C HD2969
CR04C HD2969
TP-C
HD2969 & HD4607- HUGHES PRODUCTS PART NO.


CARD AEB
PIN 1

MULTIPLE TIME DELAY
AFA, AFB

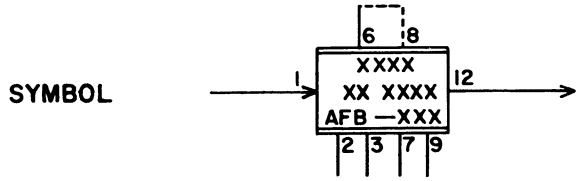
The multiple time delay card is used to delay the positive transition of an input (logic level) signal an amount of time determined by the RC time constant in the circuit. The resistance portion of the time constant includes a linear variable resistor which can be preset to give a particular delay time. More than one preset variable may be used to control the delay time of the circuit, but only one should be connected at a time. An electronic switch can be used to switch the proper resistor into the circuit (enable amplifier, type AG-series).

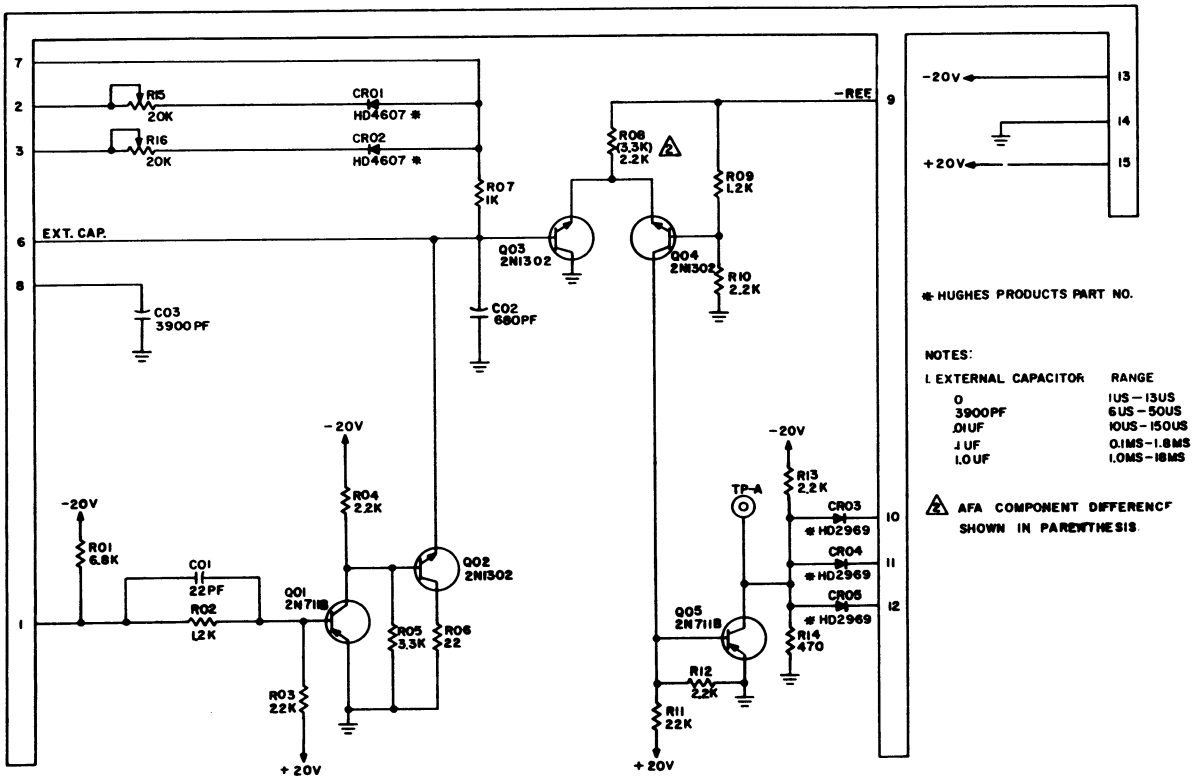
The delay circuit is armed by having a "1" input on pin 1 for 0.5 usec or more for a total delay capacitance of 5000 pf. The delay time accuracy is within $\pm$2 percent over a temperature range of 0° to 50°C. For 5000 pf delay capacitance, the delay from an input "1" to an output "1" does not exceed 0.1 usec.

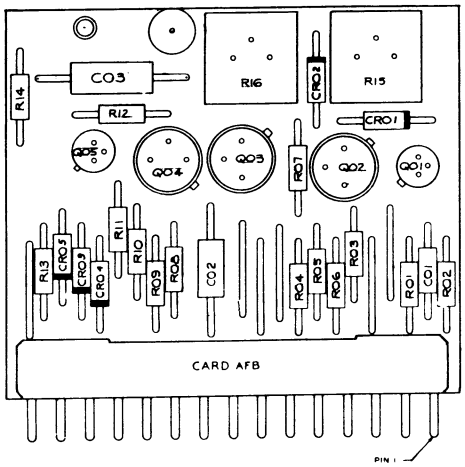
A signal on the input (pin 1) switching from a logical "1" to a "0" causes Q01 to turn off. Its collector goes to about -12v allowing emitter follower Q02 to cease conducting. Capacitor C02 (and the external capacitor if connected) starts charging through resistor R07, diode CR01, and variable resistor R15 to a negative reference voltage (pin 2). A small amount of charging current flows through transistor Q03. At the predetermined delay time, the voltage at capacitor C02 reaches the same voltage (-10v) that appears at the junction of resistors R09 and R10. The voltage supplied to resistor R09 is from the same negative reference as that supplied to R15. The differential amplifier, Q03 and Q04, switches state so that Q03 is now nonconducting and Q04 is conducting. This causes the base of transistor Q05 to go negative and start conducting, thus switching the output from "1" to "0". Similar operation is achieved using variable resistor R16 (pin 3) in the charging circuit and grounding R15 (pin 2). The diode connected to the grounded resistor serves to isolate the resistance from the timing circuit being used during the delay period.

Recovery of the circuit is accomplished by returning the input to a "1". Transistor Q01 turns on, thus grounding (-0.2v) the base of Q02. The emitter of Q02 follows, discharging capacitor C02 (and ex-

ternal capacitor) through Q02 and resistor R06. Resistor R06 limits the current thus protecting transistor Q02 from burnout. Differential amplifier, Q03 and Q04, returns to its original state with Q03 on and Q04 off. Resistor R11 reverses the base current to transistor Q05 allowing the output to return to a "1".







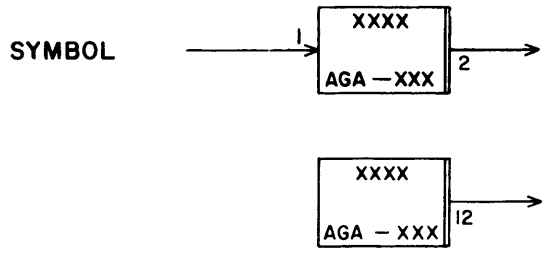
ENABLE AMPLIFIER
AGA

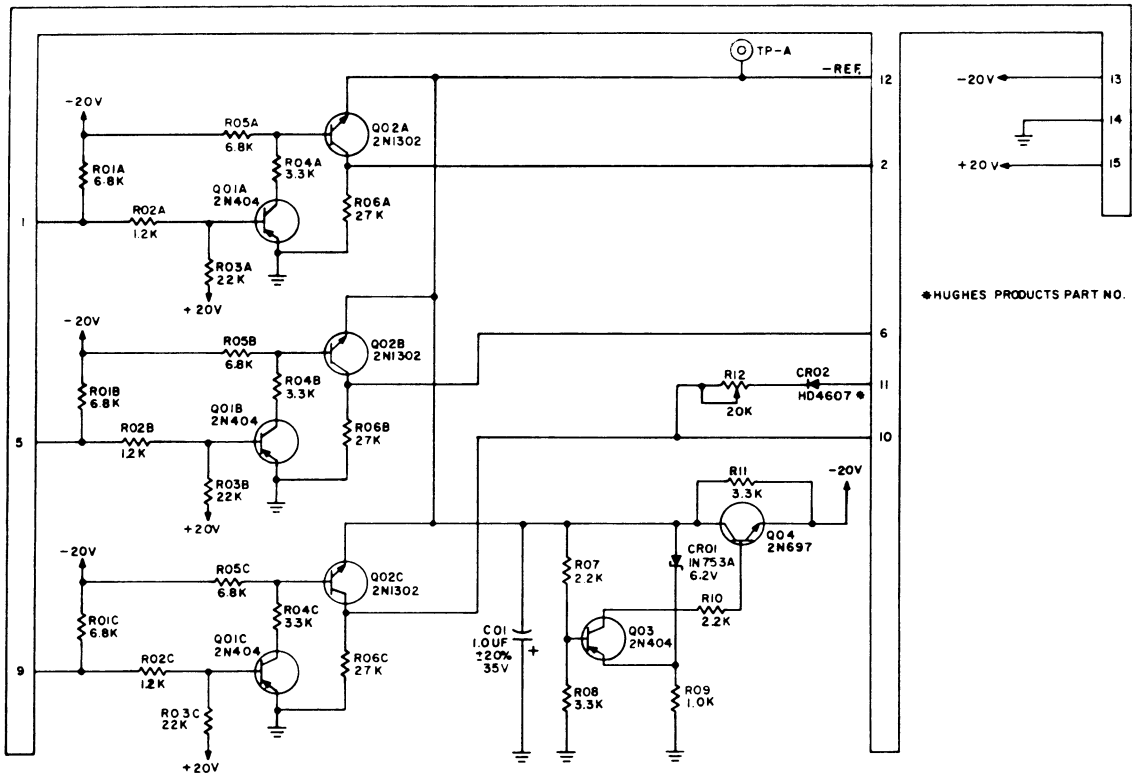
The enable amplifier card is used to select the proper variable resistor and provide a reference voltage for the time delay circuit (AF-series). There are three switching circuits per card.

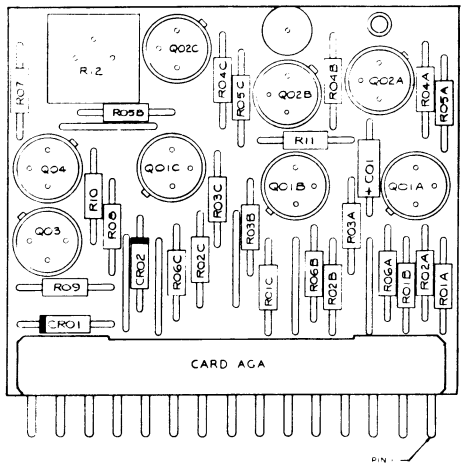
A logical "0" applied to the input pin (three identical circuits) causes transistor Q01 to turn off, allowing its collector voltage (through R04 and R05) to go more negative than the reference voltage at the emitter of Q02. Thus, Q02 is turned off allowing its collector voltage (output) to be at ground potential.

A logical "1" applied to the input pin causes transistor Q01 to turn on, grounding its collector (-0.2v) and turning on Q02 by providing base current through R04. The collector (output) of Q02 then goes to the reference voltage (about -15v). Thus, an external circuit element may be switched to the reference voltage when a "1" is applied to the enable amplifier and returned to ground when a "0" is applied.

The reference voltage section supplies a regulated and filtered current at -15v. This voltage is supplied to both the variable resistor and the differential amplifier on the time delay card (AF-series). The voltage is regulated in the following manner. Resistor R11 supplies starting current to the bridge composed of R07, R08, R09, and CR01. Transistor Q03 senses any voltage difference between the two legs of the bridge and changes the current to the base of transistor Q04 in proportion to the error in voltage. This allows Q04 to supply more or less current to the bridge and load such that the voltage returns to the normal value. Voltage regulation is in the order of $\pm$ 2% for load current up to 100 ma (instantaneous).




TP-A
-REF.
12
-20V
13
14
+20V
15
2
6
11
10
1
5
9
-20V
R01A 6.8K
R02A 1.2K
R03A 22K
+20V
R04A 3.3K
R05A 6.8K
R06A 27K
Q01A 2N404
Q02A 2N1302
R01B 6.8K
R02B 1.2K
R03B 22K
R04B 3.3K
R05B 6.8K
R06B 27K
Q01B 2N404
Q02B 2N1302
R01C 6.8K
R02C 1.2K
R03C 22K
R04C 3.3K
R05C 6.8K
R06C 27K
Q01C 2N404
Q02C 2N1302
R12
20K
CR02
HD4607 *
R11
3.3K
Q04 2N697
CR01 IN753A 6.2V
R10 2.2K
R07 2.2K
C01 1.0UF ±20% 35V
Q03 2N404
R08 3.3K
R09 1.0K
*HUGHES PRODUCTS PART NO.


R12
Q02C
Q02B
Q02A
R11
Q04
Q01C
Q01B
Q01A
Q03
R09
CR01
CR02
CARD AGA
PIN 1

FLIP-FLOP DRIVER

AHA

The AHA flip-flop driver is a special circuit designed for economical shift registers used in large quantities in optical character reading equipment. Capacitor coupled inputs allow a single rank of flip-flops to be used in a shift register with shifting possible in both directions. An output excursion of -3/4v to -12v with 20 ma drive provided in both directions eliminates the need for an external buffer driver to operate a resistor matrix load. A 10v, 15 ma lamp in an external display may also be operated from a lamp driver output. The circuit also lends itself to operation as a toggle flip-flop.

Flip-flop operation is as follows. The bistable circuit is composed of transistors Q01A, C and Q02A, C. Q01A, C provide drive in the positive direction. Q02A, C provide drive in the negative direction. R04A, C provide direct coupling between the two basic inverters to maintain either of two stable states. Q03 acts as an emitter follower to operate a low wattage lamp such as the #344 (10v, 15 ma). The positive excursion of the output is determined by the saturation resistance of Q01A, C and CR06A, C. The negative excursion is determined by the voltage on pin 4 which limits the megative-going excursions at the base of Q02A, C. When the output is negative, the output current is limited by R07A, C in the collector of Q02A, C. CR06A, C provide turnoff voltage bias for Q02A, C respectively when Q01A, C are turned on.

Triggering of the flip-flop is as follows. Assume Q01C is conducting (Q02A conducting and Q02C and Q01A nonconducting). If pin 7 is driven within -1/4 to -1v of ground, then a positive-going excursion of about 10v on pin 3 would cause a positive pulse to be coupled through C01C and CR07C to the base of Q01C. This positive signal would overcome the negative voltage supplied by R04C and cause Q01C to turn off. In about 0.1 usec after Q01C turns off, Q01A will be turned on and have changed the flip-flop to its other stable state. Q01C could also have been turned off in a similar manner by having pin 8 near ground and applying a positive-going excursion to pin 5 through C02C and CR08C. When Q01A is on, it may be turned off to change the flip-flop state by a similar combination of signals on pins 1 and 3 or pins 2 and 5. Input signals on pins 1, 2, 7, and 8 should be equivalent in excursion to

the output of pins 6 and 12 of the AHA card.

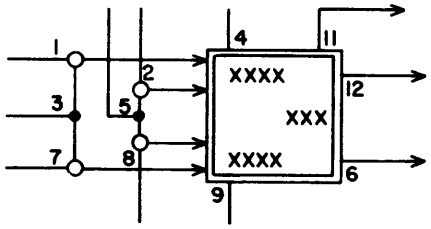
Thus, a positive-going pulse on pin 3 makes the flip-flop assume a state dependent on the levels present on pins 1 and 7 (assuming they are complimentary). Simililarly a positive-going pulse on pin 5 makes the flip-flop assume a state dependent on the levels present on pins 2 and 8. By interconnecting AHA's logically, they can be wired to shift up or down in a shift register by using one of two shift pulse lines from circuits such as the AIA which can interface with standard logic.

For clearing a counter or shift register, a clear line on pin 9 may be used. This operates from a signal from 0 to -1v and large numbers of AHA's may be cleared by one high current driver. Each AHA may require 7-25 ma (depends on load) to clear when in the set condition (lamp driver on) or 3 ma when in the clear position. The clear line should be biased between -12v and -20v when a clear is not desired.

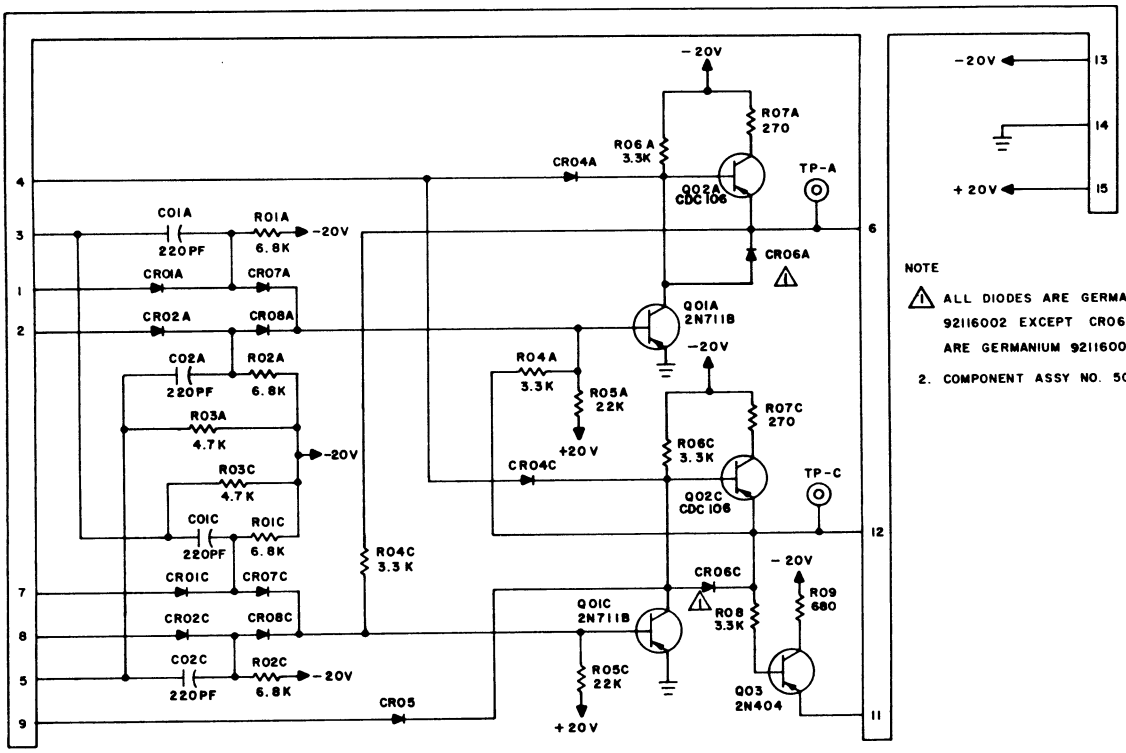
While the circuit is specifically designed for an excursion of -1/2v to -12v, clamping pin 4 to a different voltage will change the negative excursion proportionally. Lower voltages significantly reduce output drive in the positive direction and more negative voltages reduce it in the negative direction. The lamp driver circuit of Q03 is also significantly affected by such a change.

Shift pulses should have positive-going rise times of 0.150 usec or less with an excursion of 10 to 12 volts. Larger excursions with rise times this fast can cause faulty operation as can low amplitude slow rise time pulses.

SYMBOL



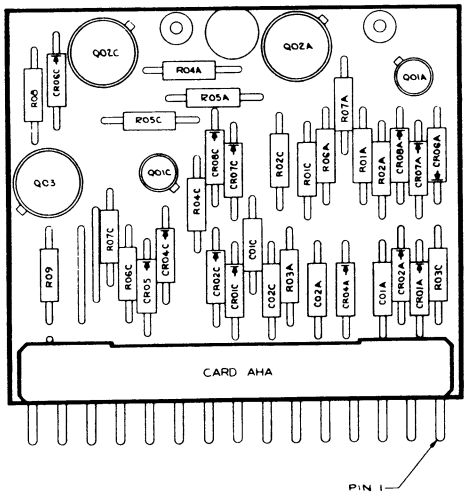
FLIP-FLOP DRIVER AHA



NOTE

⚠ ALL DIODES ARE GERMANIUM 92116002 EXCEPT CR06A & C ARE GERMANIUM 92116003

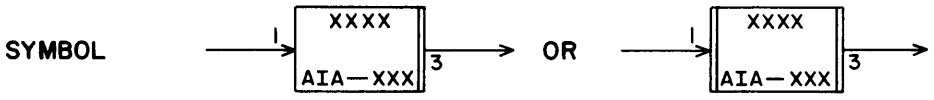
2. COMPONENT ASSY NO. 50010100.

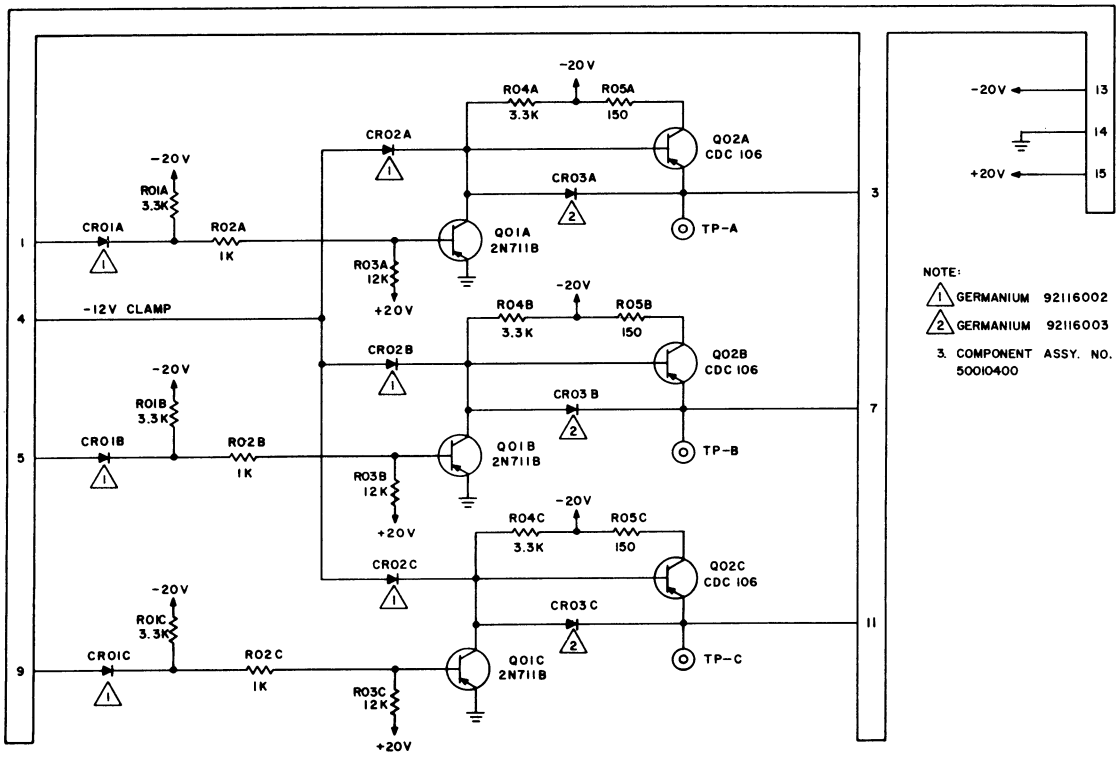


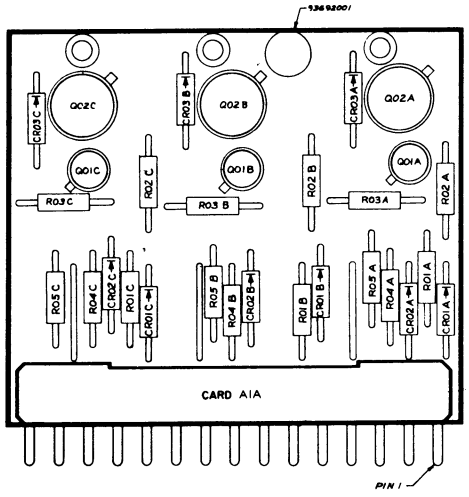
SHIFT DRIVER

AIA, AIB

The shift driver is designed to supply shift pulses and input signals for the AHA and similar circuit requirements. It provides output drive in both the positive and negative direction similar to a 3600 inverter. The output excursion is determined by the clamp voltage on pin 4 which is designed for -12v. Its input may operate from either standard 1604 logic levels or from logic levels that have greater negative excursions. However, if the negative excursion of the input is less than -5.0v, the output drive in the positive direction is reduced from a normal 70 ma to 25 ma at normal 1604 logic inputs. For positive input excursions ranging from 0 to -3/4v, the output drive in the negative direction is 45 ma maximum using a -12v clamp on pin 4. Output drive in the negative direction also reduces proportionably as the difference between -20v and the clamp voltage is reduced. Conversely, it increases if a lower clamp voltage is used. The negative voltage excursion for various loads is within 0.5v of the negative clamp voltage on pin 4. The positive excursion ranges from -0.5v at light load to a maximum of -1.0v at full load.




-20V
R04A
3.3K
R05A
150
CR02A
Q02A
CDC 106
CR03A
TP-A
R01A
3.3K
CR01A
R02A
1K
Q01A
2N711B
R03A
12K
+20V
-12V CLAMP
R04B
3.3K
R05B
150
CR02B
Q02B
CDC 106
CR03B
TP-B
R01B
3.3K
CR01B
R02B
1K
Q01B
2N711B
R03B
12K
+20V
R04C
3.3K
R05C
150
CR02C
Q02C
CDC 106
CR03C
TP-C
R01C
3.3K
CR01C
R02C
1K
Q01C
2N711B
R03C
12K
+20V
-20V
13
14
15
1
3
4
5
7
9
11
NOTE:
1 GERMANIUM 92116002
2 GERMANIUM 92116003
3. COMPONENT ASSY. NO. 50010400


CARD AIA
PIN 1

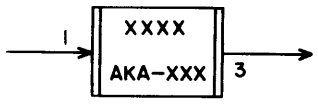
PHOTOCELL AMPLIFIER
AKA

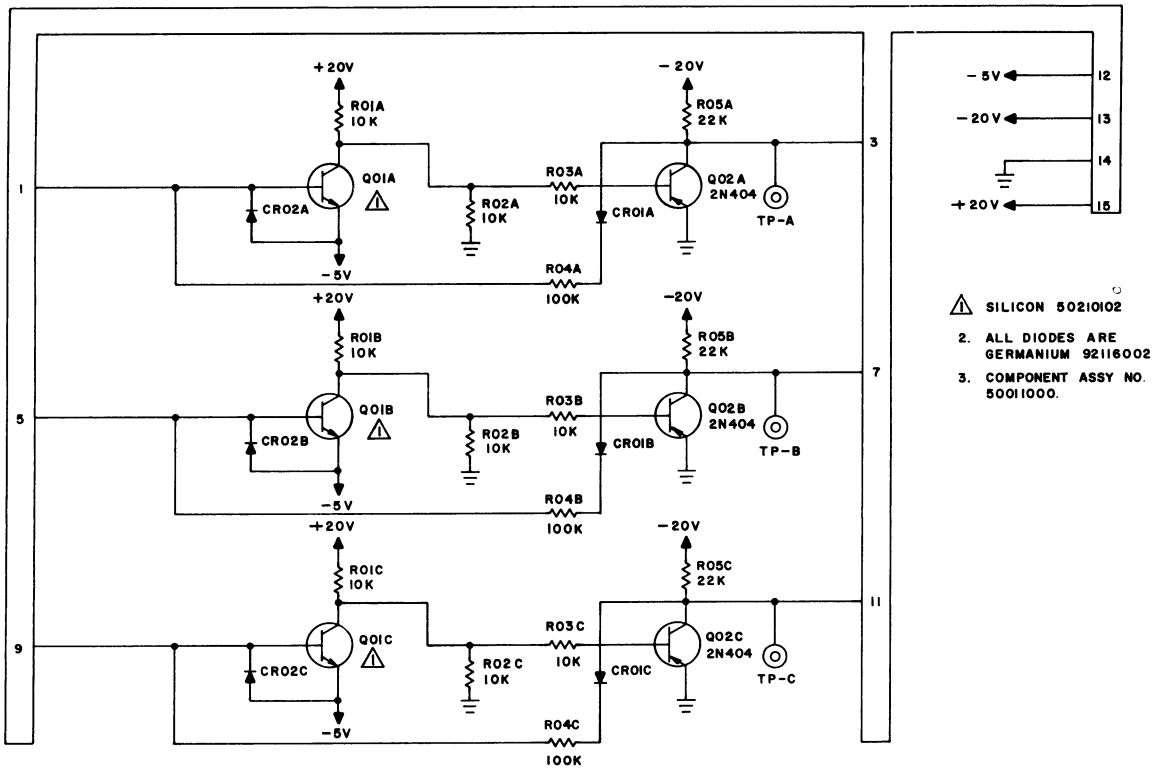
The AKA Photocell Amplifier is designed for use on the 350 and 370 Paper Tape Readers to digitize photo diode or photo transistor signals.

The output of the amplifier is normally terminated by the input of a standard "M" card, such as the 87. In the dark condition, external bias potentiometers supply current from a negative source to the input diode keeping both stages turned off, resulting in an output of -16v dc. In the illuminated state, the photocell provides positive current to the input base over-riding the bias current to turn on both stages. This results in an output of 0 to -1v dc.

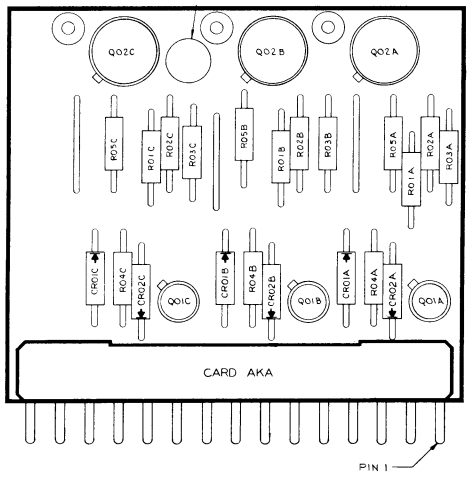
The circuit consists of two direct coupled inverting stages and a feedback circuit. The positive feedback through CR01 and R07 from output to input provides hysteresis or "snap action" to the turn-on and turn-off process. This insures the absence of Class A signals on the output during those times when the photocell is left in a partially illuminated state. Diode CR07 is intended to prevent a reverse feedback current from flowing when the photo diode is dark. Internal leakage in CR07 does allow a slight amount of positive feedback when connected to a "M" card, but this would be reduced even further if terminated by a standard inverter.

SYMBOL




+20V
R01A
10K
Q01A
CR02A
R02A
10K
R03A
10K
CR01A
-20V
R05A
22K
Q02A
2N404
TP-A
-5V
R04A
100K
+20V
R01B
10K
Q01B
CR02B
R02B
10K
R03B
10K
CR01B
-20V
R05B
22K
Q02B
2N404
TP-B
-5V
R04B
100K
+20V
R01C
10K
Q01C
CR02C
R02C
10K
R03C
10K
CR01C
-20V
R05C
22K
Q02C
2N404
TP-C
-5V
R04C
100K
1
3
5
7
9
11
-5V
12
-20V
13
14
+20V
15
1 SILICON 50210102
2. ALL DIODES ARE GERMANIUM 92116002
3. COMPONENT ASSY NO. 50011000.

AKA


Q02C
Q02B
Q02A
R05C
R01C
R02C
R03C
R05B
R01B
R02B
R03B
R05A
R01A
R02A
R03A
CR01C
R04C
CR02C
Q01C
CR01B
R04B
CR02B
Q01B
CR01A
R04A
CR02A
Q01A
CARD AKA
PIN 1

POWER SUPPLY
ALA

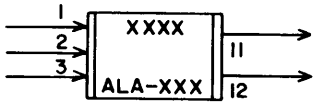
The ALA card contains a floating power supply. It is used with the FOA and FOB function generator cards in the disk file servo actuator.

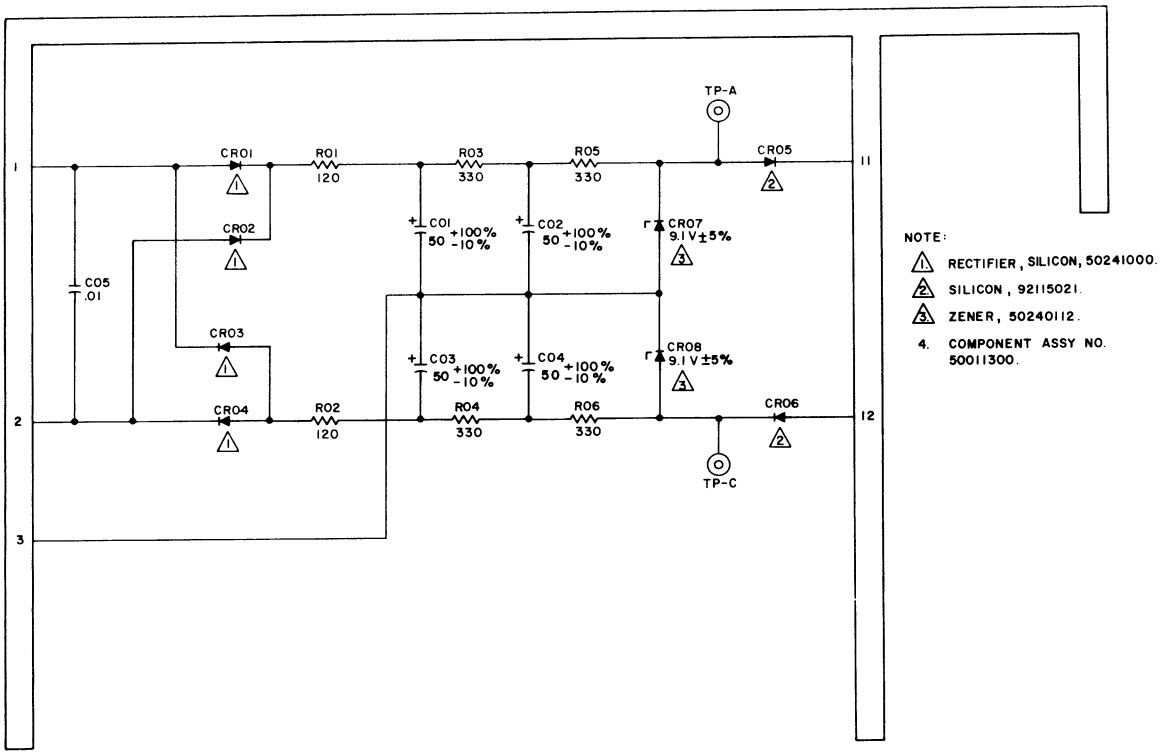
The circuit is supplied by an externally mounted 40v rms 60 cycle center tapped transformer. The transformer is connected to pins 1, 2, and 3. Pin 3 is the center tap and circuit common.

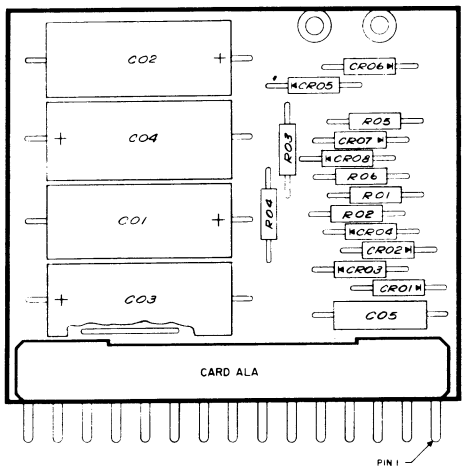
The circuit consists of two full wave rectifier circuits connected for plus and minus voltage, and the filter networks as shown on the schematic. Zener diodes CR07 and CR08 regulate the output voltages to 9.1v nominally. The maximum load is approximately 18 ma.

NOTE: This card requires two card slots.

SYMBOL




TP-A
CR01
R01
120
R03
330
R05
330
CR05
1
11
CR02
C01
50 +100% -10%
C02
50 +100% -10%
CR07
9.1V±5%
C05
.01
CR03
C03
50 +100% -10%
C04
50 +100% -10%
CR08
9.1V±5%
CR04
R02
120
R04
330
R06
330
CR06
2
12
TP-C
3
NOTE:
1. RECTIFIER, SILICON, 50241000.
2. SILICON, 92115021.
3. ZENER, 50240112.
4. COMPONENT ASSY NO. 50011300.


C02
C04
C01
C03
CR06
CR05
R05
CR07
CR08
R06
R01
R02
CR04
CR02
CR03
CR01
C05
R03
R04
CARD ALA
PIN 1

WRITE/ERASE DRIVER

AMF, AMG, AMH, AMI

CARD	USE	CURRENT AT EACH OUTPUT
AMF	852 write/erase	100 ma
AMG	853 write/erase	150 ma
AMH	807/808 write	125 ma
AMI	807/808 erase	300 ma

When transistor Q01 is on, it holds transistors Q02 and Q03 off. Zener diode CR01 is used for level translation. Diode CR03 keeps noise at the input from coupling through the capacitance of CR01 to the base of Q01. Diode CR04 is an anti-saturation diode. Resistor R06 develops a voltage drop proportional to the drive current which is used to check for proper operation (see cards ANB, ANC, AND, and AOA). Diodes CR05 and CR07 are part of the checking circuitry. Diode CR02 allows Q01 to provide turn-off current directly to Q03.

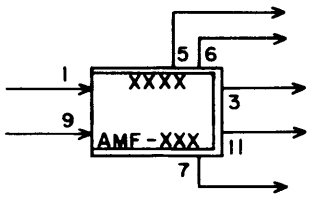
The value of capacitor C02 is 4.7 uf except in the AMG card (15 uf). This makes a longer time constant to permit correct operation of the error checking circuits in the 853 Disk Pack.

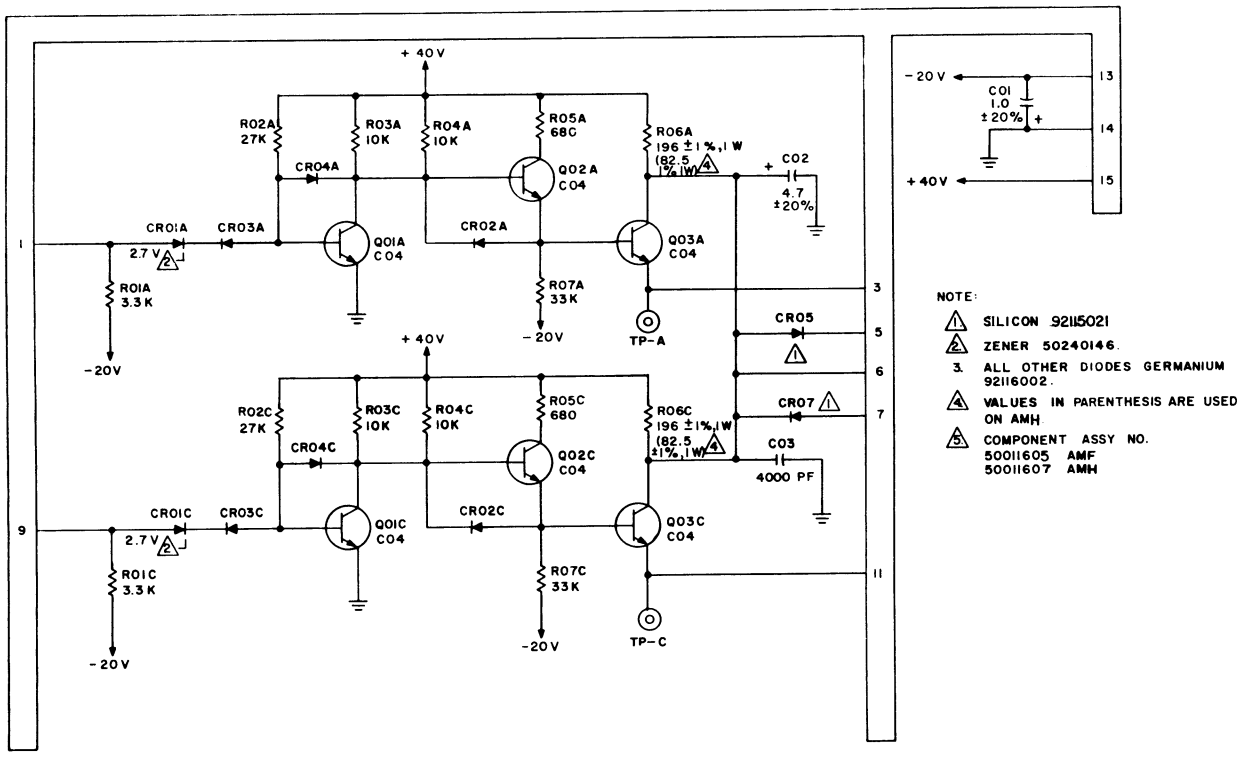
The AMI card is designed to operate on +20v rather than +40v, in order to reduce power dissipation. This was necessary because both circuits on the card are on at the same time.

With logical "1" (-3v) at the input, transistors Q02 and Q03 permit the current to flow from +40v (+20v, AMI card) toward ground. With logical "0" (ground) in, the output is open. The magnitude of the current is determined by an external resistor in series with the load.

CAUTION: These cards should not be removed from the chassis while +40v is applied.

SYMBOL

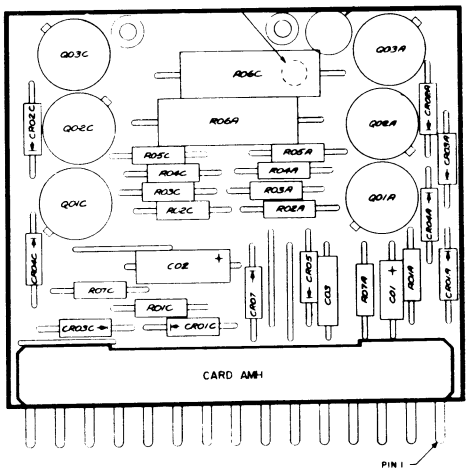


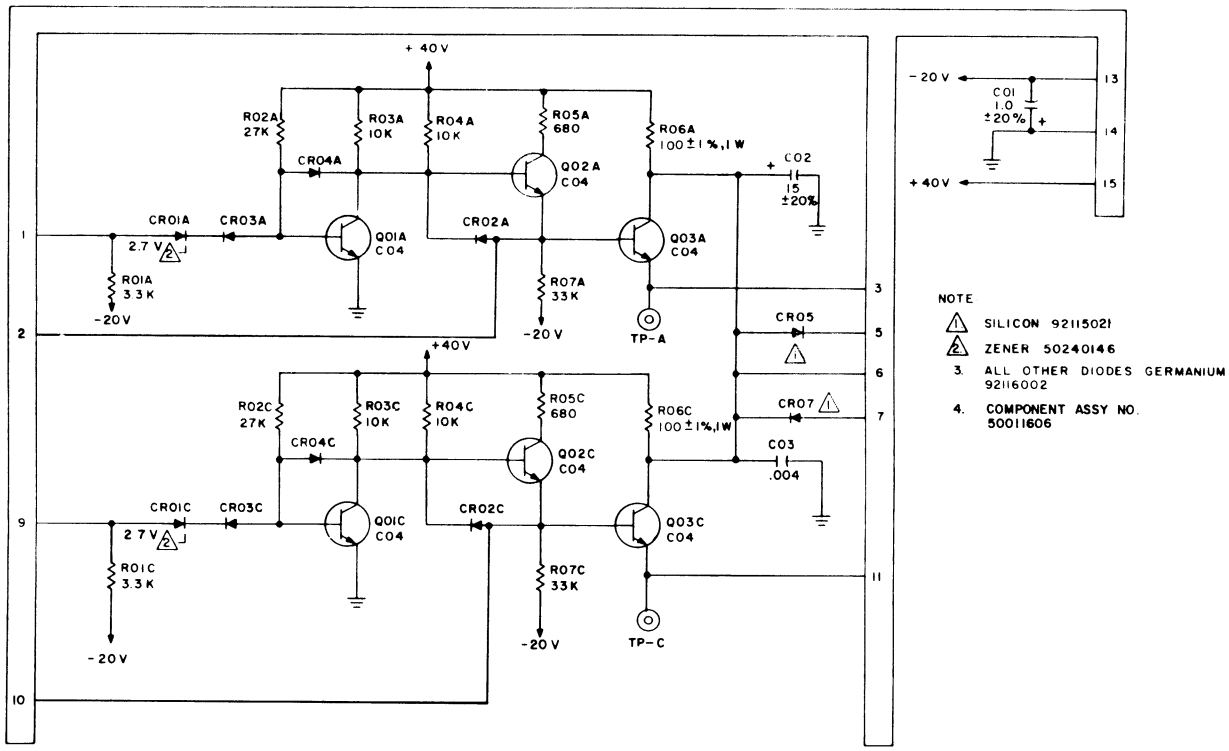


NOTE:

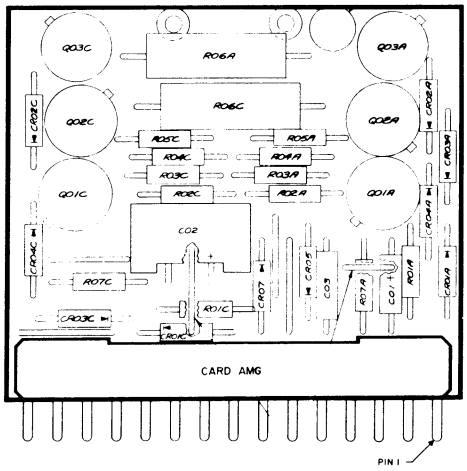
1. SILICON 92115021
2. ZENER 50240146.
3. ALL OTHER DIODES GERMANIUM 92116002.
4. VALUES IN PARENTHESIS ARE USED ON AMH.
5. COMPONENT ASSY NO.
   50011605 AMF
   50011607 AMH

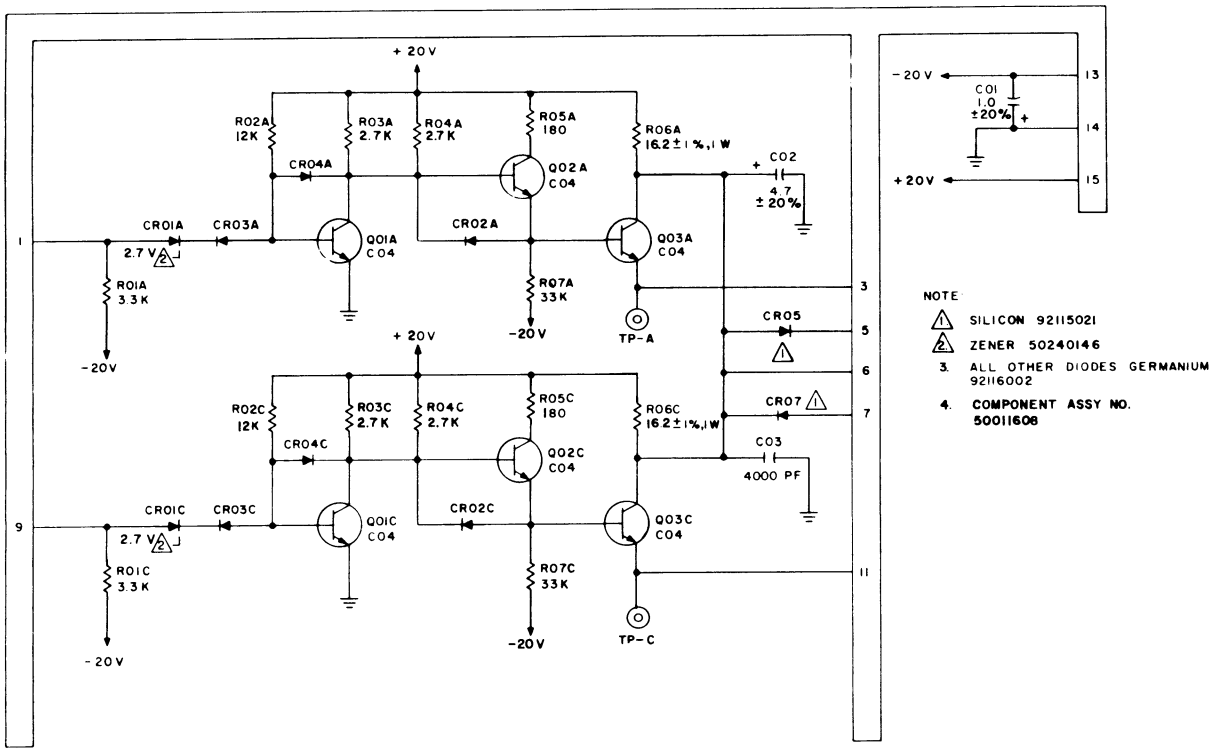
AMF, AMH



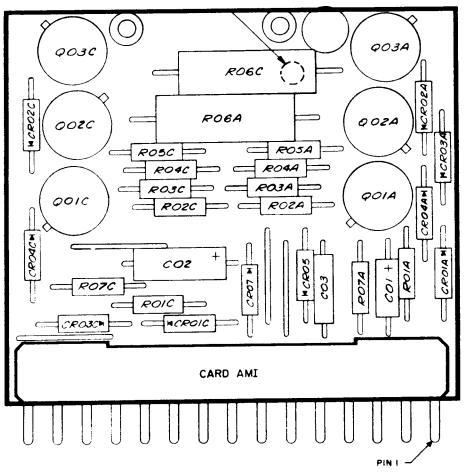

+ 40 V
R02A 27K
R03A 10K
R04A 10K
R05A 680
R06A 100 ± 1 %, 1 W
CR04A
Q02A C04
C02 .15 ±20%
CR01A
CR03A
CR02A
2.7 V
Q01A C04
Q03A C04
R01A 3.3K
-20 V
R07A 33K
-20 V
TP-A
CR05
+40V
R02C 27K
R03C 10K
R04C 10K
R05C 680
R06C 100 ± 1%, 1W
CR07
CR04C
Q02C C04
C03 .004
CR01C
CR03C
CR02C
2.7 V
Q01C C04
Q03C C04
R01C 3.3K
-20 V
R07C 33K
-20 V
TP-C
1
2
3
5
6
7
9
10
11
-20 V
C01 1.0 ±20%
+40V
13
14
15
NOTE
1. SILICON 92115021
2. ZENER 50240146
3. ALL OTHER DIODES GERMANIUM 92116002
4. COMPONENT ASSY NO. 50011606

AMG


Q03C
R06A
Q03A
R06C
Q02C
Q02A
R05C
R05A
R04C
R04A
R03C
R03A
R02C
R02A
Q01C
Q01A
C02
R07C
R01C
C03
R07A
R01A
CR07
CR03C
CARD AMG
PIN 1


+20V
R02A 12K
R03A 2.7K
R04A 2.7K
R05A 180
R06A 16.2±1%,1W
CR04A
Q02A C04
C02 4.7 ±20%
CR01A
CR03A
CR02A
2.7V
Q01A C04
Q03A C04
R01A 3.3K
R07A 33K
-20V
TP-A
CR05
CR07
R02C 12K
R03C 2.7K
R04C 2.7K
R05C 180
R06C 16.2±1%,1W
CR04C
Q02C C04
C03 4000 PF
CR01C
CR03C
CR02C
Q01C C04
Q03C C04
R01C 3.3K
R07C 33K
TP-C
-20V
C01 1.0 ±20%
+20V
NOTE
1. SILICON 92115021
2. ZENER 50240146
3. ALL OTHER DIODES GERMANIUM 92116002
4. COMPONENT ASSY NO. 50011608

AMI


Q03C
Q03A
R06C
R06A
Q02C
Q02A
R05C
R05A
R04C
R04A
R03C
R03A
R02C
R02A
Q01C
Q01A
C02
R07C
R01C
CR03C
CR01C
C03
R07A
R01A
CARD AMI
PIN 1

HEAD SELECT AND WRITE ERROR CHECKER
AND

This card is used in conjunction with write driver cards AMF and AMG, and head selector card IOB to check for proper operation.

(A) R05, CR07, CR09, and Q02 are used to determine if more than one head select circuit is on. Pins 5 and 11 of all the IOB cards are tied to pin 7. Each transistor Q03 on the IOB cards which is turned on (in saturation), draws approximately 4 ma through R05. When the voltage drop across R05 is greater than 1.6v ($\pm$0.15v), which is the sum of the voltage drops across CR07 and CR09 in series plus V_{be} of Q02, transistor Q02 will turn on. This will turn off transistor Q04. When Q04 goes off, an error has been detected. Resistor R05 is used so if one IOB card is on, Q02 will stay off. However, if two IOB cards are on, Q02 will turn on.

(B) R13, R14, CR08, and Q05 are used to determine if the current flowing out of each of a group of drivers is approximately the same. This will assure that none of them have shorts or opens. Pin 7 on both AMF or AMG cards are tied to pin 8. Pin 5 on both AMF or AMG cards are tied to pin 9. Since R06A and R06C are in parallel on the AMF or AMG card, the voltage across them is a function of the total current flowing through Q03A and Q03C. Capacitor C02 integrates this voltage. Therefore, it doesn't fluctuate with individual write cycles.

Assume that Q03A on driver number 1 becomes shorted. The current will then flow through Q03A all of the time, as well as part of the time through Q03C as dictated by input logic. The voltage at pin 6 of driver number 1 will then be more negative than the voltage at pin 6 of driver number 2. This will pull the voltage at pin 8 of the AND card more negative through CR07 on driver number 1. The voltage at the base of Q05 on card AND will stay one diode drop more negative than at pin 8. If the base of Q05 gets approximately 1.5v negative, with respect to pin 6 of driver number 2, Q05 will be turned on via CR05 on driver number 2. When Q05 turns on, Q04 turns off and an error is indicated. However, if the voltage at the collector of Q03 on driver number 1 is close enough to the voltage at collector Q03 on driver number 2, Q05 will not turn on. If these voltages are called V_1 and V_2, Q05 will turn on if the absolute

value of V_1 minus V_2 is greater than 1.77 volts. Transistor Q05 will not turn on if the absolute value of V_1 minus V_2 is less than 1.27 volts.

HEAD SELECT AND WRITE ERROR CHECKER
ANB

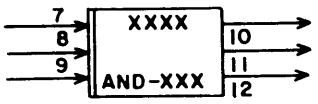
The (B) portion of the AND card description applies to card ANB. The circuits containing Q01 and CR14 are used in conjunction with card AOA to test head selects. If more than approximately 0.8 ma flows from a combination of AOA cards into pin 1, Q01 will turn off indicating an error. R15 and CR14 act as a reference voltage supply for the AOA cards.

ERASE ERROR CHECKER
ANC

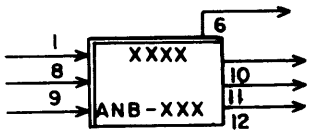
The ANC card is essentially the same as the (B) portion of the AND card description. The ANC card has been modified to test drivers that operate on +20v (AMI card) rather than +40v.

The outputs of cards ANB, ANC, and AND go to logical "1" (-3v) if an error has been detected. If the outputs are at logical "0" (ground), no error has been detected.

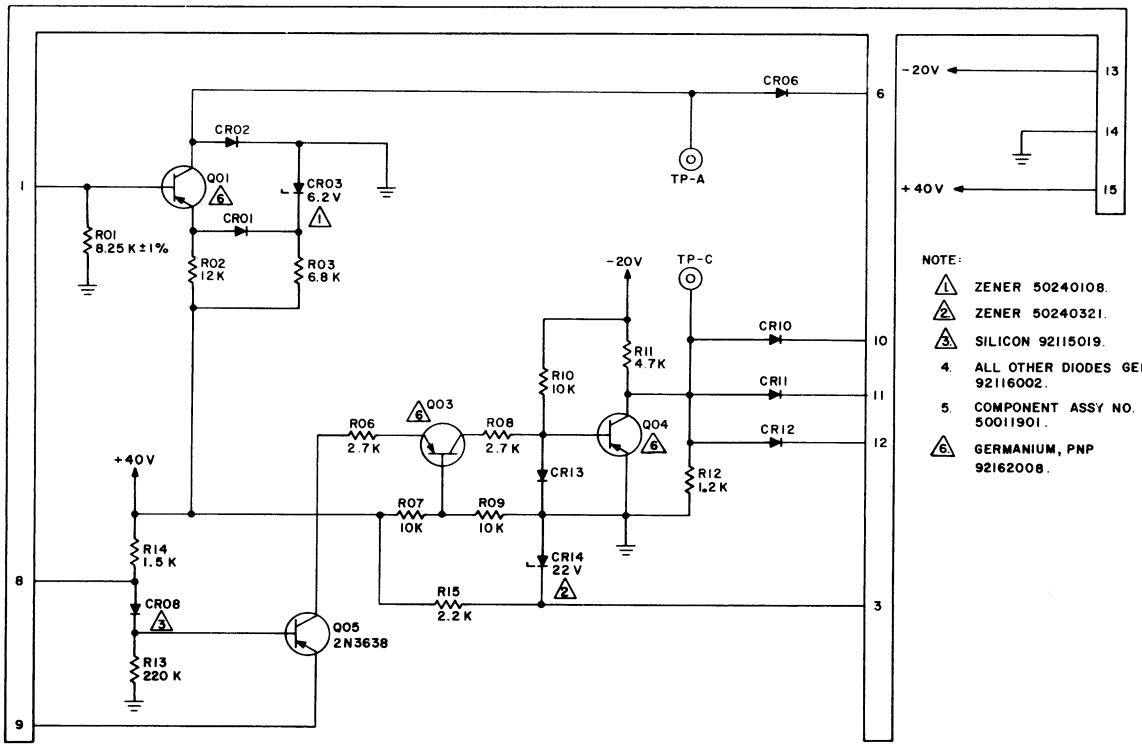
SYMBOL



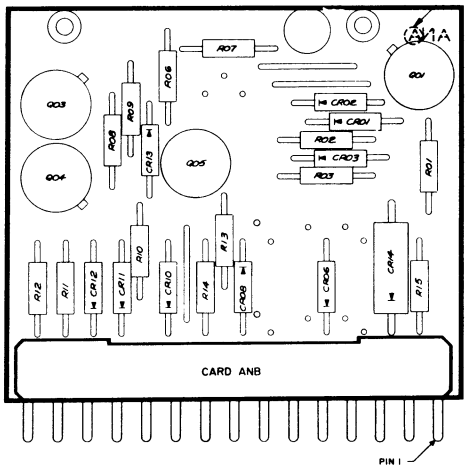
SYMBOL

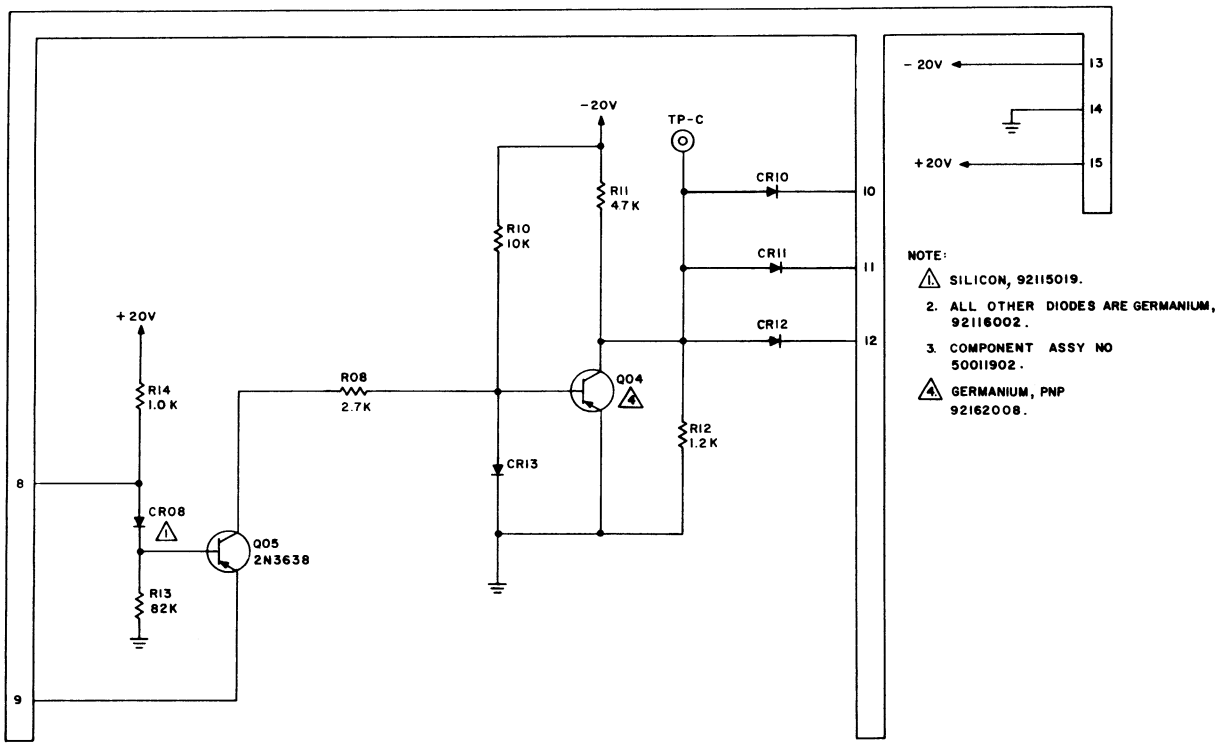


SYMBOL

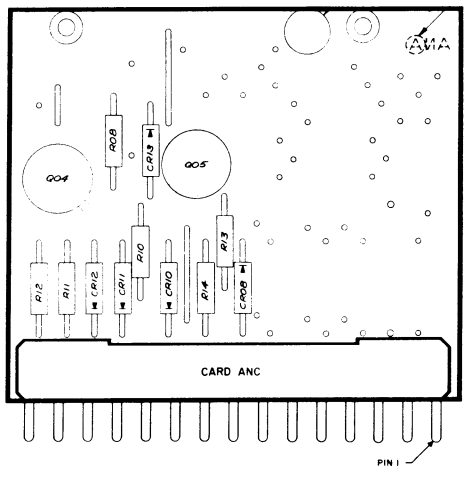

-20V
13
14
+40V
15
CR06
6
CR02
TP-A
1
Q01
6
CR03
6.2V
1
CR01
R01
8.25K ±1%
R02
12K
R03
6.8K
-20V
TP-C
CR10
10
R11
4.7K
R10
10K
CR11
11
Q03
6
R06
2.7K
R08
2.7K
Q04
6
CR12
12
CR13
R12
1.2K
+40V
R07
10K
R09
10K
R14
1.5K
CR14
22V
2
8
CR08
3
R15
2.2K
3
Q05
2N3638
R13
220K
9
NOTE:
1. ZENER 50240108.
2. ZENER 50240321.
3. SILICON 92115019.
4. ALL OTHER DIODES GERMANIUM 92116002.
5. COMPONENT ASSY NO. 50011901.
6. GERMANIUM, PNP 92162008.

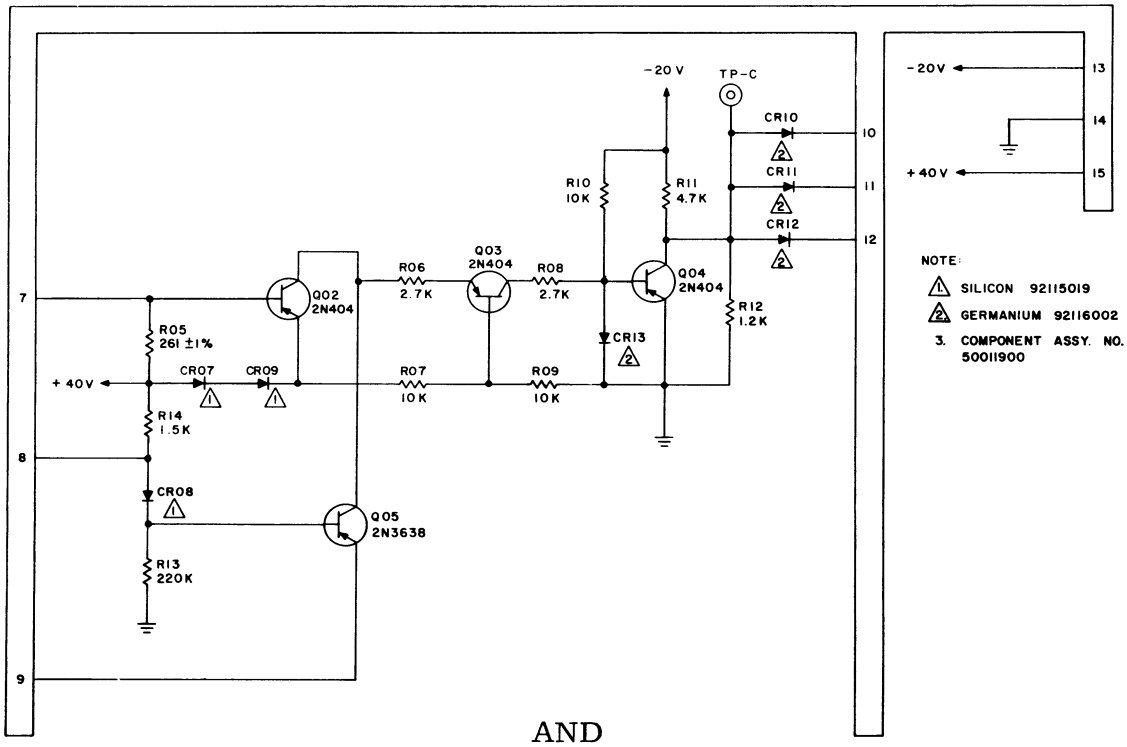
ANB


CARD ANB
PIN 1

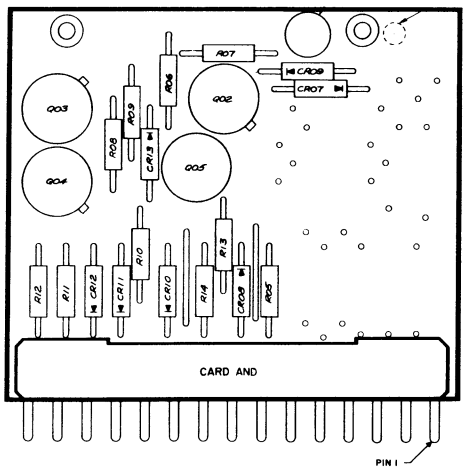

-20V
TP-C
R11
47K
R10
10K
CR10
CR11
CR12
10
11
12
13
14
15
-20V
+20V
NOTE:
1. SILICON, 92115019.
2. ALL OTHER DIODES ARE GERMANIUM, 92116002.
3. COMPONENT ASSY NO 50011902.
4. GERMANIUM, PNP 92162008.
+20V
R14
1.0K
R08
2.7K
Q04
4
R12
1.2K
CR13
8
CR08
1
Q05
2N3638
R13
82K
9

ANC


R08
CR13
Q04
Q05
R10
R13
R12
R11
CR12
CR11
CR10
R14
CR08
CARD ANC
PIN 1


-20V
TP-C
CR10
CR11
CR12
R10
10K
R11
4.7K
Q03
2N404
R06
2.7K
R08
2.7K
Q04
2N404
R12
1.2K
CR13
Q02
2N404
R05
261 ±1%
CR07
CR09
R07
10K
R09
10K
+40V
R14
1.5K
CR08
Q05
2N3638
R13
220K
7
8
9
10
11
12
13
14
15
-20V
+40V
NOTE:
1. SILICON 92115019
2. GERMANIUM 92116002
3. COMPONENT ASSY. NO. 50011900

AND

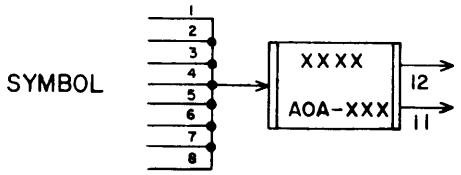

CARD AND
PIN 1

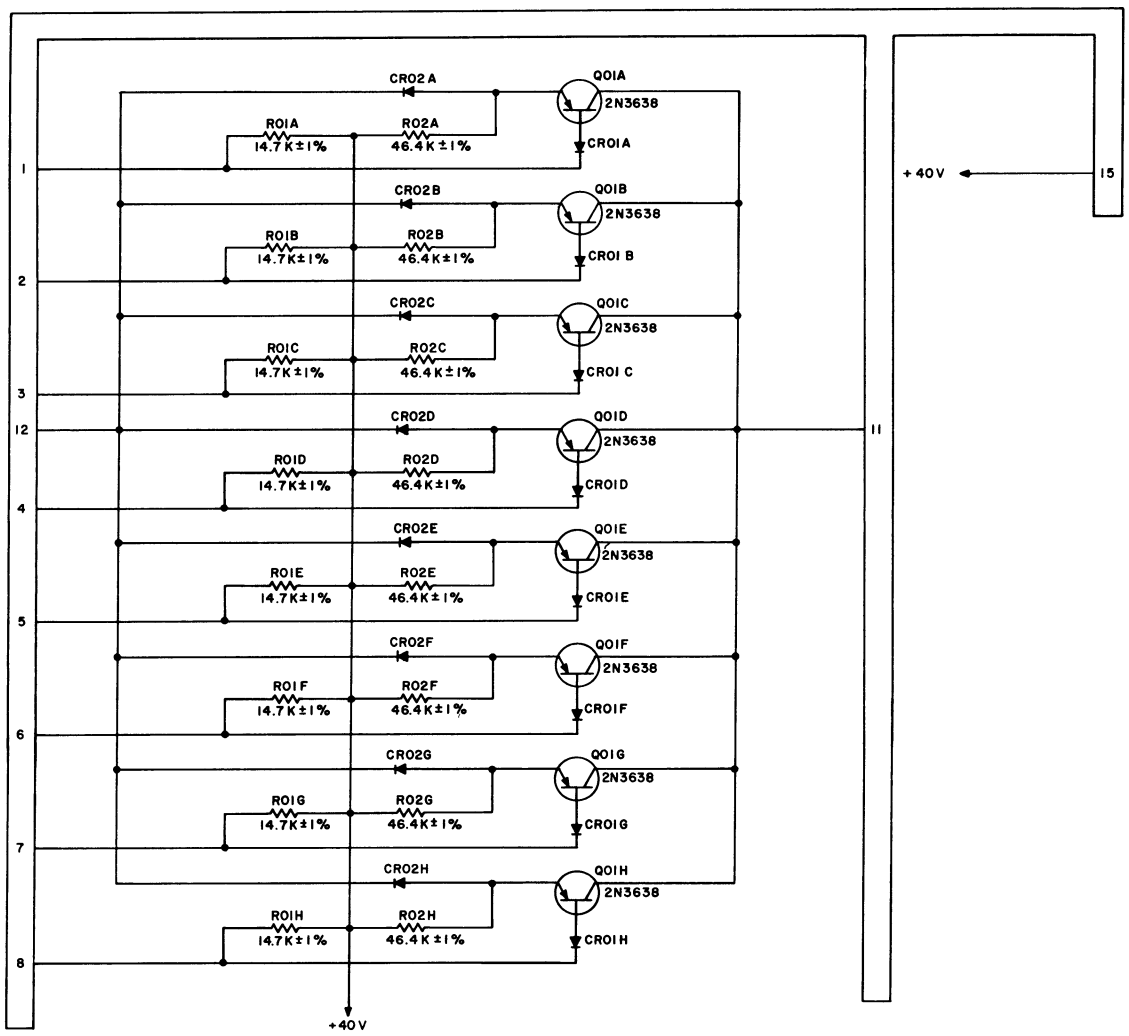
EXCLUSIVE OR CIRCUIT
AOA

The AOA card delivers +0.4 ma to an ANB card for each head select circuit (turned on) it is monitoring.

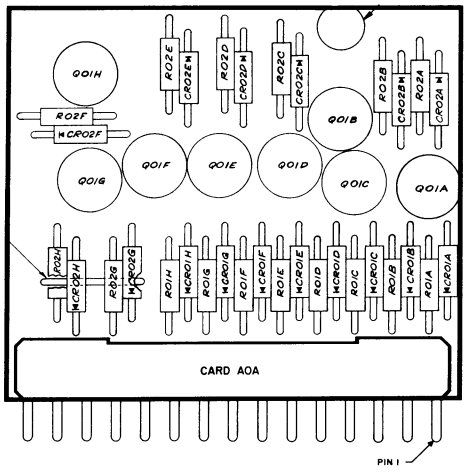
Pins 5 and 11 on the IOB cards are tied to pins 1 through 8, with only one Head Select circuit at each input pin. A total of eight Head Select circuits are tested by each AOA card, in conjunction with an ANB card. If the Head Select circuit tied to pin 1 is turned on, Q01A will be turned on, and it will allow approximately 0.4 ma to flow out pin 11 to the ANB card. The voltage at pin 1 is compared to the voltage at pin 12. If the Head Select circuit tied to any other pin of pins 1 through 8 is on, the associated transistor on the AOA card will also turn on, in the same manner at Q01A. This transistor will also allow approximately 0.4 ma to flow out pin 11 to the ANB card.

Four AOA cards are used in conjunction with one ANB card. Pin 11 on the AOA card goes to pin 1 on the ANB card; pin 12 on the AOA card goes to pin 3 on the ANB card. Thus, 32 Head Select circuits are being checked by one ANB circuit. If more than one Q01 on the four AOA cards is on, there will be 0.8 ma (or more) entering the ANB card at pin 1.




CR02A
Q01A
2N3638
R01A
14.7K±1%
R02A
46.4K±1%
CR01A
CR02B
Q01B
2N3638
R01B
14.7K±1%
R02B
46.4K±1%
CR01B
CR02C
Q01C
2N3638
R01C
14.7K±1%
R02C
46.4K±1%
CR01C
CR02D
Q01D
2N3638
R01D
14.7K±1%
R02D
46.4K±1%
CR01D
CR02E
Q01E
2N3638
R01E
14.7K±1%
R02E
46.4K±1%
CR01E
CR02F
Q01F
2N3638
R01F
14.7K±1%
R02F
46.4K±1%
CR01F
CR02G
Q01G
2N3638
R01G
14.7K±1%
R02G
46.4K±1%
CR01G
CR02H
Q01H
2N3638
R01H
14.7K±1%
R02H
46.4K±1%
CR01H
+40V
+40V
1
2
3
12
4
5
6
7
8
11
15

AOA


Q01H
R02E
CR02EM
R02D
CR02DM
R02C
CR02CM
R02B
CR02BM
R02A
CR02AM
Q01B
R02F
MCR02F
Q01G
Q01F
Q01E
Q01D
Q01C
Q01A
R02H
MCR02H
R02G
MCR02G
R01H
MCR01H
R01G
MCR01G
R01F
MCR01F
R01E
MCR01E
R01D
MCR01D
R01C
MCR01C
R01B
MCR01B
R01A
MCR01A
CARD AOA
PIN 1

GATED AMPLIFIER
ATA, ATB

This circuit has a read gate and a linear preamplifier. The read gate is comprised of diodes CR01-CR10, and resistors R01-R04 and R20. Pins 1 and 4 go through an external diode on each side, pointing the same way as CR01-02 and then to the outer terminals of the read head. CR05 and CR06 are replaced by jumpers for use with disc paks.

If pins 5 and 6 are at +5V or more positive, the circuit amplifies a signal put in on pins 1 and 4 from a center-tapped, grounded read head. If pins 5 and 6 are near ground, signals at pins 1 and 4 are ignored.

Pins 5 and 6 are connected through a balancing potentiometer to an ISC card, which is used as the gate control. When the ISC input is at ground, the emitter follower output of the ISC is off, which is equivalent to having pins 5 and 6 floating. Under these conditions, whether the center-tap of the head is at +40v (unselected) or at ground (selected), diodes CR01-CR08 are not conducting, and thus represent a large impedance between the read head and the amplifier. Also, CR09 and CR10 are conducting through R03, R04, and R20, and represent a short circuit across the input to the amplifier for any signal that might leak through the other diodes. While writing is in progress, the outside terminals of the head will experience $\pm$ 20v excursions due to $L \frac{di}{dt}$. The gate portion of the circuit attenuates these voltages, so that resulting disturbances in the read chain are minimized.

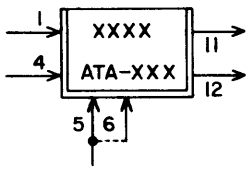
When the ISC turns on, current flows through CR01, CR02, and the two external diodes through the read head to ground via the Head Select. Current also flows through CR03-08 to R03, R04, and R20. Thus CR01-CR08 are foward biased and present a low dynamic impedance to the signal. When CR03-08 are on, CR09 and CR10 are turned off, and thus do not put a short circuit across the input to the amplifier.

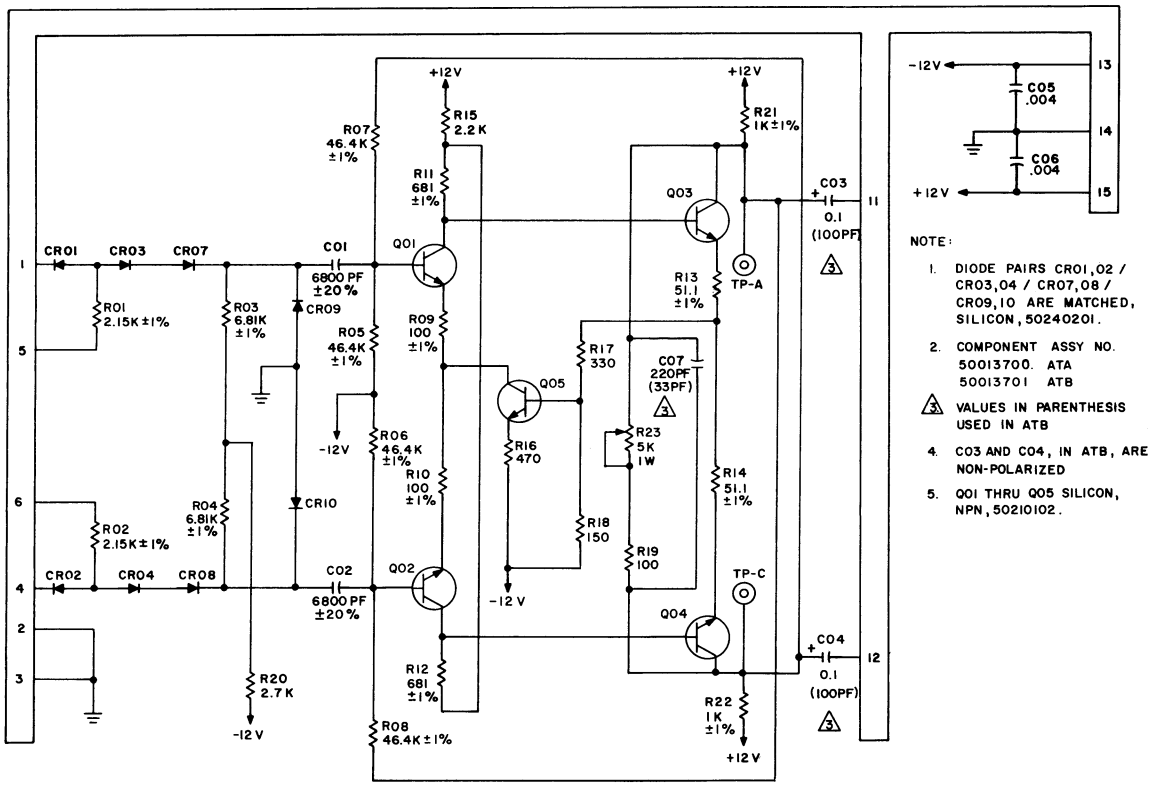
The amplifier is a two stage differential amplifier, with some dc feedback from output to input for stabilization through R07 and R08. C07 controls the high-frequency gain, and R23 controls the overall gain. +12v must be supplied at pin 15, and -12v must be supplied at pin 13. Bandpass is from 10Kc to 5Mc. This card is designed to drive EUA, EUC,

or a similar load of about 1K.

The ATB card is the same as the ATA, except that some component values are changed since the desired gain vs. frequency characteristics are different. Band pass is from 50 Kc to 5Mc.

SYMBOL

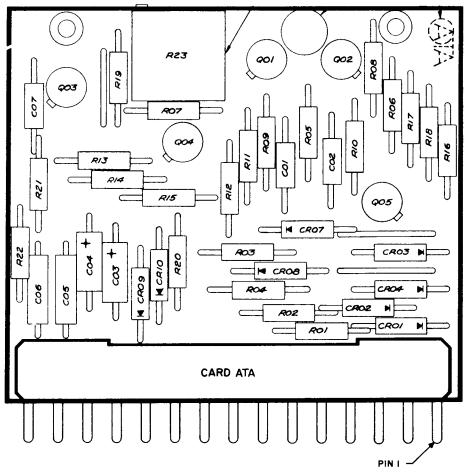




NOTE:

1. DIODE PAIRS CR01,02 / CR03,04 / CR07,08 / CR09,10 ARE MATCHED, SILICON, 50240201.
2. COMPONENT ASSY NO. 50013700. ATA 50013701 ATB
3. VALUES IN PARENTHESIS USED IN ATB
4. C03 AND C04, IN ATB, ARE NON-POLARIZED
5. Q01 THRU Q05 SILICON, NPN, 50210102.

ATA



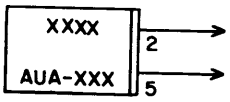
POWER SUPPLY REGULATOR
AUA

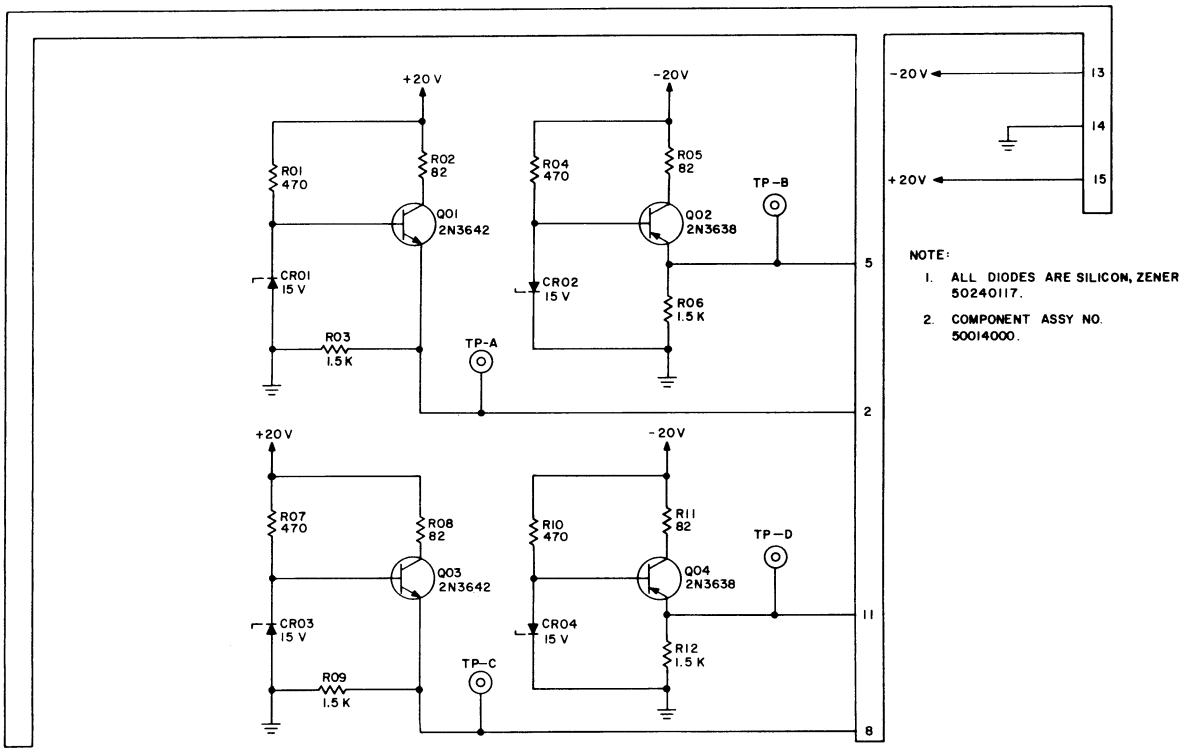
This card is used to supply regulated plus and minus 15v dc to an operational amplifier (such as the FSA card used in the servo actuator for the disk file). Each card contains two identical +15v stages and two identical -15v stages.

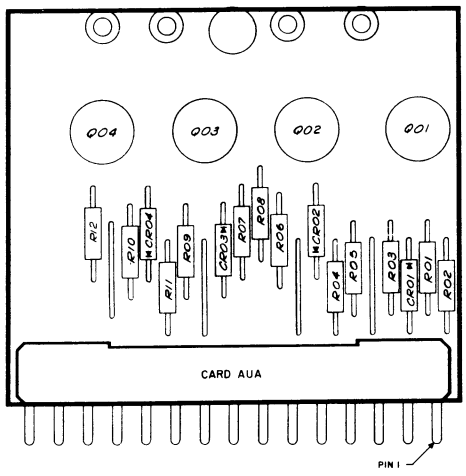
Each circuit is an emitter follower with a 15v zener diode from base to ground. The maximum load current permissible before the zener comes out of conduction, assuming 10 percent low power supply voltage, is 33 ma. This corresponds to an equivalent load resistance of 455 ohms.

The output impedance is approximately the r_e of the transistor in the Tee parameters. This is also equal to $\frac{26}{I_e}$. For these circuits, I_e is approximately 10 ma, resulting in an output impedance of 2.6 ohms.

SYMBOL




+20 V
-20V
R01
470
R02
82
Q01
2N3642
CR01
15 V
R03
1.5K
TP-A
R04
470
R05
82
TP-B
Q02
2N3638
CR02
15 V
R06
1.5 K
5
2
+20 V
-20V
R07
470
R08
82
Q03
2N3642
CR03
15 V
R09
1.5 K
TP-C
R10
470
R11
82
TP-D
Q04
2N3638
CR04
15 V
R12
1.5 K
11
8
-20V
13
14
+20V
15
NOTE:
1. ALL DIODES ARE SILICON, ZENER 50240117.
2. COMPONENT ASSY NO. 50014000.

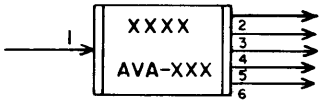

Q04
Q03
Q02
Q01
R12
R10
CR04
R09
R11
CR03
R07
R08
R06
CR02
R05
R04
R03
CR01
R01
R02
CARD AUA
PIN 1

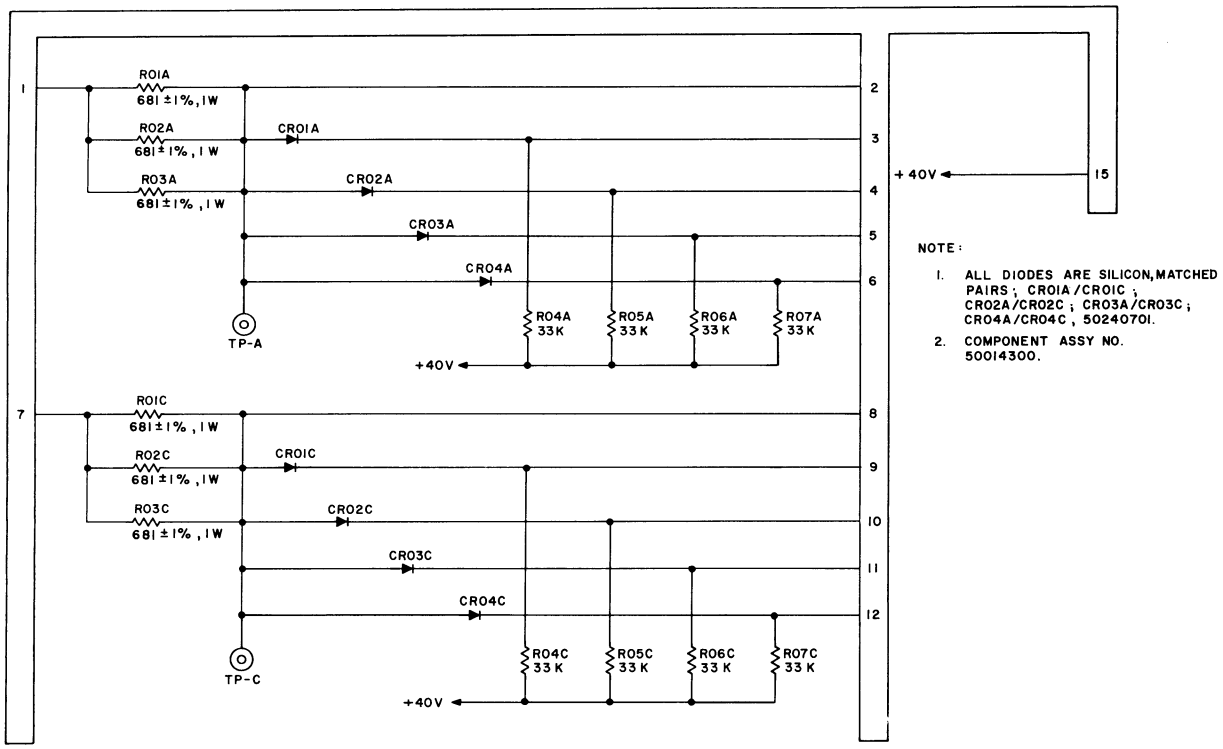
WRITE RESISTOR DIODE CARD
AVA

The AVA card is connected between the erase/write drivers and the read/write heads. The read amplifier also connects into this card in order to connect to the head.

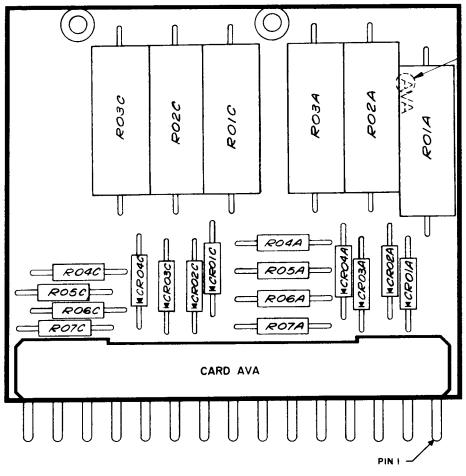
There are two identical sections per card. Each contains one resistor and several diodes. The resistor determines the magnitude of the erase/write current, and the diodes are used for isolation.

SYMBOL




1
ROIA
681 ±1%, 1W
RO2A
681 ±1%, 1W
RO3A
681 ±1%, 1W
CRO1A
CRO2A
CRO3A
CRO4A
R04A 33K
R05A 33K
R06A 33K
R07A 33K
TP-A
+40V
2
3
4
5
6
+40V
15
NOTE:
1. ALL DIODES ARE SILICON, MATCHED PAIRS; CRO1A/CRO1C; CRO2A/CRO2C; CRO3A/CRO3C; CRO4A/CRO4C, 5024070I.
2. COMPONENT ASSY NO. 50014300.
7
ROIC
681 ±1%, 1W
RO2C
681 ±1%, 1W
RO3C
681 ±1%, 1W
CRO1C
CRO2C
CRO3C
CRO4C
R04C 33K
R05C 33K
R06C 33K
R07C 33K
TP-C
+40V
8
9
10
11
12

AVA


RO3C
RO2C
RO1C
RO3A
RO2A
RO1A
AVA
RO4C
RO5C
RO6C
RO7C
CRO4C
CRO3C
CRO2C
CRO1C
RO4A
RO5A
RO6A
RO7A
CRO4A
CRO3A
CRO2A
CRO1A
CARD AVA
PIN 1

VOLTAGE CHECKER

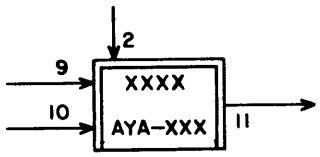
AYA

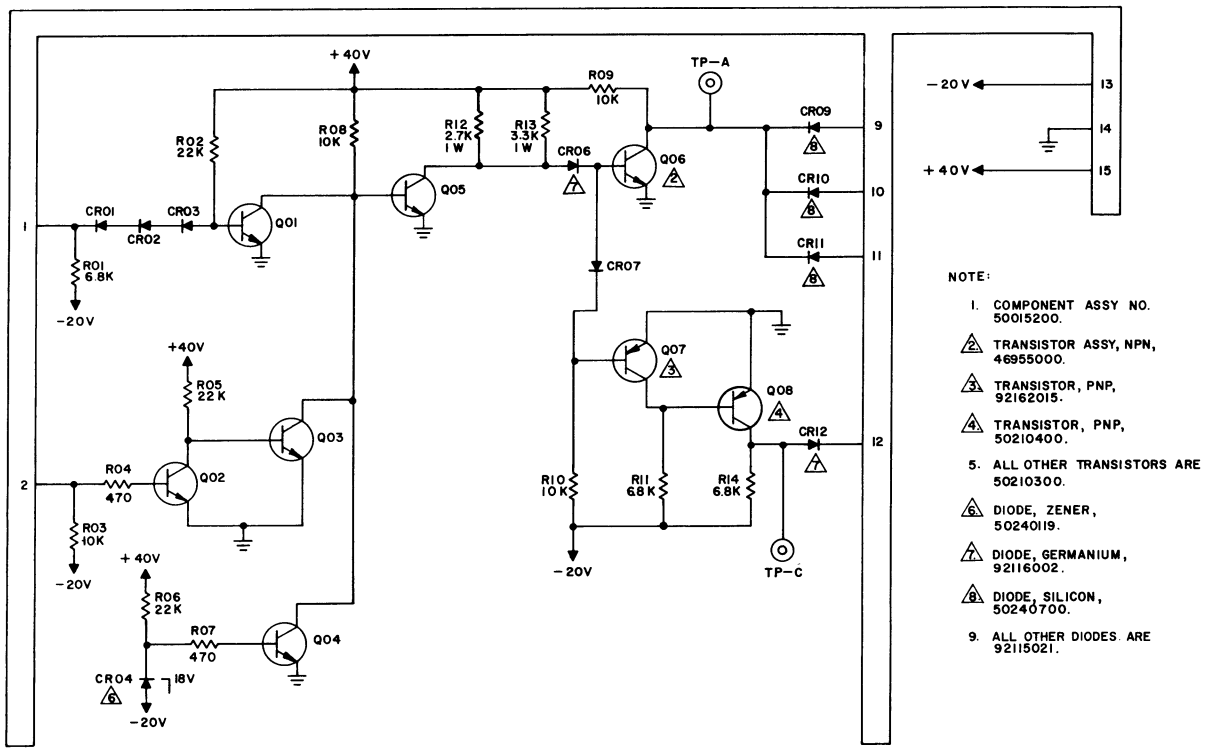
The AYA card keeps write and erase current from reaching write and erase heads if one or more of the following conditions is true: 1) If +20V drops below +17.6V nominal. 2) If -20V gets closer to ground than -17.2V nominal. 3) If an external logic signal goes to logic zero (-0.5V). A logic output goes to logic zero.

If pin 1 goes to logic zero, Q01 turns on. This turns off Q05, which turns Q06 on, and forces TP C toward -20V. Q06 absorbs up to 500 ma. CR09, 10, 11 are to isolate the AYA card and the write and erase heads from each other when the AYA card is off.

Pin 2 senses the state of the +20V supply. If it gets to +17.6 $\pm$ 0.9V, Q02 turns off and Q03 turns on. This has the same effect as Q01 turning on. Q04 turns on if -20V supply gets to -17.2V $\pm$ 0.9V. This has the same effect as Q01 turning on. If more than one of these three sensing circuits respond at one time, the effect is the same as if only one was on.

SYMBOL

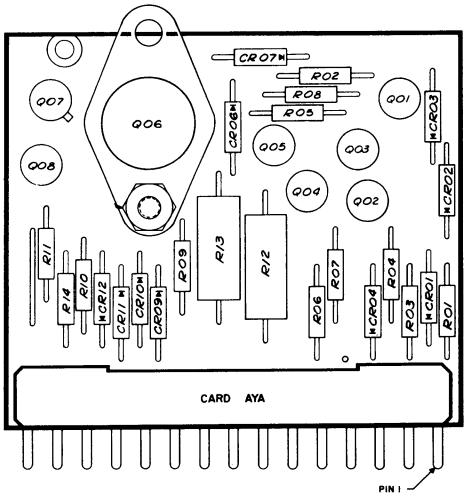




NOTE:

1. COMPONENT ASSY NO. 50015200.
2. TRANSISTOR ASSY, NPN, 46955000.
3. TRANSISTOR, PNP, 92162015.
4. TRANSISTOR, PNP, 50210400.
5. ALL OTHER TRANSISTORS ARE 50210300.
6. DIODE, ZENER, 50240119.
7. DIODE, GERMANIUM, 92116002.
8. DIODE, SILICON, 50240700.
9. ALL OTHER DIODES ARE 92115021.

AYA



VOLTAGE CHECKER
BAA, BAB, BBA, BCA

These cards keep write current and erase current from reaching write heads and erase heads, if one or more of the following conditions are true: 1) +40v drops below +35.0v nominal. 2) +20v drops below +17.6V nominal. 3) -20v gets closer to ground than -17.2v nominal. 4) An external logic signal goes to zero (-0.5v). Logic outputs go to logic zero.

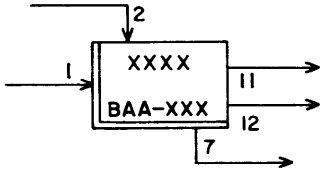
The BAA card has an input on pin 1 from the GAA card, indicating the state of +20v supply. If the +20v supply is at +17.6v ($\pm$ 0.9v), Q01 will turn off and Q02 will turn on. This will turn Q07 off, giving a logic zero out at pins 11 and 12. The Q03 circuit tests the -20V supply. If the -20v is at -17.2v ($\pm$ 0.9v), Q03 will turn on, which has the same effect as Q02 turning on. The Q04-Q05 circuit tests the +40v supply. If the +40v supply is at +35.0v ($\pm$ 1.8v), Q04 will turn off and Q05 will turn on. This has the same effect as Q02 turning on. If the input at pin 2 goes to logic zero (-0.5v), Q06 will turn on. This also has the same effect as Q02 turning on. If more than one of these four sensing circuits respond at one time, the effect is the same as if only one was on.

The BAB card is the same as the BAA card, except that the Q04, 5, and 6 circuits are left off, and R04, 12, and 16 are changed to allow operation from +20v on pin 15.

The BBA card has Q01 turned on if Q07 on the BAA card is turned off. An external resistor to $+V_s$ is required from pin 10. The BCA card has Q01 turned on if Q01 on the BBA card is turned on. Diodes CR07-12 are to isolate the BCA cards and the write and erase heads from each other when the BCA cards are off.

As used in the 807 Disc File, one BAA and BBA drive six BCA cards. Each BCA card then absorbs up to 0.8 amperes of write or erase current. These cards operate from a special $+V_s$ on pin 15, to allow operation if either +20v or +40v fails.

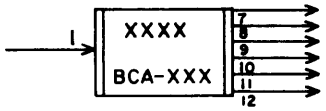
SYMBOL

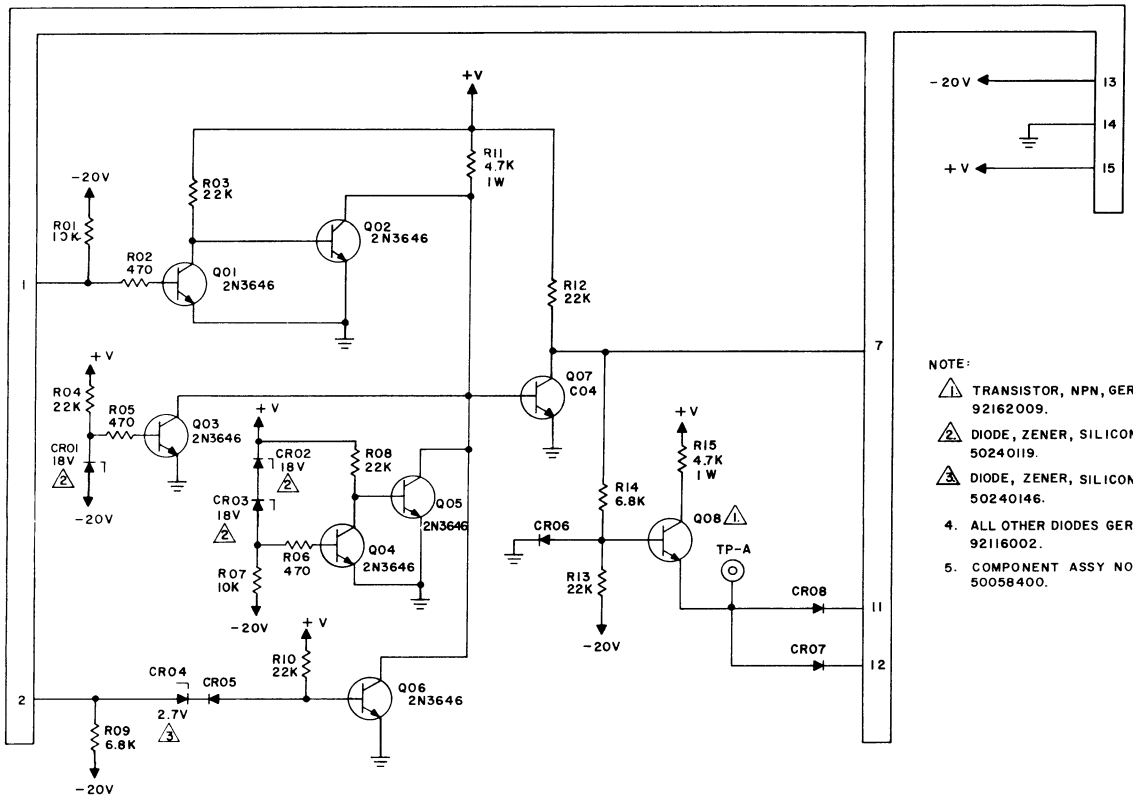


SYMBOL

SYMBOL

SYMBOL

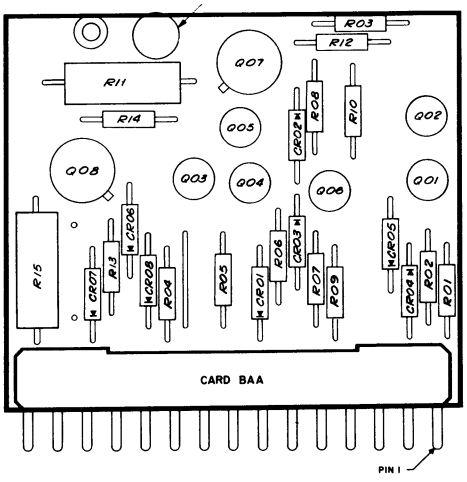


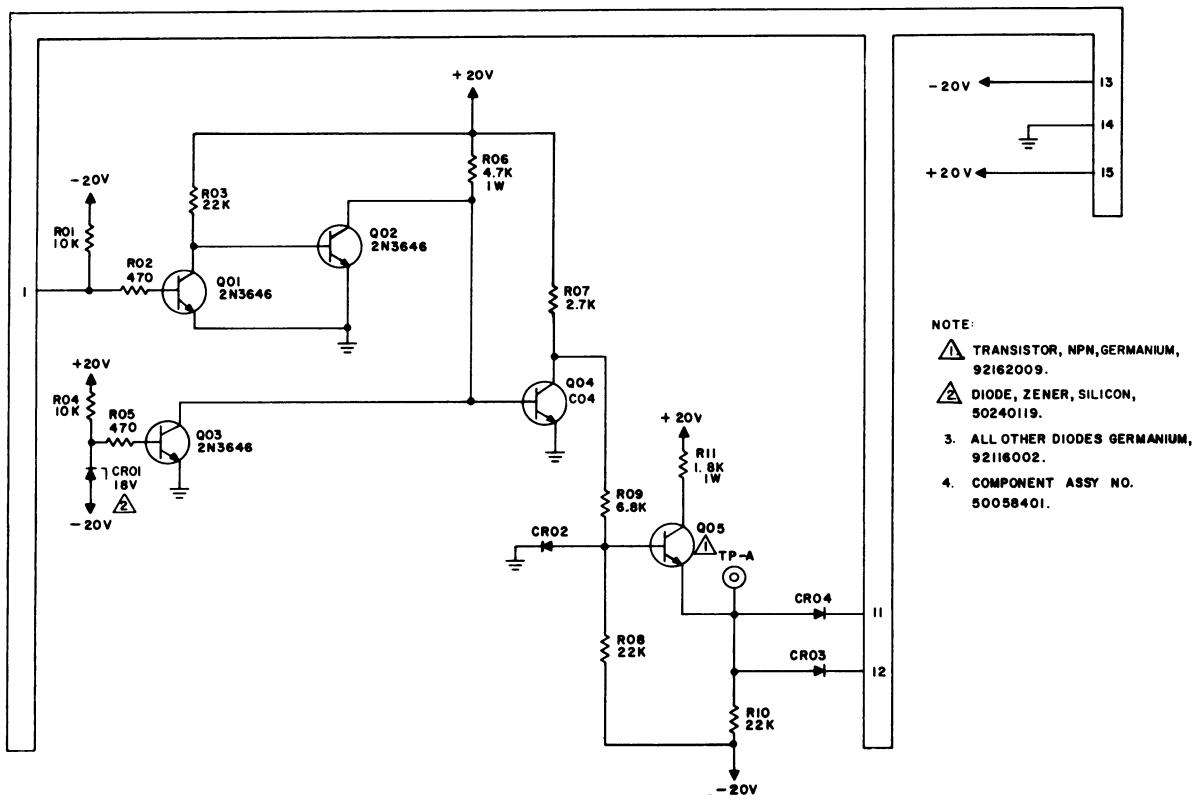


NOTE:

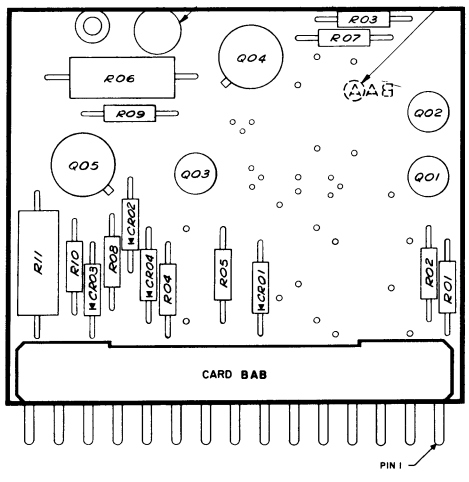
1. TRANSISTOR, NPN, GERMANIUM, 92162009.
2. DIODE, ZENER, SILICON, 50240119.
3. DIODE, ZENER, SILICON, 50240146.
4. ALL OTHER DIODES GERMANIUM, 92116002.
5. COMPONENT ASSY NO. 50058400.

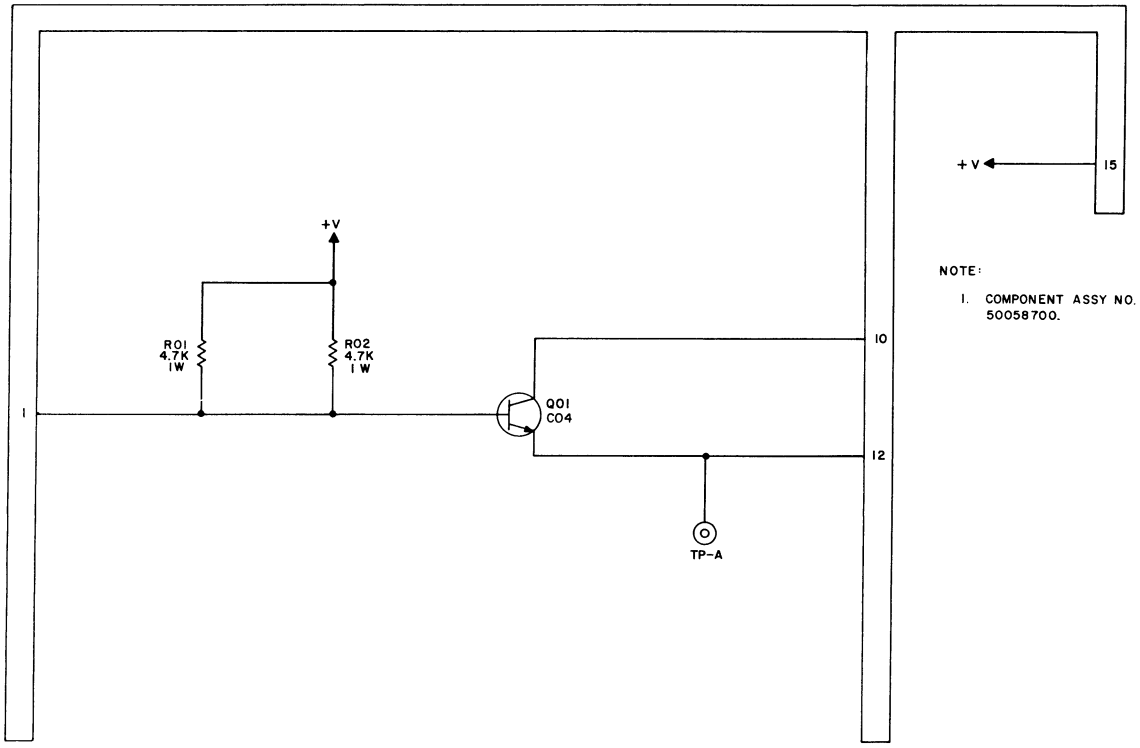
BAA



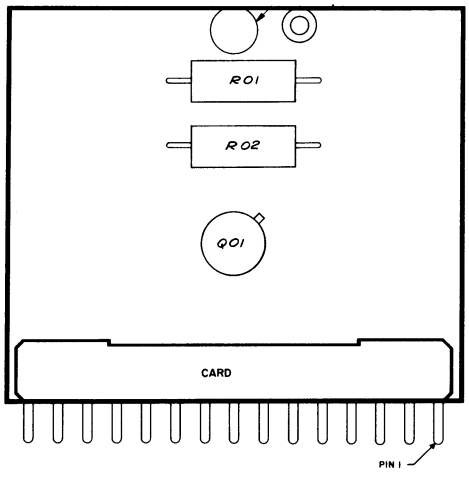

+20V
-20V
R01 10K
R02 470
R03 22K
R04 10K
R05 470
R06 4.7K 1W
R07 2.7K
R08 22K
R09 6.8K
R10 22K
R11 1.8K 1W
Q01 2N3646
Q02 2N3646
Q03 2N3646
Q04 C04
Q05
TP-A
CR01 18V
CR02
CR03
CR04
1
11
12
13
14
15
NOTE:
1. TRANSISTOR, NPN, GERMANIUM, 92162009.
2. DIODE, ZENER, SILICON, 50240119.
3. ALL OTHER DIODES GERMANIUM, 92116002.
4. COMPONENT ASSY NO. 50058401.

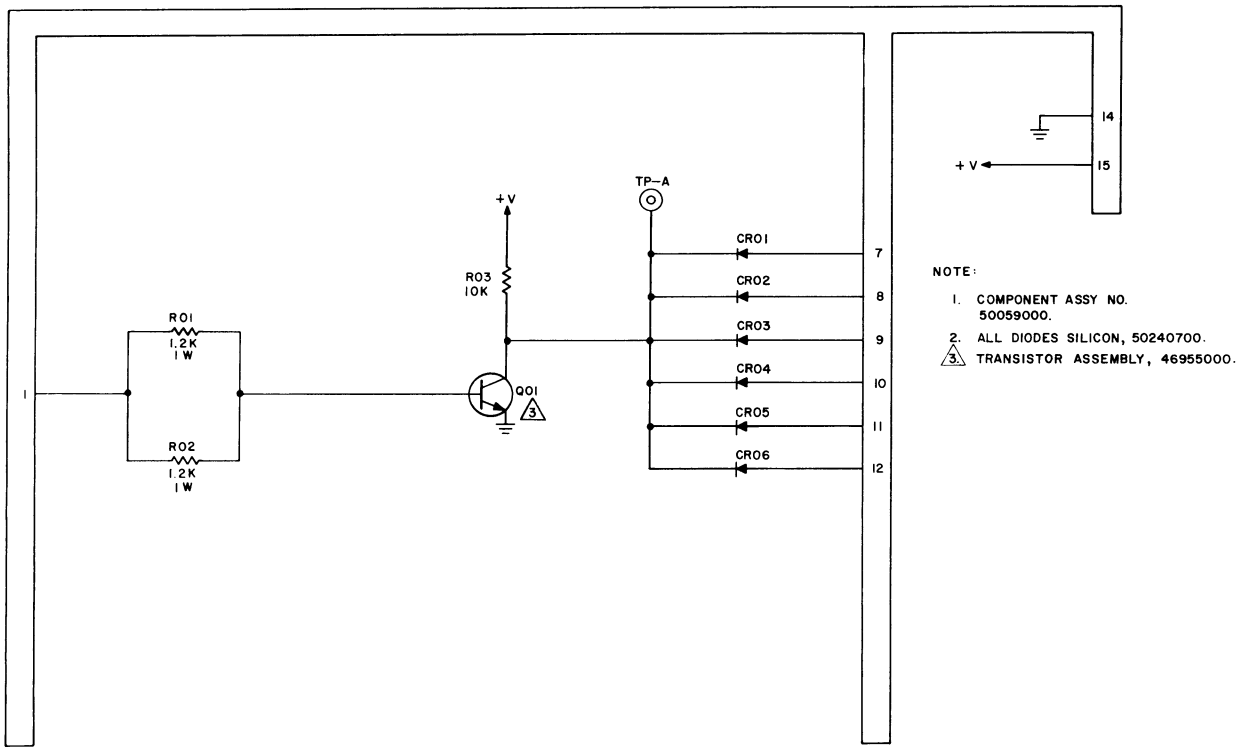
BAB


R03
R07
Q04
R06
R09
Q02
Q05
Q03
Q01
R11
R10
MCR03
R08
MCR02
MCR04
R04
R05
MCR01
R02
R01
CARD BAB
PIN 1

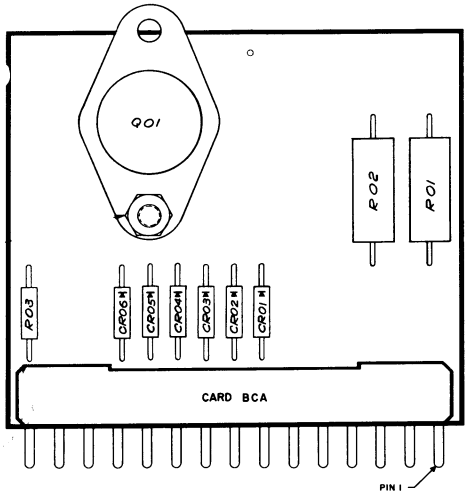

+V
15
NOTE:
1. COMPONENT ASSY NO. 50058700.
+V
R01 4.7K 1W
R02 4.7K 1W
Q01 C04
1
10
12
TP-A

BBA


R01
R02
Q01
CARD
PIN 1


14
+V
15
TP-A
+V
CR01
CR02
CR03
CR04
CR05
CR06
7
8
9
10
11
12
R03
10K
R01
1.2K
1W
R02
1.2K
1W
1
Q01
3
NOTE:
1. COMPONENT ASSY NO. 50059000.
2. ALL DIODES SILICON, 50240700.
3. TRANSISTOR ASSEMBLY, 46955000.

BCA


Q01
R02
R01
R03
CR06M
CR05M
CR04M
CR03M
CR02M
CR01M
CARD BCA
PIN 1

READ LEVEL DETECTOR
EDA

The read level detector is used in the read data circuit to amplify, rectify, and detect NRZ1 information on magnetic tape. Three outputs are provided:

1) A class A low impedance output which provides a gain of 125. Gai may be increased to 190 by means of an external jumper from groun to pin 3.
2) A rectified signal derived from the class A signal which exceeds threshold of 2 volts peak-to-peak. The rectified signal is increased by a factor of 2 from the class A signal for portions in excess of the threshold point. (The threshold may be reduced to 1.1v by means of an external jumper from ground to pin 7.)
3) A "1" output provided by a switching circuit operating from the threshold point when the peak-to-peak threshold is exceeded.

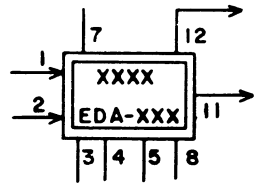
The class A amplifier incorporates a transformer input to minimize common mode signal interference. The amplifier contains one stage of volt age gain (Q01) and two stages of current gain (Q02 and Q03). A positive feedback loop is provided within the amplifier by C02 and R07. This loop returns a signal to the junction of R06 and R07 which approaches, but never exceeds, the signal at the collector of Q01. Thus, R06 presents a very high impedance in the collector load of Q01 and increases the a-c voltage gain of Q01 from a value of less than 100 to over 1000. Gain is stabilize by the negative feedback network composed of R04 and R03 which is used as a reference point for the input transformer secondary. Note that R02 may be connected externally in parallel with R03.

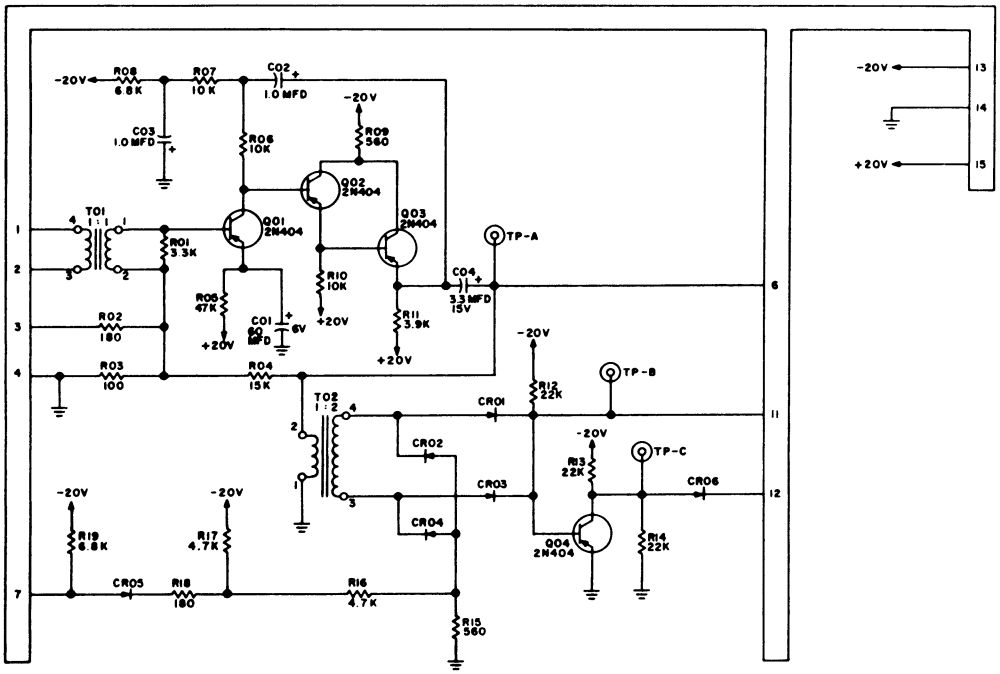
The rectifying circuit is composed of transformer T02 and diodes CR01 through CR04. The threshold at which detection takes place is determined by R15, R16, and R17 when the input to pin 7 is -12v. If pin 7 is jumpere to ground, R18 essentially parallels R15 and R16. Resistor R19 acts as a normal input load and diode CR05 provides isolation from other circuits operating in parallel.

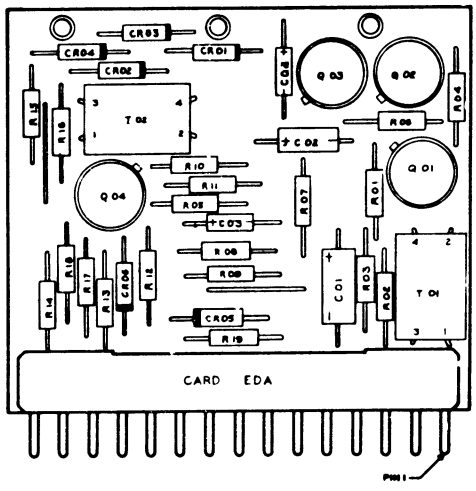
The switching circuit is composed of Q04 which turns off when the rectifier circuit reaches the threshold point. This "1" output may be use directly as a level detection point or as part of an AND term with the pea

detector output.

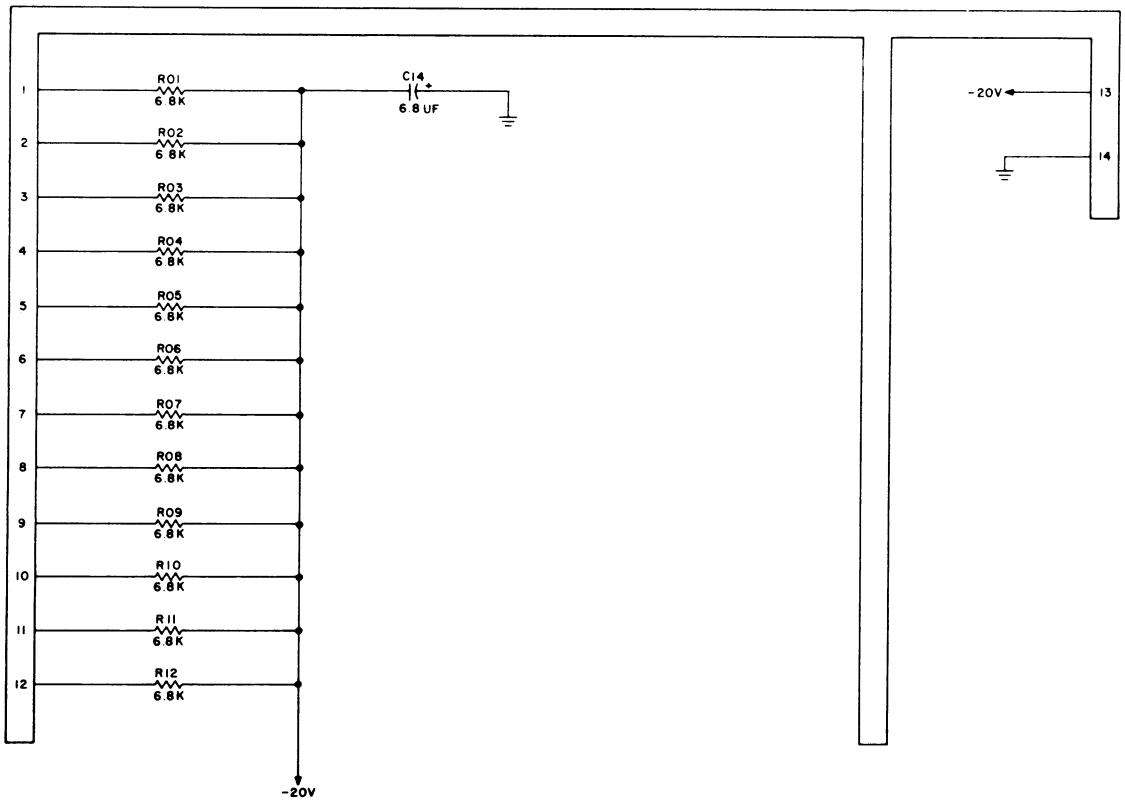
SYMBOL

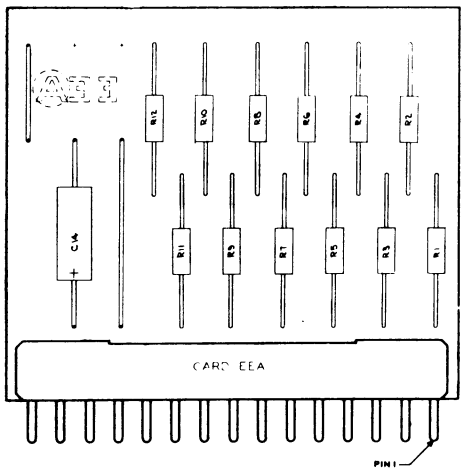






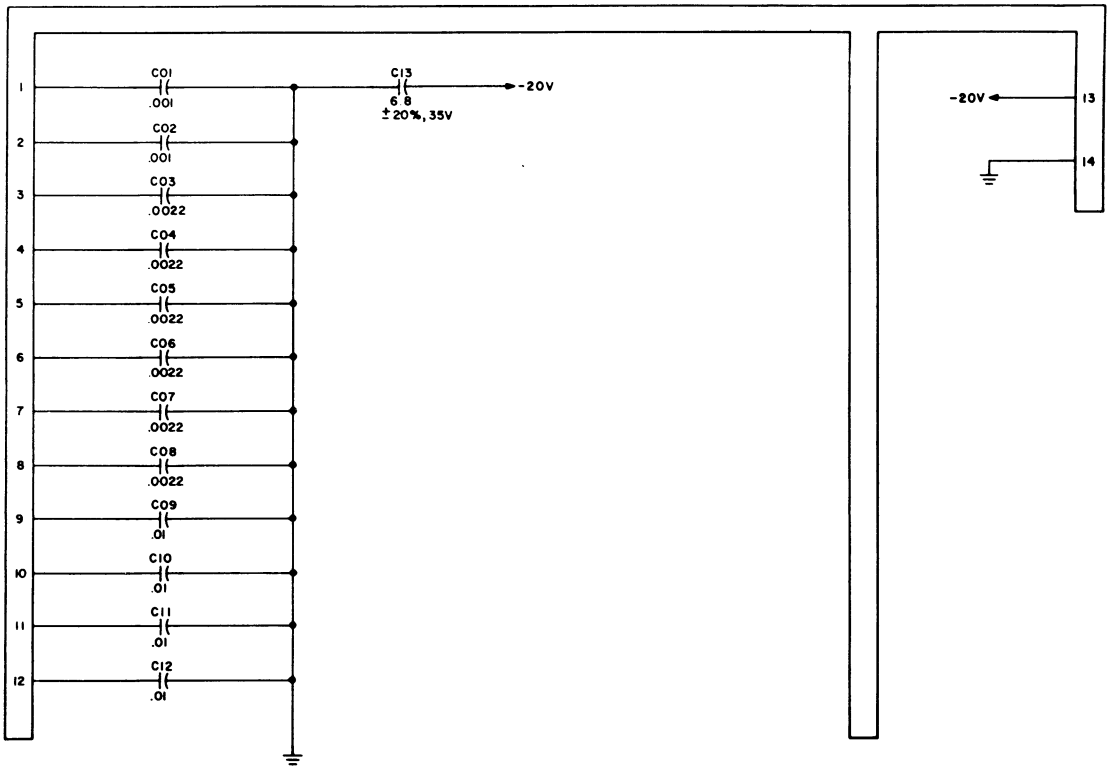
RESISTOR TERMINATION
EEA

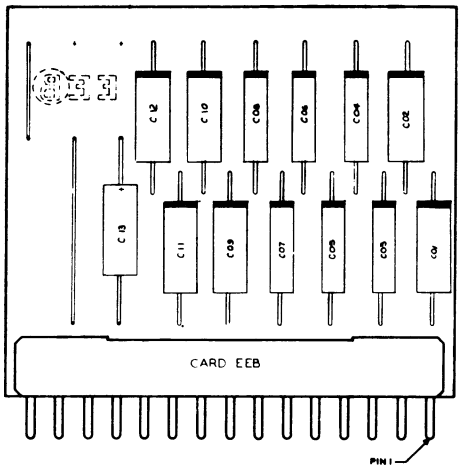




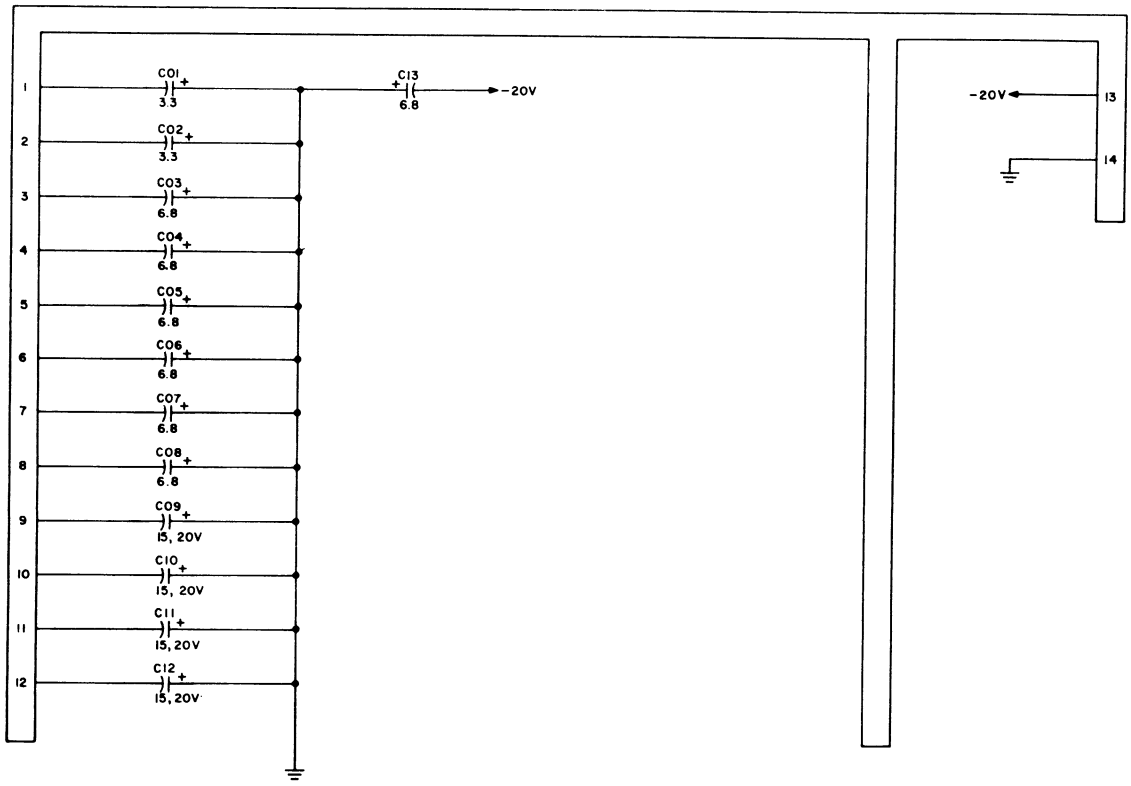
CAPACITOR TERMINATION

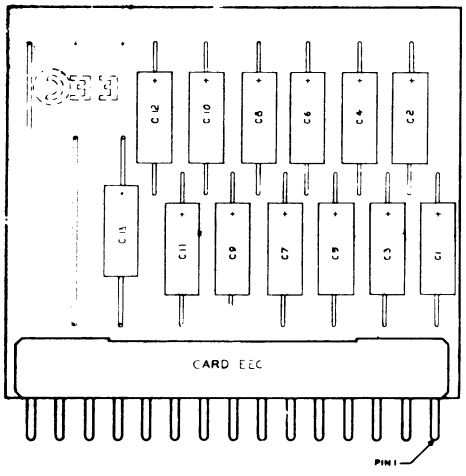
EEB



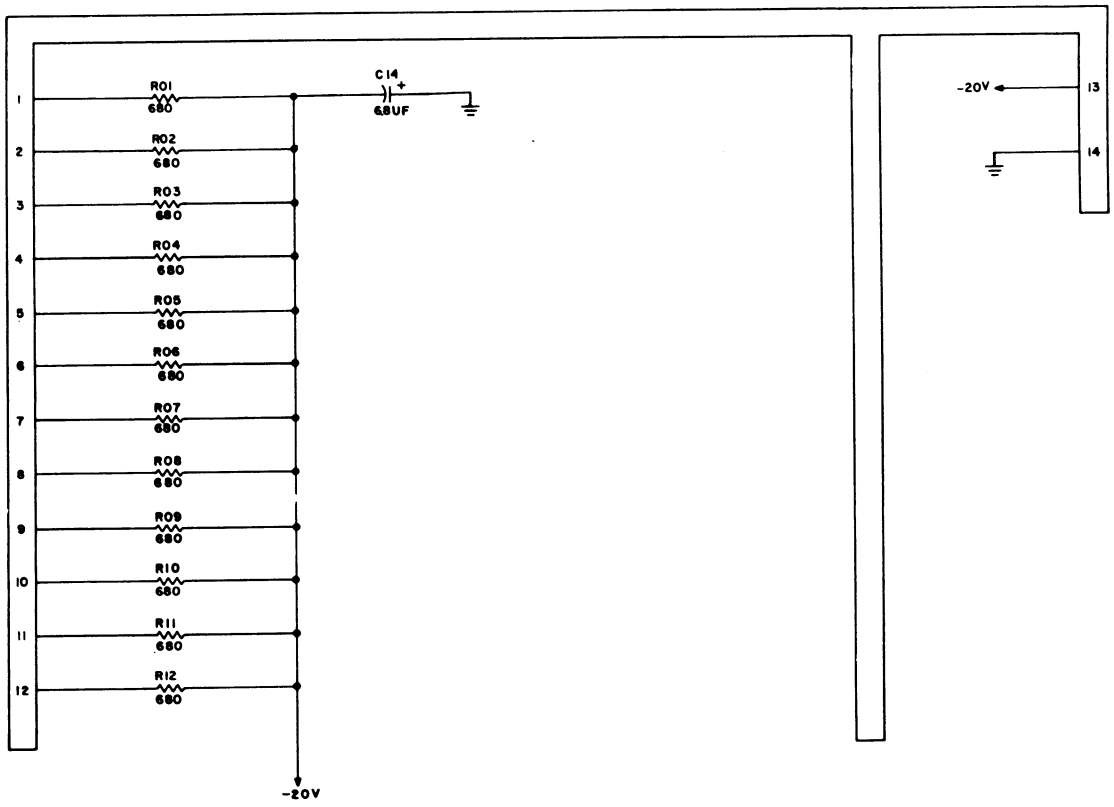


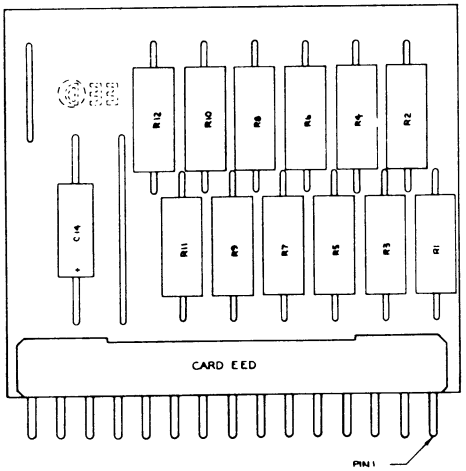
CAPACITOR TERMINATION
EEC



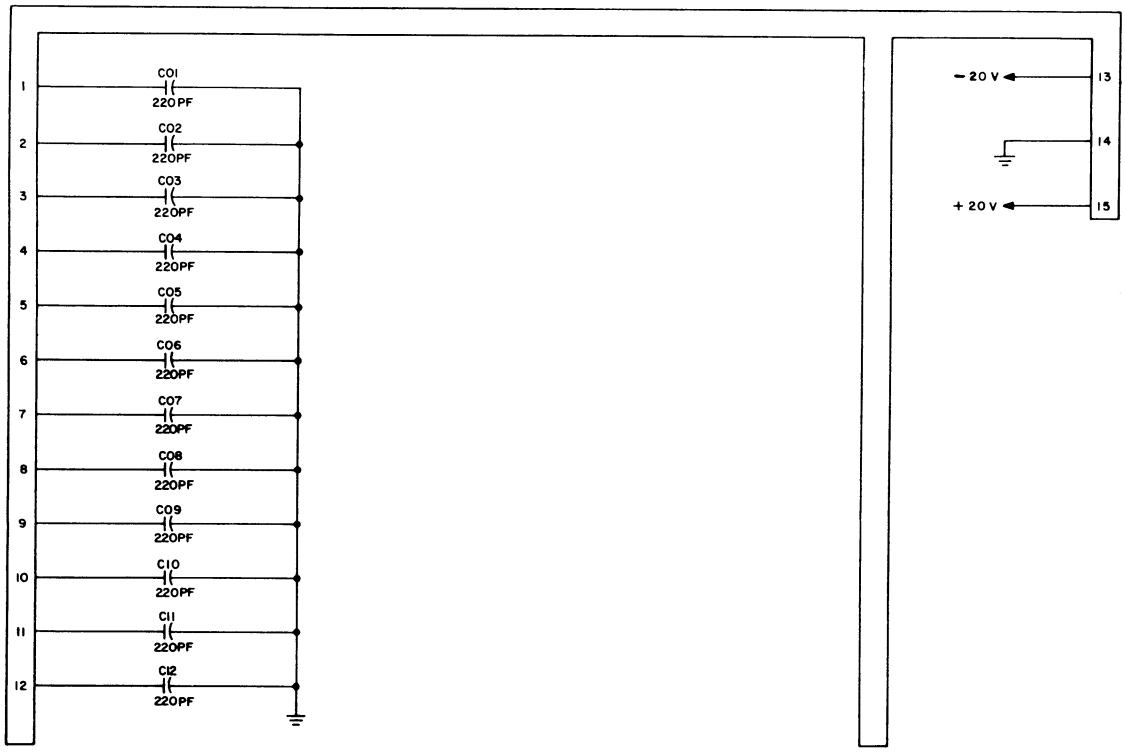


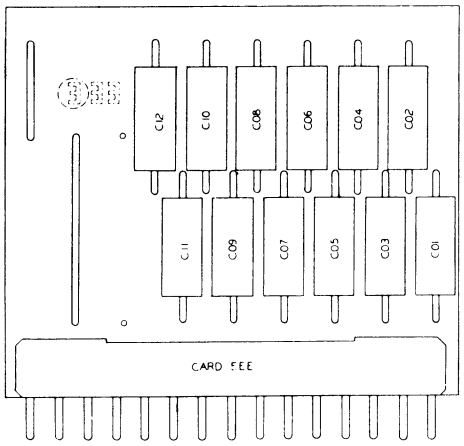
RESISTOR TERMINATION
EED



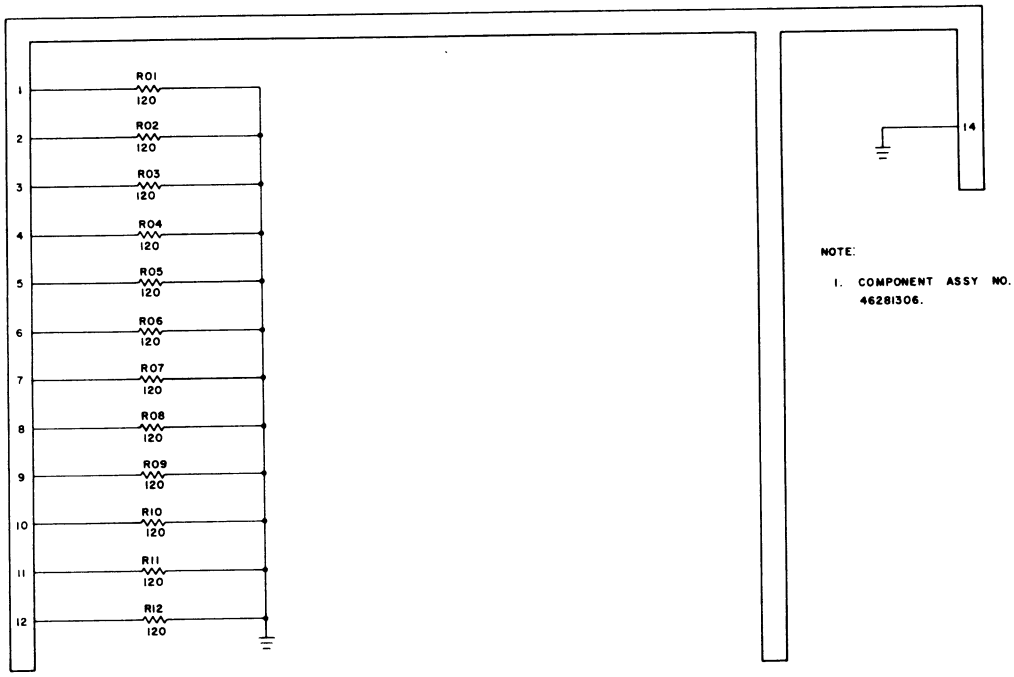


CAPACITOR TERMINATION
EEE



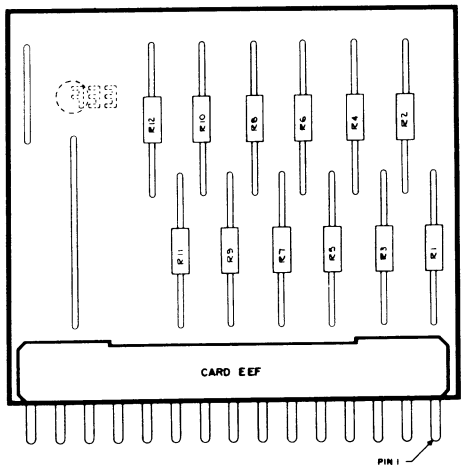


RESISTOR TERMINATION
EEF



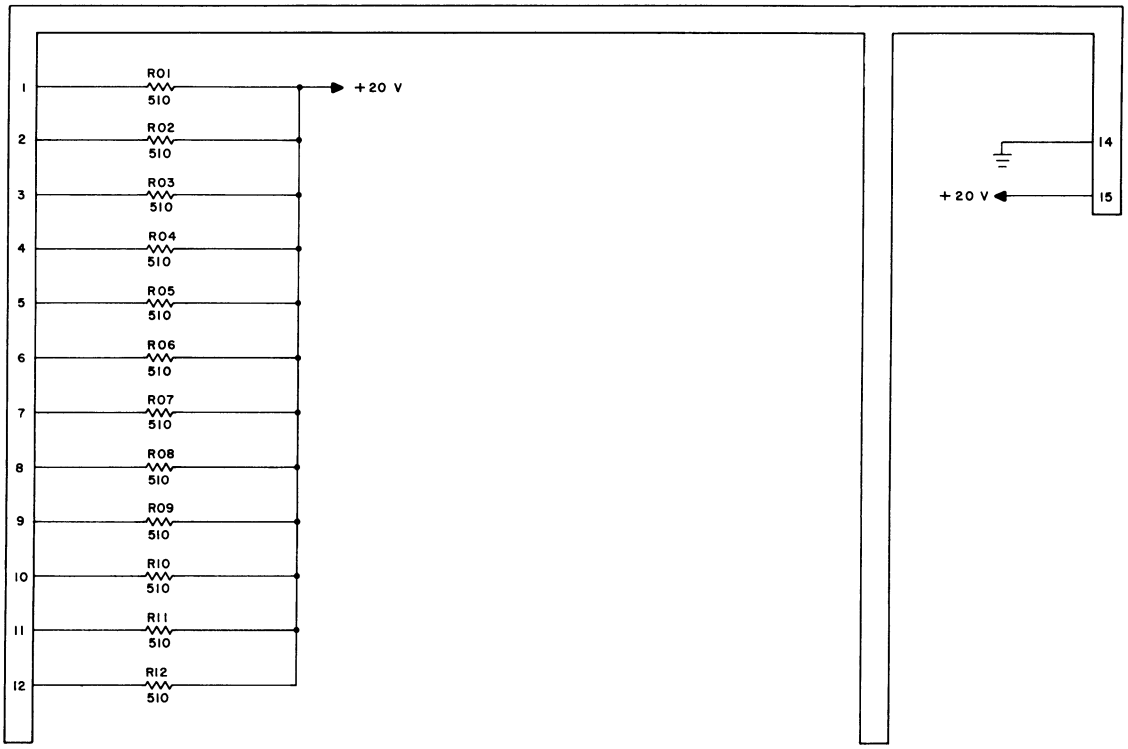
NOTE:

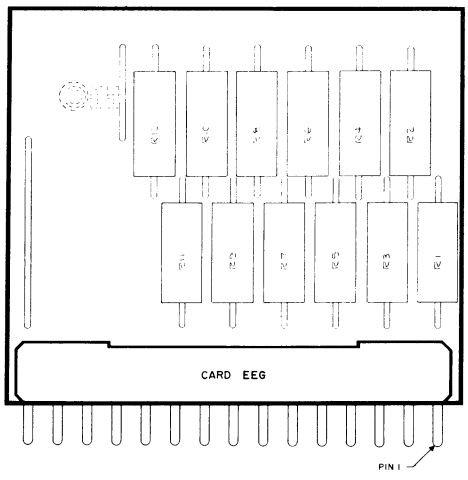
1. COMPONENT ASSY NO. 46281306.



RESISTOR TERMINATION

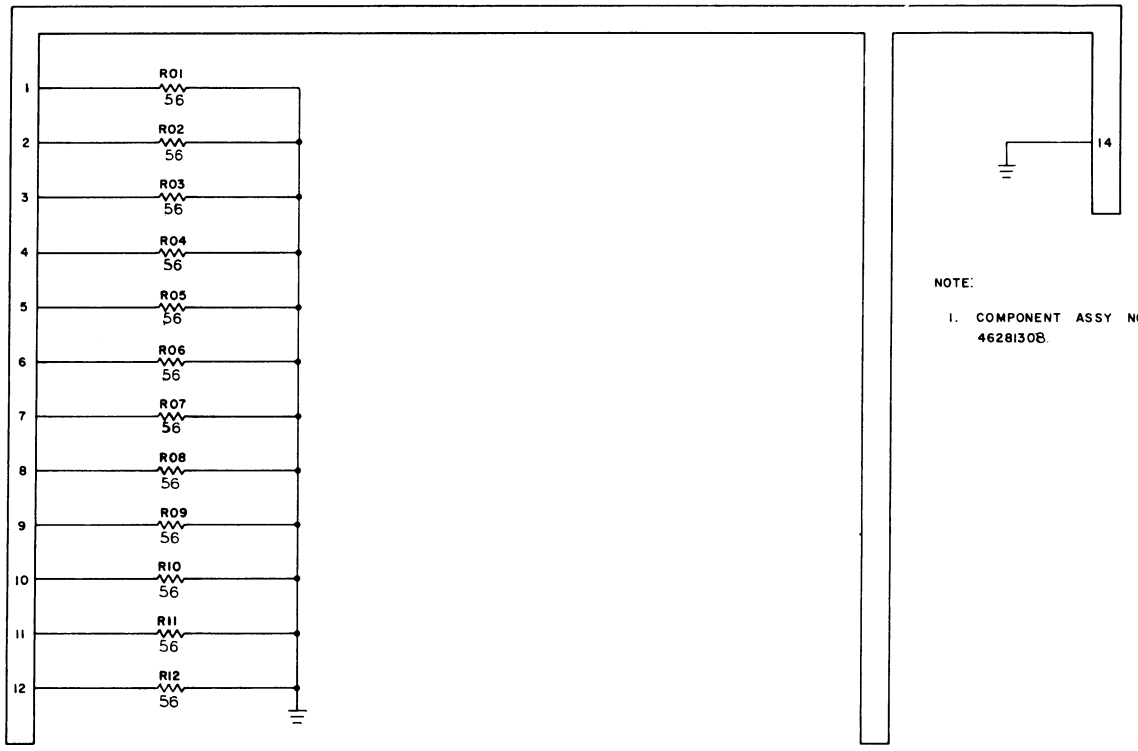
EEG





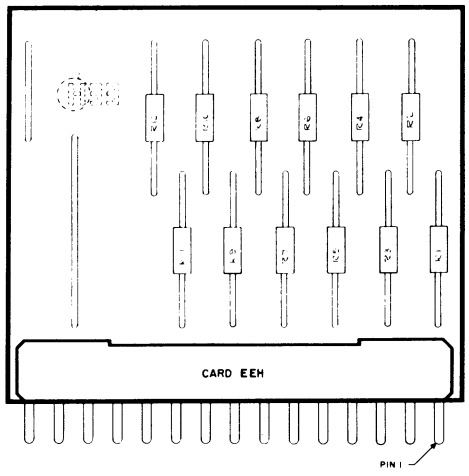
RESISTOR TERMINATION

EEH



NOTE:

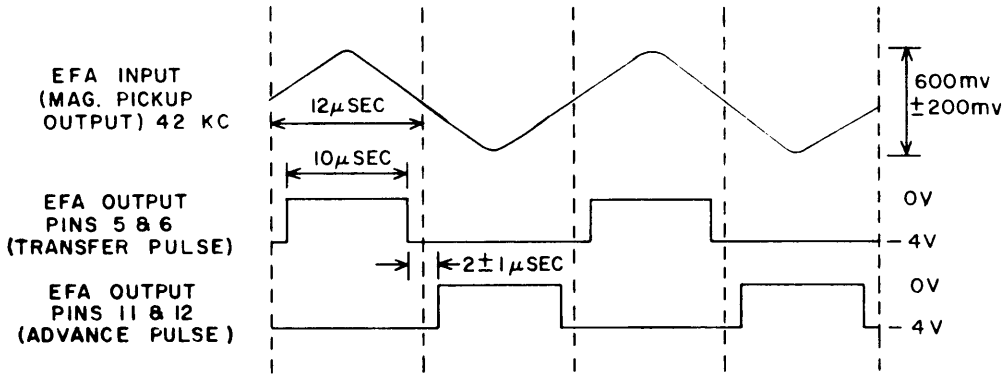
1. COMPONENT ASSY NO. 46281308.

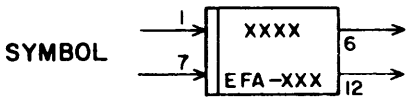


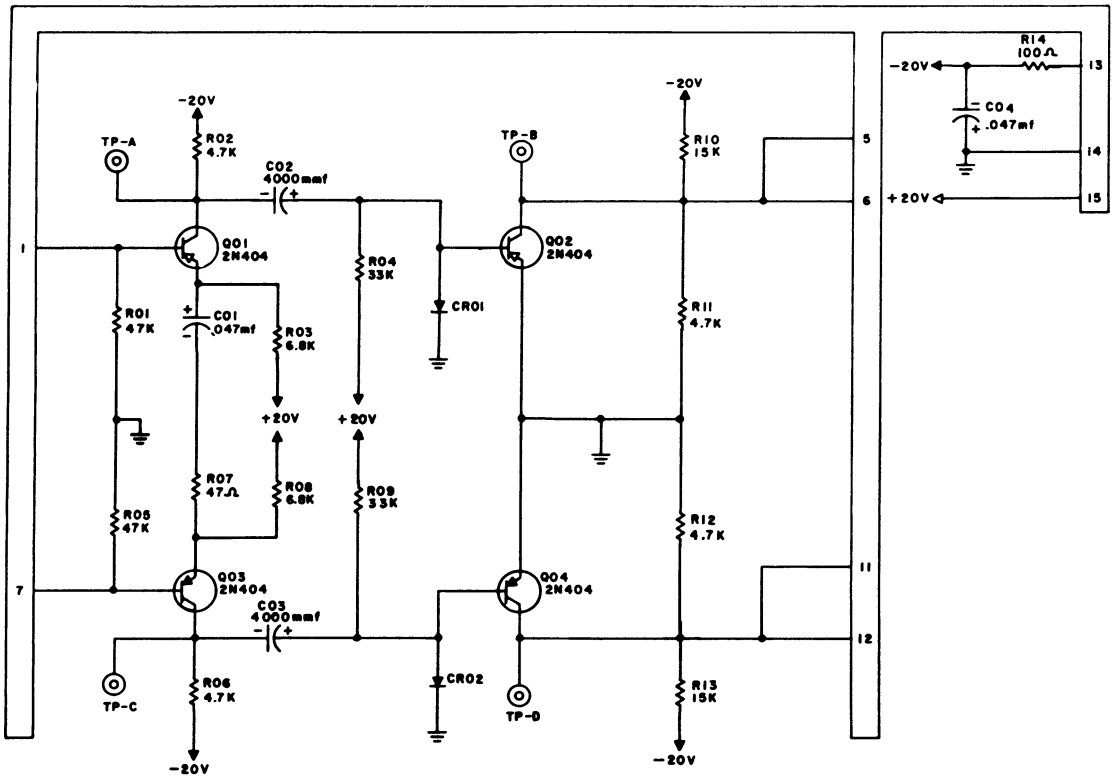
CLOCK AMPLIFIER
EFA

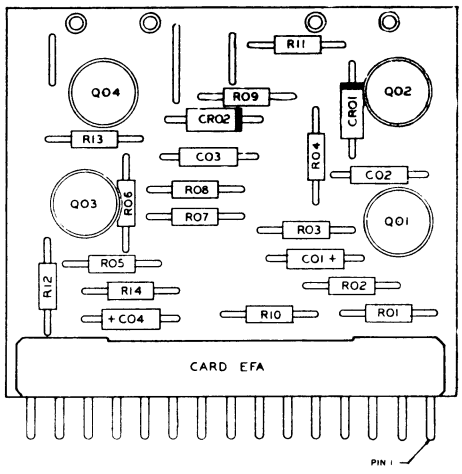
The clock amplifier circuit is intended for use in shaping a magnetic pickup signal into two nonoverlapping output pulses in a card reader. The output pulses are designed as signal sources to drive a clock counter. Typical waveforms are shown below. The circuit is designed for a 42-kc sine wave input, and the output interfaces with standard logic but does not include output diodes for AND terms.

A balanced class A amplifier circuit is used with emitter degeneration and common mode noise rejection in the first stage consisting of Q01 and Q02. A network couples and shapes the waveform to drive the output switching stage which consists of Q03 and Q04.






-20V
TP-A
R02 4.7K
C02 4000mmf
TP-B
R10 15K
R14 100Ω
C04 .047mf
Q01 2N404
Q02 2N404
R04 33K
CR01
R11 4.7K
R01 47K
C01 .047mf
R03 6.8K
+20V
R07 47Ω
R08 6.8K
R09 33K
R12 4.7K
R05 47K
Q03 2N404
Q04 2N404
C03 4000mmf
CR02
TP-C
R06 4.7K
TP-D
R13 15K
1
5
6
7
11
12
13
14
15


R11
Q04
R09
CR02
Q02
CR01
R13
C03
R04
C02
Q03
R06
R08
R07
Q01
R03
R05
C01 +
R12
R14
R02
+C04
R10
R01
CARD EFA
PIN 1

READ LEVEL DETECTOR

EGA

This circuit is a modification of the EDA level detector card with the following differences:

1) The gain can be selected by external jumpers (pins 3, 4, 5, and 8) to allow any of five feedback combinations of the network consisting of resistors R03, R04, R18, and R19. This increases the choice of head turns and tape speeds.

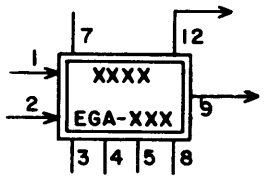
2) The level detection or threshold point is not fixed by components on the card but is selected by a reference voltage that is obtained externally (pin 7). This feature allows a vernier adjustment of the threshold point to match variations in head output or type of tape used.

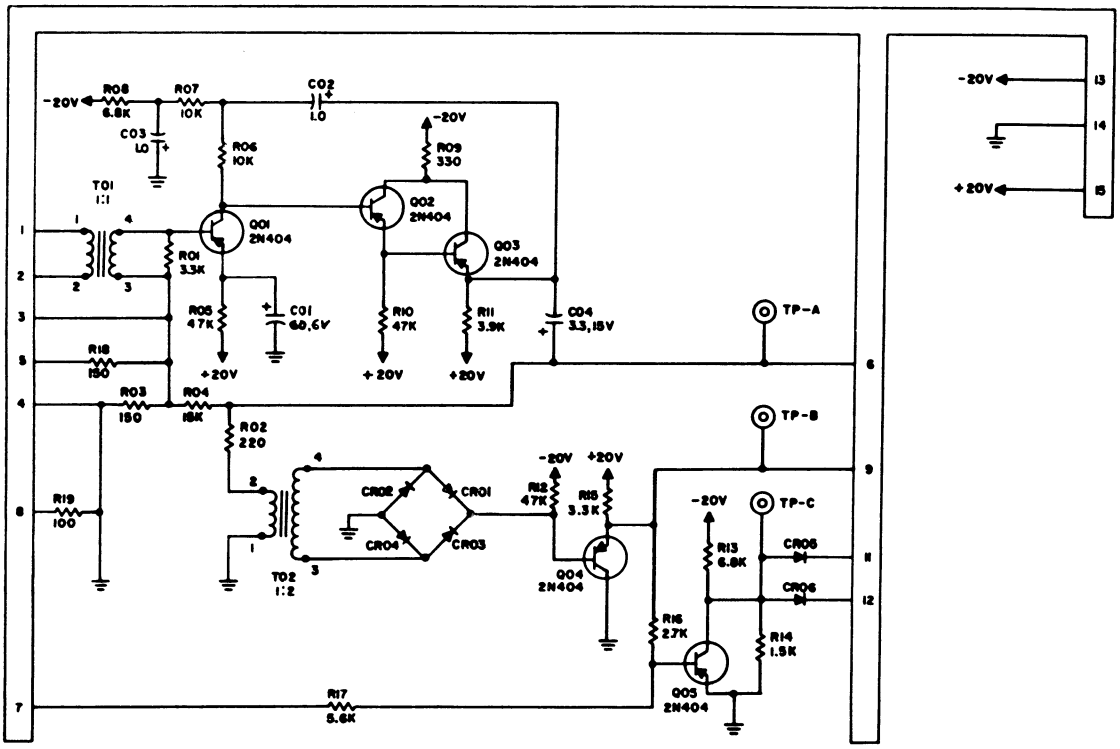
3) Two level detection diodes CR05 and CR06 are available for separate AND terms with the peak detector output.

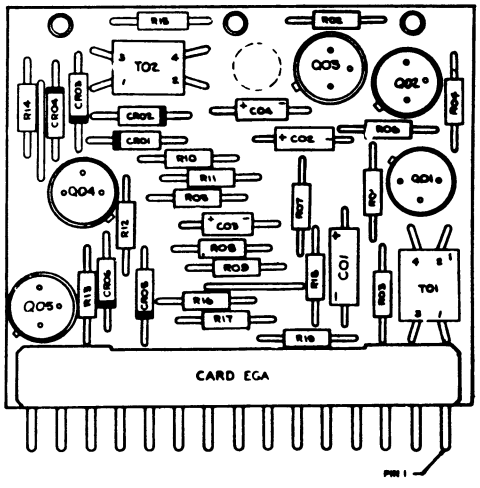
4) The rectifying circuit makes available the whole signal to the peak detector instead of passing only the part in excess of the threshold point. This reduces the ratio of minimum to maximum signal that must be accepted by the peak detector.

5) The class A overload point has been increased to approximately 11 volts in the peak-to-peak output signal.

SYMBOL




-20V
+20V
R08 6.8K
R07 10K
C02 1.0
C03 1.0
R06 10K
R09 330
T01 1:1
Q01 2N404
Q02 2N404
Q03 2N404
R01 3.3K
R05 47K
C01 60.6V
R10 47K
R11 3.9K
C04 3.3,15V
TP-A
R18 150
R03 150
R04 18K
R02 220
TP-B
R19 100
CR02
CR01
CR04
CR03
T02 1:2
R12 47K
R15 3.3K
Q04 2N404
TP-C
R13 6.8K
CR05
CR06
R16 27K
R14 1.5K
Q05 2N404
R17 5.6K
13
14
15


T02
Q03
Q02
Q04
Q01
Q05
T01
C01
CARD EGA
PIN 1

READ PREAMPLIFIER

EHA, EHB, EHC

The read preamplifier is used in the read data circuit to amplify NRZI information recorded on magnetic tape for use in subsequent level and peak detecting circuits. The amplifier circuit includes provision f a differential input and a balanced push-pull output.

The preamplifier has two differential stages of gain (Q01, 02, and Q05, 06) to minimize common mode signal interference. Each differential stage includes an isolating emitter follower output (Q03,04,07,08) to re duce loading effects on the inverting amplifier.

Coarse and fine gain adjustments are provided by negative feedback in the emitter of each stage of gain. Two steps of coarse gain may be selected in the first stage by external jumpers. Connecting pin 5 to pi 7 provides minimum gain and connecting pin 5 to pin 8 provides maximum gain. Fine gain is provided by adjusting the potentiometer R22 in the second stage. This adjustment provides the following gains:

	Jumper Pins
EHA - 150 to 550	5-7
350 to 1300	5-8
EHB - 200 to 800	5-7
500 to 1800	5-8

Except for the output and the emitter degeneration, the amplifier i direct-coupled to reduce recovery time. Power supply transients are min imized by the common mode rejection of the differential amplifier. In addition, R21 and C03 filter the negative supply for both stages; CR01 a R18 reduce the voltage for the first stage.

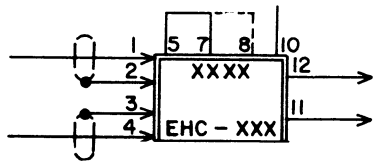
The EHC circuit differs from the EHB as follows:

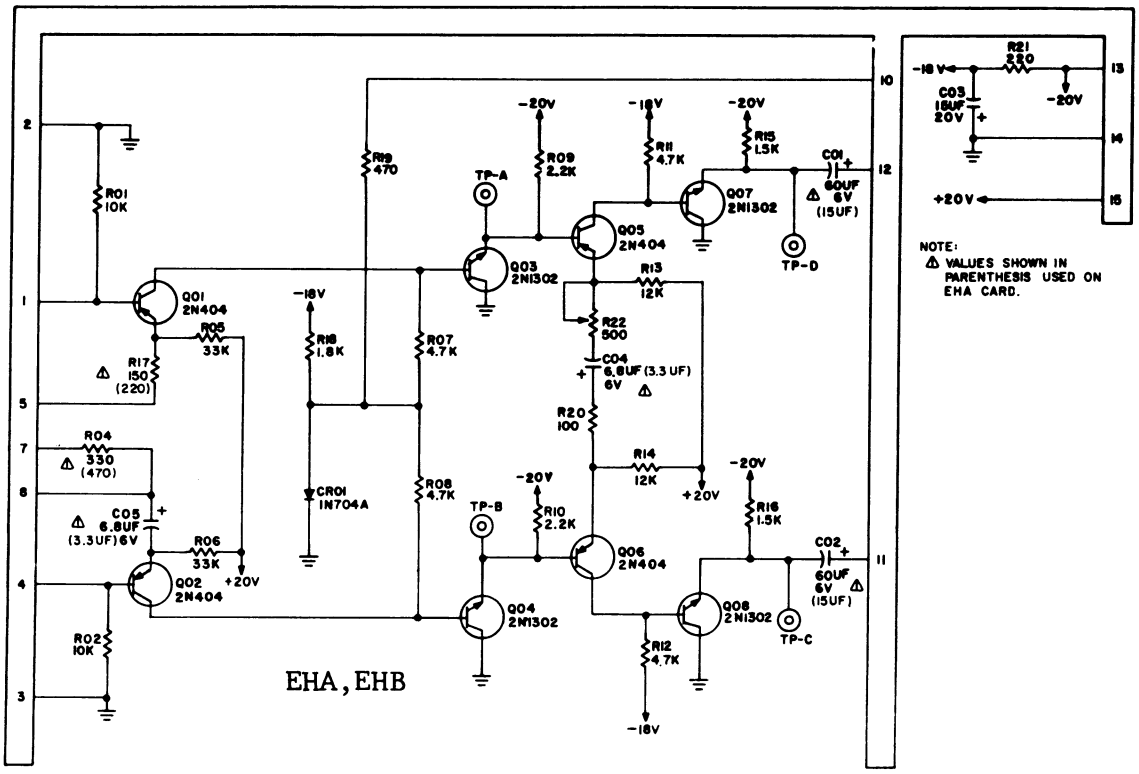
1. Capacitors C06 and C07 provide two stages of high frequenc roll-off. Each capacitor reduces gain by about 3 db at 100 kc (sine wave).
2. Output capacitors C01 and C02 are polarized for load termi ations of -10 to -16 volts or for isolated transformer windings such as those on EI-series cards.
3. Gain jumpering options are not interchangeable with the EH except when pin 5-7 is used at frequencies of 30 kc and lo Gain ranges for sine-wave frequencies of 5 to 30 kc are

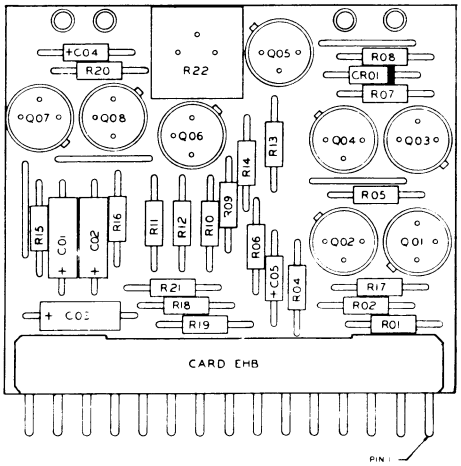
tabulated below:

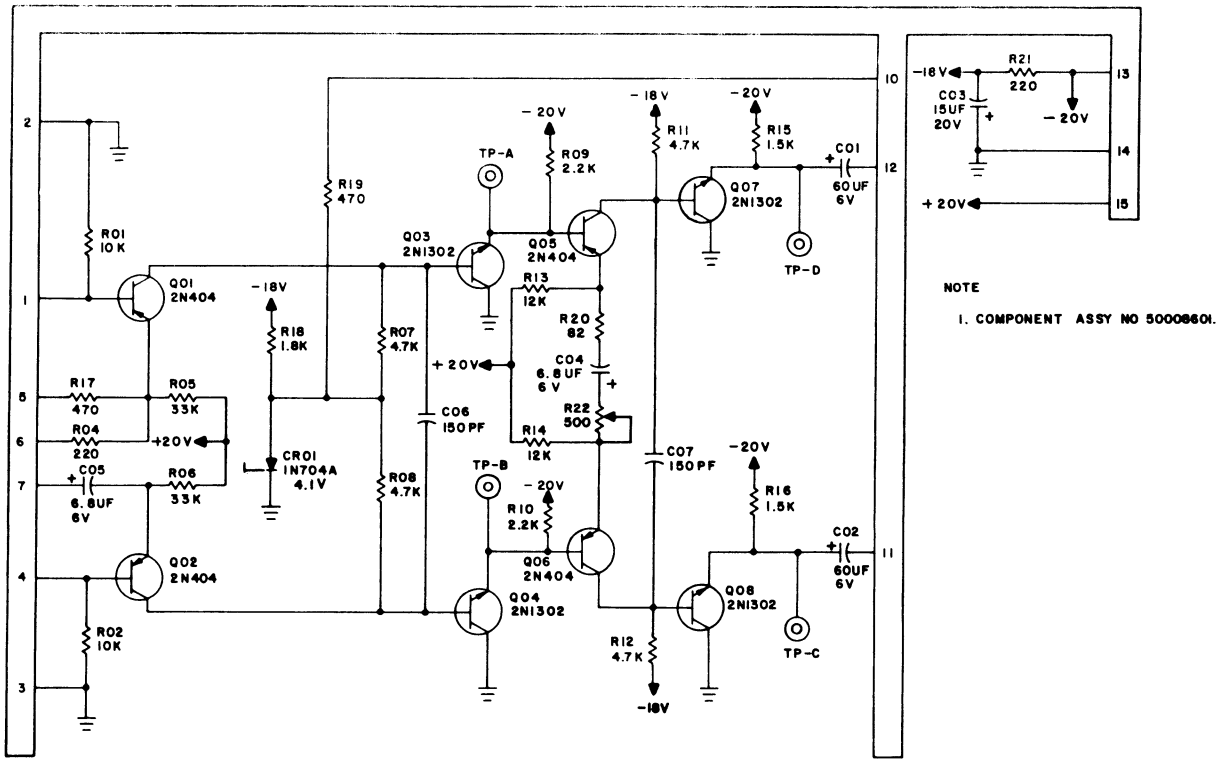
	Jumper Pins
EHC - 200-800	5-7
360-1400	6-7
500-1800	5-6-7

SYMBOL

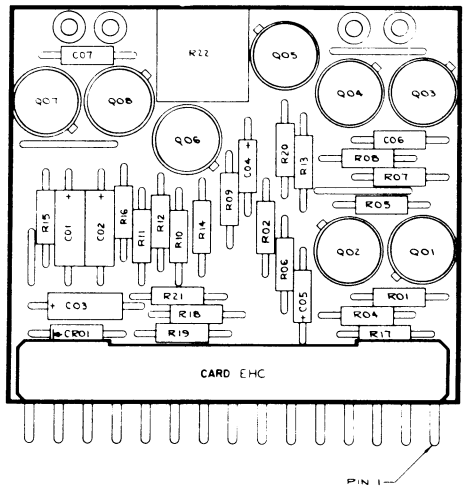







Q01 2N404
Q02 2N404
Q03 2N1302
Q04 2N1302
Q05 2N404
Q06 2N404
Q07 2N1302
Q08 2N1302
R01 10K
R02 10K
R04 220
R05 33K
R06 33K
R07 4.7K
R08 4.7K
R09 2.2K
R10 2.2K
R11 4.7K
R12 4.7K
R13 12K
R14 12K
R15 1.5K
R16 1.5K
R17 470
R18 1.8K
R19 470
R20 82
R22 500
C01 60UF 6V
C02 60UF 6V
C03 15UF 20V
C04 6.8UF 6V
C05 6.8UF 6V
C06 150PF
C07 150PF
CR01 1N704A 4.1V
TP-A
TP-B
TP-C
TP-D
-18V
-20V
+20V
R21 220
NOTE
1. COMPONENT ASSY NO 5000860I.

EHC


CARD EHC
PIN 1

READ LEVEL DETECTOR
EIA, EIB, EID, EIE

The read level detector receives the amplifed signal from the read preamplifier (EH-series) and provides a rectified signal and a threshold enable for the peak detector (OG-series) in the recovery of NRZ1 information from the magnetic tape.

The rectifying circuit is composed of transformer T01, diodes CR01 and CR02, and transistors Q01 and Q02. The negative rectified signal is then routed to the differential input stage of the level detecting circuit (Q04 and Q05). The signal is compared to the threshold input reference voltage on pin 7. The switching point is further enhanced and referenced to ground by the amplifiers consisting of transistors Q06 and Q07, in a form usable as an enable in the peak detector.

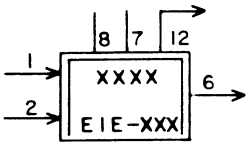
The rectified signal is also routed to an output emitter follower (Q03) which drives the RC differentiating circuit in the input stage of the peak detector.

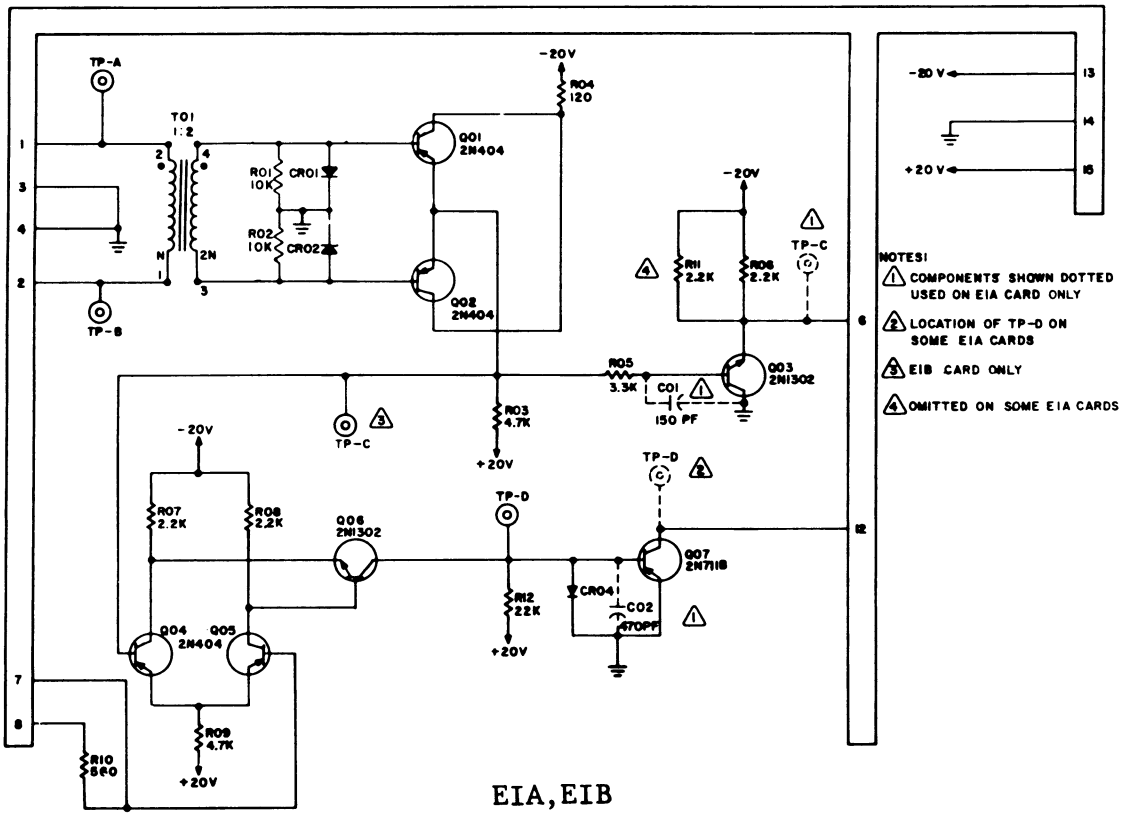
The EID and EIE circuits differ from the EIB as follows:

1. Rectifier transformer T01 is designed to pass 5 kc sine-wave signals compared to 20 kc as a lower limit on the EIB card. This delays and filters some of the higher frequency components and is intended primarily for fundamental signals not exceeding 45 kc sine-wave frequency (90 kc NRZ1 data rate).
2. Resistors R13 and R14 are added to cause diodes CR01 and CR02 to maintain a lower transformer secondary impedance during zero or weak signals.
3. Q01 and Q02 are matched transistors to assure better signal balance of both polarities of input. Transistors Q04 and Q05 are matched to provide more accurate level detection thresholds.

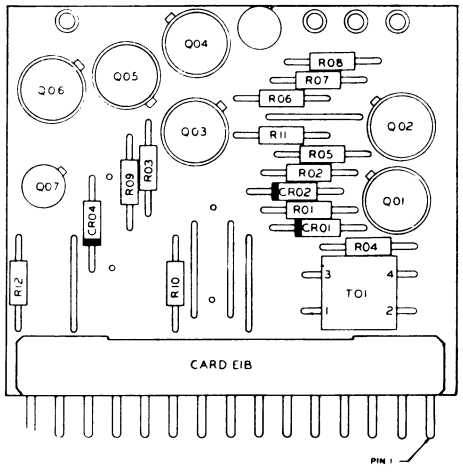
The EIE card differs from the EID only in the addition of C01, which provides one RC stage of additional high frequency roll-off (down 3 db at 200 kc data rate).

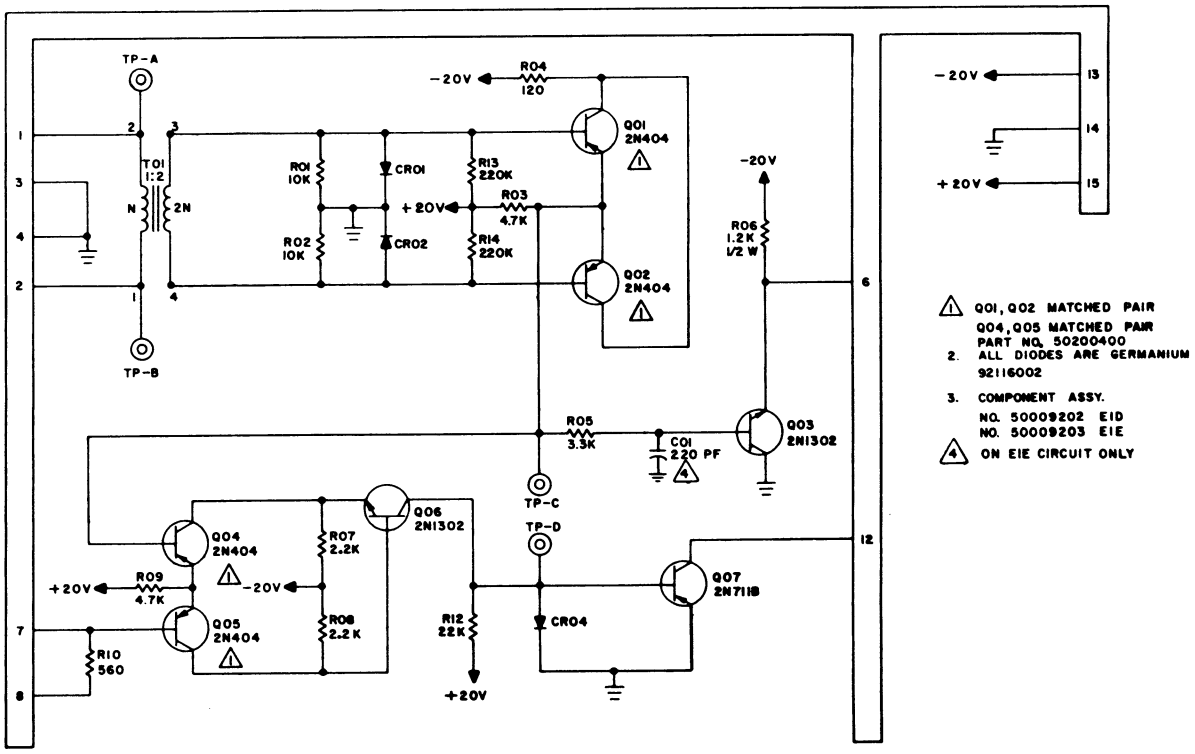
SYMBOL



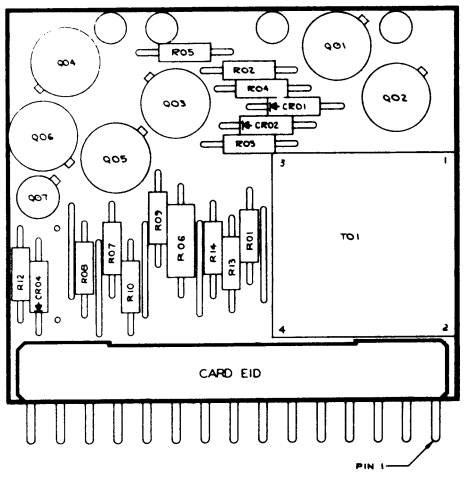


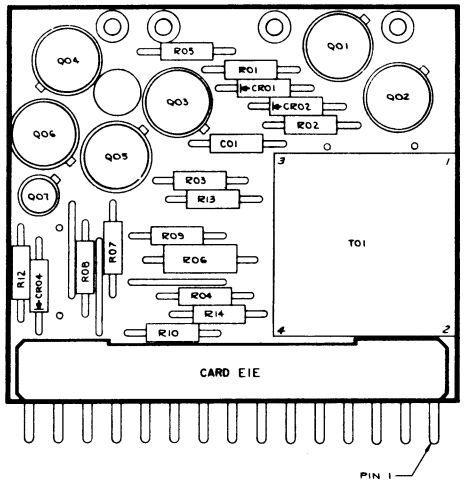
EIA, EIB




TP-A
TP-B
TP-C
TP-D
T01
1:2
N
2N
R01
10K
R02
10K
CR01
CR02
R13
220K
R14
220K
+20V
R03
4.7K
R04
120
-20V
Q01
2N404
Q02
2N404
R05
3.3K
C01
220 PF
Q03
2N1302
R06
1.2K
1/2 W
Q04
2N404
Q05
2N404
R07
2.2K
R08
2.2K
Q06
2N1302
R09
4.7K
R10
560
R12
22K
CR04
Q07
2N711B
1
2
3
4
5
6
7
8
12
13
14
15
Q01, Q02 MATCHED PAIR
Q04, Q05 MATCHED PAIR
PART NO. 50200400
2. ALL DIODES ARE GERMANIUM
92116002
3. COMPONENT ASSY.
NO. 50009202 EID
NO. 50009203 EIE
4 ON EIE CIRCUIT ONLY

EID, EIE


CARD EID
PIN 1
T01


CARD EIE
PIN 1
T01

POTENTIOMETER

EPA

The potentiometer card is designed for use with the EGA read level detector in the recovery of NRZ1 information on magnetic tape. It provides an external gain adjustment for 7 circuits when properly connected in the negative feedback loop of the preamplifier circuit of the EGA card. This allows amplifier output amplitude to be equalized for variations in head output and circuits.

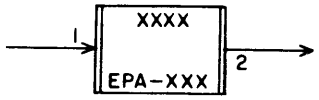
Each EPA circuit includes 7 potentiometers, connected as rheostats, one for each of the 7 bits recorded on 1/2 inch compatible tape. Five of the potentiometers have both ends brought out to external pins; the other two have 100-ohm resistors to ground to simulate R19 (pin 8) of the EGA card. This utilizes the 12 signal pins on the card.

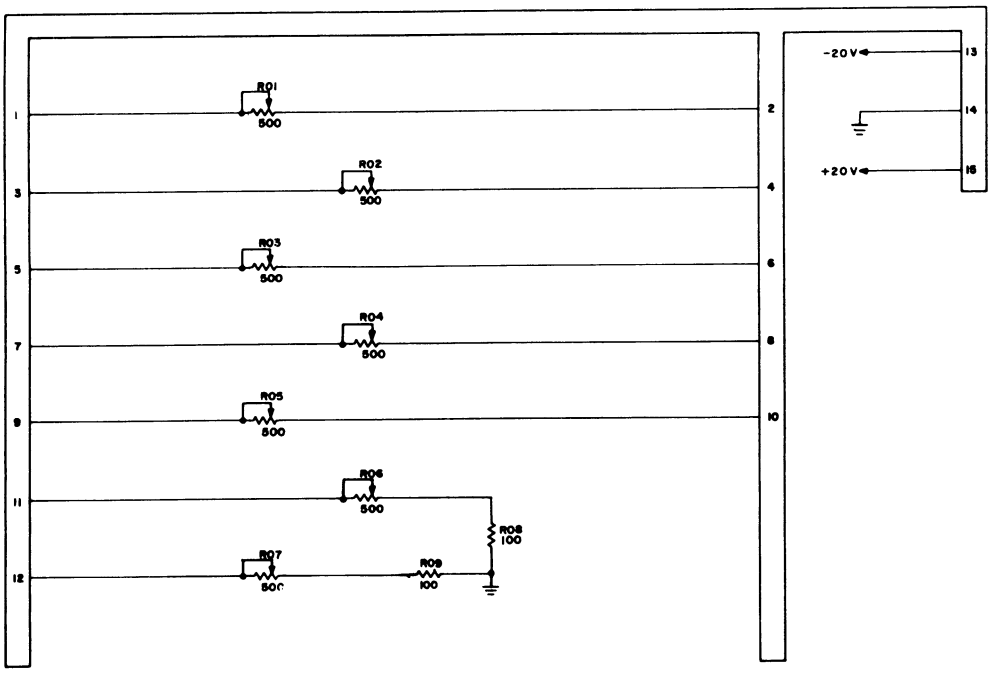
CAUTION: The height of potentiometers used on the EPA card requires that the adjacent card slot on the component side of the card be left empty. In removing and replacing the card, care should be given to minimize mechanical stress on the potentiometer cases or the internal element may be cracked.

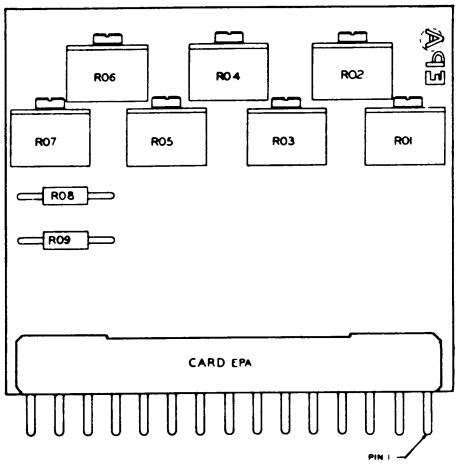
A typical connection is as follows:

EPA Pin No.		
1	3	EGA, track 0
2	8	
3	3	EGA, track 1
4	8	
5	3	EGA, track 2
6	8	
7	3	EGA, track 3
8	8	
9	3	EGA, track 4
10	8	
11	3	EGA, track 5
12	3	EGA, track 6

SYMBOL




R01
500
R02
500
R03
500
R04
500
R05
500
R06
500
R08
100
R07
500
R09
100
1
2
3
4
5
6
7
8
9
10
11
12
-20V
+20V
13
14
15

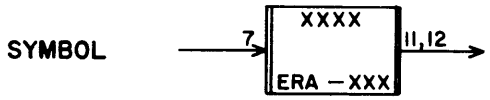

R06
R04
R02
R07
R05
R03
R01
R08
R09
CARD EPA
PIN 1

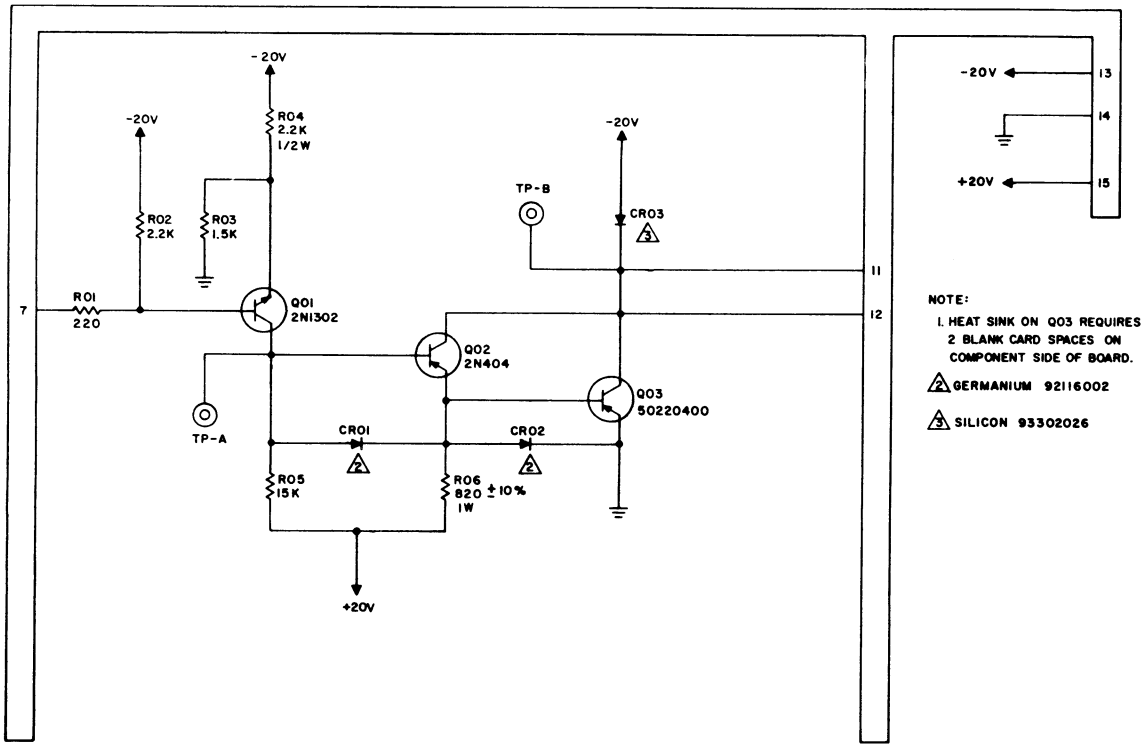
SOLENOID DRIVER
ERA

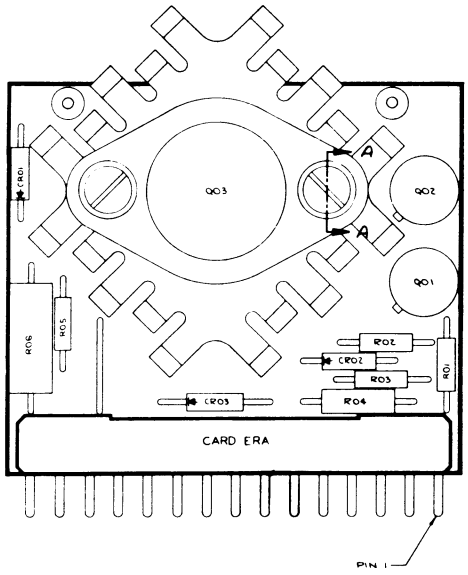
The solenoid driver is designed to switch a 2¼ ampere load terminated at a negative voltage between -2v and -20v. Its input is intended to match that of an "L" card output. When the input is at ground the output is driven to ground. Thus an open input turns the circuit off.

The circuit is intended to operate the tape unit capstan solenoid. In this application it is located apart from the general logic. The high steady state current capability of the circuit requires special heat sinking of the output transistor. The "claw" type heat sink is mounted on standard logic card hardware, but requires space equivalent to three card slots. No signals are placed on pins 1-3 to eliminate the possibility of damage if the card is inserted upside down in the normal logic connector.

Circuit operation is as follows. A ground on the input turns Q01 on. Q01 collector current turns Q02 on, which in turn turns on Q03. R03 and R04 in the emitter circuit of Q01 determine the switching point of the input signal. CR03 acts as a suppression circuit for inductive loads. Other components have functions similar to those in ordinary inverter circuits.



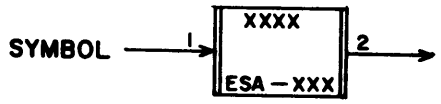

-20V
R04
2.2K
1/2W
-20V
R02
2.2K
R03
1.5K
TP-B
CR03
3
-20V
11
7
R01
220
Q01
2N1302
12
Q02
2N404
Q03
50220400
TP-A
CR01
2
CR02
2
R05
15K
R06
820 ± 10%
1W
+20V
-20V
13
14
+20V
15
NOTE:
1. HEAT SINK ON Q03 REQUIRES 2 BLANK CARD SPACES ON COMPONENT SIDE OF BOARD.
2 GERMANIUM 92116002
3 SILICON 93302026

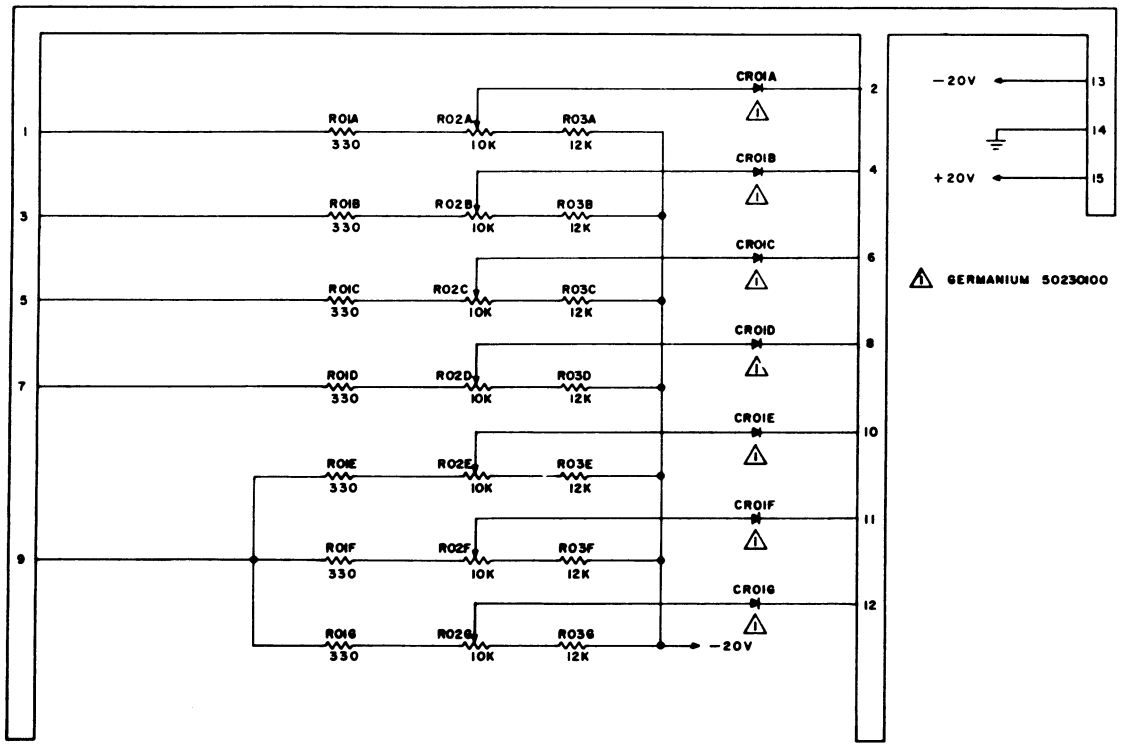

CR01
Q03
A
A
Q02
Q01
R06
R05
R02
CR02
R03
R01
CR03
R04
CARD ERA
PIN 1

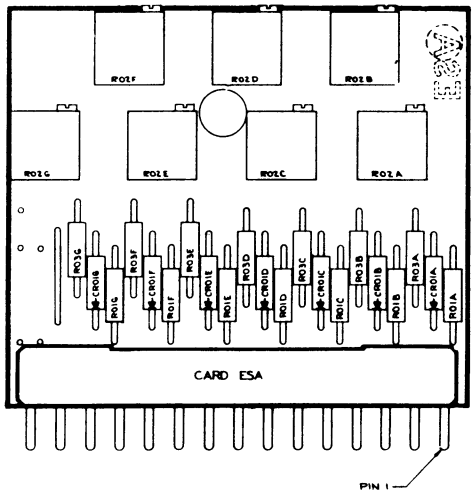
DELAY CONTROL POTENTIOMETERS
ESA

The delay control potentiometer circuit is designed for use with voltage-controlled delay circuits such as the UGA, in which it is desired to obtain one or more additional selected delays from a single delay circuit and still maintain good precision. It acts as a gating circuit to work into a positive OR terminating resistor that does not require a low-impedance input.

The card contains seven like circuits. All outputs are isolated from each other, but three of the seven inputs are paralleled to reduce the connections to the twelve pins available for signals. The seven circuits are sufficient for use with a seven-channel read recovery system in tape units. Input signals should have an excursion of 0 to -12v (or more negative) and require about 2 ma drive for a -20v terminated load on each of the seven circuits. Normally, all inputs are parallel connected and used for read reverse deskew while the potentiometers on the UGA cards are used for read forward deskew. The circuits can also be used as a voltage-reference circuit for other applications whether gated or permanently grounded on its input.




R01A 330
R02A 10K
R03A 12K
CR01A
R01B 330
R02B 10K
R03B 12K
CR01B
R01C 330
R02C 10K
R03C 12K
CR01C
R01D 330
R02D 10K
R03D 12K
CR01D
R01E 330
R02E 10K
R03E 12K
CR01E
R01F 330
R02F 10K
R03F 12K
CR01F
R01G 330
R02G 10K
R03G 12K
CR01G
-20V
+20V
GERMANIUM 50230100


CARD ESA
PIN 1

DIFFERENTIAL AMPLIFIER
EUA

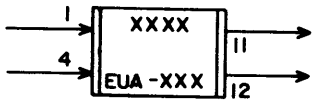
The EUA card is a differential 2-stage amplifier. The output is an amplifier reproduction of the input.

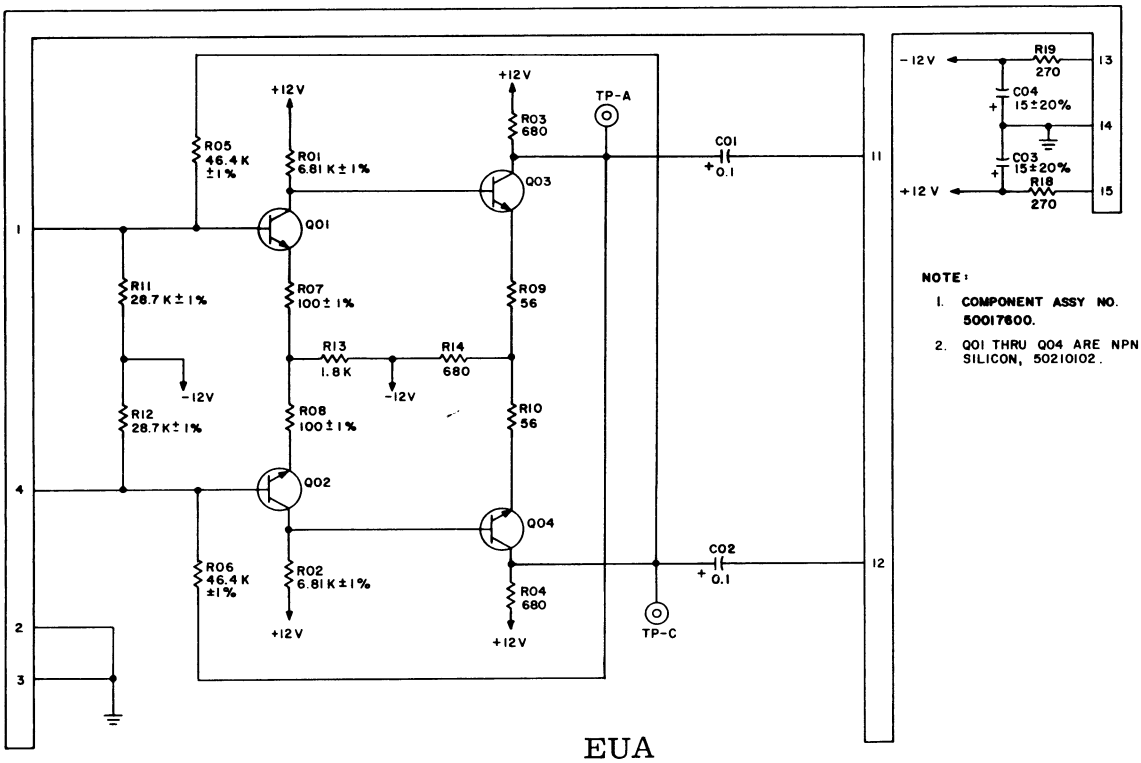
To improve operation, internal voltages are isolated from machine power supply by R-C filters. The circuit is designed to operate from a source impedance of approximately 1 K, and to drive a load of approximately 1.2 K. Bandpass is from 10 KC to 5 MC.

DIFFERENTIAL AMPLIFIER
EUC

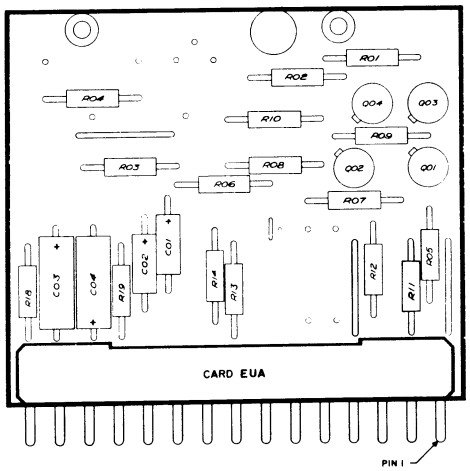
This card is similar to the EUA card. The two significant differences are: feedback paths were added from collector to base of Q01 and Q02 to reduce high frequency gain, and an output power-amplifier stage (Q05 and Q06) was added to allow the circuit to drive a low impedance load. Design source impedance is approximately 1 K, and load impedance is 500 ohms. Bandpass is from 10 KC to 2 MC.

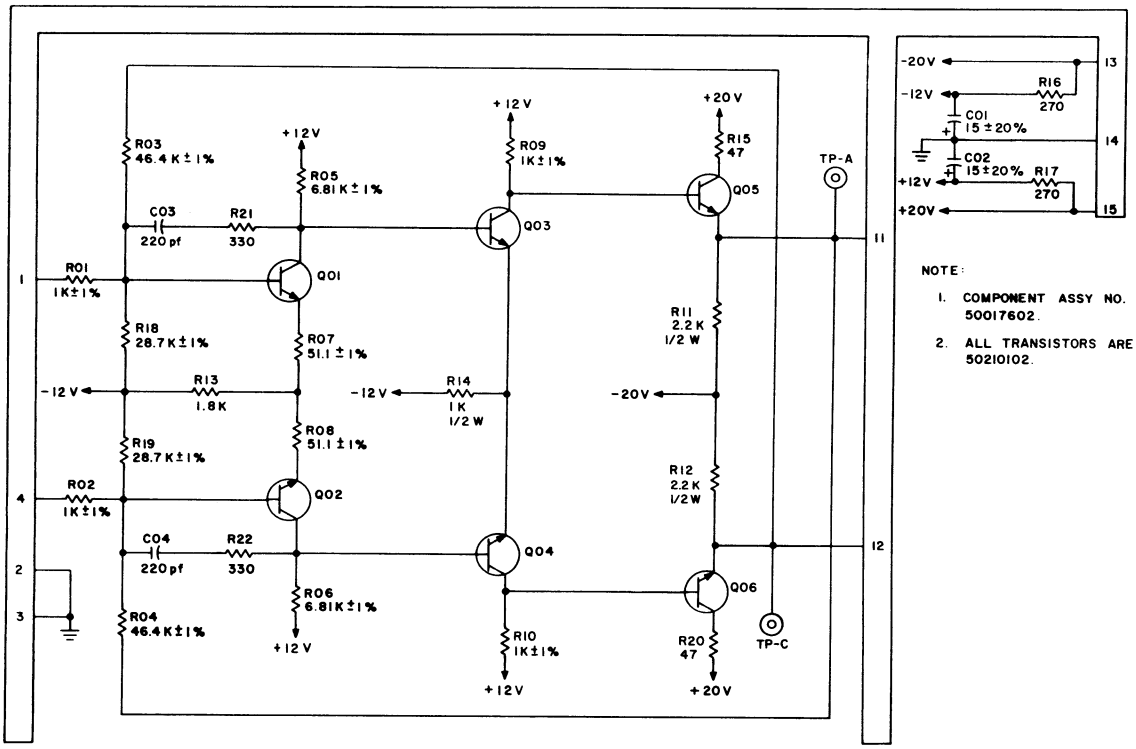
SYMBOL



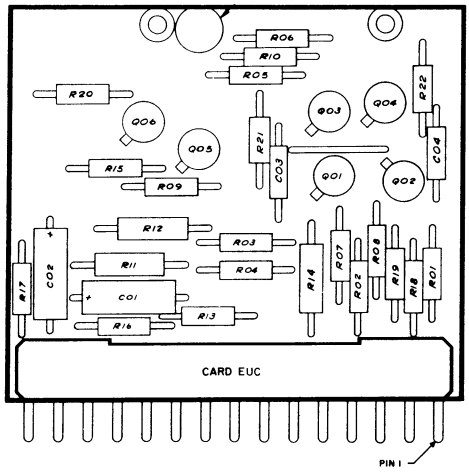

+12V
+12V
TP-A
R03
680
R05
46.4 K
±1%
R01
6.81 K ± 1%
C01
+0.1
Q03
Q01
R11
28.7 K ± 1%
R07
100 ± 1%
R09
56
R13
1.8 K
R14
680
-12V
-12V
R12
28.7 K ± 1%
R08
100 ± 1%
R10
56
Q02
Q04
C02
+0.1
R06
46.4 K
±1%
R02
6.81 K ± 1%
R04
680
+12V
+12V
TP-C
1
2
3
4
11
12
-12V
R19
270
13
C04
15 ±20%
14
C03
15 ±20%
+12V
R18
270
15
NOTE:
1. COMPONENT ASSY NO. 50017600.
2. Q01 THRU Q04 ARE NPN SILICON, 50210102.

EUA


R01
R02
R04
Q04
Q03
R10
R09
R03
R08
Q02
Q01
R06
R07
C03
C04
R19
C02
C01
R14
R13
R12
R11
C05
CARD EUA
PIN 1


R03 46.4 K ± 1%
R05 6.81 K ± 1%
+12 V
R09 1K ± 1%
+20 V
R15 47
TP-A
C03 220 pf
R21 330
Q03
Q05
R01 1K ± 1%
Q01
R18 28.7 K ± 1%
R07 51.1 ± 1%
R11 2.2 K 1/2 W
-12 V
R13 1.8 K
R14 1K 1/2 W
-20 V
R08 51.1 ± 1%
R19 28.7 K ± 1%
R12 2.2 K 1/2 W
R02 1K ± 1%
Q02
C04 220 pf
R22 330
Q04
Q06
R06 6.81 K ± 1%
R04 46.4 K ± 1%
R10 1K ± 1%
R20 47
TP-C
1
2
3
4
11
12
-20V
-12V
+12V
+20V
R16 270
C01 15 ± 20%
C02 15 ± 20%
R17 270
13
14
15
NOTE:
1. COMPONENT ASSY NO. 50017602.
2. ALL TRANSISTORS ARE 50210102.

EUC


R06
R10
R05
R20
Q06
Q05
R15
R09
Q03
Q04
R22
C04
R21
C03
Q01
Q02
R12
R03
R11
R04
C02
C01
R16
R13
R14
R07
R02
R19
R18
R01
R17
CARD EUC
PIN 1

RECEIVER FLIP-FLOP

EVB

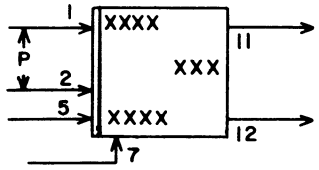
This card has a balanced twisted-pair line input, which is transferred to an internal flip-flop by an external pulse. An external gate level can inhibit transfer from the input to the flip-flop, and force both outputs to logical "0". The outputs do not have AND diodes.

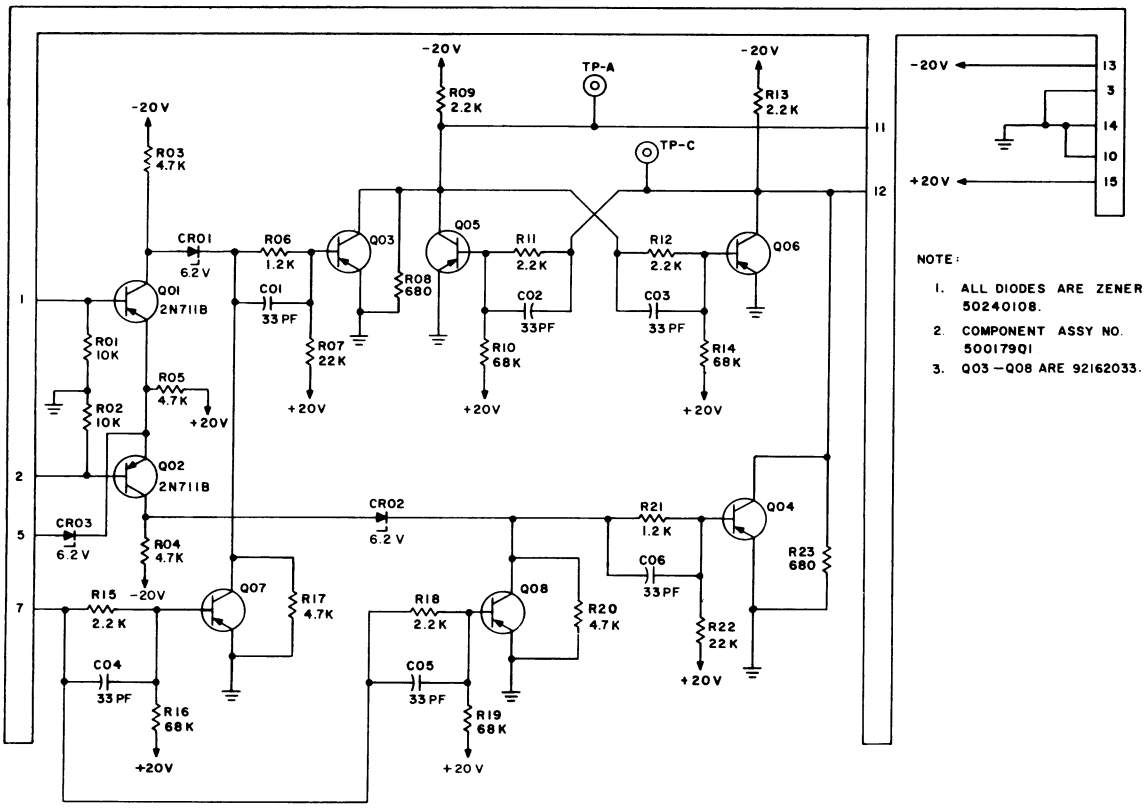
In normal operation, the Q01 and Q02 stage is the 3000 Interface receiver. With pin 5 at ground, transfer of the input at pins 1 and 2 to the flip-flop is controlled by the transfer pulse applied to pin 7. When pin 7 is at -3v or more negative, Q07 and Q08 are on, so Q03 and Q04 are turned off. Thus the flip-flop (Q05 and Q06) cannot be effected by Q01 and Q02, so it stays in its last previous state. When pin 7 goes to ground, Q07 and Q08 turn off. Then either Q03 or Q04 turns on (depending on the state of Q01 and Q02), and the state of pins 1 and 2 is transferred to pins 11 and 12. If pin 1 is more positive than pin 2, Q03 will turn on, and pin 11 will go to logical "0". Pin 12 will then be at logical "1". If pin 2 is more positive than pin 1, pin 11 will be at logical "1", and pin 12 at logical "0".

If pin 5 goes to -7v or more negative, Q01 and Q02 turn off, so the state of pins 1 and 2 cannot effect the EVB card. If pin 7 is at ground, Q03 and Q04 are turned on by CR01, CR02, R03, and R04. Both pin 11 and pin 12 will be at logical "0". If pin 7 is at -3v or more negative while pin 5 is at -7v or more negative, pins 11 and 12 will go into complementary states. However, either output could end up at logical "1" or logical "0".

Input (voltage)			Output (logic)	
State of pin 1 vs. pin 2	Pin 5	Pin 7	Pin 11	Pin 12
+	gnd	gnd	"0"	"1"
-	gnd	gnd	"1"	"0"
+ or -	gnd	-3v	last previous state	
+ or -	-7v	gnd	"0"	"0"
+ or -	-7v	-3v	complementary	

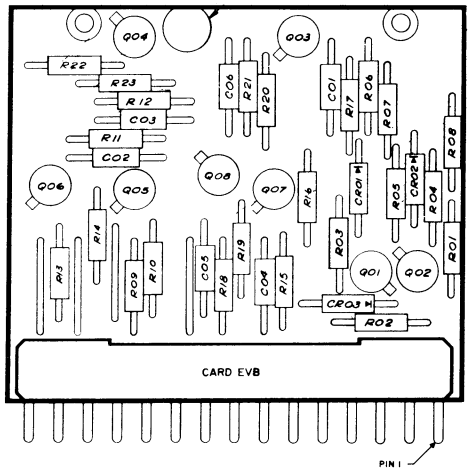
SYMBOL





NOTE:

1. ALL DIODES ARE ZENER 50240108.
2. COMPONENT ASSY NO. 5001790I
3. Q03 – Q08 ARE 92162033.



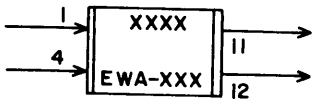
ZERO-CROSSING DETECTOR
EWA

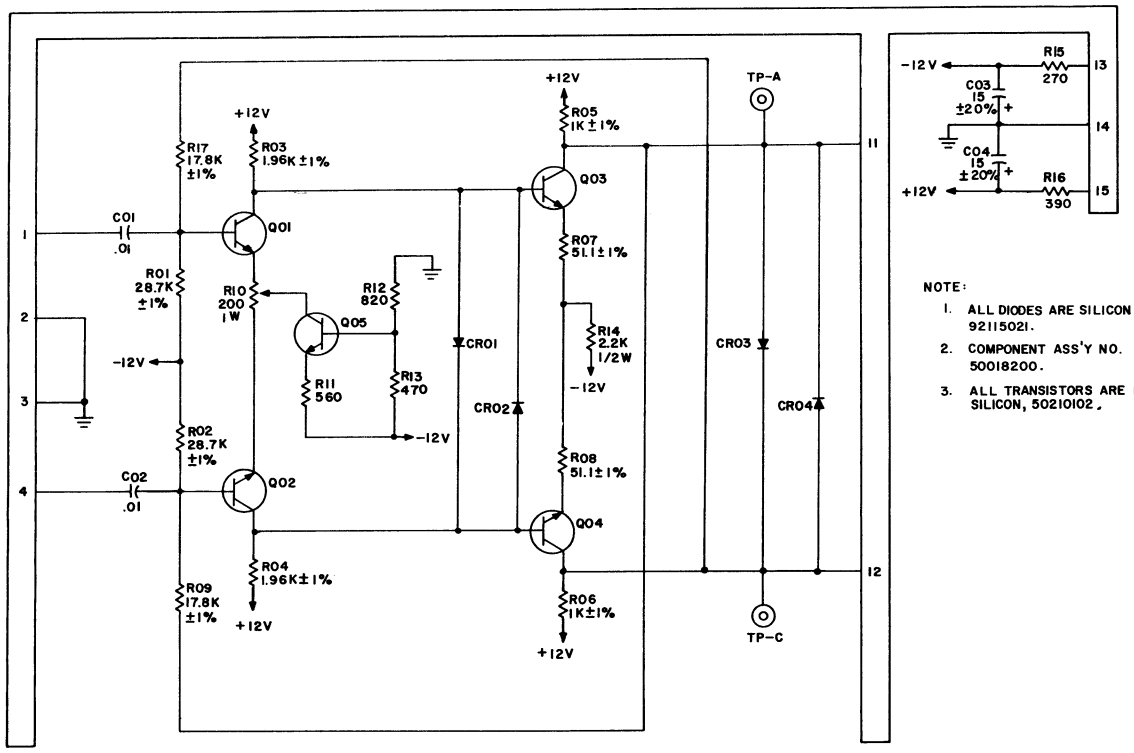
The EWA card detects zero-crossings of an input waveform. The output is a rectangular wave centered at +8v, which changes state whenever the input waveform goes through zero.

If the input is a differential signal, it is applied through C01 and C02 to the bases of Q01 and Q02. (The circuit could also be used to detect zero-crossings of a one-sided signal, by grounding the unused input pin.) If Q01 base is more positive than Q02 base, Q01 will turn on. This turns on CR02. If Q02 base goes more positive than Q01 base, Q02 and CR01 will turn on. The second differential pair, Q03 and Q04, sharpens up the resultant rectangular wave since the voltage gain is one. Either CR03 or CR04 is on so that the output between pin 11 and pin 12 is a rectangular wave of 0.6v, centered at +8v.

Internal voltages are isolated from the machine power supplies by R-C filters. Resistor R10 is adjusted for symmetrical operation over an amplitude range of input signals.

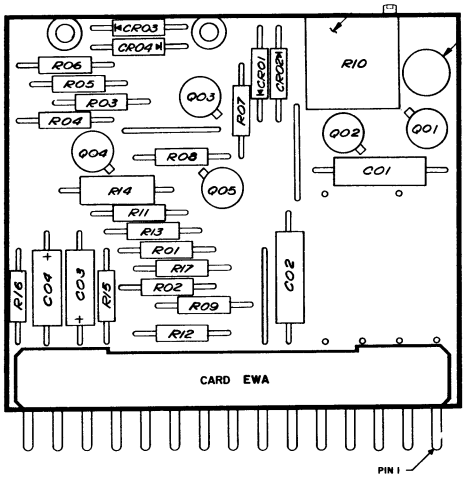
SYMBOL





NOTE:

1. ALL DIODES ARE SILICON 92115021.
2. COMPONENT ASS'Y NO. 50018200.
3. ALL TRANSISTORS ARE NPN, SILICON, 50210102.



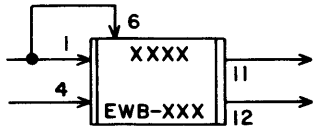
PEAK DETECTOR
EWB

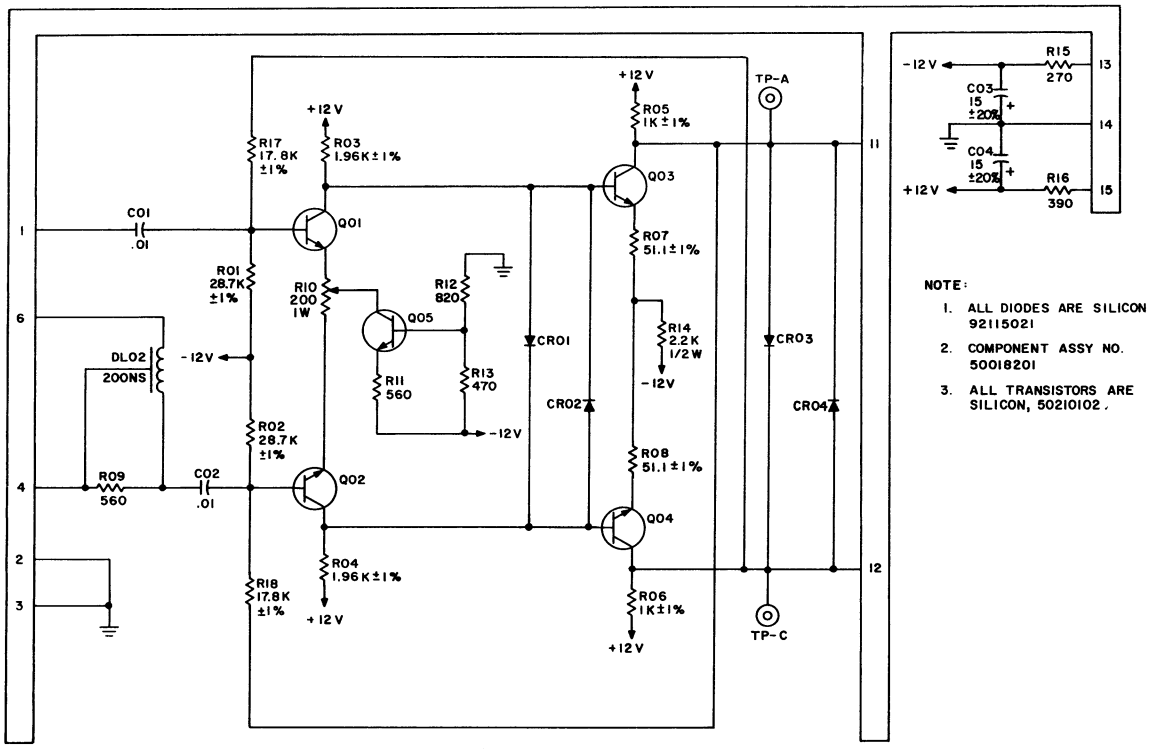
The EWB card detects peaks in read data; its output is a rectangular pulse.

The circuit uses a delay line and a differential amplifier to serve as a peak detector. The differential signal from a EUC card is applied to pins 1 and 4. The signal at pin 1 is applied directly through C01 to one base of the first differential stage. This signal is also delayed through DL02, then applied through C02 to the other base of the differential stage. The more positive base will turn on that transistor, and either CR01 and CR02 will be on. When the other base goes more positive, the other diode of the CR01 - CR02 pair will come on. The second differential stage sharpens up the resultant rectangular wave, since the voltage gain is one. Either CR03 or CR04 is on, so the output between pin 11 and pin 12 is a rectangular wave of 0.6v, centered around +8v.

Pins 1 and 6 must be tied together. Resistor R10 is adjusted for symmetrical operation over an amplitude range of input signals. The circuit tends to oscillate if the input frequency is greater than $\frac{1}{2\ (\text{delay time})}$.

SYMBOL

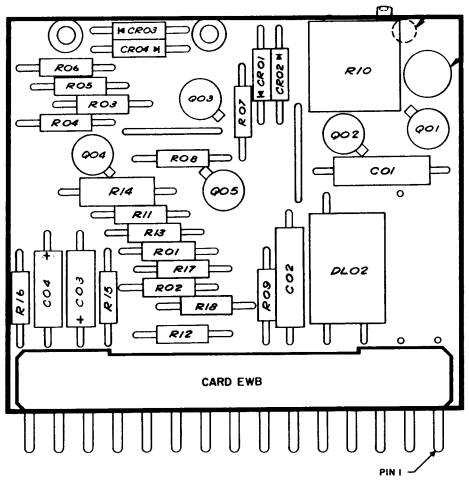




NOTE:

1. ALL DIODES ARE SILICON 92115021
2. COMPONENT ASSY NO. 50018201
3. ALL TRANSISTORS ARE SILICON, 50210102.

EWB



AGC ATTENUATOR

EZA

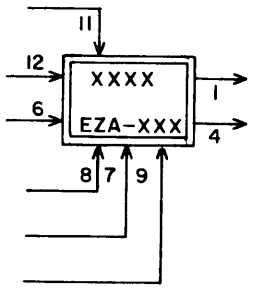
The EZA card attentuates the read signals applied to pins 11 and 12 in accordance with the control signal at pin 9, which comes from the FYA card. R07, R08, R09, and R10 present the proper load to the preceding card. Q03 and Q04 are emitter followers to reduce the load on the preceding card, and to present a low source impedance to CR01 and CR02.

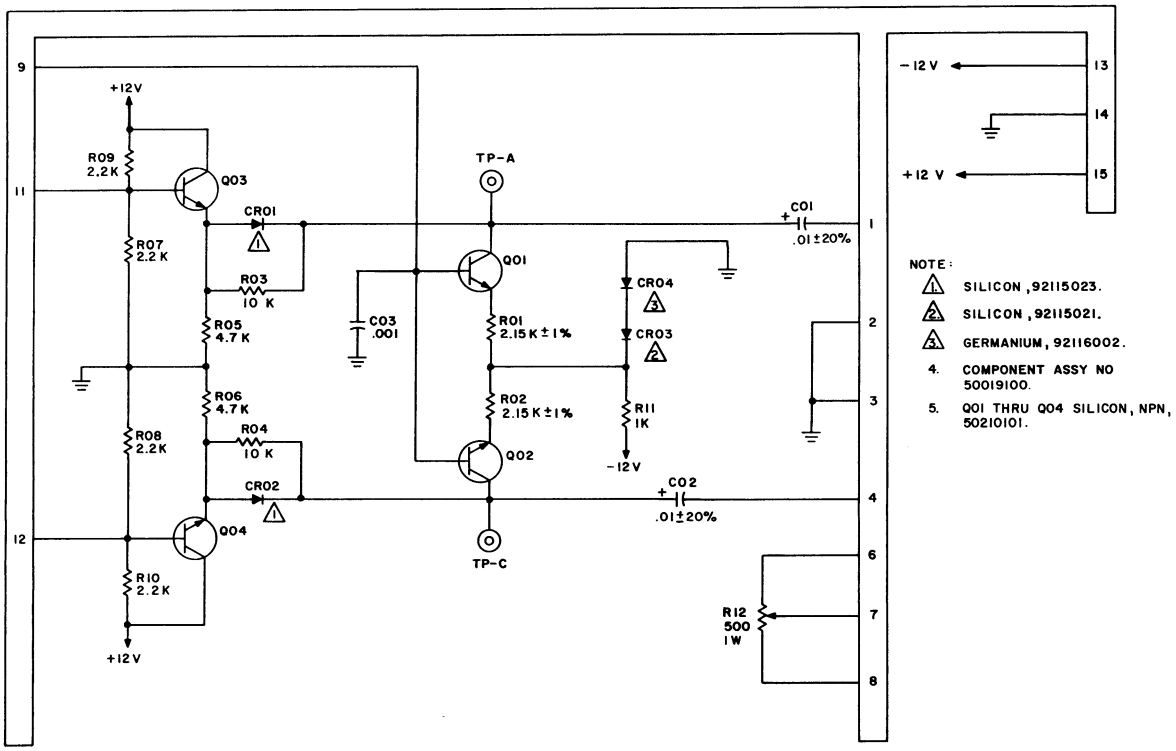
Q01 and Q02 control the bias current through CR01 and CR02 in accordance with the dc signal on pin 9. The dynamic impedance of CR01 and CR02 varies inversely with the bias current through them. When the dynamic impedance of the two diodes is large compared to the input impedance of the next card, the signal presented to the next card at pins 1 and 4 is small compared to the input signal at pins 11 and 12. When the dynamic impedance is small, the input signal is passed to the output pins unattenuated.

If the input signals are large, they may be distorted, since the impedance vs bias current curve of the diodes is not linear. If signals are on the order of 100 mv peak-to-peak, the distortion is minimized.

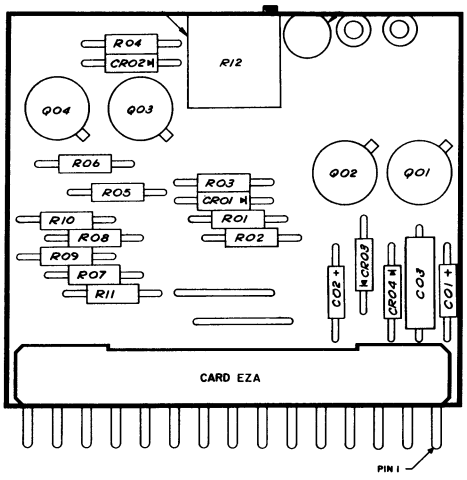
R12 is used at a different point in the 852 Disc Pak read chain.

SYMBOL




9
11
12
+12V
R09
2.2K
Q03
CR01
R07
2.2K
R03
10 K
R05
4.7 K
R06
4.7K
R08
2.2K
R04
10 K
CR02
Q04
R10
2.2K
+12V
TP-A
C03
.001
Q01
R01
2.15K±1%
R02
2.15K±1%
Q02
TP-C
CR04
CR03
R11
1K
-12V
C01
.01±20%
C02
.01±20%
1
2
3
4
6
7
8
R12
500
1W
-12 V
+12 V
13
14
15
NOTE:
1. SILICON, 92115023.
2. SILICON, 92115021.
3. GERMANIUM, 92116002.
4. COMPONENT ASSY NO 50019100.
5. Q01 THRU Q04 SILICON, NPN, 50210101.

EZA


R04
CR02
R12
Q04
Q03
R06
R05
R10
R08
R09
R07
R11
R03
CR01
R01
R02
Q02
Q01
C02
CR03
CR04
C03
C01
CARD EZA
PIN 1

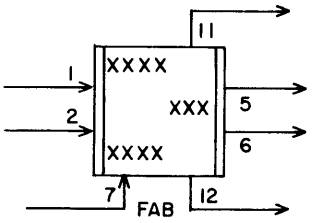
SHAPER FLIP-FLOP
FAB

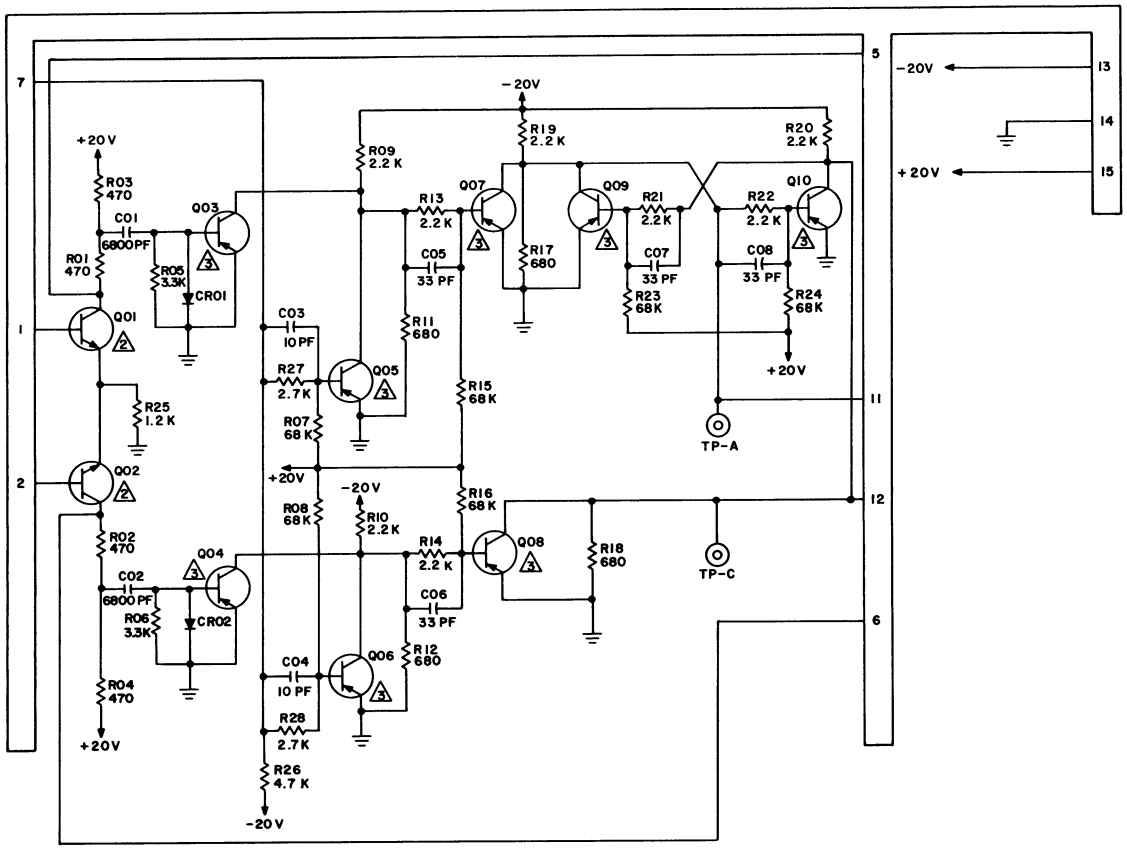
The FAB card transfers the EWA/B card output into a flip-flop, unless pin 7 is at logic one (-3V). Output pins do not have logic AND diodes.

The EWA/B card output, operating around +8v, is applied to pins 1 and 2. It is amplified and goes out on pins 5 and 6. It is also passed through C01 and C02, which cause Q03 or Q04 to turn on for negative-going edges. Positive going edges are dissipated in CR01 and CR02. The signals at the collectors of Q03 and Q04 are applied to Q07, Q08, Q09, and Q10, which constitute a flip-flop. Thus, each change of state at the output of the EWA/B card causes the flip-flop to change its state. Note that there are no AND diodes at the outputs from the flip-flop, pins 11 and 12.

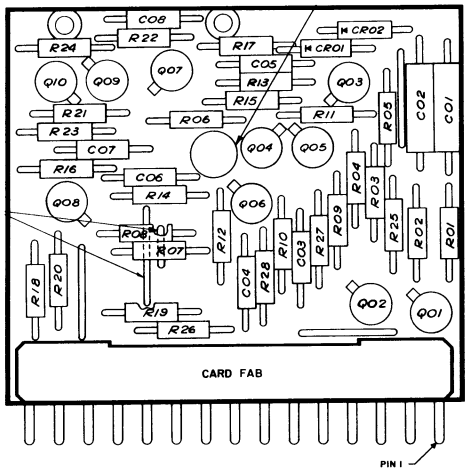
If pin 7 is at ground, the operation of the circuit is as described. If pin 7 is at -3V, Q05, and Q06 turn on, which keeps the flip-flop from responding to inputs on pins 1 and 2. Thus, pin 7 enables or disables the circuit.

SYMBOL




-20V
+20V
R09 2.2 K
R19 2.2 K
R20 2.2 K
R03 470
C01 6800 PF
Q03
R01 470
R05 3.3K
CR01
Q01
R25 1.2 K
Q02
R02 470
C02 6800 PF
R06 3.3K
CR02
Q04
R04 470
C03 10 PF
R27 2.7K
R07 68K
R08 68K
C04 10 PF
R28 2.7K
R26 4.7 K
Q05
Q06
R10 2.2 K
R11 680
R12 680
R13 2.2 K
C05 33 PF
R14 2.2 K
C06 33 PF
Q07
R17 680
R15 68K
R16 68K
Q08
R18 680
Q09
R21 2.2K
C07 33 PF
R23 68K
Q10
R22 2.2 K
C08 33 PF
R24 68K
TP-A
TP-C
5
7
1
2
11
12
6
13
14
15

FAB


C08
R24
R22
R17
CR02
CR01
C05
R13
R15
Q10
Q09
Q07
Q03
R21
R23
C07
R16
C06
R14
Q08
Q06
R06
R11
R05
C02
C01
Q04
Q05
R04
R03
R09
R12
R10
C03
R27
R25
R02
R01
R08
R07
C04
R28
R18
R20
R19
R26
Q02
Q01
CARD FAB
PIN 1

INNER AND OUTER TRACK SELECT AND SUMMING NETWORKS FCA, FCB

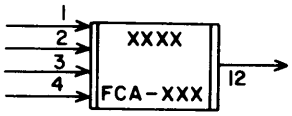
The FCA and FCB cards contain resistor networks which are used in the coarse control (long stroke) mode of the disk file servo actuator.

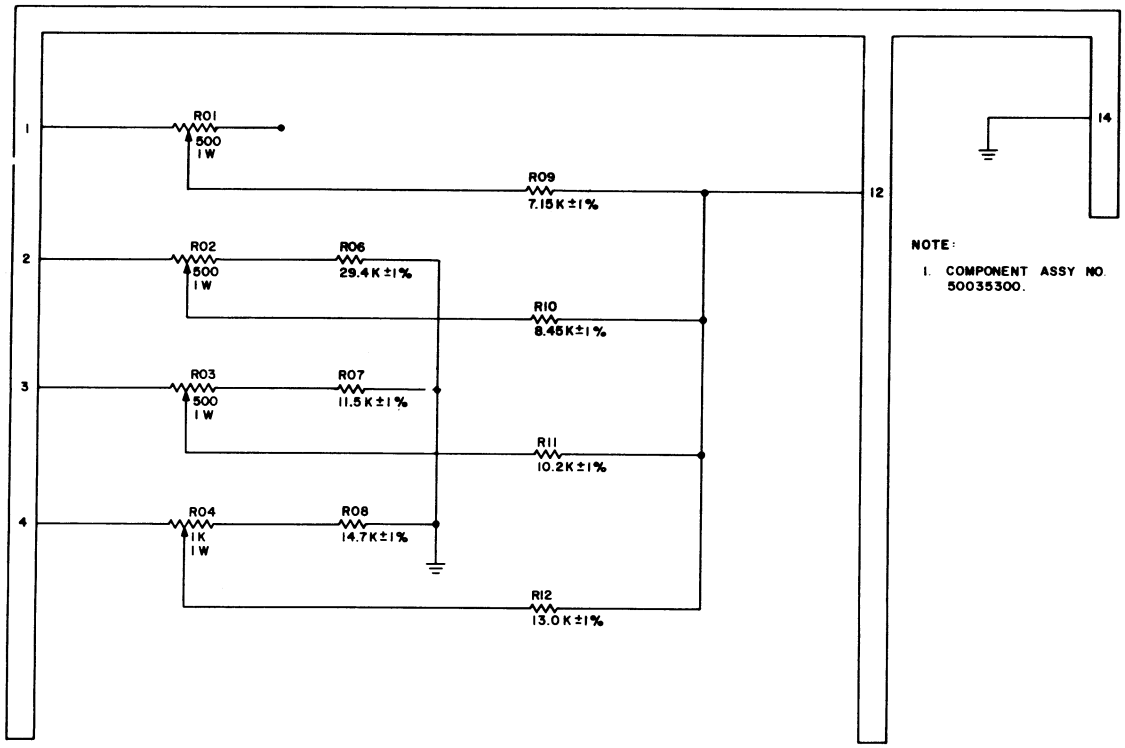
Each circuit has four input lines and one output line. The output line is common to all inputs via an appropriate resistor. This output line is normally connected to the summing point of the long stroke position operational amplifier. When a voltage of ±8v is applied from a JBA or JCA card to one of the input pins (1 through 4), a current flows through the resistor and into the summing point. The current level is trimmed by the appropriate potentiometer. This current represents the coarse command to the servo actuator for ultimate positioning at one of 14 locations.

The four farthest locations from the midpoint between locations 6 and 7 are termed "outer" tracks, and the three closest locations are termed "inner" tracks. The FCA card is used for the "outer" locations, and the FCB card for the "inner" locations.

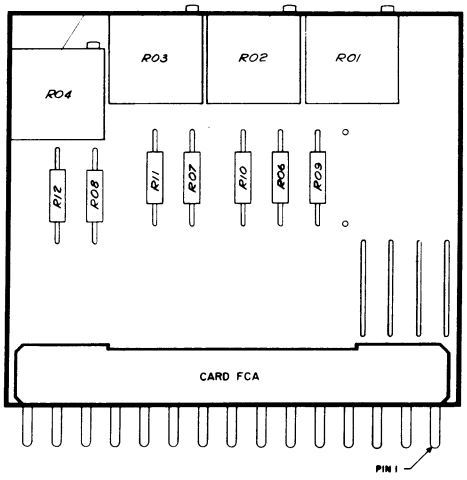
Pin number 4 on the FCB card is used for modifying the coarse control signal when positioning ±0.020 inches on either side of the 14 main locations. There are 3 tracks at each location.

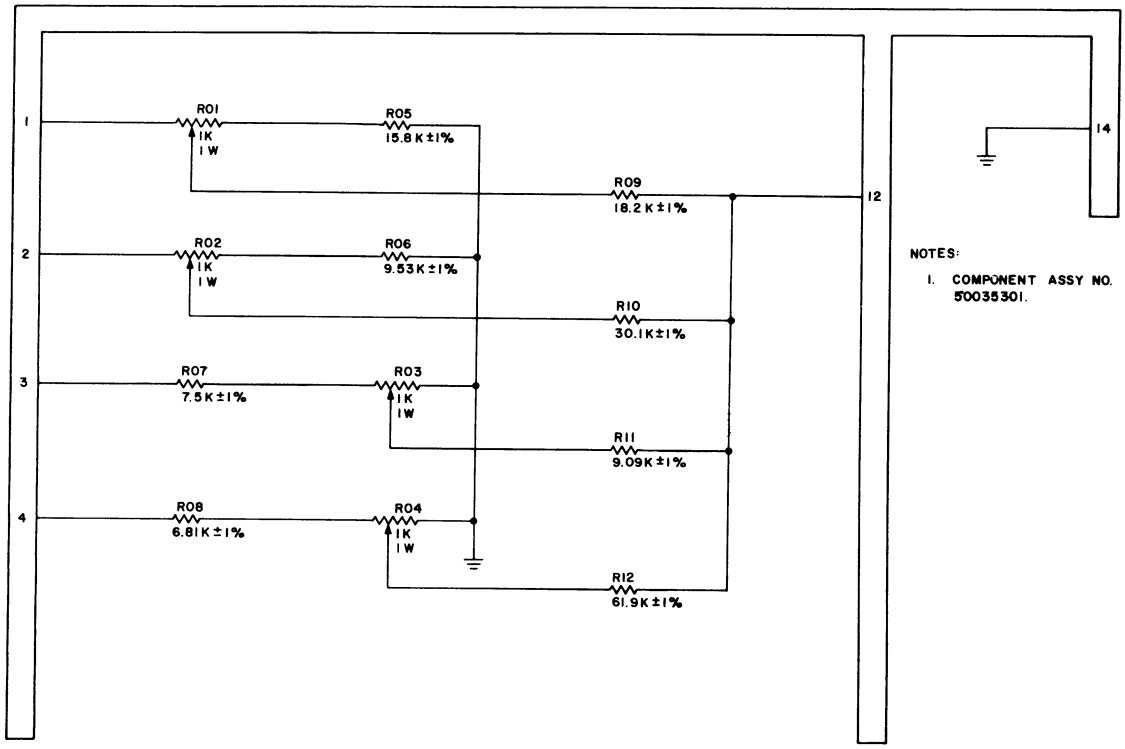
SYMBOL



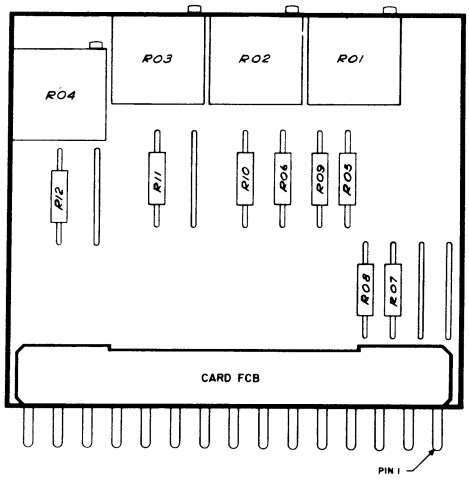

1
2
3
4
R01
500
1W
R02
500
1W
R03
500
1W
R04
1K
1W
R06
29.4K±1%
R07
11.5K±1%
R08
14.7K±1%
R09
7.15K±1%
R10
8.45K±1%
R11
10.2K±1%
R12
13.0K±1%
12
14
NOTE:
1. COMPONENT ASSY NO. 50035300.

FCA


R03
R02
R01
R04
R12
R08
R11
R07
R10
R06
R09
CARD FCA
PIN 1


1
2
3
4
R01
1K
1W
R05
15.8K±1%
R09
18.2K±1%
12
14
R02
1K
1W
R06
9.53K±1%
R10
30.1K±1%
R07
7.5K±1%
R03
1K
1W
R11
9.09K±1%
R08
6.81K±1%
R04
1K
1W
R12
61.9K±1%
NOTES:
1. COMPONENT ASSY NO. 50035301.

FCB


R03
R02
R01
R04
R12
R11
R10
R06
R09
R05
R08
R07
CARD FCB
PIN 1

OSCILLATOR
FDA

The FDA card provides a 10 KC signal which, when properly amplified, becomes the carrier for the long stroke and short stroke transducers in the disk file servo actuator. The 10 KC signal is also converted into a dc reference voltage for the servo.

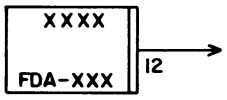
The oscillator contains an amplifying stage consisting of transistors Q01 and Q03. The output of Q03 goes to two other circuits; one containing a twin tee network and Q04, and the other containing another stage of amplification (Q02) and the amplitude regulating circuit (Q05).

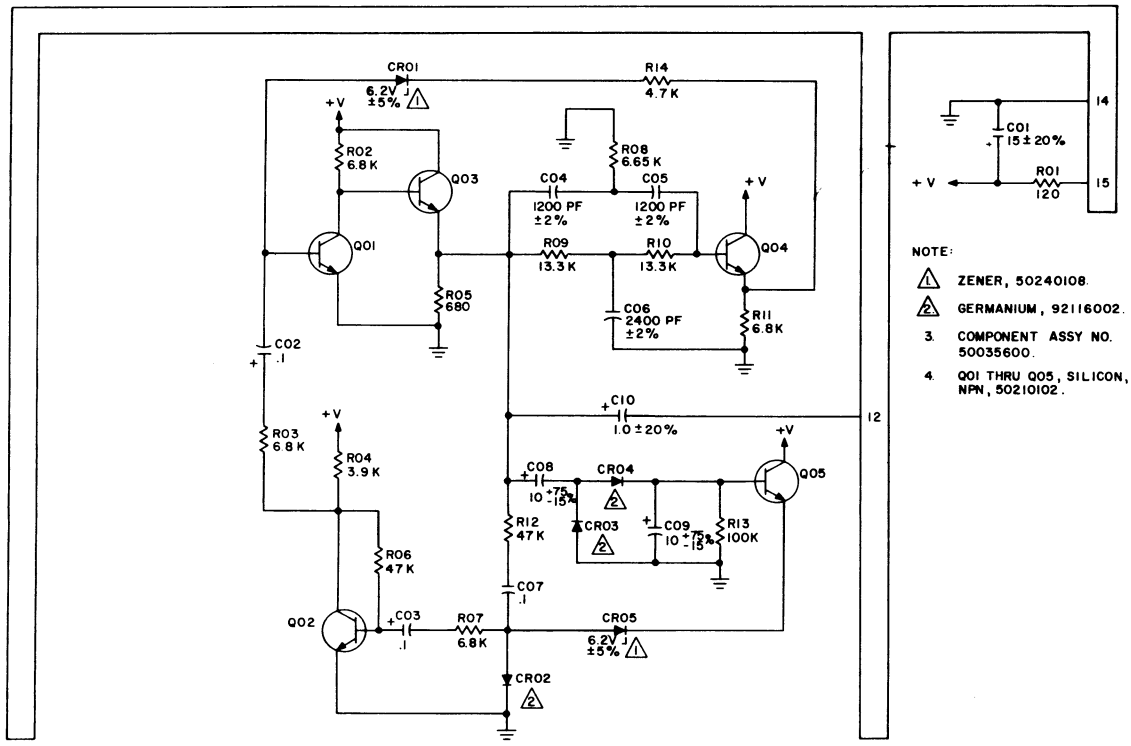
Positive feedback, which provides the necessary gain for oscillation, is provided by the two amplifying stages (Q01 and Q02). The frequency selective portion is provided by the negative feedback loop containing the twin tee, Q04, CR01, and R14. Zener diode CR01 provides dc coupling for stability.

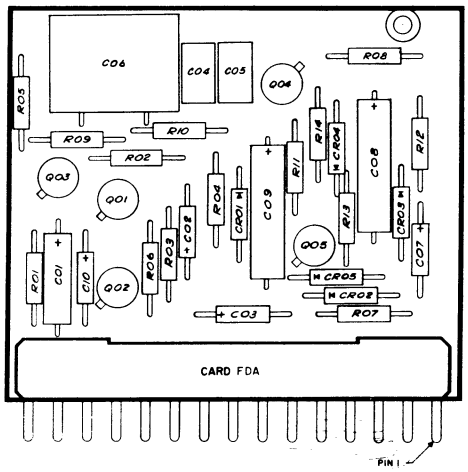
The twin tee has a null frequency of 10 KC. At this frequency no signal passes through the network, hence there is no negative feedback. At all other frequencies there is considerable negative feedback. The result of the two feedback paths is that there is positive feedback for 10 KC and negative feedback outside of a small band of frequencies as determined by the Q factor of the twin tee.

The amplitude regulating portion of the circuit consists of a voltage doubler (C08, C09, CR03, and CR04), and the emitter follower (Q05). The signal from Q03 is fed to Q02 via R12, C07, CR02, and the base network (C03 and R07). If diode CR02 is biased more or less, its impedance is decreased or increased, and therby controls the signal into Q02. The diode current is the emitter current of Q05 and is controlled by the base voltage, which is proportional to the signal. Therefore, if the output voltage rises, the base voltage and emitter current of Q05 increases. Diode CR02 current goes up and its impedance goes down. Consequently, the portion of the signal to Q02 goes down, which lowers the drive to Q01 and brings the output back down to the controlled level. This level is established by diode drop CR02, zener diode CR05, and the base-emitter drop of Q05. This is approximately 7v at the base of Q05, which is twice the peak output voltage.

SYMBOL


XXXX
FDA-XXX
12


CR01
6.2V ±5%
R14
4.7K
+V
R02
6.8K
Q03
R08
6.65K
C04
1200 PF ±2%
C05
1200 PF ±2%
+V
Q01
R09
13.3K
R10
13.3K
Q04
R05
680
C06
2400 PF ±2%
R11
6.8K
C02
.1
+C10
1.0 ±20%
12
+V
R03
6.8K
R04
3.9K
C08
10 +75 -15%
CR04
+V
Q05
R12
47K
CR03
C09
10 +75 -15%
R13
100K
R06
47K
C07
.1
Q02
C03
.1
R07
6.8K
CR05
6.2V ±5%
CR02
14
C01
15 ±20%
+V
R01
120
15
NOTE:
1. ZENER, 50240108.
2. GERMANIUM, 92116002.
3. COMPONENT ASSY NO. 50035600.
4. Q01 THRU Q05, SILICON, NPN, 50210102.


C06
C04
C05
Q04
R08
R05
R10
R09
R02
Q03
Q01
R04
C08
C09
R11
R14
CR04
R12
R13
CR03
C07
C01
R01
C10
Q02
R06
R03
CR01
CR05
CR02
C03
R07
CARD FDA
PIN 1

CLAMP AND SUMMING

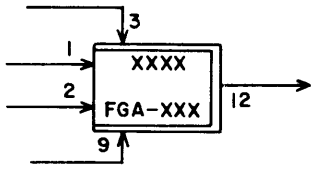
FGA

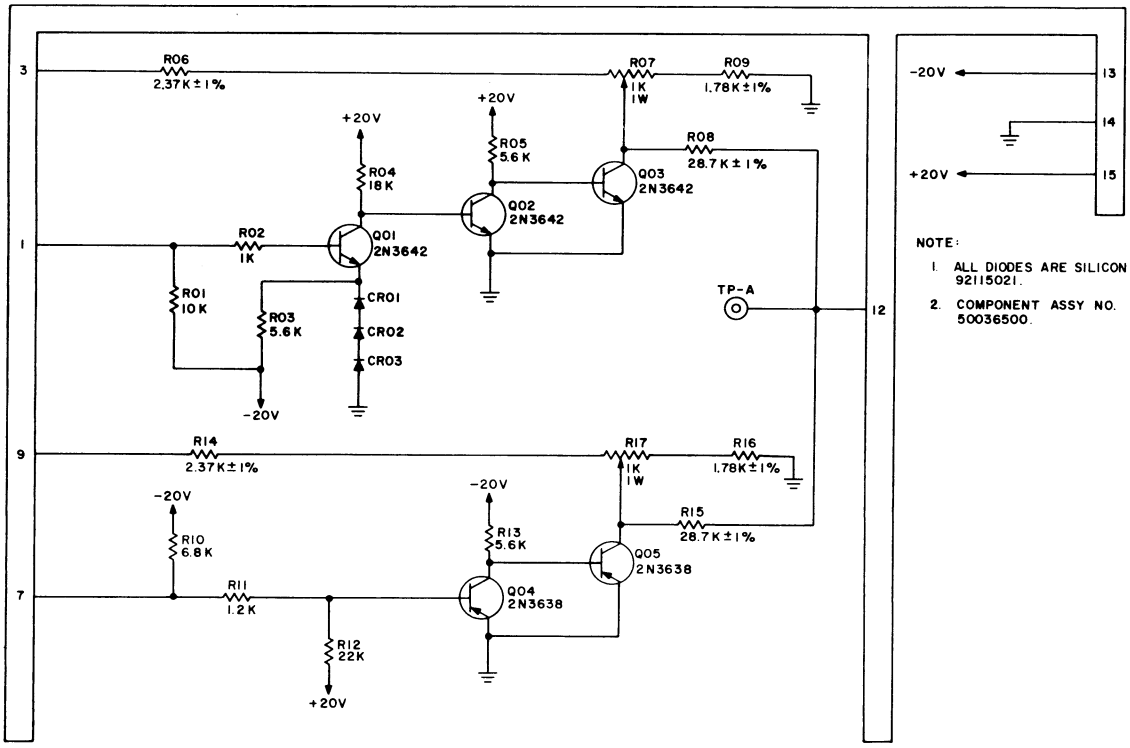
The FGA card is used in the disk file servo actuator fine control (short stroke) loop. The card provides a current, which is summed with the short stroke signal, to position the output ±0.020 inches on either side of a main track.

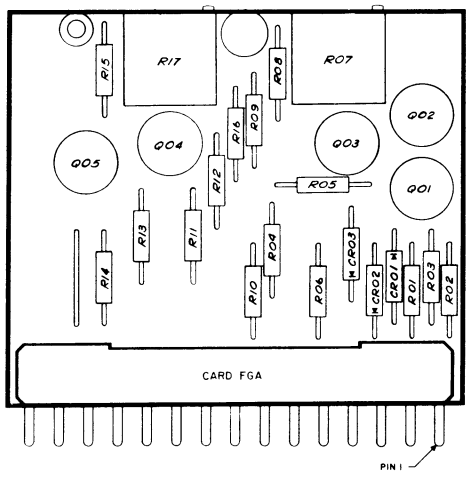
The circuit is provided with reference voltages of plus and minus 8v at pins 3 and 9 respectively. The output is taken from pin 12 and normally goes to the summing point, or virtual ground, of the short stroke operational amplifier. The output is a plus or minus short circuit current of approximately 125 ua, depending on whether Q03 or Q05 is on. A logical "1" on pin 1 turns Q01 off, Q02 on, and Q03 off, giving a plus current out. A logical "1" on pin 2 turns Q04 on and Q05 off, giving a minus current out.

Trimmer potentiometers R07 and R17 provide adjustment of the current, so the ±0.020 inches will be realized.

SYMBOL




3
1
9
7
12
R06
2.37K±1%
R07
1K
1W
R09
1.78K±1%
+20V
R04
18K
R05
5.6K
R08
28.7K±1%
Q03
2N3642
Q02
2N3642
Q01
2N3642
R02
1K
R01
10K
R03
5.6K
CR01
CR02
CR03
-20V
TP-A
R14
2.37K±1%
R17
1K
1W
R16
1.78K±1%
R15
28.7K±1%
R10
6.8K
R13
5.6K
Q05
2N3638
Q04
2N3638
R11
1.2K
R12
22K
-20V
+20V
13
14
15
NOTE:
1. ALL DIODES ARE SILICON 92115021.
2. COMPONENT ASSY NO. 50036500.


R15
R17
R08
R07
R16
R09
Q02
Q04
Q03
Q05
R12
R05
Q01
R13
R11
R04
CR03
R14
R10
R06
CR02
CR01
R01
R03
R02
CARD FGA
PIN 1

VALVE AMPLIFIER
FHA

The FHA card is used in conjunction with a FMA card. They provide the control current to the short and long stroke valves in the disk file servo actuator.

The circuit is a feedback amplifier when used with the FMA card and the loop is closed with the valve. The valve is connected to pin 4 on the FHA card, and pin 6 on the FMA card. Pins 11 and 12 connect to pins 1 and 2 respectively on the FMA card. The closed loop current gain is 91 ma as given by the ratio of R12 to R13. Therefore, a voltage at pin 1 of $\pm$6.8v peak will give a 1 ma input current. This will cause the current through the valve to be approximately 91 ma.

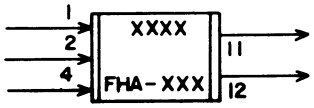
The circuit consists of the differential input stage, using a matched pair of transistors in a single TO-5 case. Potentiometer R03 allows the output current to be set at zero. Voltage applied to R03 is regulated by zener diodes CR01 and CR02. Therefore, no drift is introduced at this point. Transistors Q03 and Q04 are a Darlington pair in a common emitter circuit, whose collector load is the FMA card input impedance.

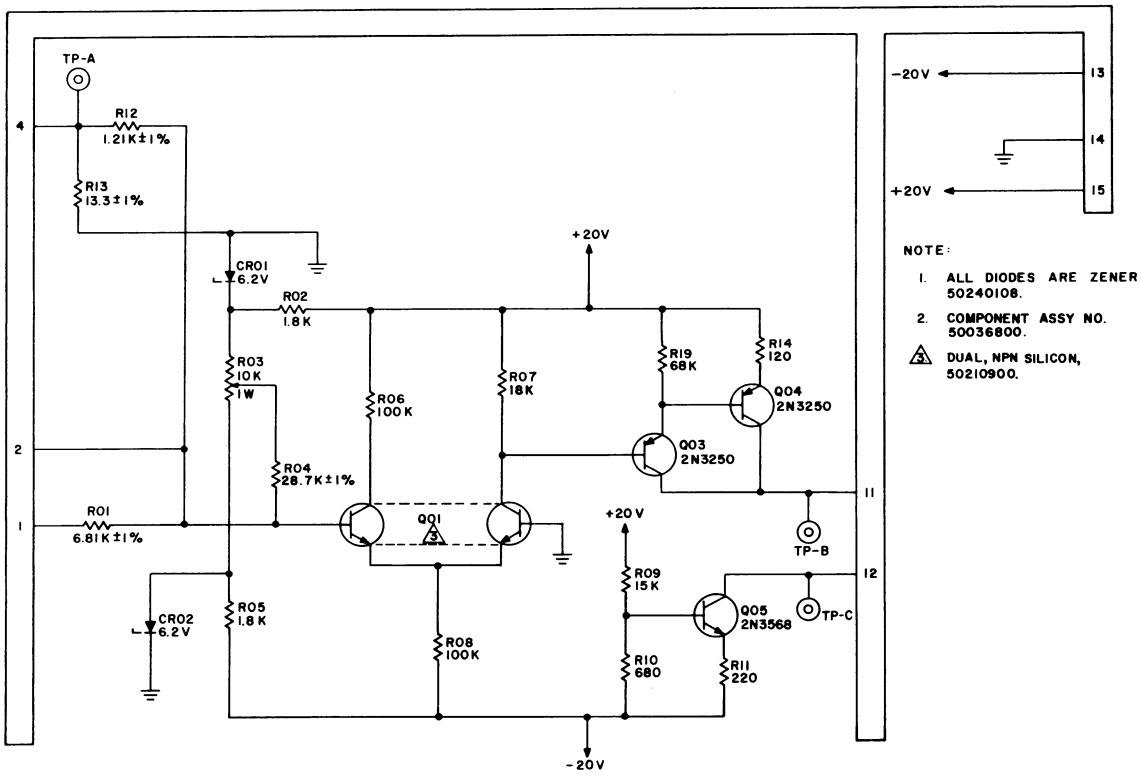
Transistor Q05 is a constant current generator, which supplies 5.2 ma nominally to diodes CR01 and CR02 on the FMA card. These diodes bias transistors Q01 and Q02 on the FMA card for class AB operation. By means of R03, the base drives to Q01 and Q02 (FMA) are adjusted to give a zero output. The current out of pin 11 is now equal to the current into pin 12 (assuming the transistors on card FMA are matched). If the input is driven positive, pin 11 goes positive and the collector current will increase on Q04. Since the current generator current is constant, the excess above 5.2 ma goes into positive drive for Q01 on the FMA card.

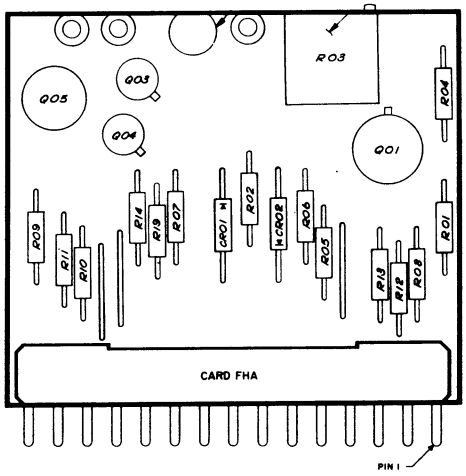
To obtain negative swings, the collector current on Q04 is reduced below 5.2 ma. Since Q05 requires 5.2 ma, the deficiency is made up by pulling current from ground through the base-emitter on card FMA.

For this combination of cards, the feedback is taken from a voltage proportional to the output current. As a result, the current through the valve will be sinusoidal for a sine wave input, but the voltage out of the FMA card will be determined by the load impedance. In this case the valve is a nonlinear inductor, so the voltage is very distorted.

SYMBOL


1
2
4
XXXX
FHA-XXX
11
12


TP-A
R12
1.21K±1%
R13
13.3±1%
CR01
6.2V
R02
1.8K
R03
10K
1W
R04
28.7K±1%
R01
6.81K±1%
CR02
6.2V
R05
1.8K
R06
100K
R07
18K
R08
100K
Q01
+20V
R19
68K
R14
120
Q04
2N3250
Q03
2N3250
+20V
R09
15K
Q05
2N3568
R10
680
R11
220
TP-B
TP-C
-20V
-20V
+20V
13
14
15
11
12
NOTE:
1. ALL DIODES ARE ZENER 50240108.
2. COMPONENT ASSY NO. 50036800.
3. DUAL, NPN SILICON, 50210900.


Q05
Q03
Q04
R03
R04
Q01
R09
R11
R10
R14
R13
R07
CR01
R02
CR02
R06
R05
R13
R12
R08
R01
CARD FHA
PIN 1

POWER AMPLIFIER
FIA

This card is used with the output stage of the FMA card to form a 10 KC power amplifier. The FIA card is basically the same as the FHA card. However, it does not have a zero adjustment, and the feedback loop is modified to sense output voltage instead of current.

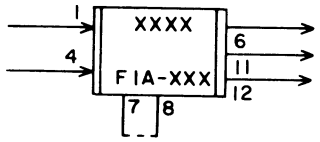
Pins 11 and 12 connect to pins 1 and 2 respectively on the FMA card. The output pin 6 of the FMA card connects to pin 4, and the output is taken off pin 6 (FIA). The load will be either a short stroke transducer and bridge rectifier, or a long stroke transformer and bridge rectifier. When the short stroke transducer load is used, it is necessary to jumper pins 7 and 8.

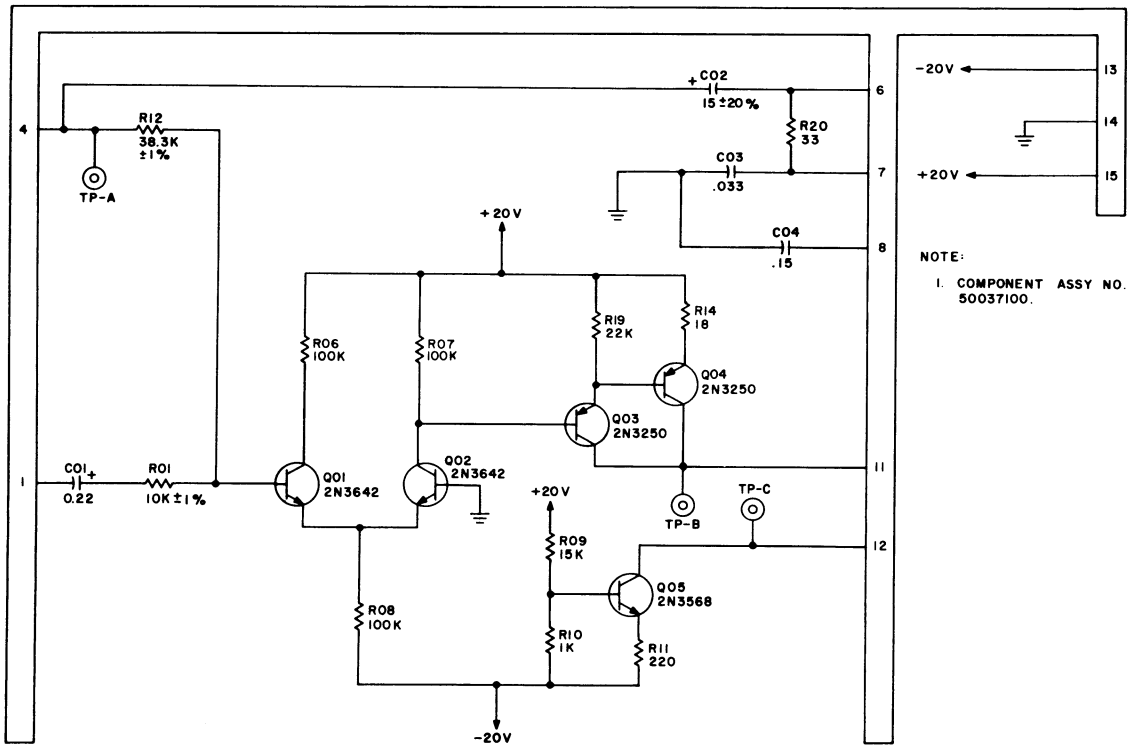
The circuit is a feedback amplifier with a voltage gain of 3.83v as determined by the ratio of R12 to R01. The 10 KC oscillator (card FDA) supplies approximately 3.5v peak to this circuit, so the output will be 13.4v peak. Since the circuit is ac coupled, a zero adjustment feature is not necessary.

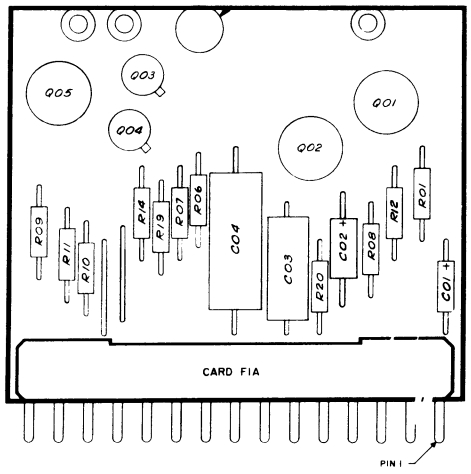
The circuit consists of a differential amplifier, transistors Q01 and Q02, and a Darlington pair (Q03 and Q04) in a common emitter configuration. These stages provide the necessary open loop gain. A current generator (Q05) is used to supply approximately 8.7 ma nominally to the FMA card diodes CR01 and CR02. These diodes bias transistors Q01 and Q02 (card FMA) for class AB operation. When the input voltage at pin 1 swings -3.5v, transistors Q03 and Q04 are driven so the collector current is greater than 8.7 ma. Since Q05 can only pass 8.7 ma, the excess becomes base drive for transistor Q01 (card FMA) and the output goes to +13.4v. If the input swings +3.5v, transistors Q03 and Q04 are driven less, so the collector current goes below 8.7 ma. However, Q05 still requires 8.7 ma, so the deficiency is made up by pulling current from ground through the transistor Q02 base-emitter junctions (card FMA). The output then goes to -13.4v.

The load on the FIA/FMA combination can be approximately 30v peak-to-peak into 150 ohms.

SYMBOL


1
4
XXXX
FIA-XXX
6
11
12
7
8


+C02
15 ±20%
R12
38.3K
±1%
TP-A
R20
33
C03
.033
C04
.15
+20V
-20V
13
14
15
NOTE:
1. COMPONENT ASSY NO. 50037100.
R19
22K
R14
18
R06
100K
R07
100K
Q04
2N3250
Q03
2N3250
C01+
0.22
R01
10K ±1%
Q01
2N3642
Q02
2N3642
TP-B
TP-C
R09
15K
Q05
2N3568
R08
100K
R10
1K
R11
220


Q05
Q03
Q04
Q01
Q02
R09
R11
R10
R14
R19
R07
R06
C04
C03
R20
C02+
R08
R12
R01
C01+
CARD FIA
PIN 1

SERVO CYCLING GENERATOR

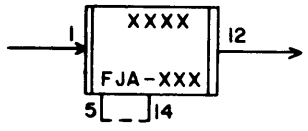
FJA

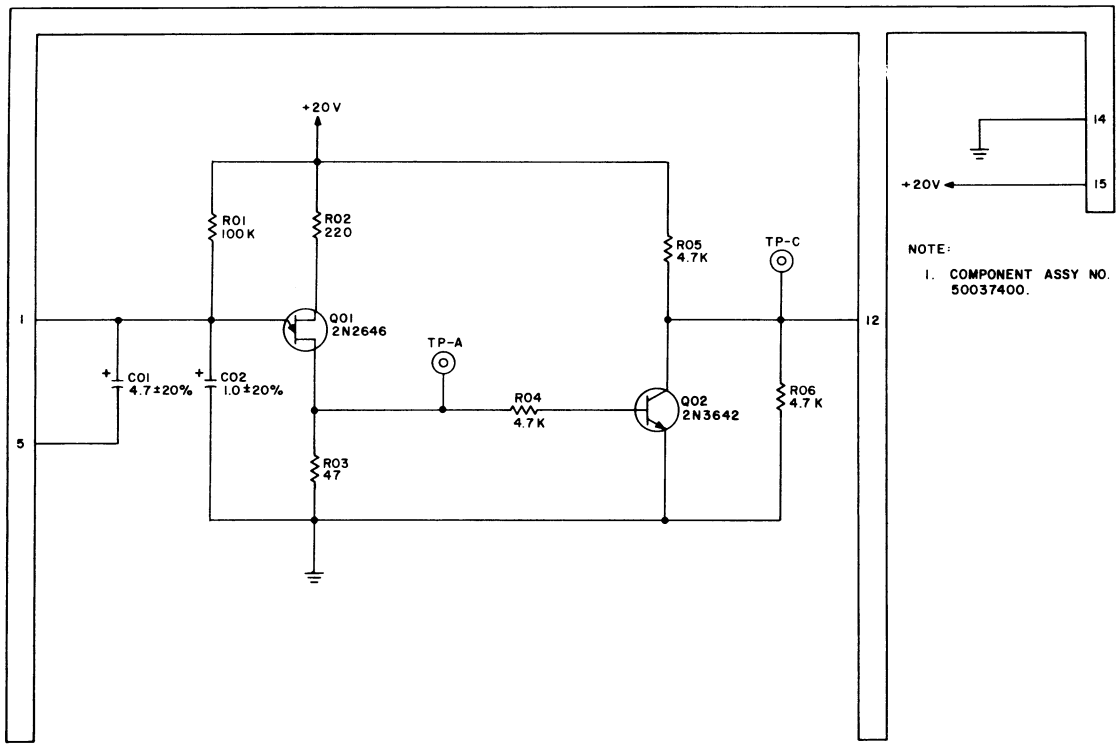
The FJA card is used to drive an OLA flip-flop card. The card generates a series of pulses for cycling the disk file servo actuator. This is necessary for maintenance purposes.

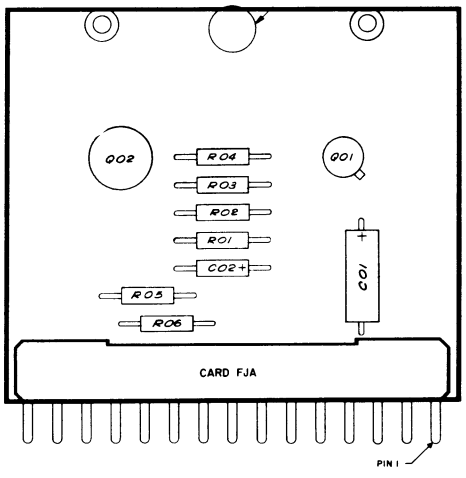
If input pin 1 is held at ground, unijunction transistor Q01 and transistor Q02 will be off. The output will be 10v.

When the input is opened, capacitor C02 (or C01 and C02 in parallel with pin 5 grounded) charges positive until a voltage of approximately 10v is reached. At this time the unijunction will fire, discharging the capacitor via the emitter to base 1 diode of Q01 and resistor R03. A positive pulse occurs across R03 which turns on Q02, driving the output from 10v to ground. The cycle will repeat as long as the input is open. The output is a series of negative going pulses approximately 50 to 100 usec wide. The pulses are spaced either 100 or 600 msec, depending on whether C02 is used, or C01 and C02 are used by grounding pin 5.

SYMBOL




+20V
R01
100K
R02
220
R05
4.7K
TP-C
Q01
2N2646
TP-A
C01
4.7±20%
C02
1.0±20%
R04
4.7K
Q02
2N3642
R06
4.7K
R03
47
1
5
12
14
15
+20V
NOTE:
1. COMPONENT ASSY NO. 50037400.


Q02
R04
R03
R02
R01
C02+
R05
R06
Q01
C01
CARD FJA
PIN 1

DEMODULATOR

FKA

The FKA card is used to convert an amplitude modulated 10 KC into a varying dc signal. This signal represents either coarse or fine position signals for the disk file servo actuator.

The input signal comes from either the short stroke or long stroke transducer. The transducer center tap goes to ground and the ends connect to pins 8 and 9. The output pin (pin 1) goes to the summing point of an operational amplifier.

When the short stroke or long stroke transducers are nulled, the voltage at pins 8 and 9 are equal in magnitude and opposite in phase. The voltages are applied to transformers T01 and T02, and are full wave rectified by the rectifiers in DA01. The voltage at test point A is then full wave positive, and at test point C full wave negative. Therefore, the output is at zero.

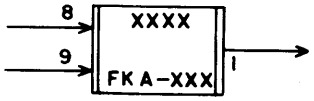
If the transducers are not nulled so the voltage at pin 8 is greater than at pin 9, the voltage at test point A is positive and greater by $+\Delta E$ than it was at null. At test point C the voltage is negative and less in magnitude (i.e. $+\Delta E$) than it was at null. The effect is that $+2\Delta E$ is realized across 10 K, or an equivalent of ΔE across 5 K.

A filter composed of L01 and C01 has a cutoff frequency of approximately 1 KC to filter out the carrier and its harmonies, but pass dc and the modulation frequencies.

The circuit delivers approximately ± 1.4 ma maximum.

NOTE: This card requires two card slots.

SYMBOL



BRIDGE RECTIFIER

FLA, FLB

The FLA and FLB cards provides a dc reference voltage to the long stroke and short stroke loops of the disk file servo actuator. The short circuit current is approximately 1.6 ma.

A 10 KC, 10 VRMS signal is applied to pins 1 and 2, and is full wave rectified by diodes CR01 through CR04. The LC filter converts the rectified wave to dc.

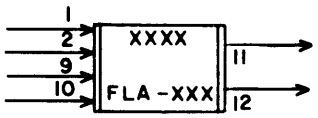
The FLA card uses a matched diode quad to obtain stability of the dc. Resistors R01 and R02 are part of the feedback network for the reference amplifier card (FPA). Diodes between pins 9 and 11, and pins 10 and 12, are used in the feedback network. They compensate for temperature effects in the rectifiers.

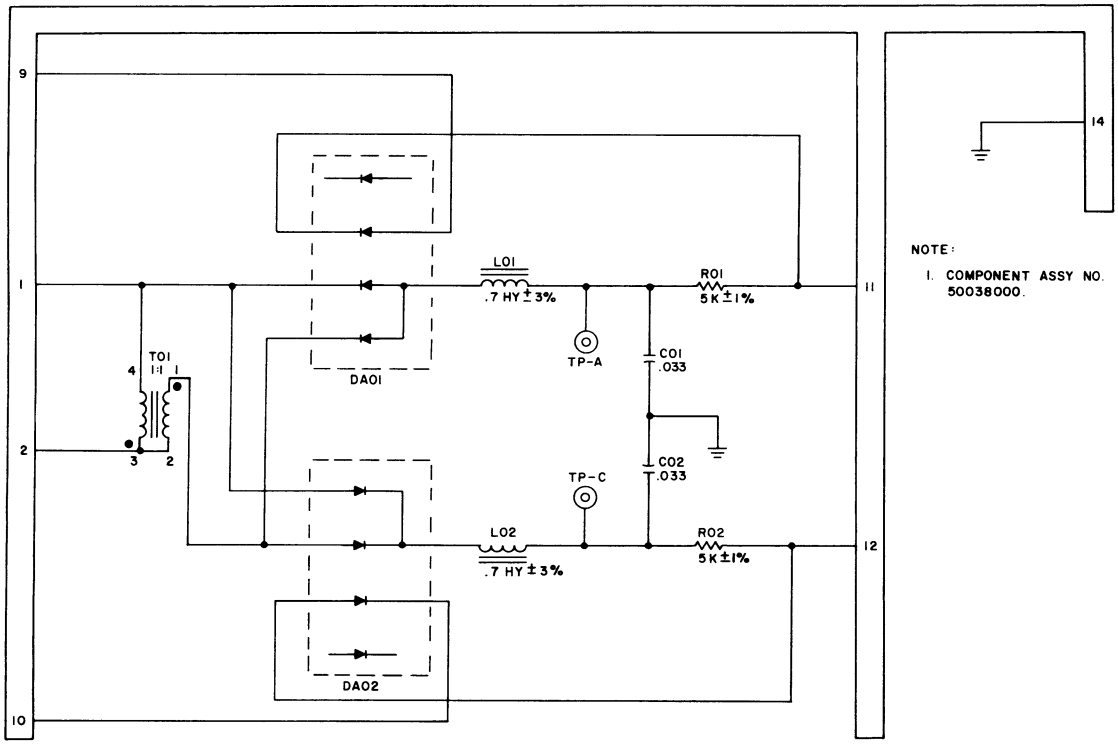
When used to drive a reference amplifier card (FPA), pin 11 connected to pin 1 on the FPA card will result in a plus reference voltage. Pin 9 must be connected to pin 2 on the FPA card to close the feedback loop. If a minus reference voltage is desired, pin 12 is connected to pin 1 (card FPA), and pin 10 is connected to pin 2 (card FPA) to close the feedback loop.

The FLB card does not contain the diodes between pins 9 and 11, and pins 10 and 12. Also, resistors R01 and R02 are replaced with jumpers. Pins 11 and 12 are connected to the load (card FGA, pins 9 and 3 respectively).

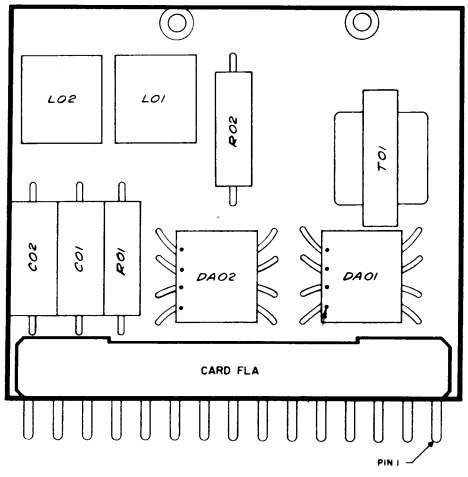
NOTE: This card requires two card slots.

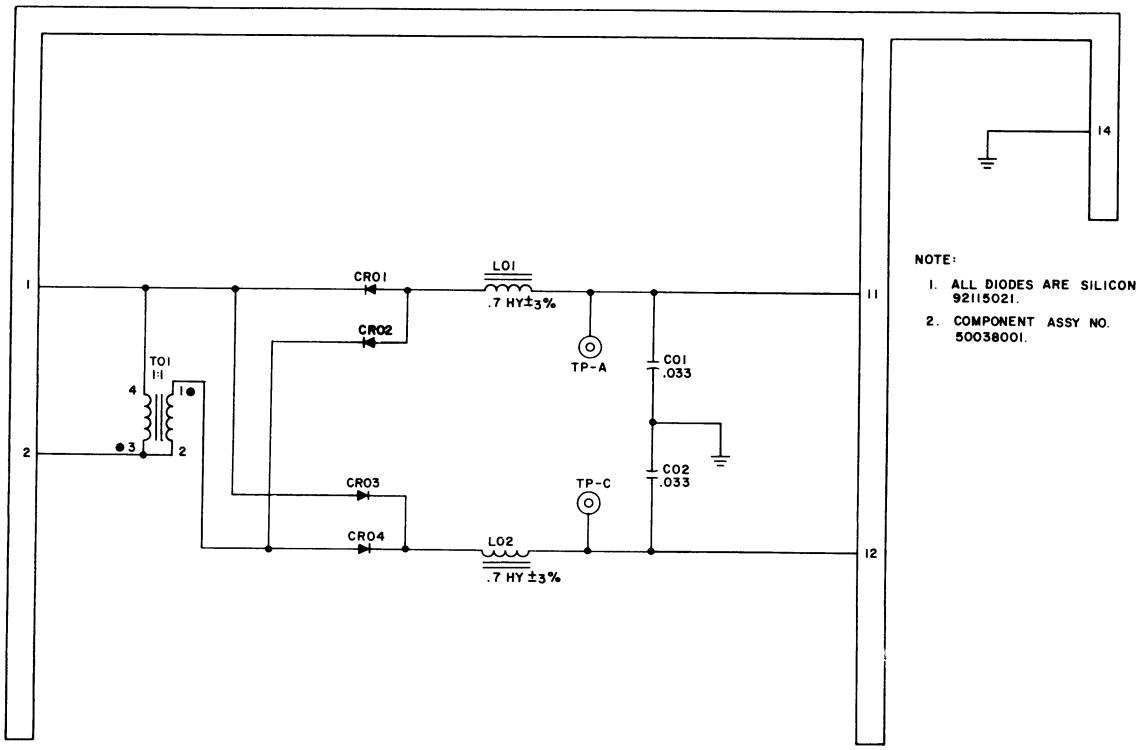
SYMBOL



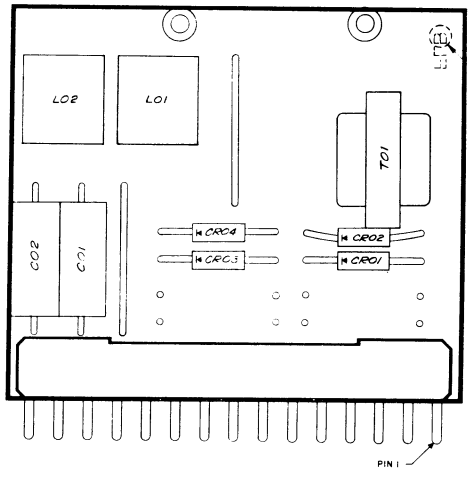

9
1
2
10
11
12
14
LO1
.7 HY ± 3%
RO1
5K ± 1%
TO1
1:1
4
3
2
DAO1
TP-A
CO1
.033
CO2
.033
TP-C
LO2
.7 HY ± 3%
RO2
5K ± 1%
DAO2
NOTE:
1. COMPONENT ASSY NO. 50038000.

FLA


LO2
LO1
RO2
TO1
CO2
CO1
RO1
DAO2
DAO1
CARD FLA
PIN 1


14
NOTE:
1. ALL DIODES ARE SILICON 92115021.
2. COMPONENT ASSY NO. 50038001.
1
2
11
12
CR01
CR02
CR03
CR04
L01
.7 HY±3%
L02
.7 HY ±3%
T01
1:1
4
1
3
2
TP-A
TP-C
C01
.033
C02
.033

FLB


L02
L01
T01
CR04
CR03
CR02
CR01
C02
C01
PIN 1

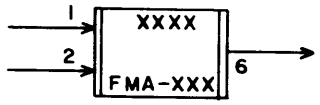
POWER AMPLIFIER OUTPUT STAGE

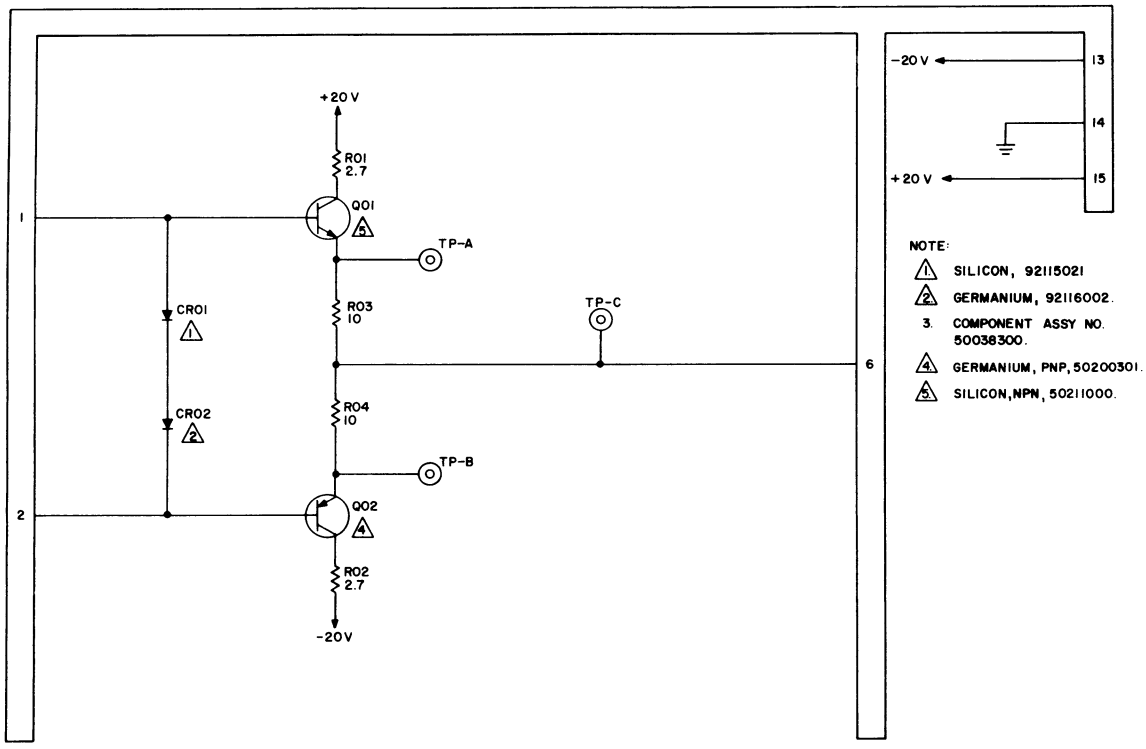
FMA

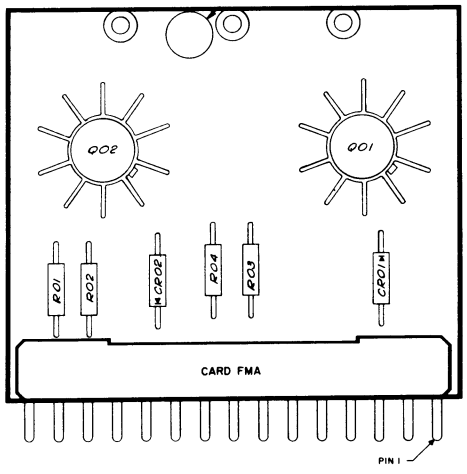
This card is used as the output stage for the FHA, FIA, or FLA/B cards as used in the disk file servo actuator.

Transistors Q01 and Q02 are direct-coupled emitter followers, with the load connected to pin 6 and operating approximately class AB as used with the FHA or FIA cards. For a further description of the input bias and output load conditions, refer to the descriptions of the FHA and FIA cards.

SYMBOL




+20 V
R01
2.7
Q01
TP-A
CR01
R03
10
TP-C
CR02
R04
10
TP-B
Q02
R02
2.7
-20V
1
2
6
-20 V
+20 V
13
14
15
NOTE:
1. SILICON, 92115021
2. GERMANIUM, 92116002.
3. COMPONENT ASSY NO. 50038300.
4. GERMANIUM, PNP, 50200301.
5. SILICON, NPN, 50211000.

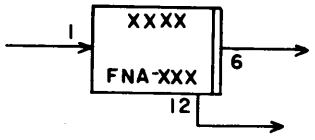

Q02
Q01
R01
R02
CR02
R04
R03
CR01
CARD FMA
PIN 1

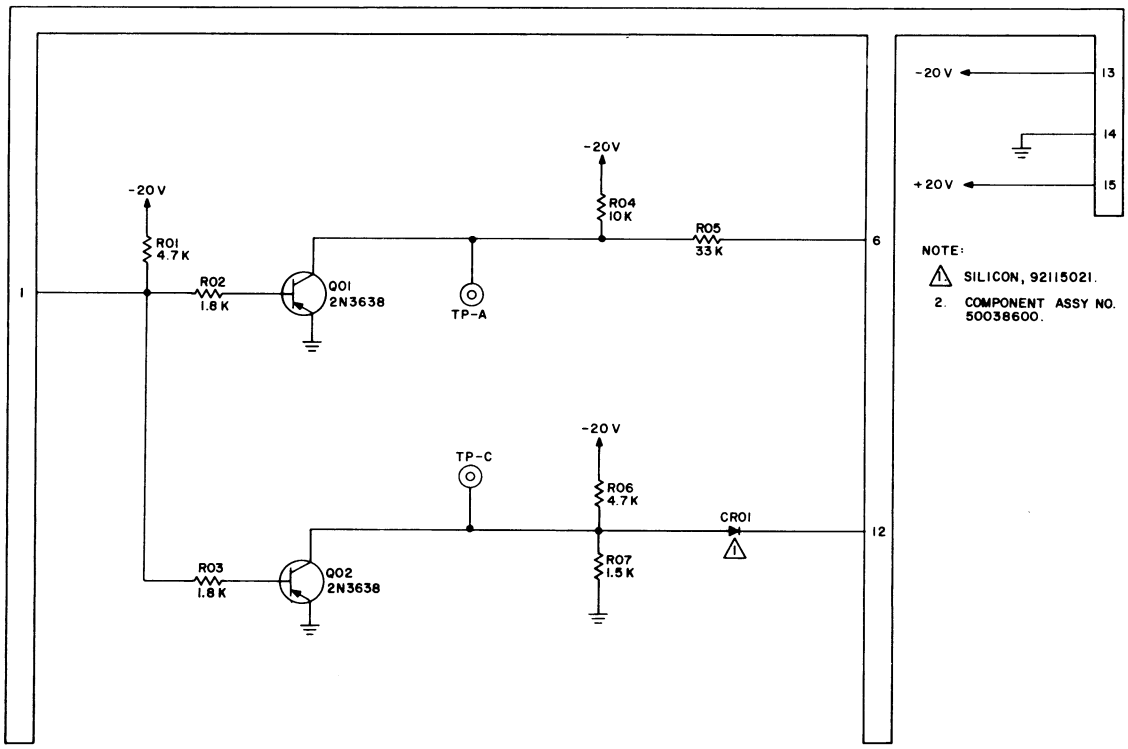
RETRACT INVERTER AND CURRENT SOURCE
FNA

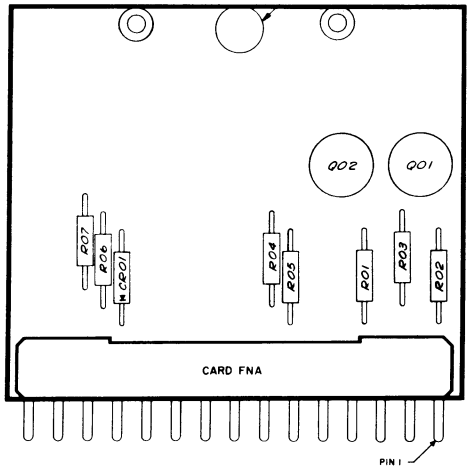
The FNA card is used in the disk file servo actuator. When supplied with relay contacts or logic signals, it causes the servo to retract the magnetic heads from between the disks.

The circuit is two common emitter switches with a common input and separate outputs. With the input pin 1 at ground (or logical "0"), the output at pin 6 provides a ½ ma short circuit current to an operational amplifier virtual ground or summing point; the output at pin 12 is -3v (or logical "1"). When the input is open (or logical "1"), transistors Q01 and Q02 are on (or logical "0"), so both outputs are at zero. This circuit is normally driven from a set of relay contacts, but can also be driven with an output card or inverter card.

SYMBOL




-20 V
13
14
+20 V
15
NOTE:
1. SILICON, 92115021.
2. COMPONENT ASSY NO. 50038600.
-20 V
R04
10K
R05
33K
6
-20 V
R01
4.7K
R02
1.8K
Q01
2N3638
TP-A
1
TP-C
-20 V
R06
4.7K
CR01
12
R03
1.8K
Q02
2N3638
R07
1.5K


Q02
Q01
R07
R06
CR01
R04
R05
R01
R03
R02
CARD FNA
PIN 1

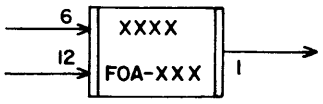
FUNCTION GENERATOR
FOA, FOB

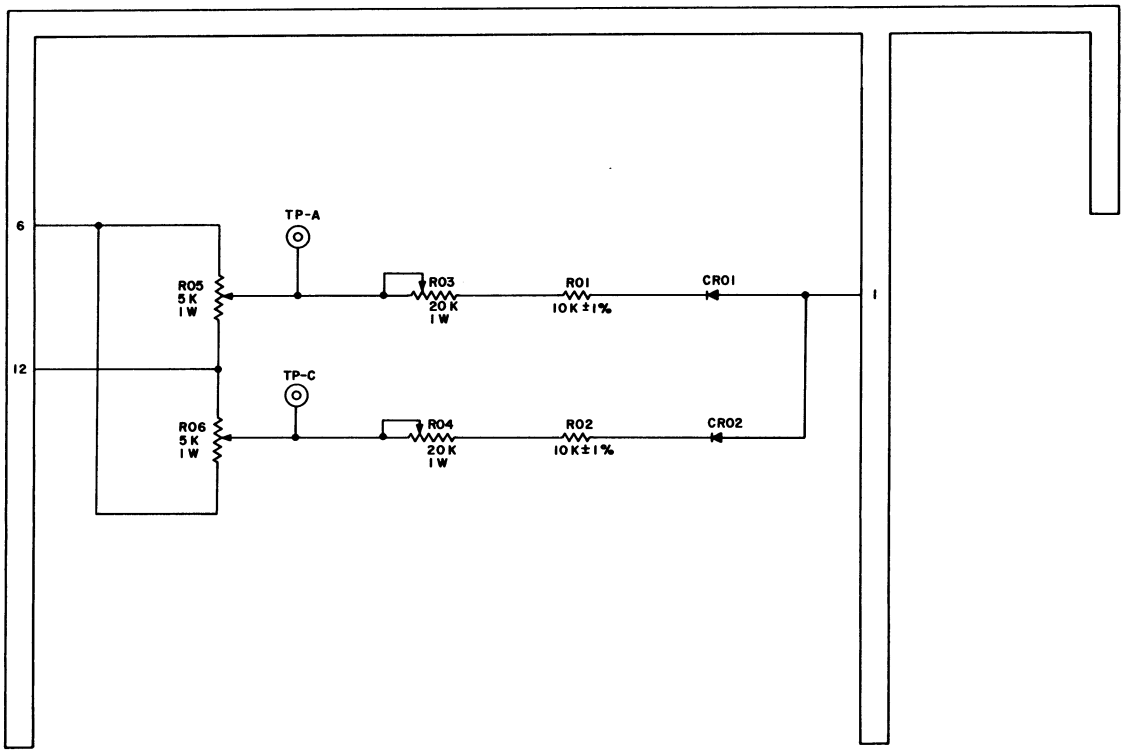
The FOA and FOB cards are used in the disc file servo actuator in the coarse (long stroke) positioning loop to shape the gain curve. For commands requiring a large signal, the gain is reduced.

The FOA and FOB cards are connected around an operational amplifier by connecting pin 1 to the operational amplifier summing point and pin 12 to the operational amplifier output. A floating power supply (ALA card) connects from pins 6 to 12 such that for the FOA pin 6 is positive relative to pin 12 and for the FOB pin 6 is negative. By adjusting potentiometers R05 and R06, the two diodes CR01 and CR02 are back biased to different levels. As the operational amplifier output swings negative, the FOA pin 6 is lowered in voltage until it reaches ground. At this point, either or both diodes can conduct, depending on the potentiometer settings since the input is at the operational amplifier summing point or virtual ground. As the diodes conduct, the gain is reduced because one or more resistors are connected in parallel with the normal feedback resistor around the operational amplifier.

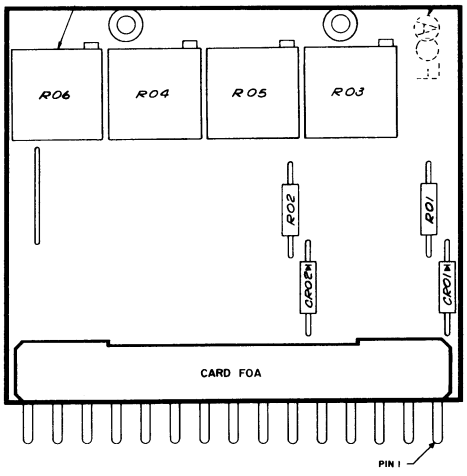
The FOB card operates the same way, except it works for positive swing on the operational amplifier output.

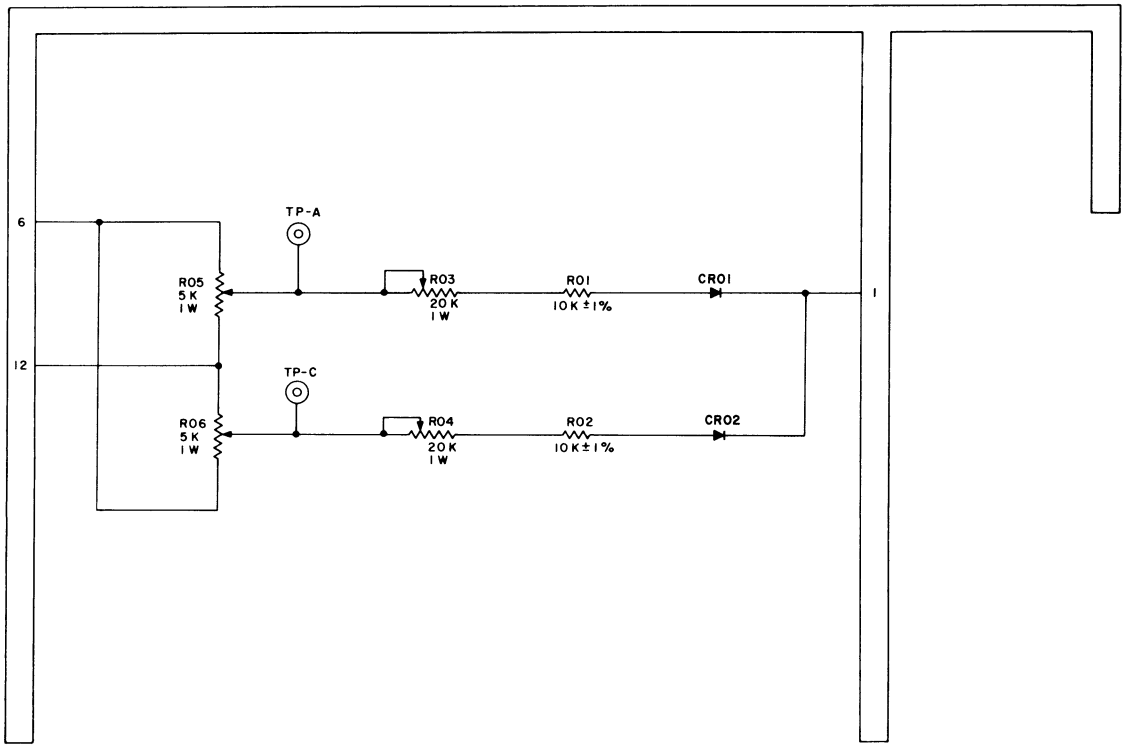
SYMBOL



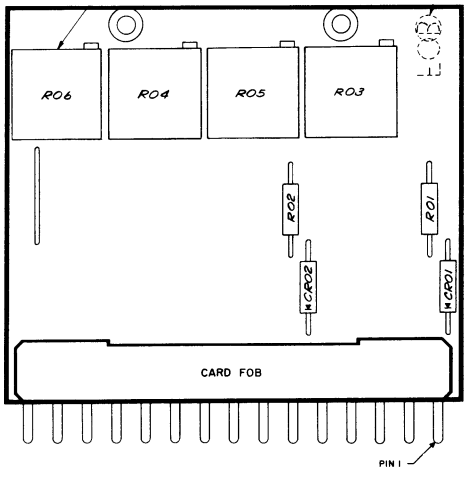

6
12
TP-A
TP-C
R05
5K
1W
R06
5K
1W
R03
20K
1W
R04
20K
1W
R01
10K±1%
R02
10K±1%
CR01
CR02
1

FOA


R06
R04
R05
R03
R02
R01
CR02
CR01
CARD FOA
PIN 1


6
12
TP-A
TP-C
R05
5K
1W
R06
5K
1W
R03
20K
1W
R04
20K
1W
R01
10K ±1%
R02
10K ±1%
CR01
CR02
1

FOB


R06
R04
R05
R03
R02
R01
CR02
CR01
CARD FOB
PIN 1

REFERENCE AMPLIFIER
FPA

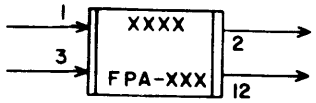
The FPA card is used in the disk file servo actuator. The circuit supplies a plus or minus 8 volt reference to the coarse positioning loop. This voltage must be stable, because it represents the coarse command to the system. The output load is approximately 10 ma maximum.

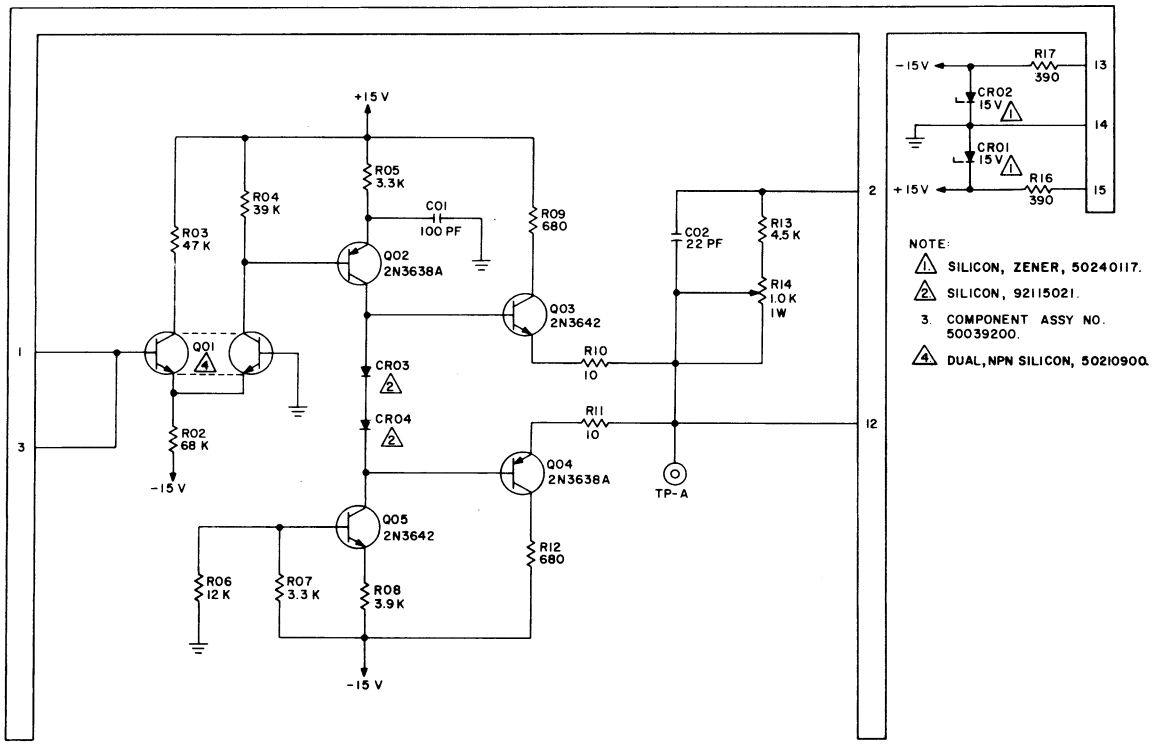
The FPA card is supplied by a FLA bridge rectifier card. Pins 1 and 2 connect with either pins 11 and 9, or 12 and 10 respectively (card FLA), for a +8v or -8v output. This combination is an operational amplifier with closed loop gain of unity, but can be varied ±10% by R14.

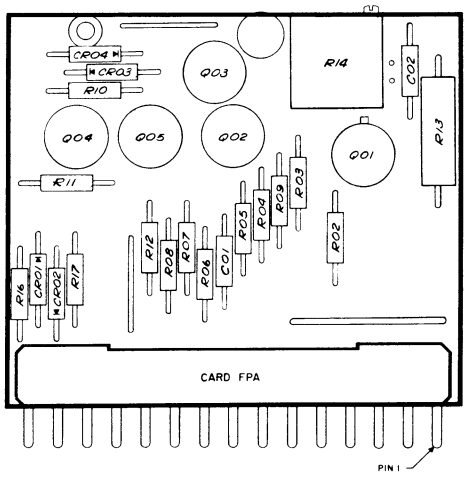
The first stage of the amplifier is a differential stage. This stage uses a matched pair of transistors in a single TO -5 can, for best temperature stability. Transistors Q01 and Q02 provide the necessary closed loop gain. Transistor Q05 is a constant current source to provide negative drive for Q04. The positive drive for Q03 comes from Q02. If the +8v output is desired, pin 1 is driven from the negative voltage pin (pin 11, FLA card). Pin 2 is connected to pin 9 of the FLA card. The negative voltage is used to give a positive voltage, because the circuit has negative gain. Under these conditions, Q03 supplies the load and Q04 is near cut-off.

If the output is to be -8v, pins 1 and 2 connect to pins 12 and 10 respectively (card FLA). Under these conditions, Q04 supplies the load and receives its base drive from the current source (Q05). Transistor Q03 is near cut-off.

SYMBOL




+15 V
R05 3.3K
C01 100 PF
R09 680
R04 39 K
R03 47 K
Q02 2N3638A
Q03 2N3642
C02 22 PF
R13 4.5 K
R14 1.0 K 1W
Q01
CR03
R10 10
CR04
R11 10
R02 68 K
-15 V
Q04 2N3638A
TP-A
Q05 2N3642
R12 680
R06 12 K
R07 3.3 K
R08 3.9K
-15 V
1
2
3
12
-15V
R17 390
13
CR02 15V
14
CR01 15V
+15V
R16 390
15
NOTE:
1. SILICON, ZENER, 50240117.
2. SILICON, 92115021.
3. COMPONENT ASSY NO. 50039200.
4. DUAL, NPN SILICON, 50210900.


CR04
CR03
R10
Q03
R14
C02
R13
Q04
Q05
Q02
Q01
R11
R12
R08
R07
R06
C01
R05
R04
R09
R03
R02
R16
CR01
CR02
R17
CARD FPA
PIN 1

VELOCITY, ACCELERATION SUMMING NETWORK
FRA, FRB, FRC, FRD

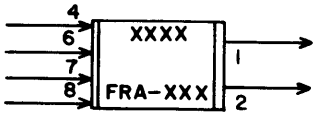
The FRA through FRD cards contain a passive circuit of resistors, capacitors, and zener diodes to be used with operational amplifiers in the disk file servo actuator.

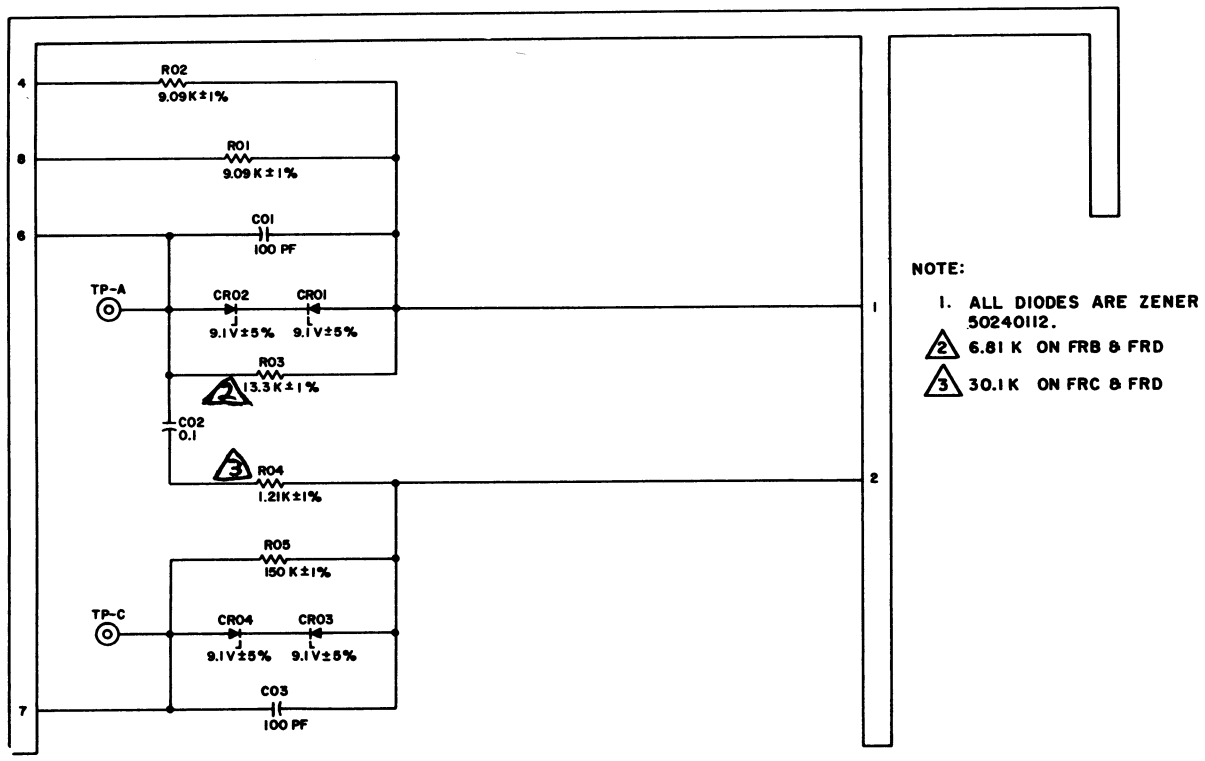
The circuit is supplied at pins 4 and 8 with voltages from velocity transducers, one end of each being grounded (the FRD is supplied from two velocity transducers). An operational amplifier connects between pins 1 and 6 (input at 1), giving an output proportional to the sum of the velocity signals at pin 6.

Zener diodes CR01 and CR02 limit the output voltage of the amplifier to about ±10 volts peak. Capacitor C01 provides high frequency cutoff at approximately 120KC.

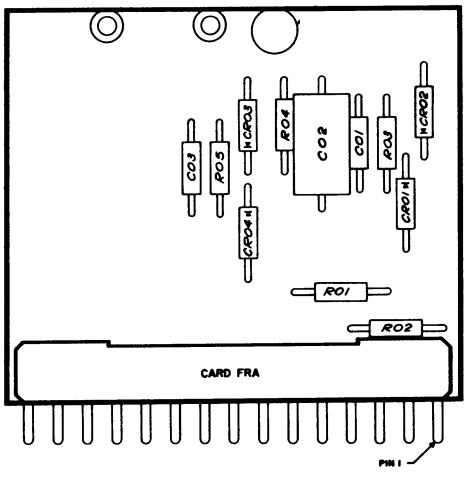
Another operational amplifier connects between pins 2 and 7 (input at 2). With the velocity signal at pin 6 also being applied to the differentiating network (C02 and R04), the output at pin 7 becomes a signal proportional to acceleration for frequencies below 13KC (50 CPS for FRC & D). Beyond 13KC (50 CPS for FRC & D) the gain levels off so the output is somewhat proportional to velocity. The useful range of frequencies for the system however is below 300 cycles. Capacitor C03 provides for frequency cutoff at approximately 16KC, and the zener diodes limit the output swing to approximately ±10 volts peak.

SYMBOL




R02
9.09K±1%
R01
9.09K±1%
C01
100 PF
TP-A
CR02
CR01
9.1V±5%
9.1V±5%
R03
13.3K±1%
C02
0.1
R04
1.21K±1%
R05
150K±1%
TP-C
CR04
CR03
9.1V±5%
9.1V±5%
C03
100 PF
4
8
6
7
1
2
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2 6.81K ON FRB & FRD
3 30.1K ON FRC & FRD

FRA


C03
R05
CR04
CR03
R04
C02
C01
R03
CR02
CR01
R01
R02
CARD FRA
PIN 1

OPERATIONAL AMPLIFIER

FSA, FSB

The FSA card contains the operational amplifier used as the main building block in the disk file servo actuator.

This card has on it the purchased modular amplifier, plus the discrete component power booster. The input to the amplifier is of a differential nature, but as used in the servo, one side (pin 5) is grounded. Pin 1 is driven and the inverted output is taken from pin 7. The amplifier cannot be used by itself in an open loop manner because the output drifts between + and -15 volts. Normally one of the feedback network cards is used (FRA, FTA, FUA, or FVA) around the amplifier between pins 1 and 7 to close the feedback loop. The output is then near zero and can be set there by the adjustment pot on the module (assuming the input resistor is grounded on the end opposite pin 1).

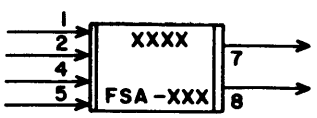
The booster stage is a complimentary emitter follower Q01 and Q03 operating approximately class AB. A constant current source is used to get positive drive for Q03. This is basically the same circuit as used on the FPA and FMA cards and discussed under FHA or FIA. The load on this card can be approximately $\pm$ 10V peak into 500 ohms.

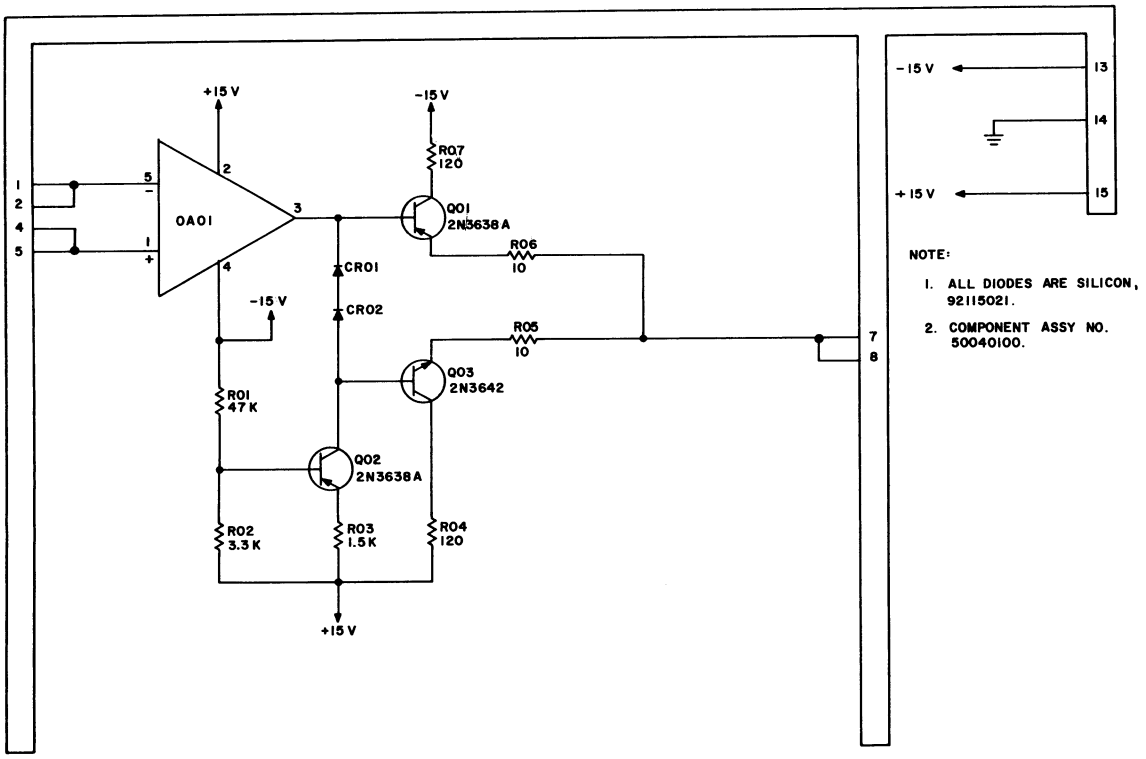
The above discussion also applies to the FSB card.

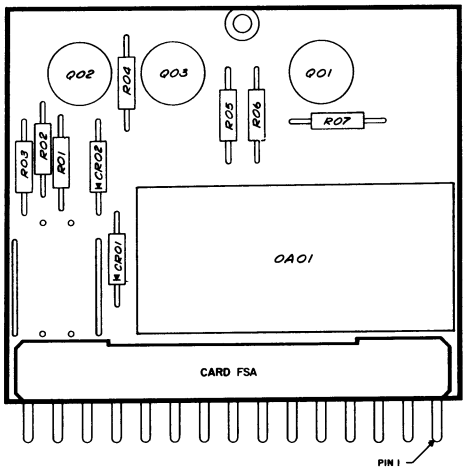
The FSB card uses a purchased op. amp. module plus the discrete component power booster. In addition, a + and -15 volt regulated power supply has been incorporated on the card. A balance pot was added to the card because the less expensive op. amp. module did not contain this balance adjustment.

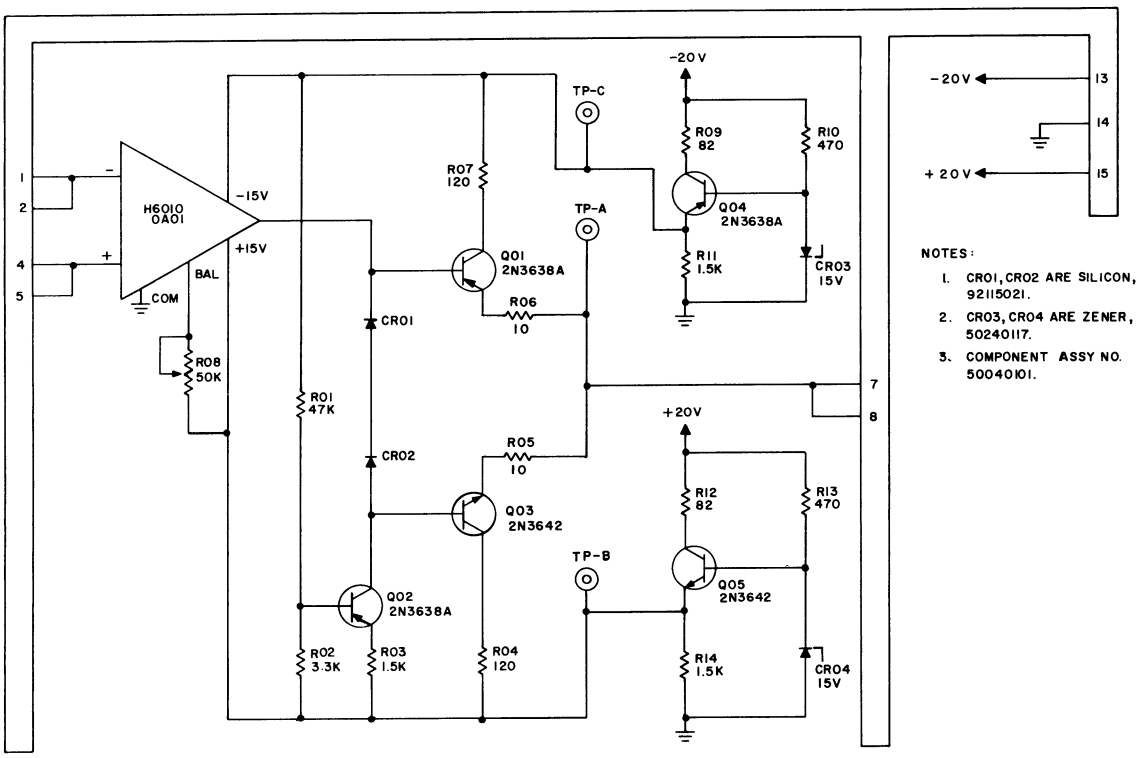
Caution: The FSA card requires three card slots. The FSB card requires two dard slots.

SYMBOL

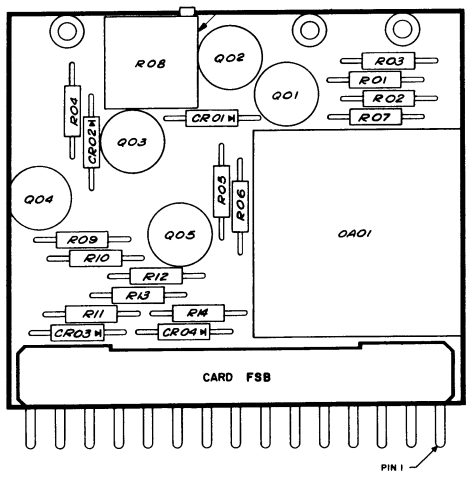



+15 V
-15 V
R07
120
Q01
2N3638A
R06
10
CR01
CR02
R05
10
Q03
2N3642
R01
47 K
Q02
2N3638A
R02
3.3 K
R03
1.5 K
R04
120
OA01
-15 V
+15 V
13
14
15
7
8
NOTE:
1. ALL DIODES ARE SILICON, 92115021.
2. COMPONENT ASSY NO. 50040100.


Q02
R04
Q03
Q01
R05
R06
R07
R03
R02
R01
CR02
CR01
OA01
CARD FSA
PIN 1


H6010
0A01
-15V
+15V
BAL
COM
R08
50K
R01
47K
R07
120
TP-C
TP-A
TP-B
-20V
R09
82
R10
470
Q04
2N3638A
R11
1.5K
CR03
15V
Q01
2N3638A
R06
10
CR01
CR02
R05
10
Q03
2N3642
+20V
R12
82
R13
470
Q05
2N3642
Q02
2N3638A
R02
3.3K
R03
1.5K
R04
120
R14
1.5K
CR04
15V
-20V
+20V
NOTES:
1. CR01, CR02 ARE SILICON, 92115021.
2. CR03, CR04 ARE ZENER, 50240117.
3. COMPONENT ASSY NO. 50040101.

FSB


R08
Q02
R03
R01
Q01
R02
R07
CR01 M
R04
CR02 M
Q03
R05
R06
Q04
0A01
Q05
R09
R10
R12
R13
R11
RM
CR03 M
CR04 M
CARD FSB
PIN 1

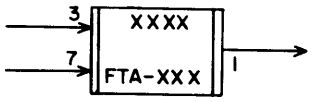
VELOCITY SUMMING NETWORK

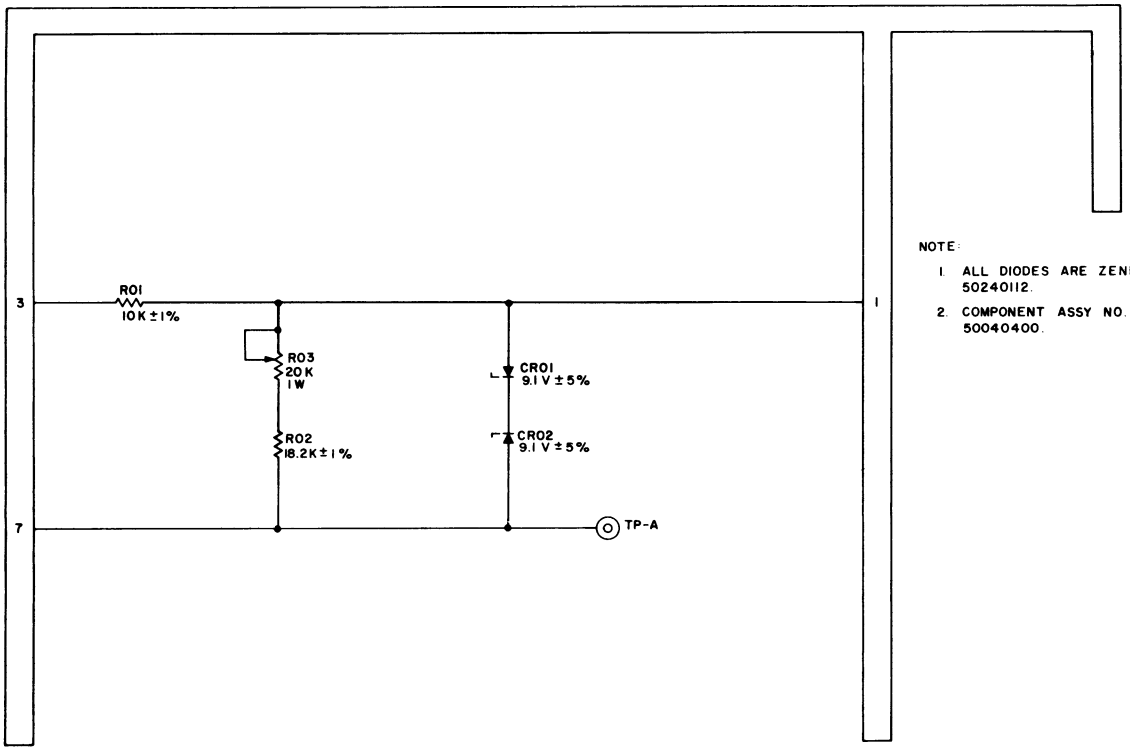
FTA

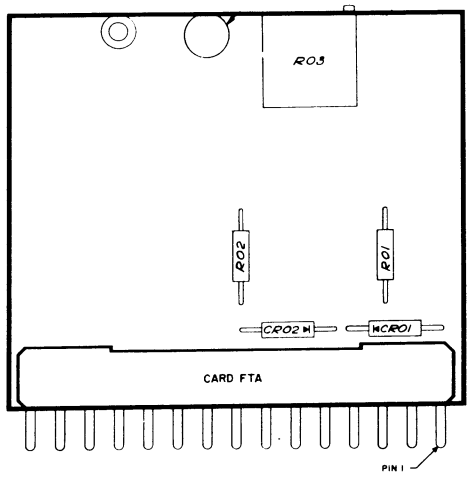
This card is used in the disk file servo actuator as a feedback network for an operational amplifier.

The circuit is supplied with a velocity signal, which is applied at pin 3. An operational amplifier is connected from pins 1 to 7, with the input at pin 1. The closed loop gain is given by the ratio of R02 plus R03 to R01. This is adjustable from 1 to 2. The output is a velocity signal with a phase inversion. Zener diodes CR01 and CR02 limit the output voltage to ±10v peak.

SYMBOL




3
7
1
R01
10K ±1%
R03
20K
1W
R02
18.2K ±1%
CR01
9.1V ±5%
CR02
9.1V ±5%
TP-A
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2. COMPONENT ASSY NO. 50040400.


R03
R02
R01
CR02
CR01
CARD FTA
PIN 1

SUMMING NETWORK A,V,X
FUA, FUB

This passive feedback network is used in the disk file servo actuator in conjunction with three operational amplifiers. One amplifier sums acceleration (A), velocity (V), and fine position (X) signals. This signal becomes the control signal for the accurate positioning of the magnetic recording heads in the file. A second amplifier is used for amplifying the fine positioning (short stroke) signal. The third amplifier is used for the generation of an on point signal which tells the computer with the disk file that the servo is at the proper location.

The short stroke amplifier connects between pins 1 and 7 with 1 to the input. The closed loop gain of 3.25 is given by R01 divided by the demodulation output impedance of 5K.

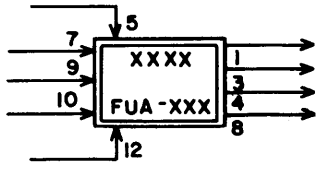
An on point amplifier connects between 8 and 9 with 8 being the input. This has a closed loop gain given by R07 over R08 which is 1.82.

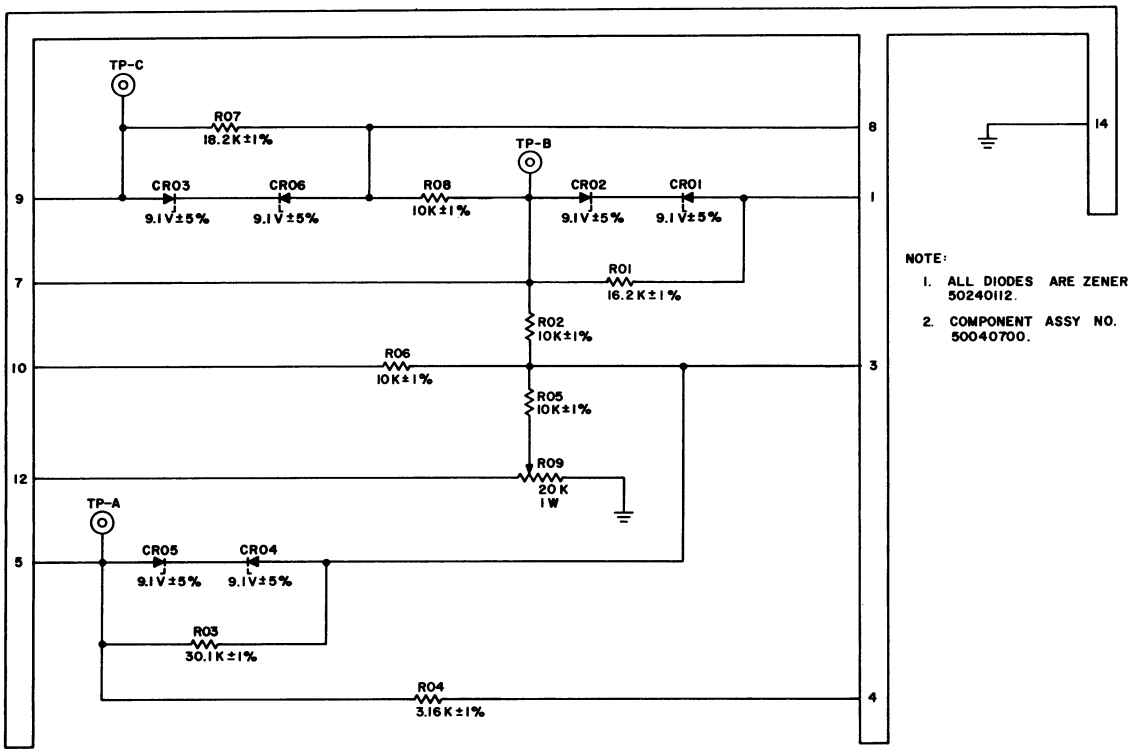
A summing amplifier connects between 3 and 5 with 3 being the input. The acceleration signal connects to pin 12, the velocity signal goes to pin 10, and the short stroke displacement is at pin 7. Adjustment of pot R09 adjusts the gain for the acceleration signal. Resistor R03 divided by R02, R05 or R06 give a closed loop gain of 3.01. The FUB card uses another pot R10 to adjust the servo loop gain to compensate for hydraulic servo valve variations.

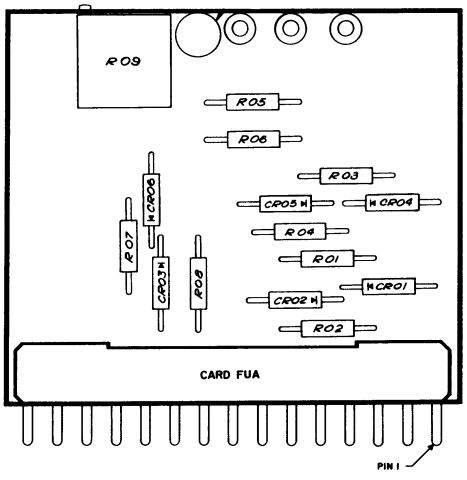
Resistor R04 is part of the input resistor for the short stroke valve amplifier (FHA).

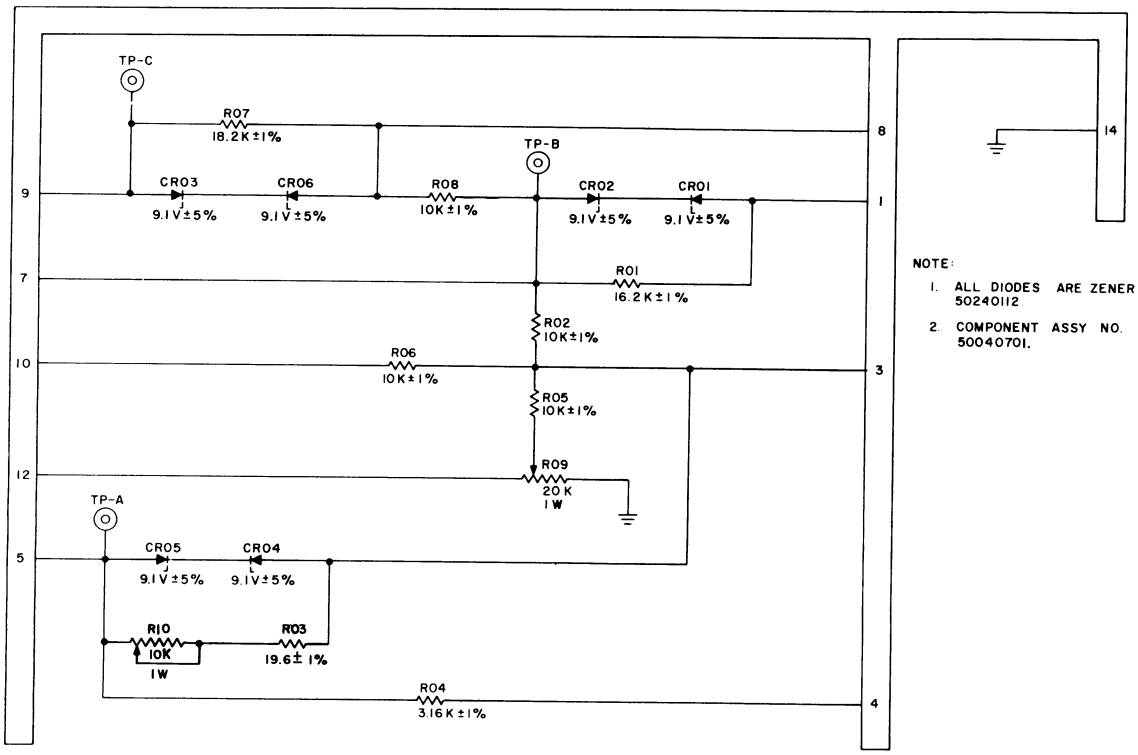
The zener diodes CR01 through CR06 limit the amplifier output voltage to $\pm$ 10V peak.

SYMBOL

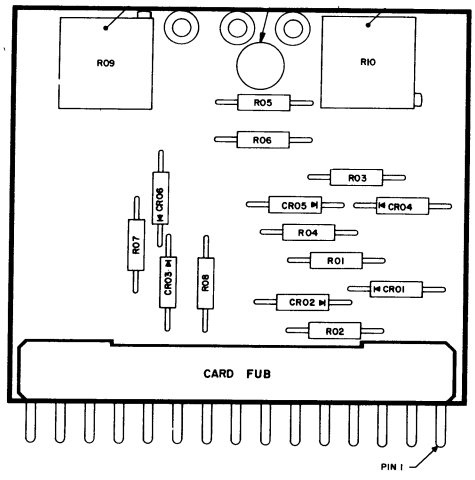



TP-C
R07
18.2K±1%
TP-B
CR03
9.1V±5%
CR06
9.1V±5%
R08
10K±1%
CR02
9.1V±5%
CR01
9.1V±5%
R01
16.2K±1%
R02
10K±1%
R06
10K±1%
R05
10K±1%
R09
20K
1W
TP-A
CR05
9.1V±5%
CR04
9.1V±5%
R03
30.1K±1%
R04
3.16K±1%
8
14
9
1
7
10
3
12
5
4
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2. COMPONENT ASSY NO. 50040700.


R09
R05
R06
R03
CR05 H
H CR04
R04
R01
H CR01
CR02 H
R02
R07
H CR06
CR03 H
R08
CARD FUA
PIN 1


TP-C
R07
18.2K ±1%
TP-B
CR03
9.1V ±5%
CR06
9.1V ±5%
R08
10K ±1%
CR02
9.1V ±5%
CR01
9.1V ±5%
R01
16.2K ±1%
R02
10K ±1%
R06
10K ±1%
R05
10K ±1%
R09
20K
1W
TP-A
CR05
9.1V ±5%
CR04
9.1V ±5%
R10
10K
1W
R03
19.6K ±1%
R04
3.16K ±1%
8
14
9
1
7
10
3
12
5
4
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2. COMPONENT ASSY NO. 50040701.

FUB


R09
R10
R05
R06
R03
CR05
CR04
R04
R01
CR01
CR02
R02
CR06
R07
CR03
R08
CARD FUB
PIN 1

POSITION AND ACCELERATION NETWORK
FVA

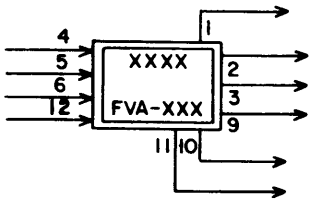
The FVA passive network is used with three operational amplifiers in the disk file servo actuator. The circuit forms the coarse control signal from the position (long stroke) and acceleration signals.

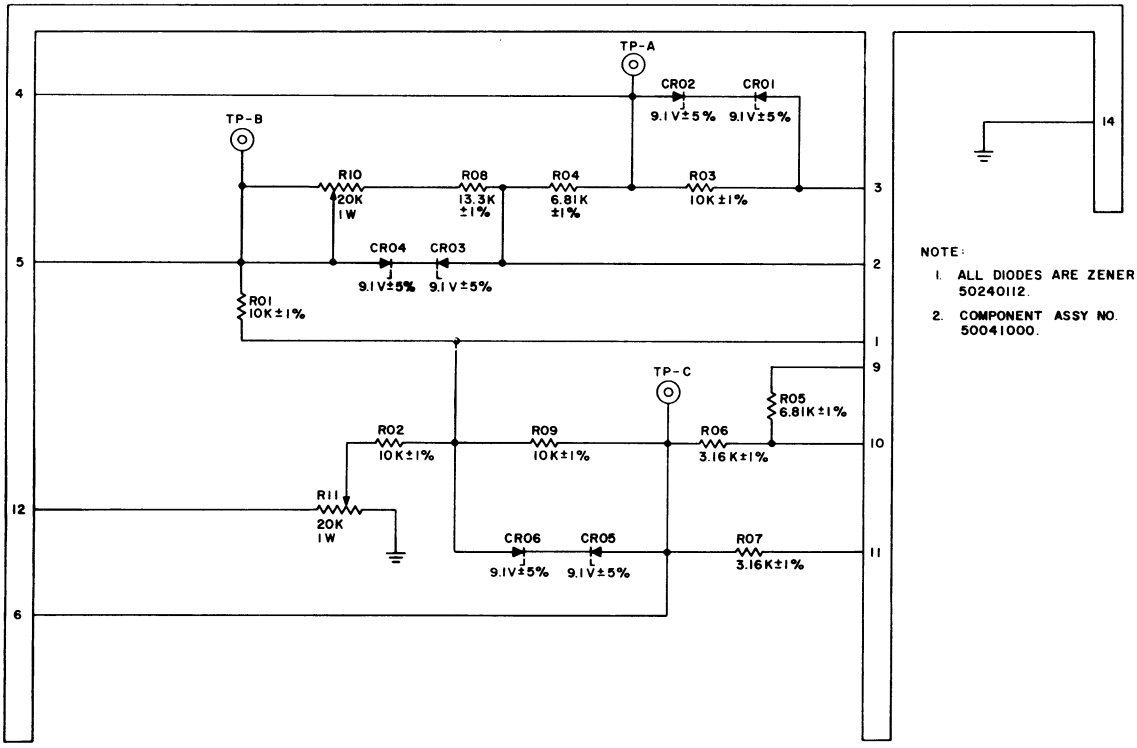
The operational amplifiers connect between pins 1 and 6, 2 and 5, and 3 and 4 (inputs at pins 1, 2, and 3). The long stroke signal goes to pin 3 and is amplified with a gain of 2 (given by the ratio of R03 and the demodulator output impedance of 5 K). This is followed by another operational amplifier between pins 2 and 5, which uses the function generator cards FOA and FOB to shape the gain curve. The low signal gain is adjustable between 1.95 and 4.9, as given by the ratio of R08 plus R10 to R04.

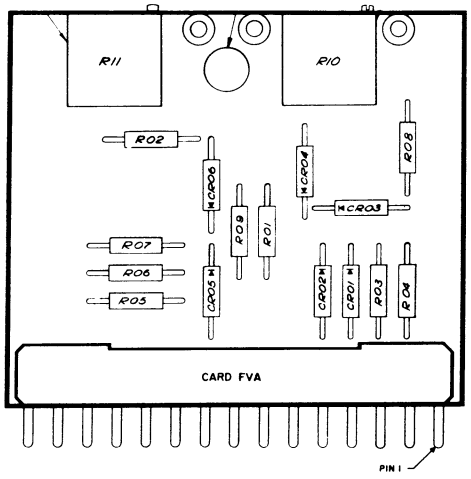
An acceleration signal is applied at pin 12, and is summed with the long stroke signal in the operational amplifier between pins 1 and 6. The acceleration gain can be adjusted by potentiometer R11. The output signal on pin 6 is applied to the short and long stroke valves via resistors R05, R06, and R07.

The zener diodes limit the output swing of the operational amplifiers to ±10v peak.

SYMBOL




TP-A
TP-B
TP-C
CR02
CR01
9.1V±5%
9.1V±5%
R10
20K
1W
R08
13.3K
±1%
R04
6.81K
±1%
R03
10K±1%
CR04
CR03
9.1V±5%
9.1V±5%
R01
10K±1%
R05
6.81K±1%
R02
10K±1%
R09
10K±1%
R06
3.16K±1%
R11
20K
1W
CR06
CR05
9.1V±5%
9.1V±5%
R07
3.16K±1%
4
5
6
12
3
2
1
9
10
11
14
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2. COMPONENT ASSY NO. 50041000.


R11
R10
R02
R08
CR04
CR06
CR03
R09
R01
R07
R06
R05
CR02
CR01
R03
R04
CARD FVA
PIN 1

TEMPERATURE SERVO AMPLIFIER
FWA

A temperature servo controls the air temperature in the vicinity of the disks in the disk file. The servo consists of the FWA amplifier, a thermistor bridge, and a shaded pole motor.

The thermistor connects between pins 1 and ground. Motor shading coils, used to reverse the motor, are connected to pins 11 and 12 via the limit switches (S01 and S02) on the motor assembly. The coil end labeled CW goes to the normally closed contact on S01, and from S01 common to pin 12. The coil end labeled CCW goes to the normally closed contact on S02, and from S02 common to pin 11.

At the operating temperature of 92°F, the thermistor bridge consisting of the thermistor, R01, R03, R04, R05, R06, and CR01 is balanced, and no signal is applied to the differential amplifier (Q01 and Q02). Therefore, the output transistors (Q05 and Q06) are off, so no unbalance exists in the motor shading coil currents. The motor will be off, allowing the proper flow of air to the disks.

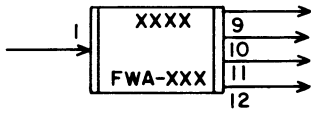
If the temperature increases, an unbalance will exist which drives Q02 base positive and Q01 base negative. The collector of Q02 goes negative and the collector of Q01 goes positive. Normally, transistors Q03 and Q04 are biased, so their collectors are at approximately zero to keep Q05 and Q06 off. Since the collector of Q02 is going negative, Q04 will be driven on so its collector goes positive and turns on Q06. The collector of Q01 is positive going, so Q03 turns further off driving Q05 further off.

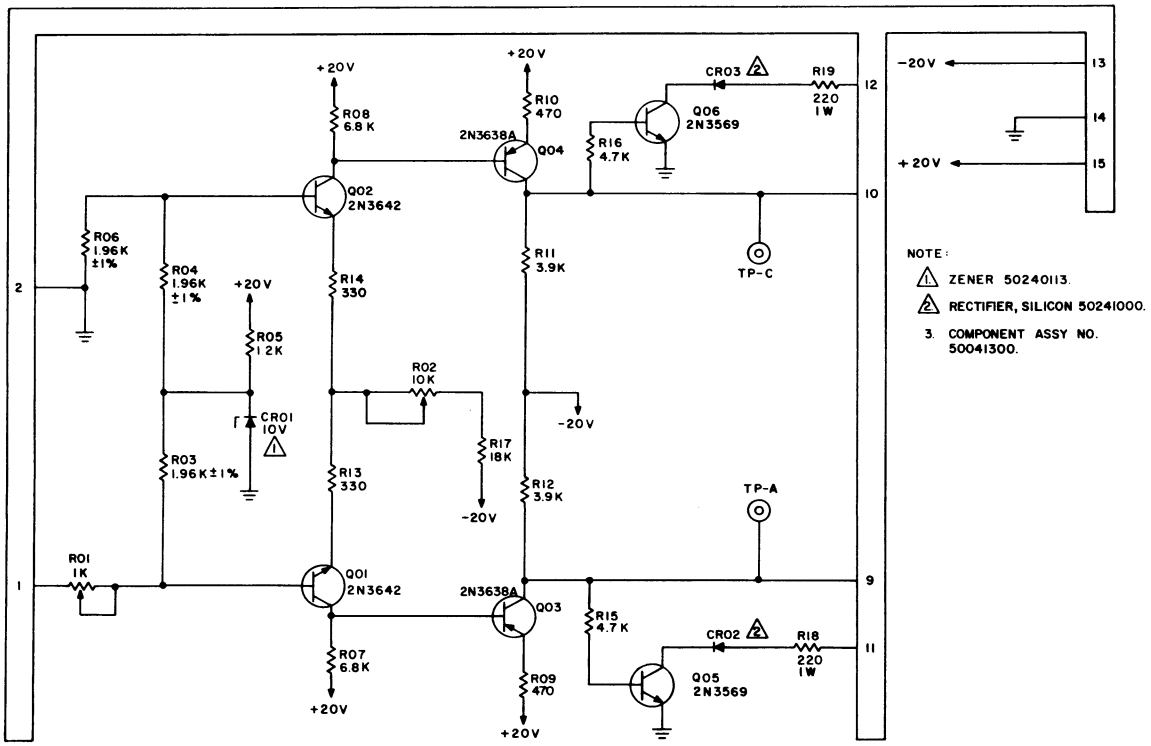
The amount Q06 turns on is proportional to the temperature change. Therefore, the motor will run at a speed proportional to the temperature difference, and in the direction that increases the air flow. This will allow the file and thermistor to cool. When a balance is again achieved, the motor will stop.

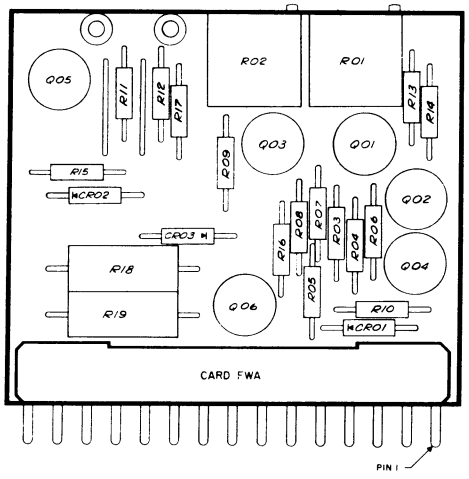
For temperatures below the control point, Q03 and Q05 turn on and reverse motor operation occurs. Air flow is reduced until the temperature rises.

A zero set condition at the desired quiescent temperature is setup by adjustment of the bridge potentiometer (R01), and the differential amplifier potentiometer (R02).

SYMBOL


XXXX
FWA-XXX
1
9
10
11
12


+20V
R08 6.8K
R10 470
2N3638A
Q04
CR03 2
R19 220 1W
Q06 2N3569
R16 4.7K
Q02 2N3642
R06 1.96K ±1%
R04 1.96K ±1%
R14 330
R11 3.9K
TP-C
R05 1.2K
R02 10K
CR01 10V 1
R17 18K
-20V
R03 1.96K±1%
R13 330
R12 3.9K
TP-A
R01 1K
Q01 2N3642
Q03
R15 4.7K
CR02 2
R18 220 1W
Q05 2N3569
R07 6.8K
R09 470
-20V
+20V
12
10
9
11
2
1
13
14
15
NOTE:
1 ZENER 50240113.
2 RECTIFIER, SILICON 50241000.
3. COMPONENT ASSY NO. 50041300.


Q05
R11
R18
R17
R02
R01
R13
R14
R09
Q03
Q01
R15
WCR02
CR03 W
Q02
R16
R08
R07
R03
R04
R06
Q04
R18
R19
Q06
R05
R10
WCR01
CARD FWA
PIN 1

TEMPERATURE SENSING AMPLIFIER
FWB

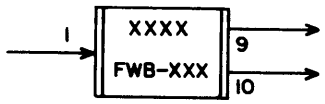
The FWB is used to sense the temperature in the vicinity of the disks in the disk file.

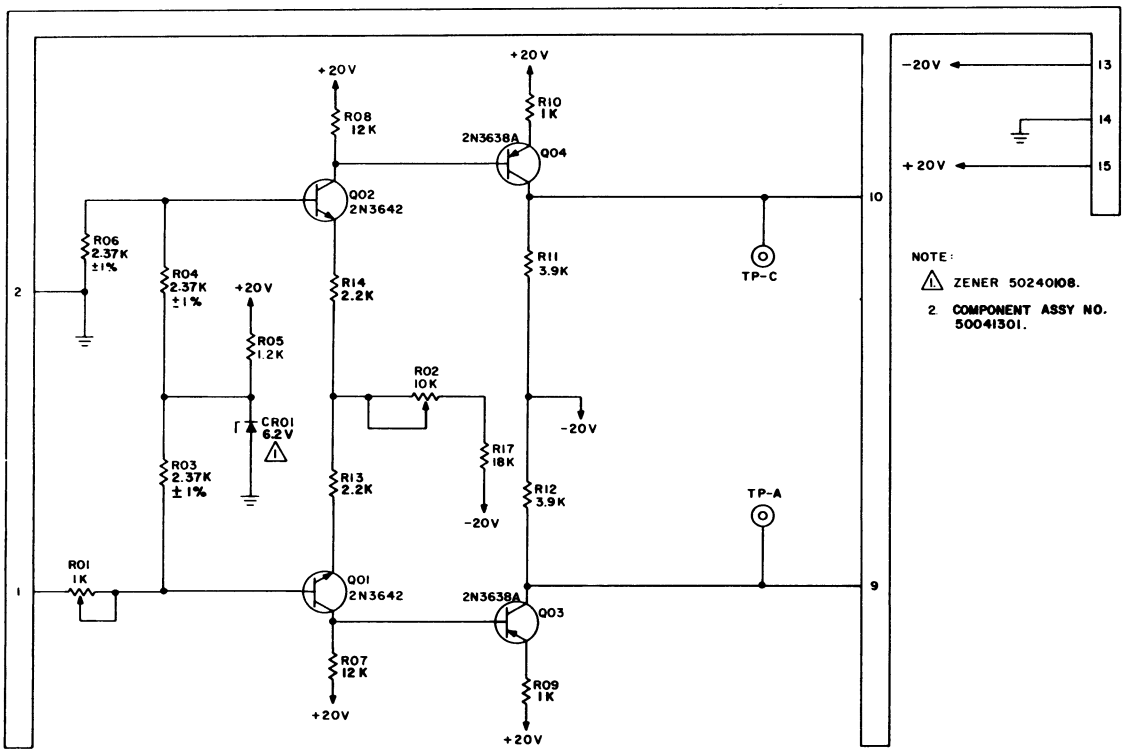
A bridge consisting of a thermistor and R01, R03, R04, and R06 is balanced near 75°F by adjusting R01. At temperatures above and below 75°F the thermistor unbalances the bridge. The unbalance in voltage is amplified by the differential amplifier consisting of Q01, Q02, Q03, and Q04.

Outputs of the amplifier are pins 9 and 10. When the temperature goes higher than 75°F (resistance of thermistor decreases), pin 9 goes negative and pin 10 goes positive. When the temperature goes lower than 75°F (resistance of thermistor increases), pin 9 goes positive and pin 10 goes negative.

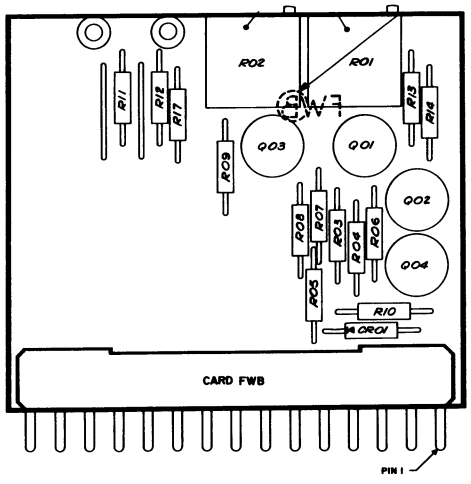
Potentiometer R02 is used to set the bias level of the outputs positive or negative.

SYMBOL




+20V
R08
12K
+20V
R10
1K
2N3638A
Q04
Q02
2N3642
R06
2.37K
±1%
R04
2.37K
±1%
+20V
R05
1.2K
R14
2.2K
R11
3.9K
TP-C
R02
10K
CR01
6.2V
R17
18K
-20V
R03
2.37K
±1%
R13
2.2K
R12
3.9K
TP-A
-20V
R01
1K
Q01
2N3642
2N3638A
Q03
R07
12K
R09
1K
+20V
+20V
-20V
13
14
+20V
15
10
9
2
1
NOTE:
1 ZENER 50240108.
2 COMPONENT ASSY NO. 50041301.

FWB


R02
R01
R11
R12
R17
R13
R14
R09
Q03
Q01
Q02
Q04
R08
R07
R03
R04
R06
R05
R10
CR01
CARD FWB
PIN 1

GATED AMPLIFIER

FXB

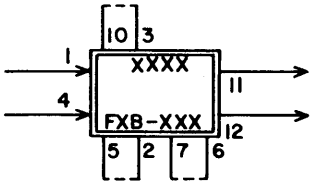
This card is similar to the ATA card. The differences are:

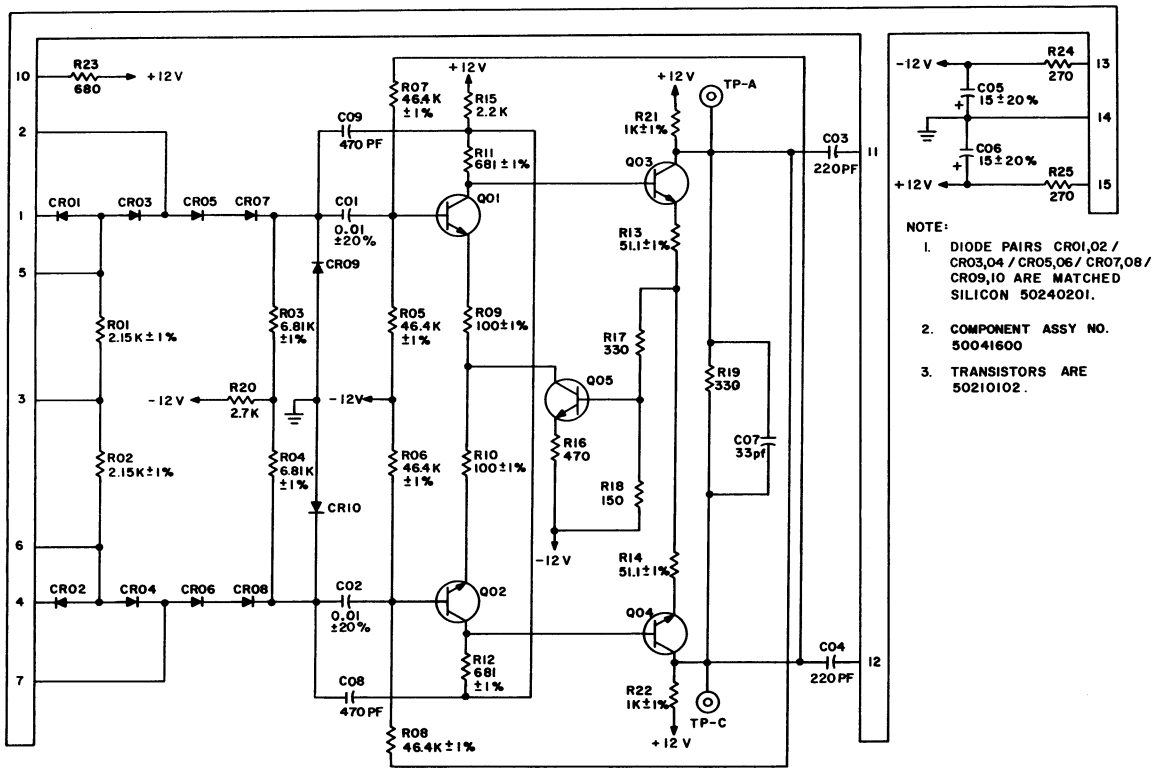
1. Jumpers can short out diodes CR03 and CR04.
2. Feedback capacitors C09 and C10 were added to decrease high-frequency gain.
3. Gain adjusting potentiometer R23 was removed.
4. R-C filters were added, so that the card operates off standard machine power supplies.
5. A fixed resistor R23 was added, so that the card could be set up to have the gate open permanently to read timing tracks.
6. Coupling capacitors were chosen for the particular applications (807/8 Disc File).

Bandpass is from 30 Kc to 2Mc.

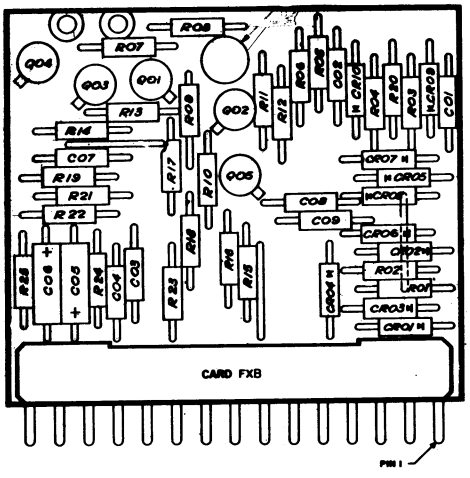
If pin 3 is at +5v or more positive, this card amplifies a signal put in on pins 1 and 4 from a center-tapped to ground read head. Pin 3 can be held positive by jumpering to pin 10.

SYMBOL




R23
680
+12V
R07
46.4K
±1%
R15
2.2K
C09
470 PF
R11
681 ±1%
Q01
C01
0.01
±20%
CR09
R01
2.15K±1%
R03
6.81K
±1%
R05
46.4K
±1%
R09
100±1%
R20
2.7K
-12V
R02
2.15K±1%
R04
6.81K
±1%
R06
46.4K
±1%
R10
100±1%
CR10
CR01
CR03
CR05
CR07
CR02
CR04
CR06
CR08
C02
0.01
±20%
Q02
R12
681
±1%
C08
470PF
R08
46.4K±1%
R21
1K±1%
TP-A
Q03
R13
5.1±1%
R17
330
Q05
R16
470
R18
150
R14
5.1±1%
Q04
R22
1K±1%
TP-C
C03
220PF
C04
220PF
R19
330
C07
33pf
R24
270
C05
15±20%
C06
15±20%
R25
270
NOTE:
1. DIODE PAIRS CR01,02 / CR03,04 / CR05,06 / CR07,08 / CR09,10 ARE MATCHED SILICON 50240201.
2. COMPONENT ASSY NO. 50041600
3. TRANSISTORS ARE 50210102.

FXB


CARD FXB
PIN 1

AGC RECTIFIER
FYA

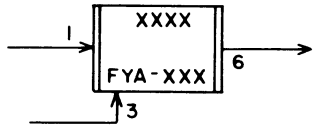
The FYA card generates a control signal for the EZA card in accordance with the average signal level of the input. The full-wave rectified output (pin 6, EJA card) is applied to pin 1. Resistors R02 and R03 define a reference voltage at the base of transistor Q01. The input signal must be more negative than this reference voltage if Q01 is to be turned on. Therefore, small disturbances at the input will be ignored.

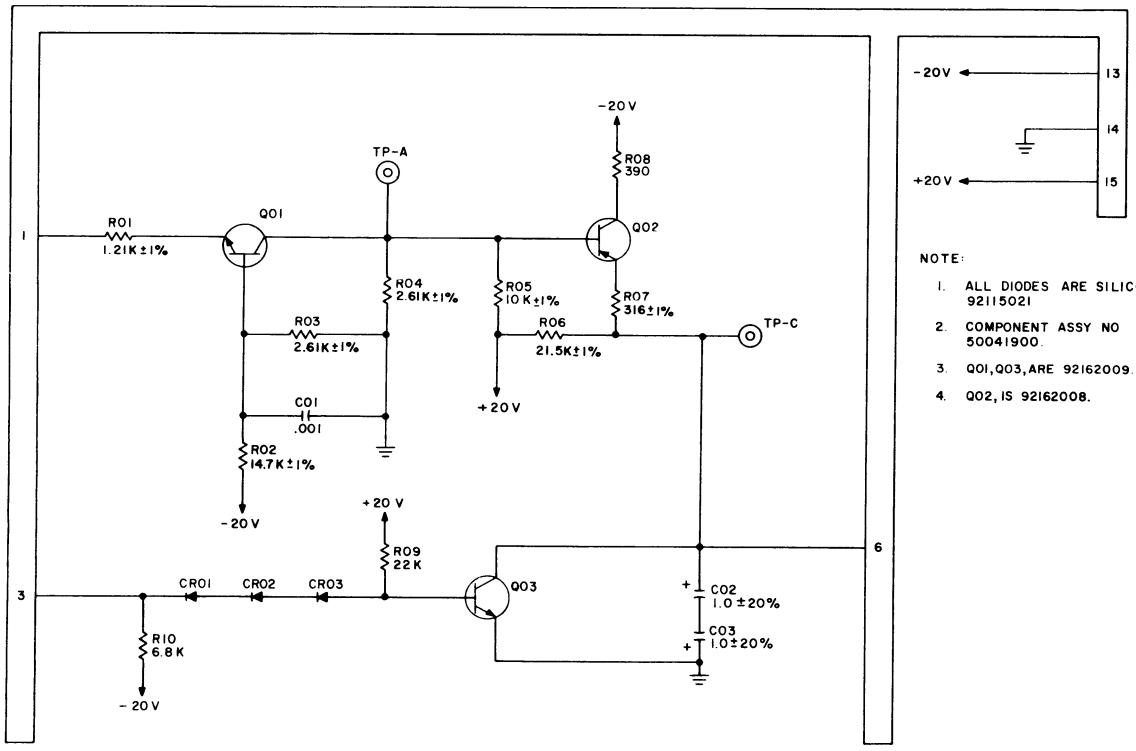
In the absence of a signal from Q01, resistors R04 and R05 will establish a steady-state voltage at the base of Q02. Resistors R06 and R07 will establish the voltage on capacitors C02 and C03. When a signal is applied at pin 1, which is more negative than the voltage on the base of Q01, Q01 will conduct. The base of Q02 goes more negative and causes Q02 to pull charge out of capacitors C02 and C03, making the voltage on pin 6 more negative. The time constant for pulling this point more negative is determined by R07, C02, and C03. Resistor R01 increases the input impedance seen by the EJA card, and helps determine the voltage transfer ratio of the Q01 circuit.

When the signal at pin 1 is no longer more negative than the voltage on the base of Q01, the voltage at pin 6 will return to its steady-state condition. The time constant for this change is determined by R06, C02, and C03. Since the value of R06 is considerably more than R07, the voltage on pin 6 can go negative more rapidly than it can go positive. This was necessary because of the data format used in the 852 Disk Pack. In this format there are 180 AGC bits, which determine the gain of the read chain for the following 900 data bits. The data in the 852 is in NRZ1. Therefore, since there may be only 300 "1's" in the 900 data bits, the time constants were adjusted to insure the voltage at pin 6 (determined by the 180 AGC bits) will not decay during the 900 data bits.

The above information applies if pin 3 is at -3v. If pin 3 is brought to ground, Q03 forces the voltage at pin 6 to ground, setting the attenuation of the EZA card to a nominal level. This is an "AGC Disable" function. The pin 6 voltage is applied to pin 9 of the EZA card as a gain control signal.

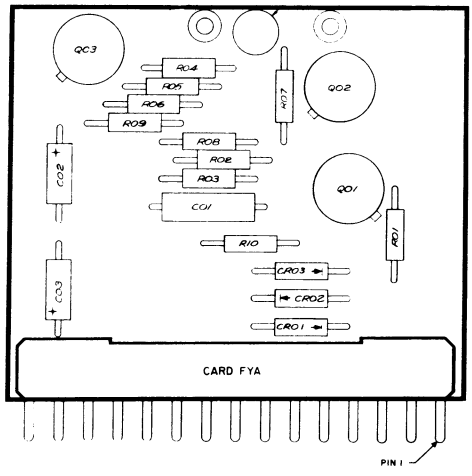
SYMBOL





NOTE:

1. ALL DIODES ARE SILICON 92115021
2. COMPONENT ASSY NO 50041900.
3. Q01, Q03, ARE 92162009.
4. Q02, IS 92162008.

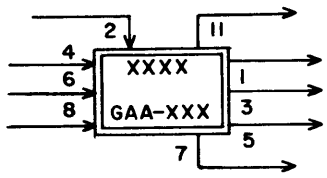


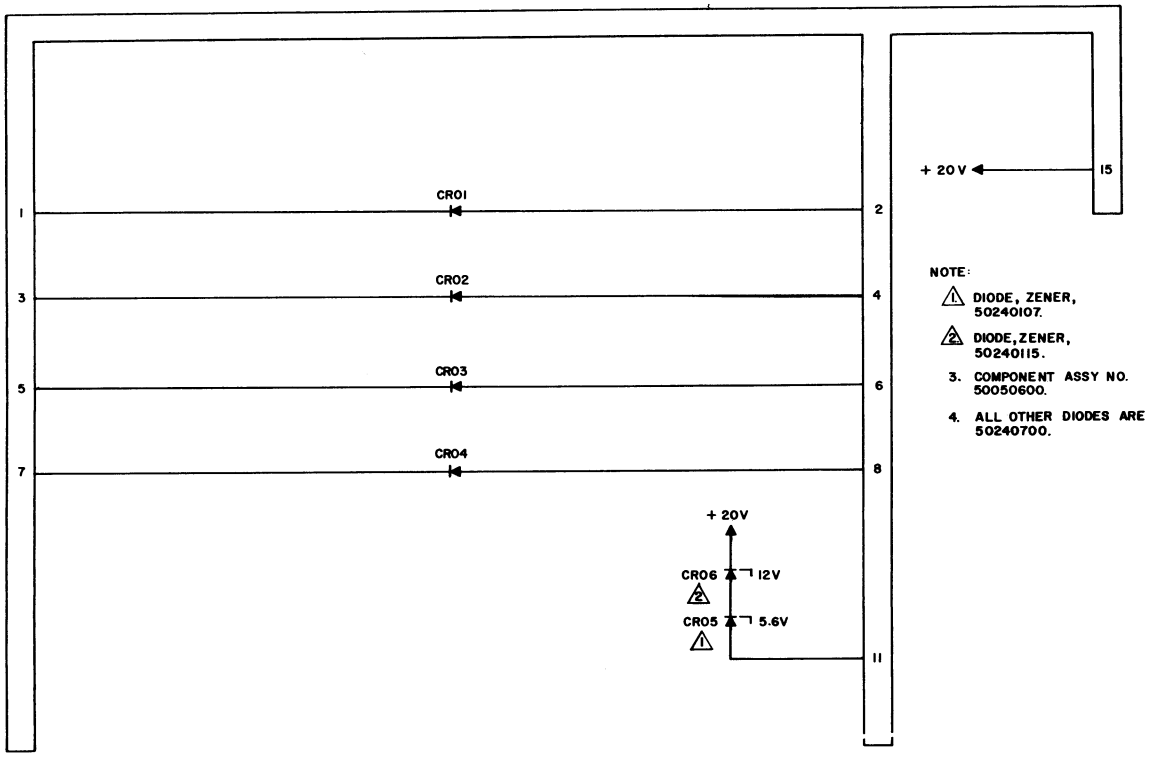
DIODE CARD
GAA

This card has four diodes CR01, 2, 3, and 4 (with space for another). They are used in series with write and erase heads to give the proper voltage levels to prohibit the flow of write and erase currents to the heads, if the voltage checking system BAA, BBA, BCA, or AYA is fired.

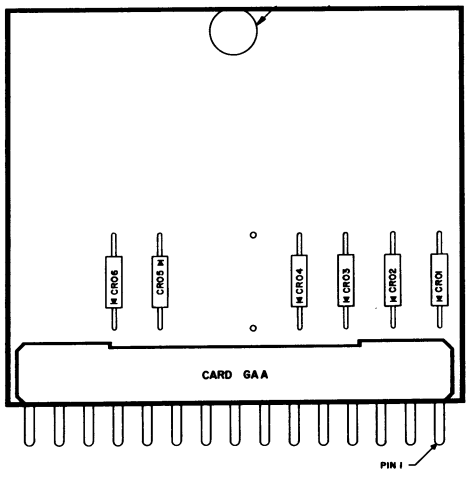
Diodes CR05 and CR06 are used in conjunction with the pin 1 input on the BAA card, or the pin 2 input on the AYA card to detect the state of the +20v supply.

SYMBOL




CR01
CR02
CR03
CR04
CR06
CR05
+ 20V
12V
5.6V
1
2
3
4
5
6
7
8
11
15
NOTE:
1. DIODE, ZENER, 50240107.
2. DIODE, ZENER, 50240115.
3. COMPONENT ASSY NO. 50050600.
4. ALL OTHER DIODES ARE 50240700.

GAA


CR06
CR05
CR04
CR03
CR02
CR01
CARD GAA
PIN 1

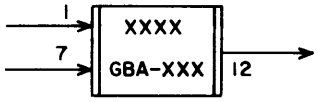
BRAKE-CLUTCH DRIVER

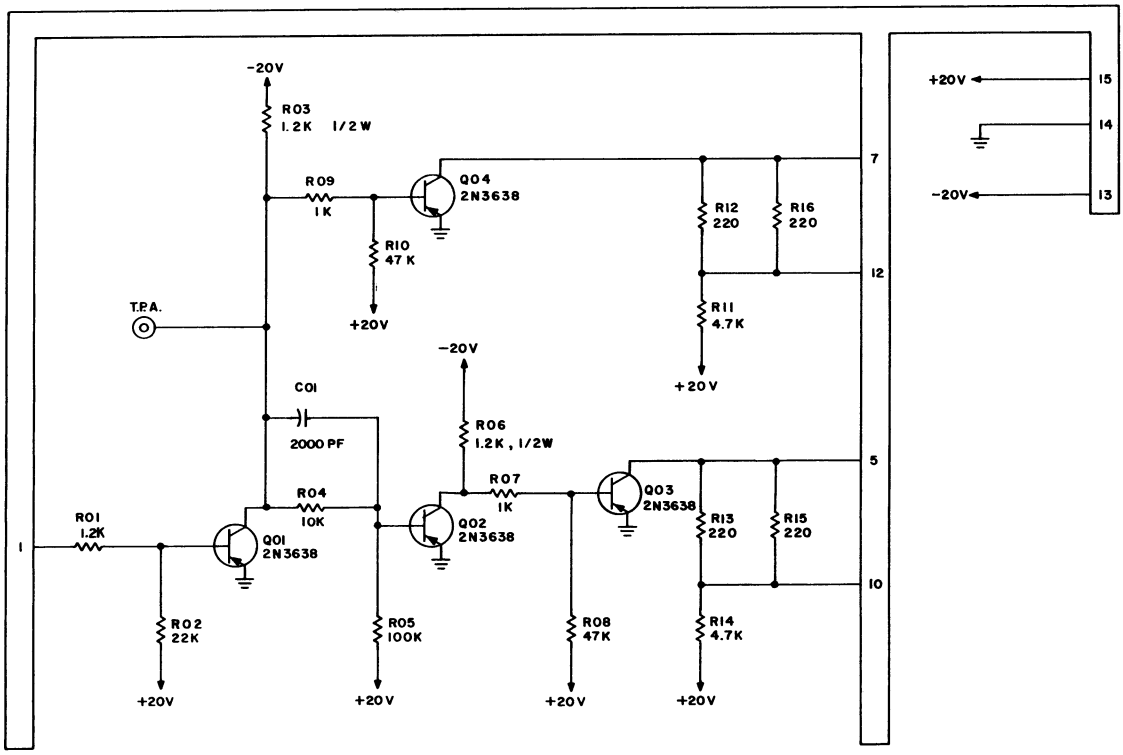
GBA

This circuit is designed for use in the 350 Paper Tape Reader when used with a 1700 Computer. It is similar to the 76A and 76B cards except the input circuit is designed for an input switching excursion of 0.3V at 0 ohm, and -5.4V at 470 ohm.

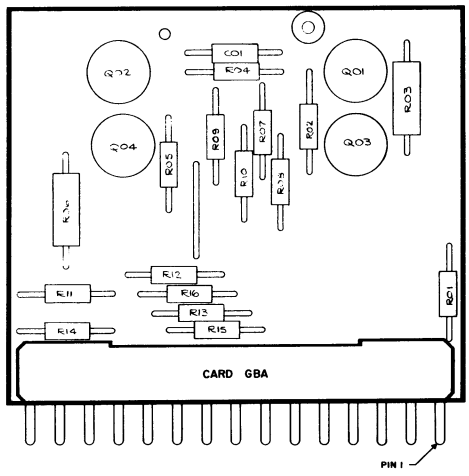
The input signal is inverted twice for the outputs at pins 7 and 12, and three times for the outputs at pins 5 and 10. Thus, one output circuit will always be on and the other off for either polarity of input. Pins 5 and 7 are normally returned to -25V via separate external 200 ohm resistors. Pins 10 and 12 are biased suitably for direct connection to the bases of separate external PNP germanium power transistors operated with grounded emitters. In this intended application, the ON condition is -0.5V max at 125 ma and the OFF condition is -9V (pins 5 and 7). The biased outputs (pins 10 and 12), when operated into the base of external PNP germanium power transistors, have approximate excursions from -1V at -75 ma to 0V at + 1ma.

SYMBOL




-20V
R03
1.2K 1/2W
R09
1K
Q04
2N3638
R10
47K
+20V
T.P.A.
C01
2000 PF
R04
10K
R01
1.2K
Q01
2N3638
R02
22K
+20V
R05
100K
+20V
-20V
R06
1.2K, 1/2W
R07
1K
Q02
2N3638
R08
47K
+20V
R12
220
R16
220
R11
4.7K
+20V
Q03
2N3638
R13
220
R15
220
R14
4.7K
+20V
+20V
-20V
15
14
13
7
12
5
10
1

GBA


C01
R04
Q02
Q01
R03
Q04
R09
R05
R07
R02
Q03
R10
R06
R12
R16
R11
R13
R15
R14
R01
CARD GBA
PIN 1

500 CYCLE TWIN "T" NOTCH NETWORK
GCA

The twin "T" network is used in the disc file servo actuator to "kill" the servo response to an undesirable mechanical response in the carriage.

An operational amplifier is connected between pins 2 and 7 with input at pin 2. The velocity signal from the servo is put into pin 1, and the output from pin 10 is put into the summing point of the servo acceleration operational amplifier.

If the velocity is assumed to be sinusoidal of constant amplitude but varying frequency, the voltage at pin 7 (with the operational amplifier connected) will be a linear increasing function of frequency for frequencies below the twin "T" notch frequency which is set to the unwanted frequency. However, the gain will be less than unity. This occurs because for frequencies below approximately 400 cycles, there is little or no attentuation thru the twin "T". Therefore, resistor R02 divided by R01 + jXc01 determines the gain. At the notch frequency of 500 cycles, no signal gets thru the twin "T", so the gain is determined by R08 divided by R01 + jXc01. At this point the gain rises to approximately 3. Thus, the output at pin 10 is seen to peak-up at 500 cycles. This peaked up signal is added in with the normal acceleration signal. However, since it has undergone one additional phase inversion in the operational amplifier, it will be out of phase with the acceleration signal and thereby subtract out the undesired 500 cycle signal. Potentiometer R03 allows for adjustment of the null depth at 500 cycles.

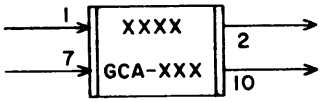
The emitter follower is used to prevent loading on the twin "T", and provide a low impedance driver for the suming resistor R02.

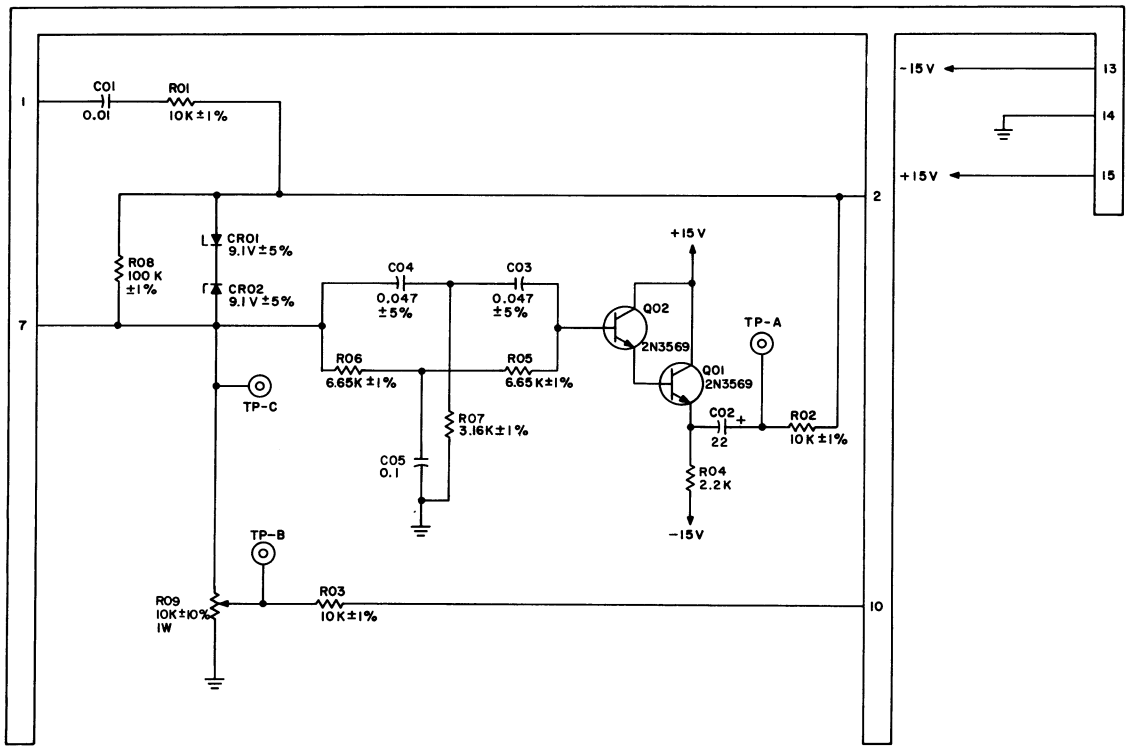
Zerner diodes CR01 and CR02 limit the output voltage of the operational amplifier to approximately $\pm$10v.

VARIABLE FREQUENCY TWIN "T" NOTCH NETWORK
GCB

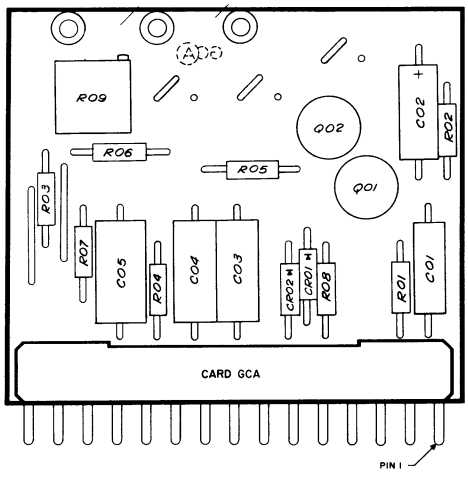
The GCB card is the same as the GCA, except that the null frequency can be adjusted by means of R10, R11, and R12 between approximately 350 and 800 cycles.

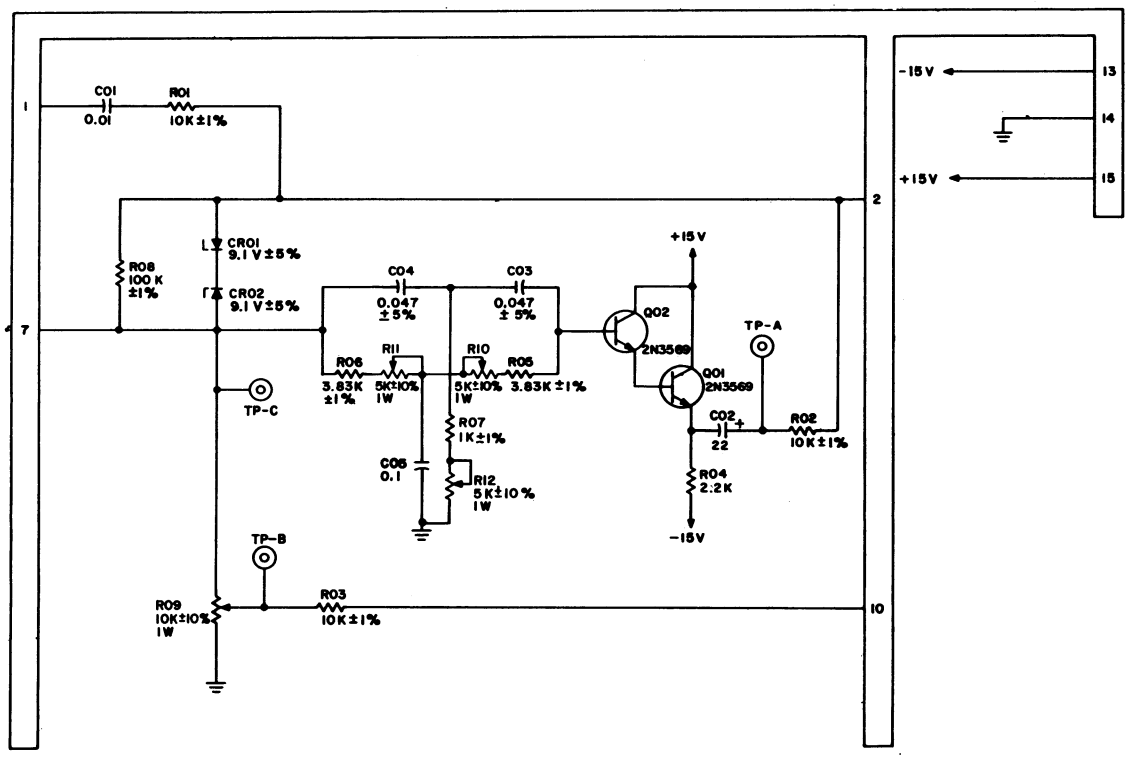
SYMBOL



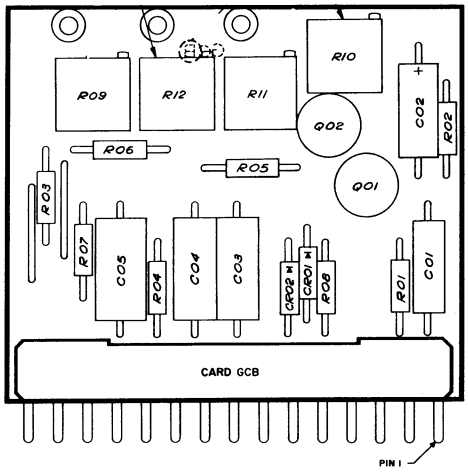

C01
0.01
R01
10K ±1%
CR01
9.1V ±5%
CR02
9.1V ±5%
R08
100 K
±1%
C04
0.047
±5%
C03
0.047
±5%
R06
6.65K ±1%
R05
6.65K ±1%
R07
3.16K ±1%
C05
0.1
TP-C
TP-B
R09
10K ±10%
1W
R03
10K ±1%
+15V
Q02
2N3569
Q01
2N3569
TP-A
C02
22
R02
10K ±1%
R04
2.2K
-15V
-15V
+15V
1
2
7
10
13
14
15

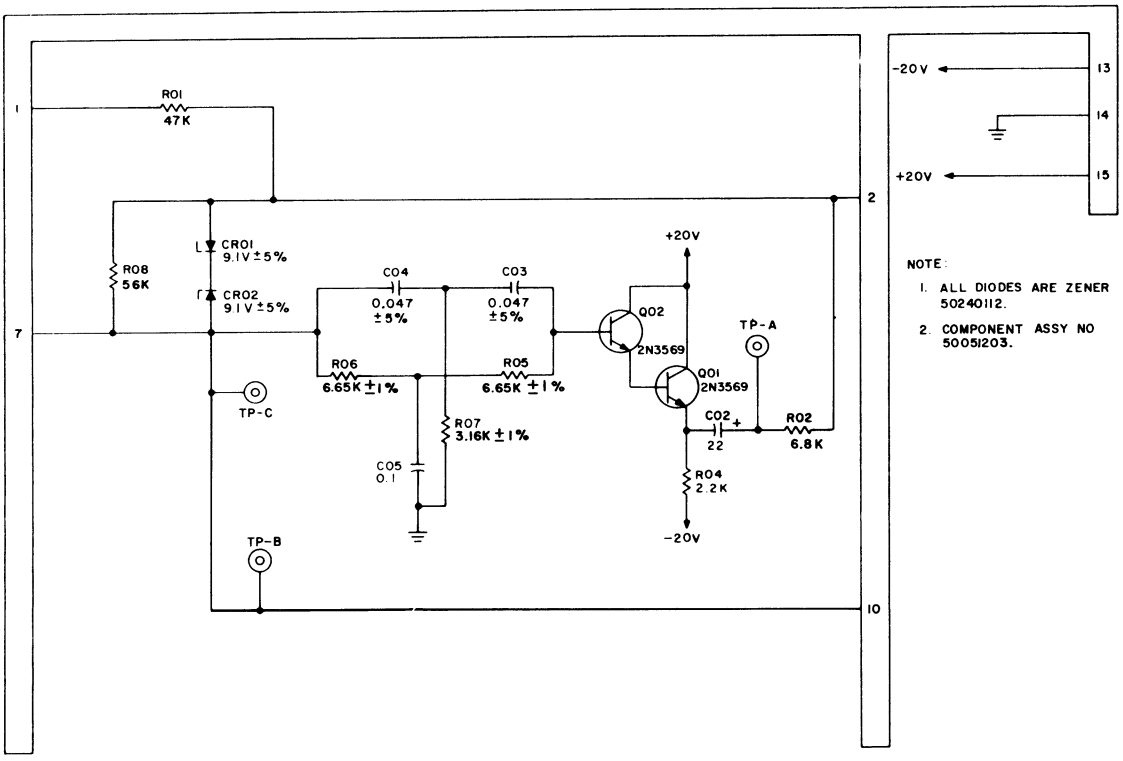
GCA


R09
Q02
C02
R02
R06
R05
Q01
R03
R07
C05
R04
C04
C03
CR02
CR01
R08
R01
C01
CARD GCA
PIN 1

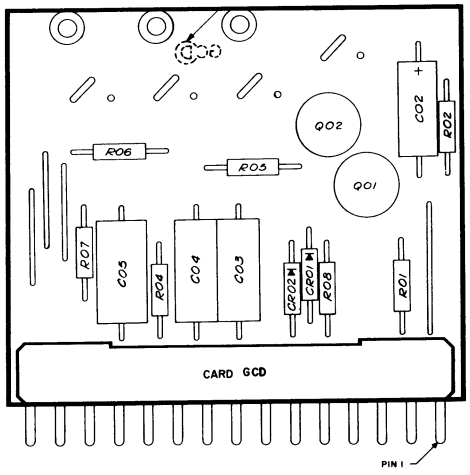

C01
0.01
R01
10K ±1%
CR01
9.1 V ±5%
CR02
9.1 V ±5%
R08
100 K
±1%
C04
0.047
±5%
C03
0.047
±5%
R06
3.83K
±1%
R11
5K±10%
1W
R10
5K±10%
1W
R05
3.83K ±1%
Q02
2N3569
Q01
2N3569
+15V
TP-A
TP-C
C02
22
R02
10K ±1%
R07
1K ±1%
C05
0.1
R12
5K±10%
1W
R04
2.2K
-15V
TP-B
R09
10K±10%
1W
R03
10K ±1%
-15V
+15V
13
14
15
1
2
7
10

GCB


R10
R09
R12
R11
Q02
C02
R02
R06
R05
Q01
R03
R07
C05
R04
C04
C03
CR02
CR01
R08
R01
C01
CARD GCB
PIN 1


R01
47K
CR01
9.1V ±5%
CR02
9.1V ±5%
R08
56K
C04
0.047
±5%
C03
0.047
±5%
R06
6.65K ±1%
R05
6.65K ±1%
R07
3.16K ±1%
C05
0.1
TP-C
TP-B
+20V
Q02
2N3569
Q01
2N3569
TP-A
C02
22
R02
6.8K
R04
2.2K
-20V
-20V
+20V
1
2
7
10
13
14
15
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2. COMPONENT ASSY NO 50051203.

GCD


Q02
C02
R02
R06
R05
Q01
R07
C05
R04
C04
C03
CR02
CR01
R08
R01
CARD GCD
PIN 1

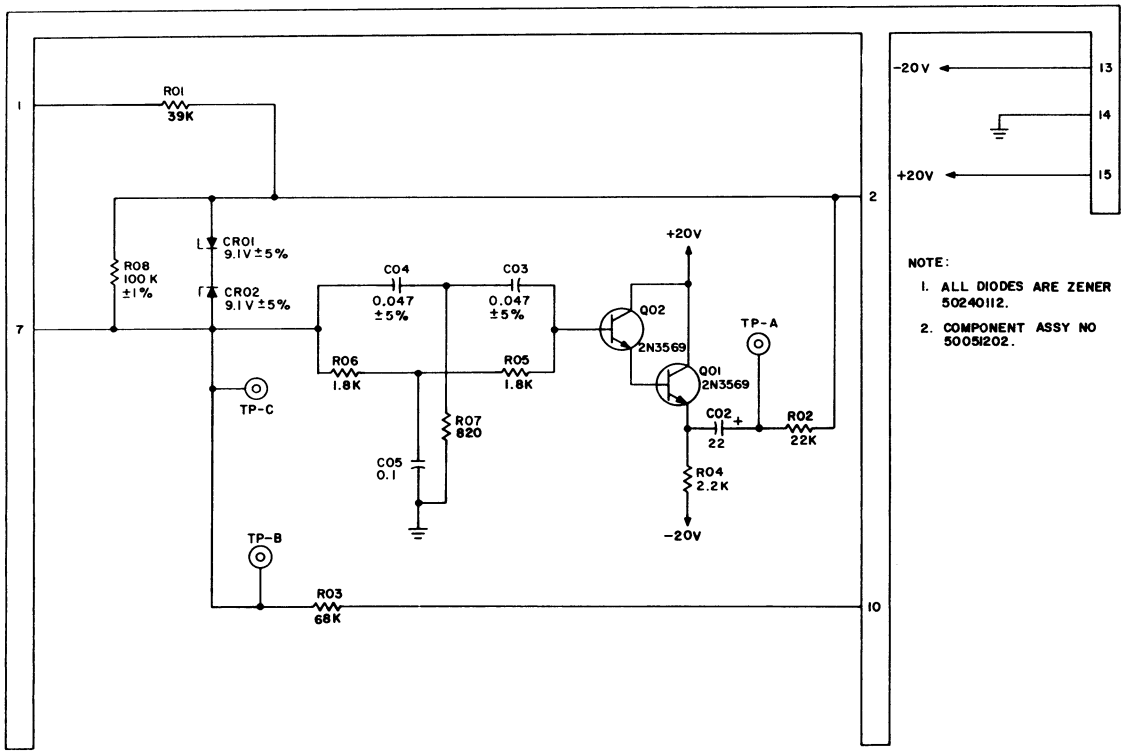
NOTCH NETWORKS
GCC, GCD

The twin "T" networks are intended to be used in cascade to attenuate the disk file servo response at frequencies of undesirable mechanical resonances of the carriage.

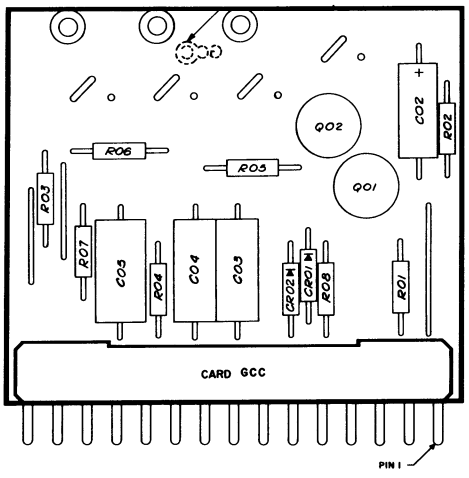
An operational amplifier is connected between pins 2 and 7 of both the GCC and GCD cards with input at pin 2. Pin 1 of the GCD is connected to the output of the acceleration amplifier. Pin 7 or 10 of the GCD is connected to pin 1 of the GCC. Pin 10 of the GCC is then connected to the input of the acceleration amplifier. This arrangement provides attenuation of the acceleration signal from approximately 450 cycles to approximately 2 KC.

At the notch frequency, 500 cycles for the GCD and 1800 cycles for the GCC, there is very little attenuation through the twin "T". The signal at these frequencies is fed back out of phase with the input signal, thereby attenuating the output of the acceleration signal.

SYMBOL



GCC



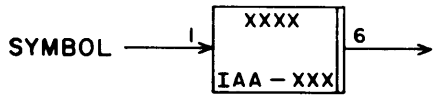
6-GCC, GCD-2

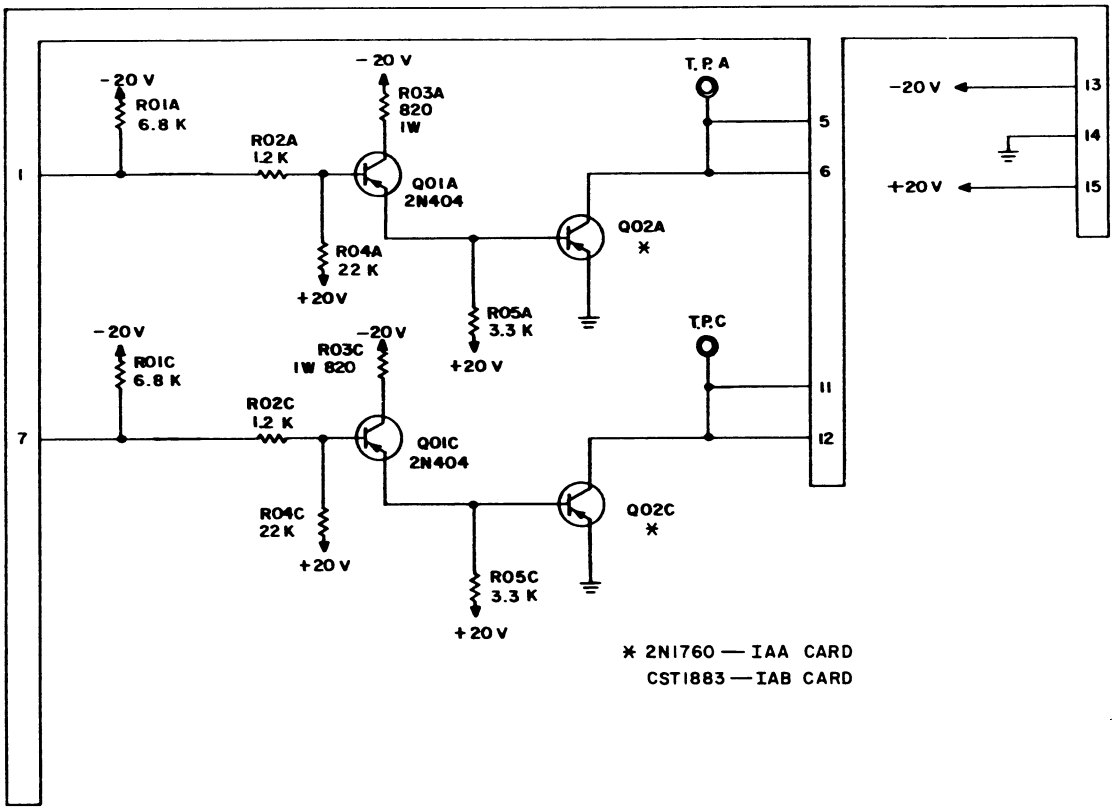
RELAY PULLER
IAA, IAB

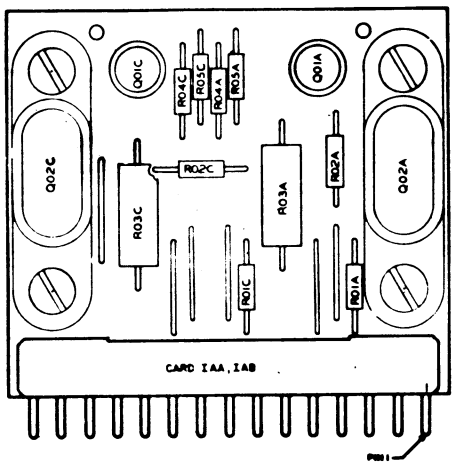
This circuit is used to drive inductive loads such as relays and solenoids and loads with high current surges such as incandescent lamps and the discharge of capacitors. It is particularly useful in driving loads up to 0.6 amp which are terminated at negative voltages from -5v to -36v. IAB cards drive loads to 0.4 amp.

The relay puller circuit can also be used as a slow L---card. The input-output voltage levels are the same for both cards.

The input stage of the relay puller circuit has its transistor connected as an emitter follower with the collector returned to -20v through a limiting resistor R03. The first stage emitter follower current does not flow through the load as it does in circuits such as the 55 card. The only current flowing to the load in the turnoff condition is the leakage current of the output transistor. The circuit limits collector voltage on Q01 to -20v; Q02 may have excursions to -36v. Turnon time is 5 usec maximum and turnoff switching is 25 usec maximum.




-20 V
R01A
6.8 K
R02A
1.2 K
-20 V
R03A
820
1W
T.P.A
Q01A
2N404
Q02A
*
R04A
22 K
+20V
R05A
3.3 K
+20 V
-20V
R01C
6.8 K
R03C
1W 820
-20V
T.P.C
R02C
1.2 K
Q01C
2N404
Q02C
*
R04C
22K
+20 V
R05C
3.3 K
+20 V
-20 V
+20 V
1
7
5
6
11
12
13
14
15
* 2N1760 — IAA CARD
CST1883 — IAB CARD

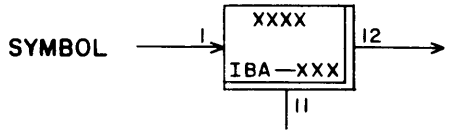

Q01C
R04C
R03C
R04A
R03A
Q01A
Q02C
R02C
R03C
R03A
R02A
Q02A
R01C
R01A
CARD IAA, IAB

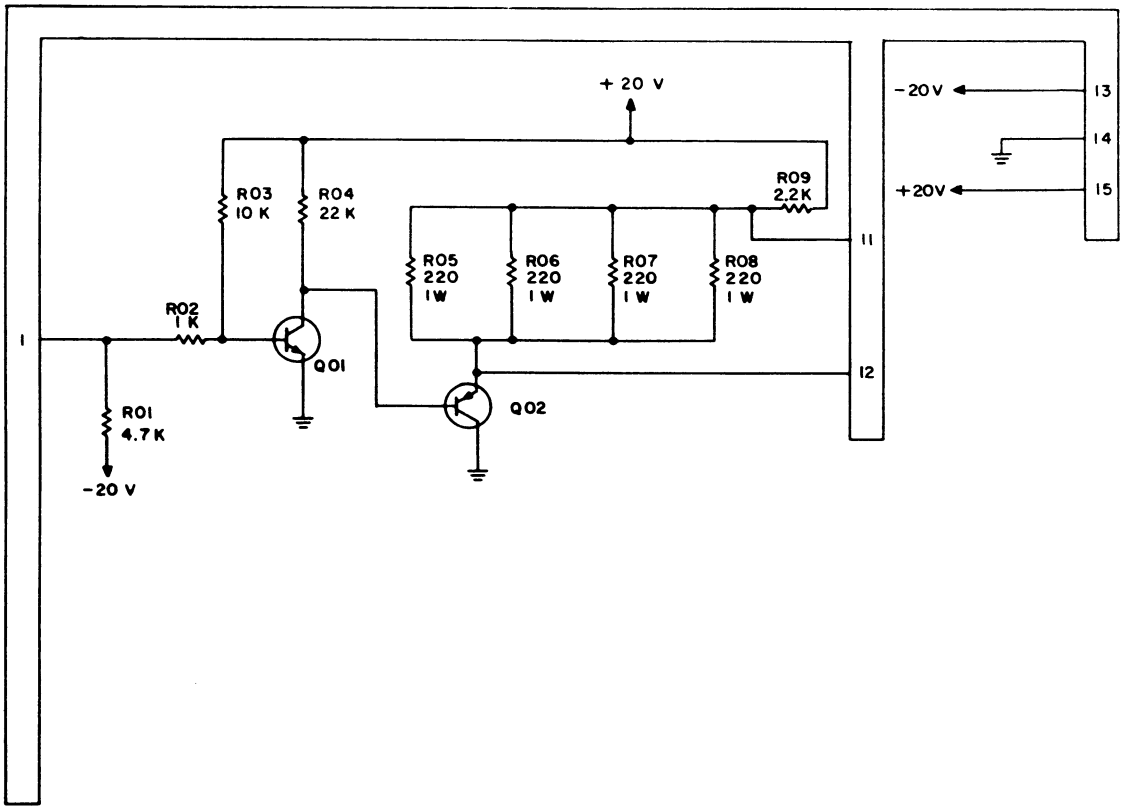
POWER EMITTER FOLLOWER
IBA

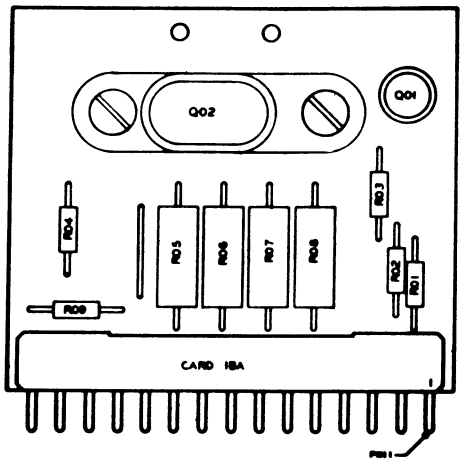
This circuit, used with a solid-state H switch (capstan drive circuit), drives diagonally opposite legs of the switch. A separate card of this type drives a switching transistor which provides a 2-msec double-magnitude current pulse to reduce actuation time.

The circuit differs from the regular inverter circuit in that the output load is returned to +20v instead of -20v.

Turnon time varies from 1 to 20 usec with the current limiting resistor output connected to +20v. Turnoff switching ranges from 5 to 50 usec. Loads on pins 11 and 12 should require a total of 0.6 amp or less and be terminated to -12v or less.




+ 20 V
-20V
+20V
13
14
15
R03
10 K
R04
22 K
R09
2.2K
R05
220
1W
R06
220
1 W
R07
220
1 W
R08
220
1 W
11
R02
1 K
1
Q01
12
Q02
R01
4.7 K
-20 V


Q02
Q01
R04
R05
R06
R07
R08
R03
R02
R01
R09
CARD IBA

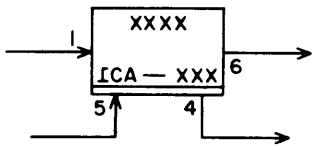
DUAL DRIVER

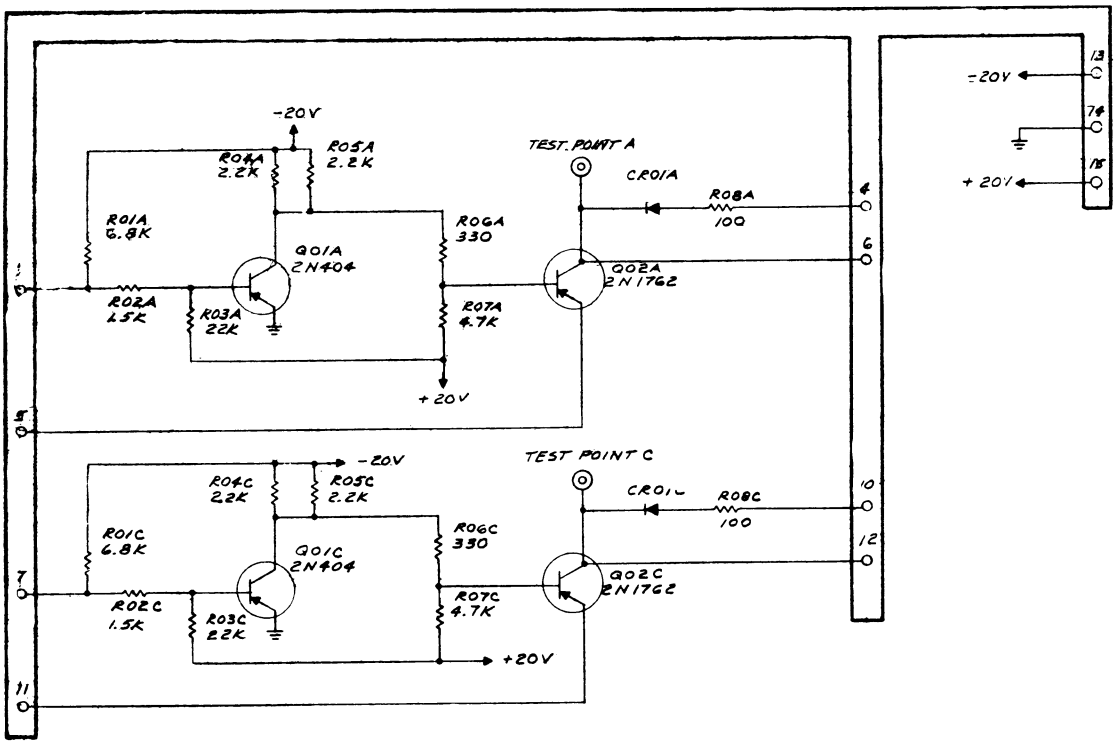
ICA

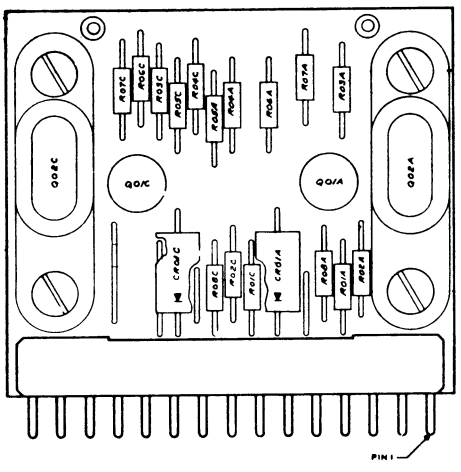
This circuit was designed to drive stepping switches and other inductive loads in the 180 Data Collector. It is particularly useful in driving loads up to 0.4 amp which are terminated at negative voltages from -5v to -60v. A small power transistor in its output circuit allows it to be used for driving incandescent lamps or discharging capacitors where the surge current reduces to 0.4 ampere within 50 milliseconds.

The circuit contains several differences when compared to more conventional output drivers. Each of the two circuits has an output that is double inverting from the first input (pin 1, 7) and noninverting from the second input (pin 5, 11). Both inputs must be driven toward ground (+ AND) to cause the output to be driven toward ground. The first input operates from normal logic "0" (-1/2v) and logic "1" (-3v) levels. The second input may be grounded directly or switched to ground by a circuit such as the IAA or ICA, which has a switching capability equal to the output of the ICA card. To switch off completely, the second input should be allowed to go to -15v. CR01 and R08 are available at pins 4, 10 and protect output transistors from inductive kicks when clamped to the load termination voltage (-60v or less).

SYMBOL




-20V
R04A 2.2K
R05A 2.2K
R01A 6.8K
R02A 1.5K
R03A 22K
Q01A 2N404
R06A 330
R07A 4.7K
+20V
TEST POINT A
CR01A
R08A 100
Q02A 2N1762
-20V
R04C 2.2K
R05C 2.2K
R01C 6.8K
R02C 1.5K
R03C 22K
Q01C 2N404
R06C 330
R07C 4.7K
+20V
TEST POINT C
CR01C
R08C 100
Q02C 2N1762
-20V
+20V
+20V
1
5
7
11
4
6
10
12
13
14
15


Q02C
Q01C
Q01A
Q02A
PIN 1

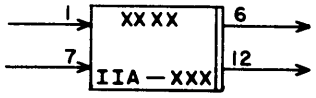
WRITE DRIVER
IIA

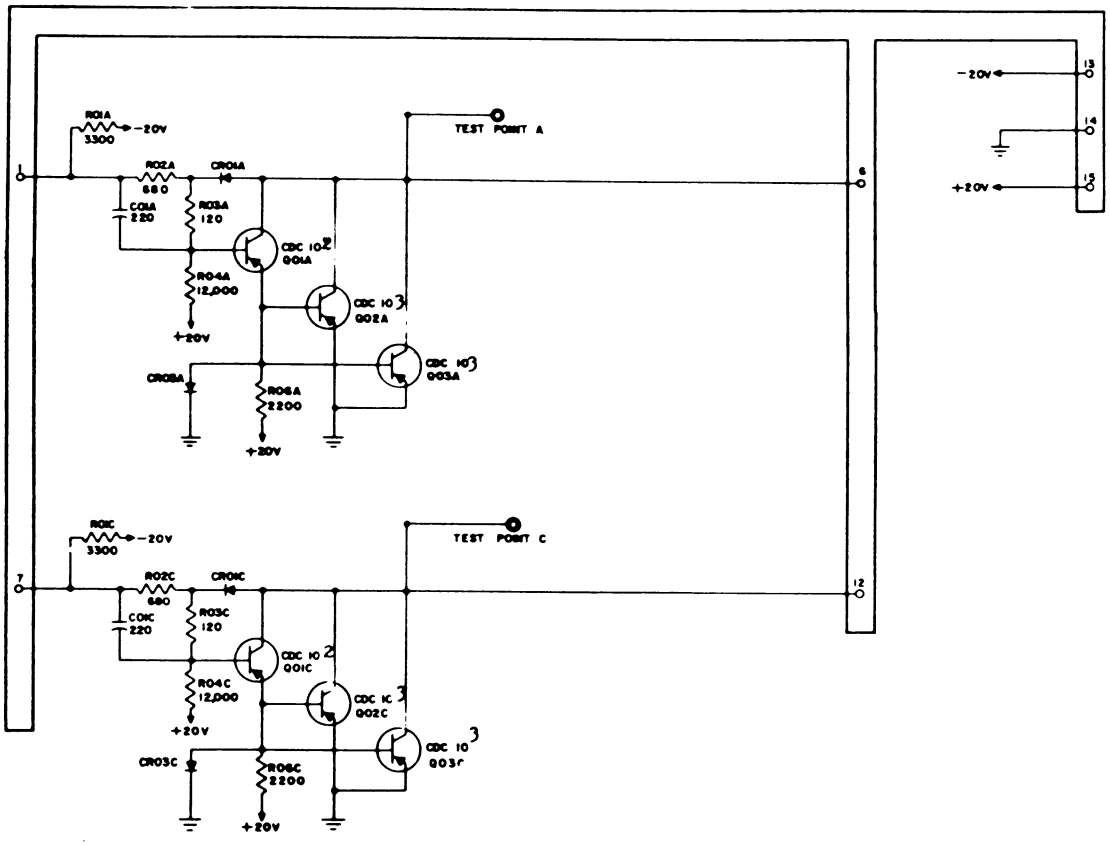
The write driver circuit switches the current through the write heads during a write operation. Each card contains two independent drive circuits whose outputs are connected to opposite ends of the windings of the write head.

The circuit consists of transistor Q01, connected as an emitter follower, and transistors Q02 and Q03 connected in parallel as amplifiers. A "0" input results in 0v at the base of Q01. The emitter of Q01 is clamped to ground by CR03; neither Q02 nor Q03 conduct. Consequently, no current flows to the output pin.

A "1" input signal causes Q01 to conduct; conduction is held below saturation by feedback diode CR01. The negative voltage applied to the bases of Q02 and Q03 causes these transistors to conduct. Current, therefore, flows through the emitter of Q02 and Q03 to the collector and then to the output pin. Maximum output current is 160 ma to a load terminated to -20v or less.

SYMBOL




-20V
TEST POINT A
+20V
TEST POINT C
CARD IIA

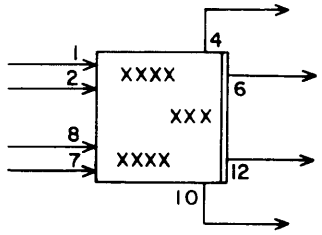
FLIP-FLOP WRITE DRIVER
IJA

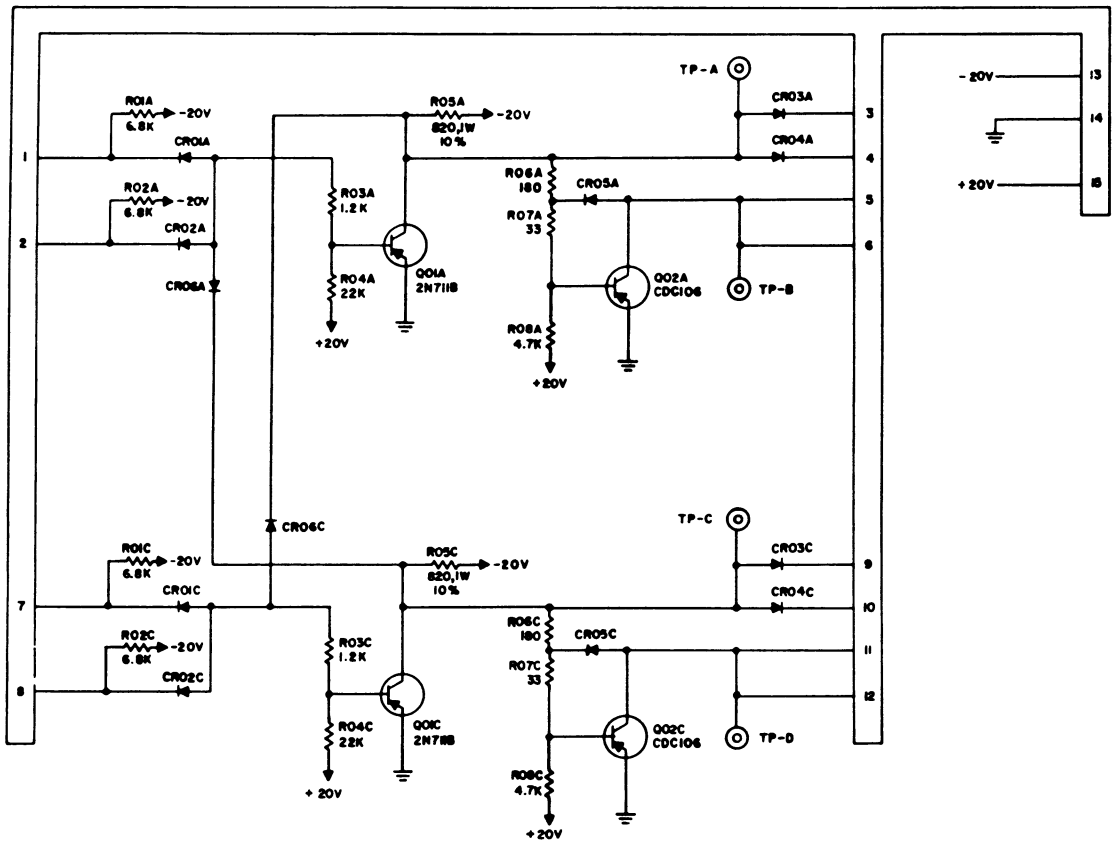
A flip-flop and write driver circuit are combined on one card (refer to IIA write driver discussion).

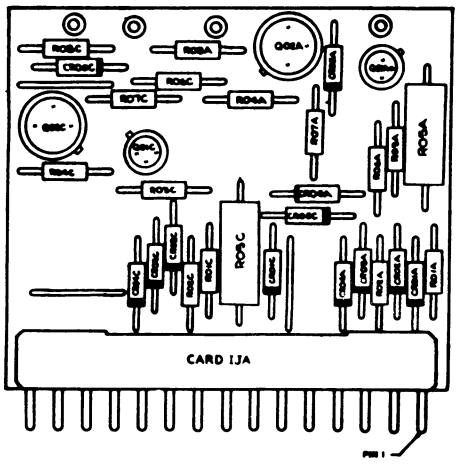
The circuit consists of two transistors (Q01A and Q01C) connected as a flip-flop, each with two OR inputs (diodes CR01 and CR02). Each side of the flip-flop is provided with two AND outputs (diodes CR03 and CR04). The remainder of the flip-flop output is used to drive transistors Q02A and Q02C, which supply up to 160 ma output load.

Because of the double inversion in this circuit, continuous "1" inputs to both sides of the flip-flop turn off both Q02A and Q02C to shut off write current.

SYMBOL




TP-A
TP-B
TP-C
TP-D
-20V
+20V
CR01A
CR02A
CR03A
CR04A
CR05A
CR06A
CR06C
CR01C
CR02C
CR03C
CR04C
CR05C
R01A
R02A
R03A
R04A
R05A
R06A
R07A
R08A
R01C
R02C
R03C
R04C
R05C
R06C
R07C
R08C
Q01A
2N718B
Q02A
CDC106
Q01C
2N718B
Q02C
CDC106


CARD IJA

OUTPUT AMPLIFIER
IKA

The output amplifier card is used to interface from standard logic signals (0 to -3v) to equipment operating from excursions of +12v to -2v. One or two receivers may be connected to each amplifier circuit. Each receiver may be on a separate line and has a series 220-ohm input resistor. The other end of this resistor is clamped at +6.5v in the positive direction and at ground in the negative direction. It is also connected to the emitters of two gating transistors in each receiver.

Two identical circuits are provided on each card. Each circuit includes four transistors. Q01 inverts standard logic input signals. Q02 supplies current amplification of the inverted signal to provide drive in the positive direction. The output of Q02 is shifted 4 volts negative by CR01 to obtain an excursion above and below ground.

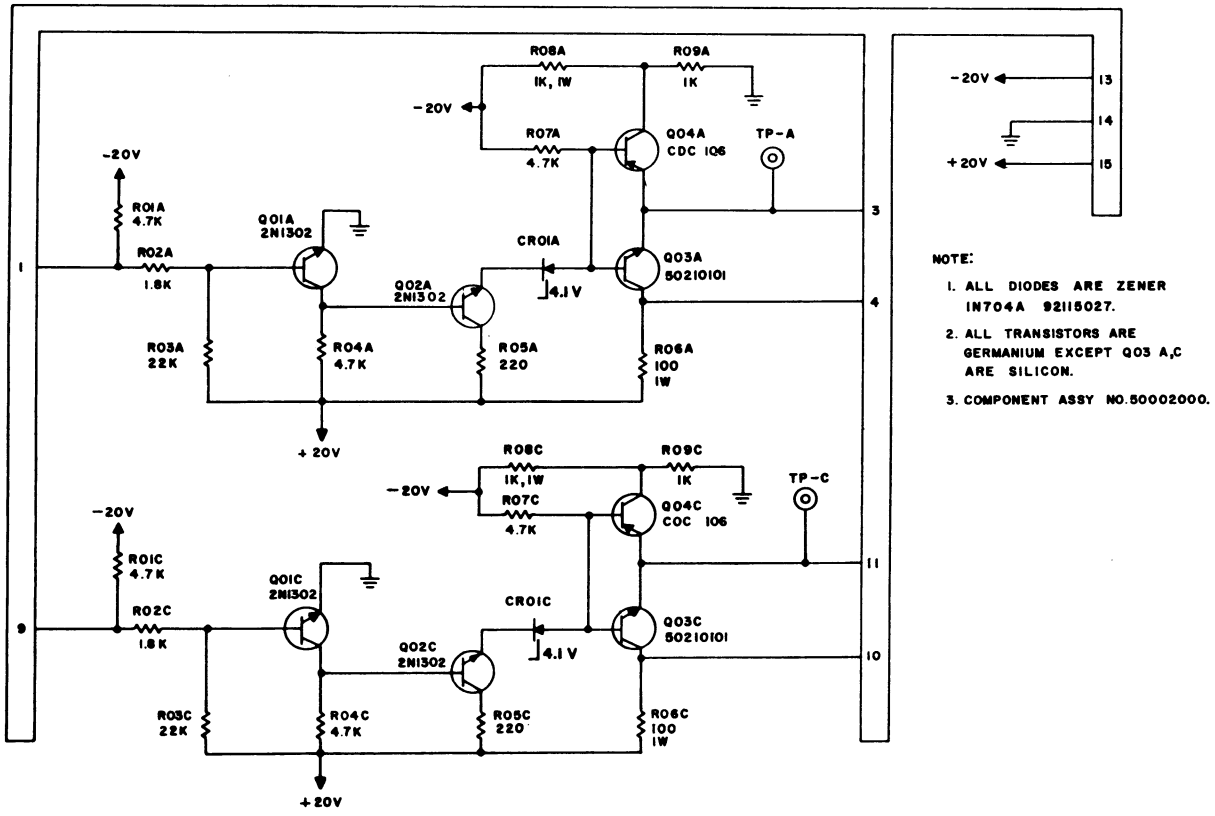
Q03 and Q04 are emitter followers which provide the output drive current. The positive drive current is limited by R06 in the collector of Q03 and the negative drive is limited by R08 in the collector of Q04. R09 limits collector voltage on Q04 during the positive output excursion.

The positive output excursion of +12v will be reduced as the external load increases to about 70 ma. The negative output excursion of -2v has a current capability of about 15 ma.

Rise time to the +10v point is 1 microsecond maximum with a cable capacity of 4400 pf and two equivalent receiver loads in parallel. Fall time to the 0v point is 1 to 2 microseconds with this same load.

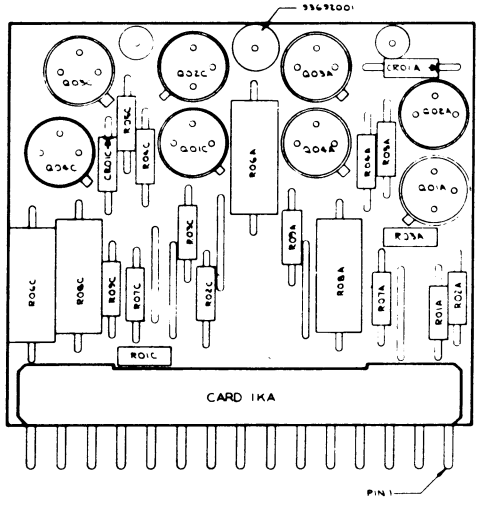
The circuit is subject to overloading the current limiting resistors R05 and R06 if an output is left shorted to ground while the input is a "1".

SYMBOL



NOTE:

1. ALL DIODES ARE ZENER IN704A 92115027.
2. ALL TRANSISTORS ARE GERMANIUM EXCEPT Q03 A,C ARE SILICON.
3. COMPONENT ASSY NO.50002000.

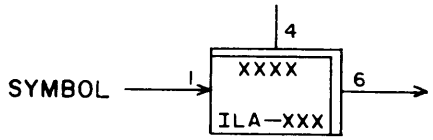


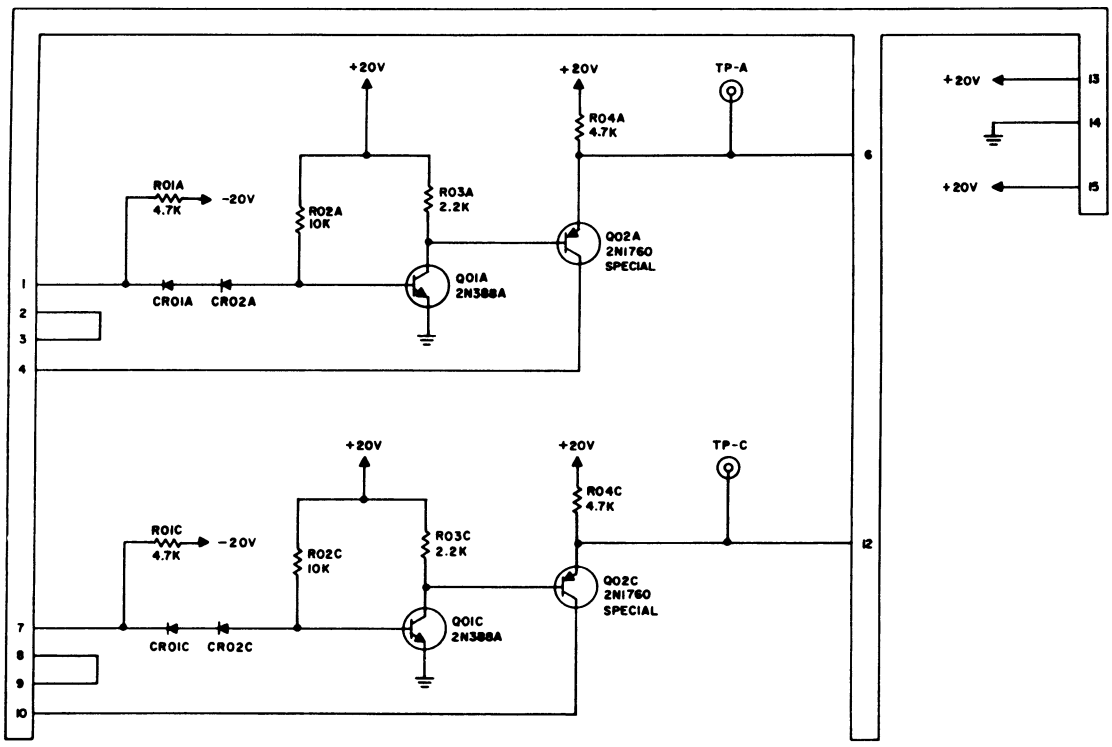
VOICE COIL DRIVER
ILA

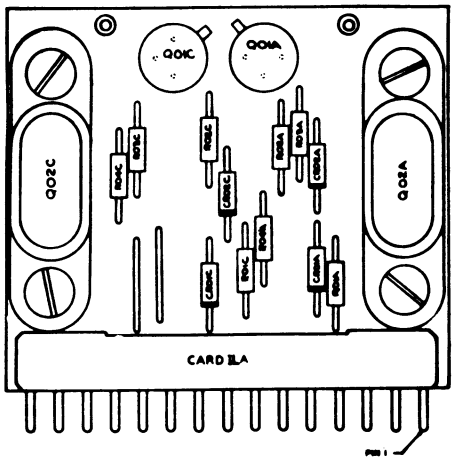
This circuit is used as a relay puller which drives inductive loads terminated at positive voltages of +12v or less.

Two circuits on this card are used as a push-pull capstan coil driver operating directly from a standard flip-flop.

The input stage is an inverting circuit using two forward drop silicon diodes CR01 and CR02 and high gain transistor Q01. The output stage, transistor Q02, is used as an emitter follower to drive a maximum load of 1¼ amperes. Separate grounds to pins 4 and 10 must be provided. Pins 2-3 and 8-9 are provided for interlocking purposes where circuits are paraleled on different ILA cards.




+20V
+20V
TP-A
R04A
4.7K
R01A
4.7K
-20V
R02A
10K
R03A
2.2K
Q02A
2N1760
SPECIAL
Q01A
2N388A
CR01A
CR02A
+20V
13
14
+20V
15
1
2
3
4
6
+20V
+20V
TP-C
R04C
4.7K
R01C
4.7K
-20V
R02C
10K
R03C
2.2K
Q02C
2N1760
SPECIAL
Q01C
2N388A
CR01C
CR02C
7
8
9
10
12


Q01C
Q01A
Q02C
Q02A
CARD ILA

OUTPUT AMPLIFIER

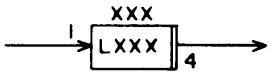
INA

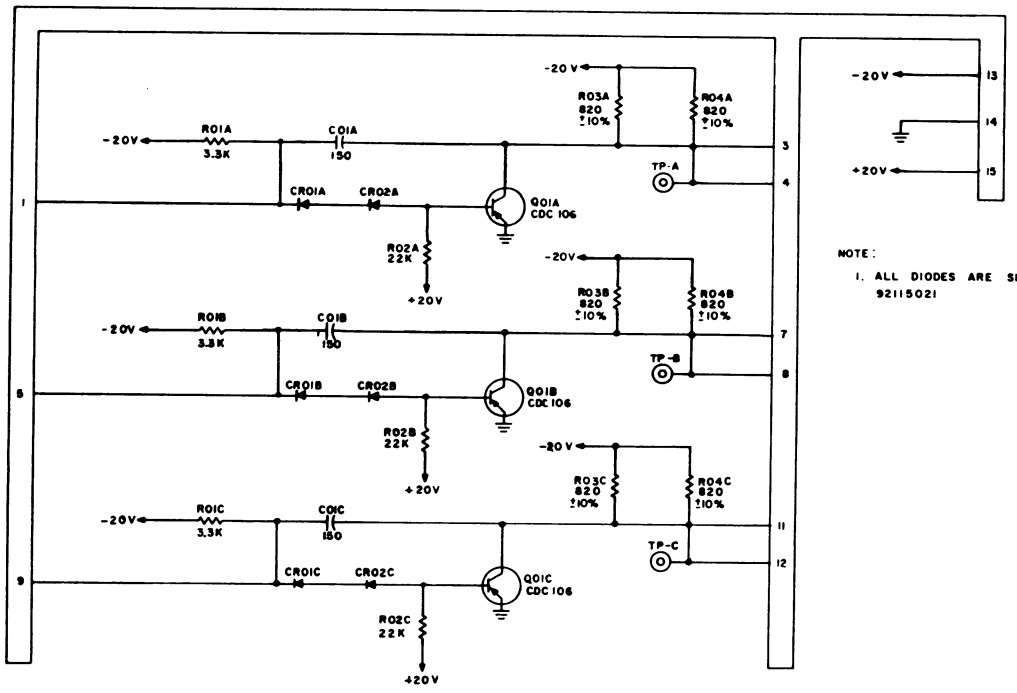
The output amplifier card is used to interface from standard logic signals (0 to -3v) to external equipment operating from excursions of 0 to -6v. The external load impedance is significant in determining the negative excursion and should closely approximate 200 ohms to ground for the standard excursion. This impedance will also approximately match twisted pair lines used in the cables between equipment.

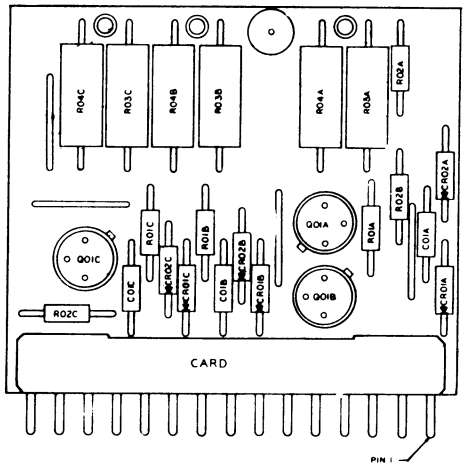
Three identical circuits are used. Each is a switching type inverter with certain variations from a typical output circuit such as the type 62 card. A single stage of gain is used to provide the output current. This requires additional base current drive and is obtained by decreasing the input resistance and using two silicon diodes (CR01, CR02) in the base voltage divider.

With a 200-ohm load to ground, the positive excursion is 0 to -1/2v and the negative excursion is -5 1/2 to -7 1/2v. Rise and fall times are less than 3/4 usec if external cable capacity is 1000 pf or less.

SYMBOL




-20V
R01A
3.3K
C01A
150
R03A
820
±10%
R04A
820
±10%
TP-A
CR01A
CR02A
Q01A
CDC 106
R02A
22K
+20V
R01B
3.3K
C01B
150
R03B
820
±10%
R04B
820
±10%
TP-B
CR01B
CR02B
Q01B
CDC 106
R02B
22K
R01C
3.3K
C01C
150
R03C
820
±10%
R04C
820
±10%
TP-C
CR01C
CR02C
Q01C
CDC 106
R02C
22K
1
3
4
5
7
8
9
11
12
13
14
15
NOTE:
1. ALL DIODES ARE SILICON
92115021


R04C
R03C
R04B
R03B
R04A
R05A
R02A
R01C
R01B
R02B
R01A
C01C
C01B
C01A
CR02C
CR01C
CR02B
CR01B
CR02A
CR01A
Q01C
Q01A
Q01B
R02C
CARD
PIN 1

HEAD SELECTOR
IOB, IOC, IOD

These cards have two circuits, each of which will absorb up to 1.5A from a positive voltage (with the proper external resistor tied in to provide drive).

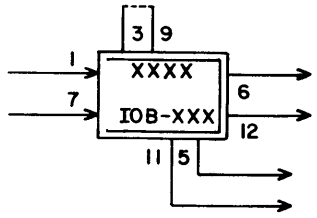
When Q01 is on, Q02 is held off. When Q02 is on, it furnishes base drive for Q03, which will accept up to 1.5A. The collector current for Q02 is determined by R04. For disc pak use, since only one out of 10 10B circuits are on at any time, R04's on various circuits can be shared. To get the proper collector current for Q02 for disc paks, two R02's on various IOB's are tied in parallel to tying pins 3 or 9 together. For the disc file, 16 R04's are paralleled in this way.

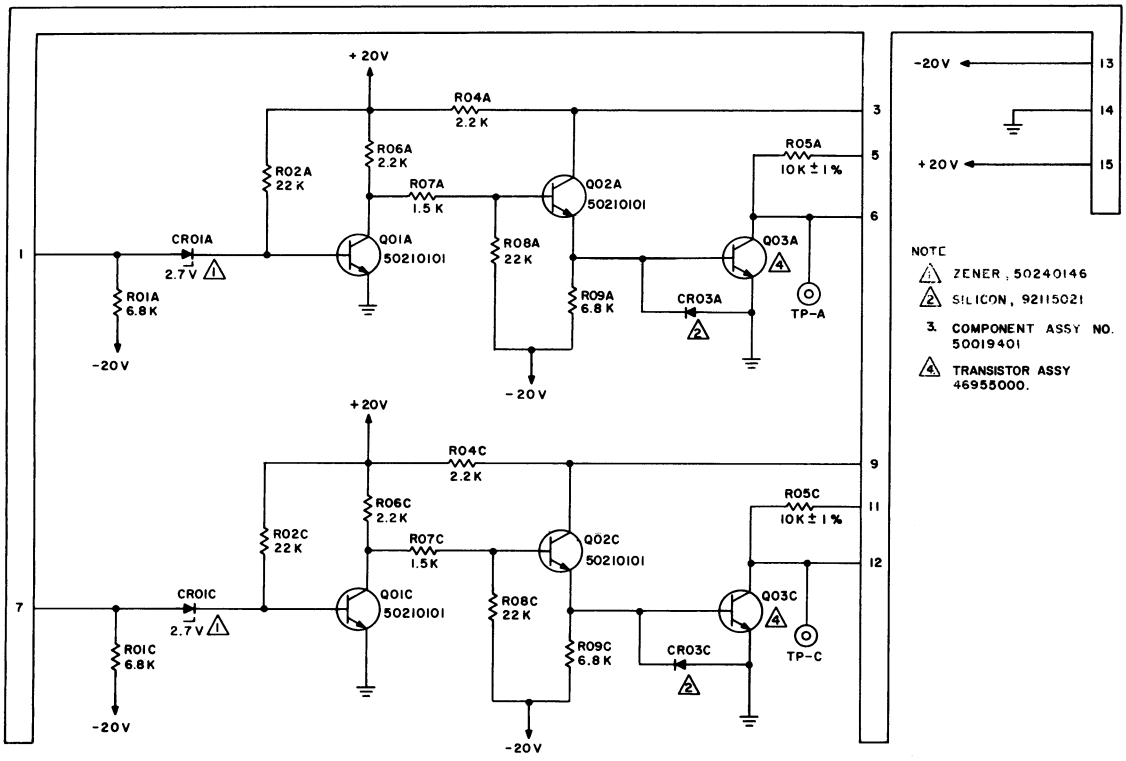
CR01 is a zener diode, used for level translation. The outputs at pins 5 and 11 are used for error detection (see cards ANB, ANC, AND, and AOA).

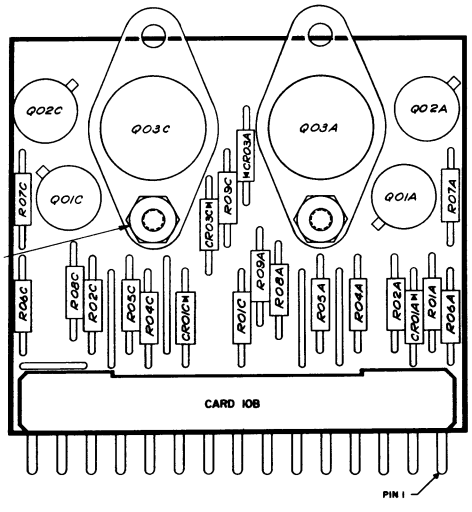
The IOC card is the same as the IOB, except that CR03A, C is replaced by R03A, C to make turn-off faster.

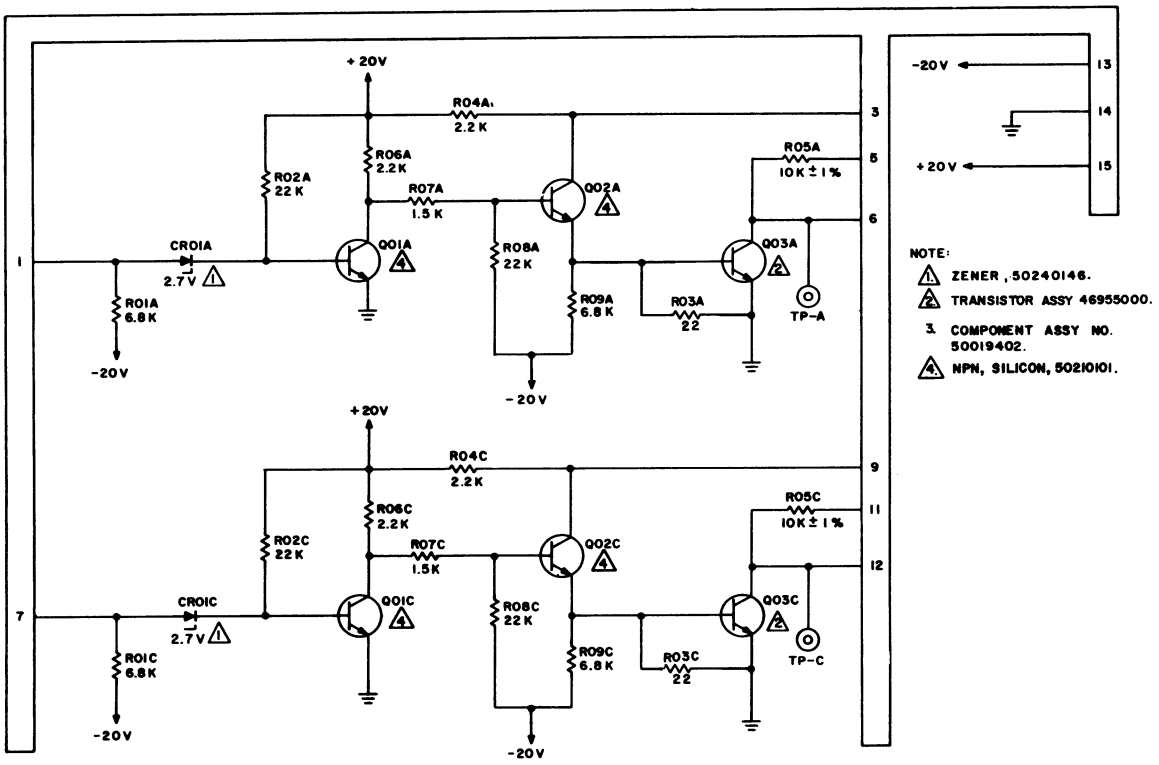
The IOD card is the same as the IOB, except that CR02A, C are added to cut down input noise sensitivity, R09A, C values are changed to make turn off-faster, and the network of C01, CR04, and R10 is added to control turn-on time. In this card I_c = 0.6A.

SYMBOL

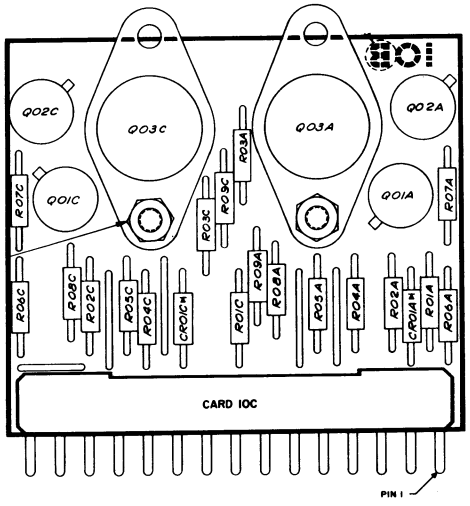


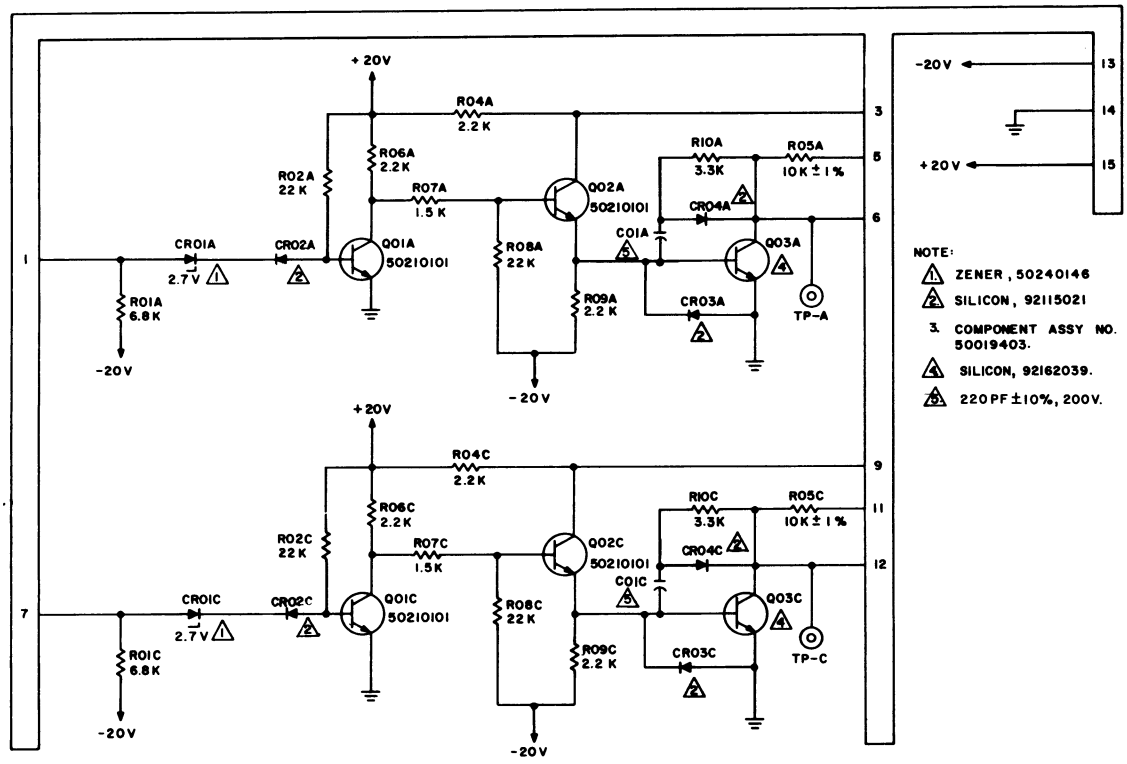

+20V
R04A
2.2 K
R06A
2.2K
R02A
22 K
R07A
1.5 K
Q02A
50210101
R05A
10K ± 1%
CR01A
2.7V
Q01A
50210101
R08A
22K
Q03A
R01A
6.8K
R09A
6.8 K
CR03A
TP-A
-20V
-20V
+20V
R04C
2.2K
R06C
2.2K
R02C
22K
R07C
1.5K
Q02C
50210101
R05C
10K ± 1%
CR01C
2.7V
Q01C
50210101
R08C
22K
Q03C
R01C
6.8K
R09C
6.8K
CR03C
TP-C
-20V
-20V
-20V
+20V
1
3
5
6
7
9
11
12
13
14
15
NOTE
1. ZENER, 50240146
2. SILICON, 92115021
3. COMPONENT ASSY NO. 50019401
4. TRANSISTOR ASSY 46955000.

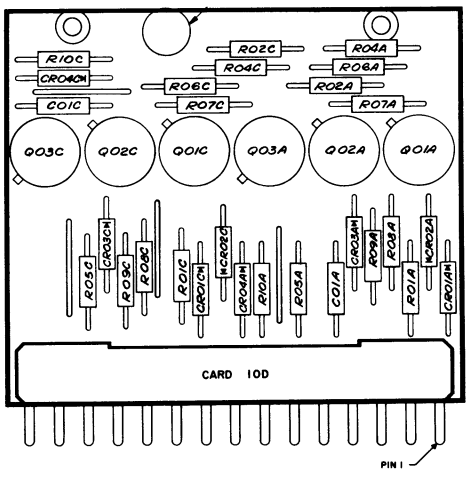

Q02C
Q03C
Q03A
Q02A
Q01C
Q01A
R07C
CR03C
CR03A
R07A
R06C
R08C
R02C
R05C
R04C
CR01C
R01C
R08A
R03A
R04A
R02A
CR01A
R01A
R06A
CARD 10B
PIN 1


+20V
R04A
2.2K
R06A
2.2K
R02A
22K
R07A
1.5K
Q02A
R05A
10K ± 1%
CR01A
2.7V
Q01A
R08A
22K
Q03A
R01A
6.8K
R09A
6.8K
R03A
22
TP-A
-20V
-20V
+20V
R04C
2.2K
R06C
2.2K
R05C
10K ± 1%
R02C
22K
R07C
1.5K
Q02C
CR01C
2.7V
Q01C
R08C
22K
Q03C
R01C
6.8K
R09C
6.8K
R03C
22
TP-C
-20V
-20V
-20V
+20V
-20V
+20V
1
3
5
6
7
9
11
12
13
14
15
NOTE:
1. ZENER, 50240146.
2. TRANSISTOR ASSY 46955000.
3. COMPONENT ASSY NO. 50019402.
4. NPN, SILICON, 50210101.

IOC


Q02C
Q03C
Q03A
Q02A
Q01C
Q01A
R07C
R03A
R03C
R03C
R06C
R05C
R02C
R03C
R04C
CR01CM
R01C
R08A
R05A
R04A
R03A
CR01AM
R01A
R06A
CARD IOC
PIN 1


+20V
R04A
2.2K
R06A
2.2K
R02A
22K
R07A
1.5K
Q02A
50210101
R10A
3.3K
R05A
10K ± 1%
CR04A
C01A
Q03A
CR01A
2.7V
CR02A
Q01A
50210101
R08A
22K
R09A
2.2K
CR03A
TP-A
R01A
6.8K
-20V
-20V
-20V
+20V
R04C
2.2K
R06C
2.2K
R02C
22K
R07C
1.5K
Q02C
50210101
R10C
3.3K
R05C
10K ± 1%
CR04C
C01C
Q03C
CR01C
2.7V
CR02C
Q01C
50210101
R08C
22K
R09C
2.2K
CR03C
TP-C
R01C
6.8K
-20V
-20V
-20V
1
3
5
6
7
9
11
12
-20V
13
14
+20V
15
NOTE:
1. ZENER, 50240146
2. SILICON, 92115021
3. COMPONENT ASSY NO. 50019403.
4. SILICON, 92162039.
5. 220PF ±10%, 200V.

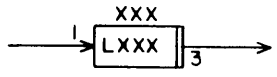

R10C
CR04CH
C01C
R02C
R04C
R06C
R07C
R04A
R06A
R02A
R07A
Q03C
Q02C
Q01C
Q03A
Q02A
Q01A
R05C
CR03CH
R03C
R06C
R01C
CR01CH
MICR02C
CR04AH
R04A
R05A
C01A
CR03AH
R09A
R06A
R01A
MCR02A
CR01AH
CARD 10D
PIN 1

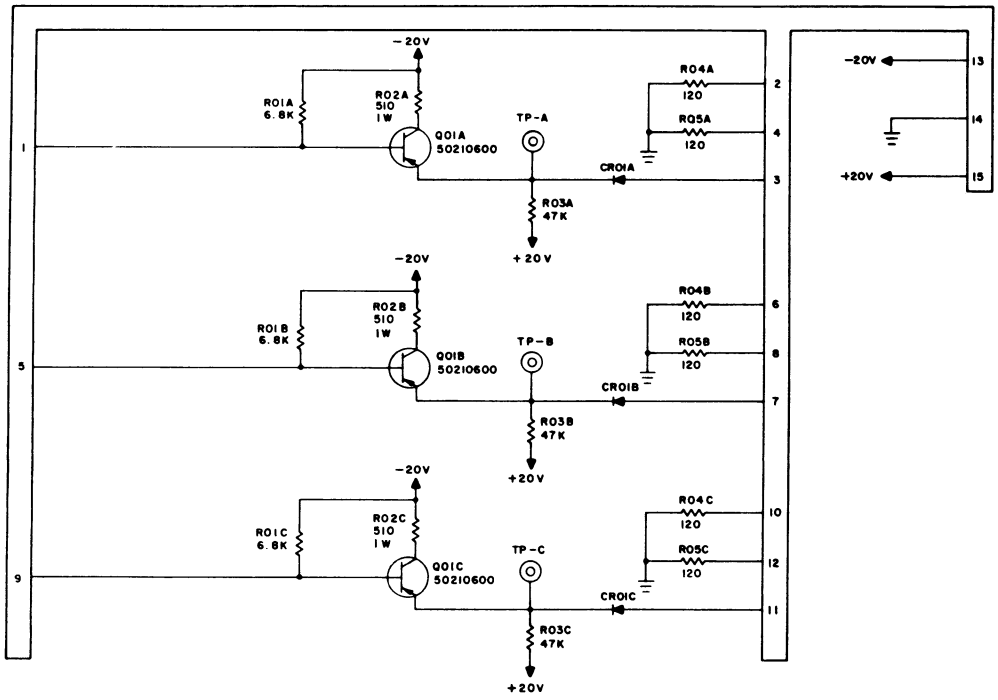
OUTPUT AMPLIFIER
IPA

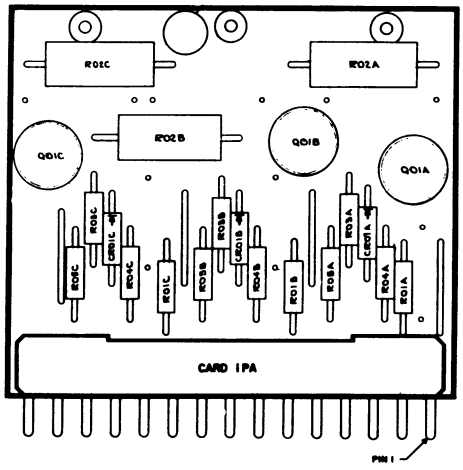
The IPA was initially designed to be used in a 699 tester adapter in conjunction with 9131 Tape Transports which have OPA receiver cards. The input is designed for standard logic signals (0 to -3v). Its output switches from 0v to -1.8v. The output should be terminated at the end of the line to match the impedance characteristic of the line. The IPA has resistors available by jumpering to its output pins for matching line impedance at the input to the line. In this application, one IPA was called on to drive six receivers (OPA) in parallel over a 25-ft. max. coax line. The IPA can be used to drive a twisted pair line if the line noise level is kept sufficiently low.

A logical "0" input (0v) provides a 0v output, and a logical "1" input (-3v) provides a -1.8v output. With a termination of 120 ohms to ground at both ends of the line, the IPA puts out 30 ma @ -1.8v. Switching times are as fast as 100 nsec, but being an emitter follower, it will vary with the switching speed of the input signal. Since the IPA circuit is an emitter follower, the output voltage will equal the input voltage, $-V_{BE}$ of Q01 - V_f of CR01. There are three identical circuits per card.

SYMBOL




-20V
R01A
6.8K
R02A
510
1W
Q01A
50210600
TP-A
CR01A
R03A
47K
+20V
R04A
120
R05A
120
1
2
3
4
-20V
+20V
13
14
15
-20V
R01B
6.8K
R02B
510
1W
Q01B
50210600
TP-B
CR01B
R03B
47K
+20V
R04B
120
R05B
120
5
6
7
8
-20V
R01C
6.8K
R02C
510
1W
Q01C
50210600
TP-C
CR01C
R03C
47K
+20V
R04C
120
R05C
120
9
10
11
12

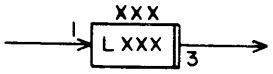

R01C
R02A
R02B
Q01C
Q01B
Q01A
CARD IPA
PIN 1

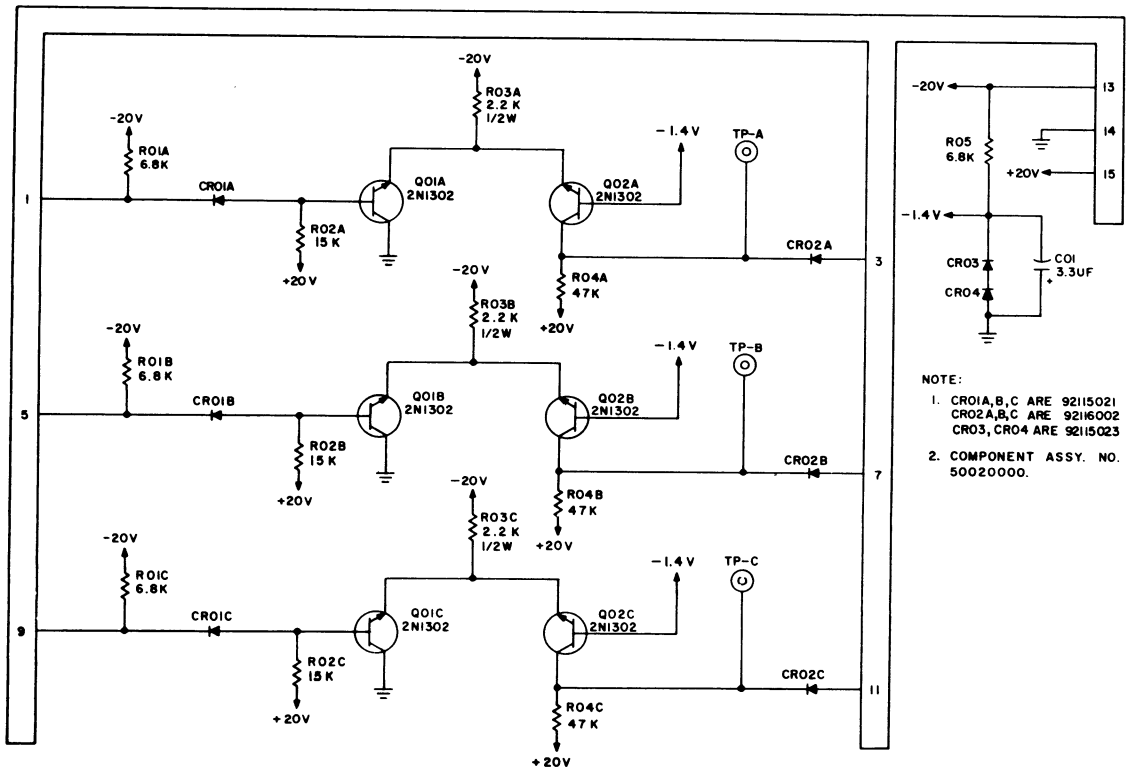
OUTPUT AMPLIFIER
IQA

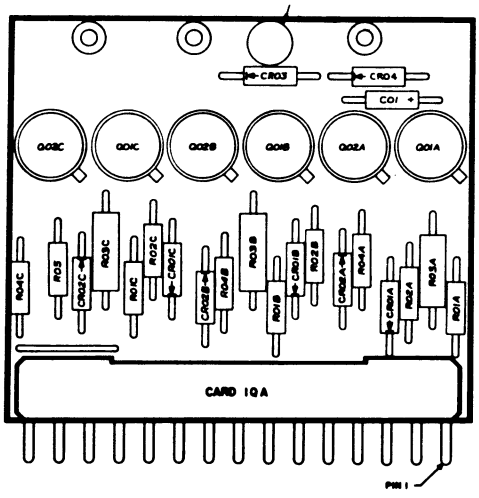
The output amplifier card, IQA, is used to interface from standard logic signals (0 to -3v) to a "n" type line driving a current mode receiver. Up to 8 outputs may be paralleled for daisy-chaining between tape handlers and an adaptor. Daisy-chaining is a term used to describe a series connection of an IQA output in one transport to a corresponding IQA output in another transport and so on to the end transport in the chain where the IQA output is connected to the line going to a receiver in the adaptor.

There are three identical circuits on each card and each circuit includes two transistors. Q01 and Q02 form a differential amplifier. CR03 and CR04 provide a nominal -1.4v at the base of Q02 for the switching threshold. Emitter resistor R03 provides 8 ma of output drive at -1v. Output diode CR02 is for isolation of "OFF" drivers from an "ON" driver in a daisy-chain connection. The IQA has a switching time of 0.5 usec maximum in either direction. A logical "1" input turns the driver on with the output at -1v. A logical "0" input turns the driver off with the receiver input circuitry determining the "0" line voltage. To avoid ringing from line reflections, the end of the line should be terminated approximately in its characteristic impedance.

SYMBOL




-20V
R01A 6.8K
CR01A
R02A 15K
+20V
R03A 2.2K 1/2W
Q01A 2N1302
Q02A 2N1302
-1.4V
TP-A
CR02A
R04A 47K
R01B 6.8K
CR01B
R02B 15K
R03B 2.2K 1/2W
Q01B 2N1302
Q02B 2N1302
TP-B
CR02B
R04B 47K
R01C 6.8K
CR01C
R02C 15K
R03C 2.2K 1/2W
Q01C 2N1302
Q02C 2N1302
TP-C
CR02C
R04C 47K
1
3
5
7
9
11
13
14
15
R05 6.8K
CR03
CR04
C01 3.3UF
NOTE:
1. CR01A,B,C ARE 92115021
CR02A,B,C ARE 92116002
CR03, CR04 ARE 92115023
2. COMPONENT ASSY. NO. 50020000.


CR03
CR04
C01
Q03C
Q01C
Q03B
Q01B
Q02A
Q01A
CARD 1QA
PIN 1

OUTPUT AMPLIFIER
ISC

The ISC output amplifier card, initially designed for 601 tape transports and controllers operating on a time-shared line, is used to interface from standard logic signals (-½ to -3v) to line signals of 0 to +2v. The external load impedance determines the positive output excursion (for example 60 ohm = +2v, 100 ohm = +3v). It is designed as part of an overall line transmission system in which considerations of cable type, cable length, terminations, crosstalk, paralleling of output and input amplifiers, simplicity of biasing voltages, and speed were considered versus overall cost. As such, it has controlled rise and fall time of 0.50 ± 0.15 microseconds.

Circuit operation of each of the three circuits is as follows: With a logical "0" input (-½v), Q01 is turned on and the base of Q02 is almost two volts negative thereby turning off Q02. When the input goes to a "1" (-3v), Q01 turns off and the current through its emitter resistor (R04) is now routed through diodes CR03, CR04, and CR05 to ground. The collector voltage of Q01 starts to go positive. However, as soon as Q02 starts to conduct current to the external load (typically equivalent to 60 ohms to ground), the voltage drop across R06 in the collector circuit of Q02 is coupled back to its base via C01 causing it to act as a Miller integrator in which the output current rises quite linearly over about 0.5 microsecond. The time constant is basically determined by C01 and R03. The end of the current rise ramp is reached as Q02 nears saturation, and output current equals about 34 ma (2 volts across a 60-ohm external load to ground).

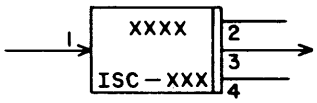
When the input returns to a logical "0", the Miller integrator circuit causes the output current to reduce quite linearly to zero. In this case, the time constant is basically determined by C01 and the divider composed of R03 and R04 which connects between +20v and -20v. Saturation-limiting diodes CR01 and CR02 reduce turnoff time of Q01 and Q02, respectively. Base current in Q01 is limited by the drop across R02. With a logical "0" input, R01 and R02 load the previous logic

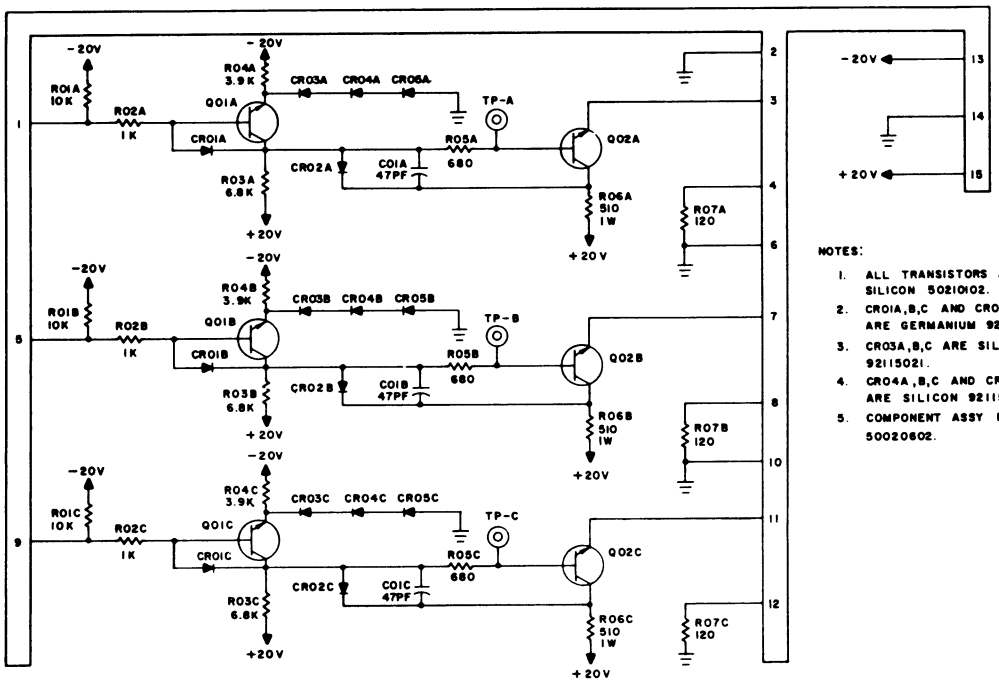
stage about 3 ma. With a logical "1" input, loading of the previous stage is limited to R01 and does not exceed 2 ma.

Line-terminating resistors are available as a jumper option for each circuit. A pin is also available for each circuit as a convenience for grounding one side of a twisted pair of the outer conductor of a coax line.

The following cautions should be observed in application and use. Capacitive loading of test probes on the test point affects the output waveform and should be minimized by using low capacitance probes or eliminated by monitoring the output pin with a card extender in critical timing situations. The current supplied to the load through the internal collector supply resistor (R06) increases power from 0.2w per circuit to nearly 0.8w per circuit when the input switches from a logical "0" to a logical "1". While the silicon transistors used in the circuit are designed to operate at above normal logic card temperature, it is generally advisable to avoid logic card assignments which cause all three circuits of the ISC card to remain continuously in a "1" state.

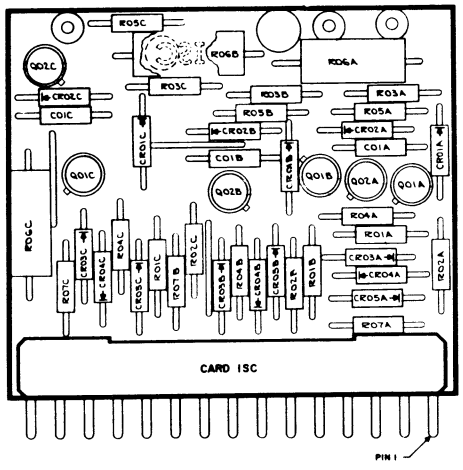
SYMBOL





NOTES:

1. ALL TRANSISTORS ARE SILICON 50210102.
2. CR01A,B,C AND CR02A,B,C ARE GERMANIUM 92116002.
3. CR03A,B,C ARE SILICON 92115021.
4. CR04A,B,C AND CR05A,B,C ARE SILICON 92115019.
5. COMPONENT ASSY NO. 50020602.



PULSE DELAY AND OUTPUT AMPLIFIER
ITA/ITB/ITC

The ITA, ITB, and ITC circuits are functionally interchangeable with the improved ITD circuit. Existing ITA and ITB circuits are retrofittable to ITC and ITD circuits respectively to eliminate tendency toward runt output pulses (by increasing the value of R02) and from delay failure at low temperatures (by changing CR03 from germanium to silicon). The ITA and ITC incorporate a different output circuit associated with Q06 and Q07 than used in the ITB and ITD. While the ITA and ITC test points are less susceptible to capacitive loading of test prods than the ITB and ITD, a greater production yield problem is experienced with uniformity in generating the rising ramp on the ITA and ITC output circuit. The ITB and ITD circuit improve uniformity of the output pulse shape by using a lower storage transistor for Q06 and by adding a resistor in the base of Q07.

The delay portion of the circuit is covered in the UGA description. Additional output circuit and application information are included in the following ITD circuit.

PULSE DELAY AND OUTPUT AMPLIFIER
ITD

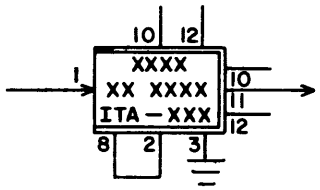
The ITD pulse delay and output amplifier circuit is used for read deskew adjustment in magnetic tape units which interface to a controller with 1 usec digital pulse signals ahead of an accumulation register used to group the bits of each frame of data. Except for the value of R and the line transmitter output, the circuit is the same as the UGA voltage controlled pulse delay. The output circuit is designed to provide an output signal similar to the IS.. series output amplifiers. The output signal is designed to be transmitted on a twisted pair 120-ohm line for receipt by an OS.. series input amplifier. Up to eight ITD outputs may be paralleled for time sharing of a common signal line. Except for the small capacitance of the output emitters, parallel transmitters cause no perceptible loading of the signal on the line. This applies whether parallel circuits have power on or off.

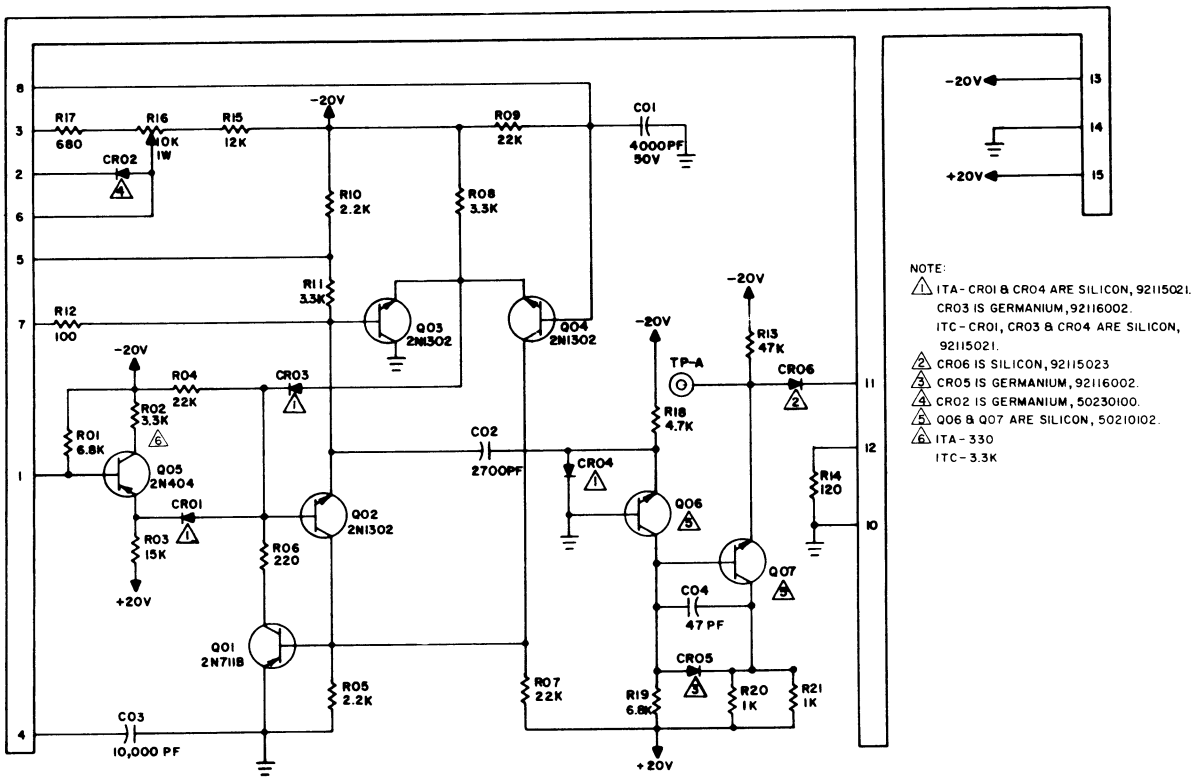
For a description of the delay portion of the circuit, refer to the

description of the UGA circuit. This applies to Q01 through Q05 and their associated components for which reference symbol designations are identical. Thus wiring for pins 1 through 8 does not change between the ITA and UGA when used on the same delay ranges.

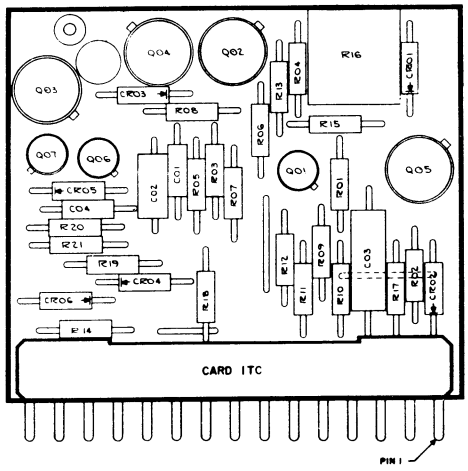
The output circuit consists of Q06 and Q07. The width of the output pulse at the end of the delay period is a function of the time constant of C02 and R18 over a voltage excursion determined by the sum of the forward voltage drops of CR04 and V_{EB} of Q06. This shuts Q06 off for about 1 usec at the end of the delay period. Q07 acts as an output driver with controlled rise (0.5 $\pm$ .15 usec) and fall (0.5 $\pm$ .15 usec) times. It is designed to drive a +2.0v min signal into a 60-ohm load terminated to ground. This is equivalent to a line with 120-ohm characteristic impedance terminated at each end with a 120-ohm load. Rise and fall time of the output drive current are determined by a Miller integrating circuit composed of C04, R19, and R18. The output circuit is compatible with the ISC card, and capacitive loading of test probes on the test point affects the output waveform. This loading should be minimized by using low capacitance probes or eliminated by monitoring the output pin with a card extender in critical timing situations. R14 may be connected as an option to the output when an ITD is used at one end of a line and it is undesirable to use a separate 120-ohm terminating resistor external to the card. The 120-ohm terminating impedance to ground provides the off voltage of Ov. Output pulse width over the recommended delay ranges is 1.0 $\pm$ .3 usec at 16 2/3 ma (60 ohm @ 1v).

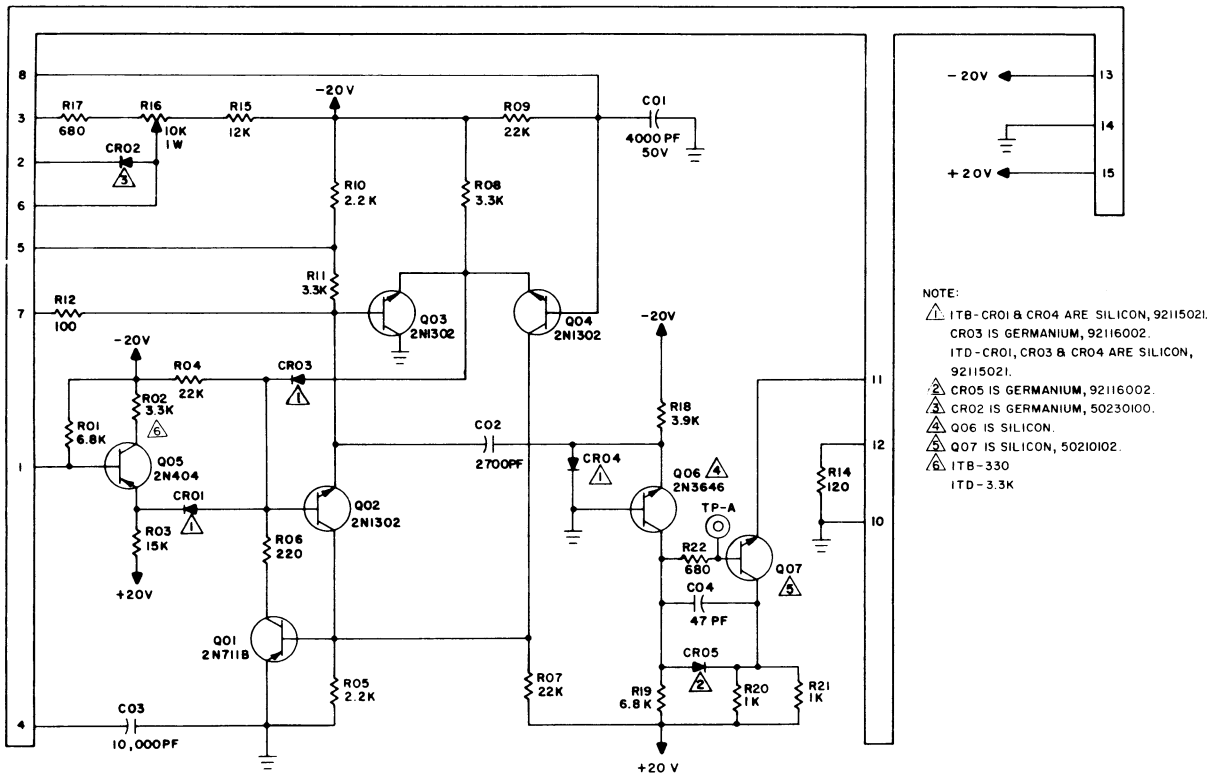
SYMBOL



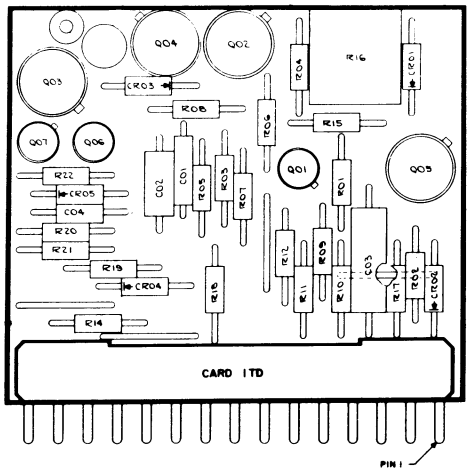

-20V
13
14
+20V
15
R17 680
R16 10K 1W
R15 12K
CR02
R09 22K
C01 4000PF 50V
R10 2.2K
R08 3.3K
R11 3.3K
R12 100
Q03 2N1302
Q04 2N1302
R13 47K
CR06
TP-A
R18 4.7K
R04 22K
CR03
R02 3.3K
R01 6.8K
Q05 2N404
C02 2700PF
CR04
R14 120
CR01
Q02 2N1302
Q06
R03 15K
R06 220
+20V
Q07
C04 47 PF
Q01 2N7118
CR05
R05 2.2K
R07 22K
R19 6.8K
R20 1K
R21 1K
C03 10,000 PF
+20V
NOTE:
1 ITA - CR01 & CR04 ARE SILICON, 92115021.
CR03 IS GERMANIUM, 92116002.
ITC - CR01, CR03 & CR04 ARE SILICON, 92115021.
2 CR06 IS SILICON, 92115023
3 CR05 IS GERMANIUM, 92116002.
4 CR02 IS GERMANIUM, 50230100.
5 Q06 & Q07 ARE SILICON, 50210102.
6 ITA - 330
ITC - 3.3K

ITA, ITC


Q04
Q02
R16
C801
Q03
CR03
R13
R04
R08
R15
R06
Q07
Q06
Q01
Q05
CR05
C04
C02
C01
R05
R03
R07
R20
R21
R01
R19
CR04
R12
R09
C03
R11
R10
R17
R02
CR02
CR06
R14
CARD ITC
PIN 1


-20V
+20V
+20 V
R17 680
R16 10K 1W
R15 12K
R09 22K
C01 4000 PF 50V
CR02
R10 2.2 K
R08 3.3K
R11 3.3K
R12 100
Q03 2N1302
Q04 2N1302
R04 22K
CR03
R02 3.3K
R01 6.8K
Q05 2N404
CR01
R03 15K
R06 220
Q02 2N1302
C02 2700PF
CR04
R18 3.9K
Q06 2N3646
TP-A
R22 680
Q07
C04 47 PF
R14 120
Q01 2N711B
R05 2.2K
R07 22K
CR05
R19 6.8 K
R20 1K
R21 1K
C03 10,000PF
- 20V
+ 20V
NOTE:
1. ITB-CR01 & CR04 ARE SILICON, 92115021. CR03 IS GERMANIUM, 92116002. ITD-CR01, CR03 & CR04 ARE SILICON, 92115021.
2. CR05 IS GERMANIUM, 92116002.
3. CR02 IS GERMANIUM, 50230100.
4. Q06 IS SILICON.
5. Q07 IS SILICON, 50210102.
6. ITB-330 ITD-3.3K

ITB, ITD


CARD ITD
PIN 1

OUTPUT AMPLIFIER
IYA

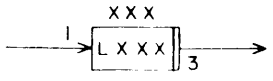
The output amplifier card, IYA, is used to interface between standard logic signals (0v to -3v) and equipment operating from excursions of -12v to -1v. Only one receiver circuit is to be connected to the output amplifier circuit.

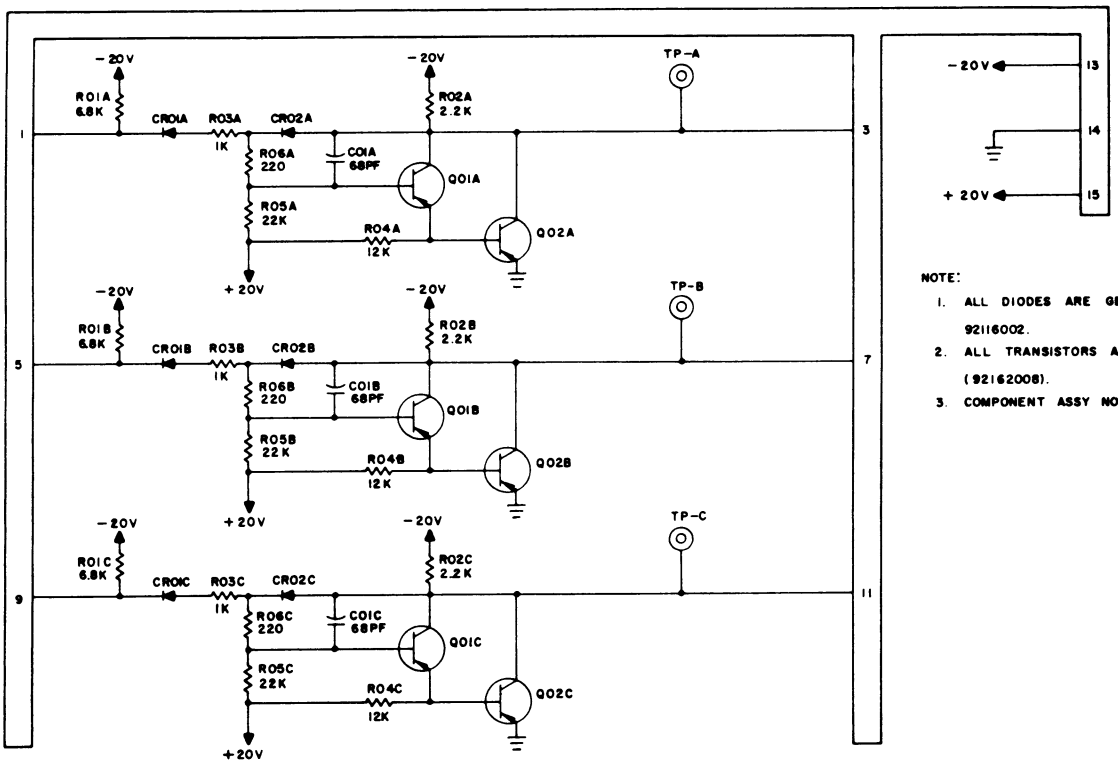
Each IYA card has three identical circuits. The circuit converts a logical "1" (-3v) input to a -0.5v output, and a logical "0" (-0.5v) input to a -14v output when connected to a Beckman receiver and external load resistor.

The IYA circuit is basically a 60 series output amplifier with a different feedback capacitor to modify the output voltage rise and fall times. With a -3v input, forward emitter to base bias for Q02 is provided by voltage divider R01, R03, R06 and R05, and emitter follower Q01. Q02 turns on with a rise time that is controlled by a Miller integrating circuit composed of C01 and the voltage divider. Diode CR02 is used as feedback to the base to prevent Q01 from going into saturation thus minimizing storage time problems. With a "0" input (-0.5v), the divider and Q01 provide a back bias on Q02 emitter-base and Q02 turns off with a fall time controlled by the integrating circuit.

This application called for 60 feet max. twisted-pair output lines to be terminated in a Beckman receiver circuit. An external load resistor of 680 ohms to -20v was added to the circuit to provide the necessary line charging current when Q02 switches off to bring the fall time into the required range. With this arrangement, the IYA switches between the levels of -14v and -0.5v with a rise time of 1.2 usec $\pm$0.6 usec and a fall time (switching from -1v to -10v) of 1.2 usec $\pm$0.6 usec. When turned on, the circuit is required to deliver 10 ma to the receiver.

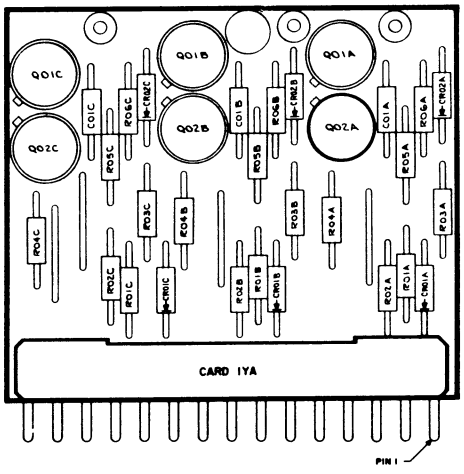
SYMBOL





NOTE:

1. ALL DIODES ARE GERMANIUM 92116002.
2. ALL TRANSISTORS ARE 2N404 (92162008).
3. COMPONENT ASSY NO. 50022400.



POSITIVE VOLTAGE REFERENCE SWITCH
JBA

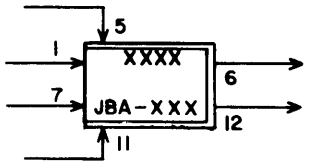
The JBA card is used in the disk file servo actuator coarse control loop. There are two identical circuits per card. Seven circuits are needed to position to each of seven tracks, and an eighth circuit is needed for positioning $\pm$0.020 inches either side of each track. A total of four JBA cards are used per servo.

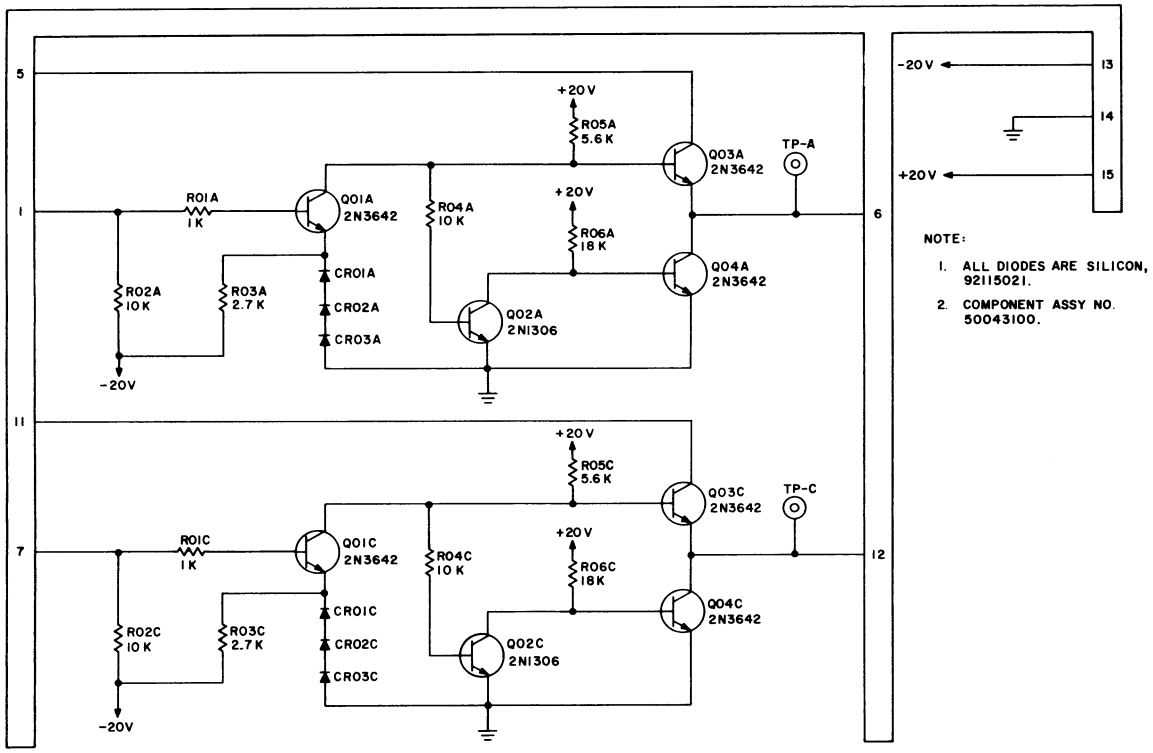
By means of logic signals in, the circuit performs the function of applying a positive 8v reference to an output line, or shorting that line to ground. The 8v is applied to pins 5 and 11, with the output taken from pins 6 and 12.

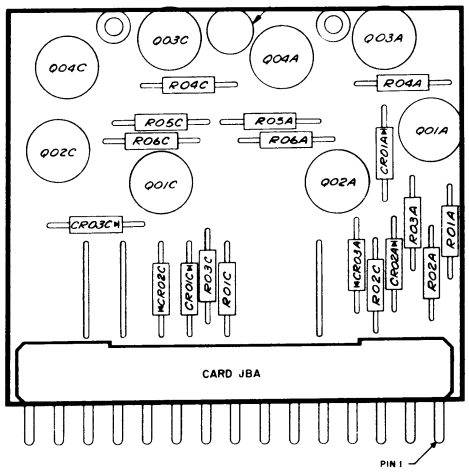
With a logical "1" input at pin 1 (or pin 7), transistor Q01A turns off. Transistor Q02A turns on, causing Q04A to turn off. At the same time, transistor Q03A turns on.

A logical "0" input at pin 1 (or pin 7) will turn Q01A on, holding both Q02A and Q03A off. Since Q02A is off, Q04A will be turned on, shorting the output line to within approximately 15mv of ground. The load current has a maximum value of approximately 1.1 ma.

SYMBOL




5
1
11
7
+20V
R05A
5.6 K
Q03A
2N3642
TP-A
R01A
1K
Q01A
2N3642
R04A
10 K
+20V
R06A
18 K
Q04A
2N3642
6
R02A
10 K
R03A
2.7 K
CR01A
CR02A
CR03A
Q02A
2N1306
-20V
+20V
R05C
5.6 K
Q03C
2N3642
TP-C
R01C
1K
Q01C
2N3642
R04C
10 K
+20V
R06C
18K
Q04C
2N3642
12
R02C
10 K
R03C
2.7 K
CR01C
CR02C
CR03C
Q02C
2N1306
-20V
-20V
13
14
+20V
15
NOTE:
1. ALL DIODES ARE SILICON, 92115021.
2. COMPONENT ASSY NO. 50043100.


Q03C
Q04A
Q03A
Q04C
R04C
R04A
R05C
R06C
R05A
R06A
Q01A
Q02C
Q01C
Q02A
CR01A
CR03C
R03A
R01A
R02A
R02C
R03C
R01C
CARD JBA
PIN 1

NEGATIVE VOLTAGE REFERENCE SWITCH
JCA

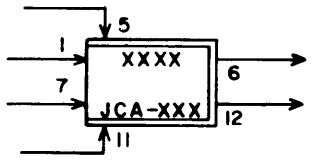
This card is used in the coarse control loop of the disk file servo actuator. There are two identical circuits on each card. Seven circuits are needed to position to each of seven tracks, and an eighth circuit is used for positioning ±0.020 inches either side of each track. A total of four JCA cards are used per servo.

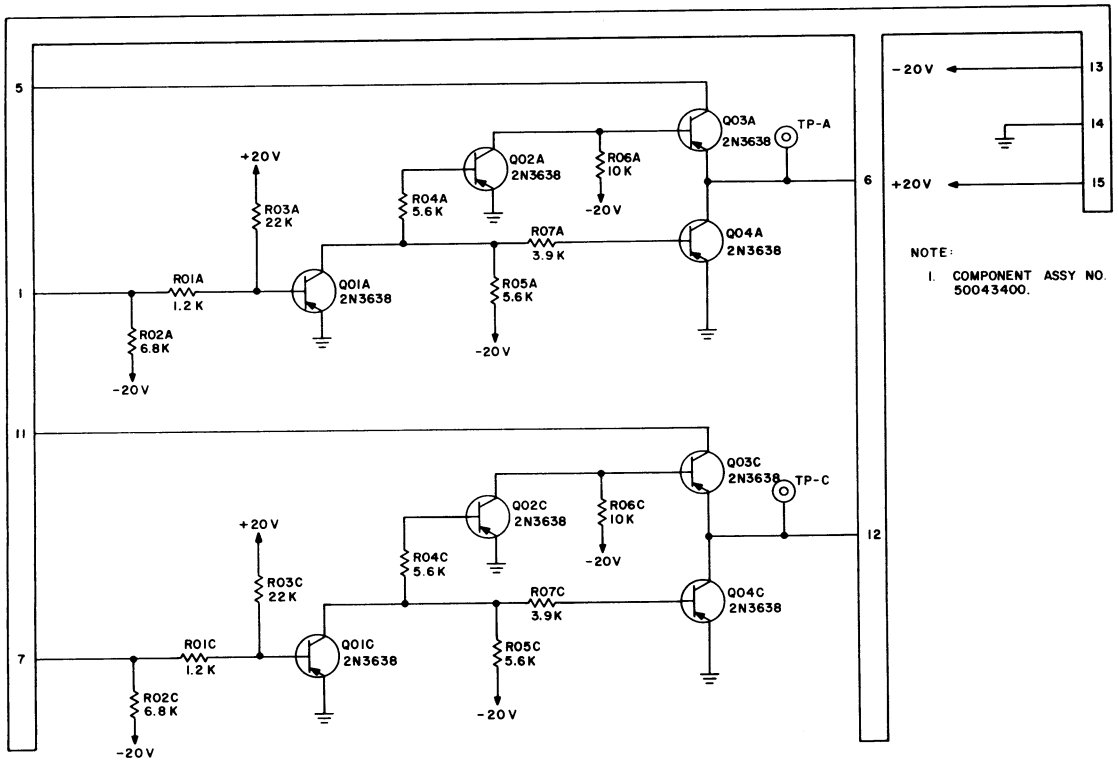
By means of logic signals in at pins 1 and 7, the circuit performs the function of applying a negative 8v reference to an output line, or shorting that line to ground. The -8v is applied to pins 5 and 11, with the output taken from pins 6 and 12.

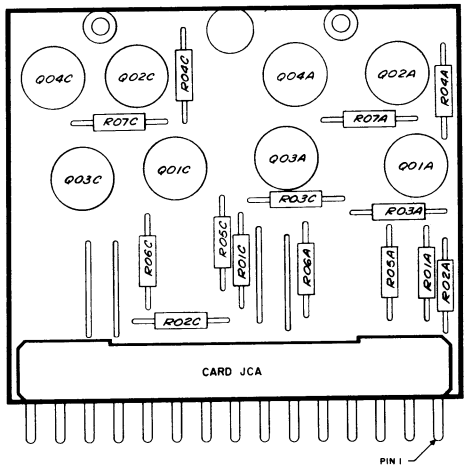
When the input at pin 1 (or pin 7) is at logical "0", Q01A is off, allowing both Q02A and Q04A to be on. Since Q02A is on, Q03A must be off. Therefore, the output line is shorted to within approximately 15mv of ground. With a logical "1" input, Q01A goes on, turning Q02A and Q04A off. This allows Q03A to turn on, thereby connecting the reference voltage to the output line.

The load current supplied by this card is approximately 1.1 ma maximum.

SYMBOL




5
1
11
7
6
12
13
14
15
-20V
+20V
TP-A
TP-C
Q01A 2N3638
Q02A 2N3638
Q03A 2N3638
Q04A 2N3638
Q01C 2N3638
Q02C 2N3638
Q03C 2N3638
Q04C 2N3638
R01A 1.2 K
R02A 6.8K
R03A 22K
R04A 5.6K
R05A 5.6K
R06A 10K
R07A 3.9 K
R01C 1.2 K
R02C 6.8 K
R03C 22K
R04C 5.6K
R05C 5.6K
R06C 10K
R07C 3.9K
NOTE:
1. COMPONENT ASSY NO. 50043400.


Q04C
Q02C
R04C
Q04A
Q02A
R04A
R07C
R07A
Q03C
Q01C
Q03A
Q01A
R03C
R03A
R05C
R01C
R06A
R05A
R01A
R02A
R06C
R02C
CARD JCA
PIN 1

LONG STROKE AND SHORT STROKE SWITCH
JDA

The JDA card is used in the disk file servo actuator. The circuit performs the function of removing the short stroke (fine control) signal from the short stroke valve amplifier when the system is in the long stroke (coarse control) mode. It is also used for removing the long stroke signal from the long stroke valve amplifier when the system is in the short stroke mode.

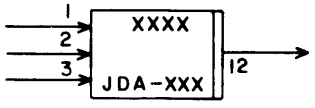
The circuit has three input lines and one output line tied to the collectors of a NPN and PNP transistor. This is done so either polarity of the input signal can be shorted to ground.

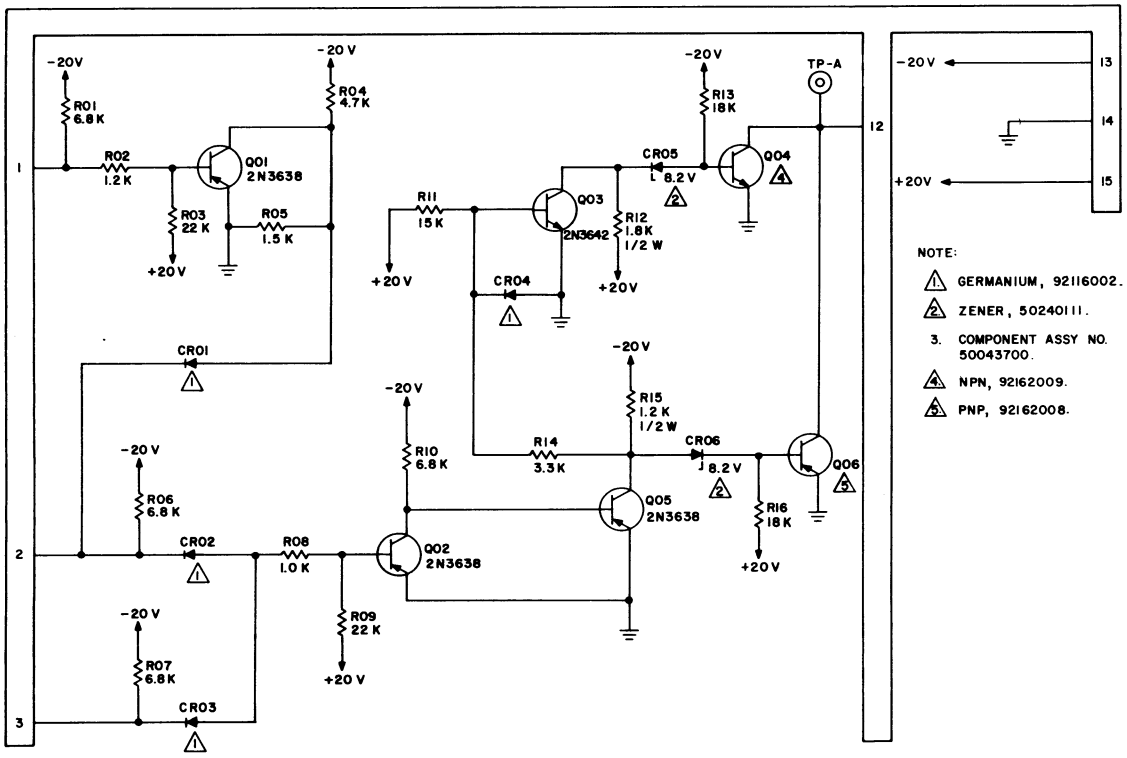
The normal input signals on pins 1, 2, and 3 are -0.5v and -3v (logical "0" and "1" respectively). The output on pin 12 is open or grounded and is defined as logical "0" and "1" respectively. The logic performed by the circuit satisfies the equation: $V_{12} = \overline{V}_1 \cdot V_2 + V_3$, where the subscripts refer to the input and output pins. Thus if pin 3 is a logical "1", the output is also a logical "1" (i.e. grounded). Pin 3 at -3v, regardless of the voltage on pin 2, causes Q02 to turn on. This turns off Q05, allowing Q06 to turn on. Also, Q03 turns off and Q04 turns on. The positive and negative voltages on pin 12 are now grounded (output at logical "1").

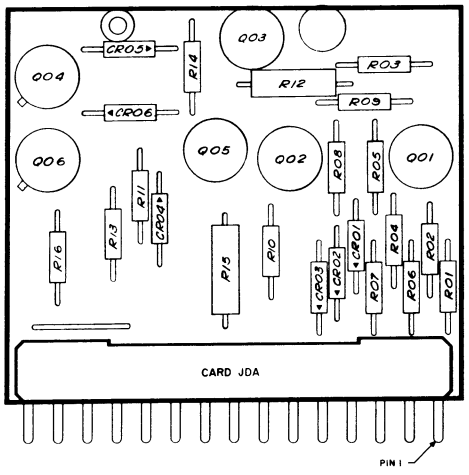
The circuit involving Q01 is an inverter, which is diode coupled to input pin 2. This can be recognized as an AND circuit, since both the collector of Q01 and the voltage at pin 2 must be -3v (logical "1"), before transistor Q02 can turn on. This requires pin 1 to be at "0". The first term of the logic equation is then realized.

This circuit can pass approximately ± 3 ma peak when in the logical "1" state.

SYMBOL




-20V
R01 6.8K
R02 1.2K
R03 22K
+20V
Q01 2N3638
R04 4.7K
R05 1.5K
CR01
CR02
CR03
R06 6.8K
R07 6.8K
R08 1.0K
R09 22K
Q02 2N3638
R10 6.8K
R11 15K
Q03 2N3642
R12 1.8K 1/2W
CR04
R13 18K
CR05 8.2V
Q04
TP-A
R14 3.3K
R15 1.2K 1/2W
CR06 8.2V
Q05 2N3638
Q06
R16 18K
1
2
3
12
13
14
15
NOTE:
1. GERMANIUM, 92116002.
2. ZENER, 50240111.
3. COMPONENT ASSY NO. 50043700.
4. NPN, 92162009.
5. PNP, 92162008.


CR03
R14
Q03
R03
R12
R09
CR06
Q04
Q06
Q05
Q02
Q01
R08
R05
R11
CR04
CR01
R04
R02
R16
R13
R15
R10
CR02
R07
R06
R01
CARD JDA
PIN 1

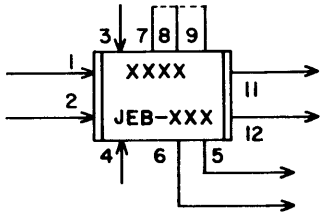
TUNED AMPLIFIER
JEB, JEC

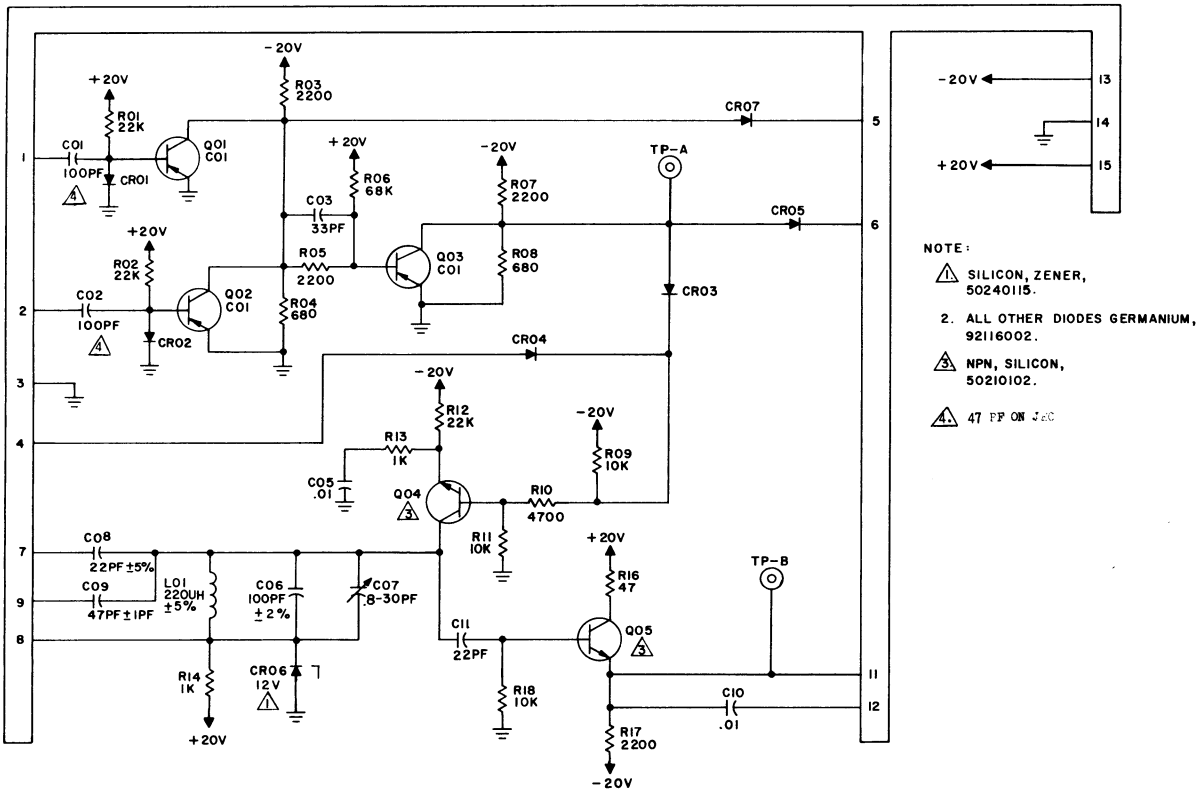
This card is intended for use in the read/write chain in the disk file. Its function is to provide a sine wave output at a basic frequency, which is insensitive to slight variations of input frequency, caused by the effects of peak shifting in the data.

The inputs applied at pins 1 and 2 are complimentary negative square waves derived from the recorded information. These are differentiated by C01, Q01 and C02, Q02. The outputs of Q01 and Q02 are summed across R04 and applied to the base of Q03. The voltage across R04 is therefore a series of positive pulses occurring for each negative going transition on pins 1 and 2.

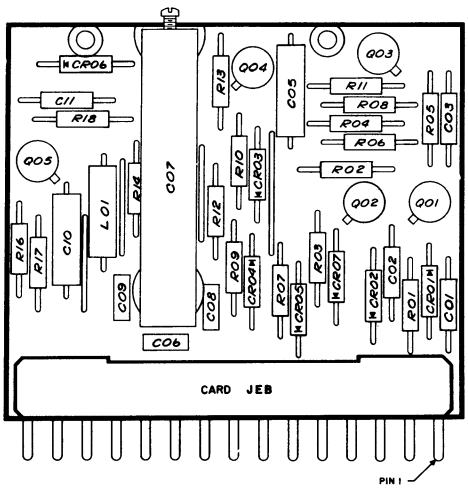
Amplifier Q03 passes the negative going pulses through the "AND" circuit CR03, CR04, and R09 (assuming pin 4 is negative providing the enable) and then to the under damped tuned collector amplifier Q04. This stage is normally on and is turned off by the incoming negative pulses. This allows the stored energy in the tank inductor to oscillate between L01, C06, C07 and possibly C08 and/or C09 if they are externally connected. The sine wave of voltage across the tank is coupled to the output by the emitter follower Q05.

SYMBOL




-20V
+20V
R03 2200
R01 22K
CR07
C01 100PF
Q01 C01
CR01
+20V
R06 68K
-20V
R07 2200
TP-A
C03 33PF
CR05
+20V
R02 22K
R05 2200
Q03 C01
R08 680
C02 100PF
Q02 C01
R04 680
CR03
CR02
CR04
-20V
R12 22K
-20V
R13 1K
R09 10K
C05 .01
Q04
R10 4700
C08 22PF ±5%
R11 10K
+20V
R16 47
TP-B
C09 47PF ±1PF
L01 220UH ±5%
C06 100PF ±2%
C07 8-30PF
C11 22PF
Q05
R14 1K
CR06 12V
R18 10K
C10 .01
R17 2200
-20V
+20V
-20V
13
14
15
NOTE:
1. SILICON, ZENER, 50240115.
2. ALL OTHER DIODES GERMANIUM, 92116002.
3. NPN, SILICON, 50210102.
4. 47 PF ON J&C

JEB


CR06
C11
R18
Q05
R14
L01
C10
C09
C08
C07
C06
R16
R17
R13
Q04
C05
Q03
R11
R08
R04
R06
R02
R05
C03
R10
CR03
R12
R09
CR04
R07
CR05
R03
CR07
C02
R01
CR01
C01
Q02
Q01
CARD JEB
PIN 1

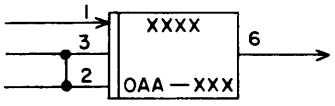
PHOTOCELL AMPLIFIER
OAA

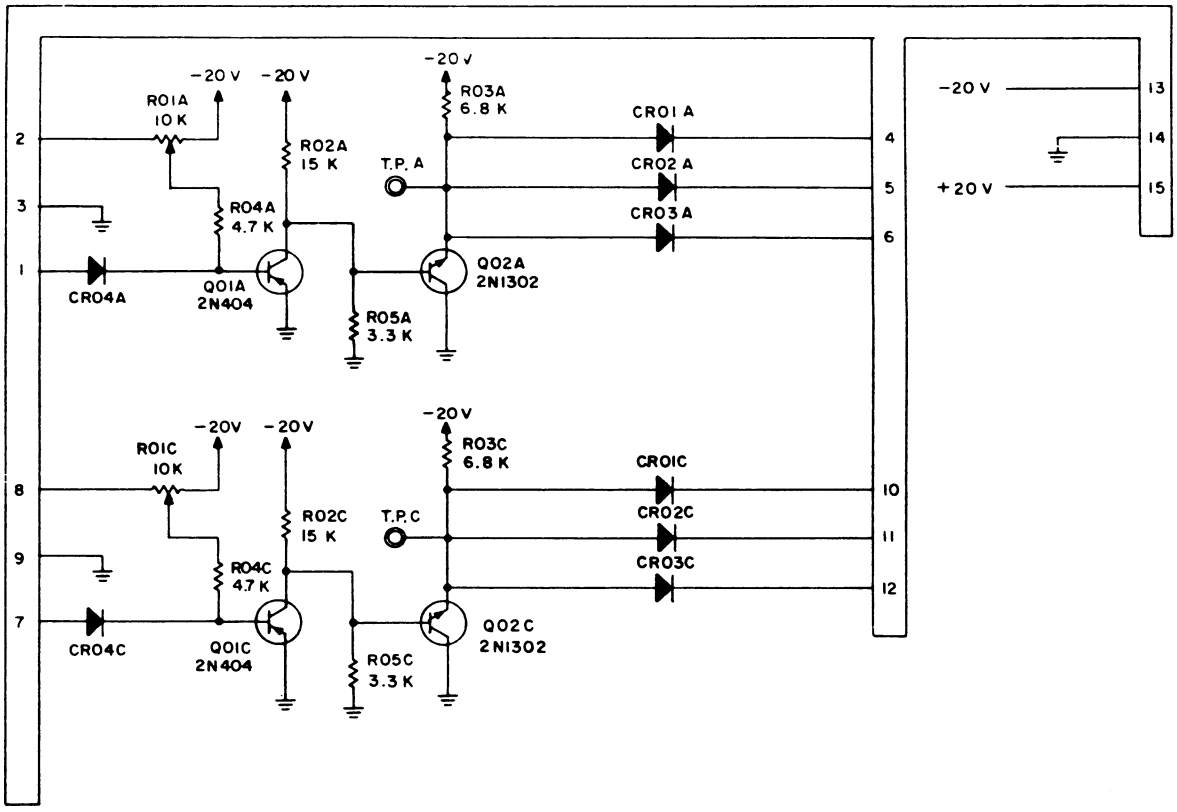
The photocell amplifier receives inputs from silicon solar cells. The output from the amplifier is a "1" when the solar cell is illuminated and a "0" when unlighted. An adjustable potentiometer is provided because of low level signals normally available from the solar cells. This allows optimum centering of the switching point of the amplifier to compensate for the overall photocell excitation, sensitivity, and amplifier tolerances.

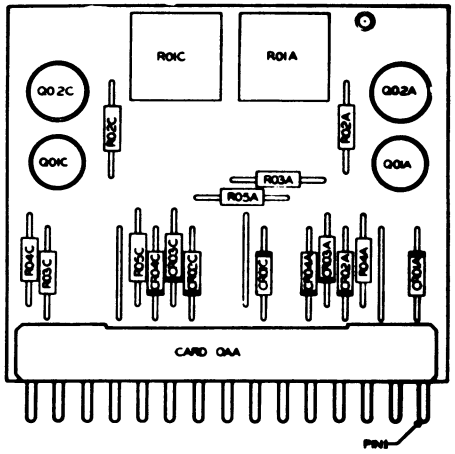
The first stage of the amplifier consists of an inverting amplifier Q01. This transistor is turned on by drive current flowing through R04 from potentiometer R01. Normally pin 2 is jumpered externally to pin 3 to provide R01 with the maximum range of adjustment. The positive terminal of the photocell counteracts the turnon current of R04. Sufficient output from the photocell turns off Q01. CR04 compensates for the change in base to emitter potential of Q01 with changing temperature.

The output of Q01 is directly coupled to Q02 which acts as an emitter follower. The logical "1" excursion at the output is determined primarily by the divider composed of R02 and R05 since the gain of Q02 is sufficient to provide only minor loading of this resistance regardless of the number of outputs actually used. Three diodes (CR01, 02, 03) are provided for ANDing with other logical circuits.

SYMBOL




-20 V
-20 V
-20 V
R01A
10 K
R02A
15 K
R03A
6.8 K
CR01 A
CR02 A
CR03 A
T.P. A
R04A
4.7 K
Q02A
2N1302
CR04A
Q01A
2N404
R05A
3.3 K
-20V
-20V
-20 V
R01C
10K
R02C
15 K
R03C
6.8 K
CR01C
CR02C
CR03C
T.P.C
R04C
4.7 K
Q02C
2N1302
CR04C
Q01C
2N404
R05C
3.3 K
-20 V
+20 V
2
3
1
8
9
7
4
5
6
10
11
12
13
14
15

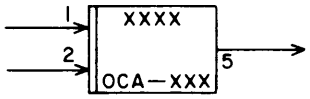

R01C
R01A
Q02C
Q02A
Q01C
Q01A
R02C
R02A
R03A
R05A
R04C
R03C
R05C
R04A
R03A
R05A
R02A
Q02A
R01A
Q01A
CARD OAA
PINS

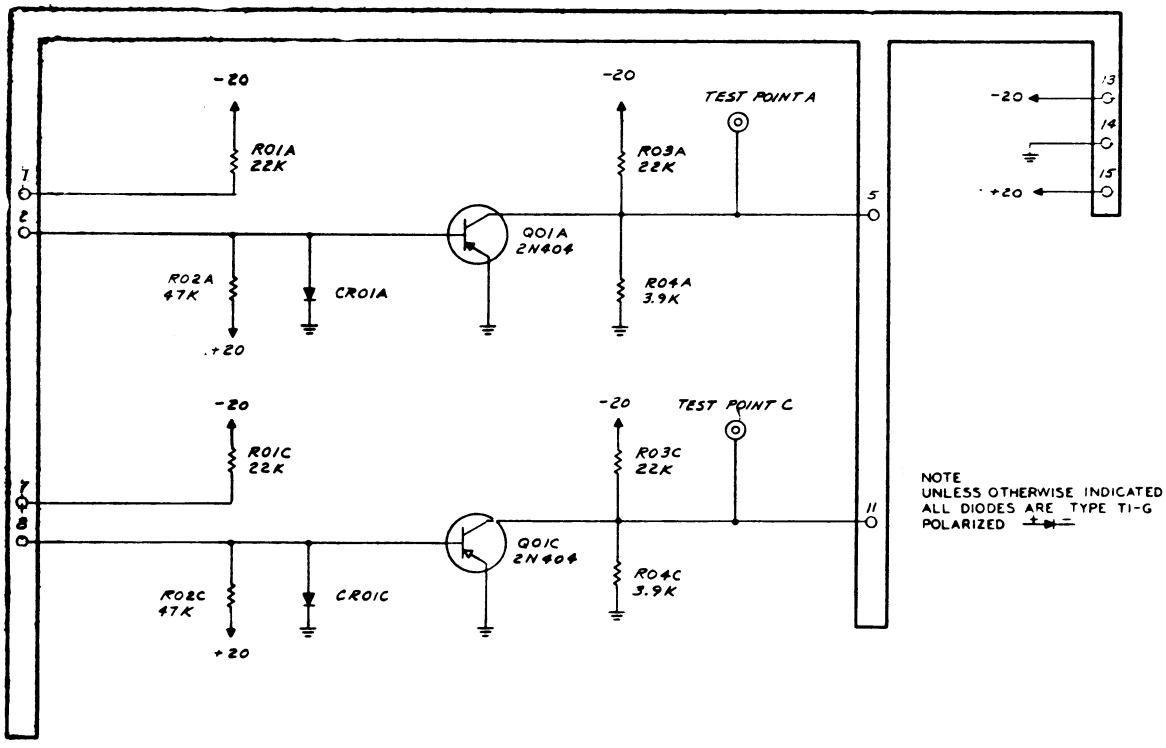
DUAL PHOTOCELL AMPLIFIER

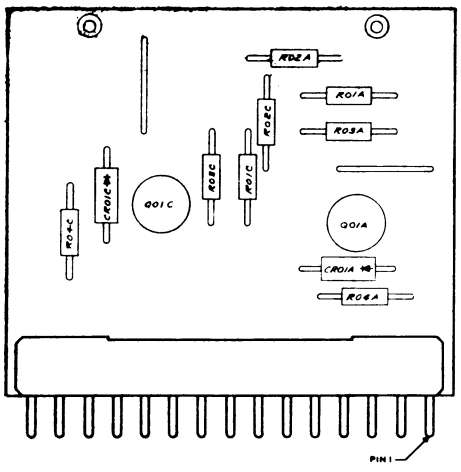
OCA

This photocell amplifier card was designed to work with the photo electric timer circuit of the 180 Data Collector. The input photocell is connected between pins 1 and 2 (or 7 and 8). When its resistance becomes low, Q01 turns on and its output becomes a logic "0" (-1/2v). When the photocell resistance becomes greater than 25K, Q01 turns off and its output becomes a logic "1" (-3v).

SYMBOL




-20
R01A
22K
-20
TEST POINT A
R03A
22K
1
2
Q01A
2N404
5
R02A
47K
CR01A
R04A
3.9K
+20
-20
R01C
22K
-20
TEST POINT C
R03C
22K
7
8
Q01C
2N404
11
R02C
47K
CR01C
R04C
3.9K
+20
-20
13
14
15
+20
NOTE
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED


R02A
R01A
R03A
R02C
CR01C
R04C
Q01C
R03C
R01C
Q01A
CR01A
R04A
PIN 1

READ PEAK DETECTOR

ODA

The read peak detector is used with the output of the level detector. The level detector full-wave rectifies a class A signal into positive pulses and passes the portion of the signal which exceeds a predetermined level to the peak detector.

Peak detection is accomplished by first differentiating the rectified class A signal and then detecting the zero crossover point of this differentiated signal.

The first portion of the peak detector circuit consists of the differentiating amplifier (C01, R01, and R02). Because R02 is connected to the output of the high-gain amplifier, the resistance presented to the differentiating capacitor is essentially R02/G where G equals the gain of the amplifier (approximately 1000).

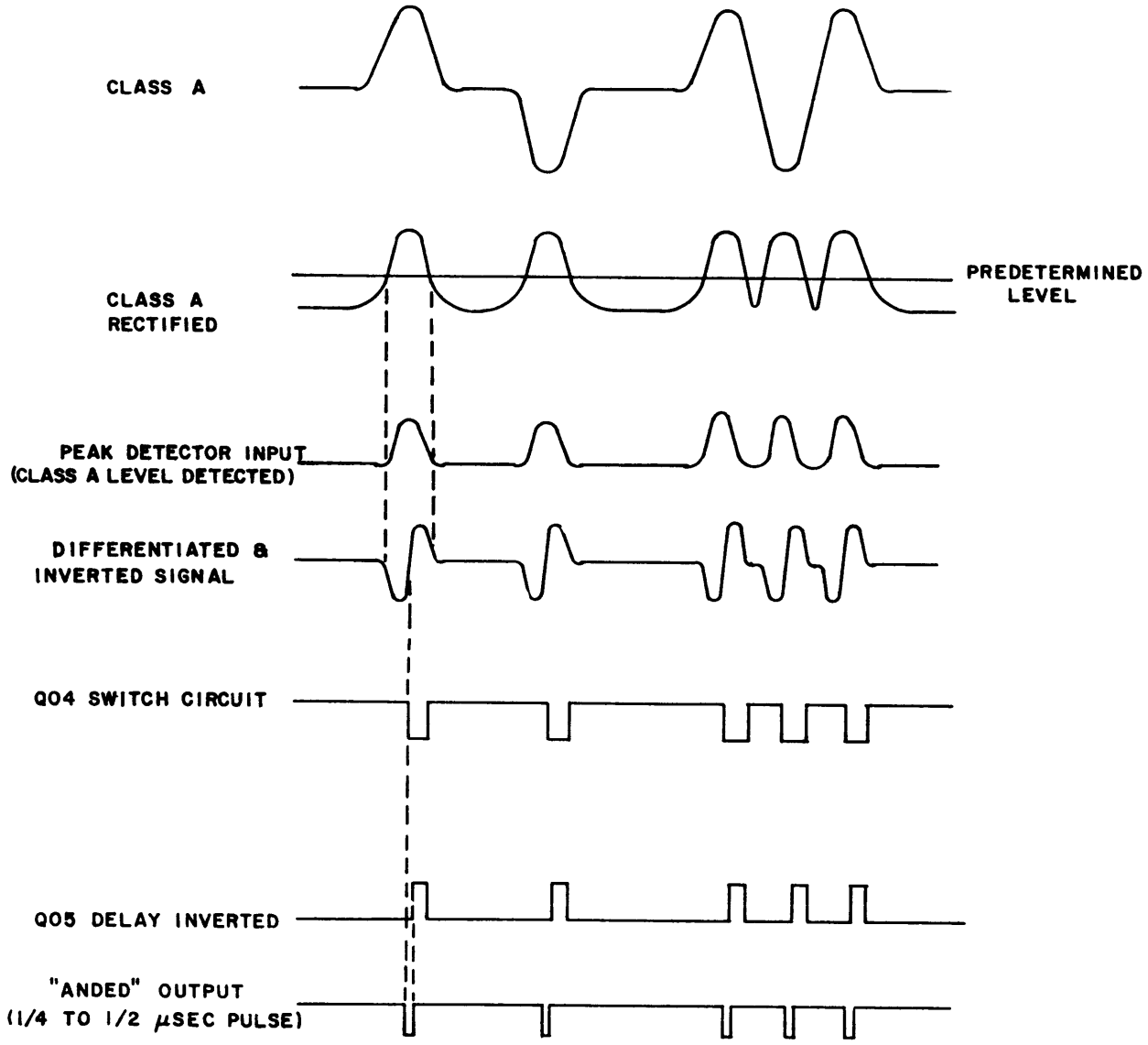
The high-gain amplifier uses three transistors in a single inverting circuit. Q01 is the voltage amplifier; Q02 and Q03 are emitter follower-connected and provide current gain. A positive feedback loop (C04 and R04) returns a signal to the junction of R03 and R04. This signal approaches, but never exceeds, the signal at the collector of Q01. Resistor R03 presents a very high impedance in the collector load of Q01, and increases the a-c voltage gain of Q01 from 100 to 1000. Because the voltage returned to the junction of R03 and R04 is always slightly less than that at the output of Q01, the circuit is free of the usual oscillatory problems associated with positive feedback. The coupling capacitor C04 eliminates d-c positive feedback and thermal drift problems associated with high impedance loads. The d-c (8v) operating point at the output of the amplifier is made stable by the negative feedback divider (R01 and R02).

The differentiated output is coupled by C05 to the zero crossover switching circuit of Q04. R10 normally biases Q04 in the on state. When a signal appears, CR01 prevents Q04 from being overdriven by the differentiated signal which initially swings in the negative direction. When the differentiated signal swings positive and exceeds 0v, CR01 conducts and removes the drive from Q04 causing it to turn off. R09 acts as a load on C05, reducing the effect of nonlinear loading by the switching circuit.

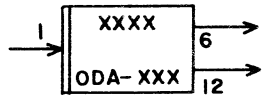
Q05 is used in a simplified version of the normal inverter logic cir-

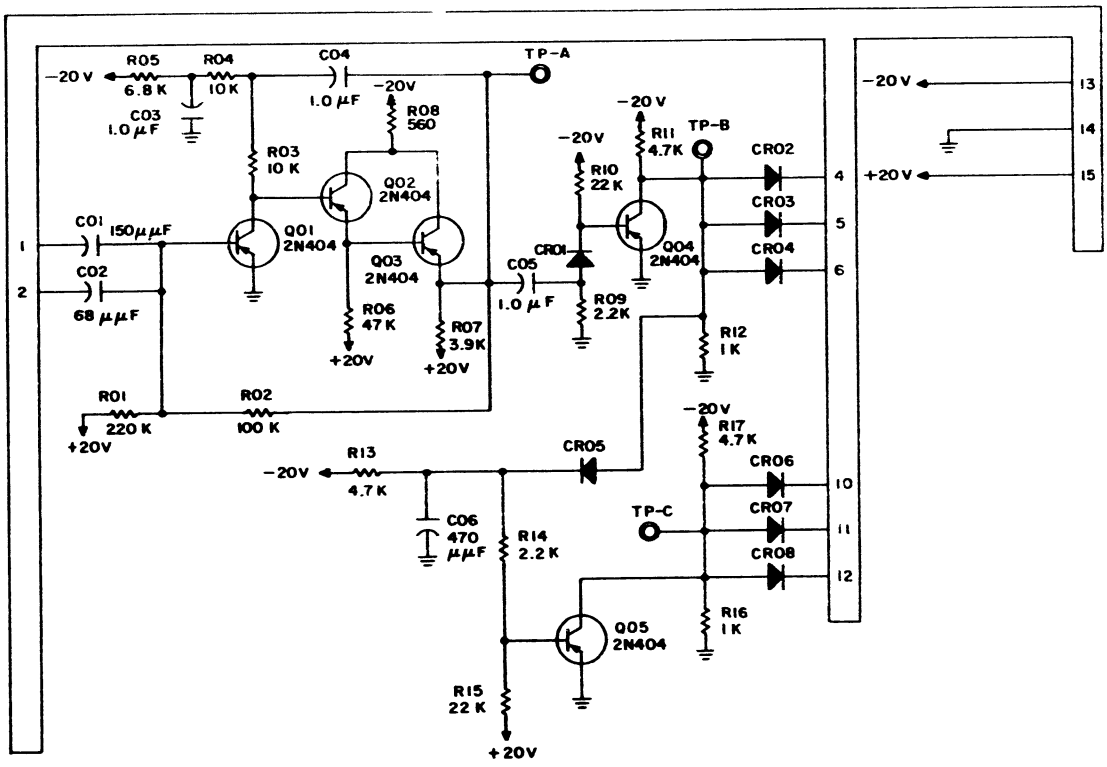
cuit. A delay capacitor, C06, delays the "1" (negative) excursion at the input, and the "0" (positive) excursion at the output.

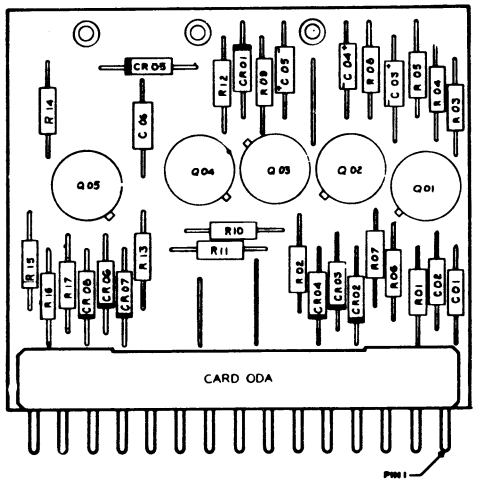
A narrow negative output pulse (1/4 to 1/2 usec) is produced when the output diodes of Q04 and Q05 are ANDed. The "1" (negative) output pulse corresponds to a point just following the positive peak on the input, or the zero crossover point in the positive direction of the differentiator output.



SYMBOL


1
XXXX
6
ODA-XXX
12


-20 V
R05
6.8 K
R04
10 K
C04
1.0 μF
TP-A
C03
1.0 μF
-20V
R08
560
-20 V
-20V
R11
4.7K
TP-B
R10
22 K
CR02
R03
10 K
Q02
2N404
CR03
C01
150μμF
Q01
2N404
Q04
2N404
CR04
CR01
C02
68 μμF
Q03
2N404
C05
1.0 μF
R09
2.2K
R06
47 K
R07
3.9K
+20V
+20V
R12
1K
R01
220 K
R02
100 K
+20V
-20V
R17
4.7K
R13
-20V
4.7 K
CR05
CR06
CR07
TP-C
C06
470
μμF
R14
2.2 K
CR08
R16
1K
Q05
2N404
R15
22 K
+20V
-20 V
+20 V
13
14
15
1
2
4
5
6
10
11
12


CR 05
R 14
C 06
Q 05
Q 04
Q 03
Q 02
Q 01
R 12
CR 01
R 09
C 05
C 04
R 06
C 03
R 05
R 04
R 03
R 10
R 11
R 15
R 16
R 17
CR 06
CR 07
R 13
R 02
C 04
CR 03
CR 02
R 07
R 06
R 01
C 02
C 01
CARD ODA
PIN 1

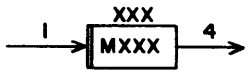
INPUT AMPLIFIER
OFA

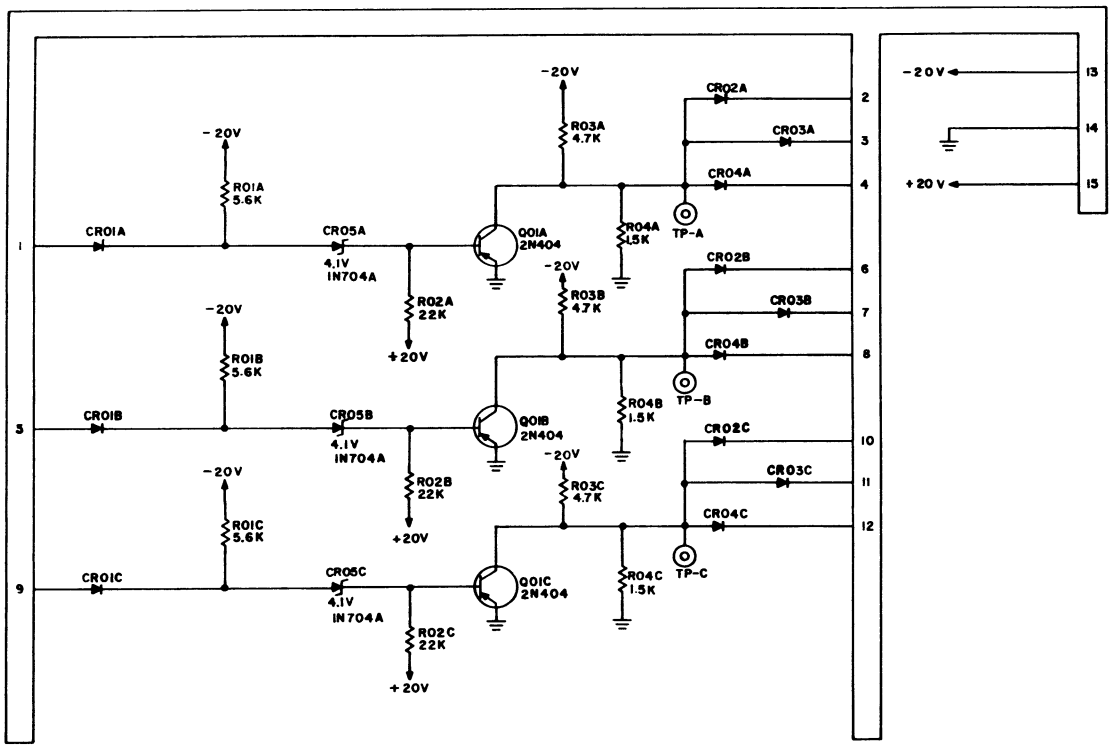
This input amplifier is used to operate from a common line in parallel with other like input amplifiers in other units, part or all of which may have internal power on or off.

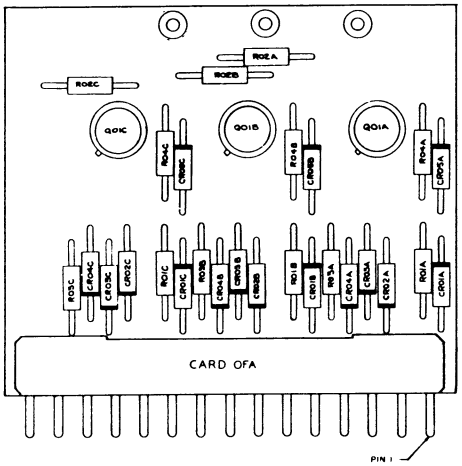
The circuit is a switching type inverter with certain small variations. Diode CR01 minimizes loading of the line in a positive direction when power is removed from this unit. Zener diode CR05 increases the efficiency of the base divider providing the proper switching point (about 4.4 volts negative) for the 0 to -8v input line.

Three standard logic output signals with their isolating diodes are available for each of the three circuits.

SYMBOL




-20V
R01A 5.6K
CR01A
CR05A
4.1V IN704A
R02A 22K
+20V
Q01A 2N404
R03A 4.7K
R04A 1.5K
CR02A
CR03A
CR04A
TP-A
R01B 5.6K
CR01B
CR05B
4.1V IN704A
R02B 22K
+20V
Q01B 2N404
R03B 4.7K
R04B 1.5K
CR02B
CR03B
CR04B
TP-B
R01C 5.6K
CR01C
CR05C
4.1V IN704A
R02C 22K
+20V
Q01C 2N404
R03C 4.7K
R04C 1.5K
CR02C
CR03C
CR04C
TP-C
1
5
9
2
3
4
6
7
8
10
11
12
13
14
15
-20V
+20V


CARD OFA
PIN 1

PEAK DETECTOR

OGA, OGB, OGC

The peak detector operates from either positive or negative rectified signals from the output of level detectors. The peak detector can also be used with class A signals to locate either positive or negative peaks as selected by the input wiring. Provision is included for threshold enablin prior to the output when used with level detector (EI-Series) or "diode ANDing" at the output of level detector (EDA, EGA). The output of the peak detector is shaped to a nominal 3/4-usec pulse independent of the exact shape of the peak.

Peak detection is accomplished by first differentiating the input signal (C01, R01 and C04, R02) and then detecting the zero crossover point of this differentiated signal in the two-stage differential amplifier (Q01 Q02, and Q03, Q04). The detected zero crossover point is re-referenced to ground by Q05 and then shaped by the multivibrator (Q06, Q07) into a nominal 3/4-usec "1" pulse. Pin 8 receives the threshold enable signal, when used with the level detector to disable the output shaper. Other threshold enables (level detector EDA, EGA) are ANDed with pins 11 and 12. Mixing resistors are provided at pins 9 and 10 for use in forming composit signals with peak detectors on other tracks for deskewing purposes.

Pin 1* is used to receive positive rectified signals (pin 5** grounded); and pin 5** is used to receive negative rectified signals (pin 1* grounded). Therefore, the peak detector looks for a negative peak on pin 5** or a positive peak on pin 1*. Balanced or single-ended class A signal may be used also, and the input wiring determines which polarity peak is detected.

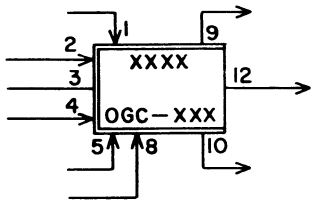
The multivibrator is triggered by the negative input signal at the base of Q06. Conduction of Q06 couples a positive pulse to the base of Q07 and causes it to switch off. Multivibrator regeneration is completed by the common emitter resistor R13. The period of the mutivibrator is determined by C07 and R14. Recycle time is determined by R15, R16, and C07. Diode CR03 supplies the additional emitter current necessary for the collector load of Q07 and references the emitter current to near ground for this stable state of the multivibrator. During the multivibrator period

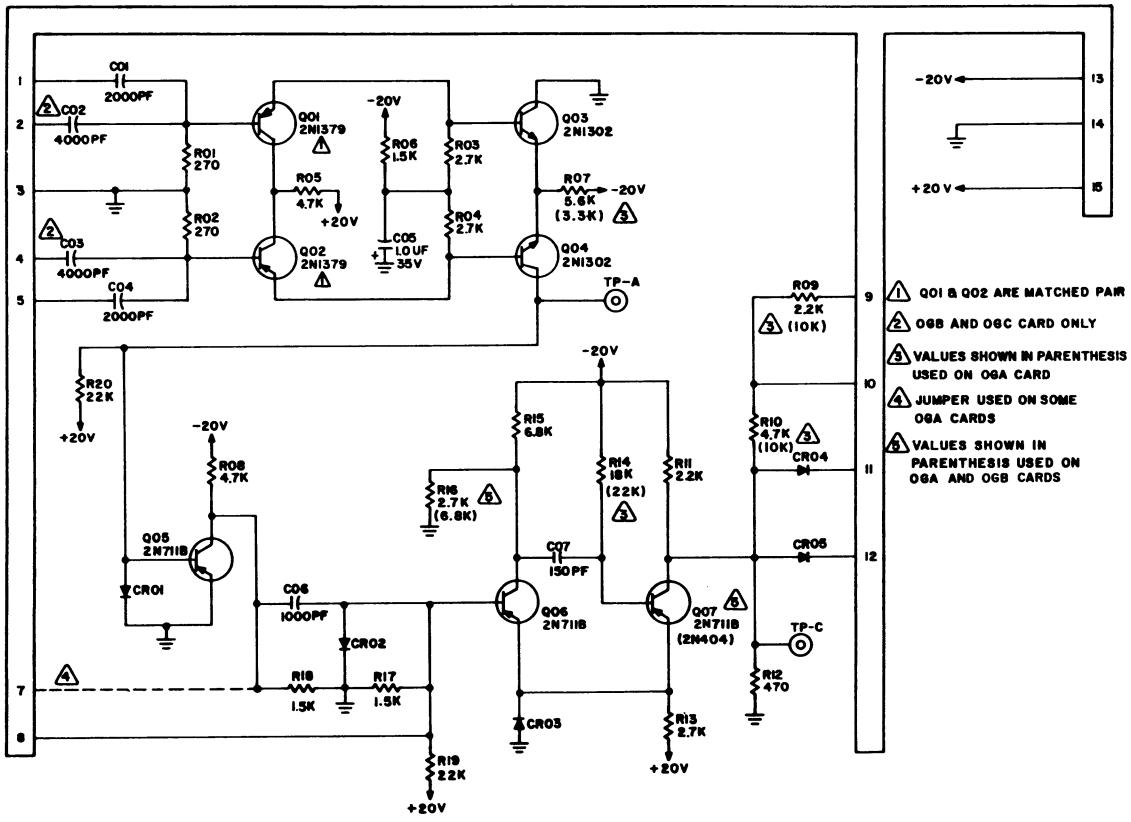
* Pin 2 for 75 ips, OGB, OGC only

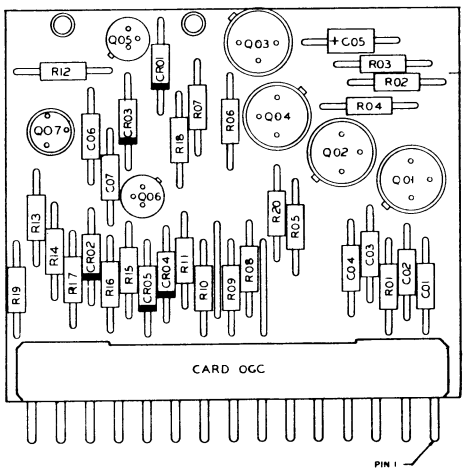
** Pin 4 for 75 ips, OGB, OGC only

CR03 is reverse-biased, permitting the gain of Q06 and Q07 to be utilized through a common emitter resistance R13, providing fast fall and rise times.

SYMBOL







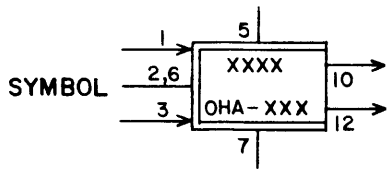
PEAK DETECTOR
OHA

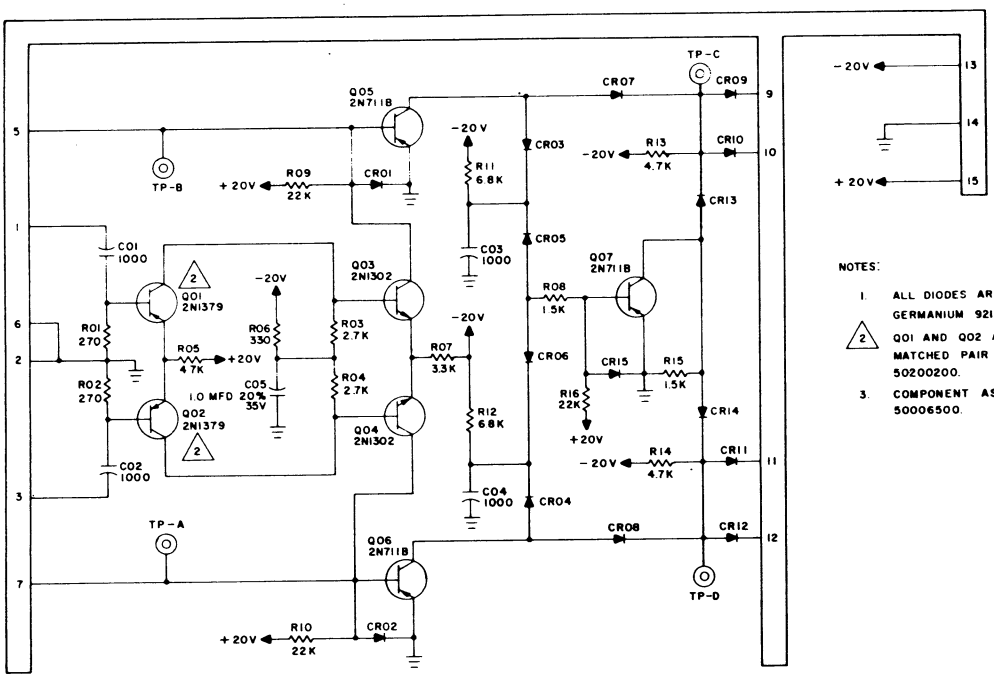
The peak detector operates from a Class A amplified head signal. It is designed for use with balanced input signals but may also be operated single ended by grounding the other input pin. The circuit has two output sections. TP-C provides an output logic "1" pulse for a negative peak (pin 1 relative to pin 3), and TP-D provides an output logic "1" pulse for a positive peak. Both pulses are 0.5 to 1.1 usec width at the -2v level. Provision is included (pins 5 and 7) for threshold enabling prior to the output when used with the ELA or a similar circuit. The circuit is designed for 120 kc data rates (60 and 120 kc sine-wave components) in phase modulation recovery where the amplitude of the nominal signal is 8v peak-to-peak.

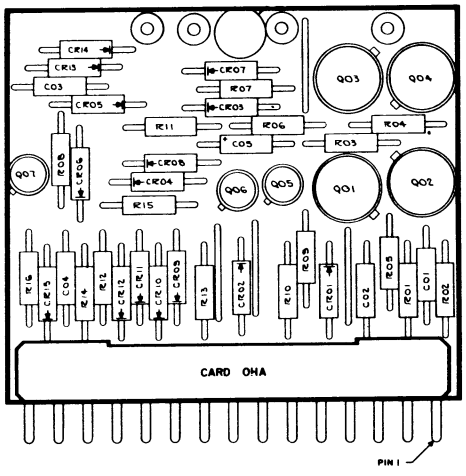
Peak detection is accomplished by first differentiating the input signal (C01, R01 and C02, R02) and then detecting the zero crossover point of this differentiated signal in the two-stage differential amplifier (Q01, Q02 and Q03, Q04). The detected zero crossover point is re-referenced to ground by Q05 and Q06. Threshold disabling may also be connected to the base leads of Q05 and Q06 by supplying current from a negative source. A minimum of 2 ma is required for either transistor and pins 5 and 7 must be from isolated circuits to prevent interaction between Q05 and Q06.

An output pulse appears when Q05 (TP-C) or Q06 (TP-D) turns off. The width of either output pulse is determined by the time Q07 remains off following the switching off of either Q05 or Q06. When Q05 turns off, C03 and R11 in the base circuit of Q07 determine the output pulse width. When Q06 turns off, C04 and R12 determine the width.

Caution should be exercised in using this circuit to drive standard inverters since logic "0" outputs may range from -0.6v to -1.2v. This is caused by the additional series output diode used in the pulse shaping circuit.




TP-C
TP-B
TP-A
TP-D
Q01 2N1379
Q02 2N1379
Q03 2N1302
Q04 2N1302
Q05 2N7118
Q06 2N7118
Q07 2N7118
-20V
+20V
R01 270
R02 270
R03 2.7K
R04 2.7K
R05 4.7K
R06 330
R07 3.3K
R08 1.5K
R09 22K
R10 22K
R11 6.8K
R12 6.8K
R13 4.7K
R14 4.7K
R15 1.5K
R16 22K
C01 1000
C02 1000
C03 1000
C04 1000
C05 1.0 MFD 20% 35V
CR01
CR02
CR03
CR04
CR05
CR06
CR07
CR08
CR09
CR10
CR11
CR12
CR13
CR14
CR15
- 20V
+ 20V
NOTES:
1. ALL DIODES ARE GERMANIUM 92116002.
2. Q01 AND Q02 ARE MATCHED PAIR PER 50200200.
3. COMPONENT ASSY NO. 50006500.


CARD OHA
PIN 1

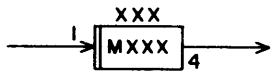
INPUT AMPLIFIER

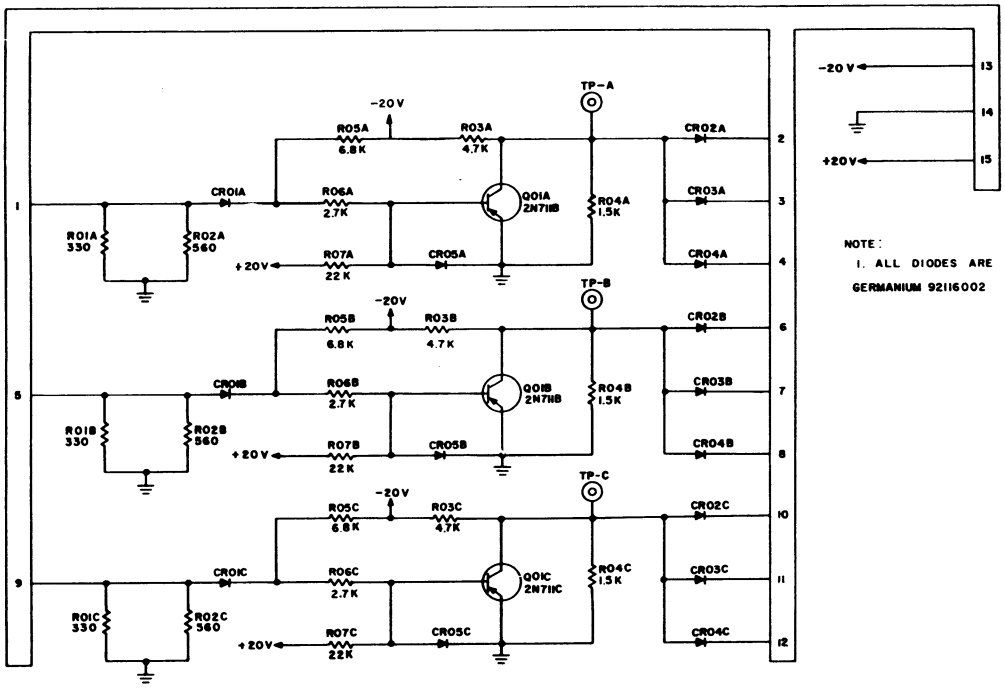
OIA

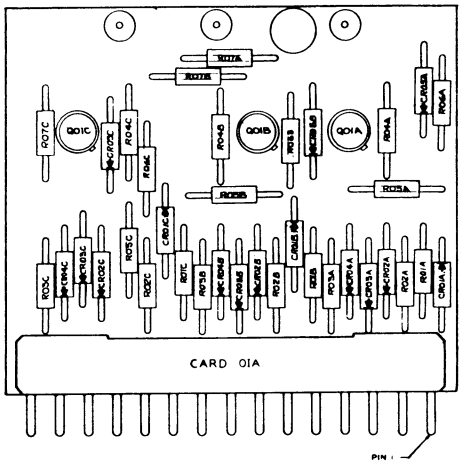
The input amplifier card is used to interface from external equipment operating with signal excursions of 0 to -6v. Its output matches standard logic signals (0 to -3v). The input terminates a line at approximately 200 ohms to ground and switches on minimum excursions of -1 1/2 to -4 1/2v.

Three identical circuits are used. Each circuit has three output diodes for AND terms.

SYMBOL




-20 V
13
14
+20V
15
NOTE:
1. ALL DIODES ARE
GERMANIUM 92116002
TP-A
TP-B
TP-C
-20V
R05A
6.8K
R03A
4.7K
CR02A
CR01A
R06A
2.7K
Q01A
2N711B
R04A
1.5K
CR03A
R01A
330
R02A
560
+20V
R07A
22K
CR05A
CR04A
R05B
6.8K
R03B
4.7K
CR02B
CR01B
R06B
2.7K
Q01B
2N711B
R04B
1.5K
CR03B
R01B
330
R02B
560
+20V
R07B
22K
CR05B
CR04B
R05C
6.8K
R03C
4.7K
CR02C
CR01C
R06C
2.7K
Q01C
2N711C
R04C
1.5K
CR03C
R01C
330
R02C
560
+20V
R07C
22K
CR05C
CR04C
1
2
3
4
5
6
7
8
9
10
11
12


CARD 01A
PIN 1

LONG TERM DELAY
OJB

The OJB card is intended for applications requiring a long delay which does not have to be accurately adjusted. By means of jumper options, a total of twenty discrete delays of a logic "0" input can be selected in the range of 2 msec to 50 sec. Table 1 lists the delays for a given set of jumpers. An alternate presentation of the delays is shown in figure 1 and is used when some intermediate value of delay is needed. This can be accomplished with external capacitors between pins 1 and 4.

The input and output waveforms are shown in figure 2. The input is derived from an output card or opening of a set of contacts.

Referring to the schematic, the circuit contains a unijunction transistor (Q02), the basic timer, a silicon controlled rectifier as a bistable device (Q03), and the output transistor (Q01).

The input is applied at pin 1. If this is at ground, no voltage exists on the Q02 - Q03 combination. Therefore, since Q01 has no base voltage, it will be off and the output is -3 volts.

Assuming the input is allowed to go negative, approaching -20v or opened, voltage is applied to the unijunction transistor timer via R01. The timing capacitor C01 (or C01 in parallel with C02) will begin to charge through R01, R02, and R03 (or R03 in parallel with R04, R05, and/or R06). Although the timing capacitor is shunted by the emitter to base 1 circuit of the unijunction transistor, this is not a problem since it represents an impedance of over 3 meg ohms.

When the capacitor reaches 6 to 8 volts with polarity as indicated on the schematic, the unijunction transistor becomes regenerative so the emitter to base 1 impedance becomes very small (approximately 20 ohms). This discharges the capacitor around the emitter-base 1 and R08 loop and generates a positive pulse on R08. This pulse is applied to the gate-emitter junction of Q03. Q03 turns on applying a negative voltage to Q01 so it also turns on. Since the junction of C01 and R01 is only two diode drops from ground when Q01 and Q03 turn on, the voltage on the timing circuit is reduced to approximately -1.6 volts. This prevents the unijunction transistor from becoming a free running oscil-

lator. The output of Q01 remains within a fraction of a volt of ground after the delay period.

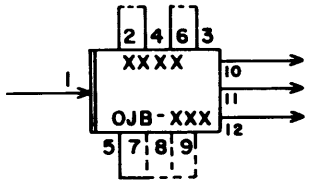
Normally the time delay is changed by changing either the timing capacitor (C01, C02) or the timing resistor (R02, R03). However, by jumpering between pins 3 and 6, a resistor divider reduces the voltage across the unijunction transistor base 1 to base 2. This indicates the capacitor charges to a lower level before regeneration occurs in the unijunction transistor, thereby reducing the delay.

If the input is again brought to ground, the bottom end of R01 is pulled to approximately -0.6v of ground. Since this is less than the voltage drop across Q03 plus the base-emitter junction of Q01, Q03 and Q01 will both turn off. Note that if pin 1 does not come within -1.0v of ground, Q03 and Q01 may not turn off.

The current through Q03 must delay to the holding current level before it will turn off; this takes approximately 40 usec. Therefore, the input logic "1" pulse wodth W in figure 2 should be at least 50 usec wide.

If the input in figure 2 is returned to 0 volts or logic "1" before the time delay has expired, the output will remain at logic "1". Since the timing capacitor may have charged close to the unijunction firing level, it will have to discharge to almost 0 before a new delay period can be initiated. The length of the waiting period should be 10% or more of the minimum delay given in figure 1 for either the 1 uf or 68 uf capacitor (200 usec for the 1 uf capacitor and approximately 14 msec for the 68 uf capacitor). Under these conditions a 10% change in the time delay can be expected due to residual voltage on the capacitor.

SYMBOL



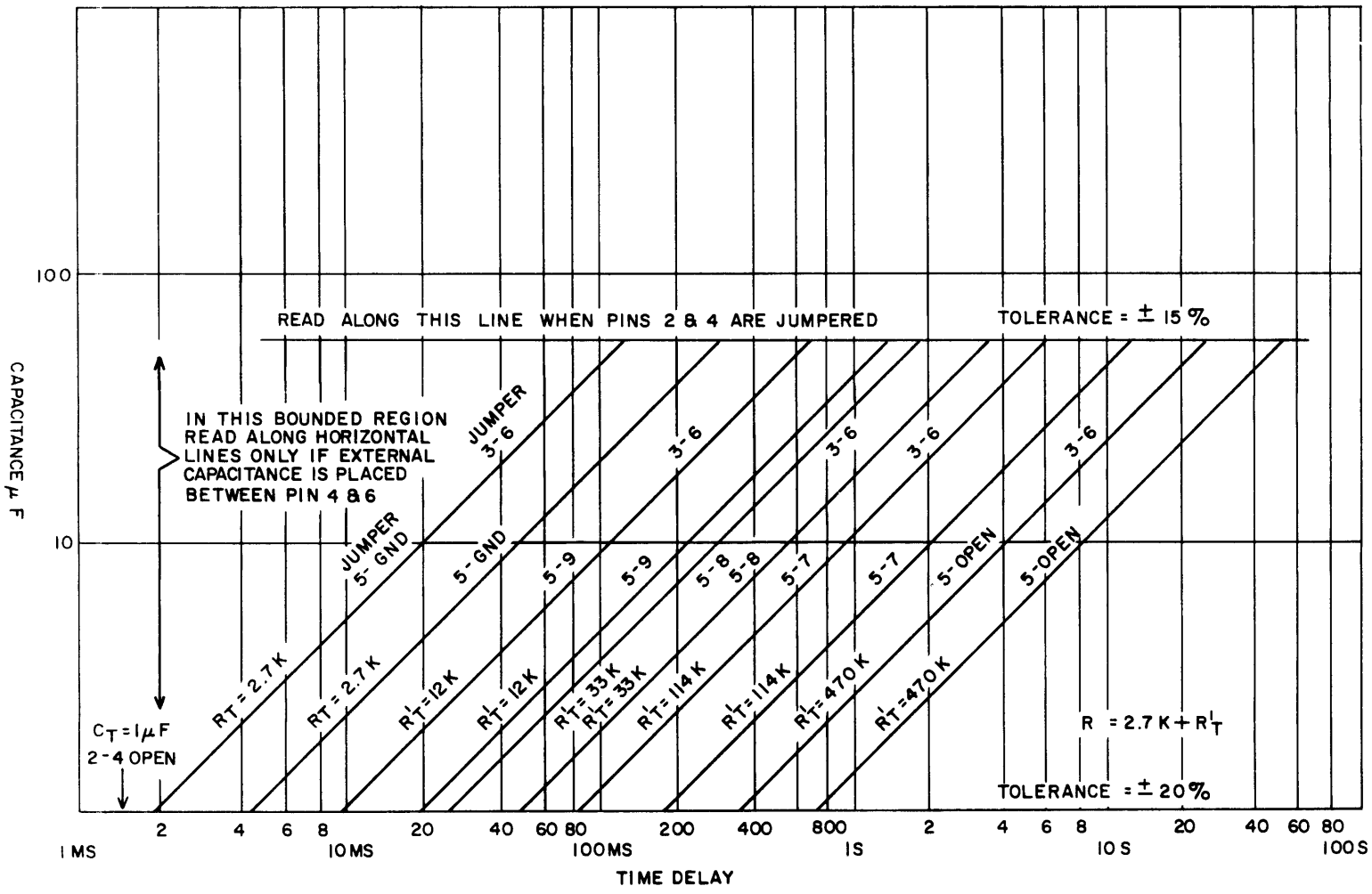
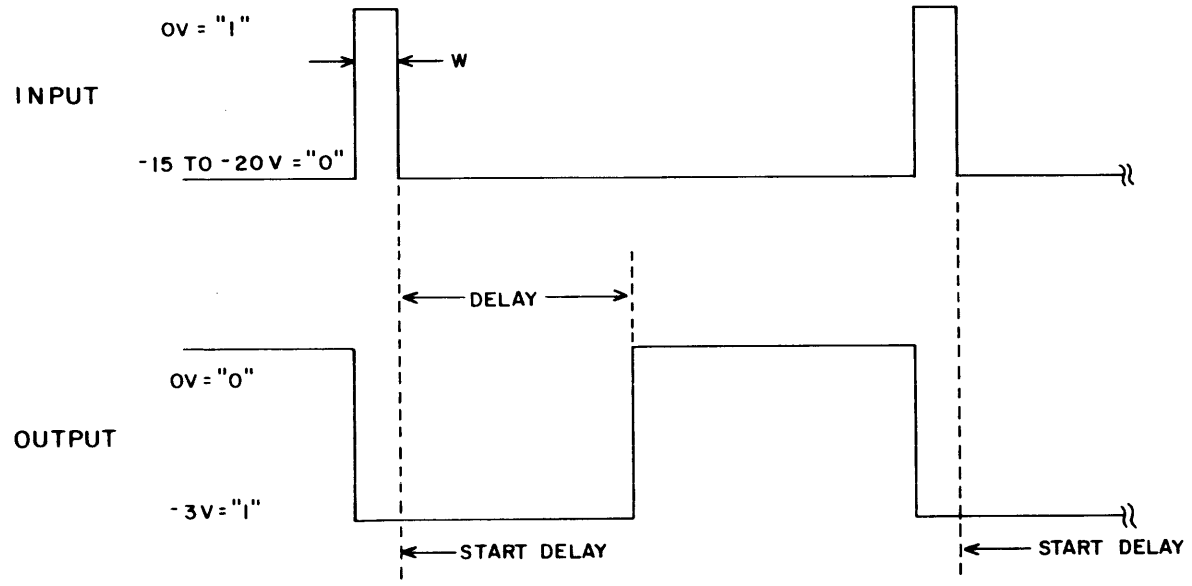
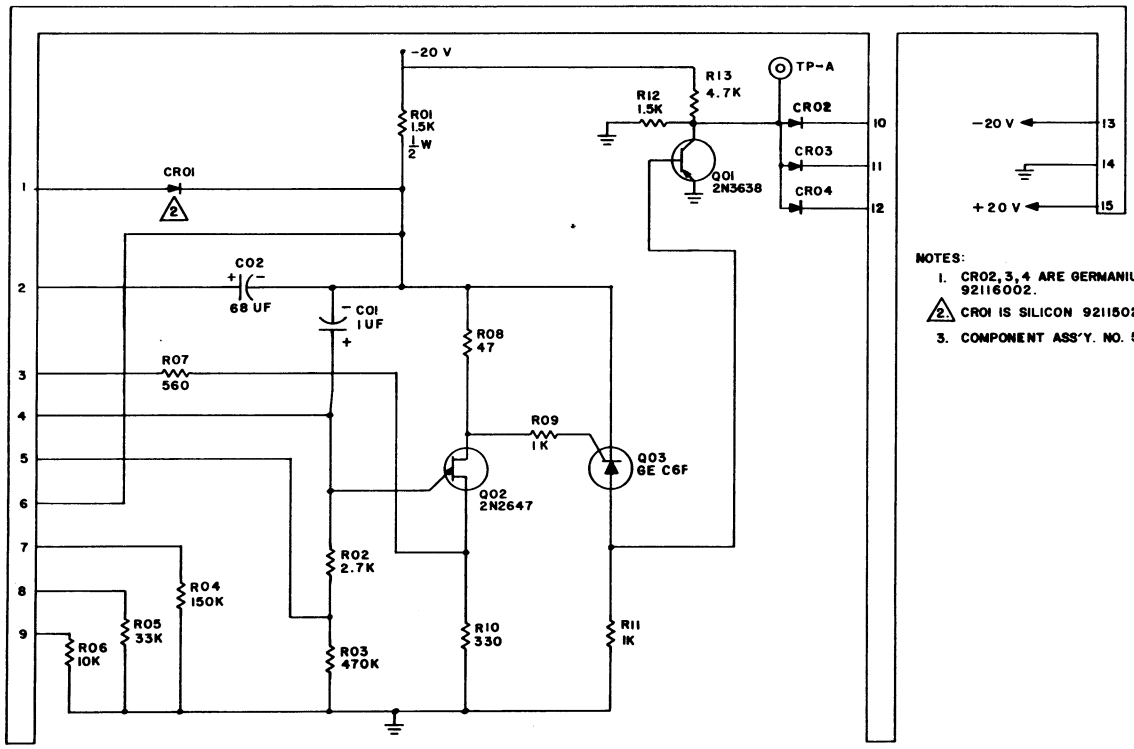


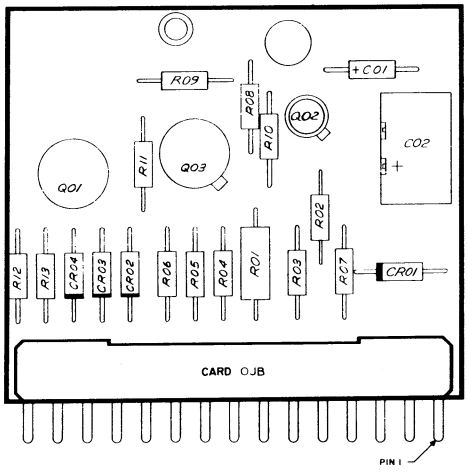
FIGURE 1. TIME DELAY VS EXTERNAL CONNECTIONS

Table 1. Delays

Delay ±20%	Jumper Pins	Delay ±20%	Jumper Pins
1.9 msec	3-6, 5-gnd	340 msec	3-6
4.4 msec	5-gnd	650 msec	2-4, 3-6, 5-9
8.8 msec	3-6, 5-9	760 msec	none
19 msec	5-9	1.3 sec	2-4, 5-9
23 msec	3-6, 5-8	1.7 sec	2-4, 3-6, 5-8
50 msec	5-8	3.6 sec	2-4, 5-8
84 msec	3-6, 5-7	6.0 sec	2-4, 3-6, 5-7
145 msec	2-4, 3-6, 5-gnd	11.5 sec	2-4, 5-7
183 msec	5-7	24 sec	2-4, 3-6
315 msec	2-4, 5-gnd	52 sec	2-4




-20 V
TP-A
R13
4.7K
R12
1.5K
R01
1.5K
1/2 W
CR02
CR03
CR04
Q01
2N3638
CR01
C02
68 UF
C01
1UF
R08
47
R07
560
R09
1K
Q03
GE C6F
Q02
2N2647
R02
2.7K
R04
150K
R05
33K
R06
10K
R03
470K
R10
330
R11
1K
-20 V
+20 V
NOTES:
1. CR02, 3, 4 ARE GERMANIUM 92116002.
2. CR01 IS SILICON 92115021.
3. COMPONENT ASS'Y. NO. 5002301.

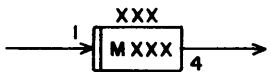

R09
+C01
R08
Q02
C02
R10
Q03
R11
Q01
R02
R12
R13
CR04
CR03
CR02
R06
R05
R04
R01
R03
R07
CR01
CARD OJB
PIN 1

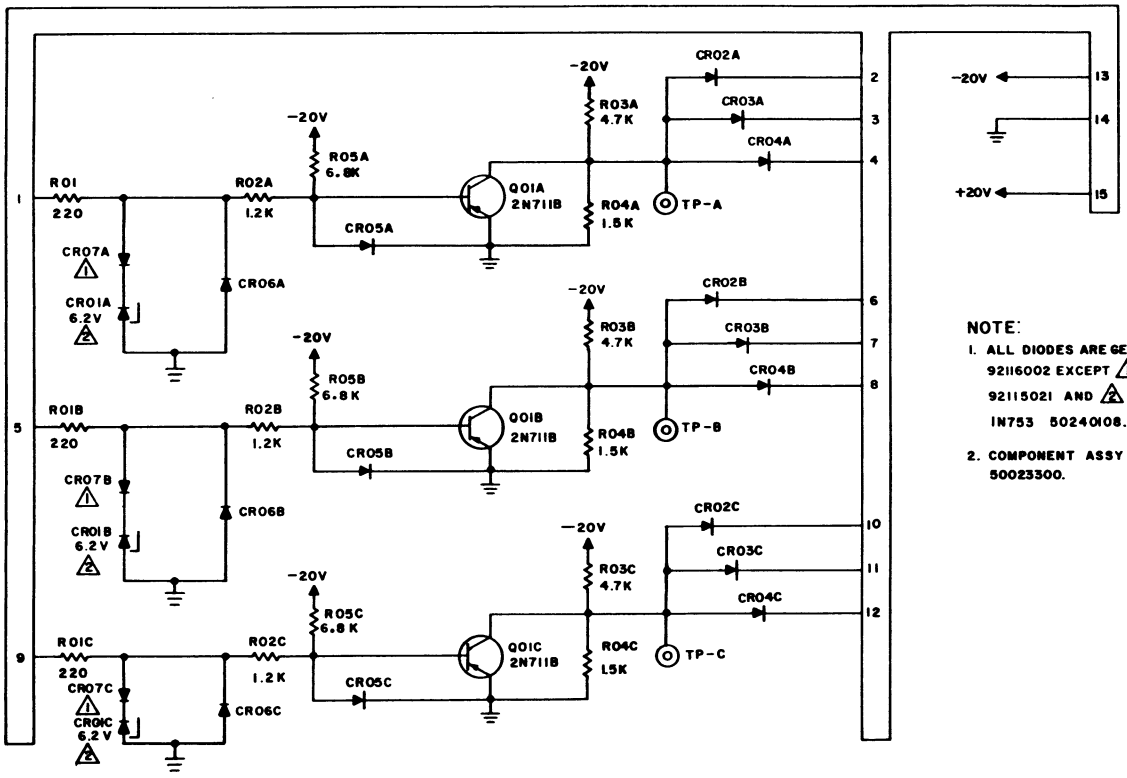
INPUT AMPLIFIER
OKA

The input amplifier card is used to interface from external equipment operating with signal excursions from 0 to +9v. Its output matches standard logic signals (0 to -3v). Input to the amplifier is via a 220-ohm series resistor. The other end of the resistor is clamped at +6.5v in the positive direction and at ground in the negative direction. A minimum excursion of +2v to +6v is required at the input pins. Line noise and ringing shall be outside this +2v to +6v region to prevent unwanted switching of the circuit.

Three identical circuits are provided on each card. Each circuit has three output diodes for AND terms.

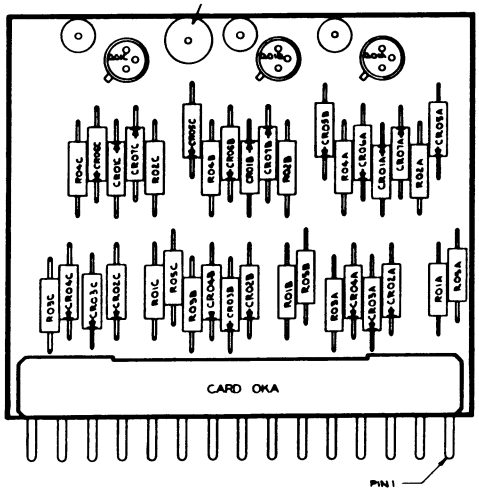
SYMBOL





NOTE:

1. ALL DIODES ARE GERMANIUM 92116002 EXCEPT ⚠1 SILICON 92115021 AND ⚠2 ZENER IN753 50240108.
2. COMPONENT ASSY NO. 50023300.



FLYBACK VERIFY FLIP-FLOP
OLA

This flip-flop was originally designed for use in the 501 Printer error-checking system known as echo checking. The device is a toggle flip-flop with a 2-term AND on the set input, a clear line, and a toggle input. The circuit is normally set when a given character is to be printed. After the hammer for that particular character fires, an inductive-kick pulse, during current delay, toggles the flip-flop back to a cleared state. A lamp is provided on the card so that one can see what state the circuit is in. The output from 12 such cards are capable of being Anded together for forming of an error signal. Output voltage at the test points is nominally -10v instead of the usual -3v.

The circuit is set when standard -3v levels exist on both terms of the AND input or both inputs are open. The flip-flop is cleared by 0 volts on the clear line. Negative pulses on the toggle input of at least 4v will change the state of the flip-flop. The toggle pulse is typically developed from the inductive kick initiated at turnoff of the current to the inductive load (a hammer in the 501 Printer).

Cirucit operation is best understood by referring to the circuit schematic. Assume the following sequence on the inputs: a) the circuit is cleared, b) set pulses are put in, and c) the toggle pulse is applied.

When pin 9, the clear line, is pulsed to within -1.0v of ground, and at least one set input is near 0v, the collector of Q03 is grounded. By the divider action of R08, R09, and R10, a plus voltage of about 1.0v results at the base of Q02. This turns Q02 off and its collector voltage becomes -10v. Since Q02 collector is tied to Q03 base by resistor R12, the -10v collector voltage holds the base of Q03 on. The circuit is now in the cleared state and will remain there until either the set pulses or toggle pulse are applied.

To set the flip-flop, assume that a negative 3 volts appears on both pins 2 and 3 or that both are open, i.e., the AND term is complete and that pin 9 is either open or more negative than -10 volts. Pin 9 voltage should not be less than -10v, otherwise the collector of Q03 will be clamped to whatever the clear line voltage is (assuming a low impedance clear source). Under these conditions, the junction of R07 and R08 is un-

clamped. The voltage divider composed of R07, R08, R09, and R10 lets the base of Q02 go negative thus turning Q02 on. Q02 collector voltage is now near zero and is coupled to the base of Q03 via R12. By the divider action of R12 and R14, the base of Q03 is driven +1 volt so that Q03 is off. The collector of Q03 goes to -10v which now supplies about 1 ma of base current to Q02, holding it on although the input on pins 2 and/or 3 goes back to ground. The flip-flop is now in the set state where it remains until cleared or a toggle pulse occurs.

When the hammer in the printer fires, an inductive kick pulse is formed at the end of the current pulse. This pulse is negative and about 10 volts. The toggle input to the flip-flop is applied to pin 1. Transistor Q01 has its base biased 3.5 volts positive so that the input pulse must rise to -3.7 volts before Q01 turns on. This is done to discriminate against noise pulses on the toggle line. Resistors R04 and R06 form a divider which hold Q01 collector at -10 volts. When Q01 goes on, its collector goes to ground as long as the input pulse is above -3.7 volts. The positive transition from -10v to ground on Q01 is passed through capacitors C03 and C04 as a positive 10-volt pulse.

At this point, consider the voltage across diodes CR05 and CR06. With Q02 on its collector is at about -0.2v. This is passed through forward biased diode CR04 so that the junction of R05 and CR05 is at nearly-0.4 volt. Since Q02 is on, its base voltage is also at about -0.2 volt. Thus it is seen that CR05 is reversed biased only about 0.2 volt.

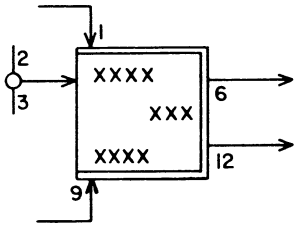
During this time Q03 is off, so its collector voltage of -10 volts is passed through forward-biased diode CR07. The junction of CR06 and R17 is therefore at about -10 volts. The base of Q03 is reversed biased by 1 volt so that diode CR06 is seen to be reverse biased by 11 volts.

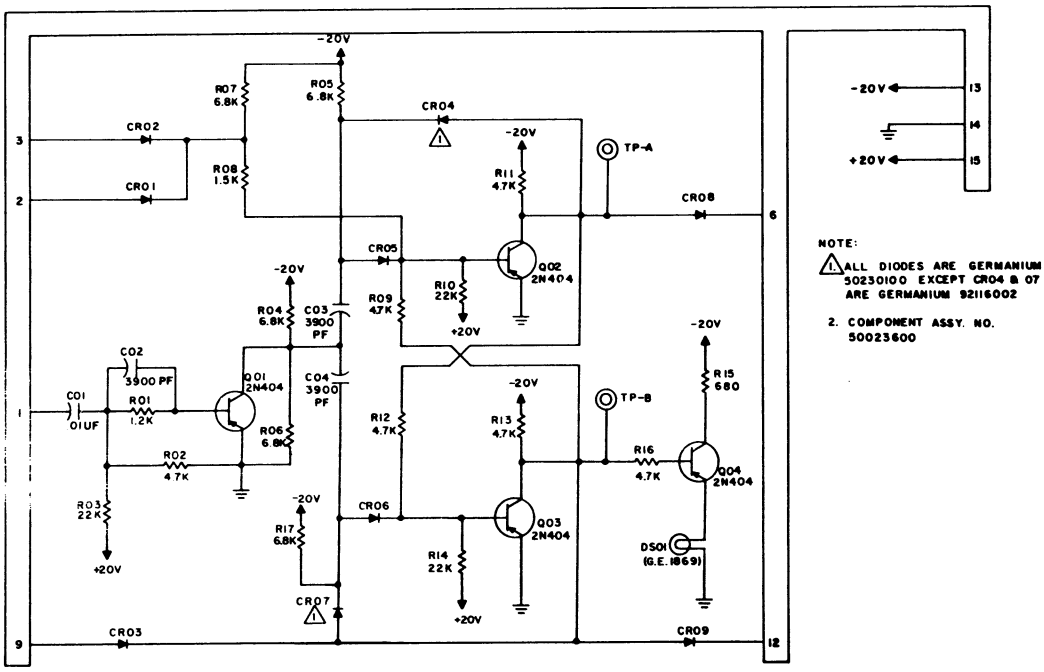
When the 10-volt pulse from Q01 passes through C03 and C04, it sees diodes CR05 and CR06 but can only pass through CR05 because the reverse bias on CR06 exceeds the pulse amplitude. Thus, the toggle pulse turns off the "on" transistor. If Q03 had been on, diode CR05 would be reverse biased and the toggle pulse steered to Q03 instead.

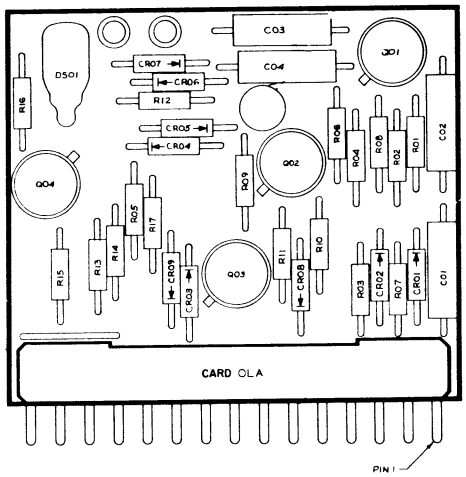
The indicator lamp is lighted when the flip-flop is set. Trans-

istor Q04 is basically an emitter follower circuit. When Q03 is off, the -10 volts on the collector allows base current to flow in Q04 and apply 10 volts to the lamp and the remaining 10v acorss R15.

SYMBOL







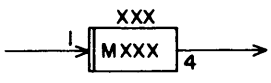
INPUT AMPLIFIER, HIGH FAN-OUT
OMA

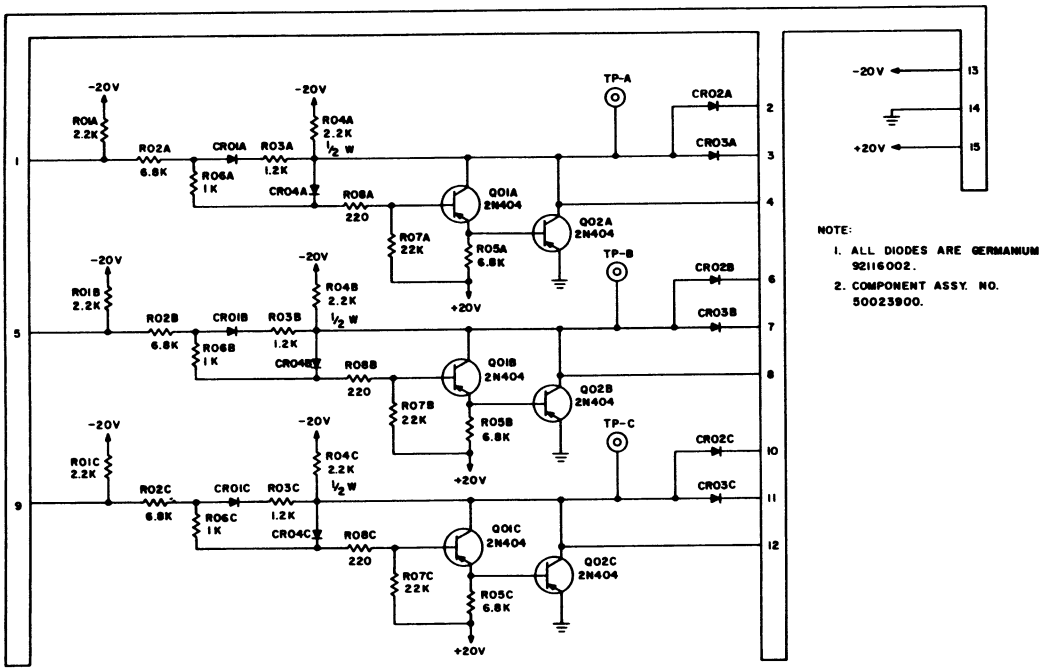
The OMA is a circuit designed to provide high fan-out logic signals for use in printer echo check circuitry. The OMA is essentially an "M" card, i.e., an input amplifier which matches the output of an "L" card. The difference between this card and an "M" card is that one output diode per circuit is omitted on the OMA. There are three identical circuits per card. Output pins 4, 8, and 12 are connected directly to the collector of the output transistor and are the only output pins to be used for the high fan-out. The other two outputs per circuit have the logic diode in series to provide signals for ordinary logic circuits if desired.

When the input signal is at ground, the output switches to -3v. Thus an open input causes the output to switch toward ground. Each output (4, 8, or 12) may be fanned out to as many as 17 input logic circuits requiring 3 ma each, i.e., a 50-ma output at -.5v.

Circuit operation is as follows: an open input provides more negative drive to the base of Q02 through divider R02, R06, R08, R07, and emitter follower Q01. Q02 nears saturation but is held in the active region by CR04 and R08 feeding back negatively to the base of Q01. The output is held at -.5v. A ground at the input provides less drive to the base of Q02 through the divider and Q01. Q02 nears cut-off but is held in the active region by divider R04, R03, CR01, R06, R08, and R07. The output is maintained at -3v.

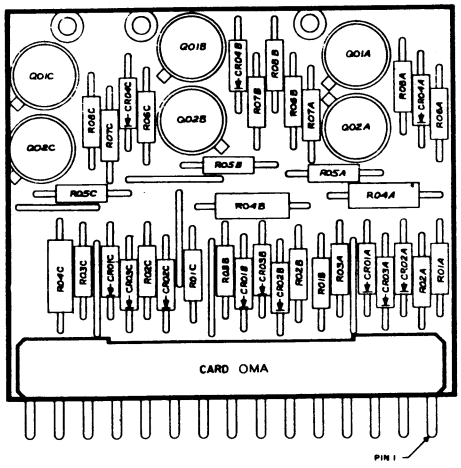
SYMBOL





NOTE:

1. ALL DIODES ARE GERMANIUM 92116002.
2. COMPONENT ASSY. NO. 50023900.



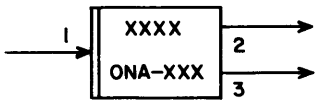
PHOTOCELL AMPLIFIER

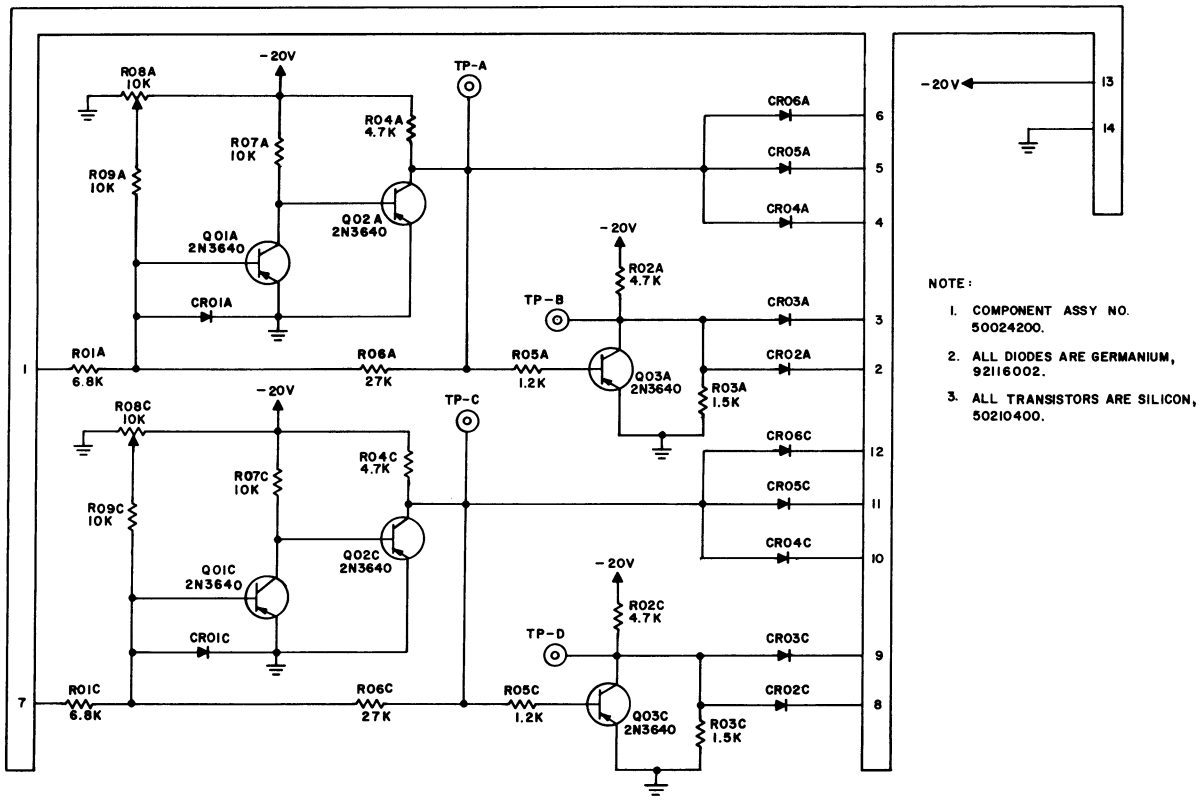
ONA

The photocell amplifier is designed to receive its input from a silicon photo transistor returned to +20V. When the photo transistor is illuminated, output of transistor Q03 is a "1" and Q02 is a "0". Outputs reverse when the photo transistor is unlighted. An adjustable potentiometer is provided to allow optimum centering of the amplifier switching point for tolerances in the light source, the photo transistor, and the input stage of the amplifier. Positive feedback around the first two stages of the amplifier provides a small amount of hysteresis to the input switching point to minimize the possibility of remaining in an intermediate state or switching on hum components of light sources.

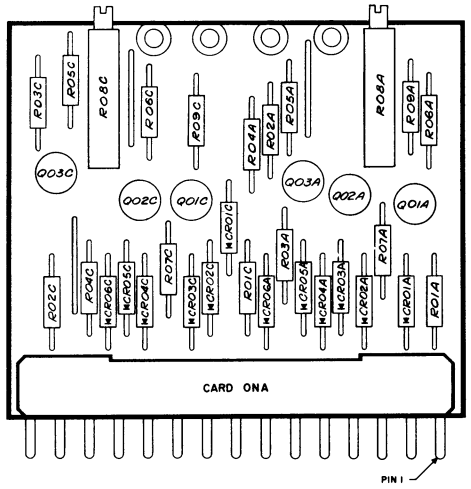
Q01 is an input inverting amplifier that is normally turned on by drive current through R09 from potentiometer R08. Q01 is turned off by supplying sufficient current to pin 1 via a photo transistor. Q02 acts as a second inverter that drives three output diodes for "AND" terms. The output of Q02 is coupled back to the input via R06 to provide a controlled amount of hysteresis in the input switching current. The output of Q02 is also used as an input to Q03. This input loading also limits the negative excursion at the collector output of Q02. Q03 compliments the output of Q02 by inversion, and has two output diodes for "AND" terms. Two identical circuits are provided on each card.

SYMBOL




-20V
TP-A
R08A 10K
R07A 10K
R04A 4.7K
R09A 10K
Q02A 2N3640
Q01A 2N3640
CR01A
R01A 6.8K
R06A 27K
R05A 1.2K
TP-B
R02A 4.7K
Q03A 2N3640
R03A 1.5K
CR06A
CR05A
CR04A
CR03A
CR02A
TP-C
R08C 10K
R07C 10K
R04C 4.7K
R09C 10K
Q02C 2N3640
Q01C 2N3640
CR01C
R01C 6.8K
R06C 27K
R05C 1.2K
TP-D
R02C 4.7K
Q03C 2N3640
R03C 1.5K
CR06C
CR05C
CR04C
CR03C
CR02C
1
2
3
4
5
6
7
8
9
10
11
12
13
14
NOTE:
1. COMPONENT ASSY NO. 50024200.
2. ALL DIODES ARE GERMANIUM, 92116002.
3. ALL TRANSISTORS ARE SILICON, 50210400.

ONA


CARD ONA
PIN 1

INPUT AMPLIFIER
OPA

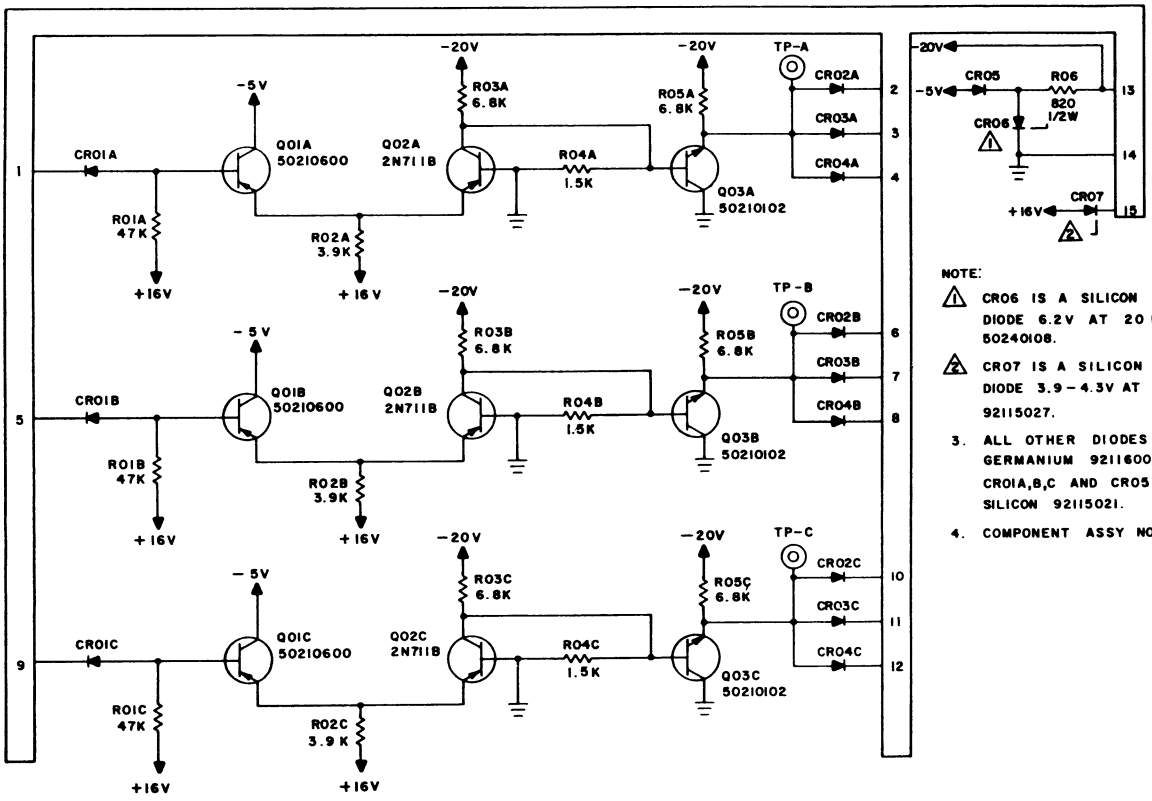
The OPA input amplifier card was initially designed for use on time shared lines between PED 9131 tape units and a controller used by Mitsubishi Co. of Toyko, Japan. The input is designed for signal excursions from +1.5v to -3.5v. Its output matches standard logic signals (0 to -3v). Original application utilizes 8 or less OPA circuits in parallel on twisted pair I/O lines of 100 ft. maximum length.

Loading of the line signal is minimized to permit OPA input amplifiers to be paralleled whether their power supply voltages are present or not. The OPA circuit includes power supply disconnect features to minimize loading to ground when voltages are not present. CR07 prevents loading when +20v supply is off. With -20v supply off, CR05 prevents loading to ground. Q01 is one-half of a differential amplifier (Q01, Q02) and represents very little loading to the line. Input switching threshold is -1v $\pm$ .2v. Q03 acts as an emitter follower to drive three output diodes available for AND terms.

A -3.5v input provides a logic "1" output (-4v min). A +1.5v input provides a logic "0" output (-3/4v). Switching time after the input signal is outside the threshold region (-.8v to -1.2v) is 200 nanoseconds or less in both directions.

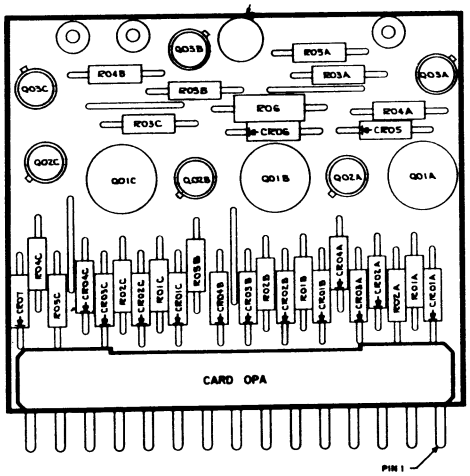
The line driver used in conjunction with the OPA will provide a "1" signal of -3.5v. When the driver is turned off, a termination at the end piece of equipment determines the "0" voltage on the line. The termination should match the line characteristics and provide a positive "0" voltage (when the line driver is off) sufficient to overcome line attenuation, crosstalk and other related factors.

SYMBOL



NOTE:

1. CR06 IS A SILICON ZENER DIODE 6.2V AT 20 MA, 50240108.
2. CR07 IS A SILICON ZENER DIODE 3.9-4.3V AT 5 MA, 92115027.
3. ALL OTHER DIODES ARE GERMANIUM 92116002, EXCEPT CR01A,B,C AND CR05 ARE SILICON 92115021.
4. COMPONENT ASSY NO.50024800.



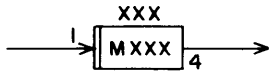
INPUT AMPLIFIER
0QA

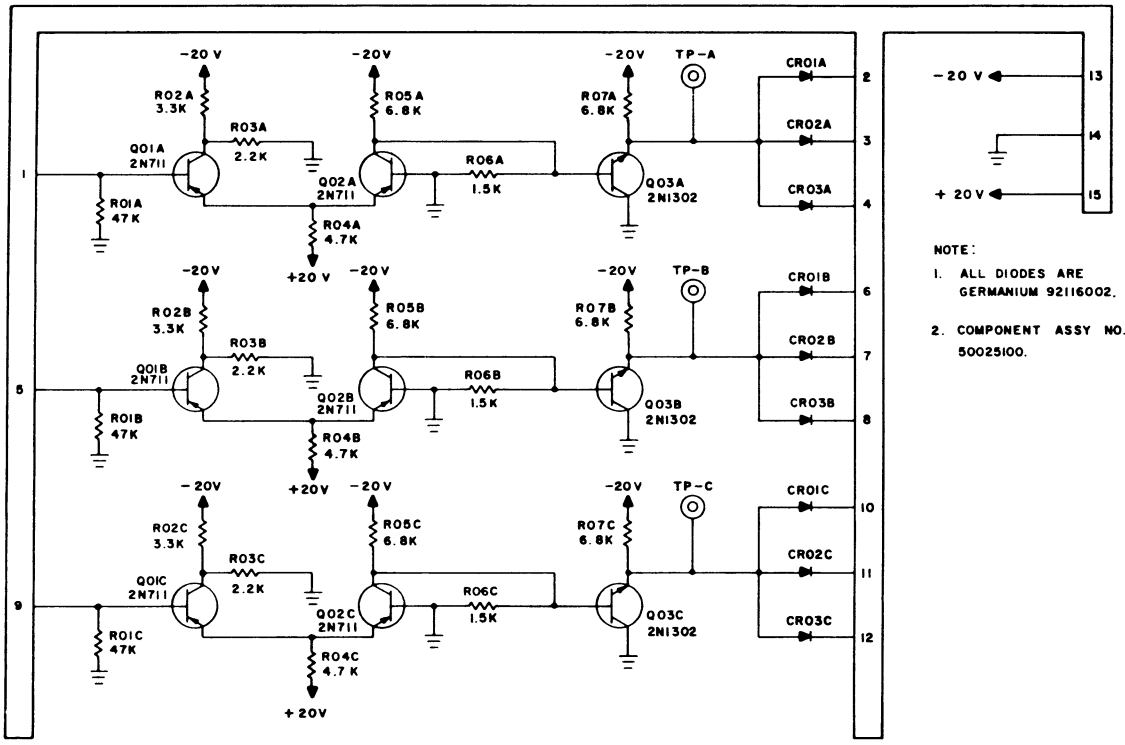
The input amplifier card is used to interface from a signal similar to IBM "n" levels to standard logic signals (0 to -3v). Up to eight 0QA receiver circuits may be paralleled (daisy-chained) on one line and located in various equipment such as magnetic tape units. To prevent excessive line loading, power is required on all receivers connected to a given line.

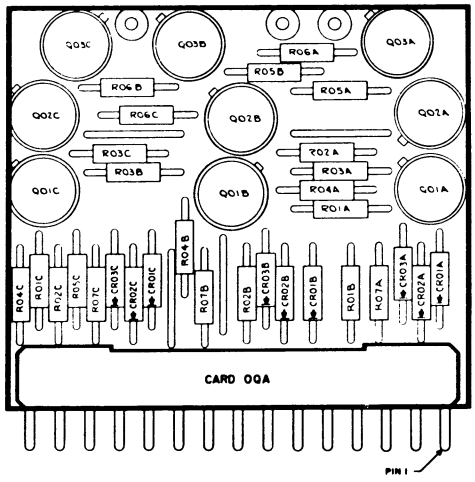
There are three identical circuits on each card and each circuit includes three transistors. Q01 and Q02 form a differential amplifier. The base of Q02 is tied to ground and provides the switching threshold of the circuit. Q03 is an emitter follower output. Each circuit has three output diodes for AND terms.

A minimum excursion of +0.4v to -0.4v free of noise is required at the input. The driver used in conjunction with the 0QA will provide a "1" signal of -3.5v. When the driver is turned off, a termination at the end piece of equipment determines the "0" voltage on the line. The recommended termination at the end of the line is 1200 ohms to +20v and 100 ohms to ground, making the "0" voltage +1.5v. The 0QA will switch to a "1" (-4v) with a "1" input in 0.25 usec and will switch to a "0" (0v) with a "0" input in 0.35 usec. Both switching times are maximum.

SYMBOL




-20 V
-20V
TP-A
TP-B
TP-C
R02A 3.3K
R03A 2.2K
R05A 6.8K
R07A 6.8K
Q01A 2N711
Q02A 2N711
Q03A 2N1302
R06A 1.5K
R01A 47K
R04A 4.7K
+20 V
CR01A
CR02A
CR03A
R02B 3.3K
R03B 2.2K
R05B 6.8K
R07B 6.8K
Q01B 2N711
Q02B 2N711
Q03B 2N1302
R06B 1.5K
R01B 47K
R04B 4.7K
+20V
CR01B
CR02B
CR03B
R02C 3.3K
R03C 2.2K
R05C 6.8K
R07C 6.8K
Q01C 2N711
Q02C 2N711
Q03C 2N1302
R06C 1.5K
R01C 47K
R04C 4.7 K
CR01C
CR02C
CR03C
1
5
9
2
3
4
6
7
8
10
11
12
13
14
15
NOTE:
1. ALL DIODES ARE GERMANIUM 92116002.
2. COMPONENT ASSY NO. 50025100.


Q03C
Q03B
Q03A
Q02C
Q02B
Q02A
Q01C
Q01B
Q01A
R06A
R05B
R06B
R05A
R06C
R02A
R03C
R03A
R03B
R04A
R01A
R04B
R04C
R01C
R02C
R05C
R07C
CR03C
CR02C
CR01C
R07B
R02B
CR03B
CR02B
CR01B
R01B
R07A
CR03A
CR02A
CR01A
CARD OQA
PIN 1

COMPARATOR AND READOUT
ORA

The ORA is specifically designed for large usage in optical reading machines using the map-matching principle to determine closest comparison to a set of ideal characters prewired in the form of a resistor matrix to a large flip-flop register. The flip-flop register represents the dark and light squares of the character area being optically scanned. The input to each ORA card is a varying analog signal from one output of a large resistor matrix. The ORA card charges its internal storage capacitor with the peak negative excursion of the analog input during an externally controlled time period. At the end of the period, the peak voltages stored in many ORA cards are probed and compared with each other. The ORA card with the most negative voltage stored causes a simplified flip-flop to be set in its output circuit. Flip-flops in other ORA cards normally remain unset, but if two ORA cards have closely equal voltages stored, both may be set. If two are set, a "doubles" circuit connected externally to the negative-going side of the ORA flip-flop monitors this undesired condition to denote a reject. The output flip-flop of each ORA card has five outputs on the side that approaches ground when set. Typically the flip-flop output diodes are used to encode a binary character which thus identifies the ORA card that has the largest negative voltage.

As soon as the probe and readout of the capacitors is completed and the flip-flop set, the internal storage capacitor may be cleared to look for a peak in the next time period. The flip-flop in the output circuit need not be cleared until just prior to the next time the capacitor voltages of the ORA cards are to be probed and compared.

Circuit operation is as follows. An analog signal swinging on both sides of -6v over a maximum range from 0 to -12v is applied to pin 1 and connected to emitter follower Q01. The peak negative excursions are used to charge C01 in a negative direction through CR03. The negative charge on C01 is retained by back-biasing CR02 during this period with a voltage at least 12 volts negative applied to pin 2. Pin 3 is also logically connected to a voltage near ground during this period to prevent R14 from charging the capacitor to more than about

-6v. R01 limits the steady state dissipation of Q01, and C02 stores energy to supply peak current during fast charging of C01. During this time, Q02 is also disconnected logically from the circuit by holding pin 4 at least 12 volts negative.

When the time period allowing C01 to charge on all ORA cards is completed, the comparison of the charge on C01 for all ORA's may then begin. This is accomplished by allowing pin 3 to go negative. This causes C01 to charge toward -20v at a slow rate determined by the time constant of R14, R15, and C01. Thus the voltage at the base of Q02 will be determined by the previous charge on C01 and the drop across CR03 and R15. R15 is selected to compensate for differences in the sum of base to emitter drops of Q01 and Q02 to provide better uniformity between ORA cards. Since CR03 is forward biased during charge of the capacitor as well as during readout, use of a high conductance diode eliminates most of the problem of variations of CR03 on different cards.

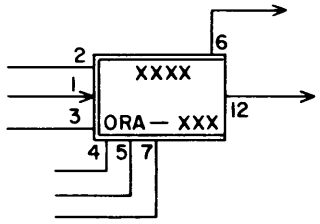
Pin 4 of all ORA cards is connected to a bus which is driven in the positive direction by an external current source. Thus, whichever ORA card has the most negative voltage at the emitter of Q02 when biased forward will hog all the current available from the bus with the constant current source. This will cause collector current to flow in the collector of Q02 of this ORA causing a voltage drop across R04, which will normally cause the base of Q04 to be more positive than the level reference on pin 5. This causes Q03 to turn off and Q04 to turn on. Normally pin 5 has a reference voltage that requires only 30-45 percent of the current available from the constant current source to turn Q04 on.

Q05 and Q06 are connected as a flip-flop. Assuming a clear pulse (pin 7 momentarily driven to near ground) had been applied, Q06 would be conducting and Q05 nonconducting. When Q04 turnon current equals 1-2 ma, this will cause Q05 to also turn on to put the flip-flop in its "set" state (TP-C near ground). Output pins 8-12 have normal logic levels for standard inverter signals. Output pin 6 is used in an external "doubles" circuit where pin 6 of all ORA cards are connected to a load terminated at ground. R11 limits the drive current in the negative direction. Thus if two or more ORA cards have their flip-flops set, the pin 6 bus will become sufficiently more negative so that an

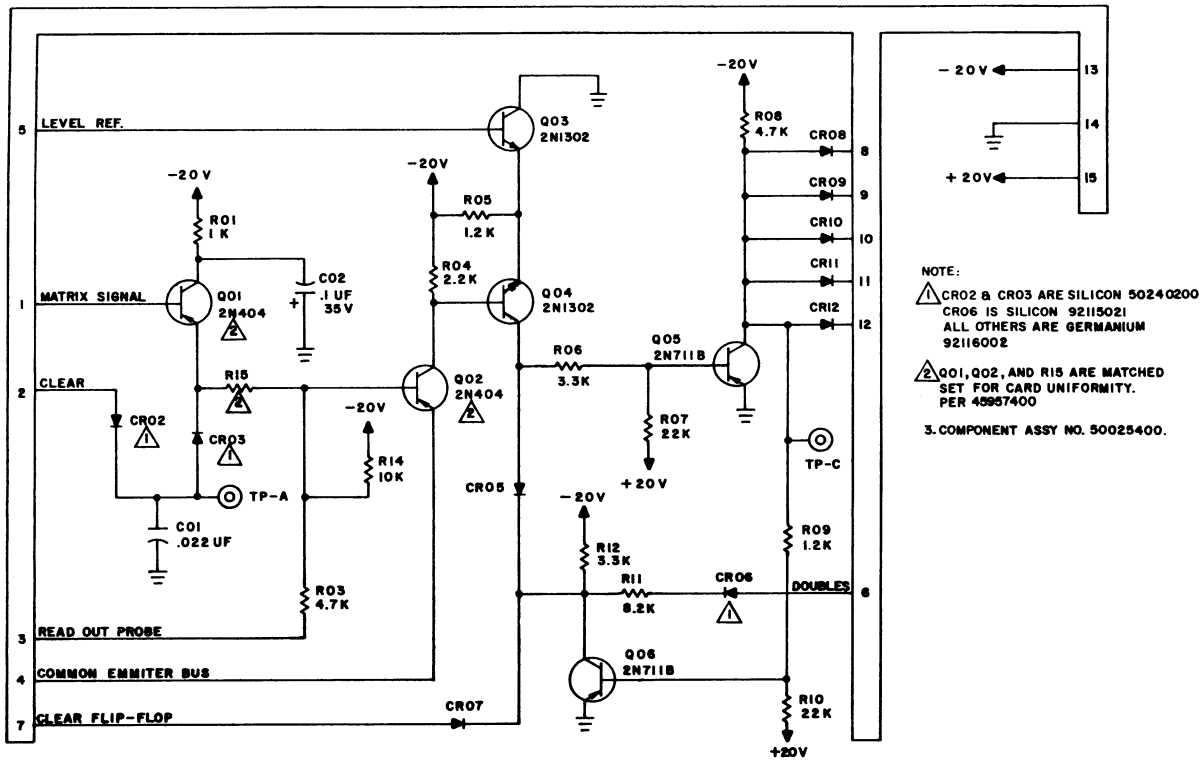
external quantizing circuit can easily detect the undesired condition which indicates two closely equal peak analog voltages.

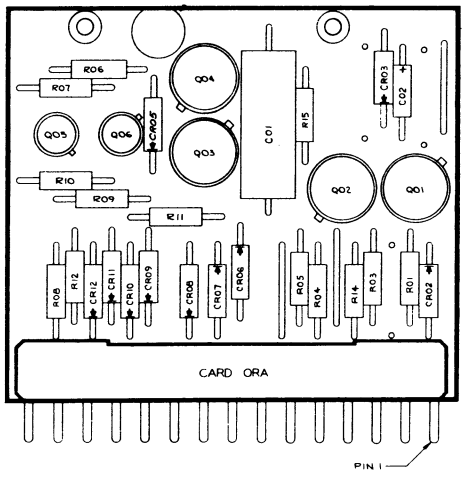
Certain considerations should be observed in use of the ORA circuit. The peak storage circuit ability to follow the input signal without excessive loading depends on both impedance and rate of change of the input. As an example, a 3v step function with 1K impedance requires 2.5 usec to charge to peak value. The rate at which the constant current source is applied during comparator readout can create a problem when the common emitter bus becomes long, so it should be slowly increased over at least 1 microsecond. The bias between the peak input signal and the common emitter readout changes with operating temperature. If all cards are at nearly the same temperature, as they should be, this will cause the temperature offset to be nearly equal on all ORA cards and not affect accuracy to a significant extent.

SYMBOL



COMPARATOR READOUT ORA





INPUT AMPLIFIER
OSA, OSB

The OSA input amplifier card was initially designed for use on time shared lines between 601 tape units and a 601 synchronizer. The input is designed for signal excursions from 0 to +2v. It's output matches standard logic signals (0 to -3v). Original application utilizes 4 or less OSA circuits on standard 24 pin I/O lines of 100 ft. maximum length (23 twisted pairs on a common ground reference). The input circuit is designed for use in conjunction with circuits such as the IS.. series output amplifiers or the ITA pulse delay and output amplifier. Loading of the line signal is minimized to permit several OSA input amplifiers to be paralleled whether their power supply voltages are present or absent.

Each of the three circuits function as follows. Q01 acts as an emitter follower to reduce line loading. Input switching threshold is $1.0 \pm .2$v and is determined by combining silicon and germanium semiconductor drops as follows.

$$(V_{BE} \text{ of } Q01) + (V_{fwd} \text{ of } CR01) - (V_{BE} \text{ of } Q02).$$

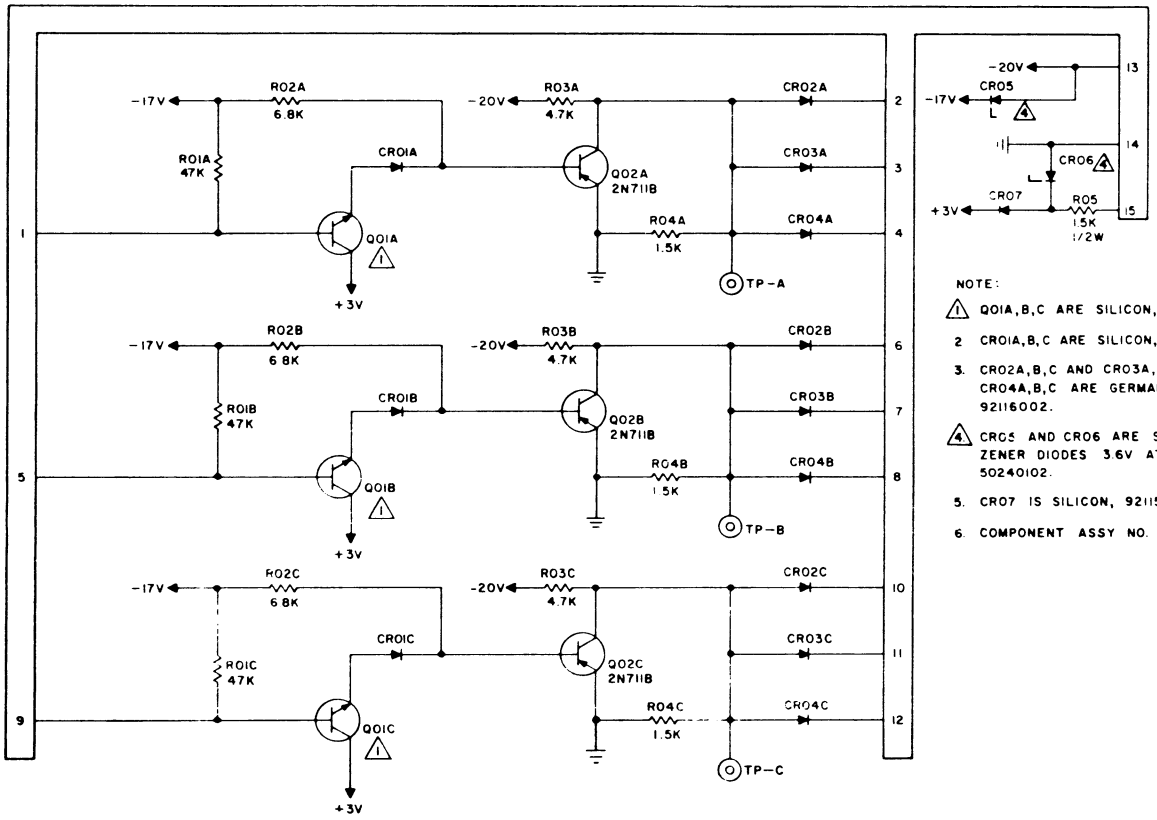
Q02 acts as an inverting circuit to drive three output diodes available for AND terms.

The OSA circuit includes power supply disconnect features to minimize loading to ground when voltages are not present. With +20v voltage off, the base to collector diode in Q01 cannot load to ground because of CR07 in the +3v network. With -20v voltage off, diode CR05 prevents R02 from loading to ground.

Signal polarity is as follows: A +2v input provides a logic "1" output (-4v min). A 0v input provides a logic "0" output (-3/4v). Switching time after the input signal is outside the threshold region (+0.8 to +1.2v) is 150 nanoseconds or less in both directions. The number of OSA input amplifiers paralleled depends on the margin of input signal provided as regards driving source, line attenuation, crosstalk and other related factors. Each OSA circuit can be expected to bias the line about 30 mv negative with 120 ohm terminations at both ends of a line.

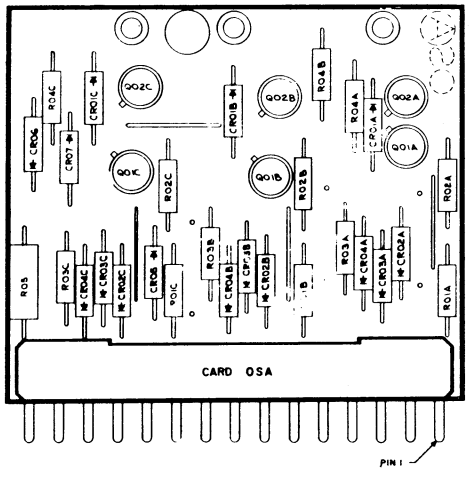
The OSB circuit is the same as the OSA as regards signal level conversion but is designed for use where a receiver is at one end of a line and it is undesirable to use a separate 120 ohm terminating resistor external to the card. The OSB does not incorporate the power supply disconnect features of the OSA circuit. It should therefore have its power supply on if OSA or similar circuits are to be active in receiving signals on the same line.

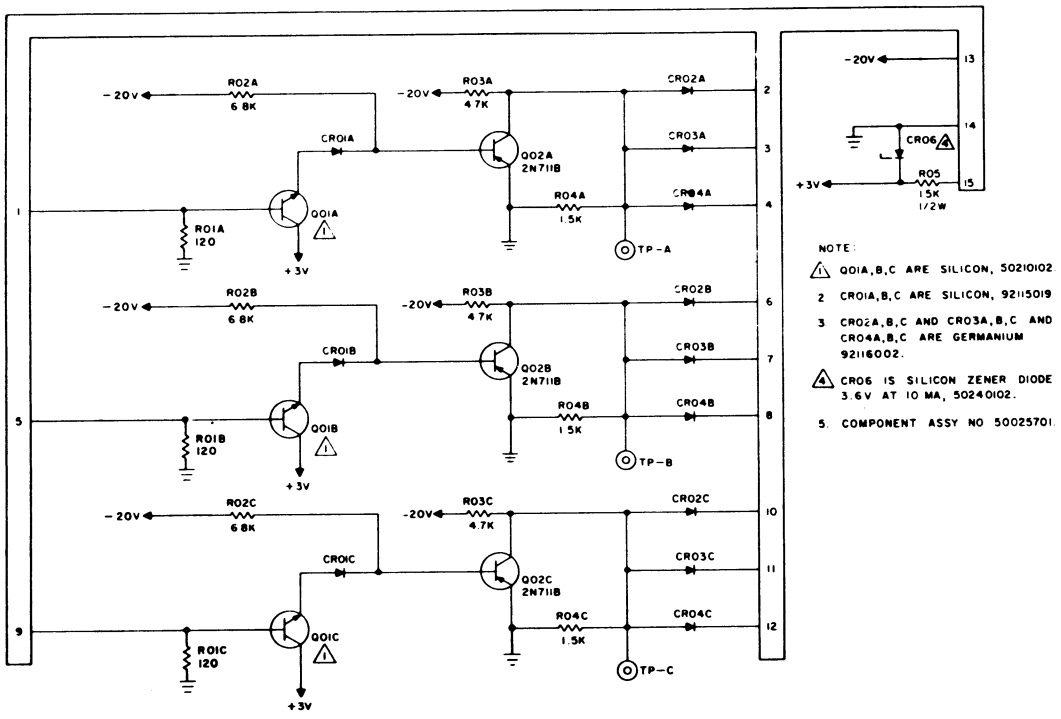
SYMBOL 

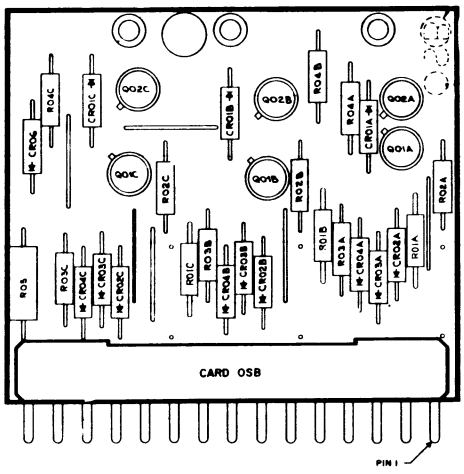


NOTE:

1. Q01A,B,C ARE SILICON, 50210102.
2. CR01A,B,C ARE SILICON, 92115019
3. CR02A,B,C AND CR03A,B,C AND CR04A,B,C ARE GERMANIUM 92116002.
4. CR05 AND CR06 ARE SILICON ZENER DIODES 3.6V AT 10 MA, 50240102.
5. CR07 IS SILICON, 92115021.
6. COMPONENT ASSY NO. 50025700.




-20V
R02A
6.8K
CR01A
Q01A
R01A
120
+3V
R03A
4.7K
CR02A
CR03A
CR04A
Q02A
2N7118
R04A
1.5K
TP-A
R02B
R01B
R03B
CR02B
CR03B
CR04B
Q01B
Q02B
R04B
TP-B
R02C
R01C
R03C
CR02C
CR03C
CR04C
Q01C
Q02C
R04C
TP-C
CR06
R05
1.5K
1/2W
NOTE:
1. Q01A,B,C ARE SILICON, 50210102.
2. CR01A,B,C ARE SILICON, 92115019.
3. CR02A,B,C AND CR03A,B,C AND CR04A,B,C ARE GERMANIUM 92116002.
4. CR06 IS SILICON ZENER DIODE 3.6V AT 10 MA, 50240102.
5. COMPONENT ASSY NO 50025701.


CARD OSB
PIN 1

LEVEL SWITCH
OTA

The OTA card is used in the disk file servo actuator. The circuit performs the function of switching the system between coarse and fine (long stroke and short stroke) control modes, when the long stroke signal gets near the trigger level.

The input at pin 1 can be driven between plus and minus 10 volts. The output line at pin 12 has standard logic levels. The plus or minus trigger levels can be set between approximately 50 and 400mv by potentiometers R03 and R05.

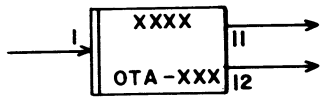
The circuit consists of two similar channels. The one for positive inputs consists of transistors Q02, Q04, and Q06. The one for negative inputs consists of transistors Q01, Q03, and Q05.

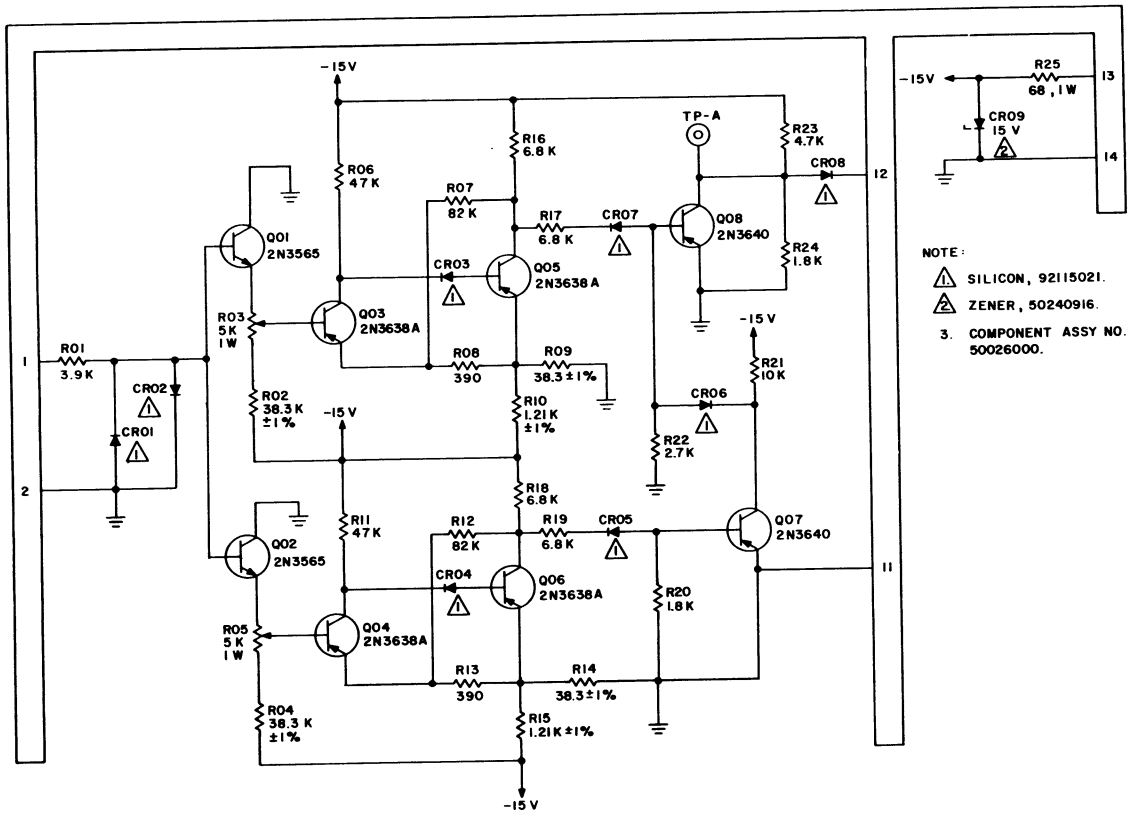
Assuming the trigger levels are set at approximately $\pm$50mv, if the input is within this range transistor Q03 is adjusted by R03 turning it off, and Q04 is adjusted by R05 turning it on. Transistor Q06 is then off, and Q05 and Q07 are on. There is no base drive for Q08, so it is off and the output is at logical "1".

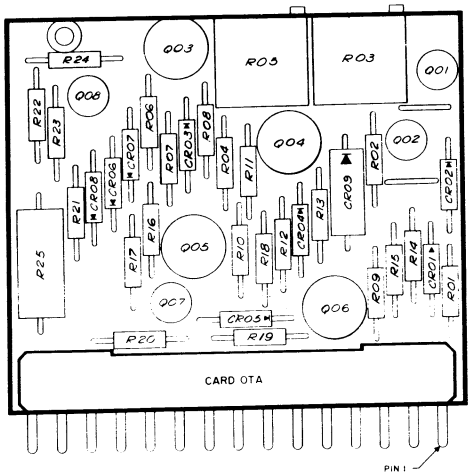
If the input exceeds the trigger level, the output will be at logical "0". Assuming a positive input, Q02 is driven so its emitter goes positive. This turns off Q04 and allows Q06 to turn on. Transistors Q04 and Q06 form a Schmitt trigger circuit. With Q06 turned on, its collector is near ground, so transistor Q07 goes off allowing its collector to go negative. During this time no change occurs in the states of transistors Q03 and Q05. Although Q05 tends to hold the base of Q08 at ground, diode CR07 opens, so the base of Q08 is driven on by Q07's being off. Therefore, transistor Q08 turns on and grounds the output to give a logical "0".

If the input goes negative above the trigger level, the emitters of Q01 and Q02 go more negative tending to turn on Q03 and Q04. Stages with Q05 and Q06 will both be off at this time. Transistor Q07 will now be on since the collector of Q06 is negative (approximately -7.5v). However, since Q05 is also off and its collector is also approximately -7.5v, Q08 will be driven on and the output is again at ground (logical "0"). Diode CR06 becomes back biased, so the on state of Q07 does not take base drive away from Q08.

SYMBOL


XXXX
OTA-XXX
1
11
12


-15V
R16 6.8K
R06 47K
R07 82K
R17 6.8K
CR07
TP-A
R23 4.7K
CR08
12
Q01 2N3565
CR03
Q05 2N3638A
Q08 2N3640
R24 1.8K
Q03 2N3638A
R03 5K 1W
R01 3.9K
CR02
CR01
R08 390
R09 38.3±1%
-15V
R21 10K
R02 38.3K ±1%
R10 1.21K ±1%
CR06
R22 2.7K
R18 6.8K
R11 47K
R12 82K
R19 6.8K
CR05
Q07 2N3640
Q02 2N3565
CR04
Q06 2N3638A
R20 1.8K
11
Q04 2N3638A
R05 5K 1W
R13 390
R14 38.3±1%
R04 38.3K ±1%
R15 1.21K±1%
-15V
1
2
-15V
R25 68, 1W
13
CR09 15V
14
NOTE:
1. SILICON, 92115021.
2. ZENER, 50240916.
3. COMPONENT ASSY NO. 50026000.


Q03
R05
R03
Q01
R24
Q06
R22
R23
R06
R08
Q04
R07
CR03
R04
R11
Q02
R21
CR08
CR07
CR04
R16
R25
Q05
R17
R10
R18
R12
CR04
R13
CR09
R02
CR02
R09
R15
R14
CR01
R01
Q07
CR05
R20
R19
CARD OTA
PIN 1

SCHMITT TRIGGER

OUA

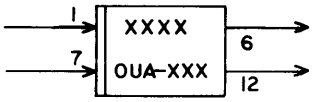
This circuit is used in the temperature servo for the disc file. It is used to indicate when the temperature in the file exceeds certain limits from the control temperature. There are two identical circuits per card.

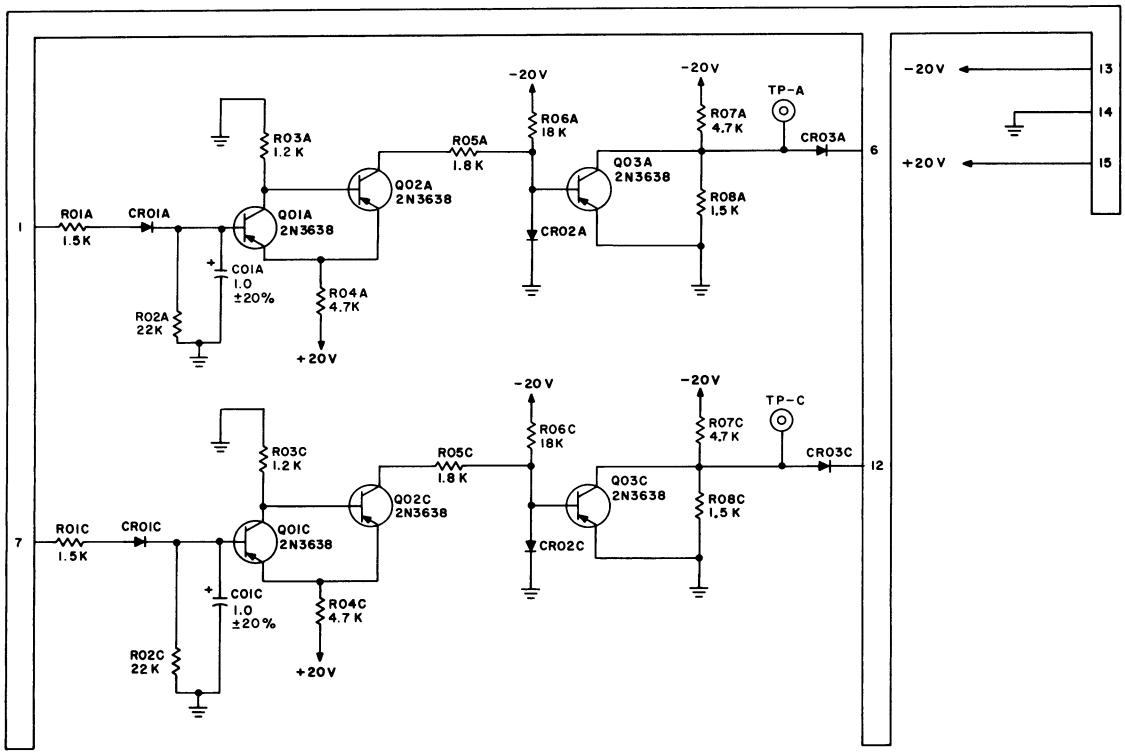
With the input voltage less than approximately +2.5v, transistor Q01 is on and Q02 is off, allowing Q03 to be on. The output is then at a logic "0" (-0.5v).

If the input voltage rises to about +3.5 volts, Q01 will turn off and Q02 goes on. This action removes the base drive to Q03, so it goes off and the output becomes a logic "1" (-3v).

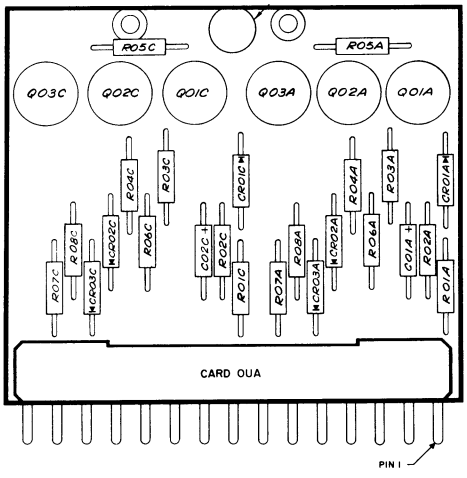
This card (at logic "0") will handle a load of 20 ma, but in this application is only approximately 3 ma.

SYMBOL




-20V
-20V
TP-A
R03A
1.2 K
R05A
1.8 K
R06A
18 K
R07A
4.7 K
CR03A
Q02A
2N3638
Q03A
2N3638
R08A
1.5 K
R01A
1.5K
CR01A
Q01A
2N3638
CR02A
C01A
1.0
±20%
R04A
4.7K
R02A
22K
+20V
-20V
-20V
TP-C
R03C
1.2 K
R05C
1.8 K
R06C
18K
R07C
4.7 K
CR03C
Q02C
2N3638
Q03C
2N3638
R08C
1.5 K
R01C
1.5K
CR01C
Q01C
2N3638
CR02C
C01C
1.0
±20%
R04C
4.7 K
R02C
22 K
+20V
-20V
+20V
13
14
15
1
6
7
12

OUA


R05C
R05A
Q03C
Q02C
Q01C
Q03A
Q02A
Q01A
CARD OUA
PIN 1

GATED PULSE SHAPER
OVA

The OVA circuit was designed to produce a nominal 210nsec, 1604 Logic Level pulse for each switchover of differential input level. The input is a differential 0.7 volt signal switching about a bias level of +8 volts provided by an EW- circuit. The OVA is designed for a maximum nominal input signal repetition rate of 1.25 megacycles. The output can be gated on or off with a logic level signal.

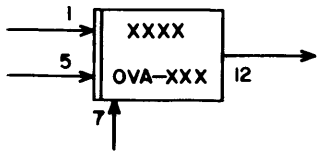
Pins 1 and 5 are the differential input pins with the output at pin 12. Pin 7 is the gate input.

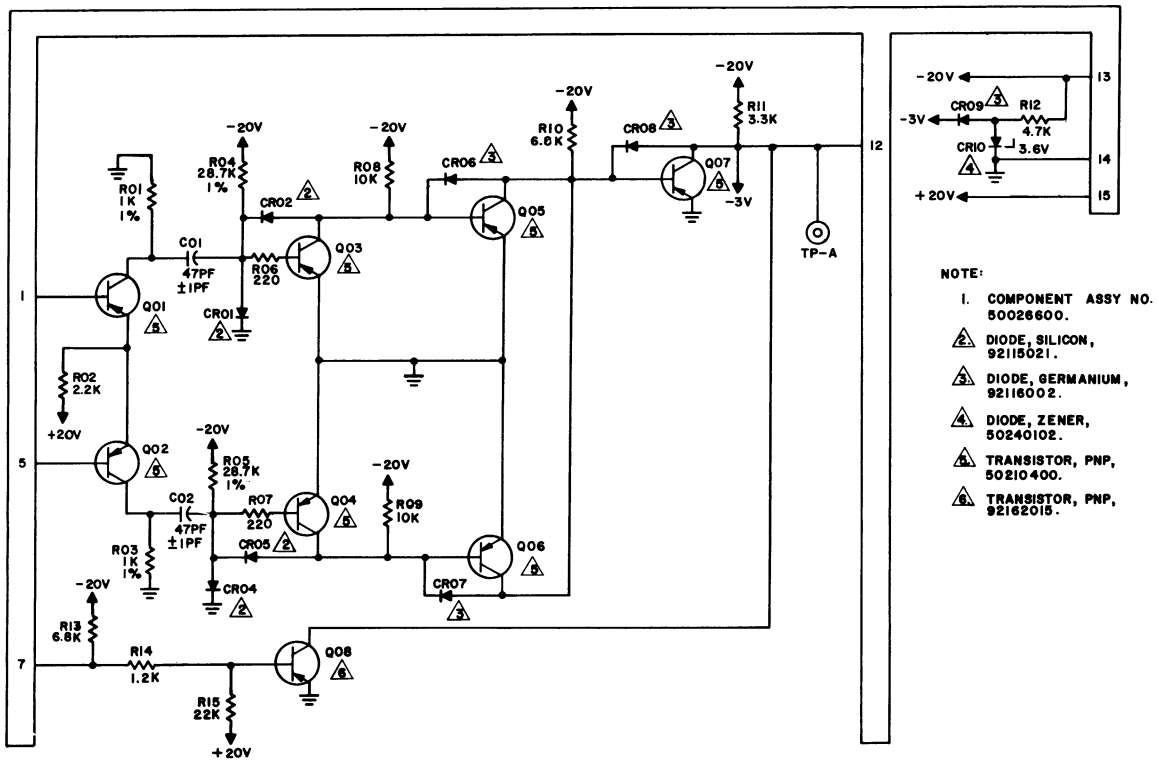
With an EW- Series card providing the signal and the bias for Q01 and Q02, the common emitters are held at approximately +9 volts. The transistor whose base is swinging negative (assume Q01) will be turning on while the other turns off. The collector of Q01 then goes positive to +5 volts (determined by emitter resistor value). This positive going transition is coupled by C01 into the base circuitry of Q03, turning it off. CR01 clamps the pulse height and C01, R01, and R04 determine the "off" time of Q03, and hence the pulse width appearing at the collector of Q03. The other side of the circuit (ie. Q02, Q04, etc.), functions in an identical manner to that described above. Q05 and Q06 then are simply inversions which are necessary to properly "or" these pulses to a common output via Q07. The pulse widths should be 210nsec $\pm$ 10%. When the output goes negative, it gets clamped to a -3.6 volt zener, which produces a better negative going transition than hold-down resistors.

CR06, CR07, and CR08 are germanium anti-saturation diodes. CR02 and CR05 are silicon anti-saturation diodes used in conjunction with R06 and R07 to keep Q03 and Q04 out of saturation.

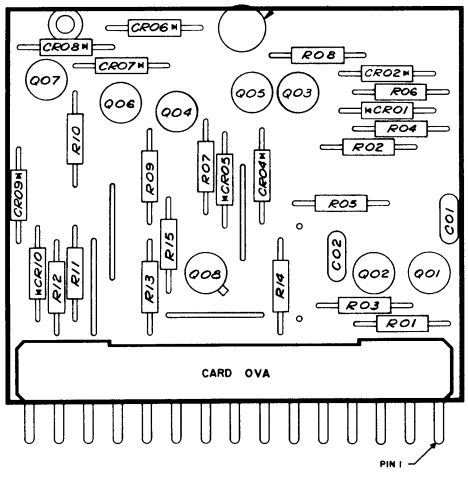
The output can be gated on or off by means of a logic signal into pin 7. A logical "1" (-3V) will turn Q08 on, which holds the output (pin 12) at a constant "0". A logical "0" (0V) input will turn Q08 off, permitting pulse output at pin 12.

SYMBOL




-20V
-3V
+20V
R01 1K 1%
R02 2.2K
R03 1K 1%
R04 28.7K 1%
R05 28.7K 1%
R06 220
R07 220
R08 10K
R09 10K
R10 6.8K
R11 3.3K
R12 4.7K
R13 6.8K
R14 1.2K
R15 22K
C01 47PF ±1PF
C02 47PF ±1PF
CR01
CR02
CR04
CR05
CR06
CR07
CR08
CR09
CR10 3.6V
Q01
Q02
Q03
Q04
Q05
Q06
Q07
Q08
TP-A
1
5
7
12
13
14
15
NOTE:
1. COMPONENT ASSY NO. 50026600.
2. DIODE, SILICON, 92115021.
3. DIODE, GERMANIUM, 92116002.
4. DIODE, ZENER, 50240102.
5. TRANSISTOR, PNP, 50210400.
6. TRANSISTOR, PNP, 92162015.

OVA


CR06 M
CR08 M
CR07 M
R08
CR02 M
R06
CR01 M
R04
R02
Q07
Q06
Q04
Q05
Q03
R10
R09
R07
CR05 M
CR04 M
CR09 M
R05
C01
C02
Q02
Q01
R15
R12
R11
R13
Q08
R14
R03
R01
CR10 M
CARD OVA
PIN 1

INPUT AMPLIFIER
OYA

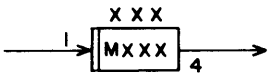
The input amplifier card OYA is used to interface between equipment operating with excursions of -12v to -1v and standard logic signals (0v to -3v).

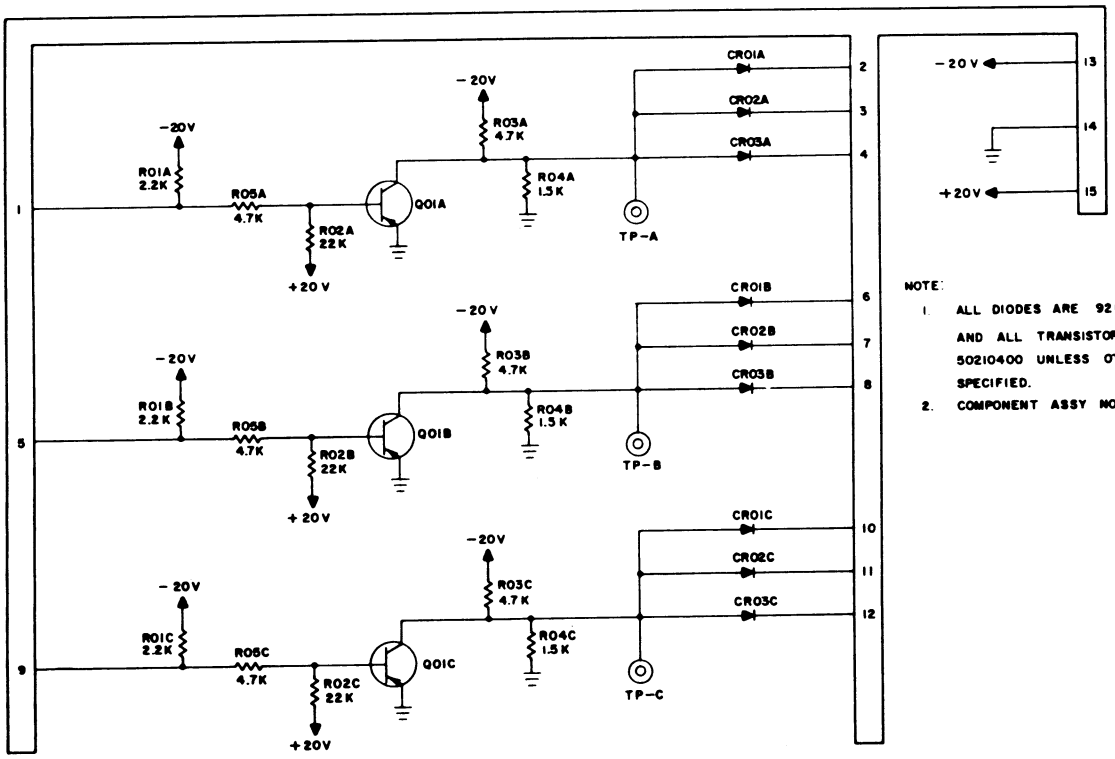
Each OYA card has three identical circuits. The circuit converts a -12v signal input to a "0" (-0.5v) logic signal output and a -1v signal input to a "1" (-3v) logic signal output.

With a -12v input, the emitter-base of Q01 will forward biased and Q01 will turn on. R05 is chosen so that Q01 will switch when the input signal is at a nominal -6v. Q01 is then in a saturated state capable of providing 12 ma at about -0.5v. With a -1v input, the emitter-base of Q01 will be back biased and Q01 will turn off. Voltage divider R03 and R04 then determine the "1" output voltage.

Each circuit represents a load of about 10 ma when the input is held to ground. The threshold point of the circuit is at -6v $\pm$ 1.5v. Output diodes CR01, CR02 and CR03 provide for AND terms if required.

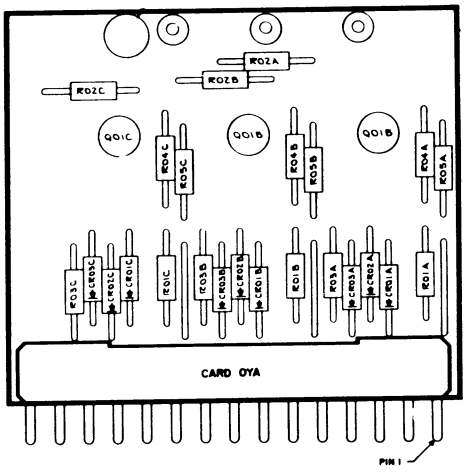
SYMBOL

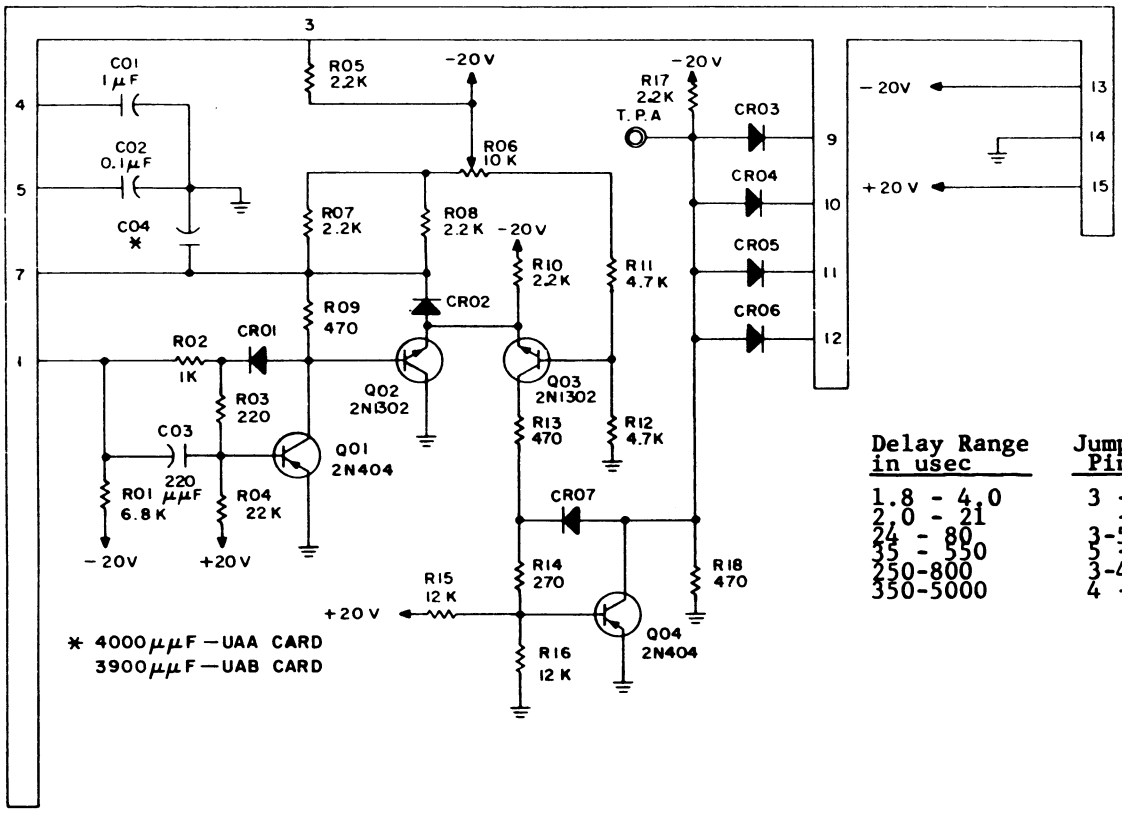




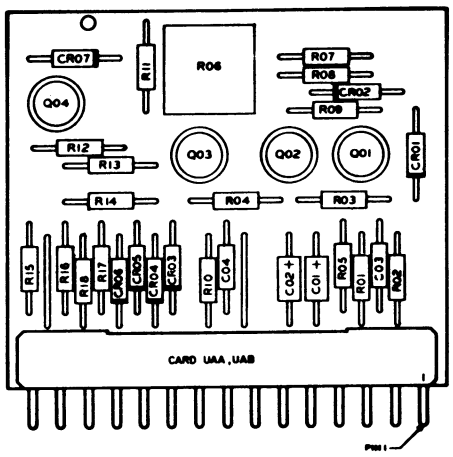
NOTE:

1. ALL DIODES ARE 92116002 AND ALL TRANSISTORS ARE 50210400 UNLESS OTHERWISE SPECIFIED.
2. COMPONENT ASSY NO. 50027500.





Delay Range in usec	Jumper Pin
1.8 - 4.0	3 - 7
2.0 - 21	-
24 - 80	3-5-7
35 - 550	5 - 7
250-800	3-4-7
350-5000	4 - 7



ADJUSTABLE DELAY

UAA, UAB

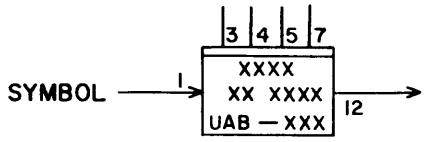
The adjustable delay circuit is noninverting in relation to the input but changes from "1" to "0" are delayed at the output.

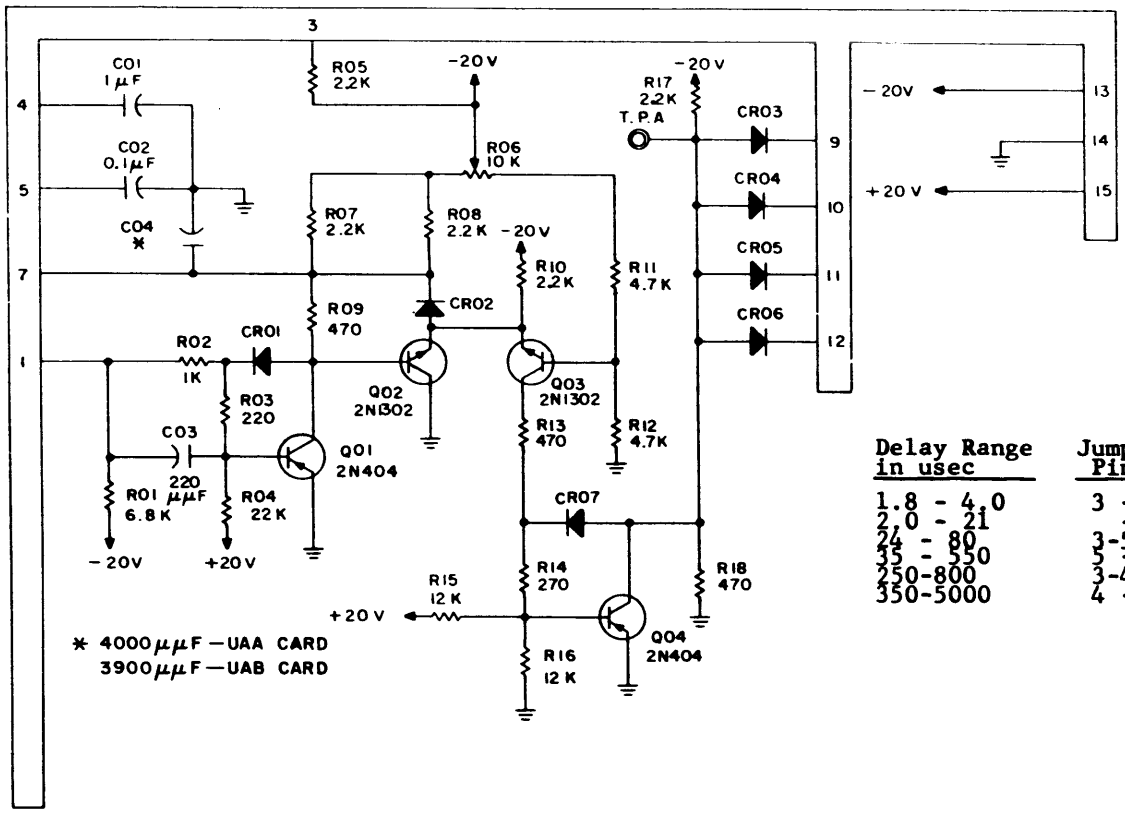
The input stage of the circuit is an inverting circuit with a speed-up diode (CR01) to reduce turnoff time in Q01. The timing circuit is composed of C04, R07, R08, and potentiometer R06. Longer range delays are obtained by paralleling C04 with C01 and/or C02 with external jumpers. A limited delay adjustment may be obtained by paralleling R05 with the charge network (R07, R08, and R06). Some external adjustment may also be obtained by connecting a potentiometer between pins 3 and 7. The UAB card has a temperature stable capacitor, C04, for delays below 25 usec.

Discharge of C04, which recycles the delay, is accomplished by the emitter follower (Q02) in the second stage through diode CR02. Drive to Q02 is determined by the drop across R09 which also provides a small percentage of the current to discharge C04. To provide 98% of the full delay period, a recycle time of 1 usec is required when using C04 alone, 2 usec when C02 is added, and 10 usec when C01 is added.

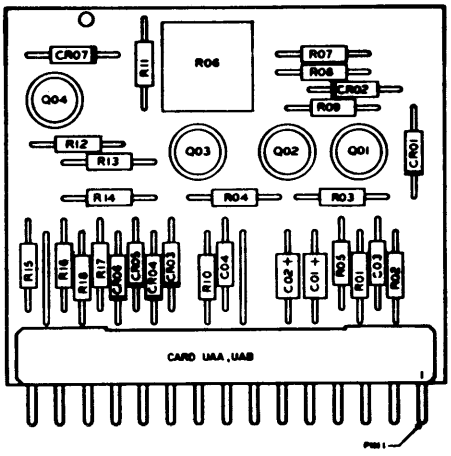
The third stage is emitter driven to obtain voltage gain and proper bias reference to switch the output stage. The base circuit reference is changed by connecting R06 as a voltage divider. As R06 inserts resistance to increase the RC time constant, it also removes resistance in the base divider of Q03. A greater portion of the RC time constant can be used for long delays. The normal adjustment range of 9 to 1 is extended to approximately 20 to 1.

The fourth and final stage, Q04, is an inverter circuit with a saturation limiting diode (CR07) which limits base drive. A divider circuit in the base allows considerable voltage swing to improve turnon time. The output excursions are limited in the negative direction by a resistance divider.





Delay Range in usec	Jumper Pin
1.8 - 4.0	3 - 7
2.0 - 21	-
24 - 80	3-5-7
35 - 350	5 - 7
250-800	3-4-7
350-5000	4 - 7



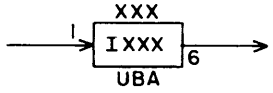
DOUBLE INVERTER

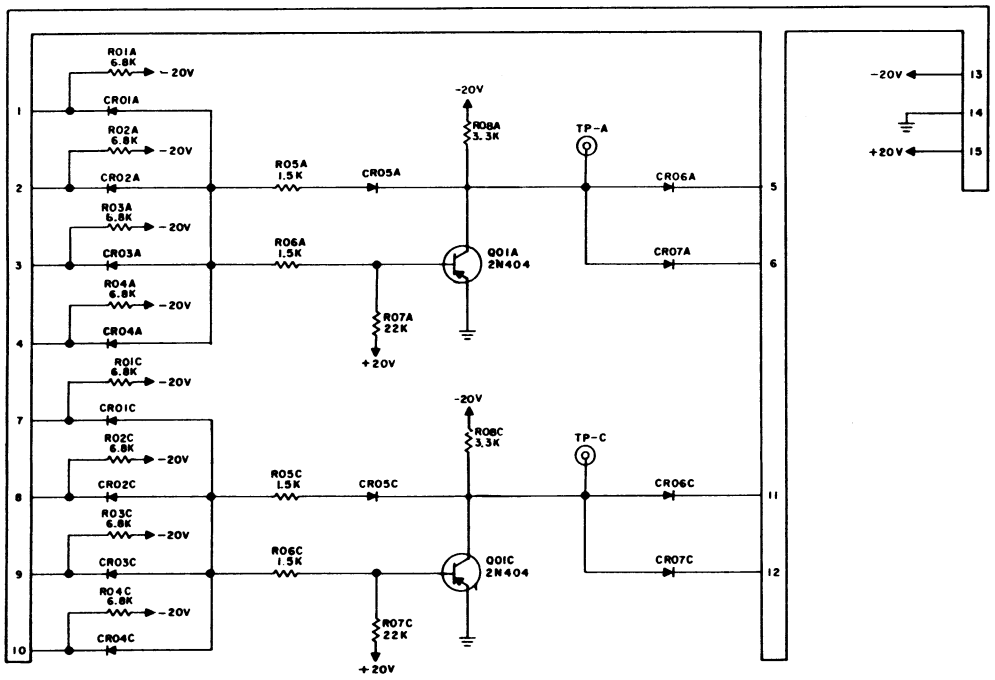
UBA

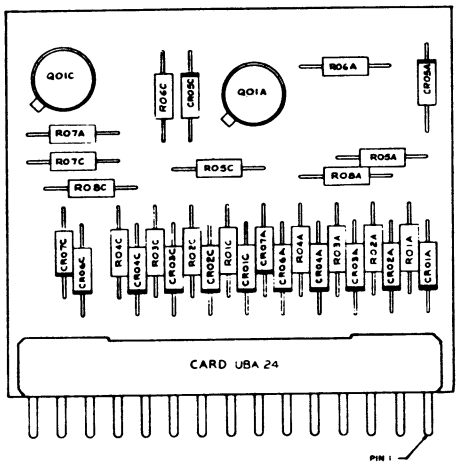
This inverter card was designed for use in the 180 Data Collector where speed requirements could be relaxed to favor low cost. Except for the number of input OR terms and output AND terms, it is the same basic circuit as Control Corporation cards CC-21, CC-22, and CC-23.

Since the newer Computer Division 24A card now closely approaches the cost of the UBA card, the UBA is no longer recommended for new designs in the interest of reducing the number of card types to be handled from a logistics standpoint in production and in the field.

SYMBOL




R01A 6.8K
-20V
CR01A
R02A 6.8K
CR02A
R03A 6.8K
CR03A
R04A 6.8K
CR04A
R01C 6.8K
CR01C
R02C 6.8K
CR02C
R03C 6.8K
CR03C
R04C 6.8K
CR04C
R05A 1.5K
CR05A
R06A 1.5K
R07A 22K
+20V
R08A 3.3K
Q01A 2N404
TP-A
CR06A
CR07A
R05C 1.5K
CR05C
R06C 1.5K
R07C 22K
R08C 3.3K
Q01C 2N404
TP-C
CR06C
CR07C
1
2
3
4
7
8
9
10
5
6
11
12
13
14
15


Q01C
Q01A
R06A
CR08A
R07A
R07C
R08C
R05C
R05A
R08A
CARD UBA 24
PIN 1

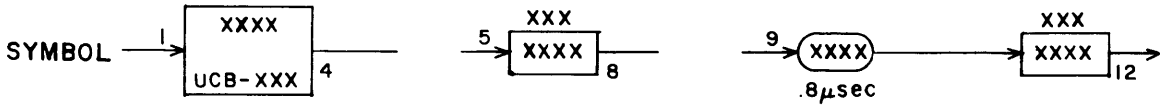
ADJUSTABLE PULSE DELAY
UCB

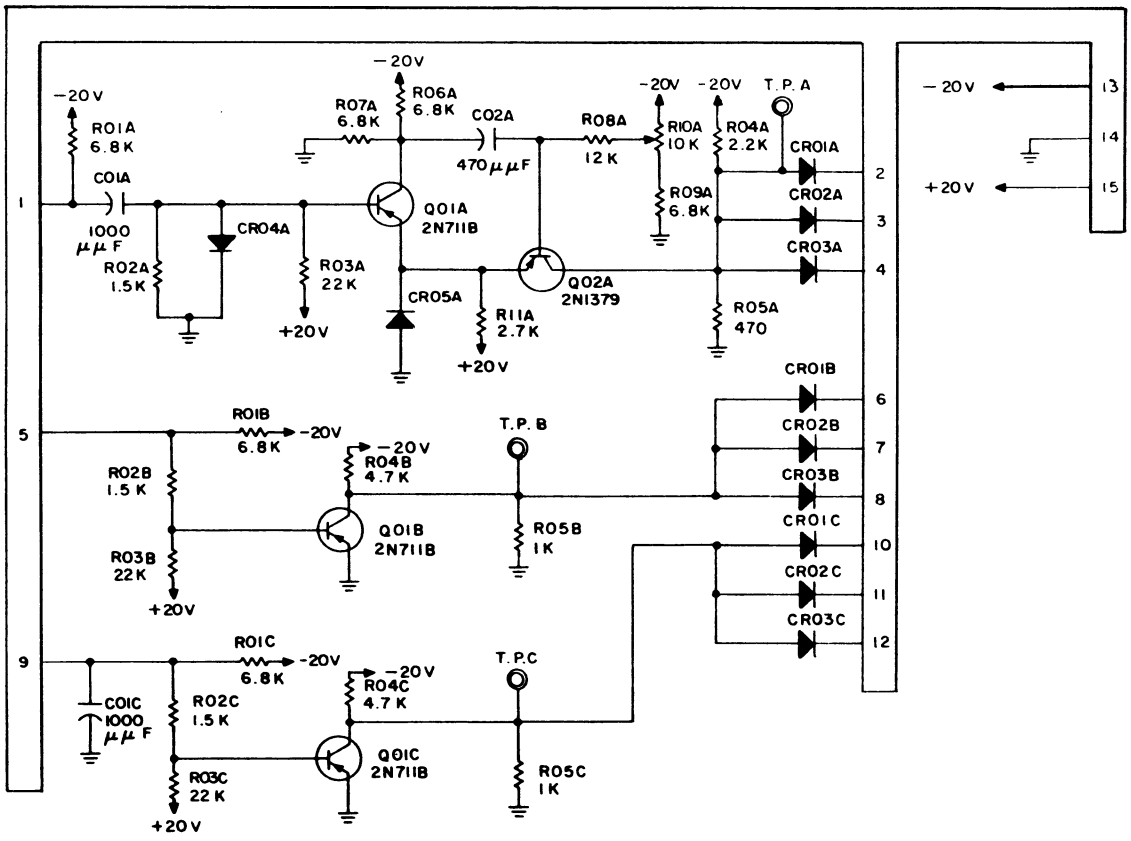
The pulse delay card is used as a read and write skew adjustment which compensates for mechanical misalignment of head gaps and small switching delays or phase lags in the electronic amplifiers. The card produces a narrow output pulse after a short adjustable delay (1 3/4 - 5 usec). A recycle time of 5 usec is necessary for delays to equal 95% of the specified delay period.

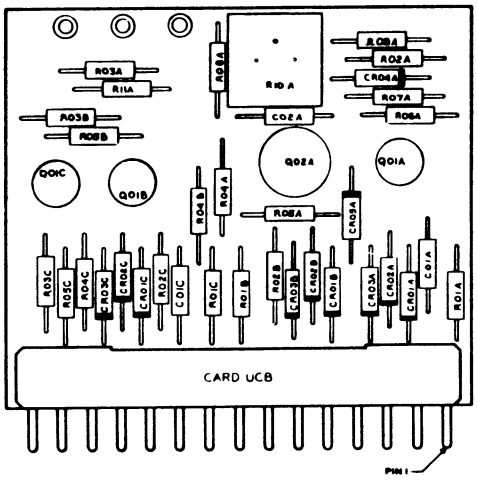
The circuit is divided into three sections. Circuit A is a one-shot multivibrator circuit composed of transistors Q01A and Q02A. The multivibrator is triggered by a negative input signal passing through a differentiating network to the base of Q01A. Conduction of Q01A couples a positive pulse to the base of Q02A and causes it to switch off. Multivibrator regeneration is completed by the common emitter resistor R11A. The period of the multivibrator is determined by R08A, C02A, and the resistance of potentiometer R10A. Recycle time is determined by resistors R06A and R07A and capacitor C02A. Transistor Q02A is a high-gain transistor which provides reserve output current for the limited base drive available in the circuit. Diode CR05A supplies the additional emitter current necessary for the collector load of Q02A, and references the emitter to near ground for this stable state of the multivibrator. During the multivibrator period, CR05A is reverse biased, permitting the gain of the two transistors to be utilized through a common emitter resistance (R11A) providing fast fall and rise times.

Circuits B and C are simplified inverter circuits which use a high-frequency transistor to decrease switching time. Circuit C also uses a delay capacitor C01C which allows the positive output to be delayed permitting ANDing with the output of circuit B for a 3/4-usec pulse output.

The three circuits are not connected internally and may be used as separate and complete elements. The circuits may also be connected through external jumpers to provide a delay output pulse from a negative input.




-20V
R01A 6.8K
C01A 1000 μμF
R02A 1.5K
CR04A
R03A 22K
+20V
R07A 6.8K
R06A 6.8K
C02A 470μμF
Q01A 2N711B
CR05A
R11A 2.7K
+20V
R08A 12K
Q02A 2N1379
R10A 10K
R09A 6.8K
R04A 2.2K
T.P. A
CR01A
CR02A
CR03A
R05A 470
-20V
13
14
+20V
15
1
2
3
4
R01B 6.8K
R02B 1.5K
R03B 22K
+20V
R04B 4.7K
Q01B 2N711B
T.P. B
R05B 1K
CR01B
CR02B
CR03B
CR01C
CR02C
CR03C
5
6
7
8
10
11
12
R01C 6.8K
C01C 1000 μμF
R02C 1.5K
R03C 22K
+20V
R04C 4.7K
Q01C 2N711B
T.P.C
R05C 1K
9

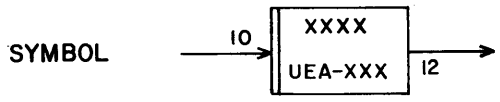

CARD UCB
PIN 1

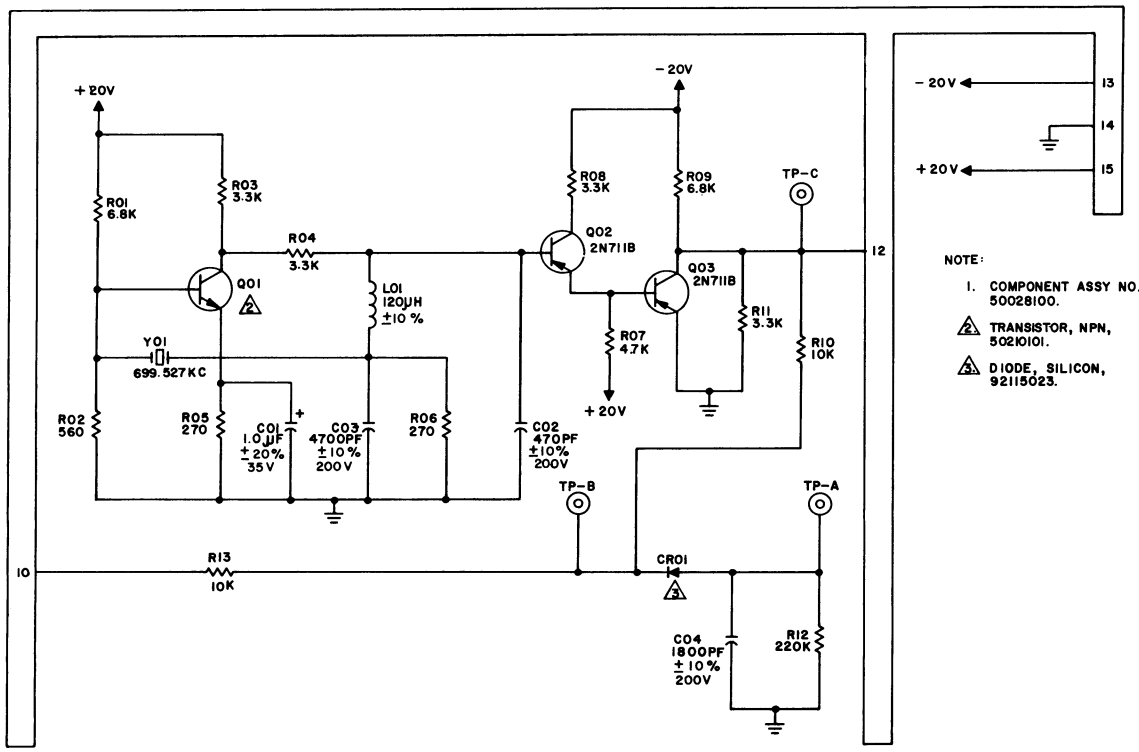
OSCILLATOR CALIBRATOR
UEA

The UEA card was designed to be used for routine maintenance on the 852 Disk Pack, to check the frequency of the IVA oscillator cards. Q01, Y01, L01, C02, C03 etc., comprise a crystal-controlled oscillator set to 699.527 Kc. Q02 and Q03 comprise a buffer amplifier to isolate the load from the oscillator, and to shape the oscillations into standard logic pulses. The output from Q03 is logic pulses at 699.527 kc repetition rate. This output appears at pin 12. It is also fed through R10 to the mixing network made up of R12, C04 and CR01. The IVA output enters pin 10 and goes through R13 to the mixing network. The sum of the two signals is seen at TP-B, and the difference (beat frequency) can be observed at TP-A.

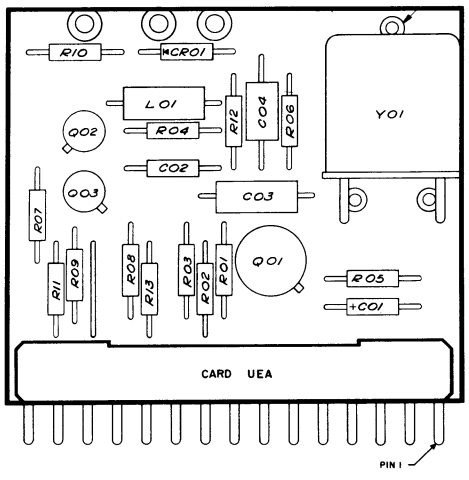
If the signal seen at TP-A is a 1Kc frequency, this indicates that the IVA signal fed in on pin 10 is either 1KC above, or 1KC below the frequency of the Q01 crystal-controlled oscillator. To tune in the IVA, it should be adjusted so the frequency seen at TP-A decreases to as near zero cycles per second as possible.

The main output is the difference in frequency between the internal oscillator and the oscillator signal fed in on pin 10.




+20V
-20V
R01 6.8K
R03 3.3K
R04 3.3K
R08 3.3K
R09 6.8K
TP-C
Q01
Q02 2N7118
Q03 2N7118
L01 120μH ±10%
Y01 699.527KC
R07 4.7K
R11 3.3K
R10 10K
R02 560
R05 270
C01 1.0μF ±20% 35V
C03 4700PF ±10% 200V
R06 270
C02 470PF ±10% 200V
TP-B
TP-A
10
R13 10K
CR01
C04 1800PF ±10% 200V
R12 220K
12
13
14
15
NOTE:
1. COMPONENT ASSY NO. 50028100.
2. TRANSISTOR, NPN, 50210101.
3. DIODE, SILICON, 92115023.

UEA


R10
CR01
L01
R04
R12
C04
R06
Y01
Q02
C02
Q03
C03
R07
Q01
R11
R09
R08
R13
R03
R02
R01
R05
C01
CARD UEA
PIN 1

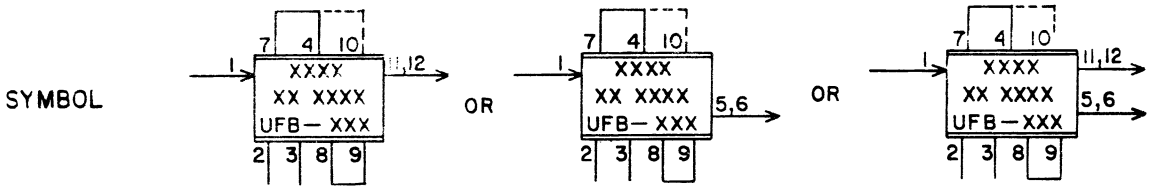
VOLTAGE CONTROLLED DELAY

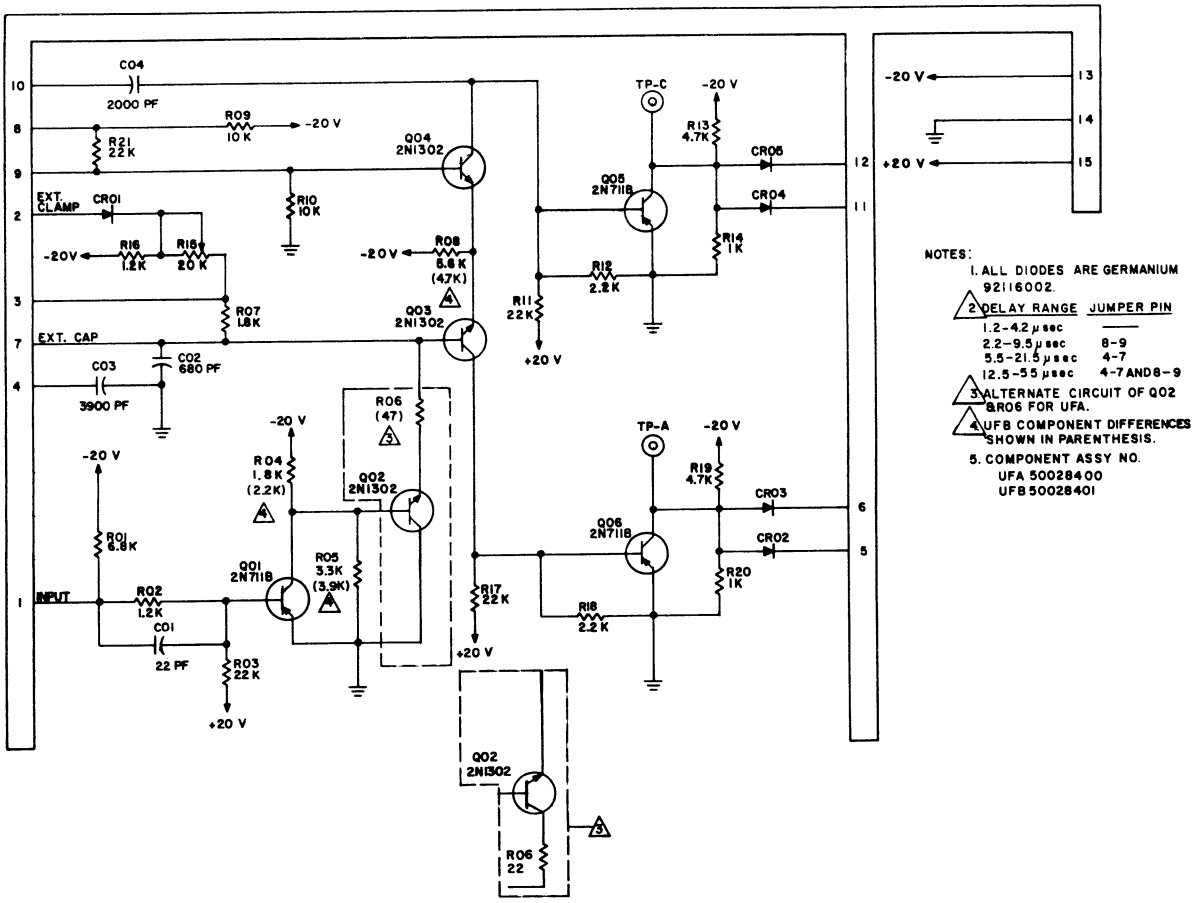
UFA, UFB

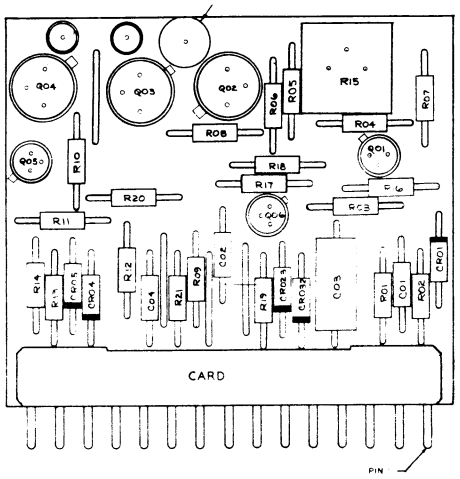
The voltage controlled delay circuit provides several options in delay duration and in the type of output signal desired at the end of the delay timeout by the use of external jumpers. It may have its delay controlled remotely by an analog d-c voltage in applications such as remote read and write deskew. It is also possible to use the circuit as a voltage comparator over a limited range.

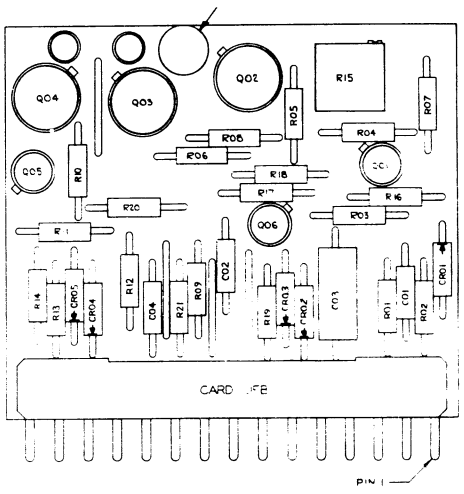
The delay period is armed by having a "1" input on pin 1 for 0.5 usec or more for delay capacitors up to 5000 pf total. While armed and during the delay period, the output of circuit A (pins 5 and 6) is a "0" and the output of circuit C (pins11 and 12) is a "1". The delay period is initiated by an input on pin 1 going from a "1" to a "0". The input must remain a "0" during the delay period, or the delay rearms and does not time out. When the delay period times out, the output of circuit A goes to a "1" and the output of circuit C goes to a "0". Grounding pin 10 delays the output of circuit C going to a "0" for 1 to 3 usec. Thus a "1" coincidence at the end of the delay may be obtained by ANDing one diode from each of the two outputs. For delays below 10 usec, where the optional capacitor on pin 4 is not used in the delay circuit, pin 10 may be connected to pin 4 and reduce the "1" coincidence by 30% or more. Other external capacitors can be used instead; but care should be exercised with external capacitors or the "1" coincidence may go to zero, particularly when the voltage on pin 9 is less than -8v. Long delays cannot reliably utilize the "1" coincidence feature of this circuit.

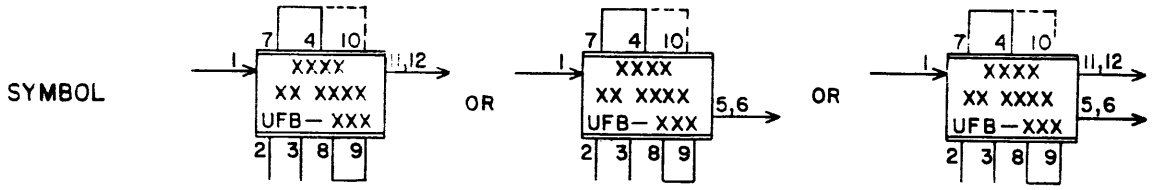
Q01 and Q02 form an inverter-emitter follower combination for discharging C02 (and any other capacitors connected to pin 7). Q03 and Q04 act as a differential comparison amplifier and switch close to the point at which pins 7 and 9 have equal voltage. This determines the timeout period which switches output circuits A and C. The RC timeout period is controlled by several factors, nearly all of which are accessible to output pins for optional timing periods. Pin 7 allows external capacitors to be added for a coarse step adjustment. Pin 2 may be used to clamp the voltage (usually about -10v) used in the RC charge circuit. Pin 3 permits some of the charge resistance to be shorted out; however, care should be taken to make sure the maximum current in potentiometer R15

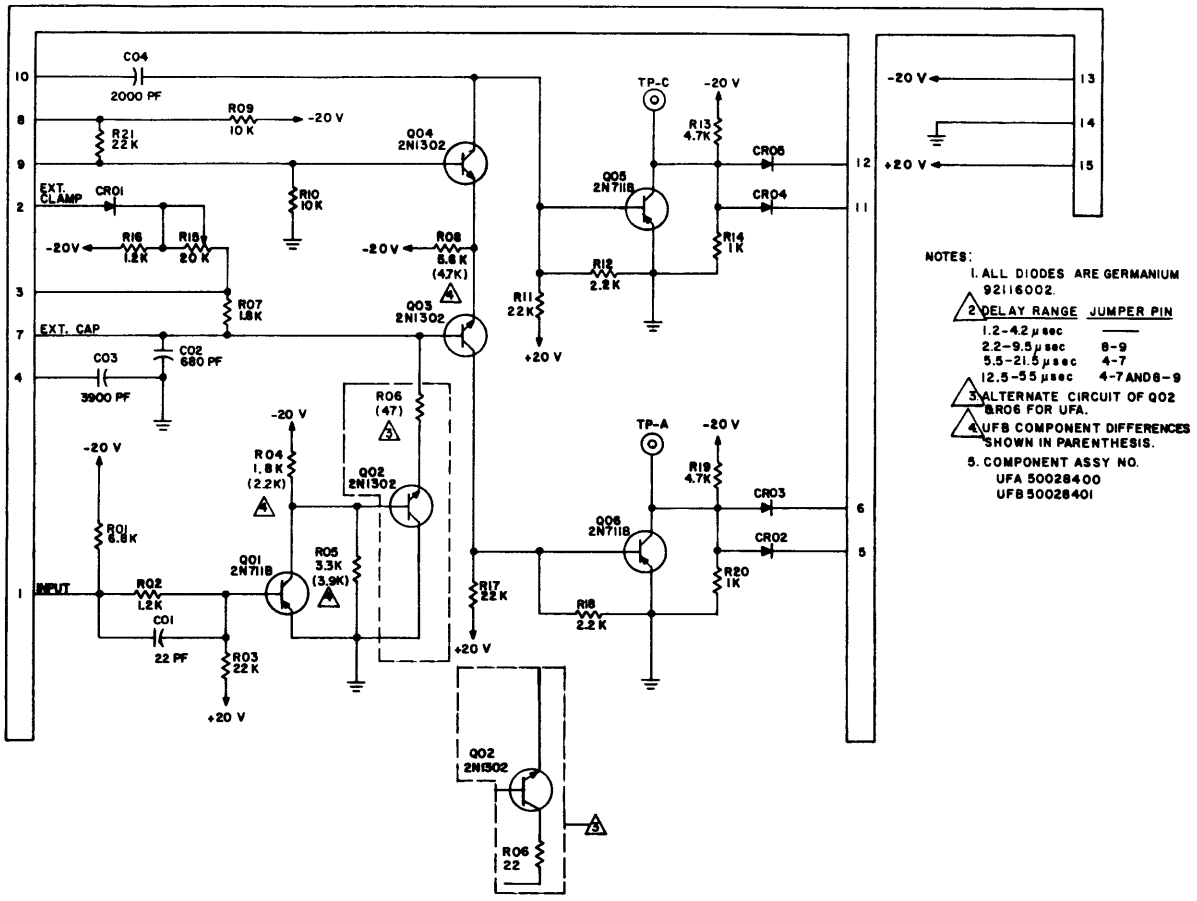

SYMBOL
7 4 10
1
XXXX
XX XXXX
UFB— XXX
11,12
2 3 8 9
OR
5,6
OR

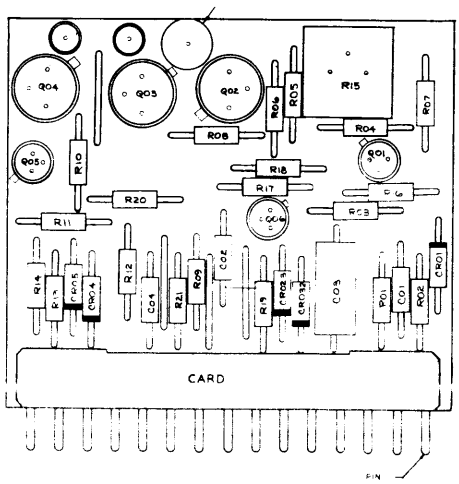

C04
2000 PF
R09
10 K
-20 V
R21
22 K
Q04
2N1302
EXT.
CLAMP
CR01
R10
10 K
-20V
R16
1.2K
R15
20 K
R08
5.6 K
(4.7K)
R07
1.8K
EXT. CAP
C02
680 PF
C03
3900 PF
R06
(47)
R04
1.8 K
(2.2K)
Q02
2N1302
R01
6.8K
INPUT
R02
1.2K
C01
22 PF
R03
22K
+20 V
Q01
2N7118
R05
3.3K
(3.9K)
R17
22K
R11
22K
Q03
2N1302
TP-C
R13
4.7K
CR05
CR04
Q05
2N7118
R12
2.2K
R14
1K
TP-A
R19
4.7K
CR03
CR02
Q06
2N7118
R20
1K
R18
2.2K
R06
22
-20 V
+20 V
NOTES:
1. ALL DIODES ARE GERMANIUM 92116002.
2 DELAY RANGE JUMPER PIN
1.2-4.2 μsec —
2.2-9.5 μsec 8-9
5.5-21.5 μsec 4-7
12.5-55 μsec 4-7 AND 8-9
3 ALTERNATE CIRCUIT OF Q02 & R06 FOR UFA.
4 UFB COMPONENT DIFFERENCES SHOWN IN PARENTHESIS.
5. COMPONENT ASSY NO.
UFA 50028400
UFB 50028401

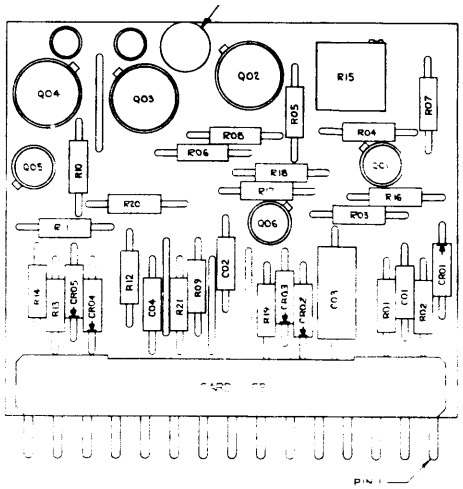

CARD
PIN 1


CARD UFB
PIN 1


SYMBOL
7 4 10
1
XXXX
XX XXXX
UFB-XXX
11,12
2 3 8 9
OR
5,6
OR


C04
2000 PF
R09
10 K
-20 V
R21
22 K
Q04
2N1302
TP-C
R13
4.7K
CR06
CR04
Q05
2N7118
R14
1K
R12
2.2K
R11
22K
+20 V
EXT. CLAMP
CR01
R16
1.2K
R15
20 K
R10
10K
R08
5.6K
(4.7K)
R07
1.8K
Q03
2N1302
EXT. CAP
C03
3900 PF
C02
680 PF
R06
(47)
R04
1.8K
(2.2K)
Q02
2N1302
TP-A
R19
4.7K
CR03
CR02
Q06
2N7118
R20
1K
R18
2.2K
R01
6.8K
INPUT
R02
1.2K
Q01
2N7118
R05
3.3K
(3.9K)
R17
22K
C01
22 PF
R03
22K
Q02
2N1302
R06
22
-20 V
+20 V
NOTES:
1. ALL DIODES ARE GERMANIUM 92116002.
2. DELAY RANGE JUMPER PIN
1.2-4.2 μsec —
2.2-9.5 μsec 8-9
5.5-21.5 μsec 4-7
12.5-55 μsec 4-7 AND 8-9
3. ALTERNATE CIRCUIT OF Q02 & R06 FOR UFA.
4. UFB COMPONENT DIFFERENCES SHOWN IN PARENTHESIS.
5. COMPONENT ASSY NO.
UFA 50028400
UFB 50028401


CARD



VOLTAGE CONTROLLED PULSE DELAY

UGA

The voltage controlled pulse delay circuit is used for read and write deskew adjustment in magnetic tape units or in similar functions where a narrow pulse (0.25 - 0.75 usec) is desired at the end of the delay period. It is also useful where optional delays are to be gated into a circuit without requiring the hardware of a complete delay circuit. The UGA card performs a function similar to the UCB pulse delay card with the following differences:

1) Shorter recycle time.

2) Increased range of delay with optional ranges available.

3) Provisions for logically selecting different delays in a given range by gating in different d-c voltages.

4) Output pulse shaping is internally wired.

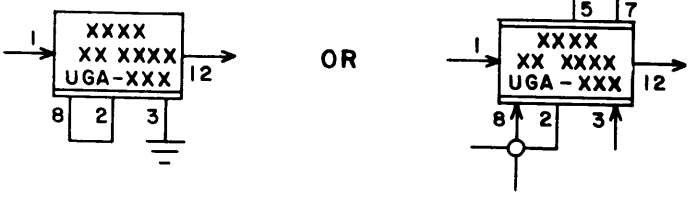
5) Input pulse width must be less than the duration of the delay.

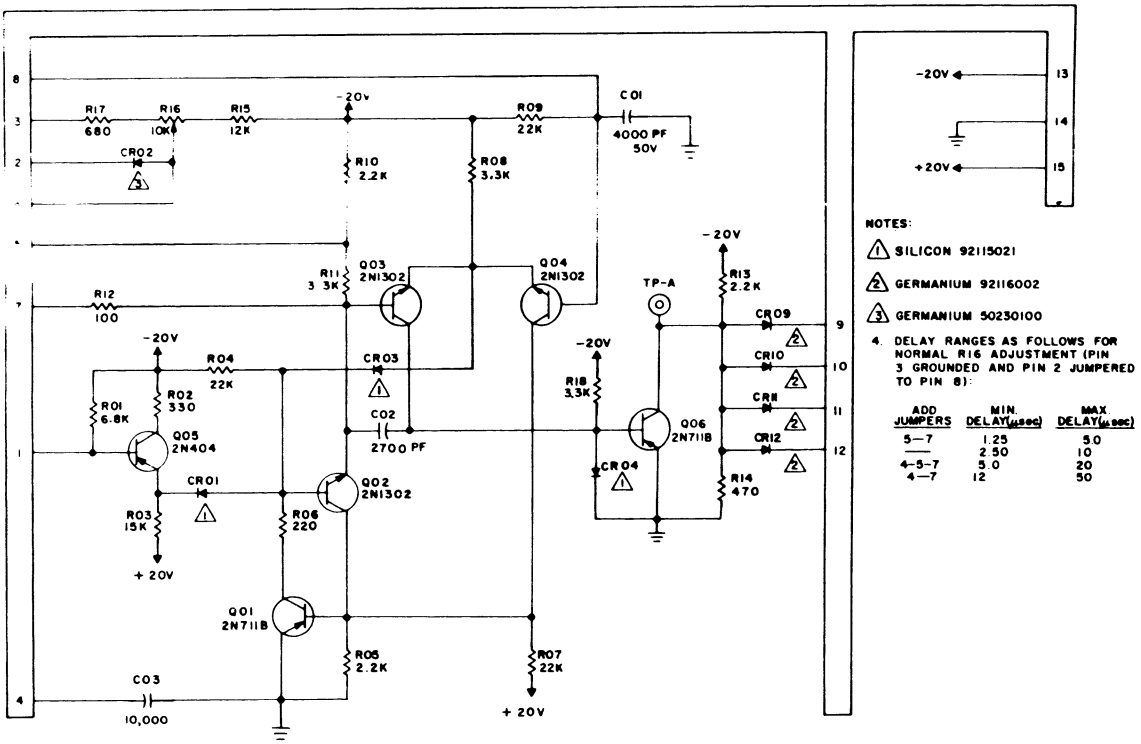
Transistors Q01 and Q02 are connected in a bistable circuit which is equivalent to that of a SCR with turnoff provisions. Q03 and Q04 act as a differential amplifier for comparing voltages on their input bases. Q06 converts the end of the delay time period to standard logic element levels. Q05 provides turnoff of the Q01, Q02 bistable circuit.

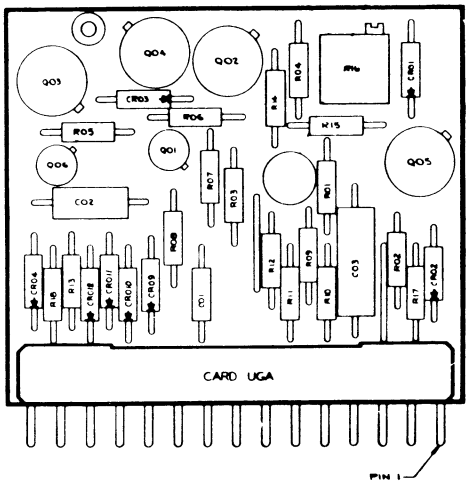
The delay period is initiated by a logical "1" pulse on Q05 (pin 1). If the previous delay period has been completed, both Q01 and Q02 would have been in a stable-on condition and pin 7 would be a fraction of a volt negative. Q05 drives the base of Q02 more negative than its emitter (pin 7) which turns Q02 off. The turnoff of Q02 results in Q01 also losing its base drive and turning off, thereby causing Q01 and Q02 to assume a stable-off condition. C02 and any additional external capacitor connected to pin 7 then charge negative through R10 and R11 with the voltage at emitter of Q03 following this charge curve. When the emitter voltage at Q03 and Q04 becomes slightly negative relative to the voltage on the base of Q04 (obtained from external connections to pin 8), then Q03 begins to turn off and Q04 starts to turn on. The collector current of Q04 then causes Q01 to be turned on. The turnon of Q01 also drives Q02 on

and Q02 continues to maintain base drive for Q01. Capacitor C02, and any external capacitors, are discharged to ground by the stable-on condition of Q01 and Q02. The discharge return current of C02 is supplied primarily by CR04 as long as the voltage at the base of Q06 is sufficiently positive for CR04 to conduct. As voltage drops below the forward conducting threshold of CR04, current from R18 and from R08 through Q03 drives the return point of C02 in a negative direction until clamped by the turn-on base to emitter voltage of Q06. Thus the time it requires for the return of C02 to re-establis its normal voltage determines the time Q06 is off and hence the "1" output pulse width. Because of the large turnon gain of the Q01, Q02 combination, the pulse width is determined almost wholly by the values of R08, R18, and C02. The use of R12 with externally added capacitors reduces the peak discharge current of the external capacitor sufficiently to maintain the output pulse width over delay ranges up to 10 sec. R12 also protects Q01 and Q02 from overload failure. As soon as C02 and any externally connected capacitors are discharged by Q01, Q02, the circuit is ready for the next delay. If an input pulse to initiate a delay comes during the previous delay period, it is ignored since Q01, Q02 are already turned off.

SYMBOL




-20V
13
14
+20V
15
R17 680
R16 10K
R15 12K
CR02
R10 2.2K
R09 2.2K
C01 4000 PF 50V
R08 3.3K
Q03 2N1302
R11 3.3K
Q04 2N1302
TP-A
R13 2.2K
R12 100
CR09
CR10
CR11
CR12
R04 22K
CR03
R18 3.3K
Q06 2N7118
R01 6.8K
R02 330
Q05 2N404
C02 2700 PF
CR04
R14 470
CR01
Q02 2N1302
R03 15K
R06 220
+20V
Q01 2N7118
R05 2.2K
R07 22K
C03 10,000
+20V
NOTES:
1. SILICON 92115021
2. GERMANIUM 92116002
3. GERMANIUM 50230100
4. DELAY RANGES AS FOLLOWS FOR NORMAL R16 ADJUSTMENT (PIN 3 GROUNDED AND PIN 2 JUMPERED TO PIN 8):
ADD JUMPERS | MIN. DELAY(μsec) | MAX. DELAY(μsec)
5—7 | 1.25 | 5.0
— | 2.50 | 10
4-5-7 | 5.0 | 20
4—7 | 12 | 50


Q04
Q02
Q03
CR03
R04
CR01
R06
R05
Q01
Q05
Q06
R07
R03
R01
C02
R08
R12
R09
C03
R02
R11
R10
R17
CR02
CR04
R16
R13
CR08
CR07
CR10
CR09
C01
CARD UGA
PIN 1

ADJUSTABLE SHORT TERM DELAY
UHB

The UHB is a one shot multivibrator which produces a logical "1" output for a logical "1" input. The output pulse width is variable between 0.1usec and 1.1usec and is independent of input pulse width.

This card is used in conjunction with the UIA pulse shaper card, to produce a highly accurate, narrow strobe pulse which gates information into a storage flip-flop (FAA).

In the stable state Q03 is conducting, Q01 is off, and C02 is charged to the voltage at the collector of Q01. A negative "1" pulse appearing at the input initiates the one shot. Q01 turns on. The base of Q03 goes positive by an amount equal to the initial voltage charge on the capacitor, thus turning Q03 off. The capacitor then discharges through the series resistance R14 and R09 to the -15v zener voltage on the center tap of R09. As the capacitor discharges through zero volts, Q03 turns on and the pulse is completed.

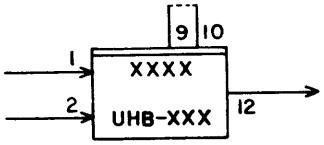
R09 not only adjusts the RC time constant, but also adjust the initial capacitor voltage which is determined by the divider R05 and R06 in series with R09. This tends to decrease the range of current that turns on Q03 and thus, minimize the change in fall time over the delay range.

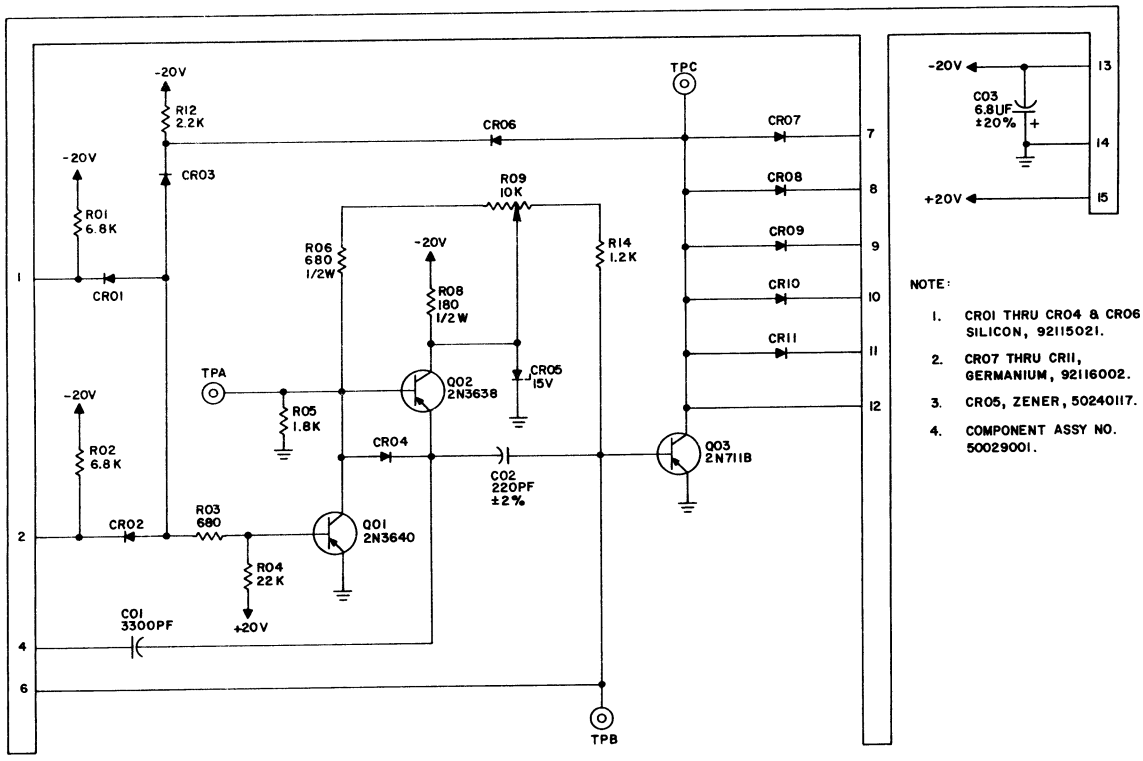
CR03 is coupled back to the input to form an "or" circuit and stabilize the output for changes in input pulse width. CR06 serves to isolate the input from the output circuit.

Test Specifications

	C02	C01 (Pin 9 Jumpered to Pin 10)
Typical Min Width	100 NSec	220 NSec
Typical Max Width	1.1 usec	17 usec
Typical Max Delay @ 50% PT	30 NSec	30 NSec
Typical Max Rise Time	30 NSec	30 NSec
Typical Max Fall Time	30 NSec	425 NSec
Typical Max Recycle Time	350 NSec	655 NSec
Typical Max Delay Change for $\Delta T = 30°C$	0.1% @1.2 usec	2.2% @ 18 usec

SYMBOL

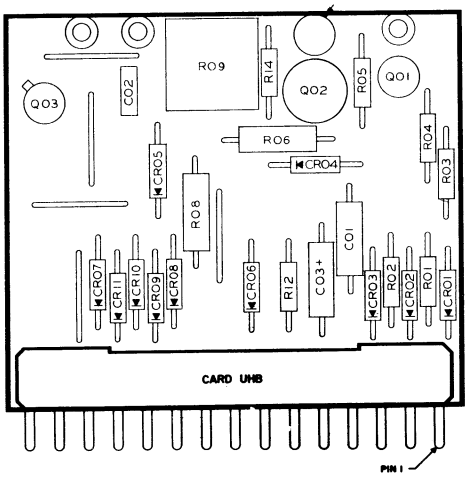




NOTE:

1. CR01 THRU CR04 & CR06, SILICON, 92115021.
2. CR07 THRU CR11, GERMANIUM, 92116002.
3. CR05, ZENER, 50240117.
4. COMPONENT ASSY NO. 50029001.

UHB



PULSE SHAPER
UIA

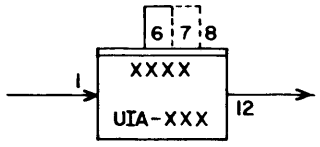
The UIA is used in conjunction with the UHB to produce a highly accurate, very narrow strobe pulse for gating information into the FAA card in the disc file.

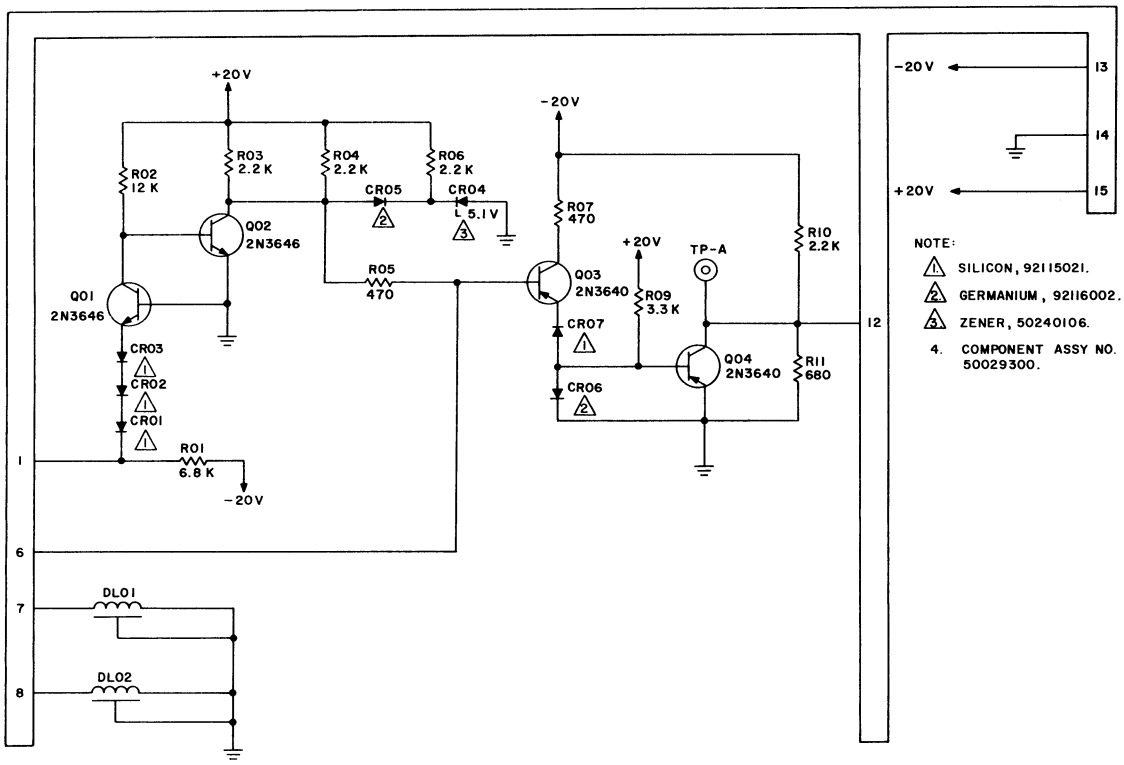
The UIA shapes a logical "0" pulse on the positive going edge of a logical "1" input pulse. The positive going edge at Pin 1 is transmitted through Q01 and turns on Q02. The negative going step voltage at the collector of Q02 propagates down the delay line and is inverted at the short circuit termination. This inversion propagates up the delay line and returns the collector of Q01 to 0 volts, producing a negative pulse equal to twice the value of the delay line at the base of emitter follower Q03. This negative "1" pulse is inverted by Q04 into positive going logical "0" pulse.

In like manner a negative going edge at Pin 1 produces a positive step at the collector of Q02. This is converted by the delay line into a positive pulse which keeps Q03 and thus Q04 in the off state. This positive pulse must time out before the negative pulse occurs or the pulse width will be affected. Therefore, to insure satisfactory operation the input pulse width and the recycle time must be greater than the output pulse width.

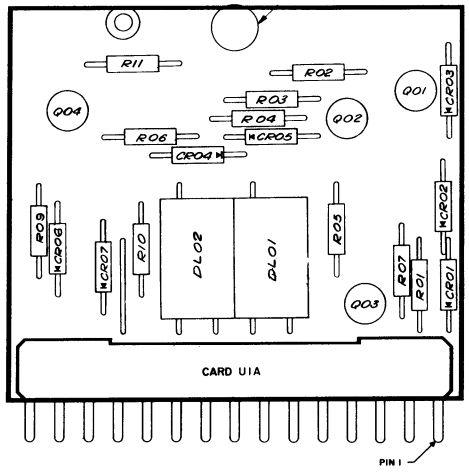
		DL_1 (30us)	DL_2 (100us)
Typical	Pulse Amplitude	4.8v	4.8v
Typical	Rise Time	20 nsec	20 nsec
Typical	Fall Time	40 nsec	70 nsec
Typical	Delay from Input @ 50% pt	60 nsec	60 nsec
Typical	Pulse Width @ - 1.5 v Pt.	80 nsec	230 nsec

SYMBOL




+20V
-20V
R02 12 K
R03 2.2 K
R04 2.2 K
R06 2.2 K
CR05
CR04 5.1V
R07 470
R10 2.2 K
Q02 2N3646
Q01 2N3646
R05 470
Q03 2N3640
R09 3.3 K
TP-A
CR07
CR03
CR02
CR01
Q04 2N3640
R11 680
CR06
R01 6.8 K
DL01
DL02
1
6
7
8
12
13
14
15
NOTE:
1. SILICON, 92115021.
2. GERMANIUM, 92116002.
3. ZENER, 50240106.
4. COMPONENT ASSY NO. 50029300.

UIA


R11
R02
R03
R04
R06
CR05
CR04
Q04
Q02
Q01
CR03
R09
CR09
CR07
R10
DL02
DL01
R05
R07
R01
CR02
CR01
Q03
CARD UIA
PIN 1

ADJUSTABLE LONG TERM DELAY
UJB, UJC

The long delay card is used for applications requiring a long delay that can be adjusted to a given value more accurately than the OJB circuit. This card differs from the OJB card in that the input on pin 1 is standard logic levels (-0.5v and -3v). Also, an input can be applied to pin 3 from either an output card, or a set of contacts. For details refer to the description of the OJB circuit.

There are two outputs on the UJB card; one inverting and one non-inverting (refer to figure 1). These are standard logic levels of -0.5 and -3 volts. The delay is initiated on the logical "0" edge of the input signal.

Delays from 400 usec to 60 sec (100 sec for UJC) are possible by means of jumper options and a potentiometer adjustment. Tables 1 and 2 show the ranges that can be covered by adjusting R07 for a given set of jumper conditions.

An alternate presentation of the delays available is shown in figure 2. Line #1 represents a timing circuit capacitance of 0.22 uf and is read horizontally. The distance between the diagonal lines labeled for a given set of jumper conditions at the intersection with line #1 is the minimum potentiometer range. Line #2 is for a circuit capacitance of 22.22 uf.

Note in figure 2 that in the 400 usec to 60 sec (100 sec for UJC) range of the circuit there exist two gaps; one of 4 msec between 4 and 8 msec, and one of 1 sec between 8 and 9 sec. These gaps can be filled by using an external capacitor between pins 4 and 8.

Referring to the schematic, note that the circuit contains three inverter stages (Q01, Q02, and Q07). There is also the timer composed of Q03, Q04, C01 (or C01 in parallel with C02), R07, R09 (or parallel combinations with R08 and R15), and the unijunction transistor Q05. SCR Q06 is used to provide a bistable device to latch-up the output. Diode CR05 is used to regulate the voltage to the timing and latching circuit, so the time delay is not effected by $\pm$20% power supply changes.

With a -3v input at pin 1 (see figure 1) Q01 will be on, so no voltage is supplied to the timer. Transistor Q02 will then be off, so its

collector voltage is -3v. Since this is also applied to the base of the output inverter Q07 it will be on, grounding the A output.

If the input at pin 1 goes to -0.5v, Q01 goes off allowing the voltage to the timer to rise to the zener voltage. A constant current generator (Q04) supplies a charging current to the timing capacitor (C01). The amount of current is determined by potentiometer R07 and the combinations of R08, R09, and R15. When the timing capacitor reaches approximately 6v with polarity as shown on the schematic, Q05 becomes regenerative and conducts from emitter (E) to base 1 (B1) discharging the capacitor. This develops a positive pulse on B1 which is applied to the gate-cathode junction of the SCR, causing it to turn on. Transistor Q02 turns on and Q07 goes off at this time. The supply voltage to the timer is within 2 diode drops (SCR anode to cathode and Q02 base-emitter) of ground. Therefore, it is pulled to approximately -1.6v at the end of the delay period. This removes the voltage from the timer and prevents free running oscillations of Q05. Transistor Q03 in the timing circuit is used as a compensating diode for temperature effects in the base-emitter junction of the constant current generator.

Any given time delay can be interrupted by returning the input to a "1", which causes Q01 to turn on and removes the voltage from the timer. However, because the timing capacitor may have charged to the full 6 volts, it will have to discharge via the unijunction emitter-base 1 junction and R10. Therefore, if C01 (0.22 uf) is used, a waiting period of approximately 50 usec must be allowed before a new delay is started. This could introduce a -5% change in the next delay period. If C02 (22 uf) is used, the waiting period would have to be approximately 5 msec for a -5% change in the next delay period. Note that the "1" input pulse width on either pin 1 or 3 should not be less than 50 usec to insure sufficient time for SCR to turn off.

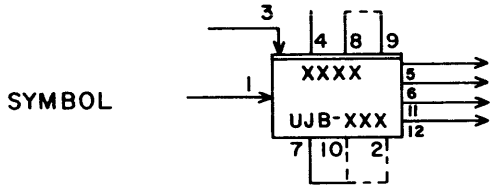
To use the card with relay or switch contacts (or an output card) pin 3 is used as the input, but pin 1 must be grounded to keep Q01 off.

Table 1. Delay Range (UJB)

Min.	Max.	Jumper Pins	Min.	Max.	Jumper Pins
0.4 msec	4 msec	7-10	40 msec	400 msec	7-10, 8-9
8 msec	80 msec	7-2	800 msec	8 sec	7-2, 8-9
90 msec	600 msec	7 open	9 sec	60 sec	7 open, 8-9

Table 2. Delay Range (UJC)

Min.	Max.	Jumper Pins	Min.	Max.	Jumper Pins
0.4 msec	10 msec	7-10	40 msec	1000 msec	7-10, 8-9
10 msec	100 msec	7-2	1000 msec	10 sec	7-2, 8-9
100 msec	1000 msec	7 open	10 sec	100 sec	7 open, 8-9



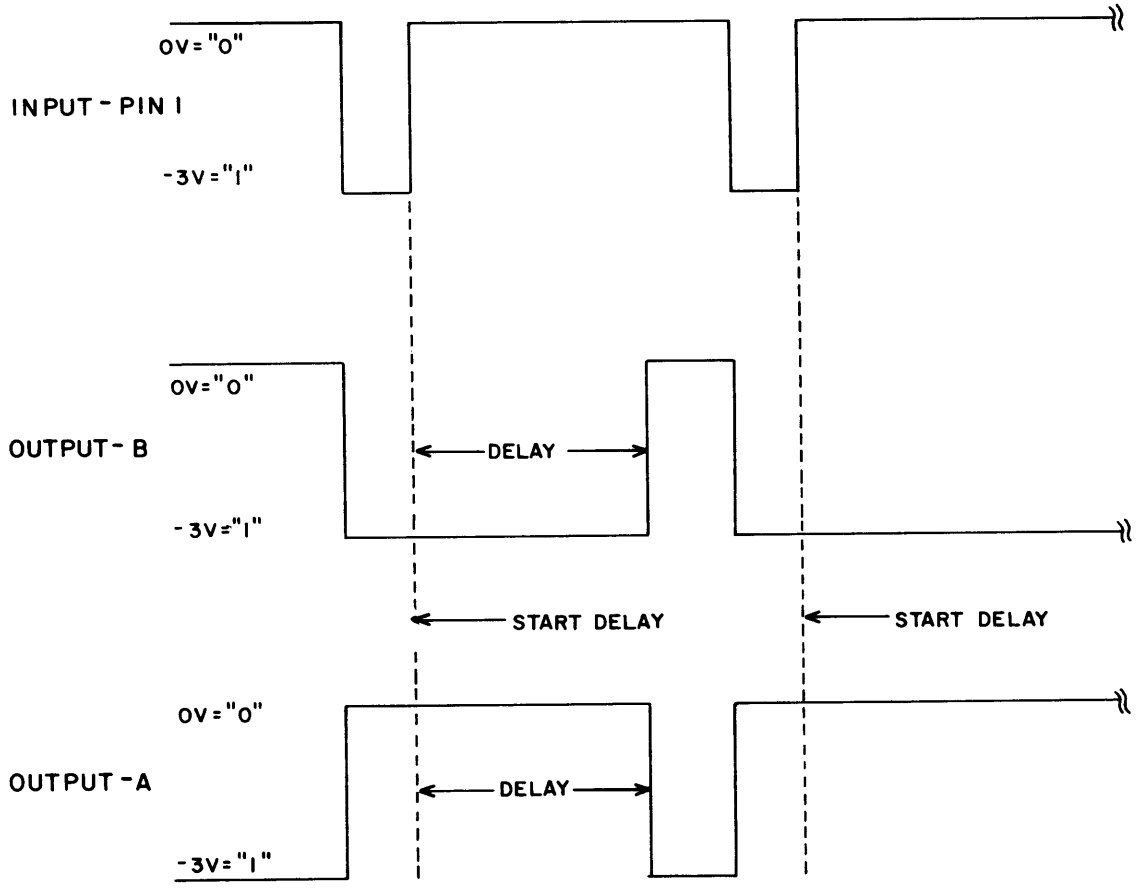


FIGURE 1. INPUT - OUTPUT WAVEFORMS

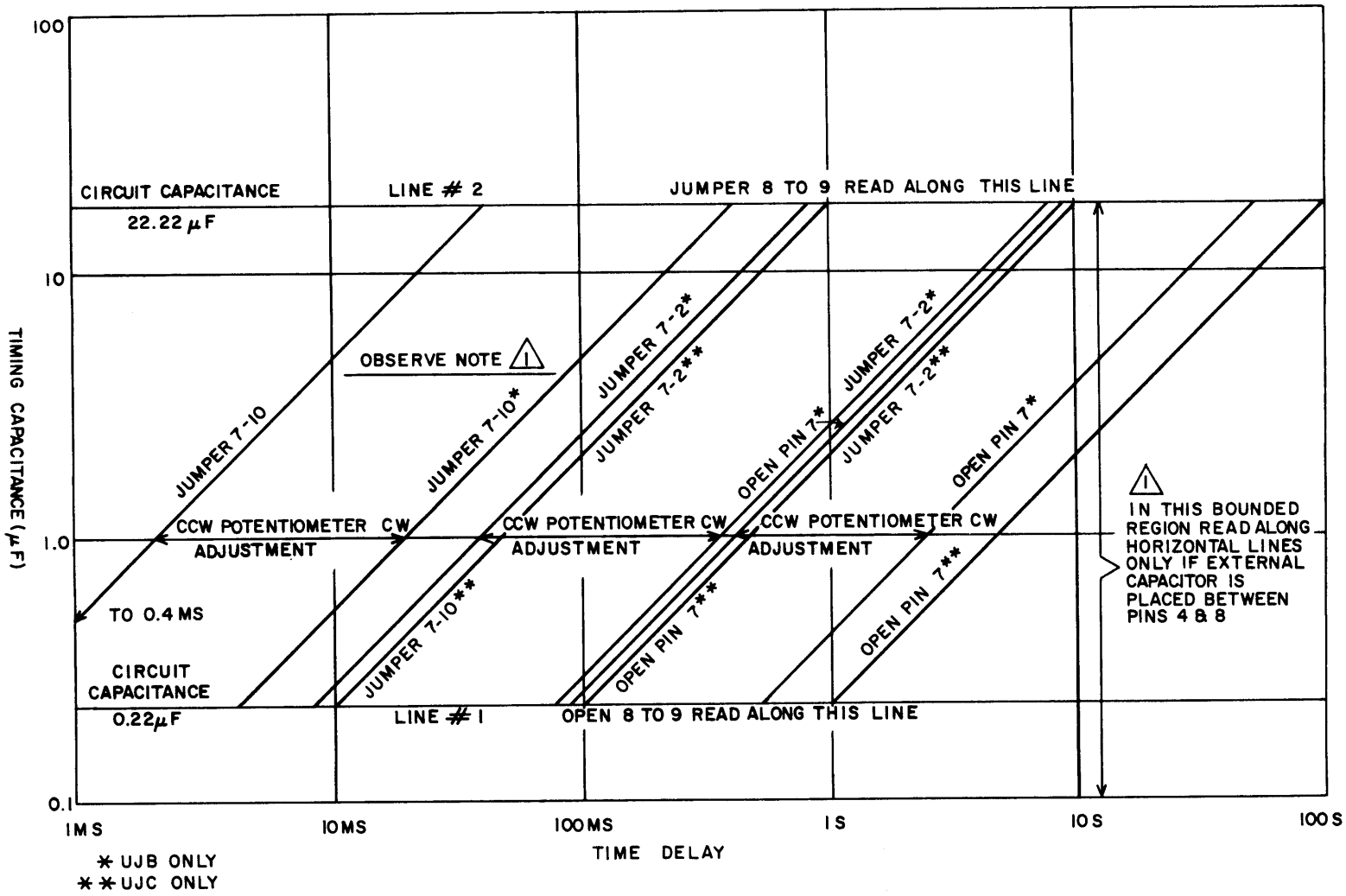
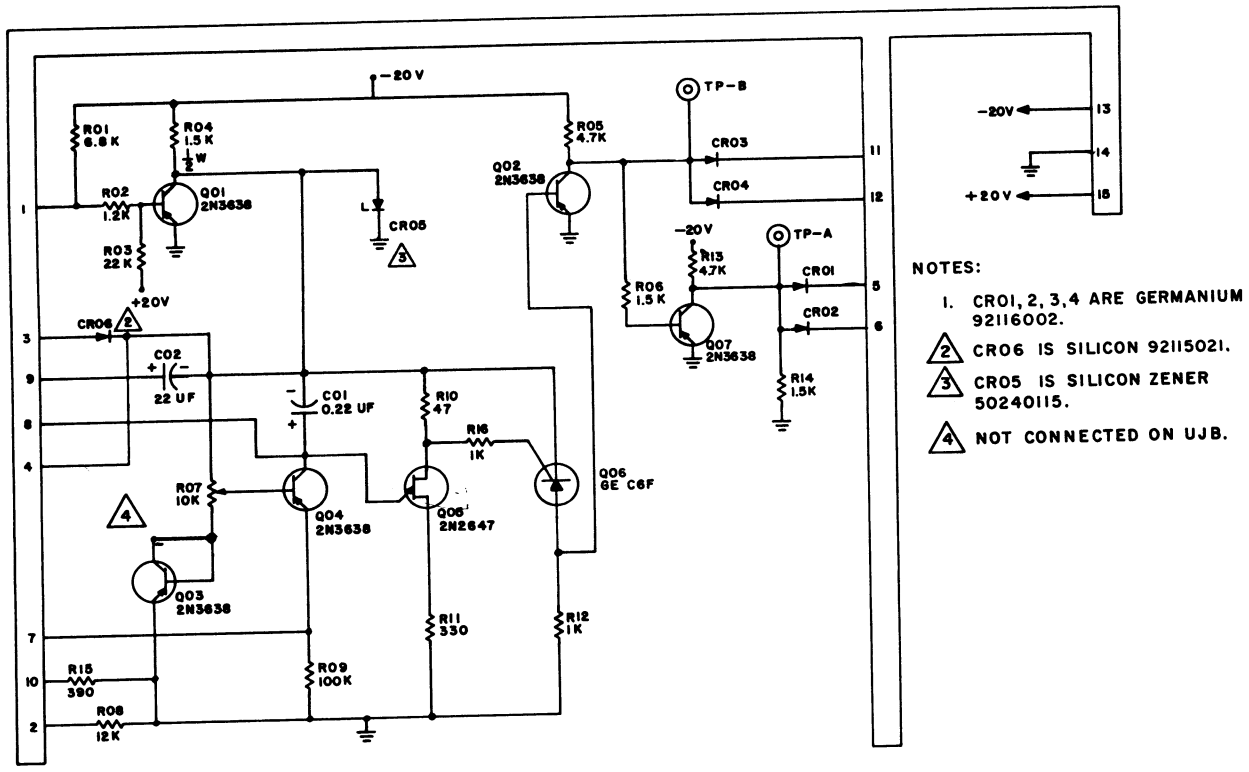
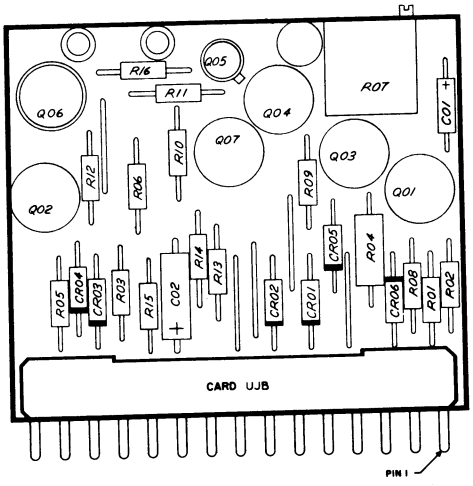


FIGURE 2. TIME DELAY VS JUMPER OPTIONS


-20V
R01 6.8K
R04 1.5K 1/2W
R02 1.2K
Q01 2N3638
R03 22K
+20V
CR06
C02 22 UF
C01 0.22 UF
R10 47
R16 1K
R07 10K
Q04 2N3638
Q05 2N2647
Q06 GE C6F
Q03 2N3638
R11 330
R12 1K
R15 390
R09 100K
R08 12K
R05 4.7K
Q02 2N3638
TP-B
CR03
CR04
CR05
-20V
TP-A
R13 4.7K
CR01
CR02
R06 1.5K
Q07 2N3638
R14 1.5K
-20V
+20V
NOTES:
1. CR01, 2, 3, 4 ARE GERMANIUM 92116002.
2 CR06 IS SILICON 92115021.
3 CR05 IS SILICON ZENER 50240115.
4 NOT CONNECTED ON UJB.

UJB


R16
Q05
R11
Q06
Q04
R07
C01
Q07
Q03
R10
R12
R06
R09
Q02
Q01
CR05
R04
R14
R13
C02
CR02
CR01
CR06
R08
R01
R02
R05
CR04
CR03
R03
R15
CARD UJB
PIN 1

GATED TOGGLE FLIP-FLOP
UKA

The UKA card is used in the 853 Disk Storage drive. When pin 3 is at logic zero (ground), a change of state from logic zero to logic one (-3V) at pin 1 causes the internal flip-flop to change state. When pin 3 is at logic one, both outputs are forced to logic zero.

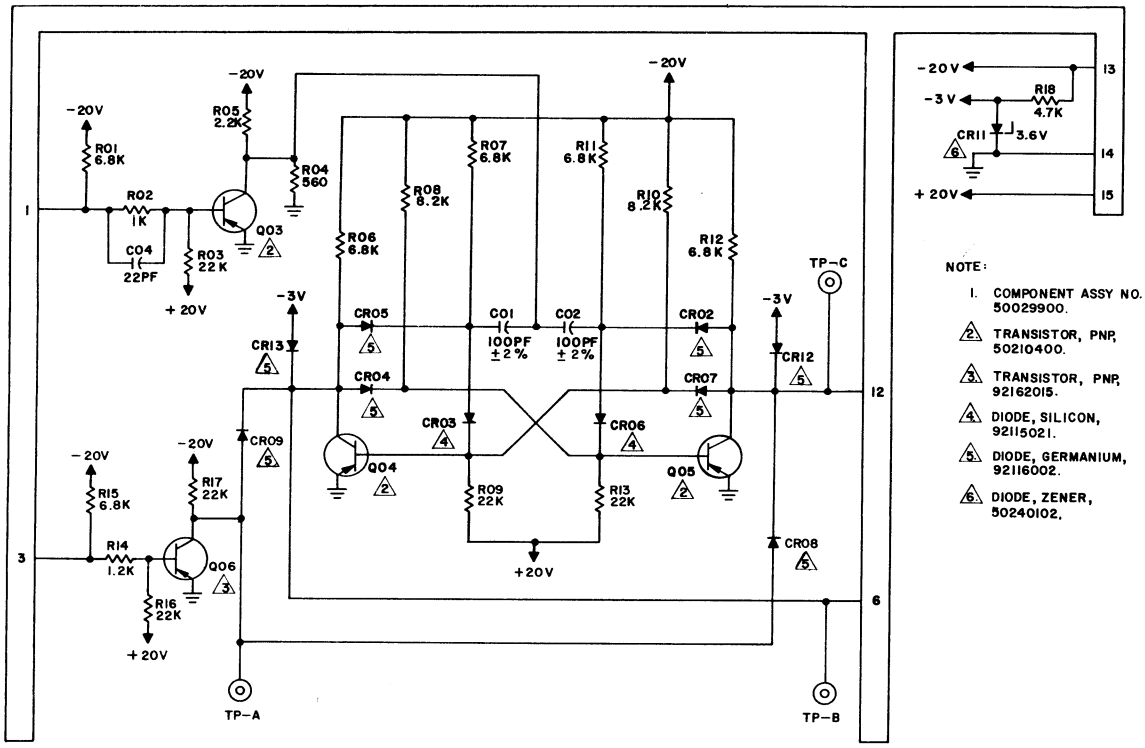
A negative going transition at pin 1 generates a positive going transition at Q03 collector. This is coupled through either C01 and CR03 to Q04 base, or through C02 and CR06 to Q05 base, depending on the state of the flip-flop. If Q04 is on, then the intersection of CR05, CR03, and C01 is at approximately -0.5V and Q04 base is at -0.8V, so that CR03 is reverse biased by 0.2V. On the other side of the flip-flop, the intersection of CR02, CR06, and C02 is at -3.6V while Q05 base is at -0.5V, so that CR06 is reverse biased by 3.1V. When Q03 turns on, current is pushed through C01 and C02 to R07 and R11, making the voltage at the anodes of CR03 and CR06 go more positive. Since CR03 is reverse biased much less than CR06, CR03 will be forward biased first, and the positive going waveform will be coupled to the base of Q04. This will turn Q04 off. As Q04 collector drops, Q05 base follows via CR04, turning Q05 on. As Q05 collector goes positive, this is coupled via CR07 to Q04 base, and the regeneration of the flip-flop is established.

The above description also applies if Q05 is on initially, with the appropriate substitution of components from one side to the other side of the flip-flop. Thus, it can be seen that every time the input at pin 1 passes the threshold going "negative", the flip-flop changes state. CR12 and CR13 clamp the off collector to the -3V internal supply made up of CR11 and R18.

When pin 3 is at ground, operation proceeds as above. When pin 3 goes to -3V, Q06 turns on, pulling both output pins 6 and 12 to -0.5V. Since this circuit drives the write/erase drivers AMC, the -0.5V output at pins 6 and 12 turns off all writing and erasing, regardless of what pin 1 does. When Q06 goes off again, the flip-flop may settle out in either state; however, since the 853 uses double-frequency recording, this is permissible.

There are no AND diodes at the outputs of this card.

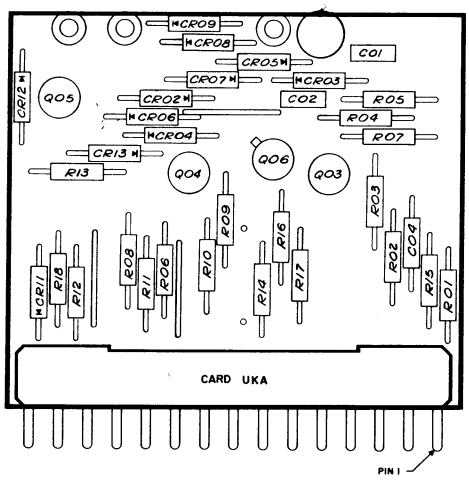
SYMBOL



NOTE:

1. COMPONENT ASSY NO. 50029900.
2. TRANSISTOR, PNP, 50210400.
3. TRANSISTOR, PNP, 92162015.
4. DIODE, SILICON, 92115021.
5. DIODE, GERMANIUM, 92116002.
6. DIODE, ZENER, 50240102.

UKA



GATED TOGGLE FLIP-FLOP
UKB

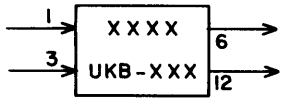
The UKB card contains a toggle flip-flop circuit and a gating circuit which, when turned on, hold the flip-flop outputs at ground. When the gate is turned off, it guarantees that the same output will reset to a "1". The flip-flop changes state with each negative going transition of a logic signal (0v to -3v) input. The gate circuit operates from a logic level input, with a "1" causing the gate to disable the flip-flop outputs. When the gate input goes to a "0", the output at pin 12 will remain at a "0" level while the output at pin 6 will come up as a "1".

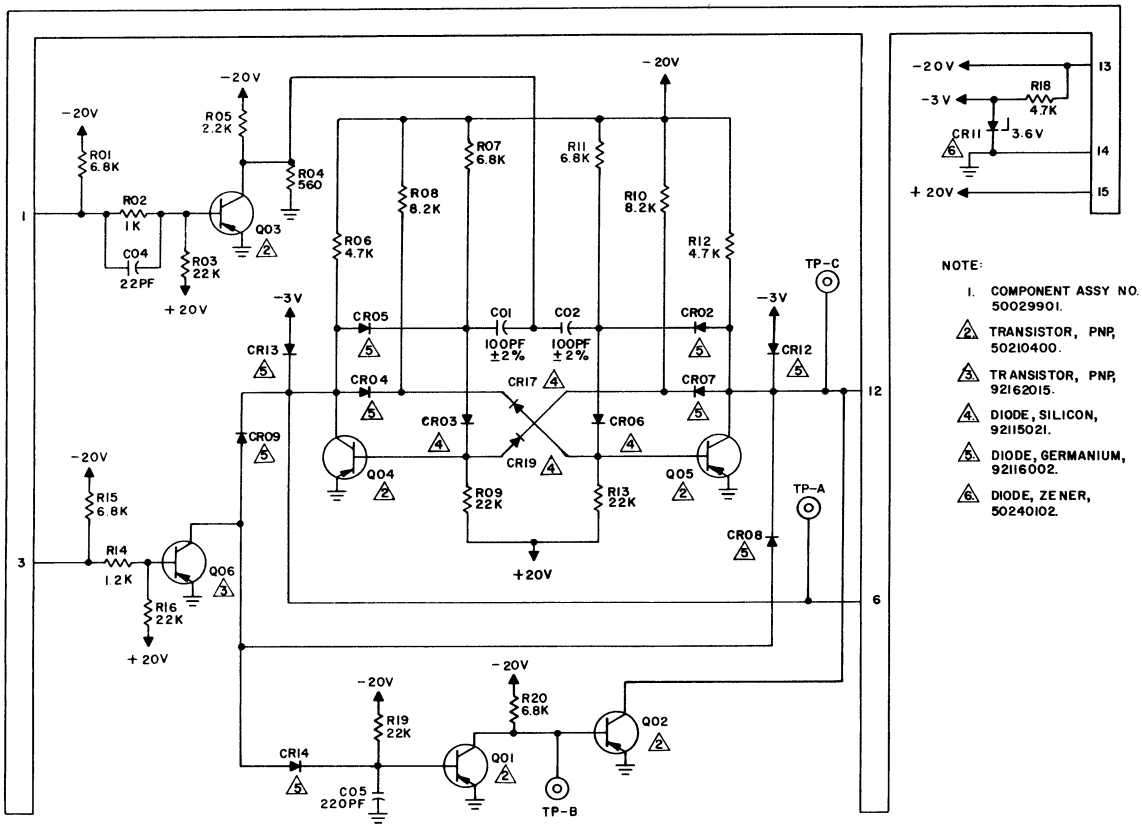
The input to the toggle flip-flop is pin 1. A negative transistion (0v to -3v) on the input causes Q03 to turn on. The collector of Q03 goes from a negative divider voltage (determined by R04 and R05) to near ground. This positive going transition is coupled through C01 and C02 to the anodes of CR03 and CR06. If Q04 is conducting and Q05 is turned off, then CR06 is back biased and CR03 conducts the positive pulse into the base of Q04 and turns it off. The collector of Q04 (pin 6) then goes toward -3.6V with CR04 conducting this change to Q05 base divider circuitry which consists of R13, CR17, and R08. The threshold of Q05 referred back to Q04 collector is at -1.2V. Q05 then turns on and the collector goes toward ground into saturation. CR07 conducts this change into Q04 base divider circuitry (R09, CR19, and R10) and holds Q04 off completing the flip-flop action. The next negative transition which appears at the input gets inverted to a positive transition by Q03 and couples through C02 and CR06 to turn off Q05. CR07 feeds back to the base circuitry of Q04 turning it on. CR04 then feeds back to the base circuitry of Q05 completing the lock up action by providing a back bias. Since the flip-flop is actuated by a short pulse, it is somewhat sensitive to any delay of its feedback mechanism. Consequently, this flip-flop will not reliably operate with more than an equivalent of approximately 100 pf to ground (and 3.3K load resistors to -20V) per output. The excursions are from -0.2V to -4V and nominal switching time is 20 nanoseconds, measured from the -2 volt levels of input to output signal (again with 3.3K loads to -20V).

The gate circuit is operated by a logic level input at pin 3. With

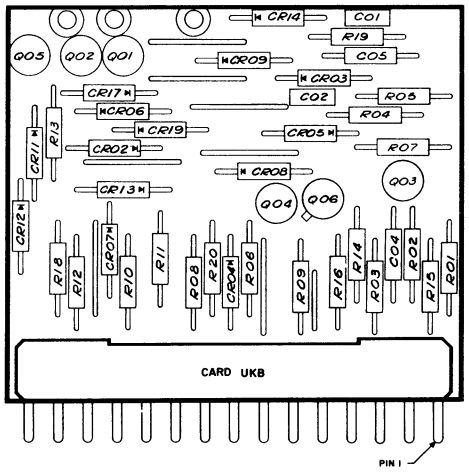
a "1" input (-3V) Q06 turns on and pulls both outputs (Pin 6 and 12) of the flip-flop through diodes to ground. Q06 quickly discharges C05 and Q01 turns off. This allows Q02 to turn on and its output is "anded" with the output of Q06 at pin 12. When the gate input goes to a "0", Q06 turns off, releasing the outputs at 6 and 12. However, pin 12 is still held at ground because of the delaying action of C05 on the reset circuit of Q01 and Q02. This delayed holding of pin 12 is nominally 0.12 microseconds, and allows pin 6 to go to a "1" (-4V) as a conditioned reset. Gate turn on time is 0.08 usec Max.

SYMBOL




-20V
R01 6.8K
R02 1K
C04 22PF
R03 22K
+20V
R05 2.2K
R04 560
Q03
R06 4.7K
R08 8.2K
R07 6.8K
R11 6.8K
R10 8.2K
R12 4.7K
-3V
CR13
CR05
C01 100PF ±2%
C02 100PF ±2%
CR02
CR12
CR04
CR17
CR07
CR03
CR06
CR09
CR19
Q04
Q05
R09 22K
R13 22K
TP-C
TP-A
CR08
R15 6.8K
R14 1.2K
Q06
R16 22K
R19 22K
R20 6.8K
Q02
Q01
CR14
C05 220PF
TP-B
1
3
6
12
-20V
-3V
R18 4.7K
CR11 3.6V
+20V
13
14
15
NOTE:
1. COMPONENT ASSY NO. 50029901.
2. TRANSISTOR, PNP, 50210400.
3. TRANSISTOR, PNP, 92162015.
4. DIODE, SILICON, 92115021.
5. DIODE, GERMANIUM, 92116002.
6. DIODE, ZENER, 50240102.

UKB


CR14
C01
R19
C05
CR09
CR03
C02
R05
R04
CR17
CR06
CR19
CR05
R07
CR02
CR08
CR13
Q05
Q02
Q01
Q04
Q06
Q03
CR12
CR11
R13
R18
R12
CR07
R10
R11
R08
R20
CR04
R06
R09
R16
R14
R03
C04
R02
R15
R01
CARD UKB
PIN 1

PULSE SHAPER

XKA

The XKA card operates as a single pulse generator with a circuit normally switched to a "0" on the output. When the last of the two inputs changes from "1" to "0" within 10 usec, the card provides a "1" output for 2 to 4 usec. If either input returns to a "1" while the output is a "1", the output switches to a "0" within 0.5 usec.

The circuit consists of an inverter stage followed by a RC differentiating circuit and an emitter follower output. The input stage is similar to a two-input inverter. The negative excursion on the output of the first stage equals -6v, which compensates for attenuation in the RC differentiator.

The variations in the emitter follower (Q02) or the number of loads connected to the output have only a second order effect on the RC time constant. The time constant depends almost entirely on the values of R07 and C01. Resistor R07 also limits the base drive and saturation.

PULSE SHAPER

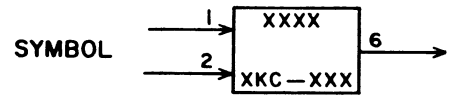
XKC

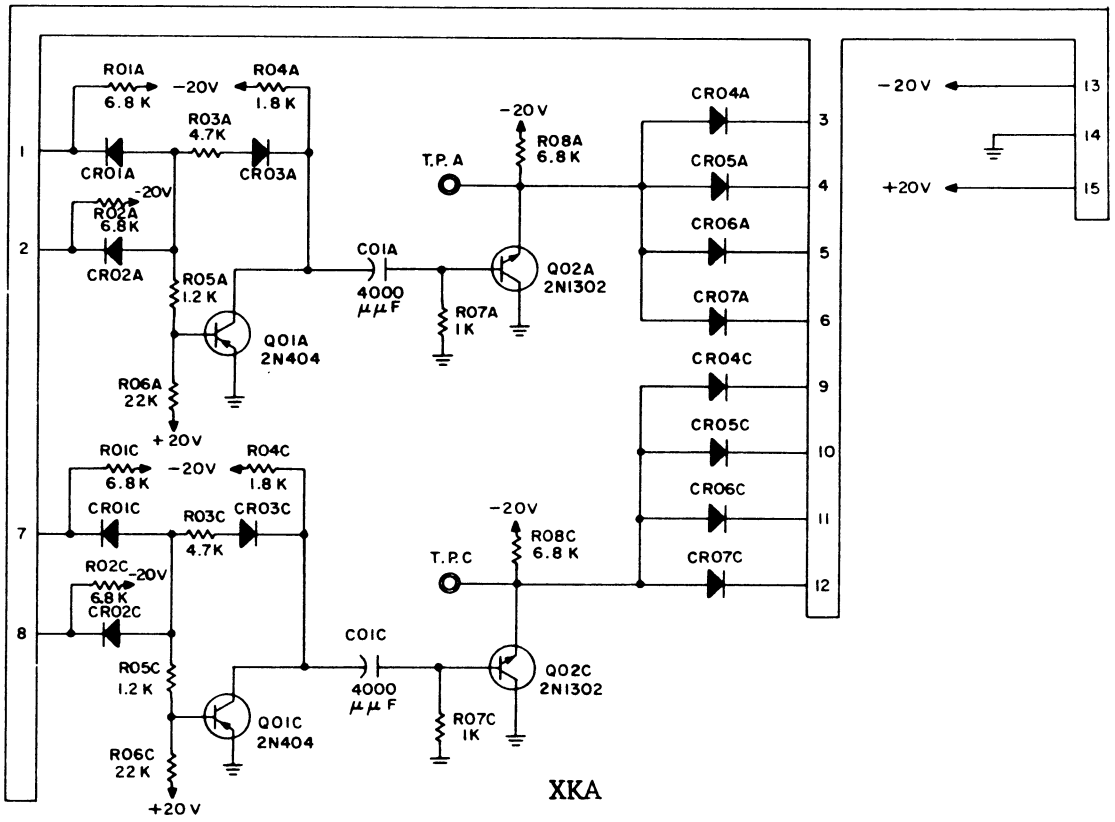
The XKC circuit operates in a similar manner to the XKA but provides much less internal delay and shorter duration output "1" pulses.

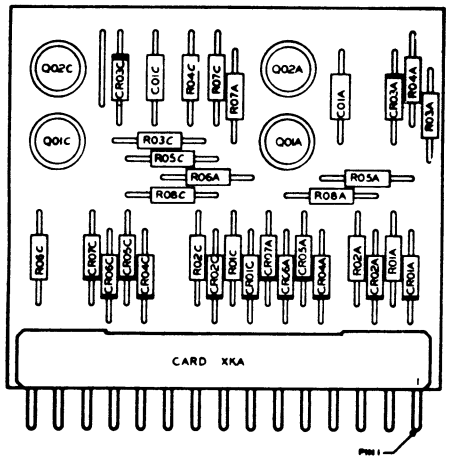
Logic "1" OR inputs feed directly to the Q01 base divider circuit and through diode CR08 to the base divider circuit of Q02. The parallel impedance of both these dividers is approximately the same as the base divider of a standard inverter. Q02 also has an "OR" input from the collector circuit of Q01. C01 in the collector circuit holds Q02 off for about 0.4 usec following a positive input signal. This determines the width of the "1" pulse output from Q02. On the return of the input to a "1", R08 delays recycling of C01 sufficiently to prevent the occurrence of runt output pulses at the time the input goes through the threshold of switching.

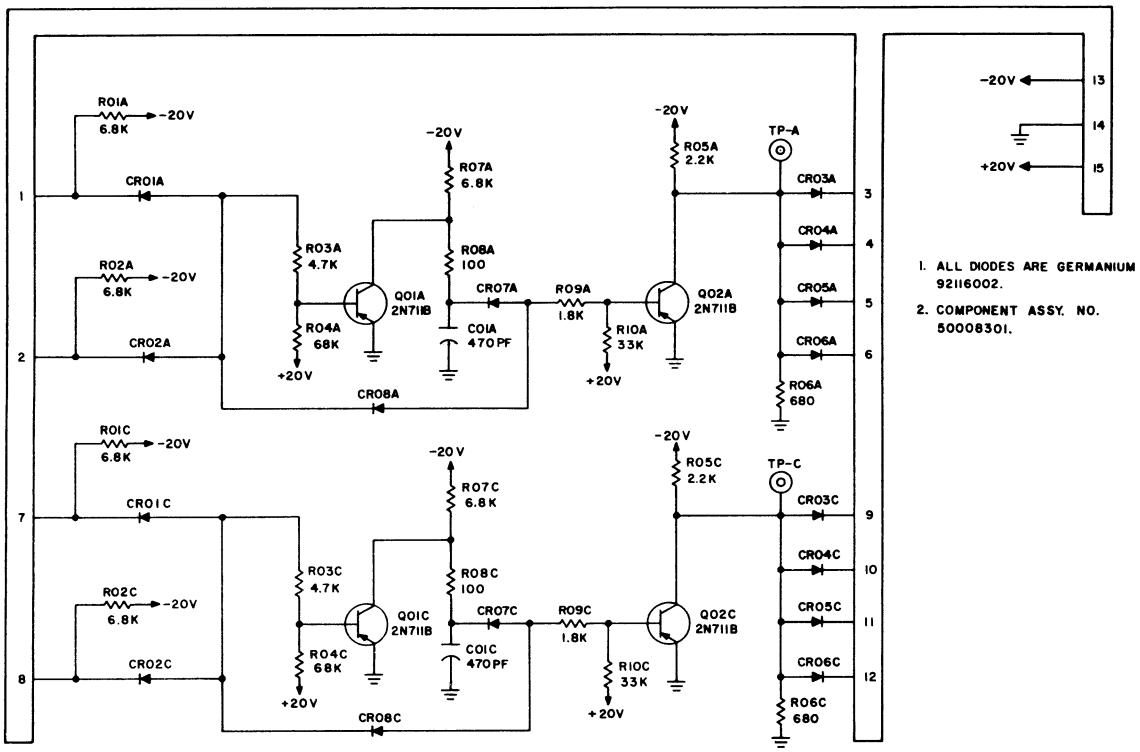
For power supplies in which the + and - voltages are equal within 1 volt and within the range of 16 to 24 volts, the output pulse width at the -2v level is 0.25 to 0.50 usec. Delay between input and output at the -2v level is 30 to 120 nsec under the same power supply conditions. The circuit is critical to rise time at the input and this should not exceed 250 nsec. In timing chain applications using a series string of XKC cards, delay from the first to last card is subject to pulse width variations of individual cards, but remains typically stable within 5% for a given set

of cards over an ambient temperature range of 75° F to 150° F.



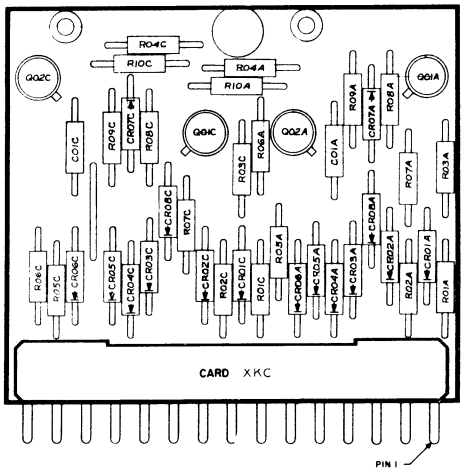






1. ALL DIODES ARE GERMANIUM 92116002.
2. COMPONENT ASSY. NO. 5000830I.

XKC



APPENDIX 1

Tabulated Listing,
Control Data Corporation
Printed Circuit Cards

NOTE:
Further up-to-date listings may be obtained at any time by ordering the Standard Printed Circuit Card Index, available from Engineering Services, Computer Division.

PIN ASSIGNMENTS

1604 & 3600

PRINTED CIRCUIT CARDS

X = Production discontinued.

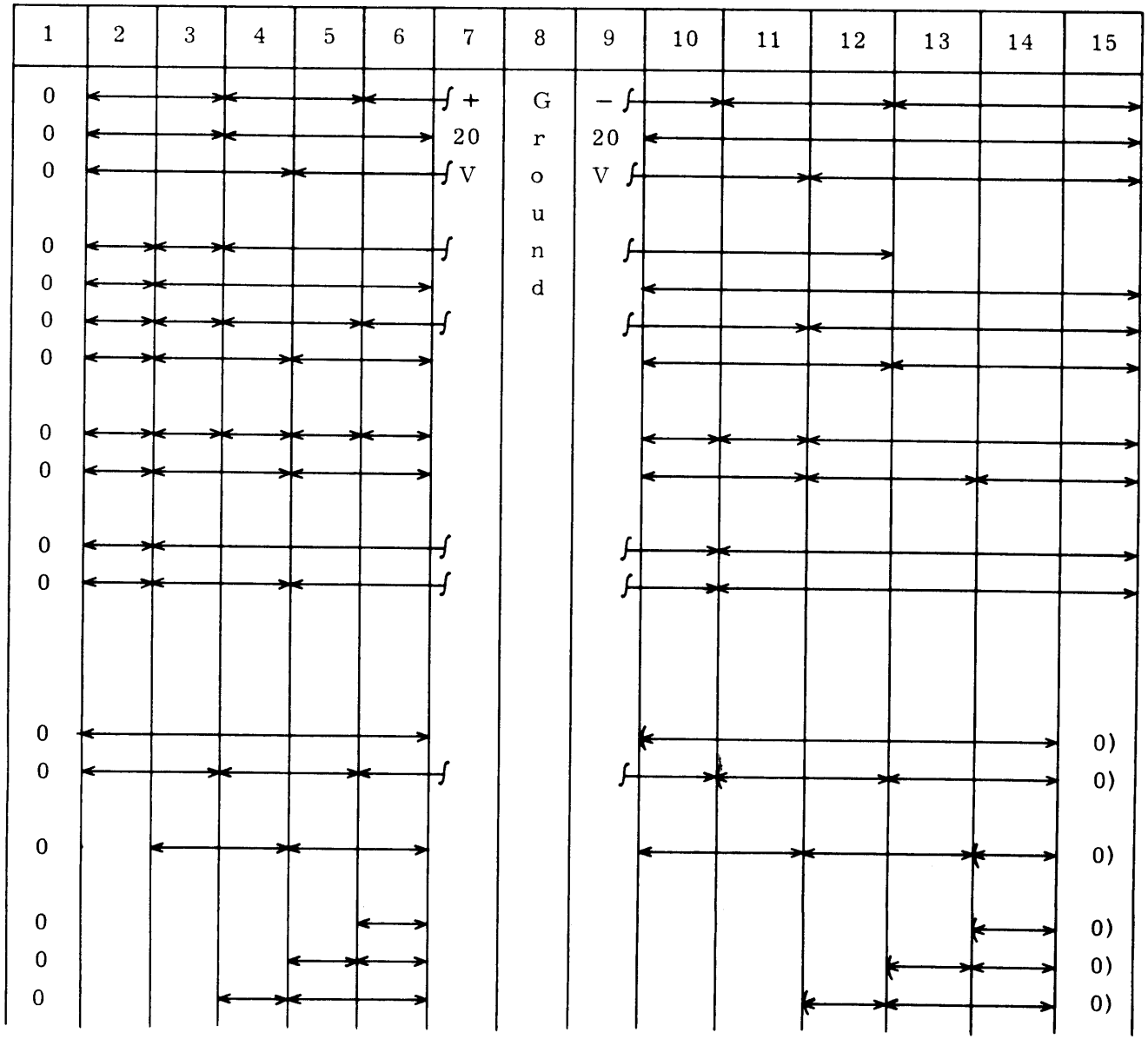
Do not use for new design.

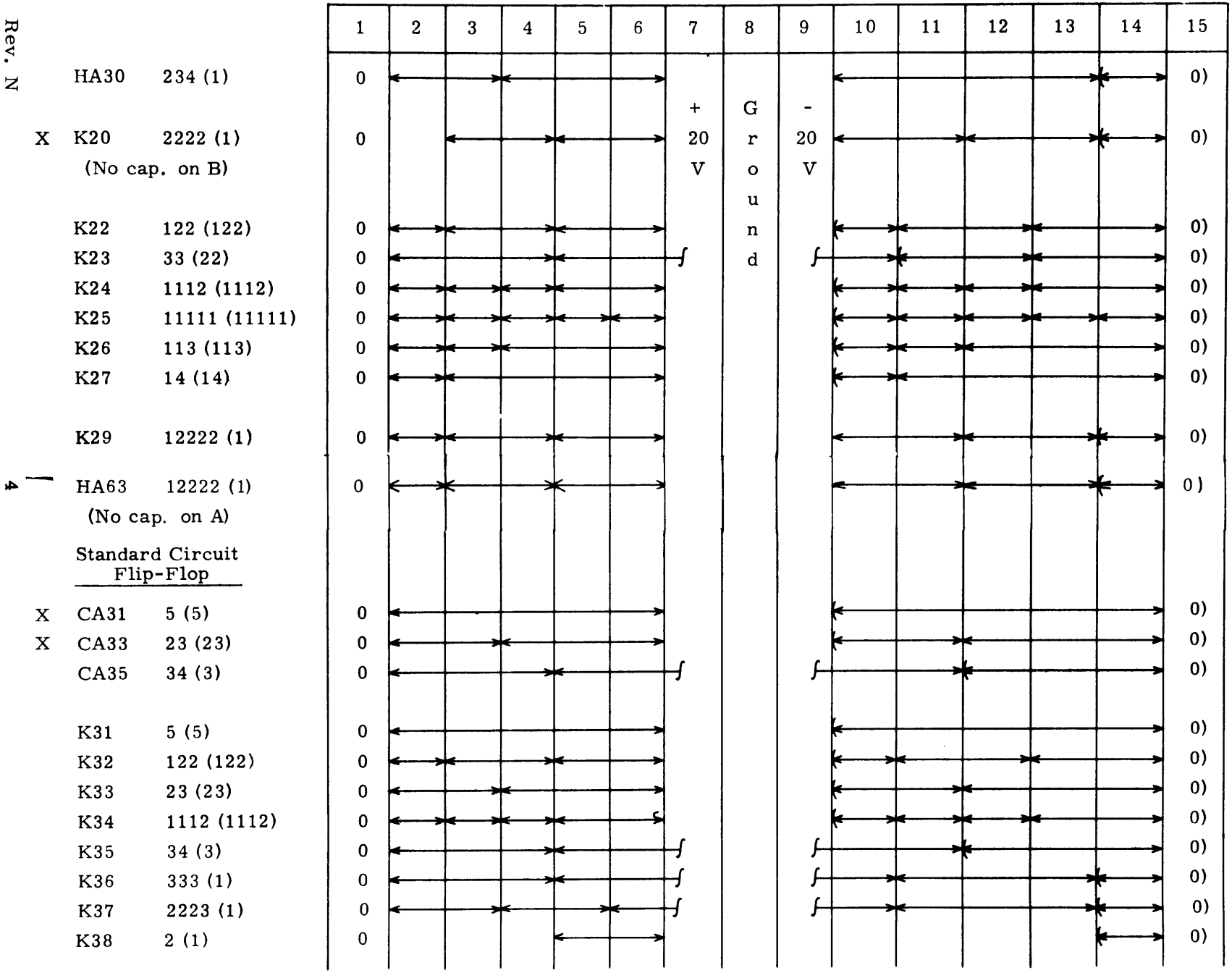
Standard Circuit Single Inverter

CA15	22223
CA52	236
CA55	344
K11	116
K12	146
K13	11234
K14	12233
K16	11111114
K17	122222
K51	155
K58	1235

Standard Circuit Double Inverter

CA21	5 (5)
CA28	222 (22)
HA05	2222 (1)
HA07	1 (1)
HA08	11 (11)
HA09	12 (12)




1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
HA30 234 (1)
X K20 2222 (1)
(No cap. on B)
K22 122 (122)
K23 33 (22)
K24 1112 (1112)
K25 11111 (11111)
K26 113 (113)
K27 14 (14)
K29 12222 (1)
HA63 12222 (1)
(No cap. on A)
Standard Circuit Flip-Flop
X CA31 5 (5)
X CA33 23 (23)
CA35 34 (3)
K31 5 (5)
K32 122 (122)
K33 23 (23)
K34 1112 (1112)
K35 34 (3)
K36 333 (1)
K37 2223 (1)
K38 2 (1)
+20 V
Ground
-20 V
0
0)

Standard Circuit Control Delay

	CA40	3
	CA44	1423
	CA46	55
	CA47	244
	CA48	2323

10 pf Capacitor Single Inverter

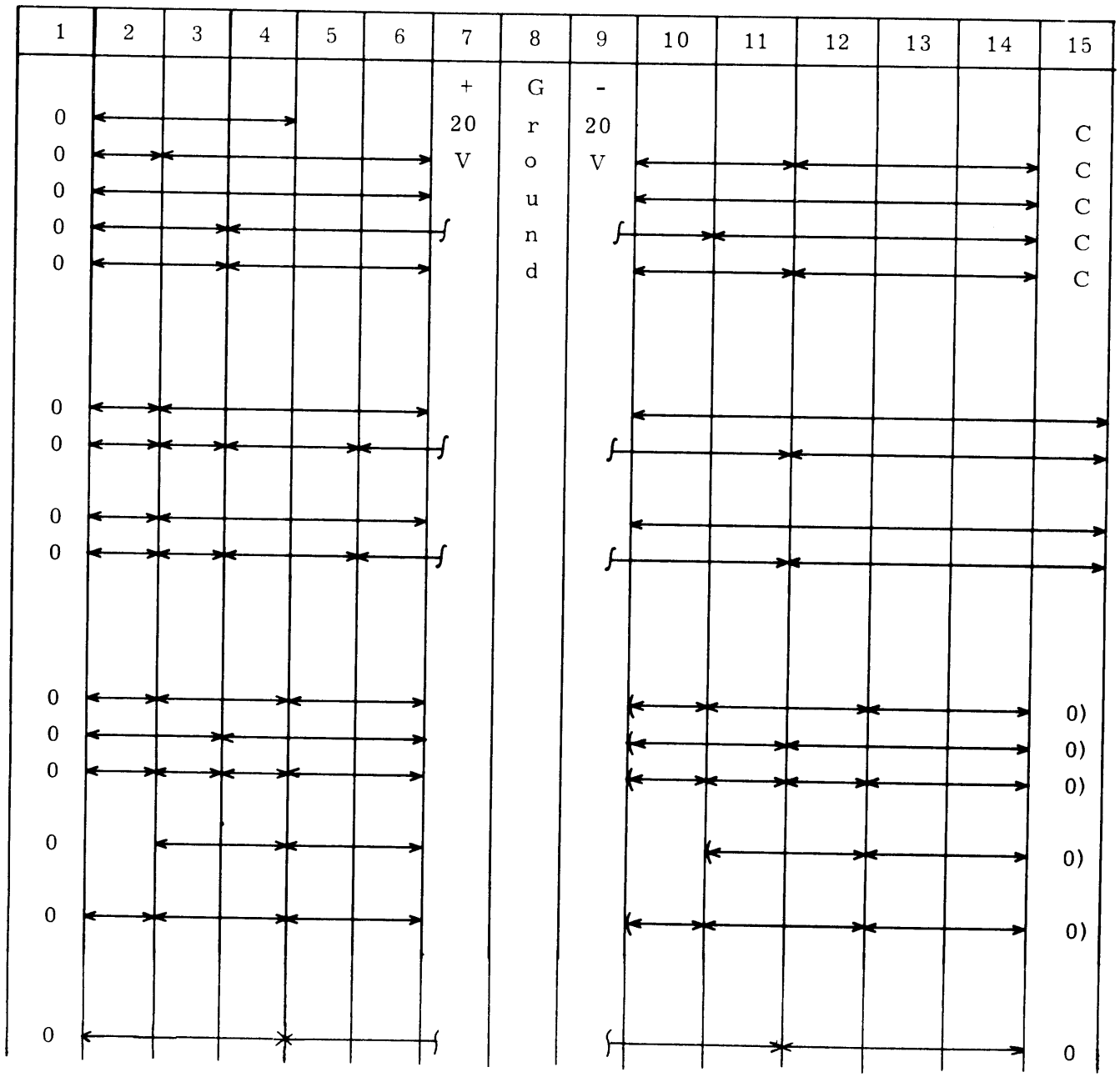
X	CA92	146
X	CA93	11234
	K92	146
	K93	11234

10 pf Capacitor Double Inverter

X	CA72	122, (122)
	CA73	23 (23)
	CA74	1112 (1112)
	HA06	22 (22)
	K72	122 (122)

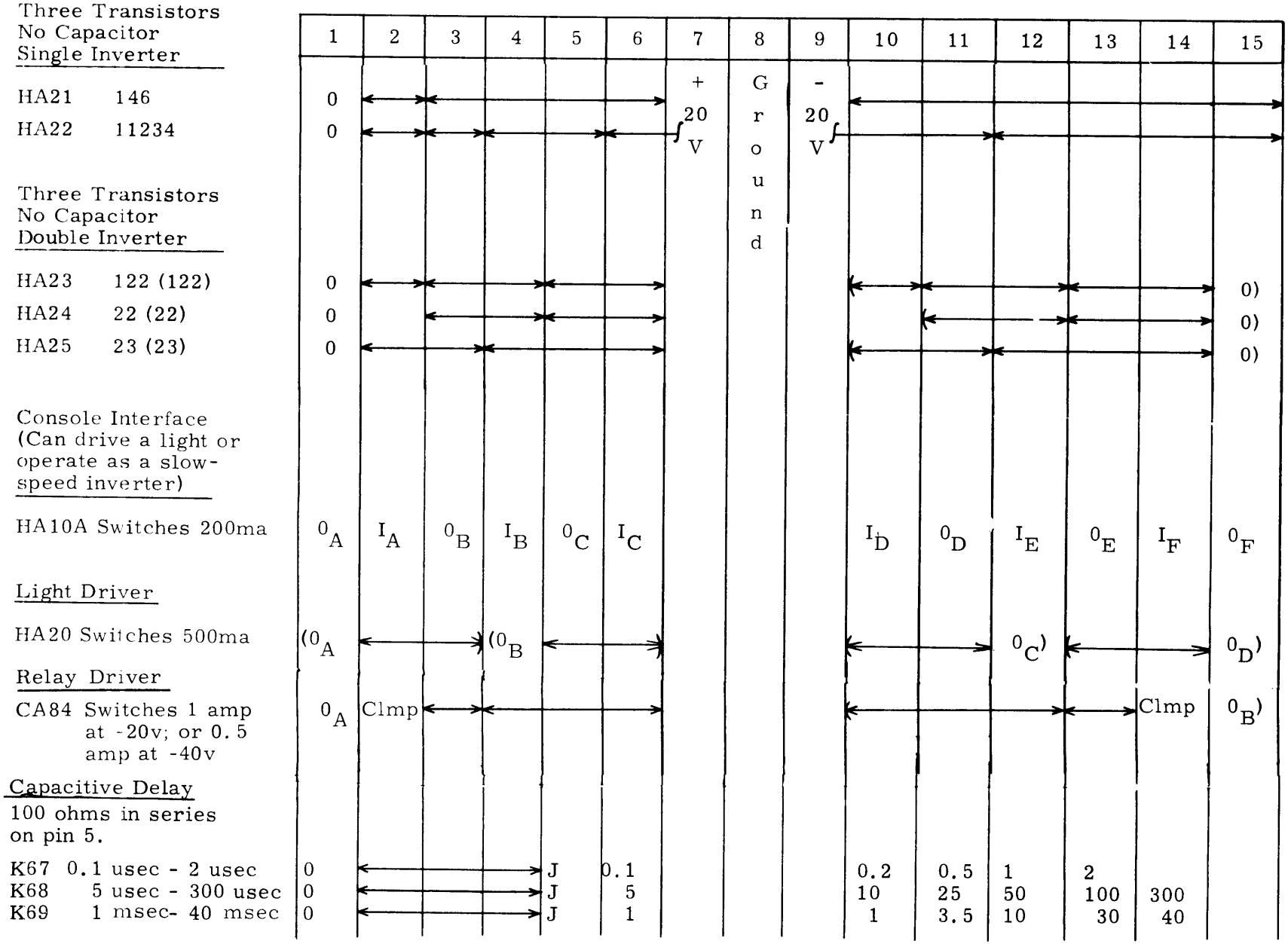
10 pf Capacitor Flip-Flop

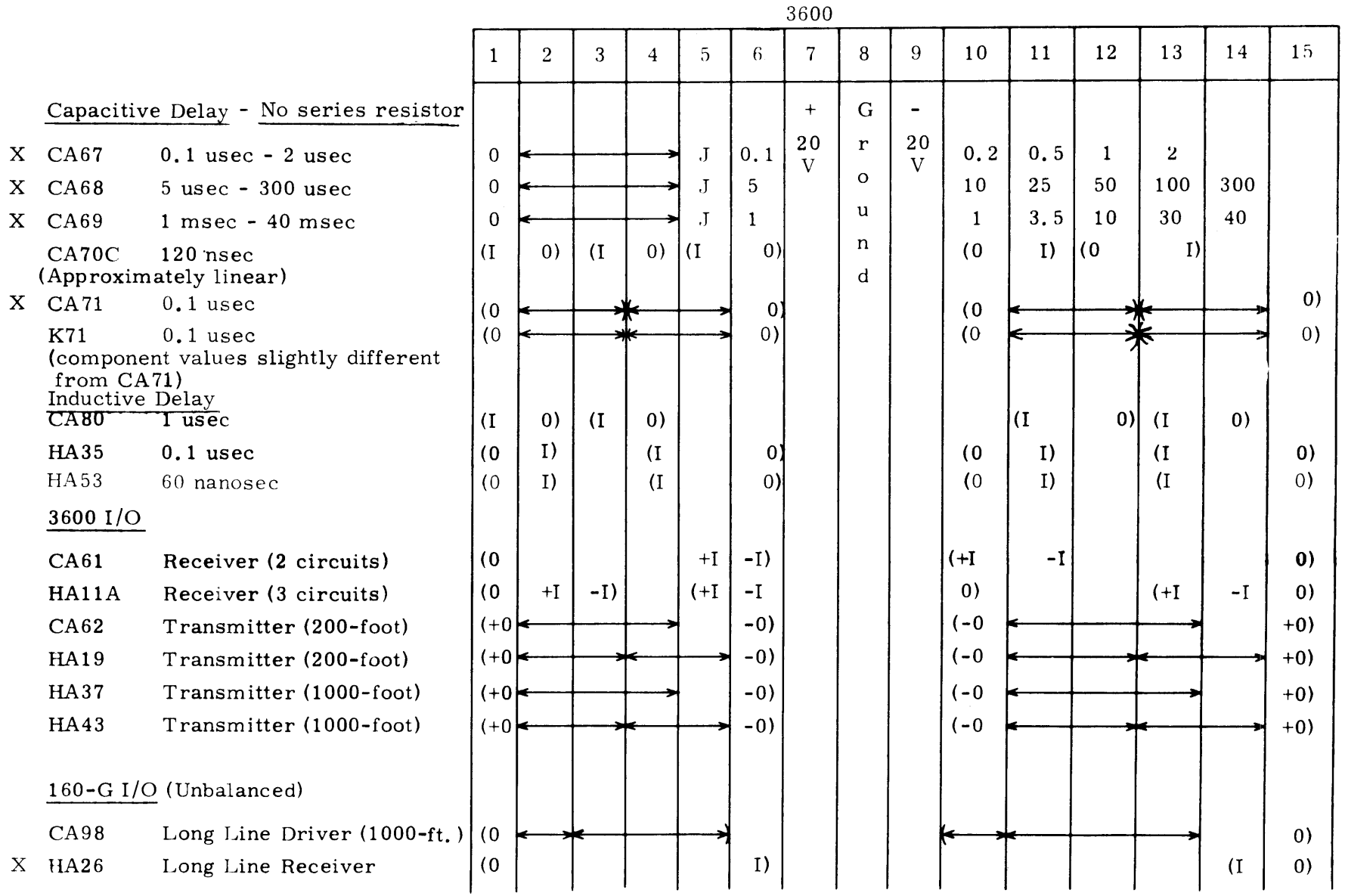
	HA67	34 (3)

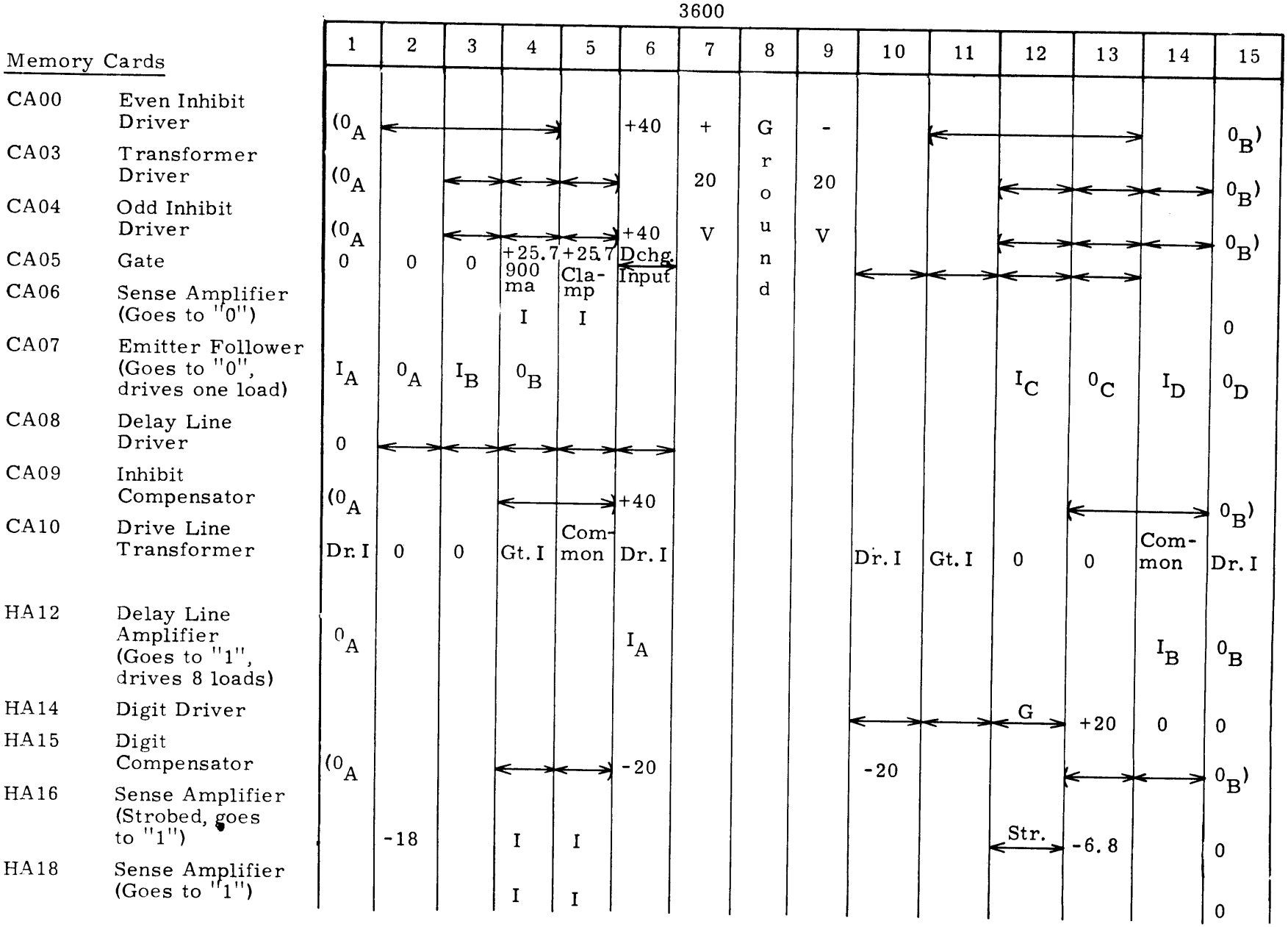


3600

			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	No Capacitor Single Inverter																
X	K18	11111114	0	←	←	←	←	←	+	G	-	←	←	←			→
X	K19	122222	0	←	←		←		20	r	20	←		←		←	→
									V	o	V						
	No Capacitor Double Inverter									u							
										n							
										d							
X	K20	2222 (1)	0		←		←					←		←		←	0)
	(No cap. on B)																
	K21	1 (1)	0					←								←	0)
	K28	11111 (11111)	0	←	←	←	←	←				←	←	←	←	←	0)
	HA63	12222 (1)	0	←	←		←					←		←		←	0)
	(No cap. on A)																
	HA68	122 (122)	0	←	←		←					←		←		←	0)
	No Capacitor Flip-Flop																
X	K30	1112 (1112)	0	←	←		←					←		←			0)
	Standard Circuit Double Flip-Flop																
	HA46	2 (2) 2 (2)	0	←		←		0)				0	←		←		0)
	Standard Circuit Quadruple Inverter																
	HA47	2 (2) 2 (2)	0	←		←		0)				0	←		←		0)
	10 pf Capacitor Quadruple Inverter																
	HA48	11 (11) 11 (11)	0	←	←	←		0)				0	←	←	←		0)


Three Transistors
No Capacitor
Single Inverter
HA21 146
HA22 11234
Three Transistors
No Capacitor
Double Inverter
HA23 122 (122)
HA24 22 (22)
HA25 23 (23)
Console Interface
(Can drive a light or operate as a slow-speed inverter)
HA10A Switches 200ma
Light Driver
HA20 Switches 500ma
Relay Driver
CA84 Switches 1 amp at -20v; or 0.5 amp at -40v
Capacitive Delay
100 ohms in series on pin 5.
K67 0.1 usec - 2 usec
K68 5 usec - 300 usec
K69 1 msec- 40 msec
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
+ 20 V
Ground
- 20 V
0A IA 0B IB 0C IC ID 0D IE 0E IF 0F
(0A (0B 0C) 0D)
0A Clmp Clmp 0B)
0 J 0.1 0.2 0.5 1 2
0 J 5 10 25 50 100 300
0 J 1 1 3.5 10 30 40


3600
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Capacitive Delay - No series resistor
X CA67 0.1 usec - 2 usec
X CA68 5 usec - 300 usec
X CA69 1 msec - 40 msec
CA70C 120 nsec
(Approximately linear)
X CA71 0.1 usec
K71 0.1 usec
(component values slightly different from CA71)
Inductive Delay
CA80 1 usec
HA35 0.1 usec
HA53 60 nanosec
3600 I/O
CA61 Receiver (2 circuits)
HA11A Receiver (3 circuits)
CA62 Transmitter (200-foot)
HA19 Transmitter (200-foot)
HA37 Transmitter (1000-foot)
HA43 Transmitter (1000-foot)
160-G I/O (Unbalanced)
CA98 Long Line Driver (1000-ft.)
X HA26 Long Line Receiver
+ 20 V
Ground
- 20 V
0 J 0.1 0.2 0.5 1 2
0 J 5 10 25 50 100 300
0 J 1 1 3.5 10 30 40


3600
Memory Cards
CA00 Even Inhibit Driver
CA03 Transformer Driver
CA04 Odd Inhibit Driver
CA05 Gate
CA06 Sense Amplifier (Goes to "0")
CA07 Emitter Follower (Goes to "0", drives one load)
CA08 Delay Line Driver
CA09 Inhibit Compensator
CA10 Drive Line Transformer
HA12 Delay Line Amplifier (Goes to "1", drives 8 loads)
HA14 Digit Driver
HA15 Digit Compensator
HA16 Sense Amplifier (Strobed, goes to "1")
HA18 Sense Amplifier (Goes to "1")
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
(0A +40 + Ground - 0B)
20 20
(0A +40 V V 0B)
0 0 0 +25.7 900 ma +25.7 Clamp Dchg. Input
I I
0
IA 0A IB 0B IC 0C ID 0D
0
(0A +40 0B)
Dr. I 0 0 Gt. I Common Dr. I Dr. I Gt. I 0 0 Common Dr. I
0A IA IB 0B
G +20 0 0
(0A -20 -20 0B)
-18 I I Str. -6.8 0
I I 0

3600

Clock	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Oscillator - Amplifier															
CA01 8 Megacycle HA50 6 Megacycle	LOGIC 0	TRAN.	SEC O	TANK 0		I	+ 20 V	Ground	- 20 V	I		TANK 0	TRANS. 0	SEC.	LOGIC 0
Clock Regulator															
CA96 8mc Crystal HA49 6mc Crystal					O_A						O_B				
Crystal Oscillator															
CA81 30 Kilocycle CA82 83.3 Kilocycle CA83 120 Kilocycle	O_{LO}	O_{HI}													
HA00 3 Kilocycle		O													
Amplifier - Shaper															
CA89 0.2 usec "1" output on positive-going input	I														O
Tuning Fork Oscillator															
HA42 1 Kilocycle	O_A														O_B
Low Speed Oscillator															
HA33 (Negative Voltage on input varies repetition rate from 3 to 50 cps on 3200 Auto-Step)	O				I										O inv

Cards to Establish Signal Levels		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CA02	Clamp (All Pins held between -0.9v and -6.5v)	I	I	I	I	I	I	+ 20 v	Ground	- 20 v	I	I	I	I	I	I
CA63	Terminator (6 twisted-pair)	(+	-)	(+	-)	(+	-)				(+	-)	(+	-)	(+	-)
HA17	Filter (Series 680Ω, 4.7 uf shunt)	O_A	I_A	O_B	I_B	O_C	I_C				I_E	O_E	I_F	O_F	I_G	O_G
HA39	Line Terminator (Negative-going spikes clamped at -6.2V)	I	I	I	I	I	I				I	I	I	I	I	I
HA44	Ground (Outputs same as "clear" FF)	-6.2v "1"														Grd. "0"
HA45	Bias (All pins held at -5.8v)	"1"	"1"	"1"	"1"	"1"	"1"				"1"	"1"	"1"	"1"	"1"	"1"
HA69	Jumper (Connects pin 1 to pin 10, and pin 15 to pin 2)															

1604

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
00	Clock Disconnect	I_A	I_A	I_A	I_A	I_A	I_A	I_B	I_B	I_B	I_B	I_B	I_B	20 V	Ground	+20 V
01	Oscillator	T_E	O_E	O_E	O_E	O_E	O_E	T_O	O_O	O_O	O_O	O_O	O_O			
02	Oscillator	T_E	O_E	O_E	O_E	O_E	O_E	T_O	O_O	O_O	O_O	O_O	O_O			
03	Crystal Oscillator, 30KC	O_{LO}	O_{HI}													
04	Amplifier Shaper	I				O	O	O	O	O	O	O	O			
05	Crystal Oscillator, 83.4KC	O_{LO}	O_{HI}													
06	Oscillator Amplifier	I_A	O_A	O_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	O_B	O_B			
07	Crystal Oscillator, 120KC	O_{LO}	O_{HI}													
11	Inverter	I				O	O	O	O	O	O	O	O			
12	Inverter	I	I			O	O	O	O	O	O	O	O			
13	Inverter	I	I	I		O	O	O	O	O	O	O	O			
14	Inverter	I	I	I	I	O	O	O	O	O	O	O	O			
15	Inverter	I	I	I	I	I	O	O	O	O	O	O	O			
16	Inverter	I	I	I	I	I	I	O	O	O	O	O	O			
20	Quadruple Inverter	I_A	O_A	O_A	I_B	O_B	O_B	I_C	O_C	O_C	I_D	O_D	O_D			
21	Double Inverter	I_A	O_A	O_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	O_B	O_B			
22	Double Inverter	I_A	I_A	O_A	O_A	O_A	O_A	I_B	I_B	O_B	O_B	O_B	O_B			
23	Double Inverter	I_A	I_A	I_A	O_A	O_A	O_A	I_B	I_B	I_B	O_B	O_B	O_B			
24	Double Inverter	I_A	I_A	I_A	I_A	O_A	O_A	I_B	I_B	I_B	I_B	O_B	O_B			
28	Triple Inverter	I_A	I_A	O_A	O_A	I_B	I_B	O_B	O_B	I_C	I_C	O_C	O_C			
29	Triple Inverter	I_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	I_C	O_C	O_C	O_C			
30	Double FF	I_A	O_A	O_A	I_B	O_B	O_B	I_C	O_C	O_C	I_D	O_D	O_D			
31	FF	I_A	O_A	O_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	O_B	O_B			
32	FF	I_A	I_A	O_A	O_A	O_A	O_A	I_B	I_B	O_B	O_B	O_B	O_B			
33	FF	I_A	I_A	I_A	O_A	O_A	O_A	I_B	I_B	I_B	O_B	O_B	O_B			
41	Control Delay	I					I_C	O	O	O	O	O	O			
42	Control Delay	I	I				I_C	O	O	O	O	O	O			
43	Control Delay	I	I	I			I_C	O	O	O	O	O	O			
44	Control Delay	I	I	I	I		I_C	O	O	O	O	O	O			

1604

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
45	Control Delay	I	I	I	I	I	I_C	O	O	O	O	O	O	- 20 V	Ground	+ 20 V
50	Capacitor	I	I	I	I	I	I	I	I	I	I	I	I			
51	Drive Generator	I			I			I			O	O	O			
52	Diverter	O	O	O	O	O	O	O	O		I	I	I			
53	Selector	I_A	I_A	O_A	O_A	O_A	O_A	I_B	I_B	O_B	O_B	O_B	O_B			
54	Current Source	I		I		I		I		I						
55	Inhibit Generator	I_A					O_A	I_B					O_B			
56	Sense Amplifier	M	I		I								O			
57	Sense Amplifier	M	I		I		B						O			
58	Inhibit Generator	I_A					O_A	I_B					O_B			
59	Inhibit Generator	I_A					O_A	I_B					O_B			
60	Output	I_A	I_A	I_A	O_A	I_B	I_B	I_B	O_B	I_C	I_C	I_C	O_C			
61	Input	I_A		O_A	O_A	I_B		O_B	O_B	I_C		O_C	O_C			
62	Output	I_A		O_A		I_B		O_B		I_C		O_C				
63	Line Driver	I				O										
64	Modified Input	I									O					
65	Speaker Driver	I											O			
66	Punch Puller	I											O			
67	Output	I_A	I_A	O_A		I_B	I_B	O_B		I_C	I_C	O_C				
68	Input	I_A		O_A	O_A	I_B		O_B	O_B	I_C		O_C	O_C			
69	Output	I_A		O_A		I_B		O_B		I_C		O_C				
70	Read Amplifier	I		B						O	O	O	O			
71	Tape Preamplifier	I_A	I_B									O_A	O_B			
72	Tape Amplifier	M	I		I								O			
73A	Variable Delay	I	O	O	O	O	O	O	O	O	O	O	O			
74	Tape Current Source	I		I		I		I		I						
75	Reader Level Amplifier	I_A	B_A	O_A	I_B	B_B	O_B	I_C	B_C	O_C	I_D	B_D	O_D			
75A	Reader Level Amplifier Brake	I_A	I_B	I_C	I_D	O_A	O_B	O_C	O_D							
76A	Reader Brake Clutch Driver	I				O		O			O		O			

1604

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
77	Variable Delay	I					O	O	O	O	O	O	O	- 20 V	Ground	+ 20 V
78	Input	I_A	O_A	O_A			I_B	O_B	O_B							
79	Output	I_A		O_A	O_A	B	B	I_B		O_B	O_B	B	B			
80	Long line Receiver, 160	I_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	I_C	O_C	O_C	O_C			
81	Voltage Divider	I	I					O	O	O						
82	Variable Delay	I	O	I	O	I	O	I	O	I	O	I	O			
83	Memory Test	I	I	I	I	O		O	O		I	O	O			
84	Load Simulator	I	I		I	I	O	I	O	I	O	I	I			
85	Magnet Puller	I_A	I_A	O_A		I_B	I_B	O_B		I_C	I_C	O_C	C			
86	Punch Puller	I_A		O_A		I_B		O_B		I_C		O_C				
87	Input	I_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	I_C	O_C	O_C	O_C			
88	Steered FF	I_A	I_A	O_A		O_A	I_A	I_A		I_B	I_B	I_B	O_B			
89	Sheffer Stroke Gate	I_A	I_A	I_A	O_A	I_B	I_B	I_B	O_B	I_C	I_C	I_C	O_C			
90	OR	O	I	I	O	I	I	O	I	I	O	I	I	O	I	I
91	Hammer Storage	I_A	I_A	I_A	I_A		I_B	I_B			G	C	O			
92	Reader Level Amplifier	I_A	I_B	I_C	I_D	O_A	O_B	O_C	O_D							
93	Long Line Transmitter, 160	I_A		O_A		I_B		O_B		I_C		O_C				
94	Long Line Transmitter, 160	I_A	I_A	O_A		I_B	I_B	O_B		I_C	I_C	O_C				
95	Long Line Transmitter, 160	I_A	I_A	I_A	O_A	I_B	I_B	I_B	O_B	I_C	I_C	I_C	O_C			
96	Clock Driver	I_A	O_A	O_A	I_B	O_B	O_B	I_C	O_C	O_C	I_D	O_D	O_D			
97A	Delay	I_A	I_A	I_A	O_A	O_A	O_A	I_B	I_B	I_B	O_B	O_B	O_B			
98	Drive Generator	I_A			I			I_B			O	O	O			
99	Long Line Receiver 160G	I_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	I_C	O_C	O_C	O_C			
101	Amplifier Shaper	I				O	O	O	O	O	O	O	O			
102	Crystal Oscillator, 480KC		O													
103	Crystal Oscillator, 1334.4KC		O													
104	Crystal Oscillator, 1920KC		O													
105	Crystal Oscillator, 240KC		O													
106	Crystal Oscillator, 667.2KC		O													
107	Crystal Oscillator, 960KC		O													

1604

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
108 Long Line Driver, 160G	I_A		O_A		I_B		O_B		I_C		O_C			G	
109 Long Line Driver, 160G	I_A	I_A	O_A		I_B	I_B	O_B		I_C	I_C	O_C		-	r	+
110 Long Line Driver, 160G	I_A	I_A	I_A	O_A	I_B	I_B	I_B	O_B	I_C	I_C	I_C	O_C	20	0	20
111 Current Source	I		I		I		I		I				V	U	V
112 Capacitor (All 0.001 uf)	I	I	I	I	I	I	I	I	I	I	I	I		n d	
114 Sense Amplifier	M	I		I		B						O			
Transistors CDC 118021															
116 Single Inverter	I				O	O	O	O	O	O	O	O			
117 Single Inverter	I	I			O	O	O	O	O	O	O	O			
118 Double Inverter	I_A	O_A	O_A	O_A	O_A	O_A	I_C	O_C	O_C	O_C	O_C	O_C			
119 Triple Inverter	I_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	I_C	O_C	O_C	O_C			
120 Flip Flop	I_A	I_A	I_A	O_A	O_A	O_A	I_C	I_C	I_C	O_C	O_C	O_C			
121 Transmitter	(I				-O	+O)	(I				-O	+O)			

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
						DISC FILE											
P01	Read Switch	I_A				O_A	O_A	I_A			O_C	O_C					YC2231201
P02	Sense Amplifier-Preamplifier	I	GND	I									O				YC2231202
P03	Sense Ampl. Pk. Dct. and Pulseformer	I															YC2231203
P04	Threshold Detector	I					O										YC2231204
P05	Head Equalization Network	I	I			O	O										YC2231205
P06	Current Source																YC2231206
P07	Head Switching Diodes																YC2231207
P08	Driver	I						I									YC2231208
P09	Current Source Dummy																YC2231209
P10	Head Switch	I	I	I	I	I											YC2231210
P11	Gated Pulse Amplifier																YC2231211
P12	Transformer																YC2231212
P13	Delay	I_A	O_A	I_B	O_B	I_C	O_C	I_D	O_D	I_E	O_E	I_F	O_F				YC2231213
P14	Transmitter	I_A				O_A	O_A	I_C				O_C	O_C				YC2231214
P15	Transmission Line Terminal																YC2231215
P16	Receiver	I_A	I_A	O_A	O_A	O_A	O_A	I_C	I_C	O_C	O_C	O_C	O_C		GND		YC2231216
P17	Solenoid Termination														GND		YC2231217
P18	Voltage Protection												$+40_L$	N.C.	GND	N.C.	YC2231218
P19	Single Inverter	I	I	I	I	I	I	O	O	O	O	O	O				YC2231219
P20	Osc. and Ampl. Buffer																YC2231220
P21	Terminator																YC2231221
						LINE PRINTER											
P51	Memory Driver	I	I	I	I		O						Cap. GND				YC2231251
P52	Memory Diverter	I	I	I	I	O	O	O	O	O	O	O	O				YC2231252
P54	Power Supply Filter and Jump.										I	I	I	I	I	I	YC2231254
P55	Power Supply Filter and Jump.												I				YC2231255
P56	Sense Amplifier	I_A	I_A	O_A	I_B	I_B	O_B	I_C	I_C	O_C	I_D	I_D	O_D				YC2231256

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
						LINE PRINTER											
P91	Hammer Driver	J				J		J									YC2231291
P92	Hammer Driver			O	O	J		J	J		I	O	O				YC2231292
P93	Pulse Shaper		I_A	O_A	O_A		I_B	O_B	O_B		I_C	O_C	O_C				YC2231293
P94	Ribbon Advance	O	O							I							YC2231294
P95	Brake-Clutch One-Shot	O	T	T							I						YC2231295
P96	Ribbon Drive and Hold	O	O	I	I		O	O									YC2231296
P97	Hammer Driver One-Shot	I	I										O				YC2231297
P98	Hammer Driver One-Shot																YC2231298
P99	Brake-Clutch One-Shot	I	T	T		OPCONCTR		O	O	O	O	O	O				
E00	Jumper	See Schematic															
E01	Crosspoint Control	See Schematic															YC2071201
E02	Crosspoint Control	See Schematic															YC2071201
E03	Crosspoint Control	See Schematic															
E04	Crosspoint Control	See Schematic															YC2071204
E05	Decoder	See Schematic															
E06	Resistor Assembly	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	YC2071206
E07	Resistor Assembly	I	I	I	I	I	I	I	I	I	I	I	I	I			YC2071207
E08	Single Pulser	I						O	O	O	O	O	O				YC2071208
E10	Integrator	I	I	I	I	I	I	I	I	I	I	I	I	-6v	GND		YC2071210
E11	Delay	I	I	I	I	I	I	I	I	I	I	I	I				YC2071211
E12	Line Driver	I_A	I_A				O_A	I_B	I_B				O_B				YC2071212
E13	Line Receiver	I_A				O_A	O_A	I_B				O_B	O_B				YC2071213
E14	Variable Clock	O_A		J_A		J_A		O_C		J_C		J_C					YC2071214
E15	Line Driver	I_A			O_A			I_B			O_B						YC2071215
E16	Line Receiver																YC2071216
E19	Terminator	I			T_A		T_B		T_C		T_D		T_E				2071219
E20	Resistor Assembly	I	I	I	I	I	I	I	I	I	I	I	I				2071220
E61	Receiver	I_A		O_A	O_A					I_B		O_B	O_B				YC2071261
E62	Driver	I_A		O_A						I_B		O_B					YC2071262
E67	Driver	I_A	I_A	O_A						I_B	I_B	O_B					YC2071267

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
CM00	Universal Matrix																
CM01	Clock Oscillator Amplifier																YC234805
CM02	Bipolar Amplifier																YC234808
CM03	Transmitter Amplifier																YC234811
CM04	Receiver Amplifier																YC234814
CM05	Low Frequency Oscillator																YC234817
CM06	Phase Splitter																YC234820
CM07	Speaker Driver																YC234823
CM08	Frequencey Switch																YC234826
CM09	Volt Phase Splitter																YC234829
CM10	Low Differential Amplifier																YC234832
CM11	Data Line Driver																YC234835
CM12	One Shot Delay																YC234838
CM13	High Differential Amplifier 1																YC234841
CM14	High Differential Amplifier 2																YC234844
CM15	Low Differential Amplifier																YC234853
CM16	High Differential Amplifier																YC234856

MICROWAVE

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
M01	Bipolar Threshold Amplifier																YC234402
M02	Wideband Amplifier																YC234406
M03	Transmitter																YC234410
M04	Receiver																YC234414
M05	Call Circuit																YC234418
M06	Filter																YC234422
M07	Filter																YC234426
M08	Equalizer																YC234429
M09	Delay Card																YC234433
M10	Clock Oscillator																YC234437
M12	Single Inverter																YC234445
M62	Output																YC234449
M63	Line Driver																YC234453
M64	Line Receiver																YC234456
M73	Delay																YC234459

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
CC10	Relay	I	O	O	O			I	O	O	O			*	*	*	
CC21	Inverter	I	O	O	O	O	O	I	O	O	O	O	O				
CC21A	Inverter	I	O	O	O	O	O	I	O	O	O	O	O				
CC22	Inverter	I	I	O	O	O	O	I	I	O	O	O	O				
CC22A	Inverter	I	I	O	O	O	O	I	I	O	O	O	O				
CC23	Inverter	I	I	I	O	O	O	I	I	I	O	O	O				
CC23A	Inverter	I	I	I	O	O	O	I	I	I	O	O	O				
CC25	Inverter	I	O	O	I	O	O	I	O	O	I	O	O				
CC25A	Inverter	I	O	O	I	O	O	I	O	O	I	O	O				
CC31	Flip Flop	I	O	O	O	O	O	I	O	O	O	O	O				
CC31A	Flip Flop	I	O	O	O	O	O	I	O	O	O	O	O				
CC32	Flip Flop	I	I	O	O	O	O	I	I	O	O	O	O				
CC32A	Flip Flop	I	I	O	O	O	O	I	I	O	O	O	O				
CC33	Flip Flop	I	I	I	O	O	O	I	I	I	O	O	O				
CC33A	Flip Flop	I	I	I	O	O	O	I	I	I	O	O	O				
CC35	Dual FF	I	O	O	I	O	O	I	O	O	I	O	O				
CC35A	Dual FF	I	O	O	I	O	O	I	O	O	I	O	O				
CC61	Input	I		O	O	I		O	O	I		O	O				
CC62	Output	I		O		I		O		I		O					
M62	Output	I		O		I		O		I		O					
CC64	Input	I		O	O					I		O	O				
CC82-1	Delay 6 usec	O	O	O	O	O	O	O	O	O	O	O	O				
CC82-2	Delay 25 usec	O	O	O	O	O	O	O	O	O	O	O	O				
CC82-3	Delay 120 & 545 usec	O		O		O		O		O		O					
CC82-4	Delay 3, 5 & 11 usec	O	O	O	O	O	O	O	O	O	O	O	O				
CC82-5	Delay 27 & 54 usec	O		O		O		O		O		O					

* Unless otherwise noted: pin 13 equals -20v; pin 14 equals ground; pin 15 equals +20v.

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
CC82-6	Delay 0.15 & 0.35 usec	O	O	O	O	O	O	O	O	O	O	O	O	*	*	*	
CC82-7	Delay 1 and 2 usec	O	O	O	O	O	O	O	O	O	O	O	O				
CC82-8	Diode Limiter and Delay	I	O			O	O	O	O		O		O				
CC82-9	Diode	O	O	O	O	O	O	O	O			I					
CC82-10	Jumper	←	—	*	—	*	—	*	—	*	—	*	—				
CC82-11	Delay	G	I				O										
CC83	Adjustable Delay	I	O	O		C		I	O	O		C					
CC100A	Push-Pull Amplifier	I		I								O	O				
CC100B	Rectifier	I							O								
CC100C	Phase Shifter	I				O	O	O	I	O	O	O	O				
CC100D	Modulator	I			I					I	O	O					
CC101	Class "A"		I	I	O	O				I	I	O	O				
CCLR	Relay/Lamp Driver	I		O		I		O		I		O					
P01	Read Switch	I		Sig. I	Sig. I	Sig. O	Sig. O	I	Sig. I	Sig. I	Sig. O	Sig. O	+40				
P02	Sense Amplifier	I	Gnd	I									O				
P03	Sense Amp., Pk. Det. and Pulse Former	Sig. I					Gate O					Sig. O	Sig. O				
P04	Threshold & Coin. Det.	Gate I	Sig. I	Sig. I		O	O	O	O	O	O	O	O				
P05	Head Equalization	O	O			I	I						+40				
P06	Current Source	O	O	O							O	O	O				
P07	Head Switching Diodes	O	Gnd	O	I	I	I	I	I	I	I	I	Gnd				
P08	Driver	Gate I					Write Curr. O	Write Curr. Source				Write Curr O	Write Curr. Source				
P09	Current Source Network	Gate I					Curr. O	Gate I					Curr. O				
P10	Head Switch	I	I	I	I	I			O	O	O	I	+40				
P11	Gated Pulse	Sig. I	Gate I	O	O	O	O	Sig. I		O	O	O	O				
P18	Voltage Protection	O	O	O	O	O	O	O	O				+40				

* Unless otherwise noted: pin 13 equals -20v; pin 14 equals ground; pin 15 equals +20v.

PERIPHERAL EQUIPMENT GROUP LOGIC CARD INDEX

	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
ABA	46278200 46278300 46278400	Relay Puller (special for opcon)	Logic "0" Logic "1"	-36V OFF 0.5V at .6A	2 circuits For terminations to -36V or less.
ACA	46514601 46514701 46514801	Photocell Amp. (Card Reader)	Photocell (-) Photocell (+)	OFF -1/4V at 10 MA	3 circuits/card
ADA	50000400 50000500 50000600	Hammer Driver (Printer)	Logic "0" Logic "1"	-1V at 10A -36V OFF	5% max. duty cycle For terminations to -36V or less.
ADB	50000400 50000501 50000601	Hammer Driver (Printer)	Logic "0" Logic "1"	-1V at 6A -36V OFF	ADA Version 2 2% max. duty cycle
ADC	50000402 50000502 50000602	Hammer Driver (501 Printer)	Logic "0" Logic "1"	-2V at 5A -36V OFF	4% max. duty cycle For terminations to -36V or less. Being replaced by ADF
ADD	50000402 50000503 50000603	Hammer Driver (Printer)	Logic "0" Logic "1"	-1.5 V at 7A -36V OFF	ADC with Zener Suppression Emergency fix for Anelex head. Fuse drop is additional. Use ADG for future design.
ADE	50000404 50000504 50000604	Hammer Driver (Printer)	Logic "0" Logic "1"	-1.5V At 7A -36V OFF	ADD with fwd. drop spec and echo check resistor Being replaced by ADG
ADF	Design Underway	Hammer Driver (501 Printer)	Logic "0" Logic "1"	-2V @5A -36V OFF	ADC with 2.2K instead of 6.8K input termination to -20V
ADG	Design Underway	Hammer Driver (501 Printer)	Logic "0" Logic "1"	-1.5V @7A -36V OFF	ADE with 2.2K instead of 6.8K input termination to -20V
ADH	50000407 50000507 50000607	Clutch Driver (501 Printer)	Logic "0" Logic "1"	-1.6V @15A -40 V OFF	Requires space of 2 standard cards due to heat sink

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
AEA	50003400 50003500 50003600	Output Driver (OEM Tag Tape for NCR)	Logic "0" Logic "1"	-8V Clamp -1V at 85MA	3 circuits Not for production use AEB below
AEB	50005800 50005900 50006000	Output Driver (OEM Mag. Tape for NCR)	Logic "0" Logic "1"	-8V Clamp -1V at 85MA	3 Circuits Requires external line termination
AFA	50007900 50008000 50008100	Delay Card (Mag. Tape)	Logic "0" Logic "1" Enable -15V	Logic "0" delayed Logic "1" Selects potentiometer	1 - 50 μsecs delay. Enable input Matches AGA output
AFB	50007900 50008001 50008100	Delay Card (Mag. Tape)	Logic "0" Logic "1" Enable -15V	Logic "0" delayed Logic "1" Selects potentiometer	1 - 50 μsecs delay on "0" Improved AFA
AGA	50004900 50005000 50005100	Selector (Mag. Tape)	Logic "0" Logic "1"	-15V @ 25MA 0V OFF -15V Ref @25MA	3 circuits Delay group selector for AFA/AFB
AHA	50010000 50010100 50010200	Driver Flip-Flop (Optical Reading Machine)	Shift =+12V pulse Enable = -1V Disable = -12V	Set= -12V @20MA Clear= -1V @ 20MA	Flip-Flop for single rank shift register and matrix driver Use AIA driver. Drawings at Rabinow.
AHB	Obsolete	Use AIA circuit			
AHC	50010001 50010101 50010200	Driver Flip-Flop (Optical Reading Machine)	Shift = +12V pulse Enable= -1V Disable= -12V	Set= -12V @ 20MA Clear = -1V @ 20 MA	Low Cost version of AHA Design at Rabinow Drawings at Rabinow

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
AIA	50010300 50010400 50010500	Shift Driver (Optical reading machines)	"0" -1/2V "1" -3V "1" = -5.5 to -16V	-12V @ 45MA -3/4V @25MA -1V @70MA	3 circuits with 3.3K input resistor. Requires -12V Zener clamp.
AIB	50010301 50010401 50010500	Shift Driver (Optical reading machines)	"0" -1/2V "1" -3V "1" = -5.5 to -16V	-12V@ 45MA -3/4V @25MA -1V @ 70 MA	Low cost version of AIA Design at Rabinow
AJA		Photocell AMP			
AKA	50010900 50011000 50011100	Photocell Amp (350 PTR)	Photocell (+) Photocell (-)	-1/4V @10MA OFF	3 circuits
ALA	50011200 50011300 50011400	Power Supply (807/808 File, Function Generator)	60 cps 40V rms Center-tapped	+9.1V @-0-18 MA -9.1V @0-18 MA	Operates from 60 cps transformer
AMA	Obsolete				USE AMB, AMC, AMD, or AME
AMB	50011501 50011601 50011701	Erase/Write Driver (852 disk Drive)	Logic "0" Logic "1"	0V OFF 100 ma @+30V each ckt	2 circuits, only one on at a time. +40V on pin 15. Drives toward + only
AMC	50011502 50011602 50011702	Erase/Write Driver (853 Disk Drive)	Logic "0" Logic "1"	0V OFF 150 ma @ +35V Each Ckt	Similar to AMB
AMD	50011501 50011603 50011703	Write Driver (807/8 Disk File)	Logic "0" Logic "1"	0V OFF 125 ma @+35V Each ckt	Similar to AMB and AMC
AME	50011501 50011604 50011704	Erase Driver (807/8 Disk File)	Logic "0" Logic "1"	0V OFF 500 ma @ +16V each ckt	2 circuits. Both should be on at the same time. Drives toward + only.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
ANA	50011800 50011900 50012000	Head Select & write error check (852 & 853 disk drive)	1) 4 ma toward gnd @+40V for each head select on; 2) +30V to +35V from Erase/Write Drivers	Logic "0" Logic "1"	+40V on pin 15
ANB	50011800 50011901 50012001	Head Select & Write Error Check (807/8 Disk File)	1) +35V from write driver; 2) 0.4 ma toward gnd for each Head Select on	1) Logic "0" Logic "I" 2) +22V for AOA card	+40 on pin 15. Used with AOA
ANC	50011800 50011902 50012002	Erase Error Check (807/8 Disk File)	+16V from Erase Driver	Logic "0" Logic "1"	Used to check AME
AND					
AOA	50012100 50012200 50012300	Head Select Check (807/8 Disk File)	1) +16V from each Head Select turned on 2) +22V from AOA	0.4 ma toward gnd for each Head Select on	+40V on pin 15. Used with ANB.
APA					
AQA		Input Amplifier Output Amplifier	+0.5V -0.5V Logic "0" Logic "1"	Logic "0" Logic "1" +1½V OFF -3½V at 50 MA	1 circuit - matches IQA 1 circuit - matches OPA Drives toward - only Requires -4V on Pin 7
ARA	Design Underway	Driver Flip-Flop (Optical Reading)	Shift= +12V pulse Enable= -1V Disable= -12V	Set= -12V at 100 MA Clear=-1V at 100 MA	Higher drive than AHA Requires -12V power
ASA	50013301 50013400 50013500	Quantizer - Output amplifier (Optical Reading)	|Analog| > |Ref|** |Analog| < |Ref| |Analog| > |Ref|	OV OFF * +2V at 17MA +3V at 15MA	3 circuits, Matches OSB *Includes internal 120 termination to ground. Reference range -1 to -10V. Analog range -½ to -15V

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
ATA	50013600 50013700 50013800	Gated Read Amplifier (852 Disk Drive)	1) 5mv p-p 1 mc analog 2) +8V gate input	Analog	Requires +12V on pin 15 -12V on pin 13 Adjustable gain
ATB	50013600 50013701 50013801	Gated Read Amplifier (853 Disk Drive)	1) 5mv p-p 1 mc analog 2) +8V gate input	Analog	Requires +12V on pin 15 -12V on pin 13 Adjustable gain
AUA	50013900 50014000 50014100	Power Supply Regulator (807/808 File, Operational Amplifier)	+20VDC -20 VDC	+15 VDC @ 0-30 MA -15 VDC @ 0-30 MA	Two +15V Circuits Two -15V circuits
AVA	50014200 50014300 50014400	Write Resistor Diode Card (807/8 Disk File)	0 to +35V	Input via 275Ω & Series diodes to drive mag. head	Two complete circuits each with four isolating diodes Input matches AMD etc.
AWA	Not to be released	Voltage sensor- Relay Puller (807/8 Disk File)	No external inputs (Monitors Power Supply Voltages)	OV out if voltages are not too close to OV. Open if voltages are too close to OV.	Three outputs, +40V on Pin 12
AXA					
AXB					
AYA	50015100 50015200 50015300	Voltage Check (852/3 Disk Drive)	1) Logic (Pin 1) 2) +20V supply via 17.6V Zener (Pin 2)	1) Logic 2) 0.8A at +1.0V	+40V on pin 15. Used with GAA Card. Pin 2 Input matches GAA circuit
AZA					

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comment
BAA	50058300 50058400 50058500	Voltage Sensor (807/8 Disk File)	1) +20V supply via 17.6V Zener (Pin 1) 2) Logic, Pin 2	1) Logic 2) On = +0.2V OFF = open	+20V or +40V on pin 15. Pin 1 Input Matches GAA pin 11 Pin 2 Input Matches BAB pin 11 or 12 Pin 7 Output Matches BBA, Pin 1
BAB	50058300 50058401 50058501	Voltage Sensor (807/8 Disk File)	+20V Supply Via 17.6 Zener	1) Logic	Input Matches GAA pin 11 Output matches BAA Pin 2.
BBA	50058600 50058700 50058800	Voltage Sensor Amplifier (807/8 Disk File)	ON = +0.2V OFF = Open	ON - 200 MA to Gnd OFF Gnd	+20V or +40V on Pin 15 Input matches BAA Pin 7 Output to six BCA's, Pin 1. Pin 10 via external 120Ω to +20V or +40V
BCA	50058900 5005900 0 50060000	Erase/Write Current Sink (807/8 Disk File)	ON = +16V OFF = Ground	OFF ON = 0.8A @ +1.0V	+20V or +40 V on Pin 15 Input matches BBA Pin 12.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EDA	46278500 46278600 46278700	Read Level Detector (Mag.Tape)	40MV p-p 40 KC	1. Class A 2. Rect. (positive) 3. Logic "1" (level detection)	Preamp, etc. #1 for Mag.Tape
EEA	46281200 46281301 46281101	Resistor Termination (Mag.Tape)	Res.Term.	Res.Term	6.8K to -20V Pins 1-12
EEB	46281200 46281302 46281102	Capacitor Termination (Mag.Tape)	Cap.Term.	Cap. Term.	1000 pf Pins 1-2 2000 pf Pins 3-8 10,000 pf Pins 9-12
EEC	46281200 46281303 46281103	Cap. Termination (Mag.Tape)	Cap.Term.	Cap. Term.	3.3 mfd Pins 1-2 6.8 mfd Pins 3-8 15 mfd Pins 9-12
EED	46281200 46281304 46281104	Resistor Term. (Mag.Tape)	Res. Term.	Res. Term.	680 ohms to -20V pins 1-12
EEE	46281200 46281305 46281105	Capacitor Termination (Mag.Tape)	Cap.Term	Cap. Term	220 pf Pins 1-12
EEF	46281200 46281306 46281106	Resistor Term (Mag. Tape Exerciser)	Res. Term	Res. Term	120 ohms to gnd. Pins 1-12
EEG	46281200 46281307 46281107	Resistor Term (Disk Drive)	Res. Term.	Res. Term.	510 ohms to +20V Pins 1-12

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EEJ					
EEK	46281200 48304100 48304000	Resistor Term (915 Page Reader)	Res. Term.	Res.Term.	560 ohms to +20V Pins 1-12 Drawings @ Rabinow
EEL	46281200 48302900 48302800	Capacitor Term (915 Page Reader)	Cap.Term.	Cap. Term.	1 mfd Pins 1-3 1.5mfd Pins 4-6 2.2 mfd Pins 7-9 3.3 mfd Pins 10-12 Drawings @ Rabinow
EEM	46281200 48302600 48302700	Resistor Term (915 Page Reader)	Res. Term.	Res. Term.	10K to -20V Pins 1-12 Drawings @ Rabinow
EEN					
EEO	46281200 48303100 48303000	Capacitor Term (915 Page Reader)	Cap.Term.	Cap.Term.	2.2 mfd Pins 1-3 4.7 mfd Pins 4-6 22 mfd Pins 7-9 180 mfd Pins 10-12 Requires two card spaces Drawings @ Rabinow

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EFA	46529001 46529101 46529201	Clock Amplifier (Card Reader)	400-1200 MV P-P, 40KC	Std. Logic	Signal from Magnetic Pick-up
EGA	50001000 50001100 50001200	Read Level Detector (Mag.Tape)	20 -40MV p-p 40KC	1. Class A 2. Rect (positive) 3. Level Detect Std. logic "1" (level detection)	Preamp etc. #2 for Mag.Tape Not for future use. Use EH.. and E.. in combination.
EHA	50002801 50002901 50003001	Read Pre-amp (Mag.Tape)	10 -50MV p-p 60 KC	Balanced Class A 8V p-p Each side	Preproduction EHB Not for design use.
EHB	50008500 50008600 50008700	Read Pre-amp (Mag.Tape)	8-40MV p-p 60KC	Balanced Class A 8V p-p each side	Preamp for Mag.Tape
EHC	50008501 50008601 50008701	Read Pre-amp (Mag.Tape)	10 -50MV p-p -30KC	Balanced Class A 8V p-p Each side	EHB with high freq. roll off.
EHD					
EIA	50003101 50003201 50003301	Read Level detector (Mag.Tape)	8V Diff. Class A	1. Rect (-8V neg) 2. Enable (non-std)	Preproduction EIB
EIB	50009100 50009200 50009300	Read Level Detector (Mag. Tape)	8V Diff. Class A	1. Rect (-8V neg) 2. Enable (non-std)	Rectifier & level Detector for Mag.Tape
EIC	Design Hold	Read Level Detector (Mag.Tape)			

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EID	50009102 50009202 50009302	Read Level Detector (Mag.Tape)	8V Diff. Class A	1. Rect (-8V neg) 2. Enable (non-std)	Lower Frequency EIB for 36-75 ips.
EIE	50009103 50009203 50009302	Read Level Detector (Mag.Tape)	8V Diff. Class A	1. Rect (-8V neg) 2. Enable (non-std)	EID with high freq. roll-off
EIF					
EJA	50003700 50003800 50003900	Read Level Detector (852 Disk Drive)	1) 3V p-p 1 mc Class A 2) Reference Voltage	1. Rect (-7V neg) 2. Enable (non-std)	Rectifier & level detector for disk storage drive Reference volts determines threshold
EKA	Not released	Dual Pre-amp (626 Experimental tape unit)	10-50MV p-p 120KC	Balanced Class A	2 circuits, 1 stage of gain
ELA	Not released	Pre-amp (626 experimental tape unit)	200-1000 MV p-p 120 KC	1. Balanced Class A 2. Level Enables (non-std)	Amp & level Detector for Phase modulation (pre-production)
EMA	50004600 50004700 50004800	Pre-amp (601 Mag Tape - Obsolete Analog interface)	10-25MV 15 KC	1. Gated, Balanced Class A 0.3V p-p 2. DC Deskew voltage	Single Stage gain plus Provision for remote control of read-write deskew. Obsolete
EMB	Not released				Similar to EMA with high freq. roll off. Obsolete
ENA	50009400 50009500 50009600	Photocell amp (350 PTR)	Photocell - Photocell +	OFF -1/4 V @ 10MA Compensated bias source	Photocell amp for feedhole 1 circuit Obsolete
ENB	50042500 50042600 50042400	Photocell amp (350 PTR)	Photocell - Photocell +	OFF -1/4 V @ 10MA Compensated bias source	Photocell amp #2 for feed-hole 1 circuit Obsolete

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EOA	50015700 50015800 50015900	Class A amp & D-C Separator			Obsolete version EOB
EOB	Design Hold	Class A amp & D-C separator (601 Mag. Tape Analog interface)	15 KC 0.3V p-p	1. Balanced Class A 2. D-C voltage for read deskew	Separates 15 KC signals & DC Deskew voltage
EOC	Design Hold	ditto	ditto	ditto	EOB with high freq. roll off.
EPA	50016000 50016101 50016201	Potentiometer card (Mag.Tape)	Class A	Gain Controls	(7) 500 ohms potentiometers for use with EGA
EQA					
ERA	50016600 50016700 50016800	Solenoid Driver (601 Mag.Tape (power supply)	-1V -16V	-0.8V @ 2 1/4A -20V OFF	Pinch Roller Driver Requires 3 card slots
ESA	50016900 50017000 50017100	Delay control potentiometers 60X tapes	0-½V -16V	-2 to -10V Adjustable -13V OFF	7 potentiometers for delay group selection of voltage controlled delay (UGA, etc)
ETA	Not Released	Differential Amplifier	5MV 2MC	Balanced Class A	Adj gain preamp for phase modulation
ETB	Not Released	Differential Amplifier	1MV 2 MC	Balanced Class A	Like ETA except higher gain.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EUA	50017200 50017600 50017700	Differential Amplifier (852 Disk Drive)	100 mv p-p 1 mc Analog	Balanced Class A	Amp. for magnetic head signals
EUB	Not Released	Differential Amplifier	100 mv p-p 2 mc Analog	Balanced Class A	Use EUC
EUC	50017502 50017602 50017702	Differential Amplifier (853 Disk Drive 807/8 Disk File)	100 mv p-p 1 mc Analog	Balanced Class A	Used with EWA/B Higher gain and lower output impedance than EUA
EVA	50017800 50017900 50018000	Gated, Strobed Receiver-Flip-Flop (807/8 Disk File)	1) Complementary rectangular waves 0.5V at 0V & Gate =0V & strobe = Logic"0" 2) Gate = -7V 3) Strobe = Logic "1"	1) Standard logic Flip-flop follows complementary inputs 2) Jammed to logic "0" 3) Flip-flop stays in last state	No AND diodes on output
EWA	50018100 50018200 50018300	Shaper (853 Disk Drive)	3V p-p 1 mc Analog	Differential 0.6V rectangular waveform referenced @ +8V.	Output changes state when input polarity reverses.
EWB	50018100 50018201 50018301	Peak Detector (807/8 Disk File)	3V p-p 1 mc analog	0.6V Square wave Referenced to +8V	Output changes state when input polarity reverses
EXP	46267000 No Assy No Schematic				Experimental Blank for Breadboard use
EYA	Design Hold				
EZA	50019000 50019100 50019200	AGC Attenuator (852 Disk Drive)	1) 100 mv p-p 1 mc Analog 2) Attenuation Control Signal (+1V to -1V)	Output is input attenuated up to 20 db	Used with FYA Requires +12V on pin 15 - 12V on pin 13

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
FAA	Not Released				Obsolete. Use FAB circuit
FAB	50034601 50034701 50034801	Shaper Flip-Flop (807/8 Disk File)			Logic Outputs have no AND diodes. Used with EWB
FBA	Not to be released	Voltage Limiter for Servo Valve Amp Input (807/8 Disk File)	Analog Signal with 0-1 ma drive capability	Same analog signal limited at +6.8V and -6.8V	1 Circuit
FCA	50035200 50035300 50035400	Outer Track Select & Summing Network (807/8 Disk File)	3 of 4 inputs at 0V, other input +8, 0, or -8V	0 to 1.1 ma dependent on input combination	Resistor Network for summing current into an operational amp.
FCB	50035200 50035301 50035401	Inner Track Select & summing network (807/8 Disk File)	2 of 3 Inputs @ 0v, 3rd input at +8V or -8V 4th input +8V,0,or-8V	0 to 0.6 ma dependent on Input combination	Resistor Network for summing current into an operational amp
FDA	50035500 50035600 50035700	10 KC Oscillator	None	7V P-P @ 10 KC Regulated	Minimum load resistance =2K

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
FGA	50036400 50036500 50036600	Clamp & Summing + 0.020 inch (807/8 Disk file)	Input pin 1, 2 Logic "0", "1" Logic "1", "0" Logic "0", "0"	-1/8 ma +1/8 ma 0 ma	Requires +8V & -8VDC Reference on pins 3 & 9. Both polorities of output current separately adjustable. Used to sum into op. amp.
FHA	50036700 50036800 50036900	Valve Amplifier (807/8 Disk File)	Analog voltage of ± 6.8V max. @ ± 1 MA max. & Feedback term	Class AB current regulated at about 5 MA	Output used with FMA to drive 30 MA into inductive load.
FIA	50037000 50037100 50037200	10 KC Power Amplifier (807/8 Disk File)	7V P-P from FDA Card & Feedback term	Class AB current regulated at about 5 MA	Output used with FMA to drive 150Ω resistive load to 30V P-P.
FJA	50037300 50037400 50037500	Servo Cycling Generator	Pin 1 - 0V Pin 1 - Open	+10V @ 2.35 K String of pulses 50-100 us wide switched to around @3 MA spaced 100 ms apart.	Used to toggle OLA circuit. Jumper option to space pulses 600 ms apart.
FKA	50037600 50037700 50037800	Demodulator (808/8 Disk File)	Two separate amplitude modulated 10KC signals	D-C difference of demodulated input max output ±1.4 ma.	Output used in summing network at input of op. amp.
FLA	50037900 50038000 50038100	Bridge Rectifier (807/8 Disk File)	10V RMS @ 10 KC	+8V Nom @ 5K -8V Nom @5K (Proportional to Input)	FMA provides suitable input, Output includes compensating diodes for negative feedback loop of op. amp.
FLB	50037900 50038001 50038101	Bridge Rectifier (807/8 Disk File)	10V RMS 10 KC	+8V (No load) -8V (No load) (Proportional to Input)	FMA provides suitable input

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
FMA	50038200 50038300 50038400	Power Amp. Output Stage (807/8 Disk File)	Class AB	Class AB - between +15 and -15VDC 150 Min. Resistive Load 30 MA peak into inductive load.	Current gain only Input matches output of FHA or FIA circuit.
FNA	50038500 50038600 50038700	Retract Inverter & Current Source (807/8 Disk File)	OV, GND Open, -3V	-20V @ 43K, pin 6 Logic "1", pin 12 OV @ 33K, pin 6 Logic "O" pin 12.	Pin 6 intended to drive current summing network for operational amp.
FOA	50038800 50038900 50039000	Feedback Function Generator (807/8 Disk File)	Position Op. Amp (+10V to -10 VDC) & + VDC Floating Power Supply.	Non-linear current feedback	Special network for FSA circuits Floating power supply on input satisfied by ALA.
FOB	50038800 50038901 50039001	Feedback Function Generator (807/8 Disk File)	Position Op. Amp (+10V to -10 VDC) & -VDC Floating Power Supply	Non-linear current feedback	Special Network for FSA circuit. Floating power. Supply on input satisfied by ALA
FPA	50039100 50039200 50039300	Reference Amplifier (807/8 Disk File)	+9.1V Ref or -9.1V Ref.	-8V @ 0-10 MA or +8V @ 0-10 MA	Input reference available from ALA circuit. Output polarity selected by input connections.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
FRA	50039700 50039800 50039900	Velocity, Acceleration Summing Networks (807/8 Disk File)	1. Velocity sensors 2. Velocity Op. Amp. 3. Acceleration Op. Amp.	Summation of Input 1 & 2. Summation of input #2 after differentiation and Input #3.	Special Network for FSA circuit
FSA	50040000 50040100 50040200	Operational Amp. & Booster Amp. (807/8 Disk File)	Low-level signals (Summation of Input & Feedback Signals)	High gain Class AB reproduction of input over +10V to -10V range into 150 Ω min load.	One side of differential input may be grounded for single-ended signals.
FTA	50040300 50040400 50040500	Velocity Summing Networks (807/8 Disk File)	1. Velocity Signal 2. Velocity Op. Amp.	Summation of Input 1 & 2	Special Network for FSA circuit with 2:1 range of gain adjustment.
FUA	50040600 50040700 50040800	Position, Velocity Acceleration Summing Networks (807/8 Disk File)	1. Velocity signal 2. Acceleration signal 3. Summing Op. Amp 4. Short Stroke Op.Amp 5. On point Op. Amp.	Summations of Inputs as follows: a. Inputs 1,2,3,4 b. Input 4 c. Input 4,8,5	Special Network for FSA circuit with gain adjustment on Input 2
FVA	50040900 50041000 50041100	Position & Acceleration Network (807/8 Disk File)	1. Long Stroke Displacement. 2. Long Stroke Displacement Op. Amp. 3. Acceleration 4. Function Gen Op. Amp. 5. Sum of 2 & 3	Summation of inputs: a. Inputs 2,3 & 4 b. Inputs 2 & 3 c. Inputs 2 & 4 d. Inputs 2,3,4	Special network for FSA circuit. Gain adjustment on inputs 3 & 4
FWA	50041200 50041300 50041400	Temperature Servo. Amp. (807/8 Disk File)	Thermistor 1.5K @ 92°F.	Half wave 60 cycle sine wave current 150 ma peak. Open circuit voltage of 40V peak supplied by motor shading coils.	Output connects to shading coils on shaded pole motor. Class "B" operation of output Transistors causes CW or CCW variable speed operation.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comment
FXA	50041500 50041600 50041700	Gated Read Amplifier (807/8 Disk File)	1) 5 mv p-p 1 mc Analog 2) +8V gate	Analog	Can be gated on and off with electronic gate signal, or jumpered on.
FYA	50041800 50041900 50042000	AGC Rectifier (852 Disk Drive)	1) Rectified Analog (-7V) 2) AGC Disable - Std Logic	Attenuation Control Signal (+1V to -1V)	Used with EZA
FZA	50042100 50042200 50042300	Gated Line Driver (853 Disk Drive)	Complementary 0.6V Rectangular waves @ +8V & Gate = Logic "1" Gate = Logic "0"	+2V, 200 ns pulse for each change of rectangular wave input OFF - 0V	120Ω output terminating resistor. Input 1) matches EWA.

Type	Card Blanks Comp. Schematic	Applications	Input	Output	Comments
GAA	50050500 50050600 50050700	Isolated Diode Cards (852/3 Disk Drive 807/8 Disk File)	Cath. of Diodes	Anode of Diodes +20V Via 17.6V Zener	4 isolated 0.3A Silicon Diodes on pins 1-8. Zener output on pin 11 matches input to AYA, BAA, or BAB.
GBA	50050800 50050900 50051000	Clutch Pre-Driver (350 Paper Tape Reader)	-6.0V 0V	Pin 7 = OFF, -7V Pin 5 =-V@125 MA Pin 7 =-0.5V@125MA Pin 5 = OFF, -7V	Pin 10 & 12 biased to switch external output drivers when pin 5 & 7 are each returned to -25V via 200Ω Similar to 76A
GCA	50051100 50051200 50051300	500 Cycle Twin "T" Notch Network (807/8 Disk File)	0 to ±10 VAC max. (servo acceleration signal)	No load output voltage equals input except near null	3 db down at 450 & 550 cps. 40 db down @ 500 cps when used with Op. Amp.
GCB	5005100 50051201 50051301	Variable Freq. Twin "T" Notch Network (807/8 Disk File)	0 to ± 10 VAC max. (Servo acceleration signal)	No load output voltage equals input except near null	40 db down point adjustable from 350-800 cps, 3 db points about 100 cps apart when used with op. amp.

Type	Card Blanks Comp. Layout Schematic	Application	Input	Output	Comments
HAA	48303600 48303700 48303800	Resistor Term (915 Page Reader)	Res. Term.	Res. Term.	680Ω to gnd. Pin 1,2 1K to gnd. Pin 3 2.2K to gnd. Pin 4,5 3.3K to gnd. Pin 6-8 Network Pin 10-11 4.7K to +20V Pin 12 Drawings at Rabinow

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
IAA	46245300 46241600 46244500	Relay Puller (Mag.Tape)	Logic "0" Logic "1"	-36V OFF - 0.6 V @ .6A	Slow Speed Driver for -3 to -36V terminated loads
IAB	50009700 50009800 50009900	Relay Puller (Mag.Tape)	Logic "0" Logic "1"	-36V OFF - 0.6V @ .5A	Derated IAA Use IAA in new designs
IBA	46245200 46241400 46244200	Power EF(+20V) (Mag.Tape)	Logic "0" Logic "1"	- 0.6V @ 0.6A +14V OFF	Special capstan Driver for +14V or less terminated loads
ICA	41060300 41060400 41060500	Driver Double Inv. (180 D C)	Logic "0" Logic "1"	0.6V @ 0.4A -60V OFF	Stepper Motor Driver 2 circuits Not currently in production.
IDA	46500000 46500100 46500200	D/A Converter (Display)	Std.Logic	Analog	Pre-Production only
IEA	46500300 46500400 46500500	D/A Converter (Display)	Std. Logic	Analog	Pre-Production only
IFA	46500600 46500700 46500800	D/A Converter (Display)	Std.Logic	Analog	Pre-Production only
IGA	46500900 46501000 46501100	Character Size (Display)	Std.Logic	Analog	Pre-Production only
IHA	46501200 46501300 46501400	Character Size (Display)	Std.Logic	Analog	Pre-Production only
IIA	46281400 46281500 46281600	Head Driver (Mag.Tape)	Logic "0" Logic "1"	-20V OFF -1V @ 160 MA	Similar to 55 card

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
IJA	50001600 50001700 50001800	Power Flip-Flop (Mag.Tape)	Logic "0" Logic "1" Logic "0" Logic "1"	Logic "0" Logic "1" -20V OFF -0.6V at 160MA	1 circuit 2 "OR" inputs Input/output pertains to 1 side - set or clear.
IKA	50001900 50002000 50002100	Output amp. (OEM Mag Tape for WU/RCA)	Logic "0" Logic "1"	+13V at 70MA -3V at 15MA	2 circuits for coax line (Matches OKA Receiver)
ILA	50002200 50002300 50002400	Voice Coil Driver (Mag.Tape)	Logic "0" Logic "1"	+0.6V at 1½A +14V OFF	2 circuits for terminations to +14V or less
IMA	Design Hold	Quadruple Driver			
INA	50005200 50005300 50005400	Line Driver (OEM Mag. Tape for West. Elect.)	Logic "0" Logic "1"	-6V at 30 MA -0.6V at 25 MA	3 circuits Coax Line Driver (Matches OIA)
IOA	Design Hold	Head Selection (mass Memory)	Logic "0" Logic "1"	OFF +0.4V at .1A or +.6V at 1.5A*	Obsolete, Use IOB
IOB	50019301 50019401 50019501	Head Selection (807/8 Disk File 852, 853 Disk Drive)	Logic "0" Logic "1"	OFF +0.4V at 0.2A +0.6V at 1.5A*	2 circuits, Only 1 circuit should be on at a time. For terminations to +40V or less *Requires external 180Ω to +20V
IOC	50019301 50019402 50019501	Head Selection (852/3 Disk Drive) (807/8 Disk File)	Logic "0" Logic "1"	OFF +0.4V @ 0.2A +0.6V @ 1.5A* +0.5V @ 0.5A**	IOB with less leakage current. *Requires ext. 180Ω to +20V **Requires ext 550Ω to +20V

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
IPA	50019600 50019700 50019800	Line Driver (Mag.Tape Exerciser for Mitsubishi)	Logic "0" Logic "1"	0V OFF -1.8V at 30MA	3 circuits (Matches OPA) 120 OHM termination jumper option.
IQA	50019900 50020000 50020100	Line Driver (OEM Mag.Tape for Mitsubishi)	Logic "0" Logic "1"	+E OFF -1.5V to + E at 8MA	3 circuits, Matches OQA Output is 8MA constant current to external termination.
IQB	Design Hold				
IRA					
ISA	Not Released	Line Driver (601 Daisy Chain)	Logic "0" Logic "1"	0V OFF +2.0V at 34MA or +3.0V at 30MA	3 circuits Matches OSA, OSB 120 ohm termination jumper option.
ISC	50020502 50020602 50020702	Line Driver (601 Daisy Chain)	Logic "0" Logic "1"	0V OFF +2.0V at 34MA or +3.0V at 30MA	Improved ISA, Matches OSA, OSB 120 ohm termination jumper option.
ISD					

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
ITA	50020800 50020900 50021000	Pulse Delay & Line Driver (601 Daisy Chain)	Logic "1" pulse	+2.0V at 34MA Pulse delayed	Pins 1-8 same function as UGA Pins 10-12 same as ISA, ISC Matches OSA, OSB. Obsolete. Use ITB in new designs.
ITB	50020801 50020901 50021001	Pulse Delay & Line Driver (601 Daisy Chain)	Logic "1" pulse	+2.0V at 34 MA Pulse delayed	Obsolete. Use ITD
ITC	50020800 50020902 50021002	Pulse Delay & Line Driver (601 Daisy Chain)	Logic "1" pulse	+2.0V @ 34 MA Pulse delayed	Supersedes ITA with improved temp characteristics. Use ITD in new designs.
ITD	50020803 50020903 50021003	Pulse Delay & Line Driver (601 Daisy Chain)	Logic "1" pulse	+2.0V @ 34MA Pulse Delayed	Improved production yield over ITA & ITC. Improved temp. char. over ITA & ITB
IUA					
IVA	50021400 50021500 50021600	Gated Oscillator (852 Disk Drive)	Logic "0" & Logic "1"	Logic "0" pulse at 699.5 KC $\pm$0.1% rate	First transition from "1" to "0" occurs within 150 nsec after input goes to ground.
IWA	Design Under-way	Controlled Rise Time amp. & FF (Pluto tapes)	Logic "0" Logic "1" Logic "0" Logic "1"	Logic "0" Logic "1" 0V OFF +3V at 20 ms	1 circuit 2 "or" inputs. Input/Output pertains to 1 side set or clear. Designed for +15V but may use +20V.
IYA	50022300 50022400 50022500	Line Driver (OEM Beckman)	Logic "0" Logic "1"	-12V -½V	3 Circuits, Matches OYA
IZA					

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
JAA JAB JAC	Not to be Released	Speed Detector			JAA, JAB & JAC are being replaced by JAD, JAE & JAF respectively.
JAD	50042702 50042803 50042903	Speed Detector (807/808 Disk File)	80 us Logic "1" Pulses Rep rate 16.7 cps Rep rate 16.7 cps	 -20V OFF -0.6V @ 0.3A	Rep rate of switching point fixed by selected components in manufacture.
JAE	50042702 50042804 50042903	Speed Detector (852 Disk Drive)	50 us Logic "1" Pulses Rep rate 400 cps Rep rate 400 cps	 -20 V OFF -0.5V @ 0.3A	Similar to JAD except for higher rep. rate
JAF	50042702 50042805 50042903	Speed Detector (853 Disk Drive)	.50 us Logic "1" Pulses Rep rate 633 Rep rate 633	 -20V OFF -0.6V @ .3A	Similar to JAD & JAE except for higher rep. rate.
JBA	50043000 50043100 50043200	Positive voltage ref. switch (807/808 Disk File)	+8V Ref Logic "0" Logic "1"	 +0.015V@ 1.1 ma +8.0V @ 1.1 ma	2 Circuits The +8V Ref Input required on pins 5 & 11 matches output of FPA circuit Output matches FCA & FCB circuits
JCA	50043300 50043400 50043500	Negative voltage ref. switch (807/808 Disk File)	+8V ref Logic "0" Logic "1"	 -0.015V @ 1.1 ma -8.0V @ 1.1 ma	2 Circuits. The -8V Ref input required on pins 5 & 11 matches output of FPA circuit. Output matches FCA & FCB circuits.
JDA	50043600 50043700 50043800	Long Stroke - Short Stroke Switch (807/808 Disk File)	Logic "0" & "1" Three inputs	Bidirectional switch to 0V when $V_3+V_2\ \overline{V}_1$ equation satisfied Otherwise output off	Subscripts in equation refer to input pins: Output in off condition should be limited to $\pm$ 10V.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
JEA	Not to be Released				Obsolete, Use JEB
JEB	50043901 50044001 50044101	Tuned Amplifier (807/8 Disk File)	1) Logic 2) Two Complementary Inputs with excursion of 6V	800 KC sine wave, 10 V	

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
OAA	46264200 46264300 46264100	Photocell amp (Mag.Tape)	Solar Cell lighted + Solar Cell dark -	Logic "1" Logic "0"	2 circuits
OAB					
OBA	Obsolete	Peak detector (Mag.Tape)	+ Peak No Peak	Logic "1" Logic "0"	Obsolete Peak Detector Use OGC
OCA	41059700 41059800 41059900	Photocell Pre-amp (180 DC)	Photocell + Photocell -	-3V OFF -½V @ 10MA	2 circuits
ODA	46278800 46278900 46279000	Read Peak Detector (Mag.Tape)	+ Peak No Peak	Logic "1" pulse Logic "0"	40 KC Peak Detector Obsolete after retrofit completed. Use OGC in new design.
OEA	Design Hold	One Second Delay (Card Reader)			
OFA	50002500 50002600 50002700	Input "M" Card (Mag.Tape NCR)	-8V -1V	Logic "0" Logic "1"	3 circuits, external termination to - Matches AEB
OGA	50001300 50001400 50001500	Read Peak Detector (Mag.Tape)	+ Peak Pin 1 - Peak Pin 5 No Peak	Logic "1" pulse Logic "1" pulse Logic "0"	Preproduction OGB Obsolete & not released.
OGB	50008800 50008900 50009000	Read Peak Detector (Mag.Tape)	+ Peak Pin 1 - Peak Pin 5 No Peak	Logic "1" pulse Logic "1" pulse Logic "0"	Peak Detector & Shaper Optional jumpers for lower freq. Use OGC below
OGC	50008801 50008901 50009000	Read Peak Detector (Mag.Tape)	+ Peak Pin 1 - Peak Pin 5 No Peak	Logic "1" pulse Logic "1" pulse Logic "0"	Improved version of OGB
OGD	50008802 50008902 50009002	Read Peak Detector (852 Disk Drive)	+ Peak Pin 1 - peak Pin 5 No peak	Logic "1" pulse Logic "1" pulse Logic "0"	Pulse width 700 ± 100 ns

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
OHA	50006400 50006500 50006600	Peak Detector (OCR and Mag Tape Phase Mod)	No Peak or no enable - Peak Pin 1 or + Peak, Pin 3 + Peak Pin 1 or - Peak, Pin 3	Logic "0" Logic "1" pulse Pin 9, 10 Logic "1" pulse Pin 11, 12	Positive & Negative Peak detector for 120 KC Class A signals
OIA	50006700 50006800 50006900	Line Receiver (OEM Mag.Tape For West. Elect.)	-6V -½V	Logic "0" Logic "1"	Matches INA 3 circuits
OJB	50022901 50023001 50023101	Long term delay (general purpose)	Open -16V 0V	Logic "0" delayed Logic "1"	Delay derived from fixed components. Jumper options from 2 ms to 50 sec.
OKA	50023200 50023300 50023400	Input Amplifier (OEM Mag.Tape for WU/RCA)	-0V +9V	Logic "0" Logic "1"	3 circuits Matches IKA
OLA	50023500 50023600 50023700	Fly back verify Flip-Flop (Printers)	Set = "1" Toggle = -Pulse Clear = "0"	Logic "0" Changes State Logic "1"	1 circuit Operates from ADC or ADE suppression circuit
OMA	50023800 50023900 50024000	High Fanout "M" Card (Printer Echo check)	-16V 0V	Logic "0" Logic "1"	3 circuits Matches "L" Cards Output for setting OLA card
ONA	50024100 50024200 50024300	Photocell Amp (852,853 Disk Drive)	Photodiode lighted+ Photodiode dark -	Logic "0" & "1" Logic "1" & "0"	2 circuits. Each has complementary outputs
OOA	50024400 50024500 50024600	Gated Line Receiver (853 Disk Drive)	Toggle= +2V pulse referenced to 0V & Gate = Logic "0" Gate = Logic "1"	Standard logic Flip-Flop toggles on each 200 ns pulse Jammed to logic "0"	Input pulse from line has 0 to +2V excursion from ISC circuit No "AND" diodes at output
OPA	50024700 50024800 50024900	Line Receiver (OEM Mag.Tape , for Mitsubishi)	0V to +1.5V -1.8V to -3.5V	Logic "0" Logic "1"	3 circuits Matches IPA & AQA

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
OQA	50025000 50025100 50025200	Line Receiver (OEM Mag.Tape for Mitsubishi)	+1V -1V	Logic "0" Logic "1"	3 circuits IBM "N" level Superseded by OPA
ORA	50025300 50025400 50025500	Read Out Comparator (Rabinow OCR)	Analog DC Probe Storage Clear	Store - Peak Logic "0" if Max Logic "1"	Many ORA cards probed simultaneously to determine best Max.
OSA	50025600 50025700 50025800	Line Receiver (601 Daisy Chain)	0V +2.0V	Logic "0" Logic "1"	3 circuits Matches IS.., series ITA & ASA
OSB	50025600 50025701 50025801	Line Receiver (Optical reading Machine)	0V +2.0V	Logic "0" Logic "1"	OSA with 120 ohms input termination
OTA	50025900 50026000 50026100	Level Switch (807/808 Disk File)	D-C Analog from +10V to -10V	Logic "1" when |Input| < Threshold Logic "0" when |Input| > Threshold	Threshold adjustable from ± 50 mv to ± 400 mv
OUA	50026200 50026300 50026400	Schmitt Trigger (807/808 Disk File)	E in > +3.5V E in < +2.5V	Logic "0" Logic "1"	2 Circuits per card
OVA	50026500 50026600 50026700	Gated Pulse Shaper (853 Disk Drive)	Complementary 0.6V Rectangular waves @+8V & Gate=Logic"1" Gate = Logic "0"	200 ns logic "1" Pulse when rectangular wave polarity reverses Logic "0"	
OWA	Design Under way				
OYA	50027400 50027500 50027600	Line Receiver (OEM Beckman)	-12V -1V	Logic "0" Logic "1"	3 Circuits, Matches IYA

Type	Card Blanks Comp. Layout Schematic	Application	Input	Output	Comments
TAA	48303200 48303300 48303400	Dual Photodiode Amplifier (915 Page Reader)	Photodiode - Photodiode +	Off, -20V -3/4V @ 5 MA	2 Circuits, Bias separately adjustable for each circuit Drawings at Rabinow

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
UAA	46245500 46241800 46244300	Adjustable Delay (Mag. Tape)	Logic "0" Logic "1"	Logic "0" delayed Logic "1"	2-5000 Micro sec delay on "0" Obsolete Use UAB for future design
UAB	50007300 50007400 50007500	Adjustable Delay (Mag. Tape)	Same as UAA		Supersedes UAA with 0-25 μs temp. stabilized delay
UBA	41060000 41060100 41060200	Dual Inverter (180 DC)	Logic "0" Logic "1"	Logic "1" Logic "0"	Similar to Control Corp. 24 Obsolete. Use 24B for future design.
UCB	50000100 50000200 50000300	Multivibrator Delay (Mag. Tape)	Logic "0" Logic "1" leading edge	Std. Logic Logic "1" pulse after delay	1.9 - 4.5 Micro sec delay Do not use in future design
UDA	46501500 46501600 46501700	Display	Std. Logic	Std. Logic8	Inverter Pre-Production only
UEA	50028000 50028100 50028200	699.527 Oscillator Calib. (852 Disk Drive)	Logic "0" Logic "1" (from IVA card)	1)-Std. logic pulses @699.5KC 2)-Beat frequency of1) with Input	Requires 2 card spaces Oscillator crystal controlled
UFA	50028300 50028400 50028500	Voltage Control Assy (Mag. Tape)	Logic "0" Logic "1"	Logic "0" & "1" delayed Logic "1" & "0"	1.2-4.2 μs delay on "0" input. Longer delays with jumpers & external capacitor. Obsolete Retrofitted by UFB.
UFB	50028301 50028401 50028500	Voltage Control delay (Mag. Tape)	Logic "0" Logic "1"	Logic "0" & "1" delayed Logic "1" & "0"	Supersedes UFA Longer delays with jumpers & external capacitor
UGA	50028600 50028700 50028800	Voltage Controlled Pulse Delay (Mag. Tape)	Logic "1" pulse	Logic "1" pulse delayed	1/4 μs input pulse delayed 1 1/4 - 5 us. Optional longer delay with jumpers & external capacitors.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
UHA	50028900 50029000 50029100	Adjustable Short Term Delay (807/808 Disk File)	Logic "1" Pulse	Logic "1" Pulse Adjustable from 0.1 to 1.2μs independent of Logic "1" input pulse width.	Requires 400 ns logic "0" input for full recycle at min delay, 100 ns at max delay. Delay initiated by negative going excursion.
UIA	50029200 50029300 50029400	Pulse Shaper (807,808 Disk File)	Logic "0" Logic "1"	Logic "0" pulse Logic "1"	Output "0" pulse of 75ns when input goes positive. with pin 6,7 jumpered. (180 ns with pin 6,8 jumpered).
UJA	Not to be released				
UJB	50029501 50029601 50029701	Adjustable Long Term Delay (General Purpose)	Logic "0" Logic "1"	Logic "0" & "1" delayed Logic "1" & "0"	Delays on "0" input. Complementary outputs. Delays from 300 μs to 100 sec by jumper options. Range of adjustment = 10:1
UKA	50029800 50029900 50030000	Gated Toggle Flip-Flop (853 Disk Drive)	Toggle = Logic Pulse & Gate = Logic "0" Gate=Logic "1"	Standard Logic, Flip-Flop Toggles on each 200 ns pulse Jammed to Logic "0"	Outputs do not include "AND" diodes.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
XKA	46245400 46241700 46244400	Counter Differentiator (Mag.Tape)	Logic "0" Logic "1"	Logic "1" pulse Logic "0"	Output pulse when input goes positive 2 circuits
XKB	50008200 50008300 50008400	Inv. and Diff. (General)	Logic "0" Logic "1"	Logic "1" pulse Logic "0"	Faster than XKA Obsolete Use XKC 2 circuits
XKC	50008201 50008301 50008401	Inv. and Diff. (General)	Logic "0" Logic "1"	Logic "1" pulse Logic "0"	Output "1" pulse for 0.4 microsecond 2 circuits

CUT ALONG LINE

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