

CONTROL DATA® OMEGA / 480 - MODEL 1 CENTRAL PROCESSING UNIT

AA125A, AA126A, AA127A, AA128A, AA129A, AA130A

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REVISION LETTERS I, O, Q AND X ARE NOT USED

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PL SYSTEMS INC.

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PREFACE

The manual contains information necessary to operate the OMEGA computer system. A visual index is provided, as an aid, for quickly locating the controls and indicators described. For a more detailed description of the OMEGA see:

- OMEGA/Theory of Operation (81-104-000)
- OMEGA/Maintenance Manual (81-104-003)

The reader of this manual is assumed to have basic computer know-ledge and experience.

This manual is divided into sections as follows:

SYSTEM CONTROL PANEL INDICATORS, SWITCHES, AND KEYS - This section describes the purpose of the individual indicators, switches and keys. It does not describe the applications of these facilities beyond the normal operating procedures.

CONSOLE FILE - This section contains the procedures required to handle the insertion and removal of the flexible magnetic disks.

CONSOLE PRINTER KEYBOARD - This section contains the printer/key board manual operations initial setup, operator adjustment, operator maintenance procedures and descriptions of indicators and controls.

OPERATING PROCEDURES - This section contains the procedures for operation initialization and error recovery.

HANDLING ABNORMAL SITUATIONS - This section contains general and specific flowcharts and text for the reader's use in analyzing abnormal situations.

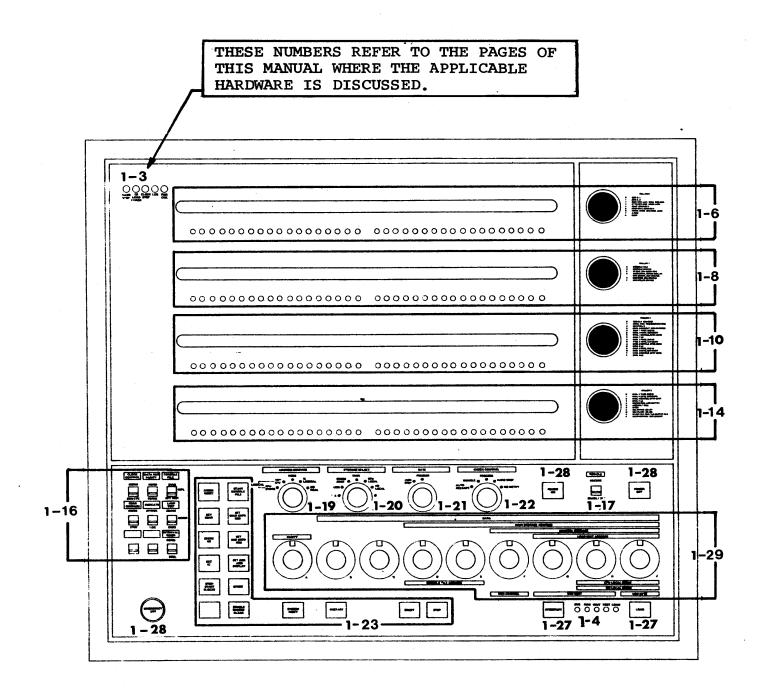
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ABBREVIATIONS

| AVIBL | available | LSA R | local storage address register |
|-------|-------------------------------------|---------|--------------------------------|
| ADR | address | MCH CHK | machine check |
| ALU | arithmetic logic unit | MPX | multiplexer |
| BFFR | buffer | MRK | mark |
| BLK | block | MS | main storage |
| BNDRY | boundary | MTR | meter |
| CDA | chain data | NEQ | not equal |
| CE | correctable error | NH | not high |
| CHAN | channel | OP | operate |
| CHK | check | PE | parity error |
| CLK | clock | PRKB | printer–keyboard |
| CMD | command | PSW | program status word |
| CMPT | complete | PTY | parity |
| CNT | control | RD | read |
| CNTL | control | RECON | reconfigure |
| CNTR | counter | REG | register |
| COMP | compare | RIP | retry in process |
| COND | condition | RST | reset |
| CONS | console | SAR | storage address register |
| CPU | central processor unit | SCU | storage control unit |
| CS | control storage | SEL | select |
| CSAR | control storage address register | SP | storage protect |
| CSIC | control storage instruction counter | SP/IVA | storage protect violation or |
| DAT | dynamic address translation | · | invalid address violation |
| DBWD | doubleword | SP VIOL | storage protect violation |
| DEGR | degrade | STATS | status register |
| DEL | delete | SUPR | suppress |
| DTB | data transfer bus | SYS | system |
| ECC | error correction control | TLB | translation lookaside buffer |
| ERR | error | TMR | timer |
| EXCP | exception | TRANS | translation |
| FWD | forward | UCW | unit control word |
| FNB | function branch | UE | uncorrectable error |
| FRWD | forward | VLD | valid |
| HRT | high resolution timer | WD | write data |
| IDAW | indirect address word | WR | write |
| INTF | interface | XER | transfer |
| ISO | inhibit select out | XF | transfer |
| IVA. | invalid address | XFR BUS | transfer bus |

VISUAL INDEX



OMEGA CONSOLE

INTRODUCTION

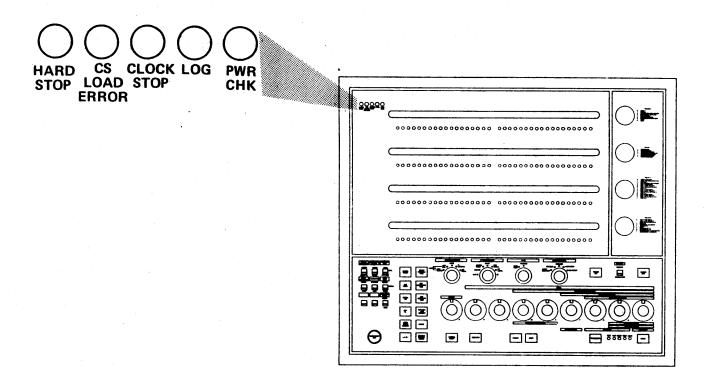
The OMEGA Computer Systems' Central Processing Unit (CPU) has indicators and manual controls that permit operation of the system and observation of the results of any operation. These indicators and controls are assembled on a panel that serves as both operator's system control and a maintenance control panel.

The Console file is the microprogram loading device for the OMEGA System. The Maintenance/File Card (MF) is the interface and control link between the CPU and the console file.

The console file, through the MF card loads control storage with either a microprogram, for user operations, or with a microdiagnostic program for checking out the CPU. An initial microprogram load (IMPL), or a diagnostic operation initiated from the CPU console, turns console-file power on.

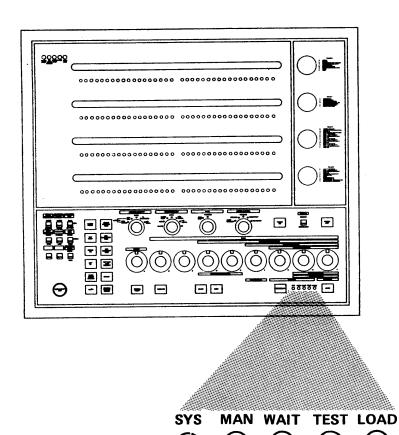
The console printer/keyboard is connected to the CPU through the multiplexer channel interface. The control unit is the OP card.

OPERATOR ACTION INDICATORS



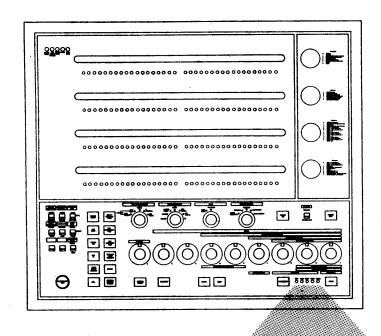
| INDICATOR | CONDITION INDICATED |
|---------------|---|
| HARD STOP | CPU is in a Hard-Stop condition. CPU clock not running. |
| CS LOAD ERROR | Floppy Disk did not load correctly to control storage. |
| CLOCK STOP | CPU clock is stopped. Microinstruction process-ing has ceased. |
| LOG | A log of the CPU status to the Console Buffer is in progress. This operation, initiated by a machine check, takes approximately 2 msecs. Should the light be on for more than an instant, the machine is constantly receiving machine checks. |
| PWR CHK | A power supply failure occurred during system operation, or a power supply is at margin. |

SYSTEM INDICATORS



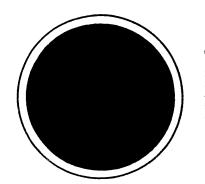
| INDICATOR | CONDITION INDICATED |
|-----------|---|
| SYS | CPU operations are in progress. |
| MAN | Program processing is stopped and will not resume until operator intervention occurs. All pending interrupts are handled. Manual store/display operations are possible only when the MAN indicator is on. |
| WAIT | System is in a wait state (CPU running but no instruction processing taking place). If an interrupt occurs, the CPU is taken out of wait state and processing is started under control of the program being executed. |

SYSTEM INDICATORS



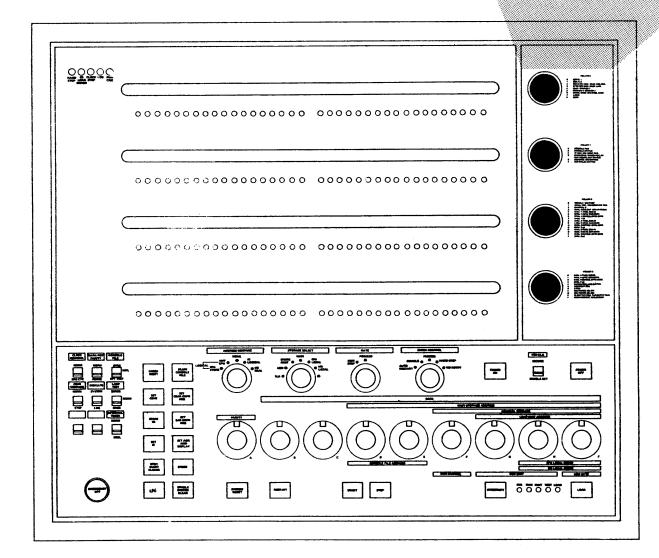
| SYS | | WAIT | | |
|-----|---------|---------|---------|---|
| 0 | \circ | \circ | \circ | 0 |

| INDICATOR | CONDITION INDICATED |
|-----------|---|
| TEST | Any of the following switches are not in the positions indicated: 1. CHECK CONTROLPROCESS 2. RATEPROCESS 3. ADDRESS COMPARENONE 4. CLOCK CONTROLNORM 5. DATA ROT PARITYNORM 6. CONSOLE FILEIMPL 7. INTERVAL TIMERNORM 8. CSAR COMPARENORM |
| LOAD | Initial Program Load (IPL) is in process. This indicator turns on when LOAD is pressed and turns off when the initial PSW is loaded successfully. |

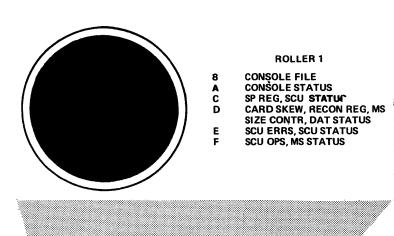


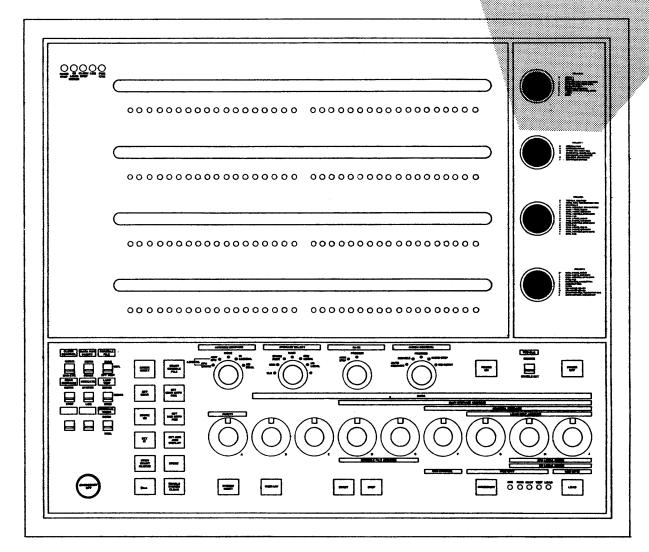
ROLLER Ø

CSIC Ø, 1
CSIC 2, 3
DATA SRV CSIC, CHNL END CSIC
BYTE MPX CSIC, CSDR LATE
CSAR, CSAR BU 1
CSAR BU 2, CSAR BU 3
STATS, EREG, CPU ERSS, LSAR
A REG
CSDR
DIAG

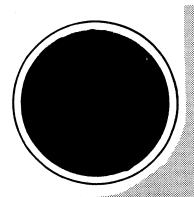


| | DISPLAY ROLLER O, SWITCH | | | | |
|-------------|--------------------------|---|--------------------------|--|--|
| SWITCH | BIT | | LOGIC | | |
| POSITION | POSITION | INFORMATION DISPLAYED | DRAWING | | |
| 0 | 4-17 | Control Storage Instruction Counter 0 (14 Bits) | anu an an a | | |
| ŏ | 22-35 | Control Strage Instruction Counter 1 (14 Bits) | CPU-CA-014 | | |
| ŏ | 18 | System Reset Trap Latch (1 bit) | CPU-CA-014 | | |
| ١٥ | 19 | Machine Check Trap Latch (1 bit) | CPU-CA-007 CPU-CA-007 | | |
| Ö | 20 | Branch Latch (1 bit) | CPU-CA-007 | | |
| ŏ | 21 | Call Latch (1 bit) | | | |
| | 1 | call bacch (I bit) | CPU-CA-007 | | |
| 1 | 0 | Store Protect/Invalid Address Trap Latch (1 bit) | SCU-SA-013 | | |
| 1 | 1 | Dynamic Address Translation Trap Latch (1 bit) | SCU-SA-023 | | |
| 1 | 2 | Function Branch 1 Latch (1 bit) | CPU-CA-007 | | |
| 1 | 3 | Function Branch 2 Latch (1 bit) | CPU-CA-007 | | |
| 1 | 4-17 | Control Stcrage Instruction Counter 2 (14 bits) | CPU-CA-015 | | |
| 1 | 18-20 | Control Stcrage Instruction Counter Pointer C.B. & A | | | |
| 8 | 1 | (3 bits) | CPU-CA-008 | | |
| 1 | 21 | Return Latch (1 bit) | CPU-CA-007 | | |
| 1 | 22-35 | Control Storage Instruction Counter 3 (14 bits) | CPU-CA-015 | | |
| |] | , | 010 01. 015 | | |
| 2 | 5-17 | Control Storage Instruction Counter Channel Data Service | CPU-CA-016 | | |
| 2 | 23-35 | Channel End Control Storage Instruction Counter (13 bits) | CPU-CA-016 | | |
| 8 | | | | | |
| 3 | 5-17 | Byte Multiplexer Control Storage Instruction Counter | CPU-CA-017 | | |
| 3 | 25-35 | Control Storage Data Register Late (11 bits) | CPU-CA-001 | | |
| | | | | | |
| 4 | 5-17 | Control Storage Address Register (13 bits) | CPU-CA-010 | | |
| 4 | 23-35 | Control Storage Address Register Backup 1 (13 bits) | CPU-CA-011 | | |
| 3 | | | | | |
| 5 | 5-17 | Control Storage Address Register Backup 2 (13 bits) | CPU-CA-011 | | |
| 5 | 23-35 | Control Storage Address Register Backup 3 (13 bits) | CPU-CA-011 | | |
| | | | | | |
| 6 | 8-0 | CPU Status (8 bits +P) | CPU-AU-017 | | |
| 6 | 9 | Data Transfer Bus Parity Error (1 bit) | CPU-AU-025 | | |
| 6 | 10-17 | Exception Register (8 bits) | CPU-AU-018 | | |
| 6 | 18 | Carry 0 (1 pit) | CPU-AU-016 | | |
| 6 | 19 | P Register Parity Error (1 bit) | CPU-AU-025 | | |
| 6 | 20 | Q Register Parity Error (1 bit) | CPU-AU-025 | | |
| 6 | 21-24 | Local Storage Address Register (4 bits) | CPU-AU-019 | | |
| 6 | 25 | Spill Left (1 bit) | CPU-AU-013 | | |
| 6 6 6 | 26 | Arithmetic Logic Unit Error (1 bit) | CPU-AU-009 | | |
| | | | | | |
| 7 | 0-35 | "A" Registe: +4 Parity Bits (36 bits) | CPU-AU-009 | | |
| 8 | 0-35 | Control Stomage Data Register | CPU-AU-001 | | |
| | | | 0.0 80 001 | | |
| F | 0-35 | Diagnostics | | | |
| | | | | | |



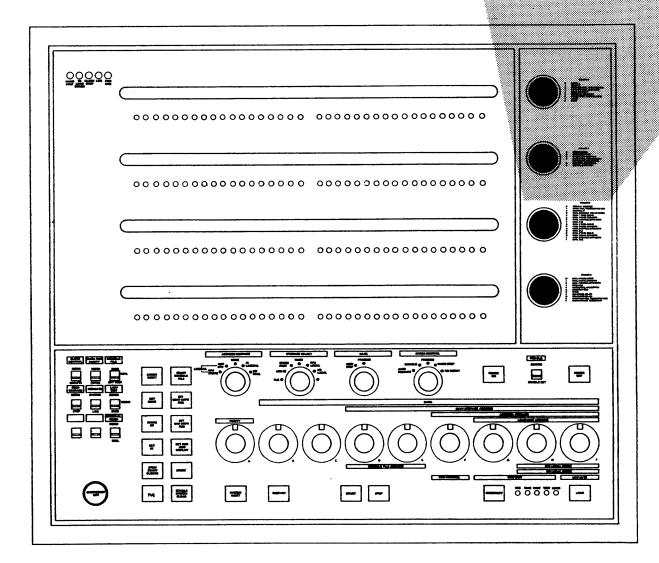


| | | DICHTAY DOLLED 1 CHIMMI | |
|--------------------|-----------------|--|----------------------------|
| CMTMOT | D.T.M. | DISPLAY ROLLER 1, SWITCH | |
| SWITCH POSITION | BIT POSITION | INFORMATION DISPLAYED | LOGIC DRAWING |
| A | 28-31 | Data Transfer Bus in Microprogram (4 bits) 0 thru 3 | CNSL-MF-002 |
| A A | 32 33 | Transfer Bs Compare Error (1 bit) Hard Stop (1 bit) | CNSL-MF-002 |
| A | 34 | Clock Stoped (1 bit) | CNSL-MF-017 CNSL-MF-017 |
| A | 35 | Log (1 bit | CNSL-MF-017 |
| 8 | 0-6 | CONSOLE FLE ADDRESS (7 Bits) | CPU-CA-028 |
| 8 | 9-17 18-26 | File Command Register !(8 bits +P) File Controls (9 bits) | CNSL-MF-006 CNSL-MF-013 |
| 8 8 | 18 19 | Start 3it (1 bit) | CNSL-MF-006 |
| 8 | 20 | File word parity (1 bit) Mode (. bit) | CNSL-MF-006 CNSL-MF-006 |
| 8 | 21 22 | Run Fi.e (1 bit) | CNSL-MF-011 |
| 8 | 23 | Ready! (1 bit) Search (1 bit) | CNSL-MF-011 CNSL-MF-011 |
| 8 8 | 24 25 | Read Lutch (1 bit) Error . (1 bit) | CNSL-MF-011 |
| 8 | 26 | Error : (1 bit) | CNSL-MF-011 CNSL-MF-011 |
| 8 | 27 28 | Send MeterOut (1 bit) Data Transer Bus Parity Error (1 bit) | CNSL-IB-008 CNSL-MF-002 |
| 8 | 29 | Control Sterage Address Register Compare Negative (1 bit) | CNSL-MF-022 |
| 8 | 30 31 | Control Sterage Data Register Parity Error (1 bit) Log Condit.on (1 bit) | CPU-CA-002 CNSL-MF-008 |
| 8 | 32 | Storage Control Unit Hard Stop (1 bit) | SCU-SC-015 |
| 8 8 | 33 34 | Central Processor Unit Error (1 bit) Console Error (1 bit) | CPU-AU-025 CNSL-MF-015 |
| с | 0-8 | Storage Pr•tect Register (9 bits) P+O thru 7 | |
| c | 9-35 | Storage Control Unit Address Register (24+3P bits) | SCU-SA-001 SCU-SA-002 |
| D | 0-8 | Main Storage Card Skew Register (9 bits) | SCU-SA-029 |
| D D | 0-2 3-5 | Bytes . & 2 (3 bits) Bytes : & 4 (3 bits) | SCU-SA-029 SCU-SA-029 |
| ם | 6-8 | Bytes & 4 (3 bits) Bytes & 6 (3 bits) | SCU-SA-029 SCU-SA-029 |
| D D | 10-13 14-17 | Reconfigure register (4 bits) 0 thru 3 | SCU-SA-028 |
| D | 19 | Main Storage Size Control (4 bits) 0 thru 3 Data Mode [1 bit) | SCU-SA-028 SCU-SC-022 |
| D D | 20-25 20 | Translation Lookaside Buffer (6 bits) Left Parity (1 bit) | SCU-SA-024 SCU-SA-024 |
| D | 21 | Left Use | SCU-SA-024 |
| D D | 22 23 | Left Delete (1 bit) Right Parity (1 bit) | SCU-SA-024 SCU-SA-024 |
| D | 34 | Right Wise (1 bit) | SCU-SA-024 |
| D D | 25 26 | Right Delete (1 bit) Dynamic Address Translation Trap (1 bit) | SCU-SA-024 SCU-SA-012 |
| D D | 28 29 | Data Transfer Bus Check (1 bit) | SCU-SA-012 |
| | | Storage Protect Output Check (1 bit) | SCU-SA-005 |
| E E | 3-35 3 | Storage Costrol Unit Errors & Status Uncorrectable Error (1 bit) | SCU-SC-005 SCU-SC-013 |
| E | 4 | Storage Data Bus In Check (1 bit) | SCU-SC-013 |
| E | 6 7 | Storage Protect Buffer Check (1 bit) Data Transfer Bus Control Check (1 bit) | SCU-SC-013 SCU-SC-013 |
| E E | 8 12-14 | Data T:ansfer Bus Address Check (1 bit) | SCU-SC-013 |
| E | 15 | SCU Cycle (3 bits) 1 thru 3 Stop Main Storage Ring Counter (1 bit) | SCU-SC-008 SCU-SC-007 |
| E E | 16 17 | Contro. Register System Reset Mode (1 bit) Contro. Register ECC Mode (1 bit) | SCU-SC-022 SCU-SC-022 |
| E | 21 | Main Storage Error - Busy (1 bit) | SCU-SC-018 |
| E E | 22 23 | Main S:orage Error - Data Available (1 bit) Main S:orage Error - Early (1 bit) | SCU-SC-018 SCU-SC-015 |
| E | 24 | Soft Machine Check Exception (1 bit) | SCU-SC-016 |
| E | 26 30 | Storage Address Register Backup Valid (1 bit) Start SCU Ring Counter (1 bit) | SCU-SC-031 SCU-SC-005 |
| E | 31 | Start Main Storage Ring Counter (1 bit) | SCU-SC-005 |
| E E | 32 33 | Load S&U Register Operation (1 bit) Purge "ranslation Lookaside Buffer Command (1 bit) | SCU-SC-021 SCU-SC-021 |
| E | 35 | SCU Exception | SCU-SC-025 |
| F | 3-35 | SCU OPERATIONS & MAIN STORAGE STATUS | |
| P P | 3 4 | Channe: Main Storage Operation (1 bit) CPU Ma:n Storage Operation (1 bit) | SCU-SC-006 SCU-SC-006 |
| F | 5 | Write (lock (1 bit) | SCU-SC-004 |
| F F | 6 7 | Read C.ock (1 bit) Read S:orage Protect (1 bit) | SCU-SC-004 SCU-SA-011 |
| F F | 8 12 | Write Storage Protect (1 bit) | SCU-SA-011 |
| F | 14 | Main Storage Double Word Operation (1 bit) Main Storage Data Transfer Bus Busy (1 bit) | SCU-SC-006 SCU-SC-009 |
| F F | 15 16 | Main Storage SCU Busy (1 bit) Data Transfer Bus Busy (1 bit) | SCU-SC-009 |
| F | 17 | SCU Busy (1 bit) | SCU-SC-009 SCU-SC-009 |
| F F | 21 22 | Main Storage Store (1 bit) Part Store (1 bit) | SCU-SC-006 SCU-SD-005 |
| F | 23 | Write Translation Lookaside Buffer (1 bit) | SCU-SA-011 |
| F F | 24 25 | Read Translation Lookaside Buffer (1 bit) Read Error Correction Control (1 bit) | SCU-SA-011 SCU-SC-004 |
| F F | 26 30 | Block Traps | SCU-SC-012 |
| F | 31 | °Main Storage Unit Busy (1 bit) Main Storage Busy (1 bit) | SCU-SC-017 SCU-SC-009 |
| F F | 32 33 | SCU Main Storage Operation (1 bit) SCU Operation Block (1 bit) | SCU-SC-006 SCU-SC-012 |
| F F | 34 | Main Storage Operation Block (1 bit) | SCU-SC-012 |
| F | 35 | CPU Hold Off (1 bit) | SCU-SC-005 |
| | | | <u> </u> |

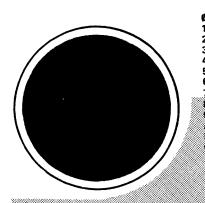


ROLLER 2

TOD CLK, SCU EXCP
INTVL TMR, TMR COMPARE REG
CHANNEL #
CHNL # BUS OUT, BRK-IN CODES
CHNL 1 TAGS, BUS IN
CHNL 1 KEYS, SAR CNTR
CHNL 1 LS
CHNL 2 TAGS, BUS IN
CHNL 2 KEYS, SAR CNTR
CHNL 2 KEYS, SAR CNTR
CHNL 2 KEYS, SAR CNTR
CHNL 2 LS
CHNL 3 TAGS, BUS IN
CHNL 3 LS
CHNL 3 TAGS, BUS IN
CHNL 3 TAGS, BUS IN
CHNL 3 CNTRLS, BYTE CNTR
CHNL 3 LS



| DISPLAY ROLLER 2, SWITCH | | | | |
|---|---|---|--|--|
| SWITCH POSITION | BIT POSITION | INFORMATION DISPLAYED | LOGIC DRAWING | |
| 8 8 | 0-35 1 | Channel 2 - Tags & Bus In Kot Inhibit Break In (1 Bit) | CH-IC-015 CH-IC-015 | |
| 8 | 2 | Operation Out (1 Bit) | CH-IC-015 | |
| 8 | 3 | Service Out (1 Bit) | CH-IC-015 | |
| 8 | 4 | Supervisor Out (1 Bit) | CH-IC-015 | |
| 8 8 | 5 | Lata Out (1 Bit) | CH-IC-015 | |
| B | 6 | Hold Out (1 Bit) Address Out (1 Bit) | CH-IC-015 CH-IC-015 | |
| 8 | 8 | Command Out (1 Bit) | CH-IC-015 | |
| 8 | 10 | Invalid Address (1 Bit) | CH-IC-032 | |
| 8 | 11 | Storage Protect Violation (1 Bit) | CH-IC-032 | |
| 8 | 14 | Storage Control Unit Data Error (1 Bit) | CH-IC-032 | |
| 8 | 15 | Fisconnect In (1 Bit) | CH-IC-032 | |
| 8 8 | 16 | Count Not Equal to Zero (1 Bit) | CH-IC-019 | |
| 8 | 17 19 | Read (1 Bit) Address In (1 Bit) | CH-IC-033 CH-IC-023 | |
| 8 | 20 | Iata In (1 Bit) | CH-IC-023 | |
| 8 | 21 | Nark O In (1 Bit) | CH-1C-023 | |
| 8 | 22 | Cperation In (1 Bit) | CH-IC-023 | |
| 8 | 23 | Select In (1 Bit) | CH-IC-023 | |
| 8 | 24 | Request In (1 Bit) | CH-IC-023 | |
| 8 | 25 | Status In (1 Bit) | CH-IC-023 | |
| 8 | 26 | Service In (1 Bit) | CH-IC-023 | |
| ۰ | 28-35 | Bus In (8 Bits) 0 thru 7 | CH-IC-024 | |
| 9 | 0-35 | Channel 2 - Keys & Storage Address Register Control | CH-IC | |
| 9 | 1-4 | Storage Protect Key (4 Bits) 0 thru 3 | CH-IC | |
| 9 | 10-32 | Storage Address Register Counter (21 Bits) 8 thru 28 | CH-IC-017 | |
| 9 | 33 | SCU Transfer Control 1 (1 Bit) | CH-IC-019 | |
| 9 | 34 | Compartment Full (1 Bit) | CH-IC-032 | |
| 9 | 35 | Compartment Empty (1 Bit) | CH-IC-032 | |
| А | 0-35 | Channel 2 - Controls & Byte Counter | CH-IC | |
| A | 1 | Chain Data (1 Bit) | CH-IC-033 | |
| A | 2 | Write (1 Bit) | CH-IC-033 | |
| A | 3 | Not Skip (1 Bit) | CH-IC-033 | |
| A | 4 | Forward (1 Bit) | CH-IC-033 | |
| ý | 5 | Not Indirect Address Word (1 Bit) | CH-IC-033 | |
| A | 10 | Not Page Boundry (1 Bit) | CH-IC-029 | |
| Ä | 11 14 | Last Store Done (1 Bit) | CH-IC-032 CH-IC-032 | |
| Ä | 15-17 | Invalid Address or Storage Protect Violation (1 Bit) Interface Transfer Counter (3 Bits) | CH-IC-019 | |
| Ä | 19-35 | Byte Counter (16 Bits) | CH-IC-019 | |
| В | 0-35 | Channel 2 - Local Storage (32 Bits) | CH-IC-020 | |
| с | 0-35 | Channel 3 - Tags & Bus In | CH-IC | |
| c | 1 | Not Inhibit Break In (1 Bit) | CH-IC-014A | |
| c | 2 | Operation Out (1 Bit) | CH-IC-014A | |
| c | 3 | Service Out (1 Bit) | CH-IC-014A | |
| c | 4 | Supervisor Out (1 Bit) | CH-IC-014A | |
| C | 5 | Data Out (1 Bit) Hold Out (1 Bit) | CH-IC-014A CH-IC-014A | |
| c | 6 7 | Address Out (1 Bit) | CH-IC-014A | |
| čl | 8 | Command Out (1 Bit) | CH-IC-014A | |
| čl | 10 | Invalid Address (1 Bit) | CH-IC-031A | |
| c | 11 | Storage Protect Violation (1 Bit) | CH-IC-031A | |
| c | 14 | Storage Control Unit Data Error (1 Bit) | CH-IC-031A | |
| c | 15 | Disconnect In (1 Bit) | CH-IC-023A | |
| c c | 16 17 | Count Not Equal to Zero (1 Bit) Read (1 Bit) | CH-IC-018A CH-IC-033A | |
| č | . 19 | Address In (1 Bit) | CH-IC-033A | |
| c | 20 | Data In (1 Bit) | CH-IC-023A | |
| c | 21 | Mark 0 In (1 Bit) | CH-IC-023A | |
| C | 22 | Operation In (1 Bit) | CH-IC-023A | |
| | | Solost In (1 Dit) | | |
| c | 23 | Select In (1 Bit) Request In (1 Bit) | CH-IC-023A | |
| c | 24 | Request In (1 Bit) | CH-IC-C23A CH-IC-C23A | |
| | 24 25 | Request In (1 Bit) Status In (1 Bit) | CH-IC-023A CH-IC-023A CH-IC-023A | |
| c c | 24 25 26 | Request In (1 Bit) | CH-IC-C23A CH-IC-C23A | |
| 0000 | 24 25 26 28-35 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A | |
| c c c | 24 25 26 28-35 0-35 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control | CH-IC-C23A CH-IC-O23A CH-IC-O23A CH-IC-O23A CH-IC-O34A | |
| C C C D | 24 25 26 28-35 0-35 1-4 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) 9us In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 | CH-IC-C23A CH-IC-O23A CH-IC-O23A CH-IC-O23A CH-IC-O34A CH-IC | |
| C C C D D D | 24 25 26 28-35 0-35 1-4 10-32 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 | CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC | |
| C C C D | 24 25 26 28-35 0-35 1-4 10-32 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC CH-IC-016A CH-IC-018A | |
| C C C C D D D D D D D | 24 25 26 28-35 0-35 1-4 10-32 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 | CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC-C16C CH-IC-C16A CH-IC-016A CH-IC-031A CH-IC-031A | |
| C C C D D D D D D D D D D D D D D D D D | 24 25 26 28–35 0–35 1–4 10–32 33 34 35 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) Channel 3 - Controls & Byte Counter | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC CH-IC-016A CH-IC-018A CH-IC-031A CH-IC-031A | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 0-35 1 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) Channel 3 - Controls & Byte Counter Chain Data (1 Bit) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC CH-IC-016A CH-IC-018A CH-IC-031A CH-IC-031A | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 0-35 1 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) Channel 3 - Controls & Byte Counter Chain Data (1 Bit) Write (1 Bit) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC-016A CH-IC-031A CH-IC-031A CH-IC-033A CH-IC-033A | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 0-35 1 2 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) Channel 3 - Controls & Byte Counter Chain Data (1 Bit) Write (1 Bit) Sot Skip (1 Bit) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC CH-IC-016A CH-IC-031A CH-IC-031A CH-IC-031A CH-IC-033A CH-IC-033A CH-IC-033A | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 0-35 1 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Full (1 Bit) Channel 3 - Controls & Byte Counter Chain Data (1 Bit) Write (1 Bit) Sot Skip (1 Bit) Sot Skip (1 Bit) Yot Indirect Address Word (1 Bit) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC-016A CH-IC-031A CH-IC-031A CH-IC-033A CH-IC-033A | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 0-35 1 2 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) Channel 3 - Controls & Byte Counter Chain Data (1 Bit) Write (1 Bit) Sot Skip (1 Bit) Sorward (1 Bit) Yot Indirect Address Word (1 Bit) Sot Page Boundary (1 Bit) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC CH-IC-016A CH-IC-031A CH-IC-031A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 0-35 1 2 3 4 5 10 11 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) Channel 3 - Controls & Byte Counter Chain Data (1 Bit) Write (1 Bit) Sot Skip (1 Bit) Sot Skip (1 Bit) Yot Indirect Address Word (1 Bit) Sot Page Boundary (1 Bit) Last Store Done (1 Bit) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC CH-IC-016A CH-IC-031A CH-IC-031A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 0-35 1 2 3 4 5 10 11 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) Channel 3 - Controls & Byte Counter Chain Data (1 Bit) Write (1 Bit) Sot Skip (1 Bit) Sot Skip (1 Bit) Tot Indirect Address Word (1 Bit) Tot Indirect Address Word (1 Bit) Last Store Done (1 Bit) Last Store Done (1 Bit) Invalid Address or Storage Protect Violation (1 Bit) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC CH-IC-016A CH-IC-031A CH-IC-031A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-031A CH-IC-031A | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 0-35 1 2 3 4 5 10 11 14 15-17 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) Channel 3 - Controls & Byte Counter chain Data (1 Bit) Sot Skip (1 Bit) Sot Skip (1 Bit) Sot Skip (1 Bit) Sot Indirect Address Word (1 Bit) fot Page Boundary (1 Bit) Last Store Done (1 Bit) Invalid Address or Storage Protect Violation (1 Bit) Interface Transfer Counter (3 Bits) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC-016A CH-IC-016A CH-IC-031A CH-IC-031A CH-IC-033A | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 0-35 1 2 3 4 5 10 11 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) Channel 3 - Controls & Byte Counter Chain Data (1 Bit) Write (1 Bit) Sot Skip (1 Bit) Sot Skip (1 Bit) Tot Indirect Address Word (1 Bit) Tot Indirect Address Word (1 Bit) Last Store Done (1 Bit) Last Store Done (1 Bit) Invalid Address or Storage Protect Violation (1 Bit) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC CH-IC CH-IC CH-IC-016A CH-IC-031A CH-IC-031A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-033A CH-IC-031A CH-IC-031A | |
| | 24 25 26 28-35 0-35 1-4 10-32 33 34 35 0-35 1 2 3 4 5 10 11 14 15-17 | Request In (1 Bit) Status In (1 Bit) Service In (1 Bit) Sus In (8 Bits) 0 thru 7 Channel 3 - Keys & Storage Address Register Control Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 SCU Transfer Control 1 (1 Bit) Compartment Full (1 Bit) Compartment Full (1 Bit) Compartment Empty (1 Bit) Channel 3 - Controls & Byte Counter chain Data (1 Bit) Sot Skip (1 Bit) Sot Skip (1 Bit) Sot Skip (1 Bit) Sot Indirect Address Word (1 Bit) fot Page Boundary (1 Bit) Last Store Done (1 Bit) Invalid Address or Storage Protect Violation (1 Bit) Interface Transfer Counter (3 Bits) | CH-IC-C23A CH-IC-023A CH-IC-023A CH-IC-023A CH-IC-034A CH-IC-016A CH-IC-016A CH-IC-031A CH-IC-031A CH-IC-033A | |



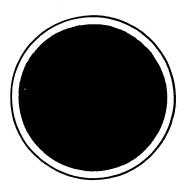
ROLLER 2

TOD CLK, SCU EXCP
INTVL TMR, TMR COMPARE REG
CHANNEL Ø
CHNL Ø BUS OUT, BRK-IN CODES
CHNL 1 TAGS, BUS IN
CHNL 1 KEYS, SAR CNTR
CHNL 1 CNTRLS, BYTE CNTR
CHNL 2 TAGS, BUS IN
CHNL 2 KEYS, SAR CNTR
CHNL 2 KEYS, SAR CNTR
CHNL 2 CNTRLS, BYTE CNTR
CHNL 3 TAGS, BUS IN
CHNL 3 TAGS, BUS IN
CHNL 3 KEYS, SAR CNTR
CHNL 3 KEYS, SAR CNTR
CHNL 3 CNTRLS, BYTE CNTR
CHNL 3 LS

DISPLAY ROLLER 2, SWITCH

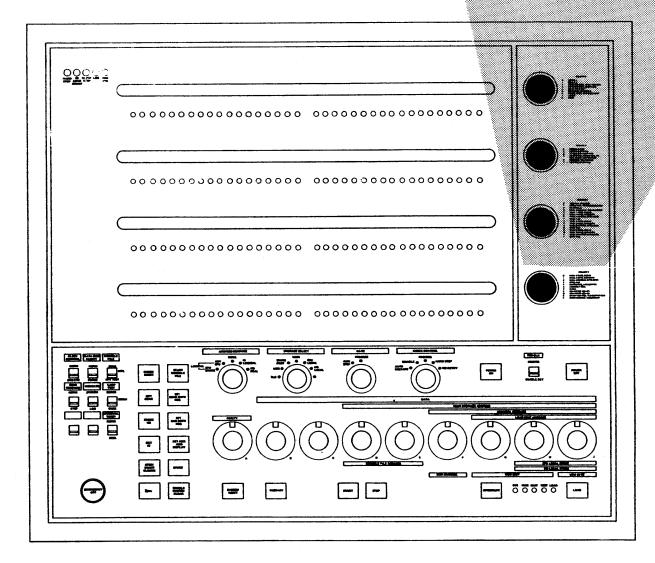
In all switch positions parity bits are in bit positions 0,9,18,27, and represent the byte to the right of the parity indicator.

| byte to t | he right o | f the parity indicator. | |
|-------------|-----------------------|--|-------------------------------------|
| SWITCH | віт | - The state of the | LOGIC |
| POSITION | POSITION | INFORMATION DISPLAYED | DRAWING |
| 0 | 0-35 | TIME OF DAY CLOCK & SCU EXCEPTIONS | į |
| 0 | 9-22 | Time of Day Clock (13 Bits) Bits 40 thru 51 | SCU-SC-023 |
| 0 | 23 | Time of Day Set (1 Bit) | SCU-SC-022 |
| 0 | 24 | Uncorrectable Error (1 Bit) | SCU-SD-022 SCU-SA-005 |
| 0 | 25 | Storage Protect Check (1 Bit) | CNSL-OP-019 |
| 0 | 26 | Cancel (1 Bit) Correctable Error (1 Bit) | SCU-SD-022 |
| 0 | 28 29 | Degrade (1 Bit) | SCU-SC-016 |
| 0 | 31-35 | Timer Exception Register (5 Bits) | SCU-SC-025 |
| ŏ | 31 | High Resolution Timer (1 Bit) | SCU-SC-025 |
| ō | 32 | Address (1 Bit) | scu-sc-025 |
| 0 | 33 | Time of Day (1 Bit) | SCU-SC-025 |
| 0 | 34 | Timer (1 Bit) | SCU-SC-025 |
| 0 | 35 | Compare (1 Bit) | SCU-SC-025 |
| 1 | 9-22 23-35 | Interval Timer (12 Bits) Bits 40 thru 51 Timer Compare Register (12 Bits) 40 thru 51 | SCU-SC-024 SCU-SC-024 |
| 2 | 0-35 | Channel 0,36 Bits | CH-IB |
| 2 | 1 | Inhibit Select Out (1 Bit) | CH-IB-005 |
| 2 | 2 | Operation Out (1 Bit) | CH-IB-005 |
| 2 | 3 | Service Out (1 Bit) | CH-IB-005 |
| 2 | 4 | Supervisor Out (1 Bit) | CH-1B-005 |
| 2 | 5 | Data Out (1 Bit) | CH-IB CH-IB-005 |
| 2 | 6 | Hold Out Log (1 Bit) | CH-IB-005 CH-IB-005 |
| 2 | 7 | Address Out (1 Bit) | CH-1B-005 |
| 2 | 8 10 | Command Out (1 Bit) Hold Out Hardware (1 Bit) | CH-1B-003 |
| 2 | 10 | Data Transfer Bus Out Error (1 Bit) | CH-IB-007 |
| 2 | 12 | Data Transfer Bus Out Error (1 Bit) | CH-IB-007 |
| 2 | 13 | Data Transfer Bus 2 Error (1 Bit) | CH-IB-007 |
| 2 | 14 | Data Transfer Bus 3 Error (1 Bit) | CH-IB-007 |
| 2 | 15 | Discontinue In (1 Bit) | CH-IB-006 |
| 2 | 16 | Interface Free (1 Bit) | CH-IB-007 |
| 2 | 17 | Bus In Parity Error (1 Bit) | CH-IB-006 |
| 2 | 19 | Address In (1 Bit) | CH-IB-006 |
| 2 | 22 | Operation In (1 Bit) | CH-IB-006 |
| 2 | 23 | Select In (1 Bit) | CH-IB-006 |
| 2 | 24 | Request In (1 Bit) | CH-IB-006 |
| 2 | 25 | Status In (1 Bit) | CH-IB-006 |
| 2 | 26 | Service In (1 Bit) | CH-IB-006 |
| 2 | 28-35 | Bus In (8 Bits) 0 thru 7 | CH-IB-006 |
| 3 3 3 | 1-8 10-17 28-35 | Low Priority Break In Code (8 Bits) 0 thru 7 High Priority Break In Code (8 Bits) 8 thru 15 Channel 0 Bus Out (8 Bits) 0 thru 7 | CH-IB-009 CH-IB-009 CH-IB-005 |
| | 0-35 | Channel I Mage and Due In | CH-IC |
| 4 | 1 | Channel 1 - Tags and Bus In Not Inhibit Break In (1 Bit) | CH-IC-014 |
| 4 | 2 | Operation Out (1 Bit) | CH-IC-014 |
| 4 | 3 | Service Out (1 Bit) | CH-IC-014 |
| 4 | 4 | Supervisor Out (1 Bit) | CH-IC-014 |
| 4 | 5 | Data Out (1 Bit) | CH-IC-014 |
| 4 | 6 | Hold Out (1 Bit) | CH-IC-014 |
| 4 | 7 | Address Out (1 Bit) | CH-IC-014 |
| 4 | 8 | Command Out (1 Bit) | CH-IC-014 |
| 4 | 10 | Invalid Address (1 Bit) | CH-IC-031 |
| 4 | 11 | Storage Protect Violation (1 Bit) | CH-IC-031 |
| 4 | 14 | Storage Control Unit Data Error (1 Bit) | CH-IC-031 |
| 4 | 15 | Disconnect In (1 Bit) | CH-IC-023 |
| 4 | 16 | Count Not Equal to Zero (1 Bit) | CH-IC-018 |
| 4 | 17 | Read (1 Bit) | CH-IC-033 |
| 4 | 19 | Address In (1 Bit) | CH-IC-023 |
| 4 | 20 | Data In (1 Bit) | CH-IC-023 CH-IC-023 |
| 4 | 21 22 | Mark 0 In (1 Bit) | CH-1C-023 |
| 1 : | 22 | Operation In (1 Bit) Select In (1 Bit) | CH-IC-023 |
| 4 | 23 | Select In (1 Bit) Request In (1 Bit) | CH-IC-023 |
| 4 | 25 | Status In (1 Bit) | CH-IC-023 |
| 4 | 26 | Service In (1 Bit) | CH-IC-023 |
| 4 | 28-35 | Bus In (8 Bits) 0 thru 7 | CH-IC-024 |
| 1 | | Channel 1 - Keys & Storage Address Register Counter | CH-IC |
| 5 | 0-35 | | CH-IC |
| 5 | 1-4 | Storage Protect Key (4 Bits) 0 thru 3 Storage Address Register Counter (21 Bits) 8 thru 28 | CH-IC-016 |
| 5 | 10-32 | Storage Address Register Counter (21 210) | CH-IC-018 |
| 5 | 33 | Compartment Full (1 Bit) | CH-IC-031 |
| 5 | 34 | Compartment Empty (1 Bit) | CH-IC-031 |
| 5 | 35 | Configs runers and of / | 1 |
| _ | 0-35 | Channel 1 Controls & Byte Counter | CH-IC |
| 6 | 1 1 | Chain Data (1 Bit) | CH-IC-033 |
| 6 | 2 | Write (1 Bit) | CH-IC-033 |
| 6 | 3 | Not Skip (1 Bit) | CH-IC-033 |
| 6 | 4 | Forward (1 Bit) | CH-IC-033 CH-IC-033 |
| 6 | 5 | Not Indirect Address Word (1 Bit) | CH-IC-033 |
| 6 | 10 | Not Page Boundry (1 Bit) | CH-IC-023 |
| 6 | 11 | Last Store Done (1 Bit) | CH-IC-031 |
| 6 | 14 | Invalid Address or Storage Protect Violation (1 Bit) | CH-IC-018 |
| 6 | 15-17 | Interface Transfer Counter (3 Bits) | CH-IC-018 |
| 6 | 19-35 | Byte Counter (16 Bits) | |
| | | Channel 1 Local Storage (32 Bits +4P) | CH-IC-020 |
| 7 | 0-35 | Chainer I book beerge (| |
| L | | | |



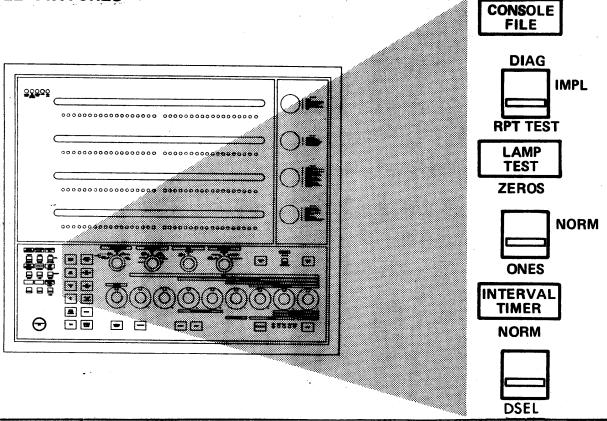
ROLLER 3

CHNL 4 TAGS, BUS IN
CHNL 4 KEYS, SAR CNTR
CHNL 4 CNTRLS, BYTE CNTR
CHNL 4 LS
SWITCH REG, LOG BUFFER
ASSEMBLY REG
B REG
SCU MERGE (00-31)
SCU MERGE (32-63)
SP OUT PUT REG, TLB OUTPUT REG
BIE/SYNDROME, SAR BACKUP



| DISPLAY ROLLER 3, SWITCH | | | | | |
|--------------------------|-----------------|--|----------------------------|--|--|
| SWITCH POSITION | BIT POSITION | information displayed | LOGIC DRAWING | | |
| 0 | 0-35 | Channel 4 - Tags and Bus In | CH-IC | | |
| 9 0 | 1 | Not Inhibit Break In (1 Bit) | CH-IC-015A | | |
| 0 | 2 | Operation Out (1 Bit) | CH-IC-015A | | |
| 0 | 3 | Service Out (1 Bit) | CH-IC-015A | | |
| Ö | 4 | Supervisor Out (1 Bit) | CH-IC-015A | | |
| Ö | 5 6 | Data Out (1 Bit) | CH-IC-015A | | |
| ŏ | 7 | Hold Out (1 Bit) | CH-IC-015A | | |
| l ŏ | é | Address Out (1 Bit) Command Out (1 Bit) | CH-IC-015A | | |
| ŏ | 10 | Invalid Address (1 Bit) | CH-IC-015A | | |
| . 0 | 11 | Storage Protect Violation (1 Bit. | CH-IC-032A | | |
| 0 | 14 | Storage Control Unit Data Error 1 Bit) | CH-IC-032A | | |
| 0 | 15 | Disconnect In (1 Bit) | CH-IC-032A CH-IC-023A | | |
| 0 | 16 | Count Not Equal to Zero (1 Bit) | CH-IC-019A | | |
| 0 | 17 | Read (1 Bit) | CH-IC-033A | | |
| 0 | 19 | Address In (1 Bit) | CH-IC-023A | | |
| 0 | 20 | Data In (1 Bit) | CH-IC-023A | | |
| 0 | 21 | Mark O In (1 Bit) | CH-IC-023A | | |
| ŏ | 22 | Operation In (1 Bit) | CH-IC-023A | | |
| ŏ | 23 24 | Select In (1 Bit) | CH-IC-023A | | |
| ŏ | 25 | Request In (1 Bit) Status In (1 Bit) | CH-IC-023A | | |
| ŏ | 26 | Service In (1 Bit) | CH-IC-023A | | |
| ō | 28-35 | Bus In (8 Bits) 0 thru 7 | CH-IC-023A | | |
| l | | 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 | CH-IC-024A | | |
| 1 | 0-35 | Channel 4 - Keys & Storage Address Rigister Counter | CH-IC | | |
| 1 | 1-4 | Storage Protect Key (4 Bits) 0 thru 3 | CH-IC | | |
| 1 | 10-32 | Storage Address Register Counter (21 Bits) 8 thru 28 | CH-IC-016A | | |
| 1 | 33 | SCU Transfer Control 1 (1 Bit) | CH-IC-019A | | |
| 1 | 34 | Compartment Full (1 Bit) | CH-IC-032A | | |
| 1 | 35 | Compartment Empty (1 Bit) | CH-IC-032A | | |
| 2 | 0-35 | Channel A. Cantural and a many and | | | |
| 2 | 1 | Channel 4 - Controls & Byte Counter | CH-IC | | |
| 2 | 2 | Chain Data (1 Bit) Write (1 Bit) | CH-IC-033A | | |
| $\tilde{2}$ | 3 | Not Skip (1 Bit) | CH-IC-033A | | |
| 2 | 4 | Forward (1 Bit) | CH-IC-033A CH-IC-033A | | |
| 2 | 5 | Not Indirect Address Word (1 Bit | CH-IC-033A | | |
| 2 | 10 | Not Page Boundry (1 Bit) | CH-IC-029A | | |
| 2 | 11 | Last Store Done (1 Bit) | CH-IC-032A | | |
| 2 | 14 | Invalid Address or Storage Protect Violation (1 Bit) | CH-IC-032A | | |
| 2 | 15-17 | Interface Transfer Counter (3 Bits) | CH-IC-019A | | |
| 2 | 19-35 | Byte Counter (16 Bits) | CH-IC-019A | | |
| 3 | 0-35 | Channel 4 - Local Storage (32 Bits) | CH-IC-020A | | |
| 4 | 0-17 | Curitah Posiston (16 Dita) | | | |
| 4 | 19 | Switch Register (16 Bits) Retry In Process 1 (1 Bit) | CNSL-MF-015 | | |
| 4 | 20 | Retry In Process 2 (1 Bit) | CNSL-MF-017 CNSL-MF-017 | | |
| 4 | 21 | Byte Control (1 Bit) | CPU-CA-009 | | |
| 4 | 22 | Block Control (1 Bit) | CPU-CA-009 | | |
| 4 | 26 | Log Buffer Parity (1 Bit) | CNSL-MF-020 | | |
| 4 | 28-35 | Log Buffer (8 Bits) | CNSL-MF-020 | | |
| 5 | 0-35 | Assembly Register (36 Bits) | CNSL-MF-006 | | |
| 7 | 0-35 | Diagnostics | , | | |
| 8 | 0-35 | B Register (36 Bits) | CPU-AU-012 | | |
| С | 0-35 | SCU Merge (36 Bits) Bits 00 to 31 | SCU-SD-006 | | |
| D | 0-35 | SCU Merge (36 Bits) Bits 32 to 63 | SCU-SD-009 | | |
| E | 0-7 | Storage Protect Output Register | SCU-SA-005 | | |
| E E | 5 6 | Petch (1 Bit) | SCU-SA-005 | | |
| E | 7 | Read (1 Bit) Changed (1 Bit) | SCU-SA-005 | | |
| E | | Translation Lookaside Buffer Output Register | SCU-SA-005 SCU-SA | | |
| Ē | 9-15 | Logical Address (8 Bits) | SCU-SA-025 | | |
| E | 19 | Use (1 Bit) | SCU-SA-025 | | |
| E | 20 | Valid (1 Bit) | SCU-SA-025 | | |
| E | 24 | Delete (1 Bit) | SCU-SA-025 | | |
| E | 25-35 | Real Address (10 Bits) | SCU-SA-026 | | |
| F F | | Byte In Error Syndrome (8 Bits) SAR Backup | SCU-SD-022 SCU-SA-030 | | |
| | | | | | |

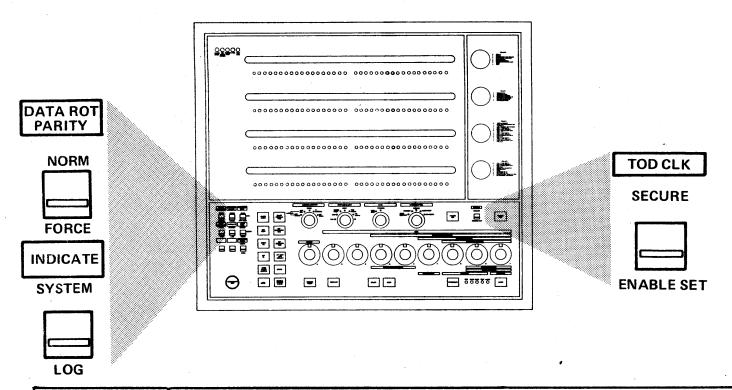
TOGGLE SWITCHES



| SWITCH | POSITION | FUNCTION |
|-------------------|----------|---|
| CONSOLE FILE | DIAG | Allows a console file read starting at the CF track specified by rotaries D and E. |
| | IMPL | Allows a console file read starting at track zero. |
| | RPT TEST | Allows a continuous console file read of the track specified by rotaries D and E. |
| LAMP TEST | ZEROS | All system control panel and PTR/KBD in- dicator lights should extinguish in this position (Except PWR CHK and TEST). |
| • | NORM | Normal Operation |
| | ONES | All system control panel and PTR/KBD in- dicator lights should illuminate in this position (Except PWR CHK and TEST). |
| INTERVAL TIMER | NORM | Allows incrementing of interval timer at location 80. |
| • | DSBL | Disables the incrementing of the interval timer. |

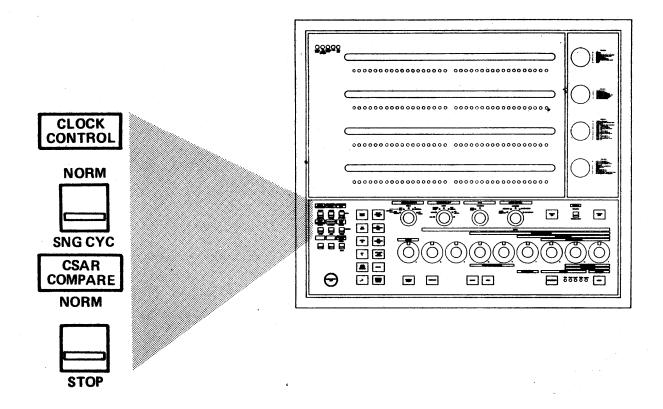
1-16

TOGGLE SWITCHES

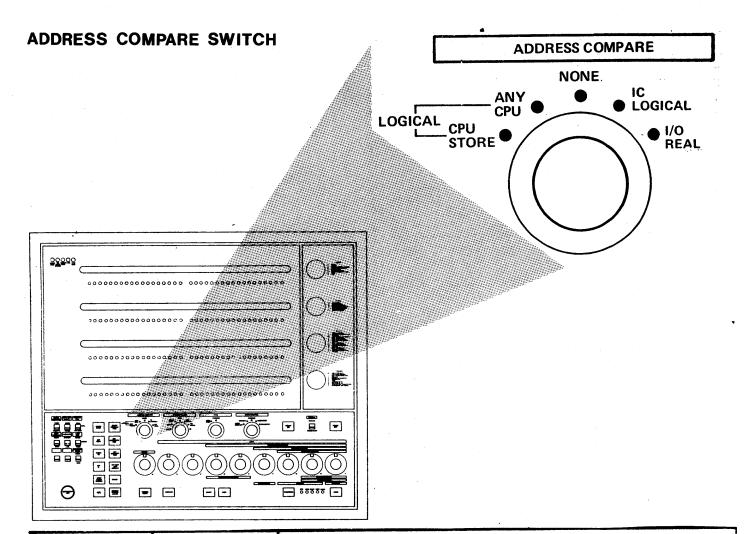


| SWITCH | POSITION | FUNCTION |
|--------------------|------------|---|
| TOD CLK | | The Time of Day (TOD) clock switch guards against an unauthorized or inadvertant change of the time-of-day clock value. |
| | SECURE | This position prevents alteration of the time of-day clock value by the SET CLOCK Inst. |
| | ENABLE SET | This position allows the SET CLOCK instruction to change the value of the TOD clock. |
| DATA ROT PARITY | NORM | Normal Processing Mode. |
| | FORCE | Allows rotary switch A to control the parity for switches B thru J. |
| INDICATE | SYSTEM | Normal processing position. |
| | LOG | Indicates current contents of Log Buffer. |

TOGGLE SWITCHES

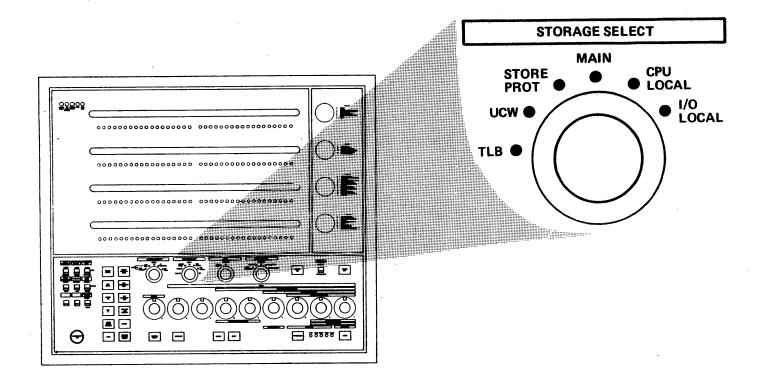


| SWITCH | POSITION | FUNCTION |
|------------------|----------|---|
| CLOCK CONTROL | NORM | Allows continuous processing of micro-instructions. |
| , | SNG CYC | Allows processing of a single micro-instruction at a time. |
| CSAR COMPARE | NORM | Normal processing position. |
| · | STOP | Allows a compare equal between CSAR and the CSAR CMPR REG to stop CPU clocks. |



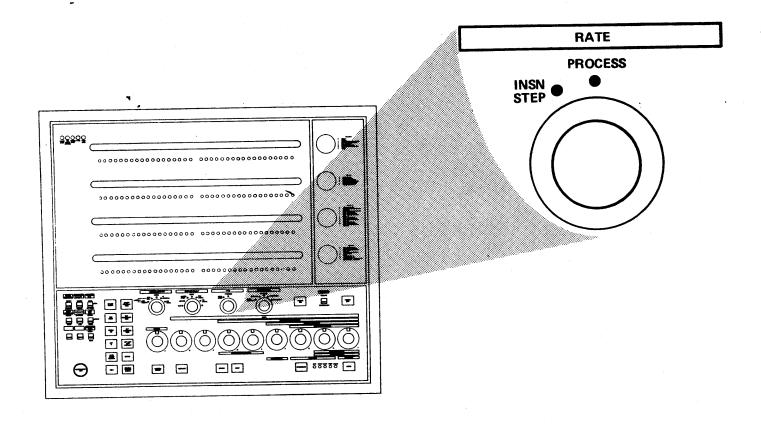
| SWITCH | POSITION | FUNCTION |
|--------------------|----------------------|--|
| ADDRESS COMPARE | | Specifies the type of main storage reference which is to be compared to the contents of the SAR Compare Register. The CPU will enter the stopped state when the compare is made. |
| | NONE | Disables the address compare operation. |
| | LOGICAL ANY CPU | Compares on any virtual address. |
| | LOGICAL CPU STORE | Compares on any virtual address used in a store operation. |
| | IC LOGICAL | Compares on any virtual address in an instruction fetch. |
| | I/O REAL | Compares on any real address used by a channel. |

STORAGE SELECT SWITCH



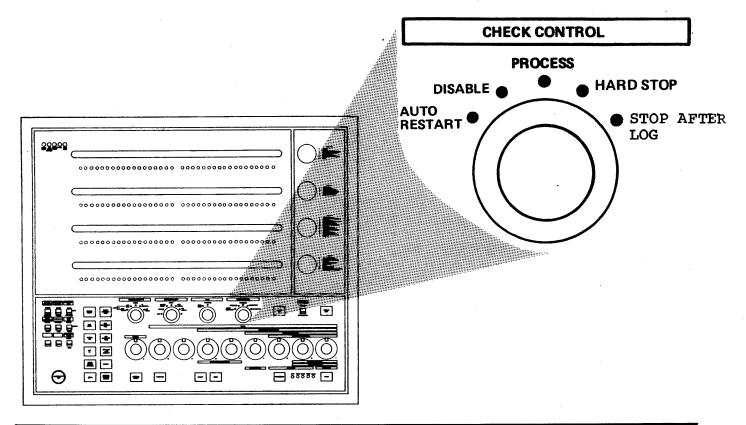
| SWITCH | POSITION | FUNCTION |
|-------------------|------------|---|
| STORAGE SELECT | | This switch selects the proper storage for manual store/display operations. |
| | MAIN | Normal program processing mode and manual store/display operations of main storage. |
| | CPU LOCAL | Selects manual store/display of general and floating point registers. |
| | I/O LOCAL | Selects manual store/display of channel LS. |
| | STORE PROT | Selects manual store/display of Key Storage. |
| | UCW | Selects manual store/display of unit Control Words. |
| | TLB | Selects manual store/display of TLB. |

RATE SWITCH

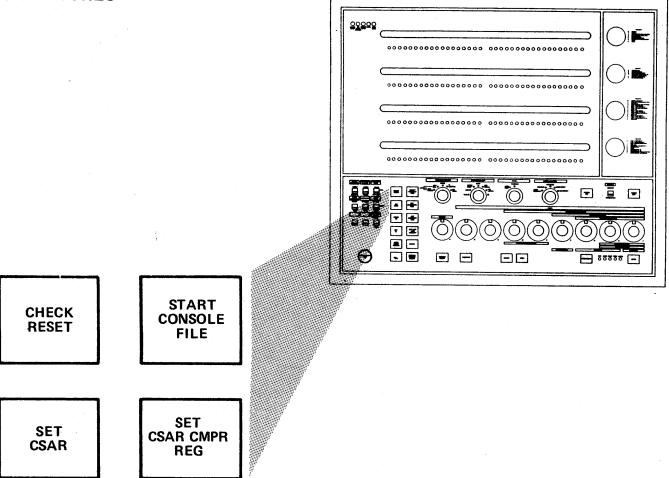


| SWITCH | POSITION | FUNCTION |
|--------|-----------|---|
| RATE | | This switch controls the rate at which the CPU processes instructions. |
| | PROCESS | Normal Program Processing. |
| | INSN STEP | In this position one complete machine lan- guage instruction (including all pending interrupts allowed by the system mask) is executed for each operation of the start key. The machine enters the manual state and the indicator turns on. The address of the next instruction is displayed in rollers 2 and 3. |

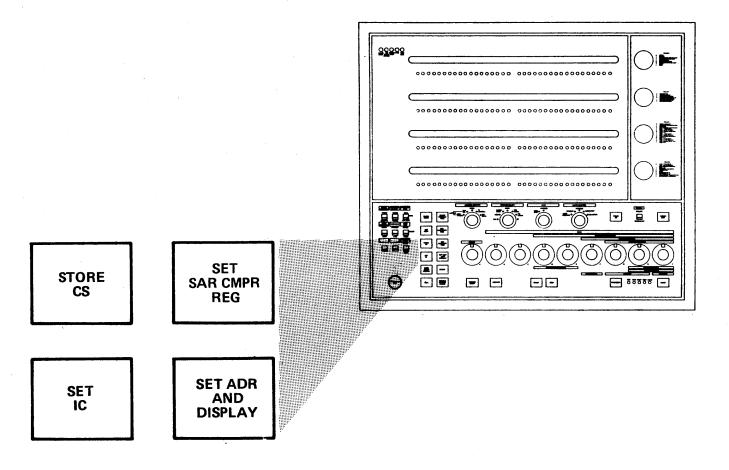
CHECK CONTROL SWITCH



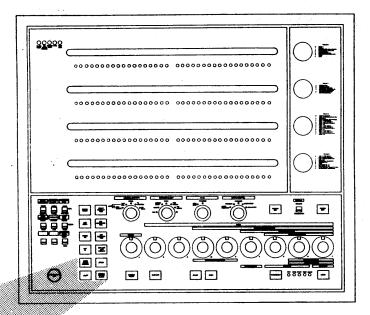
| SWITCH | POSITION | FUNCTION |
|------------------|-------------------|--|
| CHECK CONTROL | | This switch controls the action taken by the CPU when a machine check occurs. |
| ` | PROCESS | This position is for normal program processing when an operating system with automatic recording of logout data is used. |
| | HARD STOP | This position causes the machine to hard stop when an error is detected. |
| | STOP AFTER LOG | Retry is active on this position. An error causes a logout to Main Storage, the CPU then hard stops. This position is for normal program processing when an Operating System without automatic recording of logout data is used. |
| | DISABLE | This position causes all CPU errors to be ignored. |
| | AUTO RESTART | No retry is attempted, no logout is taken. Error causes PSW restart from ADDR \emptyset . |



| SWITCH | FUNCTION |
|----------------------------|--|
| CHECK RESET | Resets all machine error indicators. |
| START CONSOLE FILE | Applies power to the Console File and starts a console file read operation. |
| SET CSAR | Sets an address as specified by rotaries F thru J into control storage address register. |
| SET CSAR CMPR REG | Sets an address as specified by rotaries F thru J into CSAR compare register. |



| SWITCH | FUNCTION |
|------------------------|--|
| STORE CS | Stores the contents of rotaries A thru J into the control storage word specified by CSAR. Use of this key updates CSAR by one. |
| SET SAR CMPR REG | Sets an address as specified by rotaries D thru J into SAR compare register. |
| SET IC | Loads the contents of rotary switches D thru J into the instruction address field of the current PSW. |
| SET ADR AND DISPLAY | Set into the bottom two rows of lights the data at the main storage locations indicated by rotaries D thru J. |



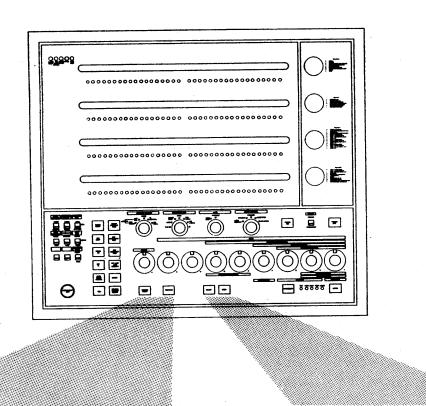
STEP/ START CLOCKS

STORE

LOG

ENABLE SYSTEM CLEAR

| SWITCH | FUNCTION |
|------------------------|--|
| STEP/START CLOCKS | Restarts CPU clock when the "clock stopped" mode is indicated. Single cycles the machine when CLOCK CONTROL switch is in the SNC CYC mode. |
| STORE | Stores rotaries A thru J into main storage at the location indicated by the preceding SET ADR AND DISPLAY. |
| ENABLE SYSTEM CLEAR | Main Storage is cleared if this key is depressed while the SYSTEM RESET or LOAD key is depressed. |
| LOG | Moves current contents of the lights to the logout buffer. No data is moved to main storage; no machine check interrupt occurs. |



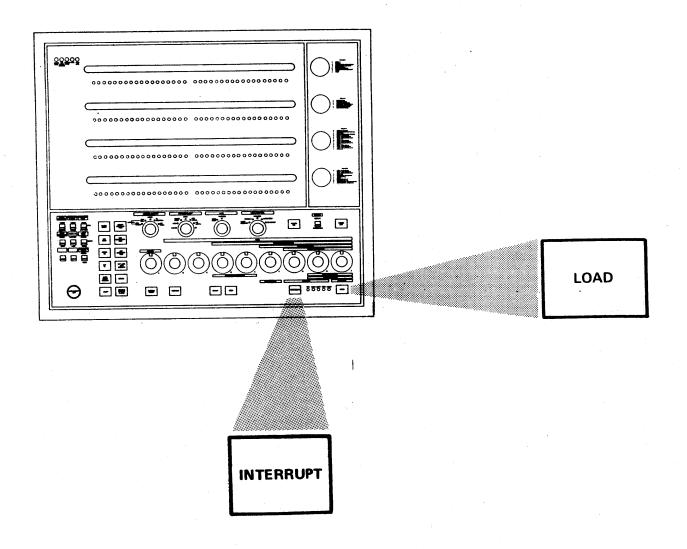
SYSTEM RESET

RESTART

START

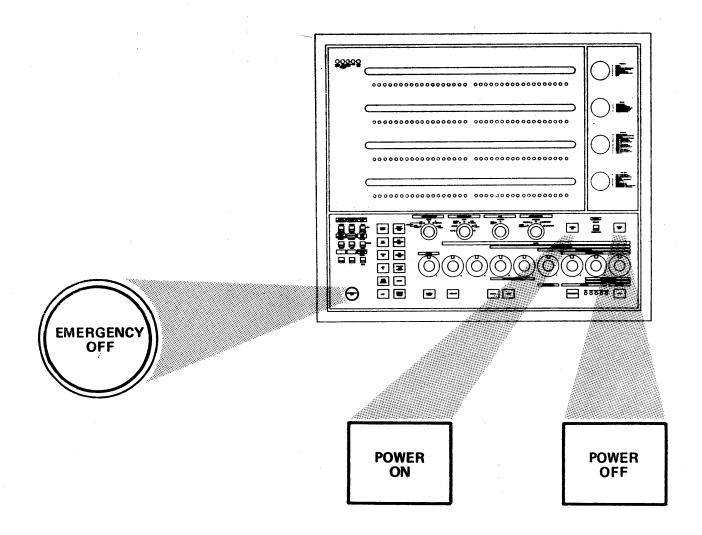
STOP

| SWITCH | FUNCTION |
|--------------|---|
| START | Initiates instruction processing. Removes CPU from Manual State. If Rate Switch = Instruction Step, processing will stop again after one instruction. |
| STOP | Stops instruction processing when the current machine instruction and pending interrupts are completed. Places CPU in Manual state. |
| RESTART | Stores the content of the current PSW in address 8, and loads the doubleword starting at address Ø as the current PSW. The channels are not reset and processing starts under control of the PSW. |
| SYSTEM RESET | Performs a system reset function. |



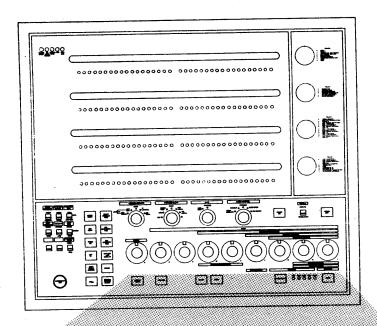
| SWITCH | FUNCTION |
|-----------|---|
| INTERRUPT | Requests an external interrupt. The in- terrupt is taken when allowed by the system mask. |
| LOAD | Starts an IPL operation. |

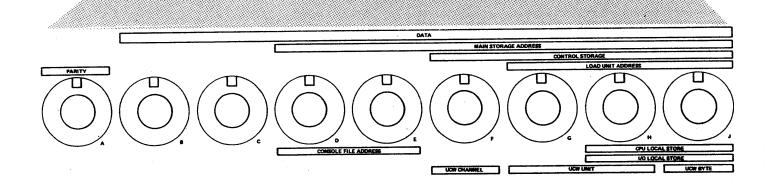
POWER SWITCHES



| SWITCH | FUNCTION |
|------------------|--|
| POWER ON | Initiates a power up sequence. |
| POWER OFF | Initiates a power down sequence. |
| EMERGENCY OFF | Initiates an unconditional power off of CPU and all attached peripherals and should ONLY be used to prevent personal injury. |

ROTARY SWITCHES A THRU J

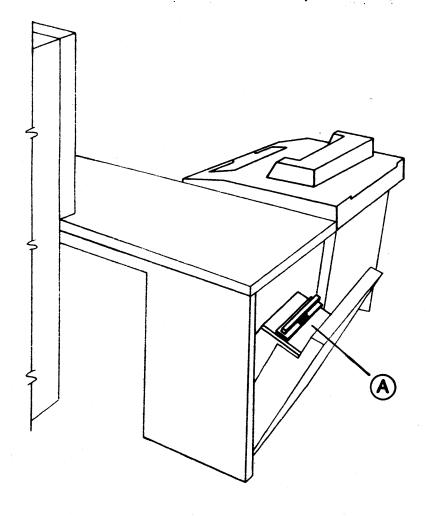




ROTARY SWITCHES A THRU J

| SWITCH | LABEL | FUNCTION |
|----------|-------------------------------|---|
| BCDEFGHJ | DATA | Specifies the value of data to be en- tered on manual store operations. |
| DEFGHJ | MAIN STORAGE ADDRESS | Specifies the main storage address for manual store/display operations. |
| FGHJ | CONTROL STORAGE ADDRESS | Specifies a control storage address for manual store/display operations. |
| GHJ | LOAD UNIT ADDRESS | Specifies the load-unit address for IPL operations. |
| А | PARITY | Specifies parity bits for each switch byte when the DATA ROT PARITY Switch is in "FORCE" mode. |
| HJ | CPU LOCAL STORE | Specifies the local storage address for manual store/display operation in con-junction with STORAGE SELECT switch CPU LOCAL position. Right-Justified |
| HJ | I/O LOCAL STORE | Specifies the I/O local storage address for manual store/display operations in conjunction with STORAGE SELECT switch I/O LOCAL position. Right-Justified |
| DEF | CONSOLE FILE ADDRESS | Specifies the track address of the console file during microprogram load operations. Right-Justified |
| J | UCW BYTE | Specifies the physical byte address when the "STORAGE SELECT" switch is in the UCW position. |
| GH | UCW UNIT | Specifies the physical unit address when the "STORAGE SELECT" switch is in the UCW position. |
| F | UCW CHANNEL | Specifies the physical channel address when the STORAGE SELECT switch is in the UCW position. |

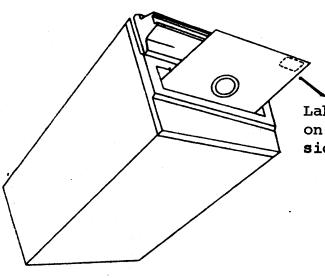
CONSOLE FILE FLEXIBLE DISK, INSERTION AND REMOVAL



TO INSERT A FLEXIBLE DISK INTO THE CONSOLE FILE:

- 1. Depress pushbutton A to open console file.
- Insert flexible disk into the load aperture with the label facing away from operator.

3. Ensure that the disk is positioned fully within the drive housing.

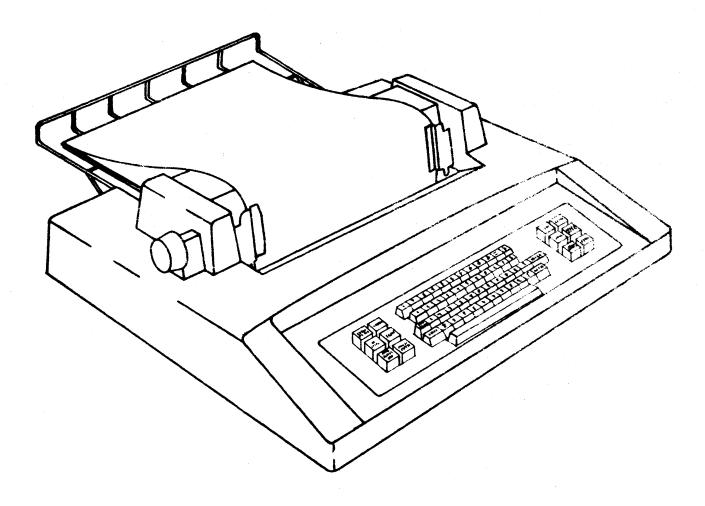


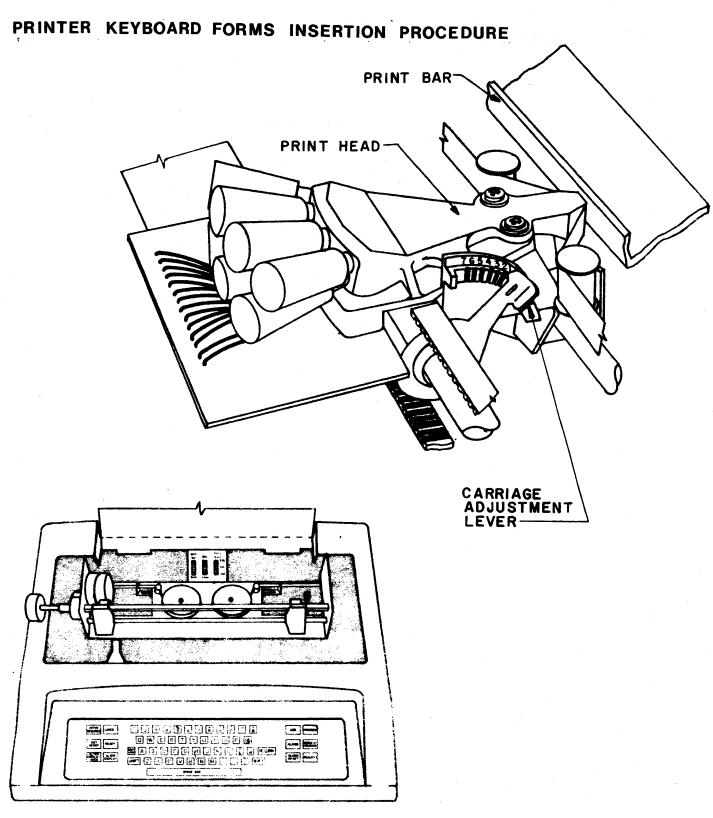
Label appears on reverse side down.

4. Close the console file by grasping the bar on the front plate and sliding it closed. The front plate will lock shut.

CONSOLE PRINTER KEYBOARD (PR-KB)

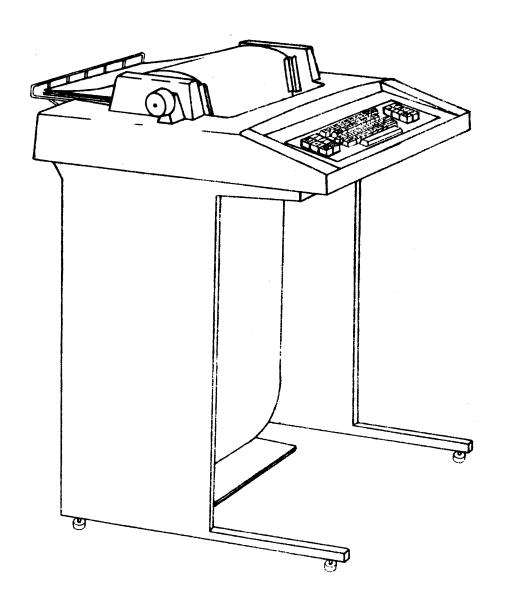
 The console printer keyboard is an input/output device which provides alter/display and control functions.





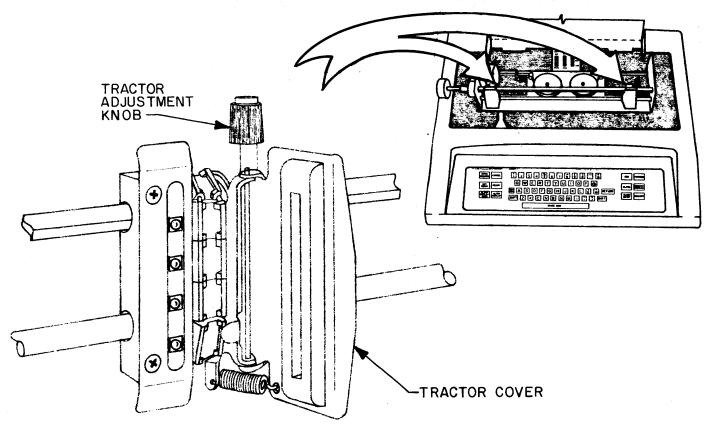
- 1. Set the POWER switch to OFF.
- 2. Move the carriage adjustment lever toward the keyboard as far as possible; this creates space for inserting the paper.

PRINTER KEYBOARD FORMS INSERTION PROCEDURE Cont.



- 3. Place the tractor-feed paper on the floor between the legs of the printer stand. (The term tractor-feed refers to the holes on either side of the paper.)
- 4. Feed the paper through the load channel under the terminal. Draw the paper up as it passes between the print head and the print bar.

PRINTER KEYBOARD FORMS INSERTION PROCEDURE Cont.



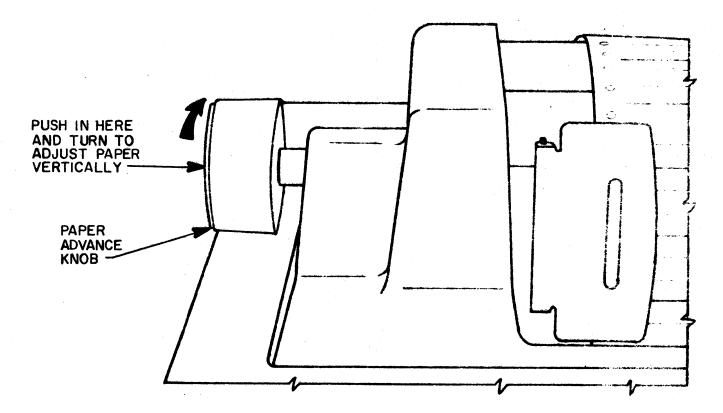
- 5. Open both tractor covers so that the tractor pins are exposed. Insert the left side of the paper with the holes aligned directly over the tractor pins. Close the left side tractor cover.
- 6. Loosen the tractor adjustment knob on the right tractor (about 1/4 turn). The tractor will now slide freely to the left or right. Slide the tractor to a position where the holes on the right margin align directly over the tractor pins. Tighten the tractor adjustment knob and close the cover.

Note:

In order to ensure proper paper feeding, do not tension paper too tightly. If the tension is excessive the following problems may occur:

- (1) Paper holes will be distorted.
- (2) Paper may become dislodged from tractor.
- (3) Spacing between lines may become uneven.

PRINTER KEYBOARD FORMS INSERTION PROCEDURE Cont.



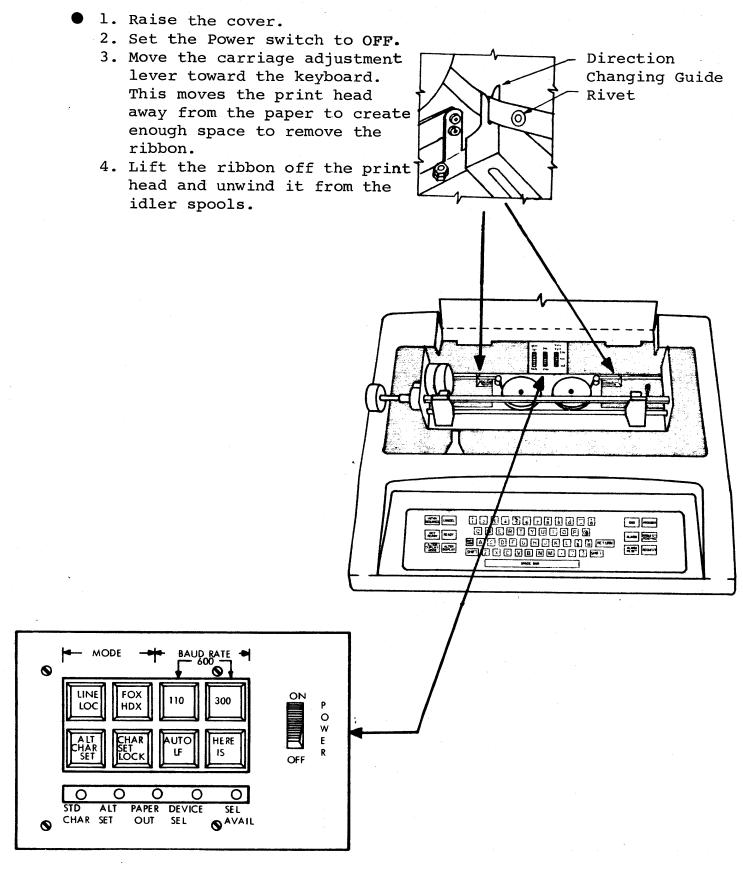
7. Adjust the carriage adjustment lever so that the print head is near, but not exerting pressure on the paper. There should be no friction between the paper and the print head as either moves.

The right side of the carriage is numbered 1-7 approximately corresponding to 1-6 part forms. Check for proper print head alignment as follows:

- Manually turn the paper advance control counterclockwise. If the print head is set too close, the paper will be smudged as it moves up past the print head.
- Set the POWER switch to ON; Set the LINE/LOCAL switch to LOCAL. Type a short line of text. If the print head is too far from the paper, characters will not print or they will have non-uniform dot density.

The paper advance control can be pushed in to position the paper such that the text is printed directly above the horizontal lines.

PRINTER KEYBOARD RIBBON REPLACEMENT PROCEDURE



PRINTER KEYBOARD RIBBON REPLACEMENT PROCEDURE Cont.

- 5. Lift the two ribbon reels from their hubs.
- 6. Place the full reel of new ribbon on the left hub and play out enough ribbon to feed around the idler spools.

Note:

Use only <u>DEC</u> recommended ribbon. (Part No. <u>36-10558</u>); use of other than this recommended ribbon can cause damage and void machine warranty.

Wind the ribbon around the outside of the idler spools and through the slot in the direction changing guide.

Make sure that the rivet is on the ribbon spool side of the direction changing guide. The direction of ribbon movement is controlled by the ribbon direction guides.

When the ribbon is nearly played out, the rivet is drawn into contact with the direction changing guide. Since the rivet cannot pass through the guide, it moves the guide away from the reel, automatically changing the direction of the ribbon flow. If the rivet is on the print head side of the guide it will:

- Not act to change the ribbon direction.
- Move around the idlers, stall the machine and blow the fuse.
- 7. Take up any slack in the ribbon by turning the takeup reel clockwise.
- 8. Return the carriage adjustment lever to its original position.
- 9. Close the cover.

PRINTER KEYBOARD OPERATOR MAINTENANCE

Do not oil the printer keyboard; moving parts are prelubricated and sealed.

Keep the cover closed at all times except when changing the ribbon.

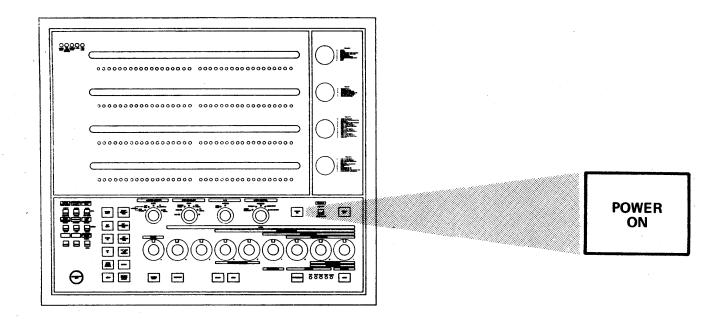
Use only a lint free cloth when cleaning the cover and the key-board. Do not use solvents or harsh cleaning agents. If excessively dirty a mild detergent or desk top cleaner may be used sparingly.

Do not use any surface of the printer keyboard to hold pencils, paper clips, staples, etc. If an object accidently falls into the machine, turn the POWER switch to OFF, unplug the power cord from the wall outlet, and carefully remove the object.

Tear the paper only along the perforations. Support paper on the cover when tearing to avoid distorting the tractor feed holes in the paper still in the machine.

Rapid off-line paper advance may be accomplished by placing the machine in LOCAL and depressing the LF and REPEAT keys simultaneously.

Power On

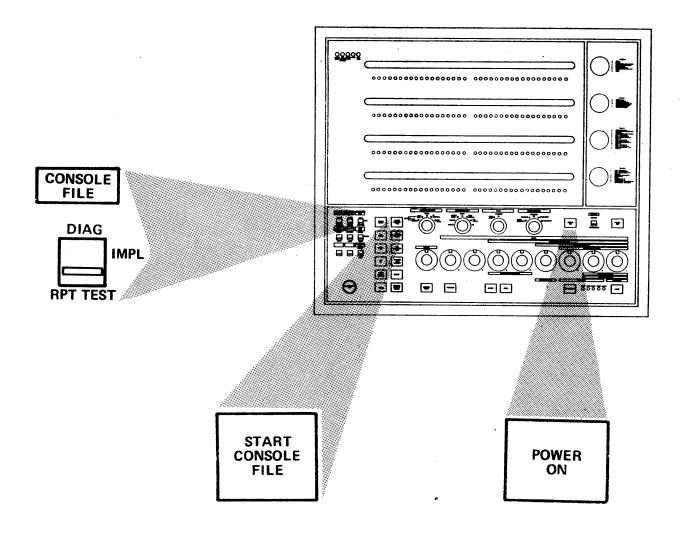


• Press the POWER-ON key

Pressing the POWER-ON key initiates a power-on sequence for the CPU and on-line I/O units. The key turns red when pressed and turns white when the power-on sequence is complete.

The time required for a power-on sequence is determined by the number and type of I/O units on-line. The contents of storage is not valid after a power-on sequence. Also, an IMPL operation is required. Note that the IMPL is automatic if the Console File switch is set to IMPL, the Clock Control toggle is set to NORMAL, the CSAR COMPARE toggle switch is set to NORM, and the microprogram disc is mounted on the console file.

Initial Microproprogram Load (IMPL)

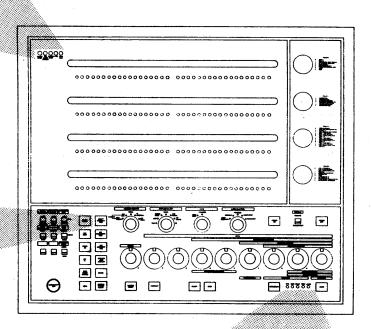


- Ensure that forms are inserted in the console PR-KB and the microprogram disc is mounted in the console file.
 - 1. If power is not on, press the POWER-ON key. An automatic IMPL occurs. (If power is on, press START CONSOLE FILE key to initiate the IMPL.)

Initial Microprogram Load (IMPL) Cont.



START CONSOLE FILE

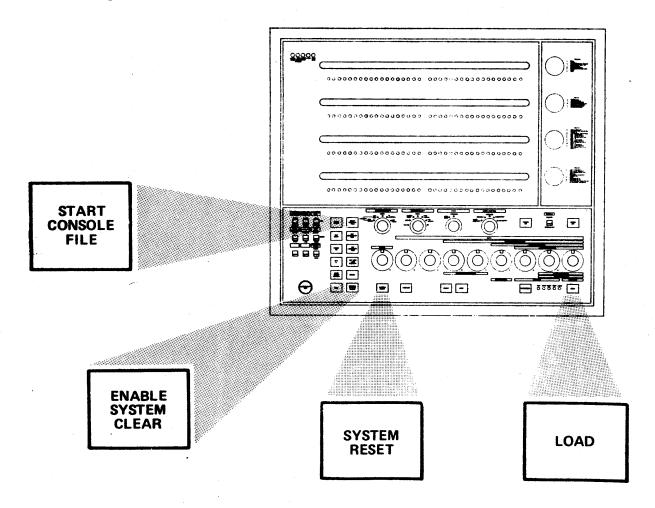


- 2. The START CONSOLE FILE key turns red.
 - When the console file starts reading, the START CONSOLE FILE key turns white.
- 3. When control storage is loaded, the console file powers off automatically and the START CONSOLE FILE key turns off.

The system reset routine executes and the CPU enters the manual state with the MAN indicator on.

The IMPL operation takes approximately 15 seconds.

Initial Microprogram Load (IMPL) Cont.

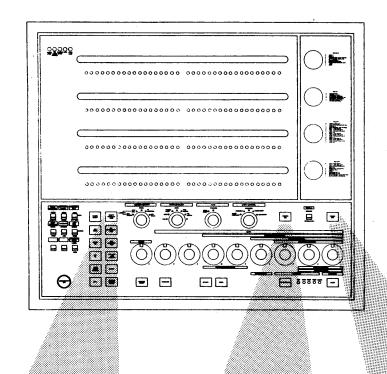


4. EXCEPTIONS

If the system has been powered on without the microprogram disc inserted in the console file, the following procedure must be performed before using the system.

- a. Insert the microprogram disc in the console file.
- b. Close cover.
- c. After IMPL is complete, perform a clear storage operation as follows:
 - (1) Press and hold ENABLE SYSTEM CLEAR key.
 - (2) Press the SYSTEM RESET or the LOAD key. All of main storage is cleared to zeros; control storage is not affected.
 - (3) Release the ENABLE SYSTEM CLEAR key.

OPERATING PROCEDURES IMPL Error Recovery



Ensure that all switches are set properly. Ensure that the flexible disc is inserted properly with the lable facing the handle of the

console file.

Attempt to re-IMPL using the START CONSOLE FILE key. If unsuccessful, press the CHECK RESET key and the POWER OFF key. Wait at least ten seconds, then re-IMPL by pressing the POWER ON key. If the problem continues. see (section 4 this manual) "HANDLING ABNORMAL

SITUATIONS, GENERAL FLOW CHART."

START CONSOLE FILE

POWER ON

POWER OFF

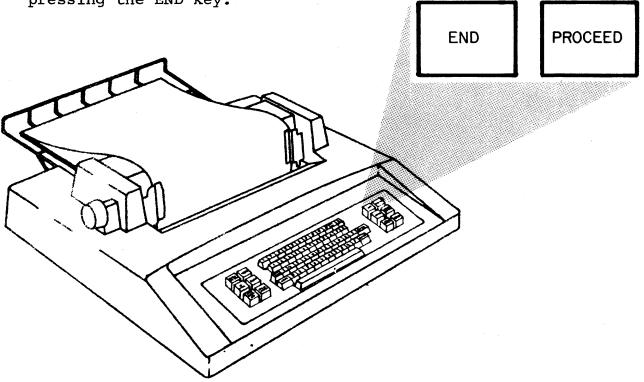
IMPL ERROR INDICATOR CHART

| INDICATOR | | | |
|------------------------------|-----------------|----------------|---|
| START CONSOLE FILE KEY | HARD STOP | CS LOAD ERR | ERROR CONDITION |
| RED | OFF or ON | OFF | DISC INSERTED UPSIDEDOWN OR BACKWARD. DISC NOT TURNING. |
| OFF | ON | ON | ERROR DURING LOADING OF CONTROL STORAGE |
| OFF | ON | OFF | CONTROL STORAGE LOADED ERROR IN EXECUTION OF SYSTEM RESET |

Console Printer-Keyboard Manual Operations

Data Entry

During a program-controlled read operation, PROCEED is turned on when the system requires data entry by the operator from the keyboard. The operation is ended by pressing the END key.



Alter/Display Operations

Alter/display operations are performed from the PR-KB. The PR-KB provides a record of the operation, the location(s) accessed, and the data involved.

Display operations print data from storage for operator inspection. The data is not changed. Alter operations change the data in storage.

Console Printer-Keyboard Manual Operations

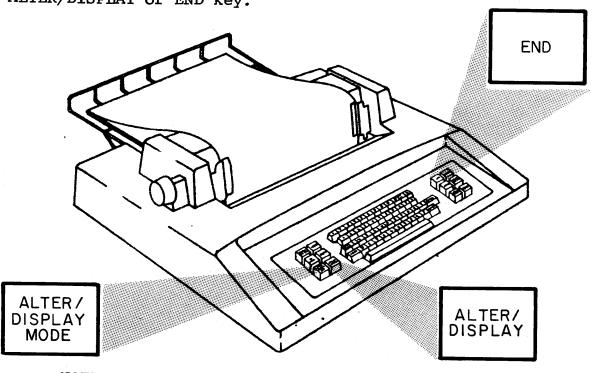
ALTER

Data is entered one hex digit at a time by using the space bar to skip over positions not being altered. The data in the skipped over positions remains unchanged and prints out each time the spacebar is operated.

To end the alter operation, press the ALTER/DISPLAY or END key.

DISPLAY

Data is printed starting at the address specified and continues until the ALTER/DISPLAY or END key is pressed, or until all data in the specific area chosen has been displayed.



NOTE:

When the operation is ended by the ALTER/DISPLAY key, the PR-KB remains in alter/display mode (ALTER/DISPLAY MODE indicator on).

When the operation in ended by the END key, alter/display mode is terminated, the machine now re-enters Manual State. When addressing main storage, word alignment is not necessary. If the starting address is not on a word boundary, the PR-KB spaces and aligns at the byte addressed.

Console Printer-Keyboard Manual Operations

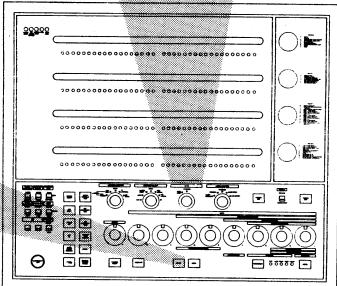
ALTER/DISPLAY PROCEDURES NOTE:

Steps 1 through 3 are common to both ALTER and DISPLAY OPERATIONS.

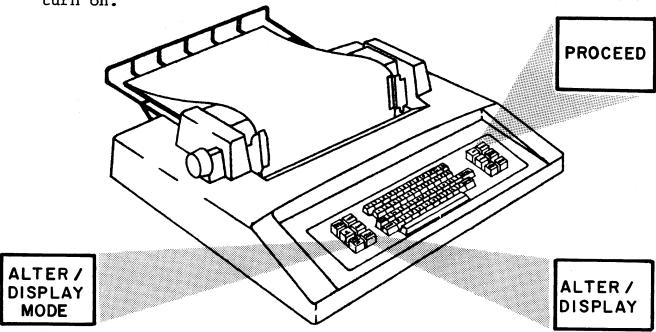
1. Place the machine in Manual state by pressing the STOP key or by setting the RATE switch to INSN STEP.

STOP

PROCESS
INSN
STEP



- 2. Press the ALTER/DISPLAY key.
- 3. Wait for both ALTER/DISPLAY MODE and PROCEED indicators to turn on.



Console Printer-Keyboard Manual Operations

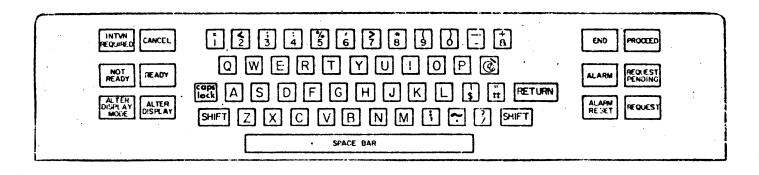
ALTER/DISPLAY PROCEDURES Cont.

4. From the following chart type the appropriate two-character mnemonic and address of the storage area or register to be altered or displayed

| STORAGE AREA | ALTER MNEMONIC | DISPLAY MNEMONIC | ADDRESS RA N GE |
|----------------------------|-------------------|---------------------|---------------------------|
| MAIN STORAGE | AM | DM | 000000-1FFFFF * |
| STORAGE KEY | AK | DK | 000000-1FFFFF * |
| CONTROL REGISTER | AC | DC | 0- F |
| GENERAL REGISTER | AG | DG | 0-F |
| FLOATING-POINT REGISTER | AF | DF | 0,2,4,6 |
| CURRENT PSW | AP | DP | None required |
| STORE STATUS | NONE | ST | None required |
| VIRTUAL STORAGE | AV | DV | 000000-FFFFFF |

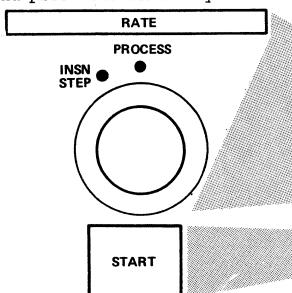
^{*}The upper boundary is movable and depends upon the capacity of main storage.

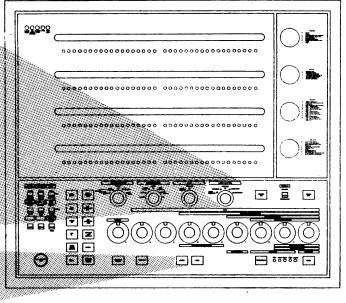
5. The display will begin immediately after the sixth digit of the address is typed. The RETURN key must be pressed after entering an address with less than six digits.



Console Printer-Keyboard Manual Operations ALTER/DISPLAY PROCEDURES Cont.

6. To continue program processing when the alter or display operation is completed return the machine to manual state and press the START key.





ALTER/DISPLAY EXAMPLES

In the following examples, the Xs represent characters displayed or entered and printed by the PR-KB.

MAIN STORAGE

DM 00008D

AM 480 (Press the RETURN key.)
XXXXXXXX XXXX (Press the ALTER/DIS-PLAY or END key.)

• FLOATING-POINT REGISTER
DF 2
XXXXXXXX XXXXXXXX XXXXXXXX ---- XX

STORAGE KEY

DK 009000

Each word contains four storage keys.

CURRENT PSW

AP XXXXXXXX XXXXXXXX

VIRTUAL STORAGE

Type in logical address: LLLLL; system types out = RRRRRR (real address)

DV LLLLL=RRRRRR

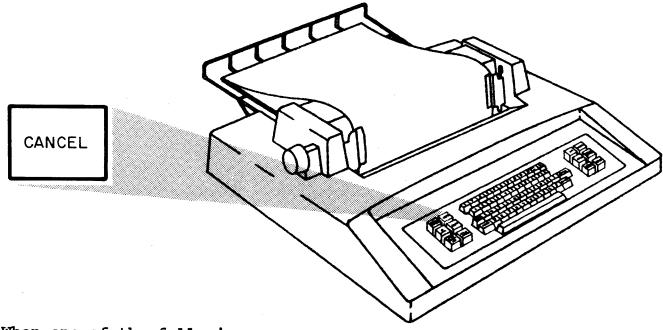
Console Printer-Keyboard Manual Operations

ALTER/DISPLAY ERROR ACTION

NO ACTION

The Console printer ignores the entered character when the following occurs:

- The first character of a mnemonic is not A,D,S or T.
- The second character is not M,K,C,G,F,P,T,V, or W.
- 3. An invalid hexadecimal digit is typed when addressing or altering data.
- 4. The CANCEL key is pressed.



When one of the following errors occur a "?" is printed.

- 1. Invalid starting address.
- Updated address exceeds the capacity of specified storage.
- 3. Non-translated logical address
 (DV LLLLLL: "?"
- 4. The translated real address exceeds the capacity of main storage. (DV LLLLLI=RRRRRR "?".

OPERATING PROCEDURES Console Printer-Keyboard Manual Operations

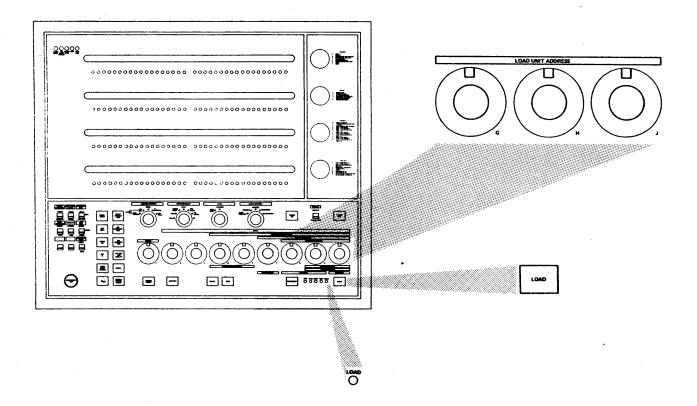
STORE STATUS

- A manually initiated function that places the programmable registers in fixed locations in processor storage.
- The function is initiated by placing the PR-KB in alter/ display mode and typing in ST.

STORE STATUS PROCEDURE

- Press the STOP key, or place the RATE switch in INSTRUC-TION STEP position. This places the CPU in a stopped state.
- Press the ALTER/DISPLAY key on the PR-KB. The PROCEED light turns on.
- 3. Type in the mnemonic ST. The function is executed, the carriage on the PR-KB returns, and the CPU exits from the ALTER/DISPLAY mode and returns to a stopped state. (No printout is given.)

Initial Program Load (IPL)



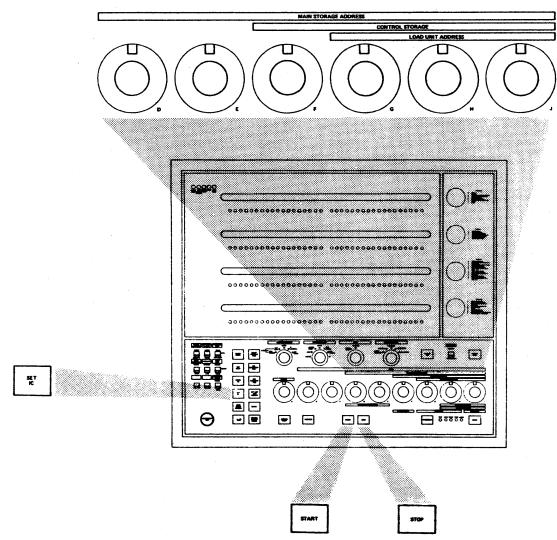
- 1. Load and ready the System Resident (SYS RES) device.
- 2. Dial the address of the IPL device into LOAD UNIT ADDRESS switches G, H, and J.
- 3. Press the LOAD key.
 - After an automatic system reset, the IPL operation starts.
 - The LOAD indicator turns on.
 - When IPL is complete, the LOAD indicator turns off and the system executes the program.

IPL ERROR RECOVERY

- Are the LOAD UNIT ADDRESS switches G, H, and J correct?
- Is SYS RES device ready?

If the setup is correct and IPL errors still occur, see (section 4 of this manual) "Handling Abnormal Situations, General Flowchart."

SET IC (Instruction Counter)



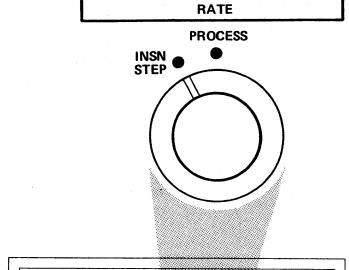
- 1. Press the STOP key.
- 2. Dial the desired address into MAIN STORAGE ADDRESS switches D, E, F, G, H, J.
- 3. Press the SET IC key.

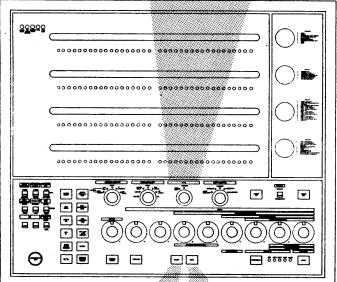
The set instruction counter operation loads the address from switches D, E, F, G, H, J into the instruction counter. Instruction processing starts from this address when the START key is pressed.

Instruction Step

1. Press the STOP key.

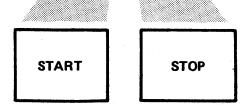
2. Set the RATE switch to INSTRUCTION STEP.





3. Press the START key.

One machine language instruction is executed for each operation of the START key. The instruction counter (displayed on roller 2 and 3 indicators) contains the address of the next instruction to be executed.



Clear Storage

 Main storage can be cleared to zeros using the following procedure.

> 1. Hold the ENABLE SYSTEM CLEAR key in the operated position. **ENABLE** SYSTEM CLEAR Press the SYSTEM RESET or 2. LOAD key. All of main storage is cleared SYSTEM LOAD

RESET

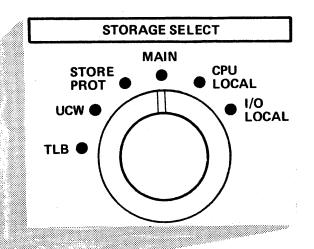
3. Release the ENABLE SYSTEM CLEAR key.

to zeros (hexadecimal 00); con-

trol storage is not affected.

OPERATING PROCEDURES Manual Store/Display Operations

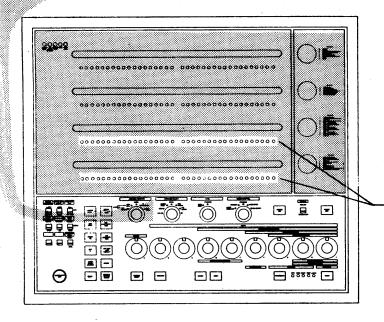
The MAN indicator must be on for the STORE and DISPLAY keys to be operative. If the CPU is running, press the STOP key to turn on the MAN indicator.



Main Storage

With the system in manual mode (MAN indicator on), store/display of main storage is performed as follows:

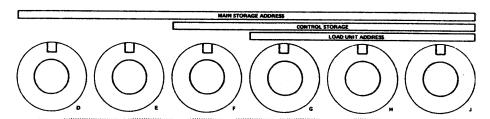
 Set the STORAGE SELECT switch to MAIN.



NOTE:

After step 2, data will be displayed on roller 2 & 3 indicators.

Manual Store/Display Operations Cont.

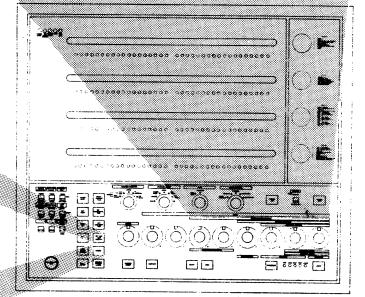


Main Storage Cont.

Dial the desired word address into rotary switches, D,E,F, G,H,J. Press SET ADR AND DISPLAY key. Data is displayed on roller 2 and 3 indicators.

> SET ADR AND DISPLAY

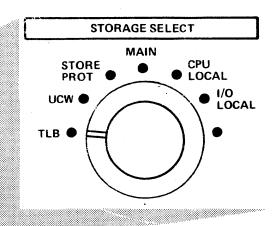
3. For a store operation, set rotary switches B thru J to the Hexadecimal word value to be stored and press STORE key.



STORE

OPERATING PROCEDURES Manual Store/Display Operations, Cont.

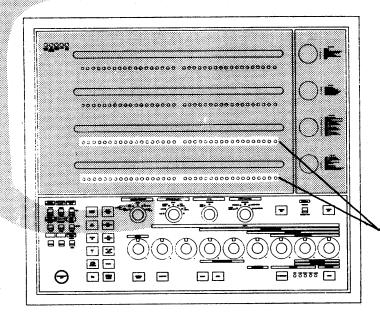
The MAN indicator must be on for the STORE and SET ADR AND DISPLAY keys to be operative. If the CPU is running, press the STOP key to turn on the MAN indicator.



TLB Storage

With the system in manual mode (MAN indicator on), store/display of TLB storage is performed as follows:

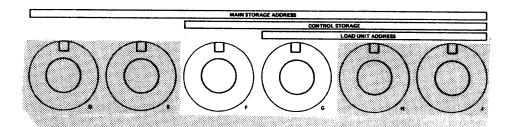
1. Set the STORAGE SELECT switch to TLB.



NOTE:

After step 2, data will be displayed on roller 2 & 3 indicators. The correct field labeling for this data can be found on roller 3 position E.

Manual Store/Display Operations Cont.

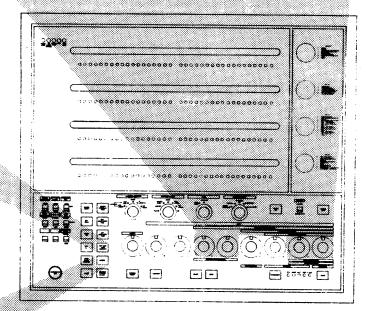


TLB Storage, cont.

Dial the desired address into rotary switches F and G. Press SET ADR AND DISPLAY key. Data is displayed on roller
 and 3 indicators. The correct field labeling for this data can be found on roller 3 position E.

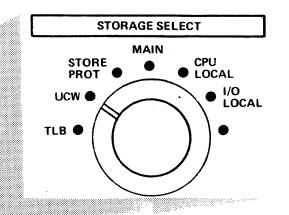


3. For a store operation, set rotary switches D thru J to the Hexadecimal value to be stored and press STORE key.



Manual Store/Display Operations Cont.

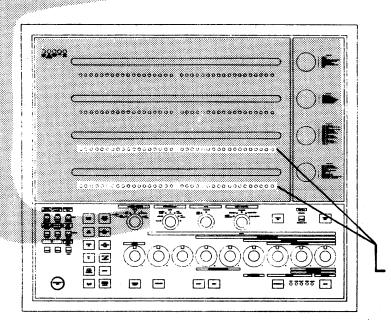
The MAN indicator must be on for the STORE AND SET ADR AND DISPLAY keys to be operative. If the CPU is running, press the STOP key to turn on the MAN indicator.



UCW Storage

With the system in manual mode (MAN indicator on), store/display of UCW storage is performed as follows:

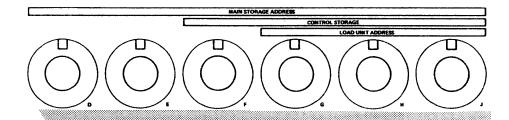
1. Set the STORAGE SELECT switch to UCW.



NOTE:

After step 2, data will be displayed on roller 2 & 3 indicators.

Manual Store/ Display Operations Cont.

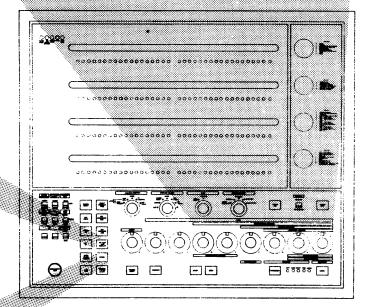


UCW Storage Cont.

2. Dial the desired word address into rotary switches, F, G, H,J. Press SET ADR AND Dis-PLAY key. Data is displayed on roller 2 and 3 indicators.

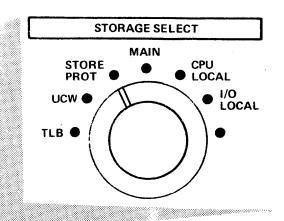


3. For a store operation, set rotary switches B thru J to the Hexadecimal word value to be stored and press STORE key.



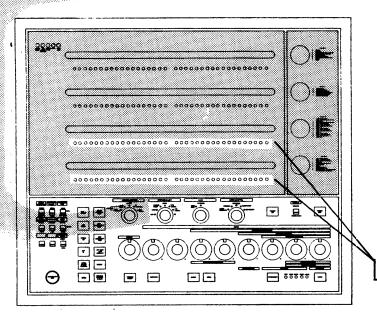
Manual Store/Display Operations Cont.

The MAN indicator must be on for the STORE and SET ADR AND DISPLAY keys to be operative. If the CPU is running, press the STOP key to turn on the MAN indicator.



Store Prot Storage

With the system in manual mode (MAN indicator on), store/display of STORE PROT STORAGE is performed as follows:

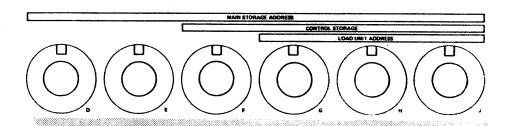


 Set the STORAGE SELECT switch to STORE PROT.

NOTE:

After step 2, data will be displayed on roller 2 & 3 indicators.

Manual Store/Display Operations Cont.

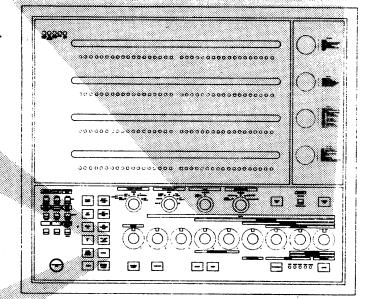


Store Prot Storage, cont.

2. Dial the desired address into rotary switches, D,E,F,G. Press SET ADR AND DISPLAY key. Data is displayed on roller 2 and 3 indicators, leftmost byte. The correct field labeling for the data can be found on roller 3 position E.

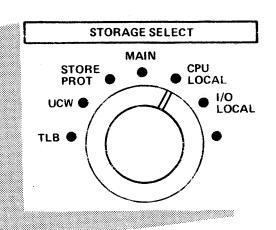


3. For a store operation, set rotary switches B and C to the Hexadecimal value to be stored and press STORE key.



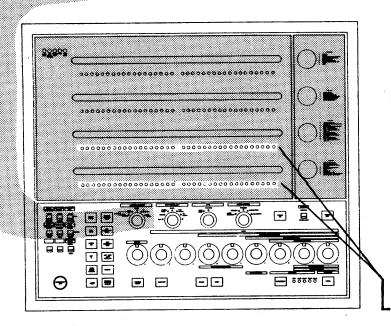
Manual Storage/Display Operations Cont.

The MAN indicator must be on for the STORE and SET ADR AND DISPLAY keys to be operative. If the CPU is running, press the STOP key to turn on the MAN indicator.



CPU Local Storage

With the system in manual mode (MAN indicator on), store/display of CPU LOCAL STORAGE is performed as follows:

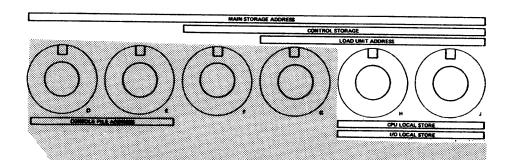


1. Set the STORAGE SELECT switch to CPU LOCAL.

NOTE:

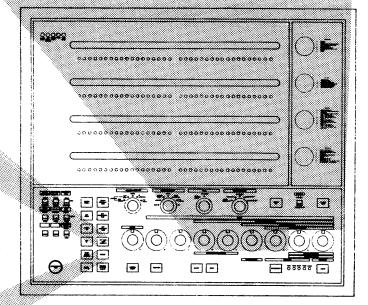
After step 2, data will be displayed on roller 2 & 3 indicators.

Manual Storage/ Display Operations Cont.



CPU Local Storage Cont.

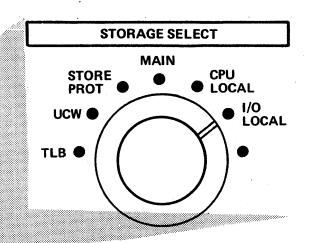
- 2. Dial the desired word address, right justified, into rotary switches, H, J. Press SET ADR AND DISPLAY key. Data is displayed on roller 2 and 3 indicators.
- 3. For a store operation, set rotary switches B thru J to the Hexadecimal word value to be stored and press STORE key.





Manual Storage/ Display Operations Cont.

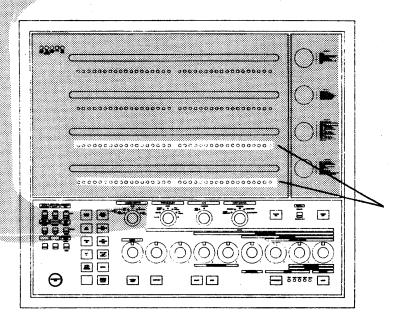
• The MAN indicator must be on for the STORE and SET ADR AND DISPLAY keys to be operative. If the CPU is running, press the STOP key to turn on the MAN indicator.



I/O Local Storage

With the system in manual mode (MAN indicator on), store/display of I/O LOCAL STORAGE is performed as follows:

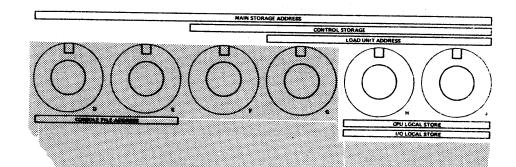
1. Set the STORAGE SELECT switch to I/O LOCAL.



NOTE:

After step 2, data will be displayed on roller 2 & 3 indicators.

Manual Storage/Display Operations Cont.

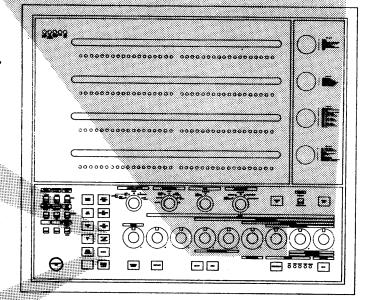


I/O Local Storage Cont.

2. Dial the desired word address into rotary switches, H. J. Press SET ADR AND DISPLAY key. Data is displayed on roller 2 and 3 indicators.



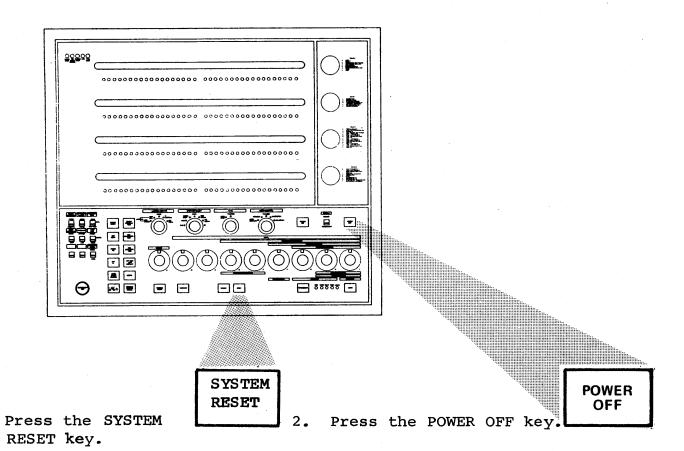
3. For a store operation, set rotary switches B thru J to the Hexadecimal word value to be stored and press STORE key.



Power Off Procedure

1.

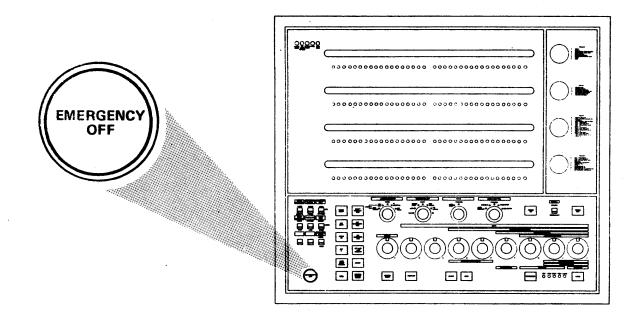
Pressing the POWER-OFF key removes power to the CPU and online I/O units. Main and control storage information is lost.



NOTE:

If the system is powered-off do not turn power back on for at least ten seconds. If the POWER-ON key is pressed before ten seconds have elapsed, a power check may occur.

Emergency Off Switch



Pushing the EMERGENCY OFF switch turns off electrical power to the CPU and online I/O units, and makes the POWER ON key ineffective until the EMERGENCY OFF switch is reset by a service representative.

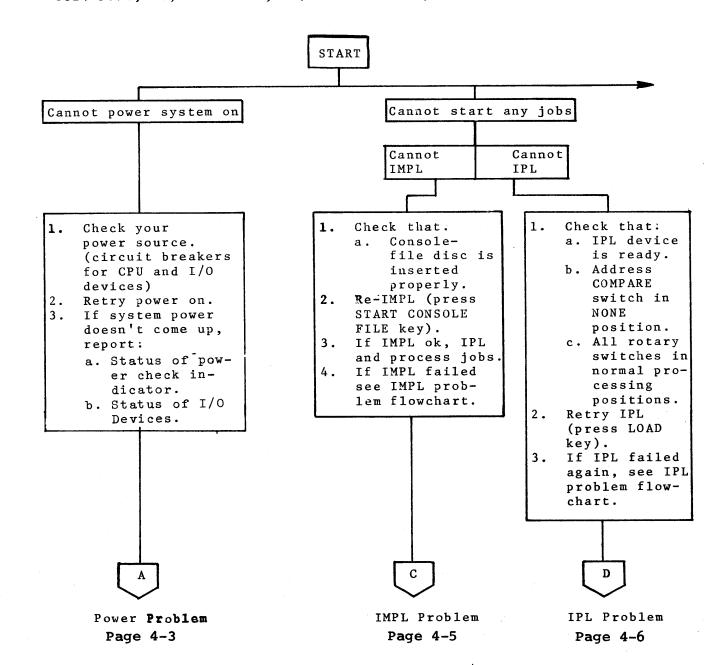
CAUTION

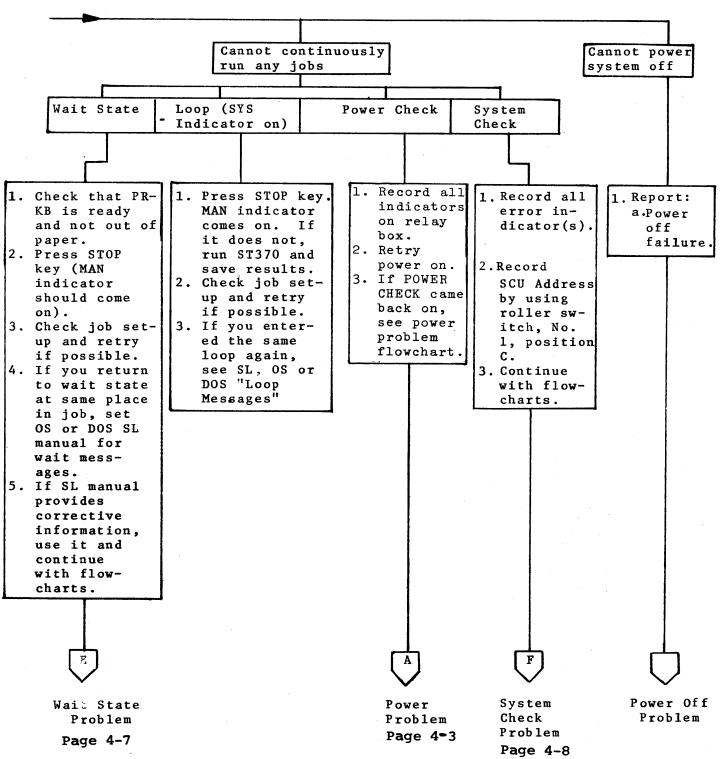
Push the EMERGENCY OFF switch in a true emergency only (a system fire or in case of danger to personnel).

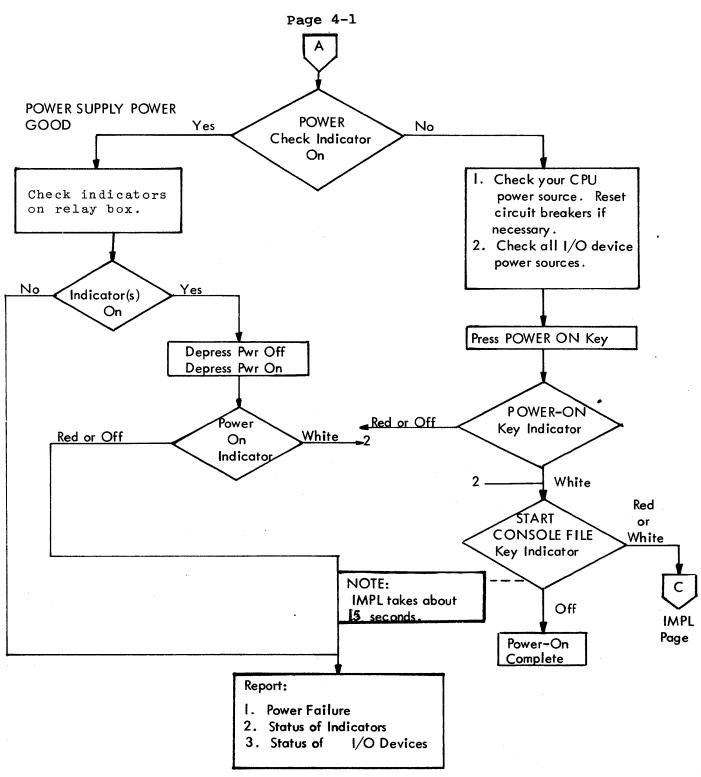
SECTION 4

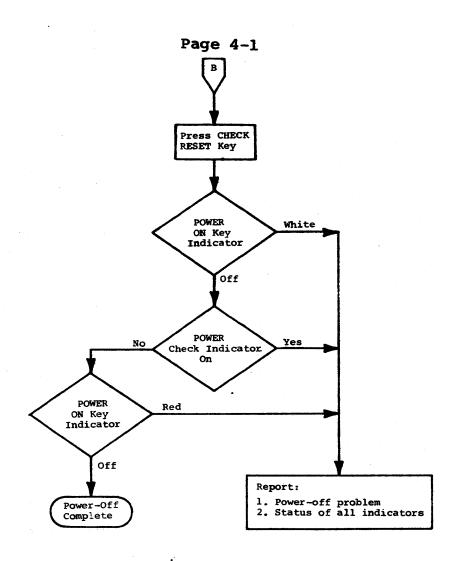
HANDLING ABNORMAL SITUATIONS

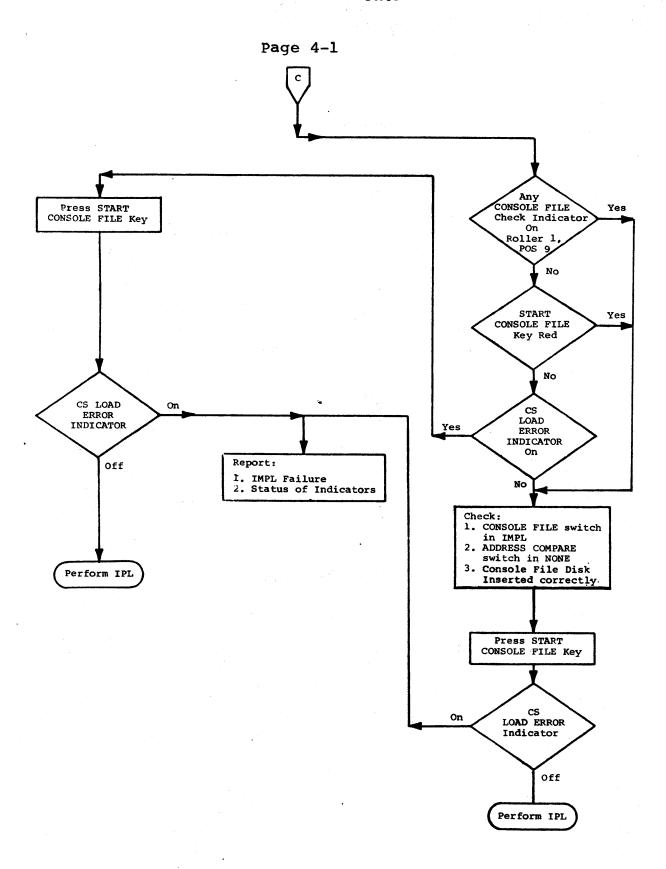
 Comply with all OS, DOS, or OS/VS messages before proceeding into flow. (Refer to appropriate Systems Library Manual: DOS, GC24-5074; OS, GC28-6631, OS/VC GC38-1001.)

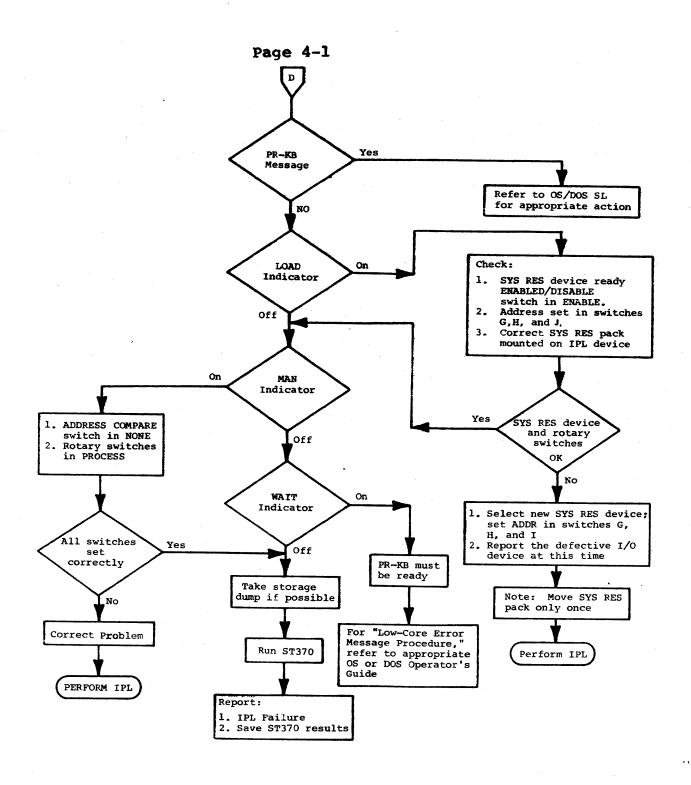


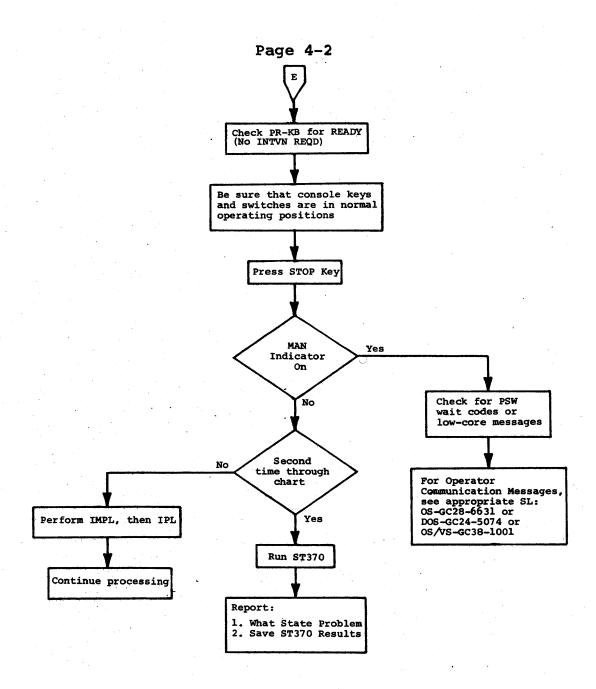


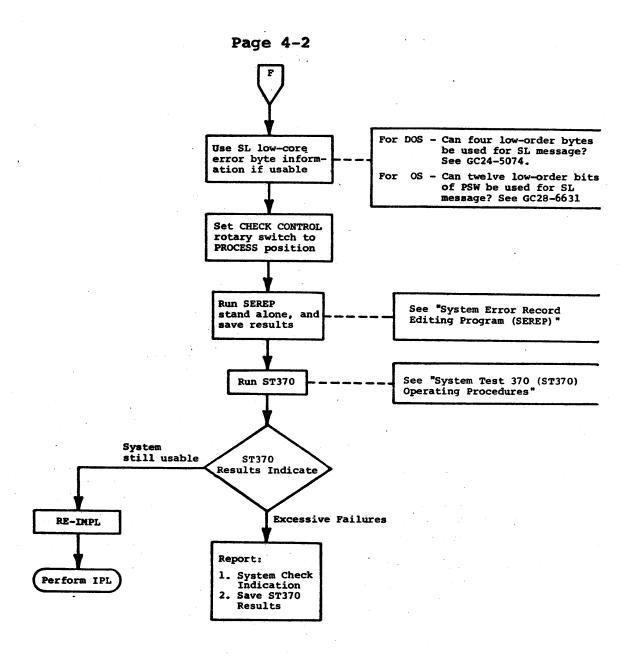












AA3419 REV. 11/69 A

COMMENT SHEET

| MANUAL TITLE | Control Data | OMEGA/480-Model I Operating Procedures |
|-----------------|---------------|--|
| PUBLICATION NO. | 22291360 | REVISION A |
| FROM: | NAME:BUSINESS | |

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