

**HARDWARE REFERENCE
MANUAL**

**CGC 7900 SERIES
COLOR GRAPHICS COMPUTERS**

CHROMATICS

CGC 7900 COLOR GRAPHICS COMPUTER SYSTEM

HARDWARE REFERENCE MANUAL
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TABLE OF CONTENTS

INTRODUCTION	1
CGC 7900 HARDWARE OVERVIEW	2
CPU CARD	3
EPROM/RASTER PROCESSOR CARD	4
BUFFER MEMORY CARDS	5
IMAGE MEMORY CARDS	5
CONFIGURATION OF MEMORY CARDS	5
VIDEO CONTROL CARDS	6
DMA/PIO	7
SERIAL PORT CONTROLLER	8
POWER SUPPLY	9
CGC 7900 SYSTEM MEMORY MAP (Illustration)	11
CGC 7900 MEMORY MAP	13
EPROM	14
EPROM INSTALLATION	15
IMAGE MEMORY	16
PLANE MODE	17
Z MODE	18
COLOR STATUS MODE	20
COLOR LOOKUP TABLE	22
COLOR LOOKUP TABLE ADDRESSES	23
OVERLAY MEMORY ADDRESSING	24
OVERLAY CHARACTER CELL ADDRESSES	26
CGC 7900 DETAILED MEMORY MAP	27
CONFIGURING 128K BUFFER MEMORY CARDS	31
CONFIGURING 512K BUFFER MEMORY CARDS	32
BUFFER MEMORY CARD ADDRESS SELECTION	33
CONFIGURING IMAGE MEMORY PLANES	34
IMAGE MEMORY CONFIGURATION JUMPERS	40
HARDWARE LATCHES AND CMOS/STATIC RAM	41
BITMAP ROLL COUNTER	42
X PAN	43

Y PAN	44
X AND Y ZOOM	45
BLINK SELECT	46
PLANE SELECT	47
PLANE VIDEO SWITCH	48
COLOR STATUS FOREGROUND/BACKGROUND	49
OVERLAY ROLL COUNTER	50
IMAGE SELECT	51
OVERLAY CURSOR BLINK	51
OVERLAY CHARACTER BLINK	51
I/O MAP	53
SERIAL PORTS	54
SERIAL PORT PINOUTS	55
INTERFACING RS232 AND RS449	56
BAUD RATE GENERATOR	57
JOYSTICK	58
BEZEL SWITCHES	60
INTERRUPT HANDLING	61
INTERRUPT MASK	62
BUS INTERRUPTS (BINT)	63
BUS CHIP SELECTS	64
BCS1 ADDRESSES	65
LIGHT PEN	65
SYNC ADDRESSES	66
BUFFER MEMORY PARITY	67
DISK PORT	68
DISK PORT PINOUT	70
REAL TIME CLOCK	71
PROGRAMMABLE SOUND GENERATOR	74
PROGRAMMING THE PSG	75
PSG REGISTERS	76
PSG MUSICAL NOTES	78
KEYBOARD	79
KEYBOARD CABLE PINOUT	81
KEYBOARD DATA BUS	82
KEYBOARD LED SELECT CODES	83
INTERFACING PERIPHERALS	84
KEYBOARD TIMING	85
HARDWARE VECTOR GENERATOR	87

SAMPLE HVG PROGRAMS	89
INTERFACE SUGGESTIONS	91
SYNC SIGNALS	93
HORIZONTAL TIMING	95
VERTICAL TIMING	96
CGC 7900 SYSTEM BUS	97
P1 CONNECTOR IDENTIFICATION	98
P1 SIGNAL DESCRIPTIONS	100
P2 CONNECTOR IDENTIFICATION	103
P2 SIGNAL DESCRIPTIONS	105

INTRODUCTION

This manual provides hardware information to users of Chromatics CGC 7900 Color Graphics Computer System. The information contained in this manual should be considered proprietary in nature. It is provided solely to aid our customers in interfacing to the 7900 hardware.

This manual should be used in conjunction with other CGC 7900 manuals. The 7900 Operator's Manual gives detailed information about standard 7900 firmware, including the graphics functions and the Terminal Emulator program, TERMEM. The 7900 DOS Manual describes the Disk Operating System, MC68000 assembler, and text editor, which will be useful in developing programs on the 7900. The 7900 also supports the Idris multi-tasking operating system, and complete Idris documentation is also available from Chromatics.

The information in this manual will be of assistance in writing custom software drivers for the 7900 hardware. Be aware, however, that nearly all of the 7900 system can be controlled through the Terminal Emulator program and routines in standard firmware. It will not be necessary to re-invent the wheel in many applications.

While the information in this document is believed to be accurate, no guarantees are made. Chromatics reserves the right to make product changes at any time.

CGC 7900 HARDWARE OVERVIEW

The CGC 7900 is a self-contained computer system. It is capable of extremely high-resolution color graphics displays. The 7900 Central Processing Unit (CPU) uses the MC68000 microprocessor. The system may be equipped with a hard disk and two floppy disks, a light pen, joystick, and several megabytes of memory for images and programs.

The chassis contains a motherboard with 12 or 24 card connectors. The lower portion of the chassis houses the digital electronics, and the upper portion contains the analog circuitry. Power supplies and the hard disk drive are mounted in the bottom of the chassis. Six fans mounted below the card cage ventilate the chassis. The system is mounted on casters for easy transportation.

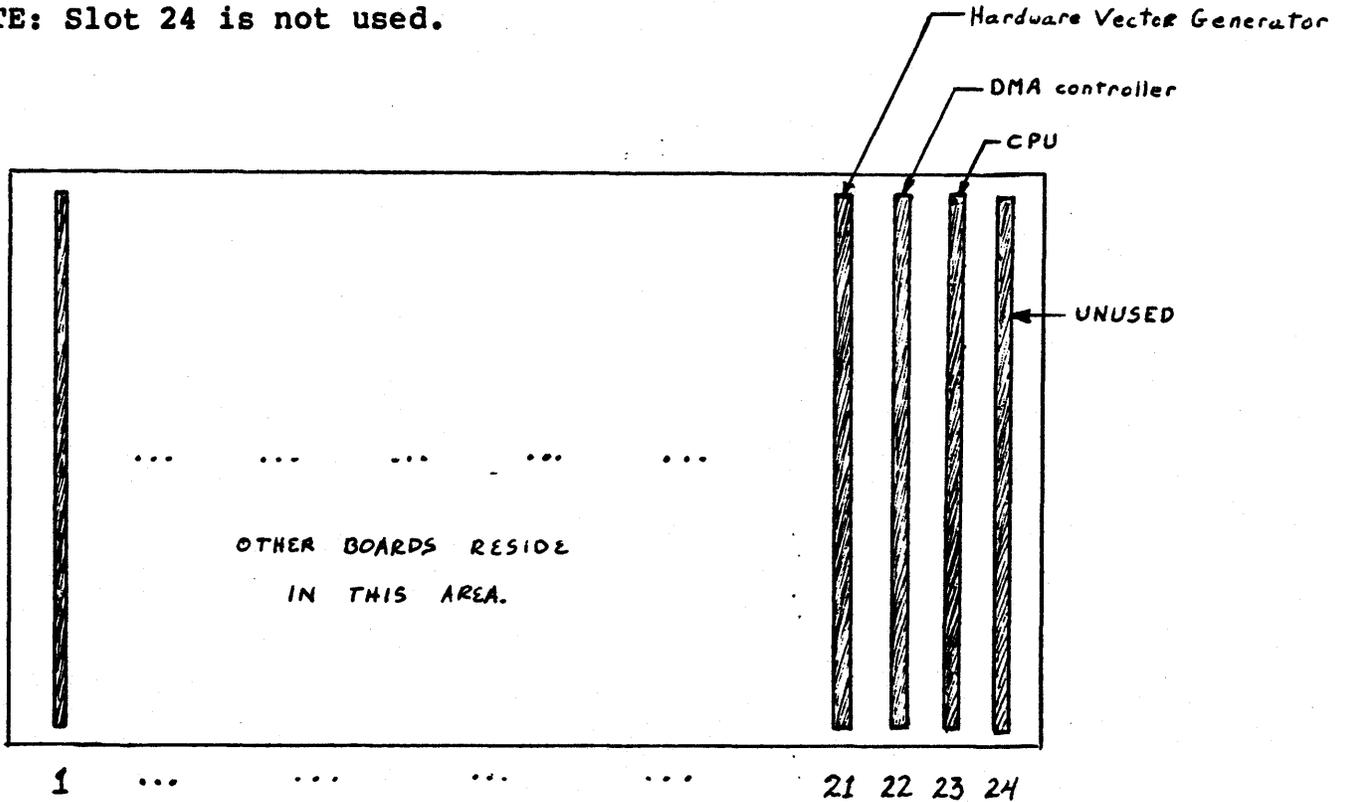
The analog chassis contains a high-resolution, 19-inch color Cathode Ray Tube (CRT). The CRT is treated with a long persistence phosphor, to minimize the problem of interlace flicker. All high voltages are present only in the analog chassis.

CGC 7900 Addendum -- Card cage layout

The following information corrects any previous information on this topic.

All bus masters (CPU, DMA, hardware vector generator) must be in the highest numbered slots in the CGC 7900 card cage. Thus, bus master boards work their way downward from slot 23. The Raster Processor must be in slot 1. Bitmap boards begin in slot 5 and work toward higher slots. I/O and memory boards pick up where the bus master boards leave off and work downward.

NOTE: Slot 24 is not used.



Hypothetical CGC 7900 card cage

CPU CARD

The CGC 7900 Central Processing Unit (CPU) card contains the MC68000 microprocessor, which can directly address 16 Megabytes of memory. This card generates most of the control signals used by the processor to control memory.

The CPU card contains 4K bytes of static memory. This may optionally be replaced by CMOS memory, powered by a battery backup supply on this card. The CMOS option includes a Real-Time Clock, also located on the CPU card.

All input/output interface hardware in the standard 7900 system is found on the CPU card. This includes the keyboard, joystick, disk, bezel keys, and two serial ports. I/O is connected to the CPU card by edge connectors on the back of the card. Each of the I/O interfaces is discussed in a separate section of this manual.

A Programmable Sound Generator is installed on the CPU card. It may be operated by the CGC system programs or by user programs. It connects to a speaker, below the keyboard, on the chassis front. A Quiet Lock key on the keyboard disables the speaker.

EPROM/RASTER PROCESSOR CARD

EPROM sockets on this card are addressed from 800000 to 80FFFF. The EPROMs must be 2532 type (32K bits), 350 nanoseconds or faster. See the "Memory Map" section of this manual for programming requirements.

The Raster Processor is a bipolar circuit, microprogrammed to perform an address translation function in the 7900 system. This device assists the MC68000 in moving pixels on the image memory screen.

This card also contains bus terminators which decrease noise on the motherboard. Because of the extremely high processor speeds (up to 8 MHz), these terminators are very important in the 7900 system.

BUFFER MEMORY CARDS

The 7900 contains one or more Buffer Memory cards. Each card holds 128K or 512K bytes of dynamic RAM for system memory requirements and user programs. The first card is addressed at zero, and other cards are usually addressed consecutively.

Each card stores a parity bit for each byte of data stored. Parity is stored with each write, and checked with each read. If a parity error is detected the card will notify the processor. Systems which use the parity checking feature must write data to ALL buffer memory when the system is powered-up, or risk a parity error if a location is read that was not previously written. (Parity checking will only function if a parity jumper is installed on each Buffer Memory card.)

IMAGE MEMORY CARDS

Up to 16 Image Memory cards, or planes, may be installed in the 7900. The number of planes determines how many simultaneous colors may be displayed in the high-resolution Bitmap memory. Typical systems will contain 1, 4, 8 or 16 Image planes.

Each plane may be accessed through several addressing modes. These are discussed under "Image Memory" in the Memory Map section of this manual. Because of the varied addressing modes, a plane might respond to addresses anywhere between A00000 and E1FFFF.

CONFIGURATION OF MEMORY CARDS

A later section of this document discusses the requirements for configuring memory cards (setting switches and jumpers).

VIDEO CONTROL CARDS

Three cards in the 7900 are used for generating and controlling the video image. These are the Overlay, Color Lookup, and Memory Controller. These cards have no programmable functions, and the descriptions below are for information only.

The Memory Controller generates all signals for operating the video memories. It allows CPU accesses, refresh accesses, and video data accesses to occur without conflicts. It produces refresh signals to sustain the dynamic RAM chips in the image memories. A ribbon cable connects the Memory Controller to the Raster Processor. This path allows the Raster Processor full access to the image memory in several addressing modes. A twisted-pair cable carries sync signals from the Memory Controller to the analog chassis.

The Overlay contains the 85 by 48 character-cell memory, and logic to generate Overlay characters and plot dots, with their associated attributes. This information is carried to the Color Lookup card over a ribbon cable. Light Pen logic is also on the Overlay.

The Color Lookup card receives image data from up to 16 Refresh Planes. Each pixel is used as an index into a high-speed RAM table, which contains the color lookup assignments. Data out of the lookup RAM is combined with Overlay data, according to the transparency attributes of the Overlay. This combined data is sent up to the analog chassis where it is converted to analog video signals by D-to-A converters. The Color Lookup is a three-layer card, to provide shielding for the high-speed ECL logic.

DMA/PIO

The 7900 DMA/PIO is an optional card. It contains a DEC-compatible DMA interface, capable of connecting to a DRV-11B, DR11-W, or DR11-B interface. The DMA interface uses two 16-bit parallel ports, one for input and one for output, and supports burst or single-cycle DMA transfers up to 500K transfers per second.

The PIO section of the DMA/PIO card is a general-purpose parallel input/output port. It has two 16-bit parallel ports, one for input and one for output; these can also be used as 8-bit parallel ports. The PIO can operate through polled or interrupt-driven software, at rates up to 150K transfers per second (software-dependent).

Additional information on the PIO/DMA hardware is available from Chromatics, in a separate document.

(DEC, DRV-11B, DR11-W, and DR11-B are trademarks of Digital Equipment Corporation.)

SERIAL PORT CONTROLLER

The 7900 Serial Port Controller (SPC) is an optional card. It contains four RS232 serial I/O ports, and an onboard Z80 processor to handle buffering and handshaking.

The SPC holds up to 8K bytes of EPROM (2532 type). It also has 4K of onboard RAM for the Z80's use in buffering data, and 1K of two-port RAM for data transfer between the 68000 and the Z80. 16 baud rates are standard. User-written firmware may be installed to support external clocking and synchronous protocols.

Additional information on the SPC is available from Chromatics, in a separate document.

POWER SUPPLY

The 7900 is powered by high-efficiency switching power supplies. The switching frequency is approximately 25 KHz, and is synchronized to the system clocks. Either one or two power supplies may be installed, depending on the options ordered in a 7900 unit. All voltages from the supplies are regulated, eliminating the need for on-card regulation.

Power supply A is always installed. It provides power for a 7900 without disk drives, and with less than 12 cards installed in the card cage. Supply A delivers the following outputs:

- +5 Volts at 20 Amps
- 5 Volts at 10 Amps

- +6.3 Volts at 1 Amp

- +12 Volts at 7 Amps
- 12 Volts at 0.3 Amp

- +25 Volts at 3.5 Amps
- 25 Volts at 2 Amps

- +9 Volts at 1 Amp
- 9 Volts at 1 Amp

- +100 Volts at 1.25 Amp

The +100, +9 and -9 Volts supplies are used only by the analog chassis. Other supplies may be used by either chassis.

CAUTION! The motherboard is designed so that two power supplies may share the +5 and +12 volt loads. The motherboard runs for these supply lines are split, and fed to separate terminals at the top of the motherboard. If only supply A is installed, it must be jumpered to feed +5 and +12 to both halves of the card cage. If supply B is installed as well, the jumpers **MUST NOT** be installed or extreme currents will be drawn.

Supply B is required if more than 12 cards are installed, or if any disk drives are installed. Supply B delivers the following outputs:

- +5 Volts at 10 Amps (to card cage and disks)
- 5 Volts at 1 Amp (to disks only)
- +12 Volts at 6 Amps (to card cage only)
- +24 Volts at 9 Amps (to disks only)

The CGC 7900 requires approximately 13 amperes of 110 volt AC power. The system has a rear panel fuse rated at 15 amperes. Each power supply is internally fused at 10 amperes.

NOTE: Because of the design of the switching regulators, it is required that the +5 volt output of each supply MUST BE LOADED AT ALL TIMES. All other voltages are referenced to the +5 output. If the +5 is not loaded, extreme voltages will result and the supply will shut down.

If excessive currents are drawn from the supply, it will fold back the output voltage in an attempt to reduce the overload. If the overload persists, the internal or external fuses may blow.

CGC 7900 SYSTEM MEMORY MAP

	000000	200000	400000	600000	800000	A00000	C00000	E00000
000000	Buffer Memory Card 0				EPR0M	Z M o d e S c r e e n M e m o r y	Image Plane 0	Color Status Map
020000	Buffer Memory Card 1						Image Plane 1	Misc
040000	.						Image Plane 2	
060000	.						.	
080000	.						.	
0A0000	.						.	
0C0000	.						.	
0E0000	.						.	
100000							Image Plane 7	
120000							Image Plane 8	
140000			One Block = 128K				.	
160000							.	
180000							.	
1A0000							.	
1C0000							.	
1E0000						Image Plane 15	I/O	

CGC 7900 MEMORY MAP

The processor in the CGC 7900 is capable of directly addressing over 16 Megabytes of memory, using a 24-bit address bus. The addressing range is 000000 to FFFFFFF (hex). Chromatics reserves the upper half of this space, beginning at 800000 (hex).

The lower half of the 7900 address space will normally contain one or more Buffer Memory cards. Each card contains 128K or 512K bytes of dynamic RAM. The first card must be located at address 000000-1FFFFFF (the first 128K of memory) to provide the processor with room for interrupt vectors. The remainder of this card, plus any other Buffer Memory cards which may be installed, is allocated among various system functions, and user programs.

The "Thaw" command in firmware allocates memory among input/output buffers, stacks, the Create Buffer, function key buffers, etc. If battery-powered CMOS RAM (optional) is installed in your system, the parameters set up by "Thaw" will be remembered and used to allocate memory next time the system is powered up. If CMOS RAM is not present, memory will be allocated according to default parameters in PROM.

EPROM

System EPROM begins at address 800000. The Raster Processor card contains EPROM for the standard system. Space is provided for 32K words (64K bytes), addressed from 800000 to 80FFFF. The card will accommodate Motorola 2532-C35 EPROMs (or equivalent) which have access times of 350 nanoseconds or faster.

2532 EPROMs are capable of storing 32K bits of data, arranged as 4K of 8-bit bytes. Since the 68000 fetches all instructions as 16-bit words, two 2532s must be accessed simultaneously for each instruction fetch. This requires that data in the 2532s be separated into "odd" bytes and "even" bytes. Each 4K of words in EPROM thus requires two 2532s, one containing all the "odd" numbered bytes in the program, and one containing all the "even" numbered bytes. A total of 16 2532s may be inserted in the sockets provided on the Raster Processor card.

A special mapping is provided for convenience during processor startup. When external Reset is applied, the 68000 fetches its stack pointer and program counter as two 32-bit words, from addresses 000000 and 000004, respectively. The EPROM circuitry maps addresses 800000 and 800004 into this space. Thus, the first two long words in EPROM should contain the initial values of stack pointer and program counter.

The figure on the following page shows where system EPROMs are installed on the Raster Processor card. Each socket is labeled with "even" or "odd", depending on whether it contains the even or odd bytes of code. Each socket is also labeled with the first three digits of its address. For example, the first socket is labeled "800 even", and it contains all even bytes between addresses 800000 and 801FFF.

EPR0M INSTALLATION

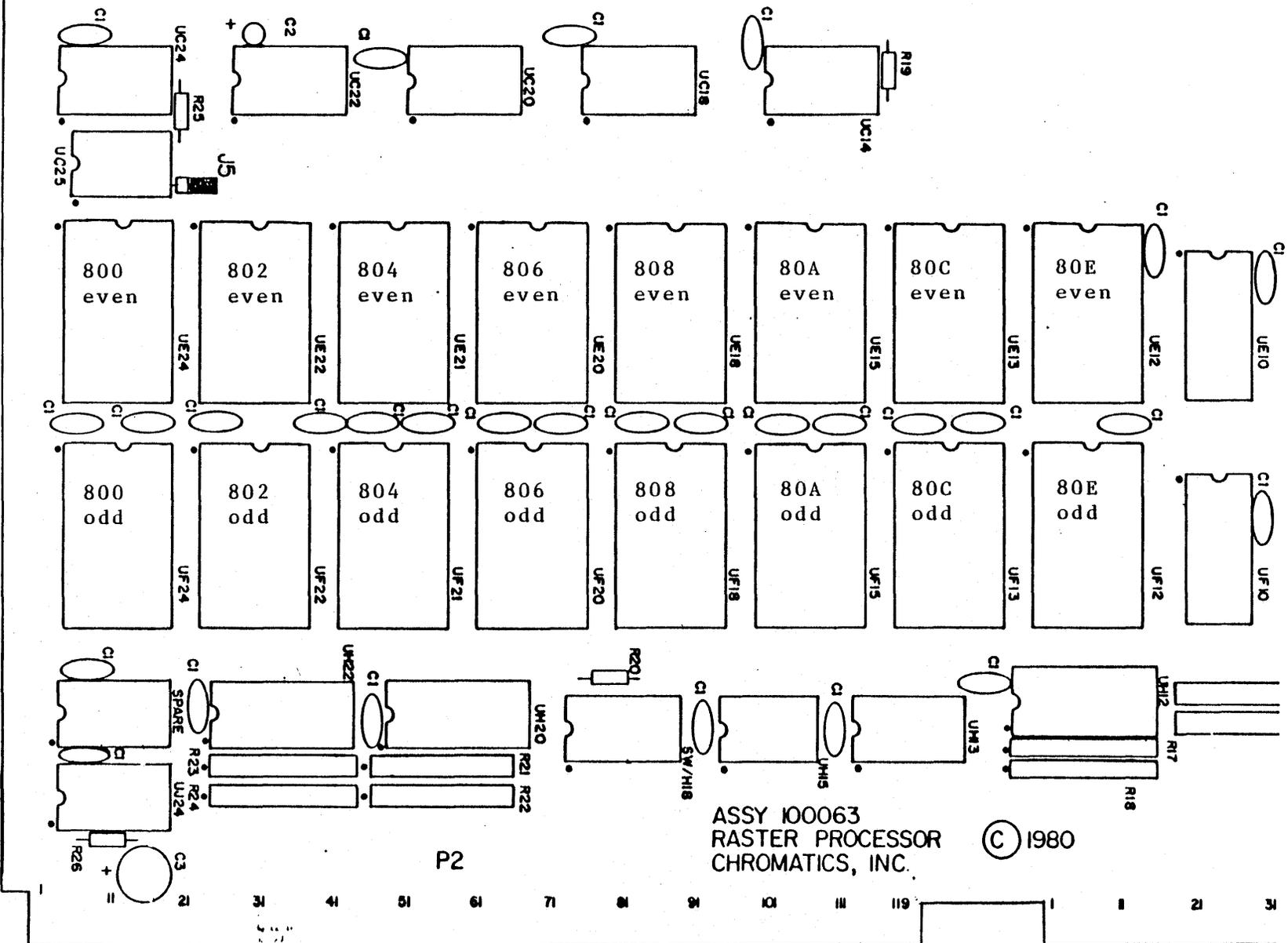


IMAGE MEMORY

Image memory on the CGC 7900 consists of from one to sixteen Refresh Memory cards. Each Refresh Memory card, or plane, contains 128K bytes of dynamic RAM. The bits on these planes are manipulated by software to produce high-resolution Bitmap images. Then, the information in the planes is brought out through the image control logic and the Color Lookup Table, to produce an image on the screen.

All areas of the memory map designated as image memory are protected against Bus Errors. Regardless of the number of planes installed in the image memory of a 7900 system, it is impossible to receive a Bus Error from image memory accesses.

The CGC 7900 provides several ways to address image memory. Each of these methods is discussed in turn.

PLANE MODE

In Plane mode, each plane of image memory is accessed as an independent 128K chunk of memory. Writing a byte, word, or long word into the image memory in Plane mode will write only into that plane. Plane mode addressing is equivalent to the way memory is addressed in most computer systems, and is the same way that Buffer Memory is addressed in the 7900.

Plane mode addressing begins at address C00000 and ends at DFFFFFF (hex). Each plane occupies 128K bytes. The planes are numbered from 0 to 15, although many systems will not have all planes installed. In particular, most systems will be configured in one of the following ways:

Total Planes In System	Plane Numbers Assigned
1	0
4	0,1,2,7
8	0 thru 7
16	0 thru 15

Plane 7 is normally assigned for use as the "blink" plane, so it is important that a plane 7 exist in all but the most basic systems.

Z MODE

Z mode is one of the two special modes provided for accessing image memory planes.

Consider the image memory to be arranged as a set of 16 planes, one in front of another. Each plane contains 1024 x 1024 bits, or 128K bytes. Each pixel on the screen is represented by a single bit from each of the 16 planes. Z mode allows the processor to write a 16-bit word to memory, and have each bit fall into the corresponding location of its plane.

For example, consider an instruction to write the first pixel in image memory (the upper left corner of the screen):

```
MOVE.W    #PixelData,$A00000
```

Bit 0 of "PixelData" will be moved into the first bit of image plane 0. Bit 1 will be moved into the first bit of image plane 1, and so on. The Z mode hardware allows writing to individual bits, without the problem of modifying adjacent bits in each plane.

Z mode addressing occupies a full 2 Megabytes of the address space. It begins at address A00000 and ends at BFFFFFF. Note that since only 768 lines of the image memory are visible at a time, the pixel addressed at BFFFFFF is not normally visible. The last visible pixel of image memory is addressed at B7FFFF (assuming pan and zoom are not in effect).

In Z mode, no assumptions are made concerning the number of planes in a system. If a plane does not exist, any bits which should be written into that plane are simply thrown away. When reading back data in Z mode, any bits which should come from non-existent planes will be returned as logical highs, or ones.

Z mode access to individual planes is restricted by Plane Select. Plane Select is a 16-bit latch, located at address E40012. If a bit of this latch is a one, the corresponding plane is enabled. If a bit is zero, the plane is disabled. Disabled planes may not be written into using Z mode, and reading from them in Z mode will return a zero in the bit positions of the disabled planes. In this way, non-existent

planes may be masked using Plane Select so that bits returned from them will be zeros.

COLOR STATUS MODE

Color Status mode provides a very fast way to write color information into the image memory planes. Color Status occupies 128K bytes, the same area one image plane occupies in Plane mode. Color Status mode is mapped from E00000 to E1FFFF. This is a "write-only" area of memory. Attempts to read from this area will return indefinite data.

Before using Color Status mode, it is necessary to load the Color Status Foreground and Background latches. Each of these contains a 16-bit number. Color Status Foreground is located at E40016, and Color Status Background is at E40018. Each of these should be loaded with the 16-bit quantity you would write into image memory if you were using Z mode addressing. For example, if the foreground of the pattern you are writing requires color number 5, you would load the Color Status Foreground latch with 5. Similarly, Color Status Background might be loaded with color number 0. (These numbers refer to entries in the Color Lookup Table.)

After loading the latches, you may write to the Color Status area of memory. Each bit you write will affect a single pixel of the image, one bit in each of the 16 image planes. If you write a bit which is a 1, the pixel will be written in foreground color, as defined by the Color Status Foreground latch. If a bit is 0, the pixel will be written in background color, defined by Color Status Background.

For example: to make the first 32 pixels of the screen white, we might execute the following code.

```

ForeG   EQU     $E40016      Foreground latch
BackG   EQU     $E40018      Background latch
ColStat EQU     $E00000      Color Status mode starts here

                MOVE.W #7,ForeG    set up FG Color Status
                                (assume color 7 = white)

WRITE    MOVE.L #$FFFFFFF,ColStat  write 32 bits of ones

```

The single instruction at label WRITE modifies the color of 32 pixels. The same operation would require 32 writes in Z mode, or 16 writes in Plane mode (to write all 16 planes).

The following example will write an alternating series of 32 red and green pixels into the first 32 pixels of the screen.

```
MOVE.W #4,ForeG      make foreground color = 4
MOVE.W #2,BackG      make background color = 2
                      (assume 4 = red, 2 = green)

MOVE.L #SAAAAAAAA,ColStat  write alternating bits
```

Color Status mode allows writing bytes, words, or long words, to modify 8, 16, or 32 pixels, respectively.

The image memory planes are grouped into two sets of 8 planes each. Each of these two sets may contain an image, and Plane Select is normally used to decide which of the two is written into when a 16-bit Z mode write is performed. When writing with Color Status, it may be useful to write both images with the same color (otherwise one image would be written with zeros). To prevent this problem from occurring, always load the Color Status latches with the same number in the upper and lower bytes. Following this rule, our first example above must be corrected to contain the statement

```
MOVE.W #S0707,ForeG  set up FG Color Status
                      (assume color 7 = white)
```

(Copying the lower byte into the upper byte of the latch information.)

COLOR LOOKUP TABLE

The Color Lookup Table consists of 256 locations, each of which holds a 24-bit number. Eight of these bits determine the red component of a color, eight for green, and eight for blue. A pixel in the Bitmap (image memory) is given a color by summing the bits in whichever set of 8 planes is being viewed (weighted binary sum), and the resulting value points to an entry in the Color Lookup Table. The color components in that entry of the Color Lookup Table provide the color of that pixel.

The table is arranged as 256 long words (1K bytes), starting at address E30000. Each long word is organized as follows:

Bits	31-24	23-16	15-8	7-0
	FF	8-bit red	8-bit green	8-bit blue

The high byte (bits 31-24) of each entry are undefined, so they read out as FF hex. The next 8 bits set the red intensity, followed by green and blue.

The Color Lookup Table may be read or written at any time. Values written into the table are not used on the screen until the next vertical retrace, so it is not useful to write a single entry more than once per screen scan (1/60 second with 60 Hz power). Writing to the Color Lookup Table at any time will not cause the display to "glitch."

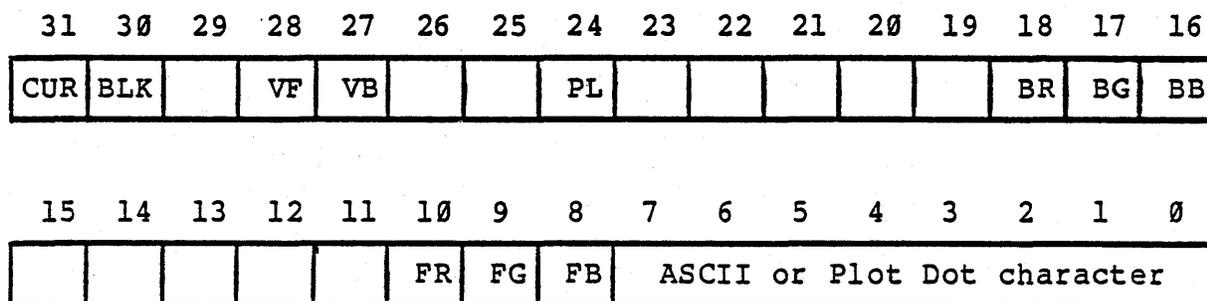
COLOR LOOKUP TABLE ADDRESSES

0	E30000	52	E300D0	104	E301A0	156	E30270	208	E30340
1	E30004	53	E300D4	105	E301A4	157	E30274	209	E30344
2	E30008	54	E300D8	106	E301A8	158	E30278	210	E30348
3	E3000C	55	E300DC	107	E301AC	159	E3027C	211	E3034C
4	E30010	56	E300E0	108	E301B0	160	E30280	212	E30350
5	E30014	57	E300E4	109	E301B4	161	E30284	213	E30354
6	E30018	58	E300E8	110	E301B8	162	E30288	214	E30358
7	E3001C	59	E300EC	111	E301BC	163	E3028C	215	E3035C
8	E30020	60	E300F0	112	E301C0	164	E30290	216	E30360
9	E30024	61	E300F4	113	E301C4	165	E30294	217	E30364
10	E30028	62	E300F8	114	E301C8	166	E30298	218	E30368
11	E3002C	63	E300FC	115	E301CC	167	E3029C	219	E3036C
12	E30030	64	E30100	116	E301D0	168	E302A0	220	E30370
13	E30034	65	E30104	117	E301D4	169	E302A4	221	E30374
14	E30038	66	E30108	118	E301D8	170	E302A8	222	E30378
15	E3003C	67	E3010C	119	E301DC	171	E302AC	223	E3037C
16	E30040	68	E30110	120	E301E0	172	E302B0	224	E30380
17	E30044	69	E30114	121	E301E4	173	E302B4	225	E30384
18	E30048	70	E30118	122	E301E8	174	E302B8	226	E30388
19	E3004C	71	E3011C	123	E301EC	175	E302BC	227	E3038C
20	E30050	72	E30120	124	E301F0	176	E302C0	228	E30390
21	E30054	73	E30124	125	E301F4	177	E302C4	229	E30394
22	E30058	74	E30128	126	E301F8	178	E302C8	230	E30398
23	E3005C	75	E3012C	127	E301FC	179	E302CC	231	E3039C
24	E30060	76	E30130	128	E30200	180	E302D0	232	E303A0
25	E30064	77	E30134	129	E30204	181	E302D4	233	E303A4
26	E30068	78	E30138	130	E30208	182	E302D8	234	E303A8
27	E3006C	79	E3013C	131	E3020C	183	E302DC	235	E303AC
28	E30070	80	E30140	132	E30210	184	E302E0	236	E303B0
29	E30074	81	E30144	133	E30214	185	E302E4	237	E303B4
30	E30078	82	E30148	134	E30218	186	E302E8	238	E303B8
31	E3007C	83	E3014C	135	E3021C	187	E302EC	239	E303BC
32	E30080	84	E30150	136	E30220	188	E302F0	240	E303C0
33	E30084	85	E30154	137	E30224	189	E302F4	241	E303C4
34	E30088	86	E30158	138	E30228	190	E302F8	242	E303C8
35	E3008C	87	E3015C	139	E3022C	191	E302FC	243	E303CC
36	E30090	88	E30160	140	E30230	192	E30300	244	E303D0
37	E30094	89	E30164	141	E30234	193	E30304	245	E303D4
38	E30098	90	E30168	142	E30238	194	E30308	246	E303D8
39	E3009C	91	E3016C	143	E3023C	195	E3030C	247	E303DC
40	E300A0	92	E30170	144	E30240	196	E30310	248	E303E0
41	E300A4	93	E30174	145	E30244	197	E30314	249	E303E4
42	E300A8	94	E30178	146	E30248	198	E30318	250	E303E8
43	E300AC	95	E3017C	147	E3024C	199	E3031C	251	E303EC
44	E300B0	96	E30180	148	E30250	200	E30320	252	E303F0
45	E300B4	97	E30184	149	E30254	201	E30324	253	E303F4
46	E300B8	98	E30188	150	E30258	202	E30328	254	E303F8
47	E300BC	99	E3018C	151	E3025C	203	E3032C	255	E303FC
48	E300C0	100	E30190	152	E30260	204	E30330		
49	E300C4	101	E30194	153	E30264	205	E30334		
50	E300C8	102	E30198	154	E30268	206	E30338		
51	E300CC	103	E3019C	155	E3026C	207	E3033C		

OVERLAY MEMORY ADDRESSING

The Overlay consists of 4080 character cells, arranged 85 per line and 48 lines. Each cell is addressed as a long word (32 bits). The Overlay is mapped from addresses E38000 to E3BFBC. (Actually, 4096 cells are present in the overlay, but 16 are invisible at any time. These 16 will come into view, and 16 others will become invisible, as the Overlay is scrolled.)

Each cell of the Overlay uses 19 of the 32 bits allocated for it.



- CUR places a cursor in the cell if SET
 BLK blinks the foreground character in the cell if SET
 VF makes the foreground visible if SET (else transparent)
 VB makes the background visible if SET (else transparent)
 PL uses bits 0-7 as PLOT DOT descriptor if SET (else ASCII)
- BR turns on Red in background if SET
 BG turns on Green in background if SET
 BB turns on Blue in background if SET
- FR turns on Red in foreground if SET
 FG turns on Green in foreground if SET
 FB turns on Blue in background if SET

Bits 0-7 are interpreted in a number of ways:

If PL is CLEAR, implying ASCII characters, bits 0-6 are used to select an ASCII character. If bit 7 is CLEAR, the character will be taken from the standard ASCII character ROM. If bit 7 is SET, the character will be taken from the alternate character set ROM.

If PL is SET, implying Plot Dots, each of the bits 0-7 is used to turn a Plot Dot on or off. The dots in each character cell are arranged as follows:

0	4
1	5
2	6
3	7

The Plot Dots above are numbered to correspond with the bits which control them. If a bit is SET, the Plot Dot associated with that bit will be in foreground color, as determined by FR, FG and FB. If a bit is CLEAR, the associated Plot Dot will be in background color, determined by BR, BG and BB.

OVERLAY CHARACTER CELL ADDRESSES

Line No.	First Cell	Last Cell
1	E38000	E38150
2	E38154	E382A4
3	E382A8	E383F8
4	E383FC	E3854C
5	E38550	E386A0
6	E386A4	E387F4
7	E387F8	E38948
8	E3894C	E38A9C
9	E38AA0	E38BF0
10	E38BF4	E38D44
11	E38D48	E38E98
12	E38E9C	E38FEC
13	E38FF0	E39140
14	E39144	E39294
15	E39298	E393E8
16	E393EC	E3953C
17	E39540	E39690
18	E39694	E397E4
19	E397E8	E39938
20	E3993C	E39A8C
21	E39A90	E39BE0
22	E39BE4	E39D34
23	E39D38	E39E88
24	E39E8C	E39FDC
25	E39FE0	E3A130
26	E3A134	E3A284
27	E3A288	E3A3D8
28	E3A3DC	E3A52C
29	E3A530	E3A680
30	E3A684	E3A7D4
31	E3A7D8	E3A928
32	E3A92C	E3AA7C
33	E3AA80	E3ABD0
34	E3ABD4	E3AD24
35	E3AD28	E3AE78
36	E3AE7C	E3AFCC
37	E3AFD0	E3B120
38	E3B124	E3B274
39	E3B278	E3B3C8
40	E3B3CC	E3B51C
41	E3B520	E3B670
42	E3B674	E3B7C4
43	E3B7C8	E3B918
44	E3B91C	E3BA6C
45	E3BA70	E3BBC0
46	E3BBC4	E3BD14
47	E3BD18	E3BE68
48	E3BE6C	E3BFBC

CGC 7900 DETAILED MEMORY MAP

000000	- 01FFFF	BWL	Buffer memory cards (128K or 512K each)
020000	- 03FFFF	.	.
040000	- 05FFFF	.	.
.	.	.	.
.	.	.	.
800000	- 80FFFF	BWL	EPROM (on Raster Processor card)
A00000	- BFFFFF	BWL	Z Mode screen memory (all planes)
C00000	- C1FFFF	BWL	Plane mode screen memory (plane 0)
C20000	- C3FFFF	BWL	(plane 1)
C40000	- C5FFFF	BWL	(plane 2)
C60000	- C7FFFF	BWL	(plane 3)
C80000	- C9FFFF	BWL	(plane 4)
CA0000	- CBFFFF	BWL	(plane 5)
CC0000	- CDFFFF	BWL	(plane 6)
CE0000	- CFFFFF	BWL	(plane 7)
D00000	- D1FFFF	BWL	(plane 8)
D20000	- D3FFFF	BWL	(plane 9)
D40000	- D5FFFF	BWL	(plane 10)
D60000	- D7FFFF	BWL	(plane 11)
D80000	- D9FFFF	BWL	(plane 12)
DA0000	- DBFFFF	BWL	(plane 13)
DC0000	- DDFFFF	BWL	(plane 14)
DE0000	- DFFFFF	BWL	(plane 15)
E00000	- E1FFFF	BWL	Color Status mode screen memory
E20000	- E23FFF		Raster Processor
E30000	- E303FF	BWL	Color Lookup Table (256 long words)
E38000	- E3BFFF	BWL	Overlay screen memory (4K long words) (visible ends at E3BFBF - 4080 cells)

E40000 - E40FFF	BWL	CMOS or static RAM, and latches
E40000	W	Bitmap roll counter (10 bits)
E40002	W	X Pan (10 bits, low 2 not used)
E40004	W	Y Pan (10 bits)
E40006 - E40007	BW	X and Y zoom (4 bits each)
E4000A - E4000F		Reserved for raster processor
E40010	W	Blink Select
E40012	W	Plane Select
E40014	W	Plane Video Switch
E40016	W	Color Status foreground
E40018	W	Color Status background
E4001A	W	Overlay Roll Counter (12 bits +)
EFC440	WL	HVG Load X
EFC442	WL	HVG Load Y
EFC444	WL	HVG Load dX
EFC446	WL	HVG Load dY
EFC448	WL	HVG Load Pixel Color
EFC44A	WL	HVG Load Trip
F00000 - F0FFFF		Reserved for future use
FF0000 - FF1FFF	B	Serial Port Controllers (4)

FF8000 - FF83FF		CPU card onboard i/o space:
FF8001	B	RS232 data port
FF8003	B	RS232 control port
FF8041	B	RS449 data port
FF8043	B	RS449 control port
FF8080	W	Keyboard
FF80C6	BW	Joystick X axis
FF80CA	BW	Joystick Y axis
FF80CC	BW	Joystick Z axis
FF8100	W	Disk data port
FF8120	W	Disk control/status port
FF8141	B	Bezel switches
FF8181	B	Baud Rate Generator
FF81C1 - FF81FF	B	Real Time Clock (odd bytes only)
FF8200	W	Interrupt Mask
FF8240	W	Light Pen enable
FF8242	W	Light Pen X value (10 bits)
FF8244	W	Light Pen Y value (10 bits)
FF8246	W	Buffer memory parity check
FF8248	W	Buffer memory parity set/reset
FF824A	W	Sync information
FF8280 - FF82BF	BWL	BCS2
FF82C0 - FF82FF	BWL	BCS3
FF8300 - FF833F	BWL	BCS4
FF8340 - FF837F	BWL	BCS5
FF8380 - FF83BF	BWL	BCS6
FF83C1	B	Sound Generator latch address
FF83C3	B	Sound Generator read
FF83C5	B	Sound Generator write
FF8400 - FF84FF	BWL	DMA/PIO cards

CONFIGURING 128K BUFFER MEMORY CARDS

The two rotary switches on the edge of the Buffer Memory card determine the card's address. To set up a card, perform the following steps:

1. Determine what the memory address of the card should be. One card must have address 000000, and if other cards are installed, they will normally have consecutive addresses following the first card. Consult the table below to see what switch settings correspond to the card's desired memory address.

NOTE: The 7900 memory map requires that Buffer Memory cards be addressed below 800000.

NOTE: All possible memory addresses require that the first switch be set to a number between 0 and 7. THE SYSTEM WILL FAIL if The left-hand switch on the card is set to 8 or higher!

2. Arrange the card so that the component side is up, and the gold edge connector is pointing away from you. The two rotary switches should now be visible on the right side of the card's rear edge.

3. Using a small screwdriver, set the two switches so that the arrow on the left switch is pointing to the first digit of the required setting, and the arrow on the right switch is pointing to the second digit. For example, if you are installing a card at address 020000, the table says that the correct setting is 01. Set the left switch to 0 and the right switch to 1.

(Some switches may not be marked at the odd numbered positions. If yours is not, assume that position 1 lies halfway between 0 and 2, and so on.)

CONFIGURING 512K BUFFER MEMORY CARDS

A 512K byte Buffer Memory card has five switches on its rear edge. Hold the card so the switches are toward you and the component side of the board is UP, and perform the following steps:

1. Determine which 2 megabyte area of the address space the card will occupy. Each 128K bank of the 512K card is independently switchable, but ALL FOUR BANKS MUST RESIDE IN THE SAME 2 MEGABYTE AREA. The left-most switch selects the 2 megabyte area. For example, if this switch is 0, the card will reside in the first 2 megabyte area, anywhere from 000000 to 1FFFFF.

2. Set the other four switches to position the four 128K banks within the 2 megabyte area. Use the following table to choose the switch settings, but use the left-hand switch as the first digit of the "Switch Position", and one of the other four switches as the second digit.

Example: The 512K card is to be placed in the first 2 megabytes of memory. The 128K banks are desired to begin at addresses 000000, 020000, 040000, and 080000. Set the left switch to 0, and the other switches to 0, 1, 2, and 4.

NOTE: Be careful that no two banks of any memory cards coincide. This will cause spurious memory errors to occur during operation.

BUFFER MEMORY CARD ADDRESS SELECTION

Switch Position	Memory Address	Switch Position	Memory Address	Switch Position	Memory Address
0	0	2	C	5	8
0	1	2	D	5	9
0	2	2	E	5	A
0	3	2	F	5	B
0	4	3	0	5	C
0	5	3	1	5	D
0	6	3	2	5	E
0	7	3	3	5	F
0	8	3	4	6	0
0	9	3	5	6	1
0	A	3	6	6	2
0	B	3	7	6	3
0	C	3	8	6	4
0	D	3	9	6	5
0	E	3	A	6	6
0	F	3	B	6	7
1	0	3	C	6	8
1	1	3	D	6	9
1	2	3	E	6	A
1	3	3	F	6	B
1	4	4	0	6	C
1	5	4	1	6	D
1	6	4	2	6	E
1	7	4	3	6	F
1	8	4	4	7	0
1	9	4	5	7	1
1	A	4	6	7	2
1	B	4	7	7	3
1	C	4	8	7	4
1	D	4	9	7	5
1	E	4	A	7	6
1	F	4	B	7	7
2	0	4	C	7	8
2	1	4	D	7	9
2	2	4	E	7	A
2	3	4	F	7	B
2	4	5	0	7	C
2	5	5	1	7	D
2	6	5	2	7	E
2	7	5	3	7	F
2	8	5	4		
2	9	5	5		
2	A	5	6		
2	B	5	7		

CONFIGURING IMAGE MEMORY PLANES

Each Image Memory plane is assigned a unique number, from 0 to 15. Two planes in a system may NOT have the same number assigned.

The planes in a system may be arranged to form either one or two images. If all the planes are numbered in the range 0 to 7, only one image is present. If planes exist in the range 0 to 7, and also from 8 to 15, two images exist. EACH IMAGE MUST BE MADE OF THE SAME NUMBER OF PLANES. For example, if planes 0 to 3 are installed as one image, and it is desired to expand the system to contain a second identical image, the additional four planes must be installed as numbers 8 to 11. It would NOT be possible, for example, to have planes 0 to 7 as one image, and 8 to 12 as a second image. The system software would become confused, and possible damage to the image cards could result.

It is recommended that the planes in a system be arranged in one of the following ways:

Plane 0 only (1-plane)

Planes 0, 1, 2, and 7 (4-plane)

Planes 0 to 7 (8-plane)

Planes 0, 1, 2, 7, and 8, 9, 10, 15 (alternate 8-plane)

Planes 0 to 15 (16-plane)

Other arrangements are possible, as long as the guidelines in this section are followed. If your system will have a different arrangement of planes from those listed above, we recommend that you always install plane 7 if possible (plane 7 enables blink and Rubber Band). Then install planes starting at 0 and going up.

To configure a plane, first determine which number will be assigned to this plane. Make a note of your chosen number, and follow the instructions on this page and the following pages.

1. If your system already has eight planes, and you are adding an additional eight, proceed to step two. Otherwise, perform this step:

Remove the Color Look-Up board from the 7900 card cage (it will be near the left side of the cage, and is a dark, multi-layer board). Locate jumpers labeled 0 thru 7 on this board. REMOVE jumpers corresponding to the plane numbers which will be installed in your system. INSTALL (or leave installed) jumpers corresponding to plane numbers which will not exist in your system. For example, if your system will have planes 0, 1, 2, and 7, REMOVE those jumpers, and INSTALL jumpers 3, 4, 5, and 6. A system containing eight planes in one or both images should have NO jumpers installed.

Replace the Color Look-Up card firmly in the card cage, re-connect all cables you removed from this card, and proceed to step 2.

2. Arrange the Image Memory card so that the component side of the card is facing you, and the gold edge connector is to the right. Locate the rotary switch, in the lower left corner of the board. The switch has a slot, which is facing down (towards you). On this side of the switch is also an arrow, which will point to one of 16 positions around the switch.

Refer to the following table, and use a small screwdriver to turn the slot until the arrow points to the proper position for your card.

Image Plane Number Switch Position

0.....0	0
1.....1	1
2.....2	2
3.....3	3
4.....4	4
5.....5	5
6.....6	6
7.....7	7
8.....8	8
9.....9	9
10.....A	A
11.....B	B
12.....C	C
13.....D	D
14.....E	E
15.....F	F

The odd numbered positions on the switch may not be labeled. If not, assume that position 1 lies halfway between 0 and 2, and so on.

3. Again, arrange the card so that the gold edge connector is to the right. Locate the two vertical rows of pins near the center of the right edge. Refer to the following chart, and place one (1) jumper on one of the pairs of pins, to select the desired plane number. Remove any other jumpers on these two rows of pins.

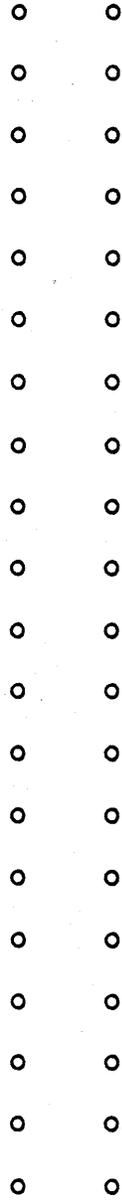
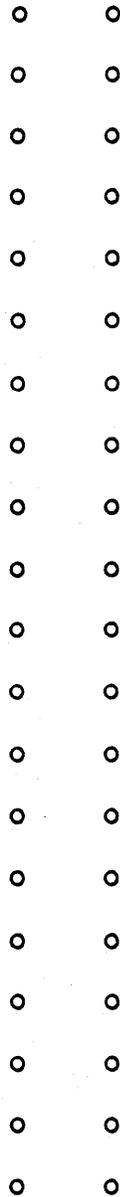
	o.15.o
	o.14.o
	o.13.o
	o.12.o
	o.11.o
	o.10.o
o..7.o	o..9.o
o..6.o	o..8.o
o..5.o	
o..4.o	Jumper J2
o..3.o	
o..2.o	
o..1.o	
o..0.o	

Jumper J1

4. Locate the two vertical rows of pins near the lower right corner of the card. Refer to the following chart, and place one (1) jumper on the pair of pins marked "0-7", or on the pair marked "8-15", depending on which of these ranges includes the desired plane number.

Jumper J3

Jumper J4



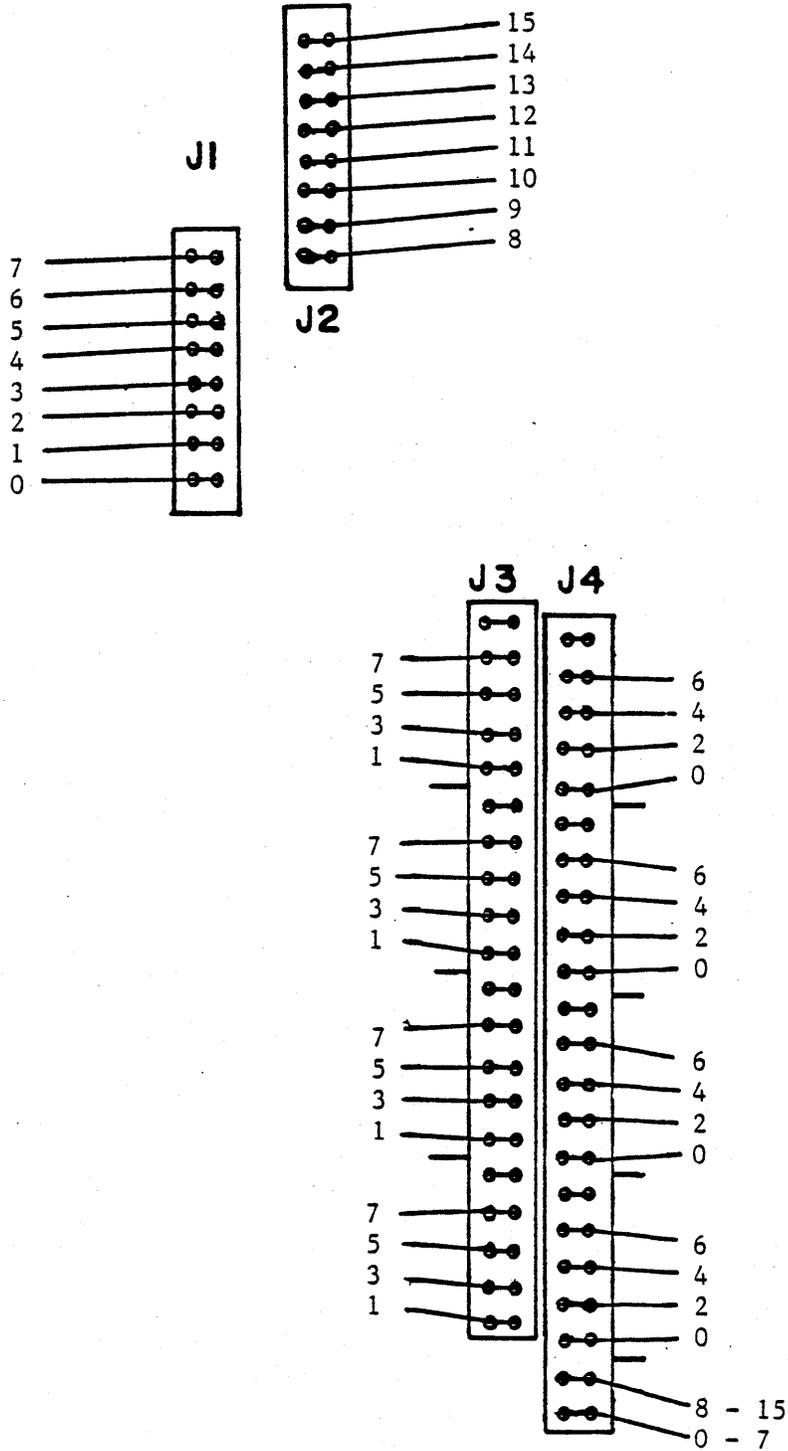
8 - 15

0 - 7

5. Now, if the desired plane number is greater than 7, subtract eight from it. Thus, plane 8 becomes 0, 9 becomes 1, and so on. (If your plane number is less than 8, do not alter it.) Refer to the following table, and place four (4) jumpers on pairs of pins marked with the plane number you have just calculated.

Jumper J3		Jumper J4	
o	o	o	o
19	—o..7.o	o..6.o	21
	o..5.o	o..4.o	
	o..3.o	o..2.o	
	o..1.o	o..0.o	
o	o	o	o
14	—o..7.o	o..6.o	16
	o..5.o	o..4.o	
	o..3.o	o..2.o	
	o..1.o	o..0.o	
o	o	o	o
9	—o..7.o	o..6.o	11
	o..5.o	o..4.o	
	o..3.o	o..2.o	
	o..1.o	o..0.o	
o	o	o	o
4	—o..7.o	o..6.o	6
	o..5.o	o..4.o	
	o..3.o	o..2.o	
	o..1.o	o..0.o	
		o	o
		o	o

IMAGE MEMORY CONFIGURATION JUMPERS



HARDWARE LATCHES AND CMOS/STATIC RAM

The area of memory from E40000 to E40FFF serves several purposes. First, the CPU card contains 4K bytes of memory at these addresses. This will either be static RAM (2114) or CMOS RAM (6514). CMOS is only installed if your system contains the optional battery backup supply, which allows the CMOS to store information while system power is off.

Second, several system features use hardware latches mapped onto the same addresses as RAM. Writing to any of these addresses will write into both RAM and the latch. Reading from the address will not affect the latch, but RAM will respond with the proper information.

If CMOS RAM is installed, the procedure for configuring these latches at power-up is simple: Read the RAM and write the data back into the same address. This will cause the latches to resume the state they had when the CMOS RAM was last written.

Address	Function
E40000	Bitmap Roll Counter
E40002.....	X Pan
E40004	Y Pan
E40006.....	X and Y Zoom
E40008	Unused (reserved)
E4000A.....	Used
E4000C	By
E4000E.....	Raster Processor
E40010	Blink Select
E40012.....	Plane Select
E40014	Plane Video Switch
E40016.....	Color Status Foreground
E40018	Color Status Background
E4001A.....	Overlay Roll Counter

This area of memory is also the default area for user-defined function keys. Function key definitions are stored in the upper 2K of this memory, so the definitions can be maintained by the battery-backed CMOS RAM (if installed). If the user requires more room for his function key definitions, the function key buffer may be moved with the "Thaw" command.

BITMAP ROLL COUNTER

The Bitmap Roll Counter is a 10-bit latch at address E40000. The value stored in this latch is left-shifted by 10 bits, and added (modulo 2^{20}) to ANY address in the Z mode of Bitmap memory, during any read, write, or screen refresh access to the Bitmap. This latch has the effect of determining which physical set of RAM bits will be accessed by addresses A00000 thru A003FF (the top raster line of the Bitmap).

Since the value in this latch is added during all Z mode accesses to the Bitmap, its function is transparent to the CPU. That is, the CPU can always read and write to A00000 as the first pixel on the Bitmap.

This latch is useful for hardware scrolling the Bitmap. If the current Bitmap character height is N pixels, adding N to the Bitmap Roll Counter will have the effect of moving all pixels on the screen up N raster lines (one character line). Then the software need only erase the bottom line of the Bitmap, and the scrolling is complete. Scrolling down is accomplished by decrementing the Bitmap Roll Counter.

The Bitmap Roll Counter is independent of the Y Pan register, although both latches have the ability to cause the Bitmap image to scroll up and down. Altering the Y Pan register causes a given point on the screen to have a different address in memory; altering the Bitmap Roll Counter will never change the address which corresponds to a given screen location (although it will cause a different RAM chip to be associated with that location). See "Y Pan."

X PAN

The X Pan register is a 10-bit latch at address E40002. The value in this latch is added (modulo 1024) to the screen refresh address counter as each line of the Bitmap is being displayed on the screen. The X Pan register has the effect of determining where the left edge of the image (the vertical column of pixels below the pixel at A00000) will appear on the screen.

NOTE: The lowest 2 bits of the X Pan register are NOT significant. X Pan will only allow the image to be moved in increments of 4 pixels. You must increment or decrement the X Pan register by at least 4, in order to alter the screen display.

It is desirable to sync Pan to vertical retrace, so that altering the Pan registers (X Pan and Y Pan) will not cause "tearing" of the image.

Y PAN

The Y Pan register is a 10-bit latch at address E40004. The value in this latch is left-shifted by 10 bits, and added (modulo 2^{20}) to the screen refresh address counter as each line of the Bitmap is being displayed on the screen. The Y Pan register has the effect of determining where the top edge of the image (the horizontal row of pixels addressed from A00000 to A003FF) will appear on the screen.

All 10 bits of the Y Pan register are significant. Since the lowest two bits of the X Pan register are NOT significant, diagonal pan may be accomplished by incrementing both X Pan and Y Pan in steps of 4.

The Y Pan register has an especially important use. Recall that the screen only displays 768 lines, but there are actually 1024 lines of pixels in the Bitmap memory. Incrementing the Y Pan register allows the remaining 256 lines to become visible.

X AND Y ZOOM

The X and Y Zoom registers are addressable together by 16-bit word operations, or individually by 8-bit byte operations. X Zoom is a 4-bit register at E40006, and Y Zoom is a 4-bit register at E40007.

The CGC 7900 performs zoom by pixel magnification. With no zoom, the X and Y Zoom registers are both zero, and each pixel in memory is refreshed to the screen only once. This provides the default conditions of 1024 pixels per horizontal line, and 768 lines visible. If each pixel in memory was brought out to the screen twice, there would be room for only 512 of them on each screen line; this corresponds to an X Zoom factor of two, and occurs when the X Zoom register contains the value 1.

If each line of pixels is brought out to the screen twice, each "dot" placed on the screen would be twice as tall as before. There would then be room for only 384 lines of information, with each line twice its previous height. This corresponds to a Y Zoom factor of two, and occurs when the Y Zoom register contains the value 1.

In general, the 4-bit contents of a Zoom register is one less than the current magnification factor. The highest magnification possible is 16 times, which occurs when one of the Zoom registers contains the value 15.

When zoom is in effect, not all of the pixels in memory may be viewed on the screen at a time. The X Pan and Y Pan registers determine what area of the memory is viewed. They contain the pixel number on the line, and the line number, of the first pixel placed on the screen.

It is desirable to sync zoom to vertical retrace, so that altering the Zoom registers will not cause "tearing" of the image.

BLINK SELECT

Blink Select is a 16-bit latch at address E40010. Each bit of the latch corresponds to one of the 16 possible planes in Bitmap memory, numbered 0 thru 15.

If a bit in the latch is SET, the information from the corresponding plane is masked to zero and unmasked at a 1.9 hertz rate. This causes a pixel containing that bit to change color numbers (point to a different color in the Lookup Table). The pixel then changes colors at 1.9 hertz.

If a bit in the latch is CLEAR, the information from the corresponding plane is not altered by the Blink Select latch.

NOTE: Blink Select should only be read or written using word (16-bit) operations.

PLANE SELECT

Plane Select is a 16-bit latch at address E40012. Each bit of the latch corresponds to one of the 16 possible planes in Bitmap memory, numbered 0 thru 15.

Plane Select controls Z mode access to the Bitmap planes. If a bit in the latch is SET, the Z mode hardware is allowed to read and write information in that plane.

If a bit in the latch is CLEAR, the Z mode hardware will not write into the corresponding plane. Reading a pixel in Z mode will cause the corresponding plane to show up as a zero bit.

NOTE: Plane Select should only be read or written using word (16-bit) operations.

PLANE VIDEO SWITCH

Plane Video Switch is a 16-bit latch at address E40014. Each bit of the latch corresponds to one of the 16 possible planes in Bitmap memory, numbered 0 thru 15.

Plane Video Switch determines which planes are allowed to feed the Color Lookup Table. If a bit in the latch is SET, the plane is enabled to feed the Lookup Table normally.

If a bit in the latch is CLEAR, the information in the plane is masked to zero before feeding to the Color Lookup Table. This restricts the total number of available colors in the system, just as if a plane had been removed from the system.

NOTE: Only 8 planes at a time feed the Color Lookup Table. An image may be composed of up to 8 planes, either plane numbers 0 thru 7, or numbers 8 thru 15. The Image Select Switch (see "Overlay Roll Counter") determines which set of 8 planes is being viewed.

NOTE: Plane Video Switch should only be read or written using word (16-bit) operations.

COLOR STATUS FOREGROUND/BACKGROUND

Color Status Foreground is a 16-bit latch at address E40016. Color Status Background is a 16-bit latch at address E40018. Each of these contains 16-bit pixel data, used when writing to the Bitmap memory in Color Status mode (addresses E00000 thru E1FFF).

See "Image Memory Addressing - Color Status Mode" for details on the use of these registers.

OVERLAY ROLL COUNTER

The Overlay Roll Counter is a latch at address E4001A. The low 12 bits are used for Overlay scrolling, and the upper 3 bits have special uses as discussed below.

The Overlay is an area of memory containing 4096 long words (32 bits each). Of these, 4080 are visible on the screen at one time, arranged 85 horizontally by 48 vertically. The low 12 bits of the Overlay Roll Counter decide which of these 4096 locations is considered as the first character cell of the Overlay, by adding the 12-bit value, modulo 4096, to any address which tries to access memory in the Overlay address space.

By altering the low 12 bits of the Overlay Roll Counter, you determine which physical RAM location is addressed as the beginning of the Overlay. As far as the CPU is concerned, however, the first cell of the Overlay is always addressed at E38000.

The Overlay Roll Counter is primarily useful for scrolling. By adding 85 to the lower 12 bits of the latch, the apparent effect is that every line of characters on the Overlay screen has moved up one line. Then, the software need only erase the last line of the Overlay (which is in a known location in memory) and scrolling is complete. Scrolling down is accomplished by subtracting 85 from the low 12 bits of the Overlay Roll Counter.

It is not necessary to scroll a line at a time. If the low 12 bits of the Overlay Roll Counter are incremented by one, every character on the screen will move left one position. The characters at the beginning of each line will move to the end of the previous line. The first character on the screen will move into the 16-cell area that is not visible.

IMAGE SELECT

Bit 13 of the Overlay Roll Counter (E4001A) is the Image Select switch. If CLEAR, Bitmap planes 0 thru 7 are selected as the image to be displayed in Bitmap. If SET, planes 8 thru 15 are selected.

OVERLAY CURSOR BLINK

Bit 14 of the Overlay Roll Counter (E4001A) determines whether the Overlay cursor will blink. If SET, any Overlay character cell with the cursor bit on will contain a blinking cursor. If CLEAR, Overlay cursor(s) will not blink.

Overlay cursors are produced by hardware, so their color is always white.

OVERLAY CHARACTER BLINK

Bit 15 of the Overlay Roll Counter (E4001A) determines whether the Overlay characters are allowed to blink. If SET, any Overlay character cell with the blink bit on will blink (foreground color will blink to background). If CLEAR, no characters in the Overlay will blink.

If this bit is clear, the blink bits in each Overlay cell may be used for other purposes, such as a flag for protected fields on the screen.

I/O MAP

Peripheral input/output is mapped into the last 32K of memory, beginning at address FF8000.

FF800X	RS232 Serial Port
FF804X	RS449 Serial Port
FF808X	Keyboard
FF80CX	Joystick
FF810X	Disk
FF814X	Bezel Switches
FF818X	Baud Rate Generator
FF81CX	Real Time Clock
FF820X	Interrupt Mask
FF824X	Bus Chip Select 1
FF828X	Bus Chip Select 2
FF82CX	Bus Chip Select 3
FF830X	Bus Chip Select 4
FF834X	Bus Chip Select 5
FF838X	Bus Chip Select 6
FF83CX	Sound Generator

SERIAL PORTS

The RS232 and RS449 serial interfaces are located on the CPU card. Peripherals connect to these ports through standard D-type connectors on the back of the CPU card.

The RS232 and RS449 ports are mapped identically. Each is configured with an Intel 8251 USART.

RS232 Serial Port

Data register: FF8001
Control/Status register: FF8003

RS449 Serial Port

Data register: FF8041
Control/Status register: FF8043

NOTE: The serial ports should be accessed only through byte (8-bit) operations.

The user is referred to Intel literature for details on programming the 8251.

SERIAL PORT PINOUTS

RS232 (25-pin connector)

Pin #	Signal	Description
2	TxD	Transmitted Data (output)
3	RxD	Received Data (input)
4	RTS	Request To Send (output)
5	CTS	Clear To Send (input)
6	DSR	Data Set Ready (input)
7	Gnd	Signal Ground
20	DTR	Data Terminal Ready (output)

Other pins are not connected in the 7900.

RS449 (37-pin connector)

Pin #	Signal	Description
4 22	SD-A SD-B	Send Data (output: equiv. to TxD)
6 24	RD-A RD-B	Receive Data (input: equiv. to RxD)
7 25	RS-A RS-B	Request to Send (output: equiv. to RTS)
9 27	CS-A CS-B	Clear to Send (input: equiv. to CTS)
11 29	DM-A DM-B	Data Mode (input: equiv. to DSR)
13 31	RR-A RR-B	Receiver Ready (output: equiv. to DTR)
18 20	TM RC	Test Mode (input: equiv. to DSR) Receiver Common (used for TM only)
19	Gnd	Signal Ground

Other pins are not connected in the 7900.

INTERFACING RS232 AND RS449

Both RS232 and RS449 are specifications for interconnecting data equipment. Originally designed for connecting a terminal to a modem, these two "standards" are now applied to interconnect a wide variety of data systems.

RS449 is a more recent specification. It allows much longer cable lengths between systems, as it employs balanced line drivers and receivers for greater noise immunity. RS449 also allows higher data rates, although the CGC 7900 limits data rates to 19,200 baud.

RS232 outputs may be fed to RS449 inputs. The RS232 output driver should be connected to the "low" side of the RS449 input receiver. The "high" side of the RS449 input receiver should be connected to RS232 signal ground, pin 7. Note that some RS232 outputs will produce a voltage of up to 25 volts, which is above the 15 volt limit for RS449 receivers. This problem will not occur with Chromatics equipment, but you should use caution when connecting other manufacturers' equipment.

RS449 outputs may be fed to RS232 inputs. The "low" side of the RS449 output driver should be connected to the RS232 input receiver. The "high" side of the RS449 output driver should be left unconnected. The "high" side is termed "-A" in the pinout chart. Note that RS449 outputs cannot produce the required voltage swing for RS232 inputs, since RS449 outputs never produce a negative voltage. This means that some RS232 equipment will not respond to RS449 signal levels. (This arrangement does work in the 7900 due to biasing resistors on the RS232 receivers.)

In these configurations, RS232 limits for cable length and data rate must be followed. Cable length should not exceed 50 feet.

BAUD RATE GENERATOR

The 7900 uses a Motorola K1135A Dual Baud Rate Generator, capable of producing two independent clocks. One of these clocks feeds the USART for the RS232 serial port, the other feeds the RS449 USART. The output frequency of the Baud Rate Generator is 16 times the selected baud rate. The USARTs should be programmed to accept a 16x clock.

This is a "write-only" area of memory; the contents of the BRG may not be read.

Both baud rates are set simultaneously by an 8-bit byte written to the Baud Rate Generator, at address FF8181. The upper 4 bits determine the RS449 baud rate, and the lower 4 determine the RS232 baud rate, according to the following table.

Baud Rate	4-bit Value
50	0
75	1
110	2
134.5	3
150	4
300	5
600	6
1200	7
1800	8
2000	9
2400	A
3600	B
4800	C
7200	D
9600	E
19200	F

Example: to set the RS449 port to 9600 baud, and the RS232 port to 110 baud, do a

```
MOVE.B    #$E2,$FF8181
```

NOTE: The Baud Rate Generator should be accessed only through byte (8-bit) operations.

JOYSTICK.

Joystick data addresses:

X: FF80C6

Y: FF80CA

Z: FF80CC

The joystick incorporates a 10-bit analog-to-digital converter. The A-to-D can only convert one axis of joystick data at a time, and it requires approximately 25 microseconds to perform a conversion.

The procedure for reading a joystick axis is as follows: Read a word from the address listed for the desired axis. This selects the axis, and causes the A-to-D to begin conversion. Then, wait for conversion to occur. You can tell when conversion is complete by testing bit 2 of the BYTE address. The example below uses the BTST instruction which works on a byte operand in memory.

	MOVE.L	#\$FF80C6,A0	point A0 to X-axis
	MOVE.W	(A0),D0	select axis & begin conversion
LOOP	BTST	#2,(A0)	conversion done?
	BNE.S	LOOP	no, so wait
	MOVE.W	(A0),D0	get the data
	ANDI.L	#\$3FF,D0	mask to 10 bits

When this routine exits, D0 contains valid data from the joystick X-axis.

The address you read from has the effect of selecting which axis of analog data is sent to the A-to-D converter. However, reading from any of the addresses above will return output data from the A-to-D. Taking advantage of this fact, it is possible to read data from a previous conversion while beginning the next conversion. For example:

```
MOVE.L  #$FF80C6,A0    point to X-axis
BSR     WAIT           wait for conversion (bit 2)
MOVE.L  #$FF80CA,A0    point to Y-axis
MOVE.W  (A0),D0        read converted X-value, and
                       also begin conversion of Y
...etc...
```

NOTE: Accessing any addresses other than those listed above may cause more than one axis to be simultaneously selected. The analog signals would be combined in unpredictable ways.

The joystick has the capacity to produce an interrupt whenever it is moved in any of the three axes. If the joystick interrupt bit is unmasked (in the Interrupt Mask register), moving the joystick "off top dead center" will cause an interrupt. The joystick continues to produce interrupts for as long as it is held off center in any of the three axes.

BEZEL SWITCHES

Bezel Switch data:

Read (byte) from FF8141

The states of all 8 Bezel Switches are read simultaneously by reading a byte from the Bezel Switch address. Bits 0 thru 7 represent the condition of the 8 switches.

Bezel Switch data is ACTIVE LOW. If a switch is depressed, the corresponding bit will be ZERO.

Pressing any Bezel Switch will cause an interrupt if the proper bit is cleared in the Interrupt Mask register.

Bezel switch bits are not in consecutive order. If the switches are labeled 1 to 8, from left to right, the ordering of the bits is:

Switch No.	Bit No.
7	0
8	1
5	2
6	3
3	4
4	5
1	6
2	7

INTERRUPT HANDLING

The CGC 7900 uses a Mask register to selectively enable and disable interrupts. This operates in conjunction with the multi-level interrupt handling capability of the MC68000 processor. The 68000 can respond to seven different priorities of interrupts, and a lower priority device may be interrupted by a higher priority device.

Interrupts are numbered from one to seven, and level seven is the highest priority. Each device which interrupts the system is assigned to a level, although more than one device may share the same interrupt level.

On the CPU card, interrupt levels four, five, and seven are used. Levels four and five are used for the interrupt-driven I/O devices and the BINTs (Bus Interrupts) described on the following pages. Level seven is used for the power-up interrupt and memory parity errors.

If a user builds a device which requires interrupt service, he has two choices in the 7900 system: either use the BINT lines provided on the bus, or design his own interrupt logic. This logic must operate at some interrupt level OTHER THAN four, five, or seven, since these levels are always decoded on the CPU card.

See the MC68000 User's Manual for more information concerning processor interrupt handling.

INTERRUPT MASK

The Interrupt Mask is a 16-bit latch which determines what interrupts are passed through to the 68000 processor. The Mask is loaded by a 16-bit Word written to address FF8200. This is a "write-only" latch. Programs which modify the Interrupt Mask should keep a copy of its contents in RAM.

The following table describes which interrupt is affected by each bit in the Mask. If a bit is SET, interrupts are INHIBITED from the corresponding device.

Vector Addr.	Mask Bit	Device	Level
12C.....	0.....	Real Time Clock.....	5
110	1	RS-449 Tx Ready	4
130.....	2.....	BINT 2 (P1-100).....	5
10C	3	RS-232 Tx Ready	4
108.....	4.....	Disk.....	4
134	5	BINT 3 (P1-102)	5
114.....	6.....	Bezel Keys.....	4
128	7	Keyboard	5
124.....	8.....	RS-449 Rx Ready.....	5
118	9	Light Pen (P1-96)	4
138.....	10.....	BINT 4 (P1-104).....	5
104	11	Joystick	4
100.....	12.....	Vertical Retrace (P2-94).4	4
13C	13	BINT 5 (P1-106)	5
11C.....	14.....	BINT 1 (P1-98).....	4
120	15	RS-232 Rx Ready	5

Here is the same information (organized by vector addresses):

100.....	12.....	Vertical Retrace (P2-94).4	4
104	11	Joystick	4
108.....	4.....	Disk.....	4
10C	3	RS-232 Tx Ready	4
110.....	1.....	RS-449 Tx Ready.....	4
114	6	Bezel Keys	4
118.....	9.....	Light Pen (P1-96).....	4
11C	14	BINT 1 (P1-98)	4
120.....	15.....	RS-232 Rx Ready.....	5
124	8	RS-449 Rx Ready	5
128.....	7.....	Keyboard.....	5
12C	0	Real Time Clock	5
130.....	2.....	BINT 2 (P1-100).....	5
134	5	BINT 3 (P1-102)	5
138.....	10.....	BINT 4 (P1-104).....	5
13C	13	BINT 5 (P1-106)	5

BUS INTERRUPTS (BINT)

Five interrupt lines are provided on the bus for peripherals to use.

BINT1 and BINT2 are in use by the 7900 system or are reserved for future use. BINT3, BINT4 and BINT5 are available for user peripherals. Each of these is pulled-up on the CPU card. User circuits should provide an open-collector gate to pull down the line to ground when an interrupt is desired. The line must remain low until the interrupt is serviced by the CPU.

Signal Name	Vector Address	Bus Pin #	Use	Level
BINT1	11C	P1-98	System	4
BINT2	130	P1-100	System	5
BINT3	134	P1-102	User	5
BINT4	138	P1-104	User	5
BINT5	13C	P1-106	User	5

When the interrupt is serviced, the processor will fetch the address of the interrupt service routine from the memory locations listed above. BINTs must be enabled and disabled through the Interrupt Mask Register. See the preceding page for mask bit assignments.

BUS CHIP SELECTS

Six lines are provided on the system bus for selecting system and user peripherals. Each of these lines will go LOW when the appropriate block of memory is accessed.

BCS1, BCS2 and BCS3 are in use by the 7900 system or are reserved for future use. BCS4, BCS5 and BCS6 are available for user peripherals. It is suggested that the user completely decode the low 6 bits of the address, in order to make efficient use of the available address space.

A block of 64 memory addresses is reserved for each Bus Chip Select line. The table below lists the starting address for each block.

Signal Name	Block Address	Bus Pin #	Use
BCS1	FF8240	P1-73	System
BCS2	FF8280	P1-76	System
BCS3	FF82C0	P1-75	System
BCS4	FF8300	P1-78	User
BCS5	FF8340	P1-77	User
BCS6	FF8380	P1-80	User

Logic on the CPU card asserts VPA whenever a BCS address is accessed. This allows slow peripherals, such as 6800 series devices, to use BCS lines for selection. VPA also eliminates the need to provide DTACK in this address space.

BCS1 ADDRESSES

Several system peripherals are selected using the signal BCS1. These are the light pen, buffer memory parity functions, and sync information (vertical and horizontal retrace timing).

LIGHT PEN

Enable Light Pen: Write (word) to FF8240

Write a 1 to enable blue flood, or 0 to disable it.

Writing to FF8240 will enable the light pen, or re-enable it from a previous "hit." If bit 0 of the data written is CLEAR, the blue flood is disabled. If bit 0 is SET, touching the light pen will cause the Overlay to flood blue in areas which have the "Foreground Visible" bit set. After a hit, blue flood is disabled until explicitly re-enabled.

If blue flood is disabled, only bright blue or white areas of the screen will be able to cause a light pen hit.

After an interrupt, read back the location of the hit:

X address: FF8242 (0 ≤ X ≤ 1022)

Y address: FF8244 (0 ≤ Y ≤ 766)

Each address holds a 10-bit number, corresponding to the absolute screen coordinates where the hit was detected. Bit 0 of the number will always be zero, so the effective resolution of the light pen is 511 by 383.

NOTE: Bits 15 through 10 of the hit location will float high, and be read back as ones!

NOTE: Light Pen addresses should be accessed only through word (16-bit) operations.

SYNC ADDRESSES

Sync:

Read (word) from FF824A

All sync information is available by reading a word (16 bits) from address FF824A. The bits reveal the following information:

Bit 0: Low during vertical retrace

Bit 1: Interlace Flag

Bit 2: Low during horizontal retrace

All other bits float high.

Bit 0 is low while the CRT beam is being blanked during vertical retrace. This bit coincides with the signal VERT (P2-94 on the bus), and the Vertical Retrace interrupt, if enabled.

Bit 1 is high during the first field of the interlaced display. Field one is the field containing the first visible line of the CRT. This bit is low during field two, the field containing the second line.

Bit 2 is low while the CRT beam is being blanked during horizontal retrace.

BUFFER MEMORY PARITY

Check for parity error:

Read (word) from FF8246

To check if a parity error has been detected in a buffer memory card, read a word (16 bits) from address FF8246. If bit 0 is low, it means one or more buffer memory cards have signalled an error.

Parity flip-flop:

Write (word) to FF8248

The parity flip-flop is set or reset by writing a word (16 bits) to address FF8248. Writing a one to this address sets the parity flip-flop which generates an immediate bus error. This is used for testing the bus error handling software. The software must read the other parity address to see if the bus error was a result of parity, or other causes.

To recover from a parity error, the software must reset the parity flip-flop by writing a zero to FF8248.

NOTE: Each buffer memory card has a jumper which must be installed before parity checking will function.

NOTE: If parity checking is enabled, the software should write into ALL buffer memory when the system is powered up. Otherwise, if a program reads from a location that was not previously written into, a parity error will result.

DISK PORT

Data:

Read/Write (word) at FF8100

Status:

Read/Write (word) at FF8120

The disk port communicates over 8 bidirectional data lines and 8 control lines. Hardware on the CPU card handles 16-bit data transfers over the 8-bit port.

The CGC 7900 disk interface was designed to accommodate an intelligent disk controller, the OMTI Model 10. (Early 7900s used a DTC model 1403D disk controller, which uses the same hardware interface but requires different software.) This controller uses a protocol which requires the controller to take the initiative in most exchanges of data. The CPU selects the controller, after which the controller asks for its instructions.

When the CPU wants to write data to the disk, it first selects the disk by writing to FF8120. This sets Select low, and also sets Data Bit 0 low. This disk controller recognizes this and asserts Busy low. Asserting Busy immediately resets Select to the high state. The controller will request instructions concerning the type of operation about to take place, and the CPU responds by writing data.

The CPU writes its 16-bit data words to FF8100. This causes Acknowledge to go low. The disk controller sets Request high and the high-order (most significant) byte is transferred to the disk. When this first byte is accepted by the disk, it sets Request low again and the low-order byte is transferred.

At the end of a transfer, the controller asserts MSG (Message). This indicates that one more word must be transferred, the completion status for the last transfer. This word will contain any error indication from the last transaction.

Bits in the status register are defined as follows:

15 thru 6	5	4	3	2	1	0
unused	RDY*	MSG*	C/D*	BSY*	REQ*	I*/O

Bit 5 is Ready, which is low when the hardware has assembled a 16-bit word for the CPU to read. Other bits are as defined in the pinout chart (see following page).

DISK PORT PINOUT

The disk connects to the CPU card at connector "A", the bottom connector on the card. The following table describes the signals on this connector. Control lines are ACTIVE LOW if indicated with an asterisk (*).

Pin No.	Description	Direction
1	Data Bit 0	Bidirectional
2	Data Bit 1	Bidirectional
3	Data Bit 2	Bidirectional
4	Data Bit 3	Bidirectional
5	Data Bit 4	Bidirectional
6	Data Bit 5	Bidirectional
7	Data Bit 6	Bidirectional
8	Data Bit 7	Bidirectional
9	Acknowledge*	CPU to Disk
10	Reset*	CPU to Disk
11	Select*	CPU to Disk
12	Busy*	Disk to CPU
13	Request*	Disk to CPU
14	Message*	Disk to CPU
15	I* / O	Disk to CPU
16	C* / D	Disk to CPU
17	Ground	
.	"	
.	"	
.	"	
26	"	

Reset* is an open-collector line. All other output lines are driven by TTL bus drivers. All control inputs are terminated on the CPU card by 220/330 ohm resistor networks.

I*/O is used by the disk to tell the CPU whether the next exchange is to be an input or output.

C*/D is used by the disk to tell the CPU whether control or data information is to be exchanged.

REAL TIME CLOCK

A National Semiconductor MM58167A Real Time Clock may optionally be installed in your 7900 system. This device contains registers for months, days, etc., down to milliseconds. A set of latches may also be programmed to produce an interrupt at selected intervals.

All access to the Real Time Clock should be through byte (8-bit) operations. The values transferred to and from the clock will be in the form of two BCD values, concatenated in an eight-bit byte. The following table describes what the upper and lower 4 bits of each register will contain.

AddressRegister Contents.....		
	(bits 7-4)	(bits 3-0)	
FF81C1	thousandths		(0-9)
FF81C3	tenths	hundredths	Seconds counters (00-99)
FF81C5	tens	units	(00-59)
FF81C7	tens	units	Minutes counter (00-59)
FF81C9	tens	units	Hours counter (00-23)
FF81CB		units	Day of Week counter (1-7)
FF81CD	tens	units	Day of Month counter (1-31)
FF81CF	tens	units	Months counter (1-12)
FF81D1	thousandths		
FF81D3	tenths	hundredths	Seconds latches
FF81D5	tens	units	
FF81D7	tens	units	Minutes latch
FF81D9	tens	units	Hours latch
FF81DB		units	Day of Week latch
FF81DD	tens	units	Day of Month latch
FF81DF	tens	units	Months latch

The following addresses in the Real Time Clock are used for command or status information (not BCD).

FF81E1	interrupt status register
FF81E3	interrupt control register
FF81E5	counter reset
FF81E7	latch reset
FF81E9	status bit
FF81EB	"GO" command
FF81ED	standby interrupt
FF81FF	test mode

Writing to the "GO" address resets all counters from seconds to thousandths of seconds.

The status bit should be read after reading any time register. The low bit of this data will be a one if the time register changed during the read, meaning the time register should be read again for valid data.

The bits in the interrupt control and status registers are defined as follows:

Bit No.	Function
0	Comparator (latch equals real-time)
1	Every Tenth of a Second
2	Every Second
3	Every Minute
4	Every Hours
5	Every Day
6	Every Week
7	Every Month

To enable an interrupt at the specified rate, write a "1" into the corresponding bit of the interrupt control register. (You must also enable the Real-Time Clock interrupt in the Interrupt Mask Register of the CPU.) To clear the interrupt, and discover what bit caused it, read the interrupt status register.

The user is referred to National Semiconductor literature for further details on programming the MM58167A.

PROGRAMMABLE SOUND GENERATOR

The 7900 uses a General Instruments AY-3-8910 Programmable Sound Generator (PSG). The PSG is located on the CPU card, along with its associated amplifier circuitry. A volume control is also located on the CPU card.

Address	Function
FF83C1	Latch Address
FF83C3	Read From PSG
FF83C5	Write To PSG

The PSG uses a multiplexed addressing system, which is not directly compatible with the MC68000 processor. It is necessary to perform two operations to write a value to the PSG: First tell it which register you want to write into, then provide the data which goes in the register.

If desired, further values can then be entered into the same register without performing the "Latch Address" function again.

Example of code to write "Value" to "Register" in the PSG:

```
MOVE.B    #Register,$FF83C1    tell it which register
MOVE.B    #Value,$FF83C5      put the value in it
```

All of the PSG registers may be read, as well as written. It is necessary to perform the same sequence as for writing: latch the register address (using a write), then read the register (using a read).

NOTE: The PSG should be accessed through byte (8-bit) operations only.

PROGRAMMING THE PSG

The CGC 7900 feeds the PSG with a clock frequency of 1/8 the main system clock frequency. In the standard 7900 system, this provides the PSG with a 1.780 Megahertz clock.

The frequency of a tone from any of the 3 analog outputs (A, B or C) is defined to be

$$F_t = F_{clk} / (16 * TP)$$

Where F_t is the frequency of the desired tone, F_{clk} is the PSG clock frequency, and TP is the number which must be entered into the PSG Tone Period register to produce the desired frequency. Solving for TP ,

$$TP = 111250 / F_t$$

TP is allowed to be up to a 12-bit number. The lower eight bits are entered into the Fine Tune register, and the upper four bits are entered into the Coarse Tune register.

The calculations for noise period are identical:

$$NP = 111250 / F_n$$

Where F_n is the desired noise frequency, and NP is the number which must be entered into the PSG Noise Period register. NP may be up to a 5-bit number.

Envelope period (the duration of a tone) is defined to be

$$T_e = 256 * EP / F_{clk}$$

Where T_e is the desired envelope duration (in seconds), F_{clk} is the PSG clock frequency defined above, and EP is the 16-bit number which must be entered into the PSG Envelope Period registers. Solving for EP ,

$$EP = T_e * 6953$$

PSG REGISTERS

The PSG contains 16 internal registers, each of which may be accessed by the Latch Address/Write to Register procedure mentioned earlier. The registers are defined as follows:

Register #	Purpose
0	Fine Tune A (8 bits)
1	Coarse Tune A (4 bits)
2	Fine Tune B (8 bits)
3	Coarse Tune B (4 bits)
4	Fine Tune C (8 bits)
5	Coarse Tune C (4 bits)
6	Noise Period (5 bits)
7	Output Enable (active low)
8	A Amplitude (5 bits)
9	B Amplitude (5 bits)
10	C Amplitude (5 bits)
11	Envelope Period Fine (8 bits)
12	Envelope Period Coarse (8 bits)
13	Envelope Shape/Cycle Control (4 bits)
14	not used
15	not used

Tone and/or noise are enabled by register 7:

7	6	5	4	3	2	1	0
X	X	An	Bn	Cn	At	Bt	Ct

A logic zero on any of the "n" bits enables noise from that channel. A logic zero on any of the "t" bits enables tone from that channel. Unused channels are turned off by writing logic ones in the desired bits.

Registers 8, 9 and 10 control the output amplitudes:

7	6	5	4	3	2	1	0
X	X	X	A	manual level ctrl			

A logic one in bit 4 specifies the channel's amplitude to be controlled by the envelope generator (Auto mode). If bit 4 is a zero, the amplitude is fixed by the value in bits 0-3.

The envelope generator is controlled by register 13:

7	6	5	4	3	2	1	0
X	X	X	X	cont	attk	alt	hold

Bits 0-3 describe the envelope with "continue," "attack," "alternate," and "hold." See General Instruments literature for the envelope waveforms.

The following table provides values which may be entered into the Tune registers (A, B or C) to produce the musical notes shown. Please note that the given values are approximations which best fit the required frequencies for each note. It is necessary to divide up each value and load the low 8 bits into the Fine Tune register, and the upper eight bits into the Coarse Tune register.

PSG MUSICAL NOTES

Note	Freq.	Dec.	Hex	Note	Freq.	Dec.	Hex
C 1	32.7	3402	0D4A	C 5	523.2	213	00D5
C# 1	34.6	3211	0C8B	C# 5	554.4	201	00C9
D 1	36.7	3031	0BD7	D 5	587.3	189	00BD
D# 1	38.9	2861	0B2D	D# 5	622.3	179	00B3
E 1	41.2	2700	0A8C	E 5	659.3	169	00A9
F 1	43.7	2548	09F4	F 5	698.5	159	009F
F# 1	46.2	2405	0965	F# 5	740	150	0096
G 1	49	2270	08DE	G 5	784	142	008E
G# 1	51.9	2143	085F	G# 5	830.6	134	0086
A 1	55	2023	07E7	A 5	880	126	007E
A# 1	58.3	1909	0775	A# 5	932.3	119	0077
B 1	61.7	1802	070A	B 5	987.8	113	0071
C 2	65.4	1701	06A5	C 6	1046.5	106	006A
C# 2	69.3	1605	0645	C# 6	1108.7	100	0064
D 2	73.4	1515	05EB	D 6	1174.7	95	005F
D# 2	77.8	1430	0596	D# 6	1244.5	89	0059
E 2	82.4	1350	0546	E 6	1318.5	84	0054
F 2	87.3	1274	04FA	F 6	1396.9	80	0050
F# 2	92.5	1203	04B3	F# 6	1480	75	004B
G 2	98	1135	046F	G 6	1568	71	0047
G# 2	103.8	1072	0430	G# 6	1661.2	67	0043
A 2	110	1011	03F3	A 6	1760	63	003F
A# 2	116.5	955	03BB	A# 6	1864.6	60	003C
B 2	123.5	901	0385	B 6	1975.5	56	0038
C 3	130.8	850	0352	C 7	2093	53	0035
C# 3	138.6	803	0323	C# 7	2217.5	50	0032
D 3	146.8	758	02F6	D 7	2349.3	47	002F
D# 3	155.6	715	02CB	D# 7	2489	45	002D
E 3	164.8	675	02A3	E 7	2637	42	002A
F 3	174.6	637	027D	F 7	2793.8	40	0028
F# 3	185	601	0259	F# 7	2959.9	38	0026
G 3	196	568	0238	G 7	3135.9	35	0023
G# 3	207.7	536	0218	G# 7	3322.4	33	0021
A 3	220	506	01FA	A 7	3520	32	0020
A# 3	233.1	477	01DD	A# 7	3729.3	30	001E
B 3	246.9	451	01C3	B 7	3951	28	001C
C 4	261.6	425	01A9	C 8	4186	27	001B
C# 4	277.2	401	0191	C# 8	4434.9	25	0019
D 4	293.7	379	017B	D 8	4698.6	24	0018
D# 4	311.1	358	0166	D# 8	4978	22	0016
E 4	329.6	338	0152	E 8	5274	21	0015
F 4	349.2	319	013F	F 8	5587.6	20	0014
F# 4	370	301	012D	F# 8	5919.9	19	0013
G 4	392	284	011C	G 8	6271.9	18	0012
G# 4	415.3	268	010C	G# 8	6644.9	17	0011
A 4	440	253	00FD	A 8	7040	16	0010
A# 4	466.2	239	00EF	A# 8	7458.6	15	000F
B 4	493.9	225	00E1	B 8	7902.1	14	000E

KEYBOARD

The CGC 7900 contains an intelligent keyboard, with its own 8035 microprocessor. The CPU communicates to the keyboard processor over a 12-bit data bus, 8 bits of which are bidirectional. The interface is asynchronous: each processor will interrupt the other when it has something to say.

When a key is pressed, the keyboard processor determines an 8-bit code to transmit. Most of these are 7-bit ASCII codes, except the labeled keys on the top of the keyboard produce special 8-bit codes which the CPU software must interpret. The M1, M2, CTRL and SHIFT modifiers are used by the keyboard processor to modify the transmitted code. These four keys are also brought out to the 12-bit data bus, so that the CPU can read them directly if necessary.

The keyboard processor next presents the data to the CPU, and strobes the Key Strobe line on the keyboard bus. Keyboard interface logic on the CPU card sets the Host Acknowledge line low to indicate that data has not yet been accepted by the CPU. When the CPU services the Key Strobe interrupt, the Host Acknowledge line is set high once again. The CPU services a Key Strobe interrupt by reading a word (16 bits) from address FF8080.

When the CPU wishes to modify the keyboard lights, it must write to the keyboard address. After writing to the keyboard lights once, the CPU must wait for data to be accepted before writing again. This requires waiting approximately 100 microseconds between writes to the keyboard lights.

NOTE: After the keyboard processor has accepted data for the lights, it will strobe the Key Strobe line on the CPU card. This pulse is "intercepted" by the keyboard interface logic on the CPU card and does not actually generate a CPU interrupt.

Several keys on the keyboard produce special functions:

RESET provides an active-low output directly to the CPU card, to reset the entire system. This is independent of the keyboard processor.

QUIET LOCK is an alternate action key, giving a high or low output to the CPU card. The 7900 uses this to enable and disable the speaker. This is independent of the keyboard processor.

ALPHA LOCK is an alternate action key which modifies the alphabetic ASCII characters produced by the typewriter area of the keyboard. When UP, alpha characters are normally upper case, and SHIFT modifies them to lower case. When DOWN, alpha keys are normally lower case and SHIFT modifies them to upper case. This is under control of the keyboard processor.

All keys on the keyboard are two-key rollover, except the cursor movement (arrow) keys. These four are N-key rollover, and produce unique codes when two are pressed simultaneously. When properly interpreted by the CPU, these unique codes allow diagonal cursor movement.

All keys on the keyboard have two repeat speeds (except for the special keys mentioned above). Auto repeat is invoked if a key is depressed for more than 0.75 second. Auto repeat occurs at 10 hertz. Manual repeat is invoked by pressing the desired key and simultaneously holding the REPEAT key. Manual repeat occurs at 50 hertz. The REPEAT key is also used to generate interrupts as part of the joystick interface.

KEYBOARD CABLE PINOUT

The keyboard connects to the CPU over a 26-pin ribbon cable. The lines are defined as follows:

Pin No.	Function
1	RESET to CPU (active low)
2	Data Bit 0
3	Data Bit 1
4	Data Bit 2
5	Data Bit 3
6	Data Bit 4
7	Data Bit 5
8	Data Bit 6
9	Data Bit 7
10	Data Bit 10
11	Data Bit 11
12	Data Bit 9
13	Data Bit 8
14	Quiet Lock (key up = logic high)
15	LED Strobe (active low)
16	Key Strobe (active low)
17	Host Acknowledge (high if CPU ready)
18	Repeat (low when REPEAT depressed)
19	Ground
21	Ground
23	Ground
25	Ground
20	+5 Volts
22	+5 Volts
24	+5 Volts
26	+5 Volts

KEYBOARD DATA BUS

The keyboard data bus bits are defined as follows:

Bit	Read (keyboard to CPU)	Write (CPU to keyboard)
0	Key Data Bit 0	LED Select Bit 0
1	Key Data Bit 1	LED Select Bit 1
2	Key Data Bit 2	LED Select Bit 2
3	Key Data Bit 3	LED Select Bit 3
4	Key Data Bit 4	LED Select Bit 4
5	Key Data Bit 5	
6	Key Data Bit 6	
7	Key Data Bit 7	LED Switch: 1-on, 0-off
8	SHIFT Key (active high)	
9	CTRL Key (active high)	
10	M1 Key (active high)	
11	M2 Key (active high)	

KEYBOARD LED SELECT CODES

To control an LED on the keyboard, it is necessary to place the proper LED select code on bits 0 thru 4 of the data bus, and set bit 7 high to turn the LED on, or low to turn it off. The following table provides select codes for each keyboard LED.

Key Name	Select Code (Hex)
F1	01
F2	02
F3	03
F4	04
F5	05
F6	06
F7	07
F8	08
F9	09
F10	0A
F11	0B
F12	0C
Calc Mode	0E
Rubber Band	0F
Plot	10
Roll	11
Create	12
Blink	13
Fill	14
Overlay	15
Cursor On/Off	16
2-color LED (Red)	17
2-color LED (Green)	18

Two special select codes are provided for direct control of all LEDs: Select code 00 turns all LEDs off (including the 2-color LED). Select code 1F (hex) turns on all LEDs (except the 2-color LED), regardless of the state of bit 7.

NOTE: You must wait approximately 100 microseconds between successive writes to the keyboard lights.

INTERFACING PERIPHERALS TO THE KEYBOARD PORT

Some users may wish to interface their own devices to the keyboard port on the 7900 CPU card. Any device connected to this port should conform to the cable wiring specifications given earlier. In addition, the following items should be noted:

If the keyboard device is powered by the supply provided on the keyboard port, it must draw less than 1.5 amperes at +5 volts.

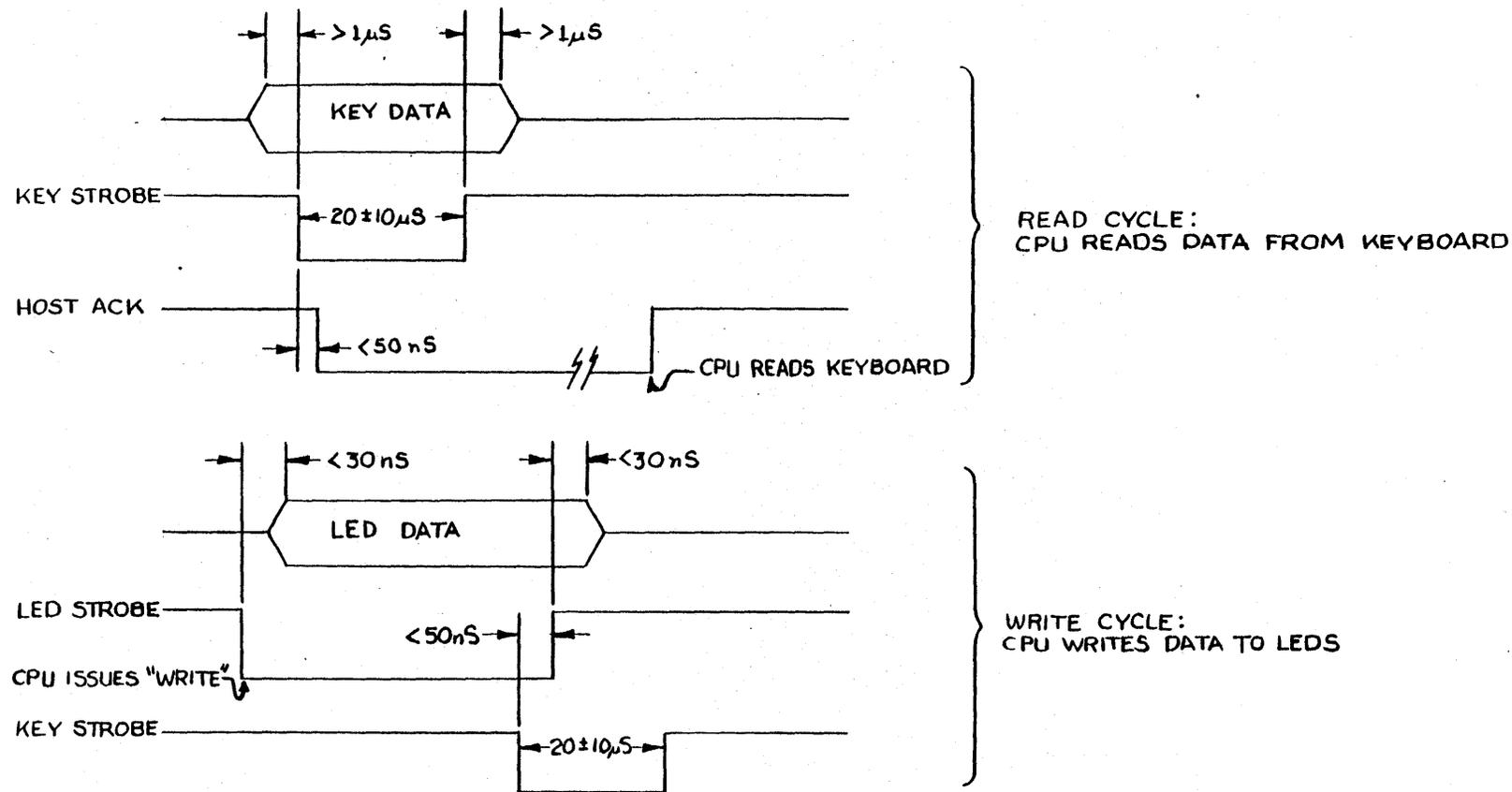
All logic levels on the keyboard bus are TTL.

When the keyboard device wishes to present data to the CPU, it must provide an active-low Key Strobe of 10 to 30 microseconds. Data must be presented on the bus during Key Strobe, and be valid at least one microsecond before and after Key Strobe. The keyboard device must recognize that while Host Acknowledge is low, the CPU is unable to receive new data.

When the CPU wants to write data to the keyboard device, it will set LED Strobe low. The keyboard device must recognize this signal as putting the keyboard bus into a "write" mode. When LED Strobe is low, the keyboard device must accept data from the CPU; then, IT MUST STROBE THE KEY STROBE LINE TO INDICATE ACCEPTANCE OF DATA. This strobe must also be 10 to 30 microseconds in duration.

NOTE: To maintain compatibility with other 7900 features, the keyboard device should provide a means for setting Quiet Lock high or low (to enable or disable the speaker), and for setting Repeat high or low (to enable interrupts from the Joystick).

KEYBOARD TIMING



HARDWARE VECTOR GENERATOR

The 7900 Hardware Vector Generator (HVG) is an optional feature. It greatly increases the speed of vectors drawn in the Bitmap. The HVG writes pixels in "Z Mode", at a rate of approximately 710 nanoseconds per pixel. (This speed is approximate since the HVG drawing operation is suspended during memory refresh cycles.)

The HVG requires four words of data: Initial X screen position, initial Y position, delta X, and delta Y. Each of these words is entered as a number in screen coordinates, between 0 and 1023. Two bits of clipping are provided; numbers between 1024 and 4095 will be recognized as "out of range" and will not be plotted. Two's complement (negative) numbers will be interpreted properly by the HVG.

Once the four data words have been loaded, the HVG requests the 7900 bus using Bus Request 1. It then receives Bus Grant, waits for the end of the current bus cycle, and asserts Bus Grant Acknowledge. The HVG then becomes bus master and draws the vector. It will, however, temporarily give up the bus if an interrupt is pending on the CPU card (this is signaled with the INTON bus line). This feature can be disabled by removing jumper J1 on the HVG. If J1 is removed, INTON will not be recognized.

The HVG occupies addresses EFC440 through EFC44F (hex). These are broken down as follows:

EFC440	Load X
EFC442	Load Y
EFC444	Load dX
EFC446	Load dY
EFC448	Load Pixel
EFC44A	Load Trip
EFC44C	Unused
EFC44E	Unused

NOTE: All of these are WORD (16-bit) addresses. You should only write words or long words, NOT BYTES, to the HVG.

NOTE: All HVG registers are write-only. Attempting to read from the HVG will cause a bus error. (If you want to write a zero into an HVG register, use the MOVE instruction, not the CLR instruction. CLR performs a read and a write, which will cause a bus error.)

Load X, Load Y, Load dX, and Load dY are registers which describe the vector (as explained above).

Load Pixel sets the pixel color, as a 16-bit number. Recall that each pixel may be up to 16 planes deep in the Bitmap.

Load Trip establishes the condition under which the HVG will begin to draw a vector. After a RESET, the HVG is set to "trip" when you write to the Load dY register. However, you may choose to "trip" the HVG by writing to some other data register. The bottom two bits of Load Trip decide this:

Load Trip	Draws After Writing To
0	Load dY
1	Load dX
2	Load Y
3	Load X

NOTE: After each vector is drawn, the "Load X" and "Load Y" values are internally updated to point to the END of the vector. This makes it simple to draw concatenated vectors, by writing the new delta-X and delta-Y into the appropriate registers. The Load X and Load Y registers need only be reloaded when you begin a new set of concatenated vectors.

SAMPLE HVG PROGRAMS

```

*
*   HVG test program to draw one 45 degree vector.
*   Draws from 0,0 to 512,512. Assumes Load Trip is set
*   to zero (as it would be after RESET)
*

```

```

HVG     EQU     $EFC440
X       EQU     HVG
Y       EQU     HVG+2
DX      EQU     HVG+4
DY      EQU     HVG+6
COLOR   EQU     HVG+8

```

```

ORG.L   $1F000

```

```

MOVE.W  #1,COLOR      Select color 1 (normally blue)

```

```

MOVE.W  #0,X          Set initial X and Y to zero
MOVE.W  #0,Y          (upper left corner of screen)

```

```

MOVE.W  #512,DX       Set delta-X to 512
MOVE.W  #512,DY       And delta-Y also

```

```

*   Now the HVG goes off and does its thing....

```

```

*
*   Here's a faster way to draw the same vector:
*

```

```

MOVE.L  #0,X          Load X and Y at once
MOVE.L  #512*65536+512,DX  Load delta-X and delta-Y

```

```

RTS

```

If a picture is described as a set of vectors, the fastest way to draw the picture would be to arrange the data as a list of X's, Y's, delta-X's and delta-Y's. Then an assembly language program can read long words from the data list, feeding them straight to the HVG. This could be written as:

```
*
*   Initialize everything in registers first.
*
      LEA    X,A0
      LEA    DX,A1
      LEA    List,A2
*
*   Now draw the picture.
*
Loop  MOVE.L (A2)+,(A0)    Load X and Y registers
      MOVE.L (A2)+,(A1)    Load delta-X and delta-Y
*
*   Check for end-of-list somehow...
      BRA.S  Loop          If not end of list, continue.
```

The above program could run even faster if the picture was composed of concatenated vectors, since the Load X and Load Y values would not have to be rewritten for each vector.

INTERFACE SUGGESTIONS

User peripherals may be connected to the "BCS" bus lines for selection. If this address space is insufficient, it will be necessary to develop an interface circuit. The guidelines below may be helpful in such an effort.

SIGNAL BUFFERING: All signal to/from the bus should be buffered, using Schmitt triggered devices. For unidirectional lines, a 74LS244 is satisfactory; use a 74LS245 or similar for bidirectional lines, such as data lines. Open collector lines should be driven with a 74LS38 or similar gate. User devices should not present more than one TTL load (per card) to the bus.

ADDRESS SELECTION: Chromatics reserves the upper half of address space, beginning at 800000 hex. User peripherals should be selected below 7FFFFFF to insure compatibility. Address Strobe (AS*) must be included in the select equation.

FUNCTION CODES: The Function Codes (FC0* - FC2*) may be included in the equation if it is desired to exclude one or more of the address spaces from selection. This will not usually be necessary.

DTACK AND VPA: A device must assert either Data Transfer ACKnowledge (DTACK*) or Valid Peripheral Address (VPA*) to indicate transfer of data on a read or write. If DTACK is used, it must be asserted after the select equation has been satisfied, using the address lines, AS*, FC0* - FC2* (if used), and one or both Data Strobes (UDS* or LDS*). If a device has slow access time, DTACK must be delayed to allow proper response time for the device. A delay line clocked by SYSCLK will usually work well.

DTACK must be removed when the Data Strobes are removed. Note that certain 68000 bus cycles have two Data Strobes within a single Address Strobe, so AS* is not sufficient to qualify DTACK.

If VPA is used instead of DTACK, the system will execute a slow cycle with 6800 characteristics. Using VPA instead of DTACK may result in a simpler interface for slow devices.

DATA STROBES: Once the select equation has been satisfied, the Data Strobes (UDS* and LDS*) perform the actual data transfer. Devices must produce data prior to the rising edge of a Data

Strobe on a read cycle, and must accept data on the rising edge of a Data Strobe during a write. UDS* is clocked for even bytes, and LDS* for odd bytes. Both are active simultaneously during a word access.

INTERRUPTS: A device requests an interrupt by driving an IRQ line low. (IRQ's are open-collector lines on the bus.) The processor will respond by performing an interrupt acknowledge cycle, which drives INTACK* low, and placing the 3-bit level number on address lines A01 through A03. Other address lines are high at this time, and the Function Codes indicate an interrupt acknowledge is in progress.

The user's device must recognize INTACK*, in coincidence with the proper level number on A01 - A03, and provide a vector number on the low 8 data lines. DTACK must also be provided to transfer the vector number. The 68000 will then fetch the service routine address from the vector provided, and begin interrupt service. The service routine must clear the IRQ.

Interrupt levels 4, 5, and 7 are in use on the CPU card. Levels 1, 2, 3, and 6 are available for expansion hardware, and may already be in use in your system depending on options installed. (The SPC and DMA/PIO can both use interrupts.)

To install more than one device at the same interrupt level, provide a method to prioritize interrupts among the various devices. A daisy-chain is one possible method: the first device in the chain will test INTACK*, and pass this signal to the next device in the chain if no interrupt request is pending in the first device. When this rippled INTACK* signal reaches the first device with an active interrupt pending, that device will provide the vector. The ripple stops at that device, so that later devices in the chain do not try to provide a vector.

Only the device providing the vector should provide DTACK. If no device provides DTACK, a spurious interrupt is declared.

Autovectoring is possible in the 7900, but not recommended since it severely limits the number of interrupt-driven devices in the system.

SYNC SIGNALS

The CGC 7900 uses interlaced scan. Odd-numbered raster lines are scanned during one field, and even-numbered lines are scanned during the next field. The fields are synchronized to the 60-cycle power line, so each field lasts 1/60 second, and it takes 1/30 second to display an entire frame. Interlacing is achieved by delaying the start of vertical sweep on odd fields.

The display scans 768 lines, with 1024 pixels per line. Each pixel is scanned for 35.11 nanoseconds. Three 8-bit digital-to-analog converters receive red, green and blue data from the Digital Chassis and convert this data into three video signals. RGB video output is available.

All of the following signals are available at the Analog Chassis, behind the CRT tube of the 7900. All sync signals are differential TTL, and may be received with Advanced Micro Devices AM26LS33 or equivalent. Note that the polarity of the received signal may be altered to suit your equipment by swapping the input lines to the receiver. Sync signals are found at J6, a 10-pin right-angle connector near the front corner of the Deflection Module. It is suggested that a Y-cable arrangement be used to feed these signals into the 7900 and the user's equipment.

NOTE: To prevent possible damage to the CGC 7900, insure that J6 is properly connected BEFORE applying power to the system. External devices connected to J6 must NOT impair the normal sync signals at this connector!

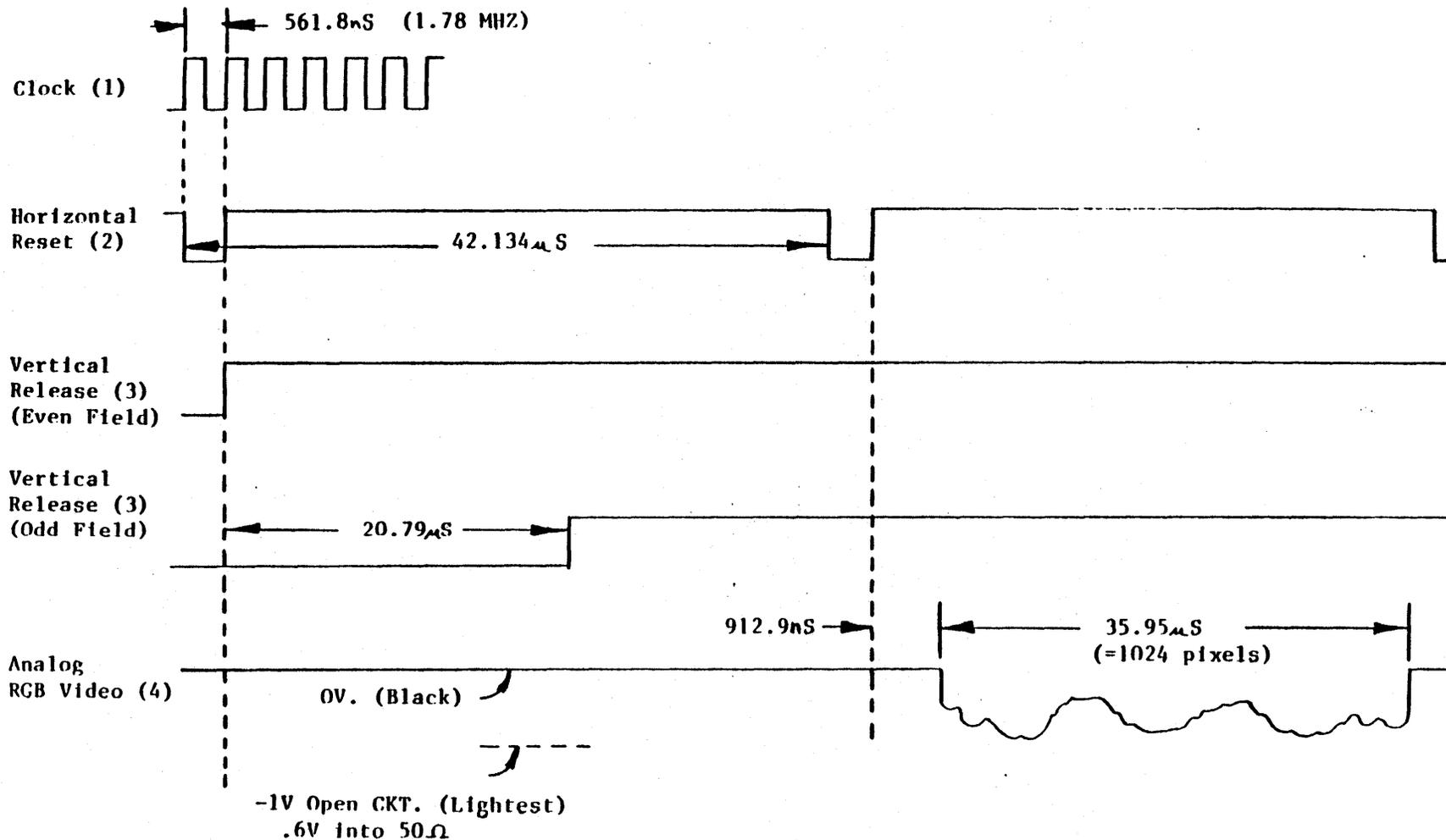
(1) Clock: J6 pins 4 and 9 (red/black pair). A 1.78 MHz square wave, from which all other syncs are derived. When video is active, 16 pixels are scanned during each cycle of this clock.

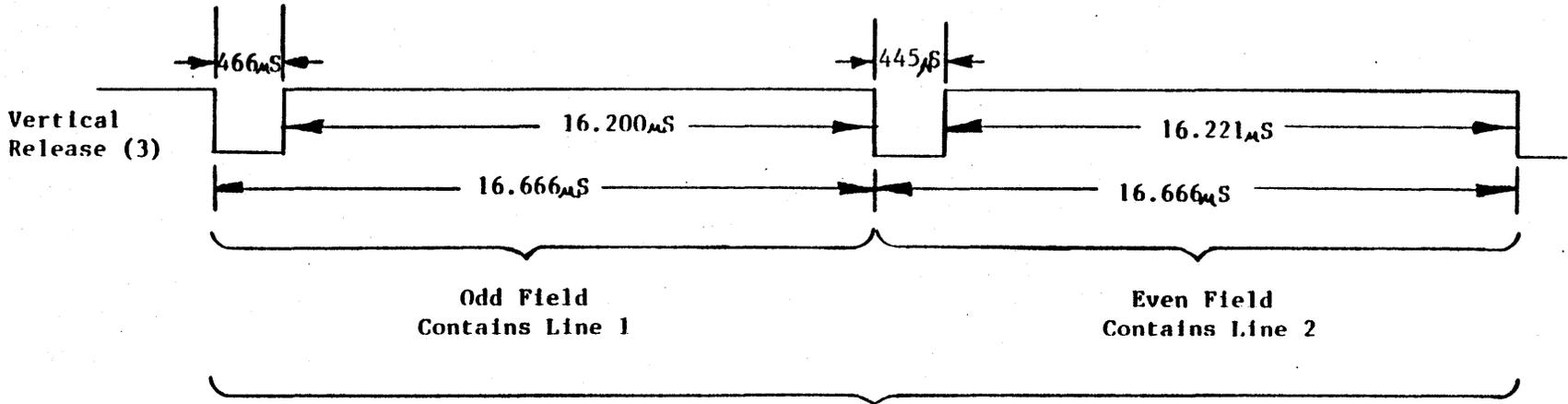
(2) Horizontal Reset: J6 pins 2 and 7 (yellow/black pair). The sync signal which triggers each horizontal line. Video begins 912.9 nanoseconds after Horizontal Reset goes high.

(3) Vertical Release: J6 pins 1 and 6 (green/black pair). The sync signal which triggers vertical sweep, and inhibits sweep at the proper times to provide interlace. On even fields, this signal rises simultaneously with a Horizontal Reset rising edge. On odd fields, it is delayed by 20.79 microseconds for interlace. The falling edge of this signal is triggered by power line frequency (60 hertz).

(4) Analog Video: These three signals are available on the Video Amplifier card, on the back wall of the Analog Chassis. P1 provides green, P2 is blue, and P3 is red. These signals should be received by a 50-ohm coaxial cable in each of the connectors. For best results, a 50-ohm load should be provided at the user's end of the cable. The voltage levels at each of these connectors are: zero for black, minus one volt (nominal) for maximum intensity. This level may not be adjusted without disturbing the 7900 video alignment.

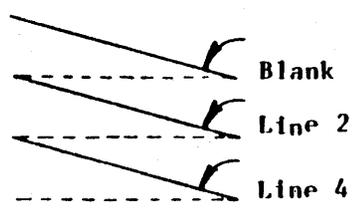
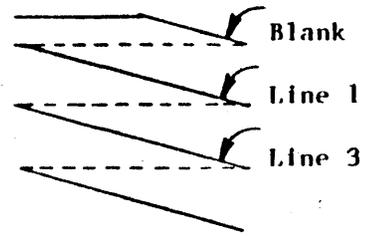
HORIZONTAL TIMING





VERTICAL TIMING

One Frame (Interlaced)



CGC 7900 SYSTEM BUS

The 7900 system bus uses two connectors, P1 and P2. P1 is the main connector for address, data and control lines, interfacing the CPU to memory and peripherals. P1 is the upper connector in the digital chassis.

P2 is the lower connector in the digital chassis. P2 is used for video data and control, including signals used to control the analog high voltage supplies. For this reason, it is recommended that P2 be considered a reserved area, for Chromatics' use only. **DAMAGE TO THE SYSTEM COULD RESULT IF USER DEVICES ARE CONNECTED TO P2!**

CGC 7900 circuit cards have the same physical dimensions as required by the Motorola VERSAbus specification. However, the bus arrangement differs significantly (see the following pages). In general, VERSAbus cards **MAY NOT** be plugged directly into the CGC 7900 card cage.

P1 CONNECTOR IDENTIFICATION

Odd Pin No. Component Side	Signal Name	Even Pin No. Circuit Side	Signal Name
1	+5V	2	+5V
3	GND	4	GND
5	D00	6	D01
7	D02	8	D03
9	D04	10	D05
11	D06	12	D07
13	D08	14	D09
15	D10	16	D11
17	D12	18	D13
19	D14	20	D15
21		22	
23	GND	24	GND
25	LDS*	26	UDS*
27	GND	28	GND
29	DTACK*	30	AS*
31	GND	32	GND
33		34	READ/WRITE*
35		36	A01
37	A02	38	A03
39	A04	40	A05
41	A06	42	A07
43	A08	44	A09
45	A10	46	A11
47	A12	48	A13
49	A14	50	A15
51	A16	52	A17
53	A18	54	A19
55	A20	56	A21
57	A22	58	A23
59		60	
61	GND	62	GND
63		64	
65		66	
67	GND	68	GND
69		70	SYSCLK

71	GND	72	GND
73	BCS1*	74	SYSRESET*
75	BCS3*	76	BCS2*
77	BCS5*	78	BCS4*
79		80	BCS6*
81	BUSERR*	82	
83	FC0*	84	FC1*
85	FC2*	86	
87	IRQ1*	88	IRQ2*
89	IRQ3*	90	IRQ4*
91	IRQ5*	92	IRQ6*
93	IRQ7*	94	INTON*
95	IACKIN*	96	LPEN*
97	BG0*	98	BINT1*
99	BG1*	100	BINT2*
101	BG2*	102	BINT3*
103	BG3*	104	BINT4*
105	BG4*	106	BINT5*
107	BRQ0*	108	BRQ1*
109	BRQ2*	110	BRQ3*
111	BRQ4*	112	
113	BGACK*	114	BVPA*
115		116	
117		118	ADDR0-7*
119	GND	120	GND
121	-12V	122	-12V
123	GND	124	GND
125	+12V	126	+12V
127	+12V	128	+12V
129	+5V	130	+5V
131	+5V	132	+5V
133	-5V	134	-5V
135	GND (FOR CMOS +5)	136	GND
137	GND	138	GND
139	GND	140	GND

P1 SIGNAL DESCRIPTIONS

D00-D15 (pins 5-20): The tristate, bidirectional data bus.

LDS* (pin 25): Lower Data Strobe. An active low, tristate signal which indicates a data transfer on D00-D07.

UDS* (pin 26): Upper Data Strobe. An active low, tristate signal which indicates a data transfer on D08-D15.

DTACK* (pin 29): Data Transfer ACKnowledge. An active low, open collector signal generated by a peripheral or memory device. It indicates acceptance of data during a write, or that data has been placed on the bus in response to a read. If a non-existent memory location is accessed and DTACK* does not occur, a bus error is generated.

AS* (pin 30): Address Strobe. An active low, tristate signal which indicates that a valid address is present on the address lines.

READ/WRITE* (pin 34): A tristate signal used to define the type of cycle in progress. This line is high for a read cycle, low for a write cycle.

A01-A23 (pins 36-58): Tristate address bus. Note that the lowest bit of the address is simulated by UDS* and LDS*, for 8-bit accesses.

SYSCLK (pin 70): System Clock. This is the highest frequency clock used on the bus, 14.24 MHz in the standard 7900 system.

BCS1*-BCS6* (pins 73, 75, 76, 77, 78, 80): Bus Chip Selects. Active low outputs from the CPU used to select certain areas of memory. See "System Memory Map."

SYSRESET* (pin 79): System Reset. An active low, open collector signal used to reset the system. It may be generated by the processor or by external devices. This line is held low during power-up.

BUSERR* (pin 81): Bus Error. An active low, open collector line which is pulled low in the event of a catastrophic system failure. The 7900 uses this for memory parity error.

FC0*-FC2* (pins 83-85): Function Code. Active low, tristate lines which indicate the state of the bus master, such as whether an interrupt acknowledge cycle is in progress.

IRQ1*-IRQ7* (pins 87-93): Interrupt Request. Open collector, active low lines which may be pulled low by peripherals to request an interrupt. IRQ7* is highest priority and is used during power-up.

INTON* (pin 94): Interrupt On CPU. Active low signal which indicates one of the 16 interrupts on the CPU card is pending. Should be tested by secondary bus masters, to allow them to release the bus if an interrupt is waiting for service.

IACKIN* (pin 95): Interrupt Acknowledge In. Active low signal which indicates the CPU is fetching an interrupt vector.

LPEN* (pin 96): Light Pen Interrupt. Active low, open collector signal asserted by the Light Pen logic when a hit is detected.

BG0*-BG4* (pins 97, 99, 101, 103, 105): Bus Grant. Active low signals which inform a device that it may become the bus master. Issued by the CPU in response to Bus Request. All tristate signals will go to a high impedance at the end of the bus cycle in which a Bus Grant is asserted.

BINT1*-BINT5* (pins 98, 100, 102, 104, 106): Bus Interrupt. Active low, open collector signals which allow peripherals to interrupt the CPU card. See "Interrupt Mask" for details.

BRQ0*-BRQ4* (pins 107-111): Bus Request. Active low, open collector signals used by secondary bus masters to gain access to the bus. BRQ4* is highest priority.

BGACK* (pin 113): Bus Grant Acknowledge. Active low signal asserted by the secondary bus master when it has assumed control of the bus.

BVPA* (pin 114): Bus Valid Peripheral Address. Active low signal which informs the CPU that an MC6800 peripheral device is responding to the current bus cycle.

ADDR0-7* (pin 118): Addresses 0-7 in use. Active low signal, asserted when memory locations 000000 thru 000007 are being accessed. Used during power-up to disable RAM and enable EPROM.

GND (for CMOS +5) (pin 135): This is the supply return for the CMOS battery power. It should not be used for normal grounding purposes.

P2 CONNECTOR IDENTIFICATION

Odd Pin No. Component Side	Signal Name	Even Pin No. Circuit Side	Signal Name
1	ground	2	ground
3	ground	4	ground
5	ground	6	ground
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13		14	
15	IBIT0	16	IBIT1
17	IBIT2	18	IBIT3
19	PWO	20	R*
21	CSF*	22	CSB*
23	PWE	24	PSEL*
25	VM0	26	VM1
27	VM2	28	VM3
29	VLC	30	VDE0*
31	VDE1*	32	IBSEL
33	VB00	34	VB01
35	VB02	36	VB03
37	VB04	38	VB05
39	VB06	40	VB07
41	VB08	42	VB09
43	VB10	44	VB11
45	VB12	46	VB13
47	VB14	48	VB15
49	VB16	50	VB17
51	VB18	52	VB19
53	VB20	54	VB21
55	VB22	56	VB23
57	VB24	58	VB25
59	VB26	60	VB27
61	VB28	62	VB29
63	VB30	64	VB31
65	VB32	66	VB33
67	VB34	68	VB35
69	VB36	70	VB37

71	VB38	72	VB39
73		74	
75	BLINK	76	OLC
77	IVLC	78	PSW*
79	LBNK*	80	RA1
81	RA2	82	RA3
83	RA4	84	RA5
85	RA6	86	WU*
87	WL*	88	BIT*
89	CSE	90	EP*
91		92	LXZ*
93	MRAS*	94	VERT*
95	RFSH*	96	OMEM*
97	MCAS*	98	CROLL*
99	RAS*	100	CAS*
101	ground	102	ground
103	CH	104	HG
105	VMUX	106	
107	RC0	108	RC1
109	RC2	110	RC3
111	RC4	112	RC5
113	RC6	114	
115		116	
117		118	14M
119	-5V	120	-5V

P2 SIGNAL DESCRIPTIONS

IBIT0-IBIT3 (pins 15-18): These lines hold a 4-bit number used to select one of 16 planes (in Plane Mode) or one of 16 bits (in Z Mode), according to the state of IBSEL.

PWO (pin 19): Plane Write Override. Keeps Plane Select latches from affecting memory accesses in Plane Mode. This line is high when Plane Mode addresses are used.

R* (pin 20): Read (active low).

CSF*, CSB* (pins 21 and 22): Color Status Foreground and Background strobes. These lines strobe information into the Color Status latches.

PWE (pin 23): Plane Write Enable. This line enables Plane Mode access to memory when low, and Z Mode or Color Status Mode when high. When asserted, this line overrides the IBIT lines.

PSEL* (pin 24): Plane Select strobe. This line strobes information into the Plane Select latch (1 bit per plane).

VM0-VM3 (pins 25-28): Video Mux select. Selects which 4 bits are currently being brought out on VB00-VB39 for display.

VLC (pin 29): Video Latch Control. This line strobes data from video RAM into latches, prior to bit selection by VM0-VM3.

VDE0*-VDE1* (pins 30-31): Video Data Enable. One of these two lines will be low, determining whether image planes 0-7 or 8-15 are currently being displayed.

IBSEL (pin 32): Selects Bit (Z mode) or Plane mode access to image memory.

VB00-VB39 (pins 33-72): Video Bus. Data from video RAM is brought out on these lines, 4 bits at a time, from each of 10 possible planes. (Note: only 8 planes, 0 thru 7, are currently supported by the CGC 7900.) Each of these lines is named in the form VBbp, where b is the bit number (0-3) and p is the plane number (0-9), of the data on the line.

BLINK (pin 75): A 1.9 Hz blink signal used to blink information

from image memory.

OLC (pin 76): Output Latch Control. This line strobes data out of image memory when the CPU wishes to read from image memory.

IVLC (pin 77): Internal Video Latch Control. This line strobes data from image RAM into "holding" latches, prior to the latches strobed by VLC.

PSW* (pin 78): Plane Video Switch. This line strobes data into the Plane Switch latches, to determine which planes are fed to the Color Lookup Table for display.

LBNK* (pin 79): Load Blink Select. This line strobes data into the Blink Select latches, to determine whether the data from each plane will blink (be masked to zero) at the rate set by BLINK.

RA1-RA6 (pins 80-85): RAM Address. In Z Mode, these lines select a pixel to be read or written. In Plane Mode, they choose one 16-bit word from the 64-bit internal data bus of the RAM card.

WU*, WL* (pins 86-87): Write Upper/Write Lower. Active low signals formed by gating UDS* and LDS* with the Write line.

BIT* (pin 88): Bit mode. Active low signal indicating a Bit mode (Z mode) access is in progress.

CSE (pin 89): Color Status Enable. This signal allows the Color Status addressing mode to become active.

EP* (pin 90): Reserved for future use (hardware erase-page function).

LXZ* (pin 92): Load X Zoom. This active low signal strobes a 4-bit number into the X Zoom register on the Color Lookup card.

MRAS*, MCAS* (pins 93 and 97): Memory Row Address Strobe and Column Address Strobe. These RAM control lines are used during CPU accesses.

VERT* (pin 94): Vertical Retrace. This line is low during the vertical retrace blanking interval.

RFSH* (pin 95): Refresh. This signal is used during memory refresh cycles.

OMEM* (pin 96): This signal pre-decodes some of the CMOS address space for video hardware latches.

CROLL* (pin 98): Character Roll strobe. This strobe loads the Overlay Roll Counter latch.

RAS*, CAS* (pins 99 and 100): Row Address Strobe and Column Address Strobe. All other memory control lines are derived from these two signals, which are always present regardless of the type of memory cycle in progress.

CH (pin 103): Character Horizontal. This signal enables the fetch of data for video display. It is advanced from HG to compensate for delays in fetching pixel data thru the Color Lookup Table.

HG (pin 104): Horizontal Gate. This is the horizontal sync signal.

VMUX (pin 105): Video Mux. This clock runs the counters whose outputs appear on VM0-VM3.

RC0-RC6 (pins 107-113): Row/Column addresses. These lines contain the addresses of whatever image memory is being accessed, in the matrixed form required by dynamic RAM.

14M (pin 118): The 14.24 MHz master clock. SYSCLK on P1 is synchronized to this signal, however its phase is different due to propagation delays.

INDEX

Capitalized entries correspond to chapter headings, and are listed in the Table of Contents.

Address selection 91
Address space 13
Alpha Lock key 80
Analog video signals 93

Background color 21
BAUD RATE GENERATOR 57
BCS 64
BCS1 ADDRESSES 65
BEZEL SWITCHES 60
BINTs 61,63
Bitmap memory 5
BITMAP ROLL COUNTER 42
Bitmap, scrolling 42
Blink (Overlay) 24,51
Blink plane 17
BLINK SELECT 46
Blue flood 65
Buffer memory 5,13
Buffer Memory, 128K 31
Buffer Memory, 512K 32
BUFFER MEMORY ADDRESS 33
BUFFER MEMORY CARDS 5
BUFFER MEMORY PARITY 67
Buffering bus signals 91
BUS CHIP SELECTS 64
Bus error 16,87
BUS INTERRUPTS (BINT) 63

Clipping, HVG 87
CGC 7900 DETAILED MEMORY MAP 27
CGC 7900 HARDWARE OVERVIEW 2
CGC 7900 MEMORY MAP 13
CGC 7900 SYSTEM BUS 97
CGC 7900 SYSTEM MEMORY MAP (Illustration) 11
Clipping, HVG 87
CLR instruction 87
CLU ADDRESSES 23
CLU jumpers 35
Color Lookup Card 6
COLOR LOOKUP TABLE 6,20,22
COLOR STATUS 20,49
CONFIGURATION, MEMORY CARDS 5,31-40
CPU CARD 3
CPU interrupt levels 61
CRT 2
Current capacity 9
Cursor (Overlay) 24

Disk controller 68
DEC computers 7
Disk controller 68
DISK PORT 68
DISK PORT PINOUT 70
DMA/PIO 7
DTACK 91

EPROM 4,14
EPROM installation 14-15
EPROM/RASTER PROCESSOR CARD 4

Firmware 13
Foreground color 21
Function codes 91
Function keys 41

HARDWARE LATCHES 41
HARDWARE VECTOR GENERATOR 87
Horizontal retrace 66
HORIZONTAL TIMING 95
HVG 87
HVG programming 89

I/O MAP 53
I/O hardware 3
IMAGE MEMORY 16
IMAGE MEMORY CARDS 5
IMAGE MEMORY CONFIGURATION 40
IMAGE SELECT 51
INTERFACE SUGGESTIONS 91
INTERFACING PERIPHERALS 84
INTERFACING RS232 AND RS449 56
Interlacing 93
INTERRUPT HANDLING 61
INTERRUPT MASK 62
Interrupt servicing 92
Interrupt vectors 13,92
INTRODUCTION 1

JOYSTICK 58

KEYBOARD 79
KEYBOARD CABLE PINOUT 81
KEYBOARD DATA BUS 82
KEYBOARD LED SELECT CODES 83
Keyboard lights 83
Keyboard lights, delay 79
Keyboard processor 79
KEYBOARD TIMING 85

LIGHT PEN 65

Manuals, 7900 1
Memory Controller 6
Memory Map (description)13
Memory Map (detailed)27
Memory Map (illustration)11
Memory, buffer 5
Memory, image 5
Motherboard 2

Overlay 6,24
OVERLAY ADDRESSES 26
OVERLAY CHARACTER BLINK 51
OVERLAY CURSOR BLINK 51
OVERLAY CURSOR BLINKS1
OVERLAY MEMORY ADDRESSING 24
OVERLAY ROLL COUNTER 50
Overlay, scrolling 50

P1 CONNECTOR IDENTIFICATION 98
P1 SIGNAL DESCRIPTIONS 100
P2 CONNECTOR IDENTIFICATION 103
P2 SIGNAL DESCRIPTIONS 105
Pan, Bitmap 43
Parity 5,67
PIO (parallel I/O) 7
Pixel data 18,20
PLANE MODE 17
Plane numbers, recommended 34
PLANE SELECT 18,21,47
PLANE VIDEO SWITCH 48
Plot dots (Overlay) 24,25
Power requirements 10
POWER SUPPLY 2,9
Priority levels 61
PROGRAMMABLE SOUND GENERATOR 74
Programming EPROMs 14
PROGRAMMING THE PSG 75
PSG MUSICAL NOTES 78
PSG REGISTERS 76

Quiet Lock key 80

Raster Processor card 14
Raster processor 4
RAM, CMOS/static 3,13,41
RAM, dynamic 5
REAL TIME CLOCK 3,71
Refresh memory 16
Regulators, power 10
Reset key 80
RGB components 22
Rollover, keyboard 80
RS232 54-56
RS449 54-56

SAMPLE HVG PROGRAMS 89
SERIAL PORT CONTROLLER 8
SERIAL PORT PINOUTS 55
SERIAL PORTS 54
Sound generator 3
SPC 8
Sound generator 3
SYNC ADDRESSES 66
SYNC SIGNALS 93

Terminators 4
Thaw command 13,41

Vertical retrace 22,43-45,66
VERTICAL TIMING 96
VIDEO CONTROL CARDS 6
Visible Overlay cells 24
Voltages 9
VPA 91

X AND Y ZOOM 45
X PAN 43

Y PAN 44

Z MODE 18
Z00 8
Zoom, X and Y 45