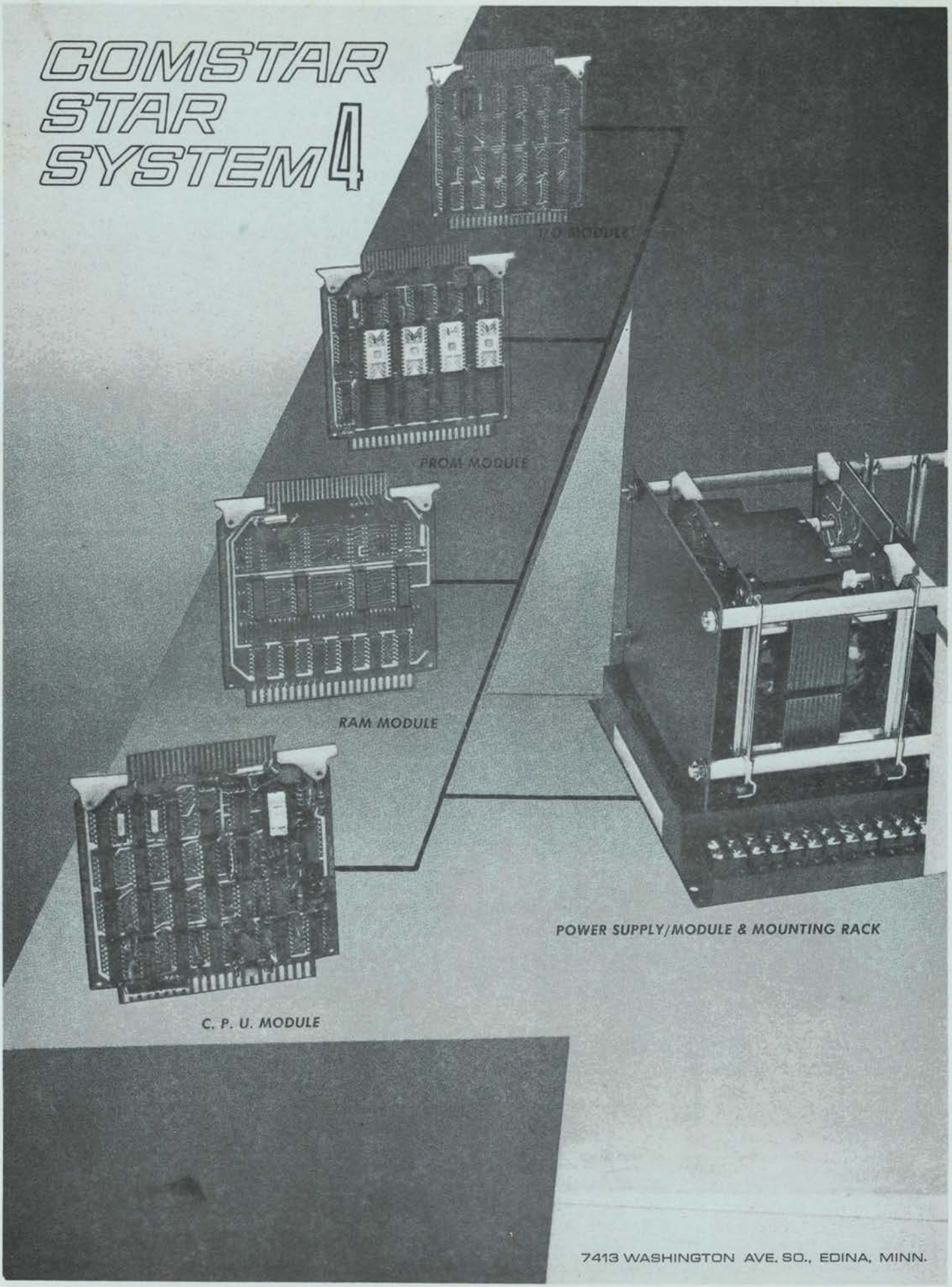
COMSTAR STAR SYSTEM 4



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P R E F A C E

INTERIM COMSTAR STAR SYSTEM 4 USERS MANUAL

WE WILL BE REVISING THE MANUAL
TO IMPROVE AND UPDATE ITS INFORMATION.
WE WELCOME ANY SUGGESTIONS OR COMMENTS
YOU MIGHT HAVE FOR IMPROVING THE MANUAL.

THANK YOU
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STAR SYSTEM 4
MICRO COMPUTER SET

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THE ALTERNATIVE TO RANDOM LOGIC SYSTEMS

GENERAL DISCUSSION

Since its inception, digital computer applications have evolved from calculation through data processing and into control. The development of the minicomputer has vastly increased the scope of computer usage. In particular, the use of minicomputers in dedicated applications has had a profound effect on systems design.

Many engineers have found that a minicomputer at the heart of a system offers significant advantages. Minicomputer systems are more flexible, can be easily personalized for a particular customer's requirements, and can be more easily changed or updated than fixed-logic design systems. For most designers, the programming of a minicomputer is a much easier and more straightforward procedure than designing a controller with random logic.

Unfortunately, the size and cost of even the smallest minicomputer has limited its use to relatively large and costly systems. This has resulted in many smaller systems being implemented with complicated random logic.

COMSTAR NOW OFFERS ANOTHER ALTERNATIVE.....

.....THE COMSTAR STAR SYSTEM 4 MICRO COMPUTER SET

THE ADVANTAGES OF A MINICOMPUTER AT ONE TENTH THE COST.

This new concept in Large Scale Integration (LSI) technology makes the power of a general purpose computer available to almost every logic designer and represents a strong attack on the dependency of systems manufacturers oncomplicated random logic systems. This MICRO-COMPUTER from COMSTAR can provide the same arithmetic, control and computing functions of a minicomputer in as few as 3 small circuit boards plus power supply and costs about one tenth as much.

A NEW CONCEPT FOR CONTROL JOBS TOO SMALL FOR A MINICOMPUTER.

The STAR SYSTEM 4 is fully as flexible and versatile as the best minicomputer. The only significant difference is in operating speed. The STAR SYSTEM 4 is actually capable of performing most tasks currently done by minicomputer where speed capabilities of the minicomputer are not heavily taxed. But the STAR SYSTEM 4 is by no means slow. For one application, SS-4s are currently in use in a tape editing system reading and punching paper tape at 110 characters per second and editing the data between characters. The SS-4 can execute roughly 100,000 instructions per second!

The heart of each system is a single card central processor unit (CPU) which performs all control and data processing functions. Auxiliary to the CPU are Programmable Read Only Memories (PROM) which store microprograms and data tables; Random Access Memories (RAM) which store data, and Input/Output cards which constitute the Input/Output capacity of the system. The Star System 4 (SS-4) system communicates with circuits and devices outside the family through Input/Output "ports" provided on each RAM and I/O card.

A system using this set of devices will usually consist of one CPU card, from one to 16 PROM's on one or two cards, up to 16 RAM's on one or two cards and up to 16 I/O cards. A minimum system could be designed with just one CPU card, one PROM card and one I/O card. With these components, you can build distributed, dedicated, or personalized computers and utilize INIFINITE COMBINATIONS OF MICROPROGRAMMING. The designer buys standard devices, and with micro-programming of the PROM, fulfills his own unique circuit requirements.

COMSTAR MICROCOMPUTERS

FEATURE FOUR MAJOR

ADVANTAGES

GREAT SYSTEM FLEXIBILITY

Easily reprogrammable; ability to increase or decrease the system; small size and low power.

EXPEDIENCY OF DESIGN

PROM programming is easier than random circuit design, therefore checkout is easier using electrically programmable and erasable PROM's and ability to insert new microprograms means no system obsolescence.

MANUFACTURING ECONOMIES

Come from compact package design, lower labor costs, lower inventory of parts and boards.

COMPLETE I/O CAPABILITY

The SS-4 is directly compatible with the full line of COMSTAR's Lee Logic Industrial Modules for signal conditioning, logic, and driver modules, and can directly drive up to 576 inputs and outputs.

SIMPLICITY OF DESIGN

When designing with random logic (logic gates, flip flops, etc.), the designer will usually start with a description of the desired function and attempt to wire counters, gates, etc. to achieve this function. Switches, displays, etc. are also connected to the logic. To correct errors or make changes in a design usually requires significant changes in wiring, often requiring that circuit boards be scrapped and replaced by new ones.

To do the same design with the SS-4 MICRO COMPUTER SET, the designer again starts with the functional description. However, he implements the required functions by encoding suitable sequences of instructions in the PROM. The SS-4 instruction set is quite complete and allows a wide variety of functions to be performed: decimal or binary arithmetic, counting, decisions, and table-lookup, switches, displays, keyboards, solenoids, etc.

As a result of this organization, the entire logic, the "personality" of the machine is determined by the instructions in PROM. Very significant modifications of machine characteristics can be made by changing or adding PROM's without making any changes in wiring or circuit boards.

THE COMSTAR SET OFFERS TREMENDOUS FLEXIBILITY OF DESIGN AND ALLOWS THE USER TO HAVE MANY OF THE DESIRABLE FEATURES OF A CUSTOM CIRCUIT DESIGN - - - - - - - -

SMALL NUMBER OF CARDS, A SET OF COMPONENTS WHICH IS UNIQUELY HIS OWN (FOR EACH USER'S PROGRAM ROUTINES ARE HIS PROPRIETARY PROPERTY)

------AND YET HAVE NONE OF THE DISADVANTAGES OF LONG DEVELOPMENT CYCLE, HIGH DEVELOPMENT COST, ETC.

APPLICATIONS

FOR THE

SS-4 MICRO COMPUTER SET

The heart of the COMSTAR SS-4 micro computer set is the CPU. This device has a powerful and versatile instruction set which allows the system to perform a wide variety of arithmetic, control and decision functions. The microprograms stored in the PROM devices give the designer the power of designing custom computers with standard components. You can use the SS-4 almost anywhere.

Here are a few examples.....

APPLICATIONS....

CONTROL FUNCTIONS - BECAUSE OF LOW INITIAL COST AND FLEXIBILITY OF PROGRAMMING, THE SS-4 CAN BE USED IN PLACE OF RANDOM LOGIC IN SYSTEMS SUCH AS THOSE IN PROCESS CONTROL, NUMERIC CONTROLS, ELEVATOR CONTROLS, HIGHWAY AND RAIL TRAFFIC CONTROLS. BY CHANGING PROM MICRO-PROGRAMS THE WHOLE SYSTEM CAN EASILY BE MODIFIED AND UPDATED.

COMPUTER PERIPHERALS - THE SYSTEM CAN BE CONVENIENTLY USED IN PERIPHERAL EQUIPMENT TO CONTROL DISPLAYS, KEYBOARDS, PRINTERS, READERS, PLOTTERS, AND TO GIVE INTELLIGENCE TO TERMINALS.

APPLICATIONS . . .

COMPUTING SYSTEMS - THE SS-4 SYSTEM IS IDEALLY SUITED FOR SUCH DEVICES AS BILLING MACHINES, CASH REGISTERS, POINT OF SALE TERMINALS AND ACCOUNTING MACHINES. FOR EXAMPLE, THE ADDING OF TWO 8 DIGIT NUMBERS CAN BE DONE IS 850 MICROSECONDS. IN ADDITION, THE SS-4 CAN BE EFFICIENTLY USED TO DECENTRALIZE CENTRAL COMPUTER FUNCTIONS.

OTHER APPLICATIONS - THE ELEMENTS OF THE SS-4 HAVE MANY APPLICATIONS WITHIN TRANSPORTATION, AUTOMOTIVE, MEDICAL ELECTRONICS AND TEST SYSTEMS, WHERE INEXPENSIVE DEDICATED COMPUTERS CAN IMPROVE SYSTEM PERFORMANCE.

FEATURES OF THE STAR SYSTEM 4

* 4-BIT PARALLEL CPU WITH 45 INSTRUCTIONS

* DECIMAL AND BINARY ARITHMETIC MODES

* 10.8 S INSTRUCTION CYCLE

* ADDITION OF TWO 8 DIGIT NUMBERS IN 850 MICROSECONDS

* NESTING OF SUBROUTINES UP TO 3 LEVELS

* INSTRUCTION SET INCLUDES CONDITIONAL BRANCHING, JUMP TO SUBROUTINE, AND INDIRECT FETCHING

* ERASABLE AND REPROGRAMMABLE PROMS

* SYNCHRONOUS OPERATION WITH MEMORIES

* DIRECT COMPATIBILITY WITH FULL LINE OF LEE LOGIC MODULES

* DIRECTLY DRIVES UP TO:
  4K BY 8 PROM
  1280 BY 4 RAM
  576 I/O LINES

* MEMORY CAPACITY EXPANDABLE THROUGH BANK SWITCHING

* SINGLE POWER SUPPLY

* EXTENSIVE USE OF METAL-OXIDE SEMICONDUCTOR CIRCUITRY

* MINIMUM SYSTEM: CPU CARD, PROM CARD AND ONE I/O CARD WITH POWER SUPPLY AND RACK

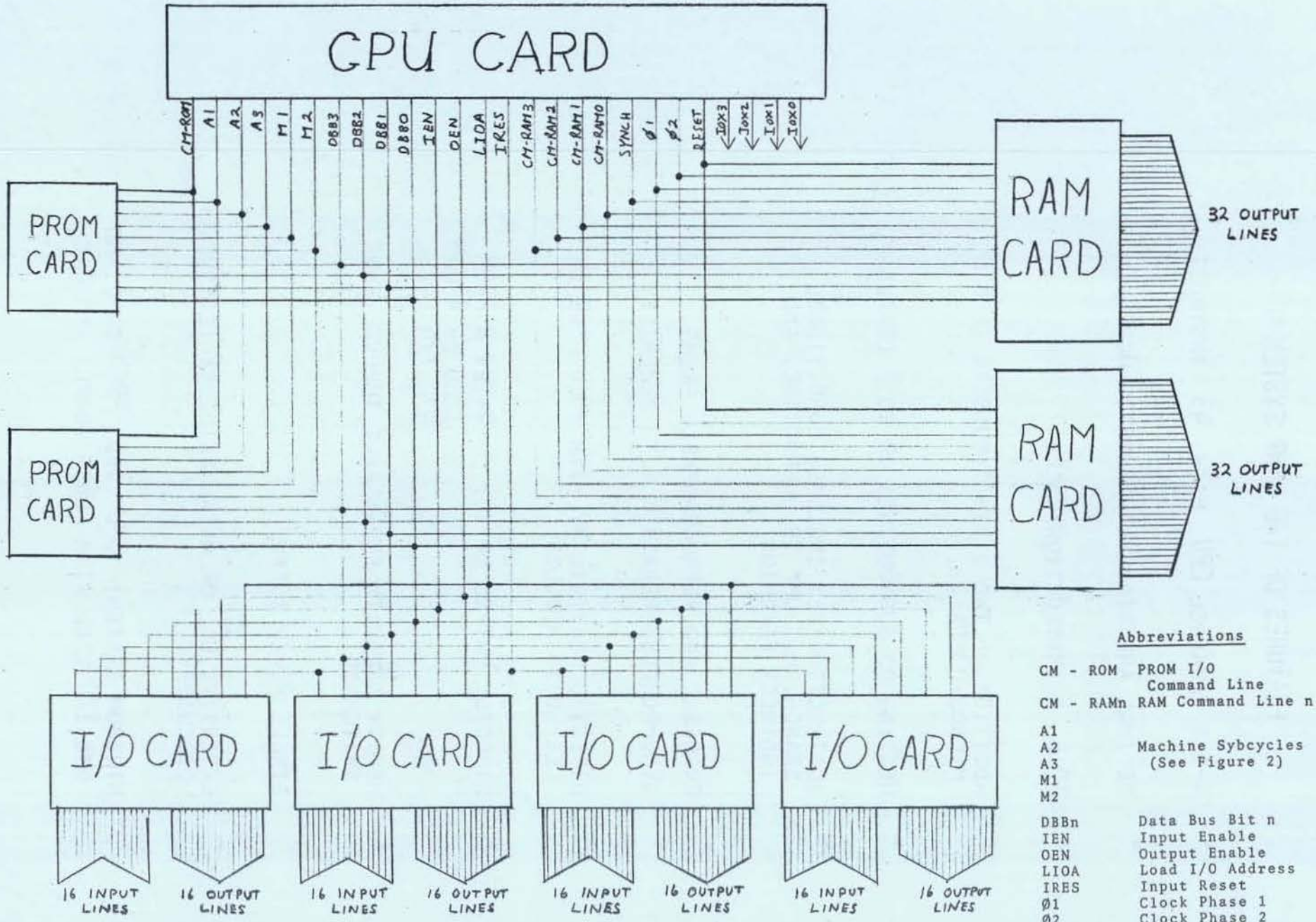


Figure 1
System Interconnection
(Maximum System without I/O Expansion Shown)

Abbreviations

CM - ROM	PROM I/O Command Line
CM - RAMn	RAM Command Line n
A1, A2, A3, M1, M2	Machine Sybcycles (See Figure 2)
DBBn	Data Bus Bit n
IEN	Input Enable
OEN	Output Enable
LIOA	Load I/O Address
IRES	Input Reset
Ø1	Clock Phase 1
Ø2	Clock Phase 2
Synch	CPU Synch Signal
Reset	CPU Reset Line
IOXn	I/O Expand Line n

THE SS-4 SYSTEM

GENERAL DESCRIPTION

Each SS-4 circuit constitutes a basic standard building block which allows the design of many different types of systems which can be fabricated using the same parts. (The only custom part is the PROM chip which will store a microprogram defined by the user.)

The SS-4 micro computer set consists of the following 4 cards:

CPU - A Central Processor Unit

PROM - A Programmable Read Only Memory

RAM - A Random Access Memory

I/O - An Input/Output card

The CPU contains the control unit and the arithmetic unit of a general purpose microprogrammable computer. The PROM stores microprograms and data tables, the RAM stores intermediate results, and the I/O card is used to interface with I/O lines.....

.....THE CARD ELEMENTS

PROM - The PROM is a 2048 Bit electrically programmable and erasable PROM providing custom microprogramming capability for the SS-4 micro computer set. Each chip is organized as 256 x 8 bit words which can be used for storing programs or data tables.

RAM - The RAM performs two functions. As a RAM it stores 320 bits per chip (8 chips per card) arranged as 4 registers of twenty 4-bit characters each. As a vehicle of communication with peripheral devices each chip is provided with 4 output lines and associated control logic to perform output operations.

I/O CARD - The I/O card has 16 input lines and 16 output lines at High-Threshold Logic (HTL) levels for direct compatibility with Lee Logic peripheral circuitry, including signal converters, triac drivers, stepper motor drivers, etc.; TTL I/O also available.

CPU - The CPU card is designed to work in conjunction with the other cards of the SS-4 micro computer set to form a completely self-contained system. The CPU communicates with the other members of the set through a four line data bus and with the peripheral devices through the RAM output ports and the I/O card. The CPU card contains 5 command control lines; four of which are used to control the RAM chips (each line can control up to 4 RAM chips for a total system capacity of 16 RAM's) and one which is used to control a bank of up to 16 PROM chips (2 PROM cards).

BASIC SYSTEM OPERATION

THE SS-4 USES A 10.8 MICROSECOND INSTRUCTION CYCLE. THE CPU GENERATES A SYNCHRONIZING SIGNAL (SYNC), INDICATING THE START OF AN INSTRUCTION CYCLE, AND SENDS IT TO THE PROM'S, RAM'S AND I/O CARDS.

Basic instruction execution requires 8 or 16 cycles of a 750 KHz clock. In a typical sequence, the CPU sends 12 bits of address (in three 4 bit bytes on the data bus) to the PROM's in the first three cycles (A_1, A_2, A_3). This address selects 1 out of 16 chips and 1 out of 256 8-bit words in that chip. The selected PROM chip sends back 8 bits of instruction (OPR, OPA) to the CPU in the next two cycles (M_1, M_2). This instruction is sent over the 4 line data bus in two 4-bit bytes. The instruction is then interpreted and executed in the final three cycles (X_1, X_2, X_3). (See Figure 2)

When an I/O instruction is received from the PROM, data is transferred between the CPU and four of the I/O lines during X_2 time.

A set of four RAM chips is controlled by one of four command control lines from the CPU. The address of a RAM chip, register and character is stored in two index registers in the CPU and is transferred to the RAM during X_2, X_3 time when an SRC instruction is executed. When the RAM output instruction is received by the CPU, the content of the CPU accumulator is transferred to the four RAM output lines.

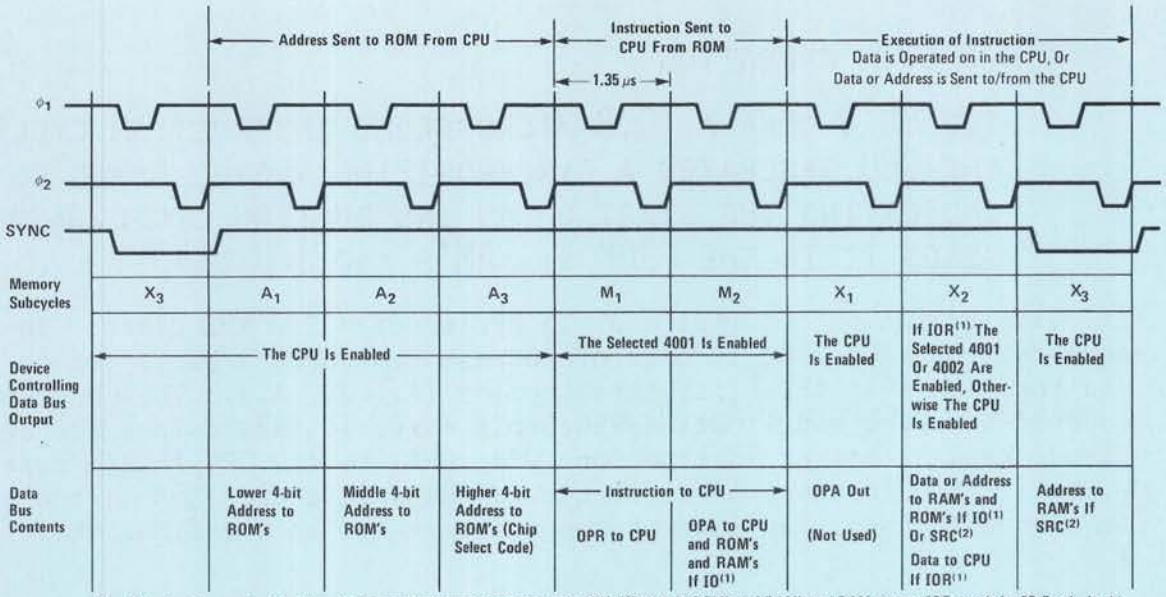
The CPU, and RAM's can be controlled by an external RESET line. While RESET is activated the contents of the registers and flip-flops are cleared. After RESET, the CPU will start from address 0 and CM-RAM_0 is selected.

THE SS-4 CAN HAVE UP TO 4K x 8 BIT PROM WORDS, 1280 x 4 BIT RAM CHARACTERS AND 576 I/O LINES, WITHOUT REQUIRING SPECIAL INTERFACE LOGIC.

BASIC SYSTEM TIMING

For the correct operation of the system two non-overlapping clock phases - $\emptyset_1$, $\emptyset_2$ are supplied by the CPU to PROM, and RAM. The CPU also generates a SYNC signal every 8 clock periods and sends it to the PROM and RAM. The SYNC signal marks the beginning of each instruction cycle. The RAM chip then generates internal timing using SYNC and $\emptyset_1$, $\emptyset_2$. The CPU also supplies necessary timing to PROM.

Figure 2 shows how a basic instruction cycle is subdivided and what the activity is on the data bus during each clock period. Each data bus output buffer has three possible states: "1", "0" and floating. At a given time, only 1 output buffer is allowed to drive a data line, therefore all the other buffers must be in a floating condition. However, more than 1 input buffer per data line can receive data at the same time.



(1) IO instructions control the flow of information between accumulator in CPU, I/O lines in ROM's and RAM's and RAM storage. IOR stands for IO Read. In this case the CPU will receive data from RAM storage locations or I/O input lines of 4001's.

(2) The SRC instruction designates the chip number and address for a following IO instruction.

Figure 2. Basic Instruction Cycle

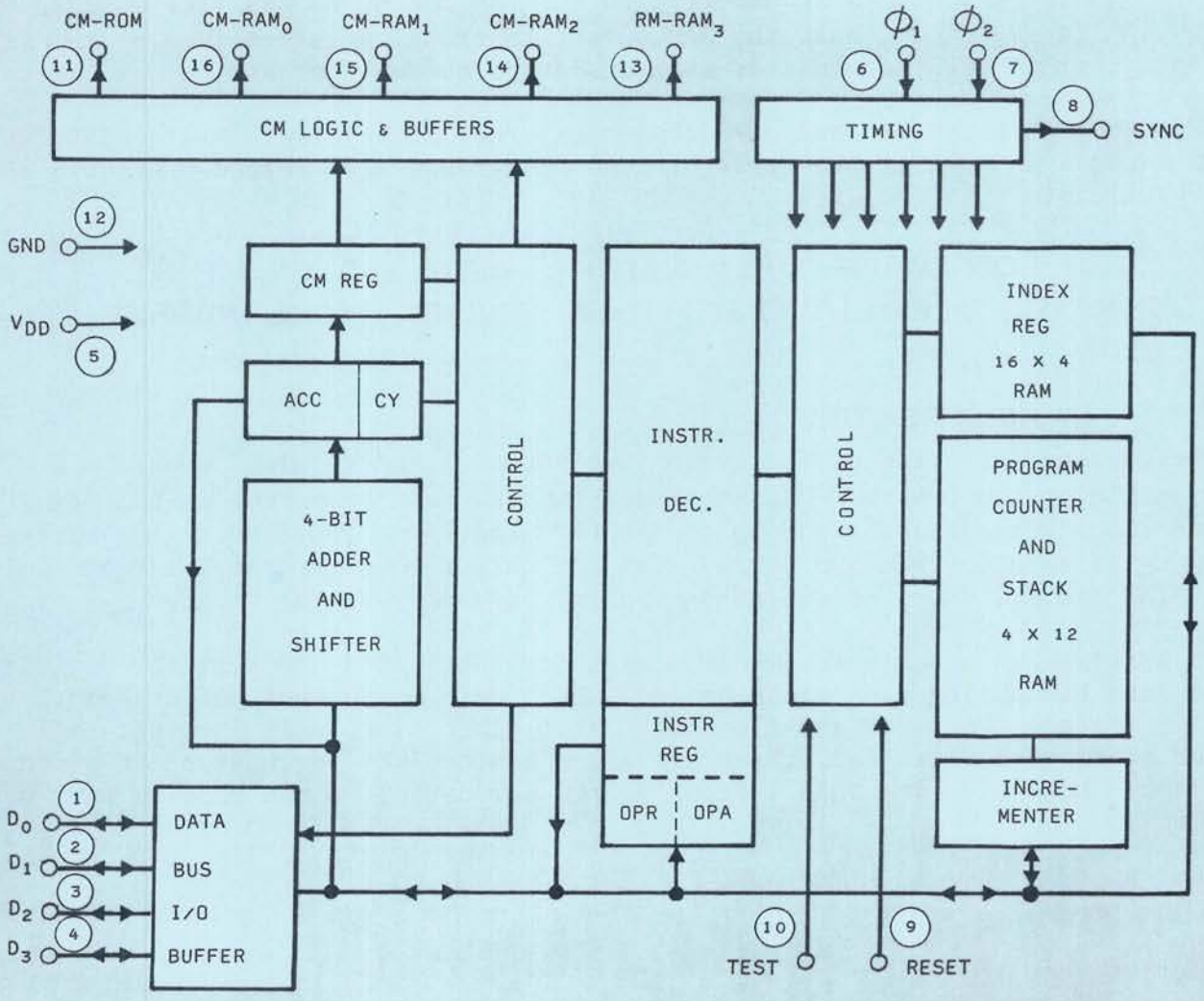


Figure 3. CPU Block Diagram

4 BIT CENTRAL PROCESSOR UNIT (CPU)

DESCRIPTION

The CPU shown in Figure 3 contains the following functional blocks:

Address register (program counter and stack organized as 4 words of 12 bits each) and address incrementer.

Index register (64 bits organized as 16 words of 4 bits each.

4-bit adder.

Instruction register (8 bits wide), decoder and control.

Peripheral circuitry.

The functional blocks communicate internally through a 4-line bus and are shown in Figure 3. The function and composition of each block is as follows:

ADDRESS REGISTER (PROGRAM COUNTER & STACK) & ADDRESS INCREMENTER

The address register is a dynamic RAM cell array of 4 x 12 bits. It contains one level used to store the effective address (program counter) and 3 levels used as a stack for subroutine calls. The stack address is provided by the effective address counter and by the refresh counter, and it is multiplexed to the decoder.

The address when read is stored in an address buffer and is demultiplexed to the internal bus during A_1, A_2, and A_3 in three 4-bit slices (see Figure 2 for basic instruction cycle). The address is incremented by a 4-bit carry look-ahead circuit (address incrementer) following the outputting of each 4-bit address slice. The incremented address is transferred back to the address buffer and finally written back into the address register.

INDEX REGISTER

The index register is a dynamic RAM cell array of 16 x 4 bits and has two modes of operation. In one mode of operation the index register provides 16 directly addressable storage locations for intermediate computation and control. In the second mode, the index register provides 8 pairs of addressable storage locations for addressing RAM and I/O as well as for storing data fetched from PROM.

The X address is provided by the internal bus and by the refresh counter and is multiplexed to the X decoder.

The read content is transferred to the internal bus through a multiplexer. Writing into the register is accomplished by transferring the content of the internal bus into a temporary register and then to the index register.

4-BIT ADDER

The 4-bit adder is the ripple-through carry type. One term of the addition comes from the "ADD" register which communicates with the internal bus on one side and can transfer data or data-not to the adder. The other term of the addition comes from the accumulator and carry flip-flop. Both data and data-not can be transferred. The output of the adder is transferred to the accumulator and carry FF. The accumulator is provided with a shifter to implement rotate right and rotate left instructions. The accumulator also communicates with the command control register, ROM's, the condition flip-flop and the internal bus. The command control register holds a 3-bit code used for CM-RAM line switching. The ROM's perform a code conversion for DAA (decimal adjust accumulator) and KBP (keyboard process) instructions. The ROM's also communicate with the internal bus. The condition logic senses ADD = 0 and ACC = 0 conditions, the state of the carry FF, and the state of an external signal (TEST) to implement JCN (jump on condition) and ISZ (increment index register skip if zero) instructions.

INSTRUCTION REGISTER DECODER AND CONTROL

The instruction register (consisting of the OPR Register and the OPA Register each 4 bits wide) is loaded with the contents of the internal bus (at M_1 and M_2 time in the instruction cycle) through a multiplexer and holds the instruction fetched from PROM. The instructions are decoded in the instruction decoder and appropriately gated with timing signals to provide the control signals for the various functional blocks. A double cycle FF is set from any one of the 5 double-length instructions. Double-length instructions are instructions that need two system cycles (16 clock cycles) for their execution. A condition FF controls JCN and ISZ instructions and is set by the condition logic.

PERIPHERAL CIRCUITRY

This includes:

The data bus input-output buffers communicating between data pads and internal bus.

The clock and timing generator.

1 ROM command control (CM-ROM) and the
4 RAM command control (CM-RAM) output buffers.

Reset flip-flop.

I/O instruction control logic.

I/O bank selection logic.

During reset, all RAM's and static FF's are cleared, and the data bus is set to "0". After reset, program control will start from "0" step and $CM\text{-}RAM_0$ is selected. To completely clear all registers and RAM locations the reset signal must be applied for at least 8 full instruction cycles (64 clock cycles) to allow the index register refresh counter to scan all locations in memory.

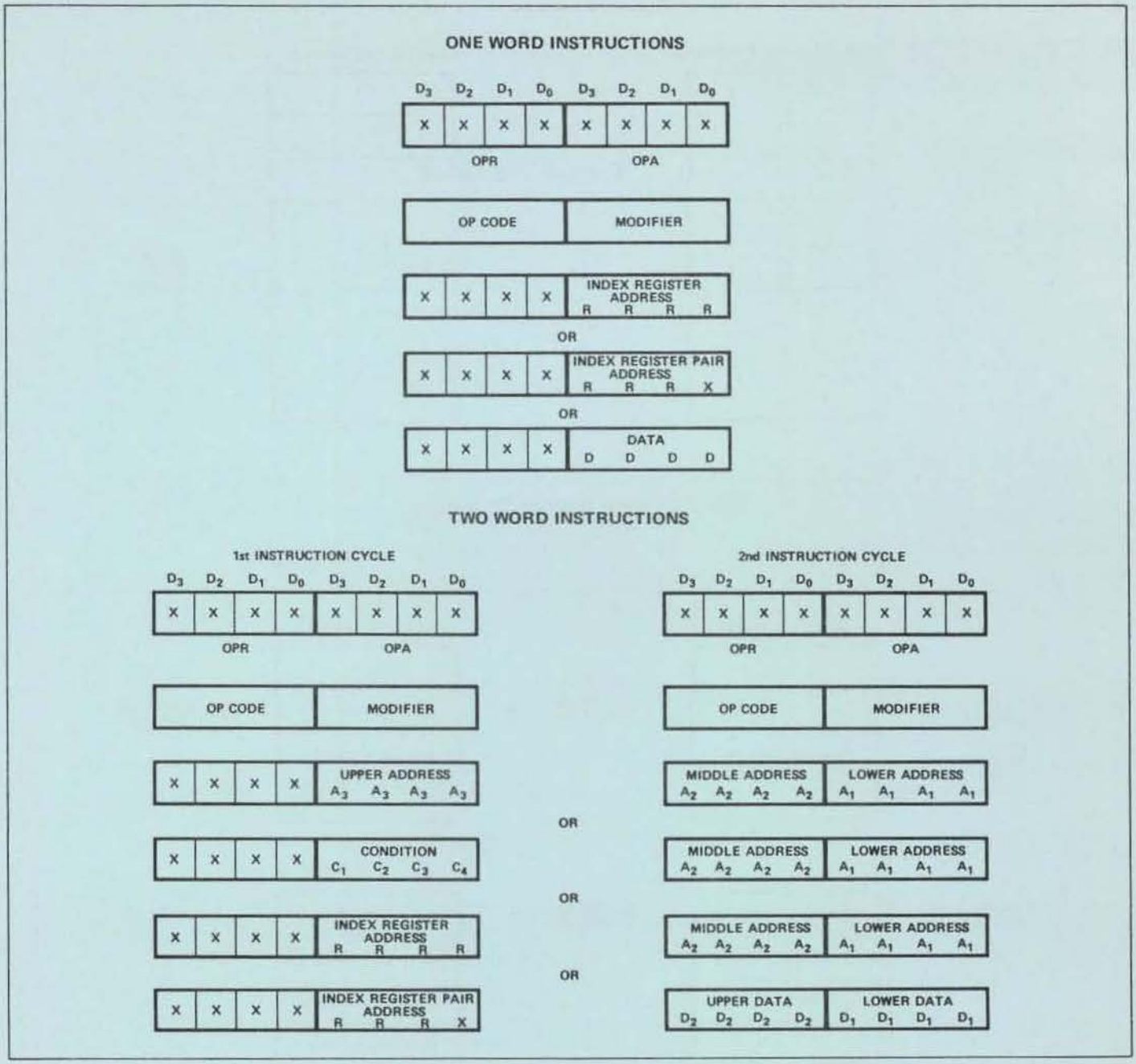


Table I - Machine Instruction Format

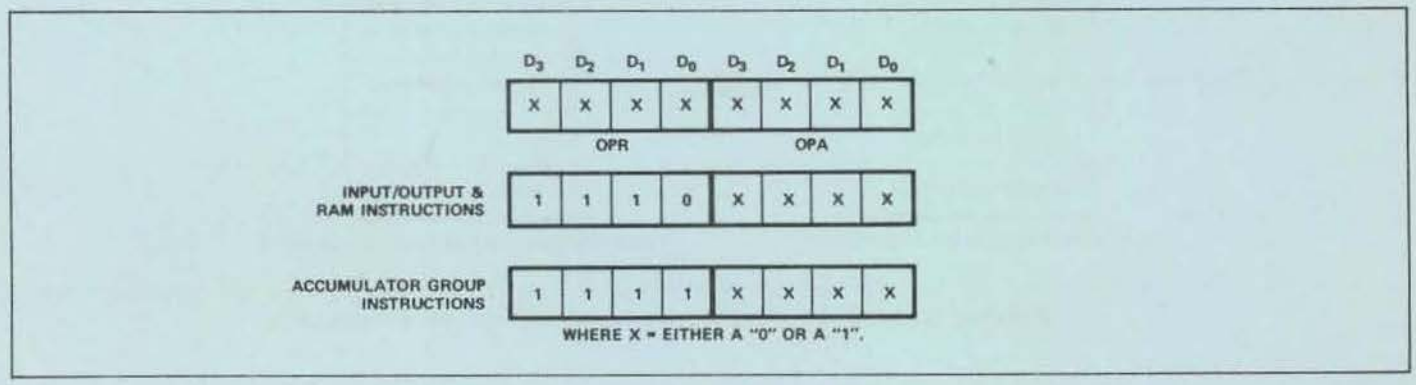


Table II - I/O and Accumulator Group Instruction Formats

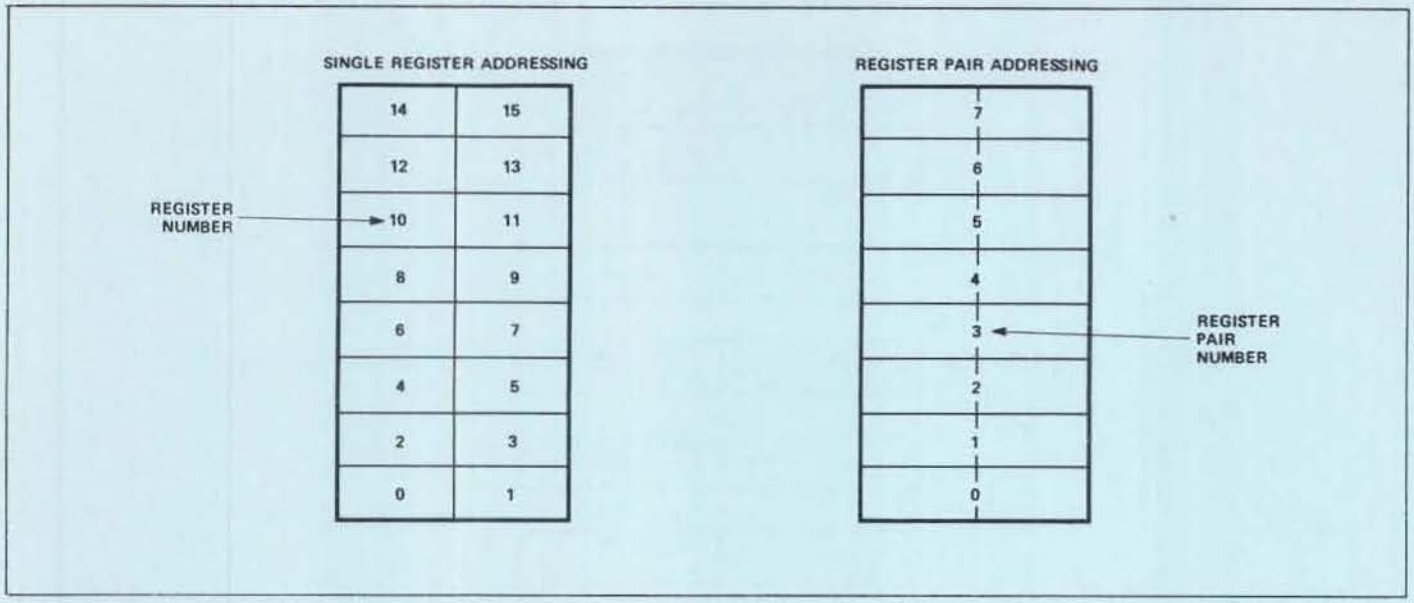
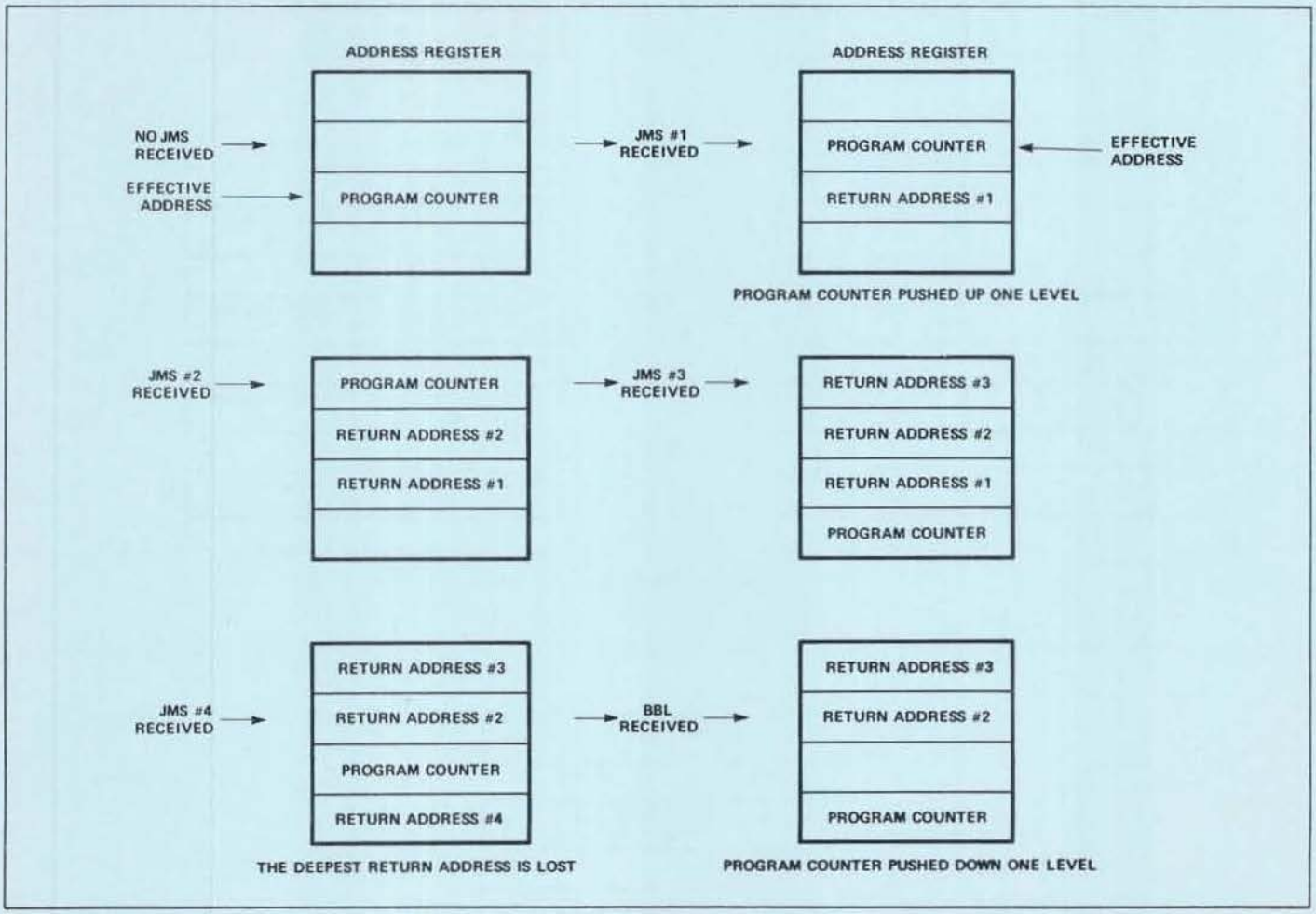


Table III - Index Register Organization



Operation of the Address Register on a Jump to Subroutine Instruction

INSTRUCTION REPERTOIRE

THE INSTRUCTION REPERTOIRE OF THE CPU CONSISTS OF:

- 16 MACHINE INSTRUCTIONS (5 OF WHICH ARE DOUBLE LENGTH)
- 14 ACCUMULATOR GROUP INSTRUCTIONS
- 15 INPUT/OUTPUT AND RAM INSTRUCTIONS

THE INSTRUCTION SET AND ITS FORMAT WILL BE BRIEFLY DESCRIBED IN THE NEXT SECTION, AND IN DETAIL FURTHER ON.

CPU INSTRUCTION SET FORMAT, INDEX REGISTER ORGANIZATION AND OPERATION OF THE ADDRESS REGISTER

INSTRUCTION SET FORMAT

MACHINE INSTRUCTIONS:

* 1-word instructions - 8 bits long and requiring 8 clock periods (1 instruction cycle)

* 2-word instructions - 16 bits long and requiring 16 clock periods (2 instruction cycles) for execution

A 1-word instruction occupies one location in PROM (each location can hold one 8-bit word) and a 2-word instruction occupies two successive locations in PROM. Each instruction word is divided into two 4-bit fields. The upper 4 bits is called the OPR and contains the operation code. The lower 4 bits is called the OPA and contains the modifier. For a single word machine instruction the operation code (OPR) contains the code of the operation that is to be performed (add, subtract, load, etc.). The modifier (OPA) contains one of 5 thing:

1) A register address.
2) A register pair address.
3) An upper portion of another PROM address.
4) 4 bits of data.
5) A condition for jumping.

For a 2-word machine instruction, the 1st word is the same as a 1-word instruction. The 2nd word contains either the middle portion (in OPR) and lower portion (in OPA) of another PROM address or 8 bits of data (the upper 4 bits in OPR and the lower 4 bits in OPA).

The upper 4 bits of instruction (OPR) will always be fetched before the lower 4 bits of instruction (OPA) during M_1 and M_2 times respectively. Table I illustrates the contents of each 4-bit field in the machine instructions.

INPUT/OUTPUT & RAM INSTRUCTIONS AND ACCUMULATOR GROUP INSTRUCTIONS

In these instructions (which are all single word) the OPR contains a 4-bit code which identifies either the I/O instruction or the accumulator group instruction and the OPA contains a 4-bit code which identifies the operation to be performed.

INDEX REGISTER ORGANIZATION

The index register can be addressed in two modes:

By specifying 1 out of 16 possible locations with an OPA code of the form RRRR. (see Table III)

By specifying 1 out of 8 pairs with an OPA code of the form RRRX. (see Table III)

When the index register is used as a pair register, the even number register (RRR0) is used as the location of the middle address or the upper data fetched from the PROM, the odd number register (RRR1) is used as the location of the lower address or the lower data fetched from the PROM.

OPERATION OF THE ADDRESS REGISTER (PROGRAM COUNTER AND STACK)

The address register contains four 12-bit registers: one register is used as the program counter and stores the effective address; the other 3 registers make up the push down stack.

Initially, any one of the 4 registers can be used as the program counter to store the effective address. In a typical sequence the program counter is incremented by 1 after the last address is sent out. This new address then becomes the effective address. If a JMS (Jump to Subroutine) instruction is received by the CPU, the program control is transferred to the address called out in the JMS instruction. This address is stored in the register just above the old program counter which now saves the address of the next instruction to be executed following the JMS. This return address becomes the effective address following the BBL instruction at the end of the subroutine.

In summary, then, a JMS instruction pushes the program counter down one level and a BBL instruction pushes the program counter up one level. Since there are 3 registers in the push down stack, 3 return addresses may be saved. If a fourth JMS occurs, the deepest return address (the first one stored) is lost.

Since the JMS instruction is a 2-word instruction the old effective address must be incremented by 2 to correctly give the address of the next instruction to be executed after the return from JMS.

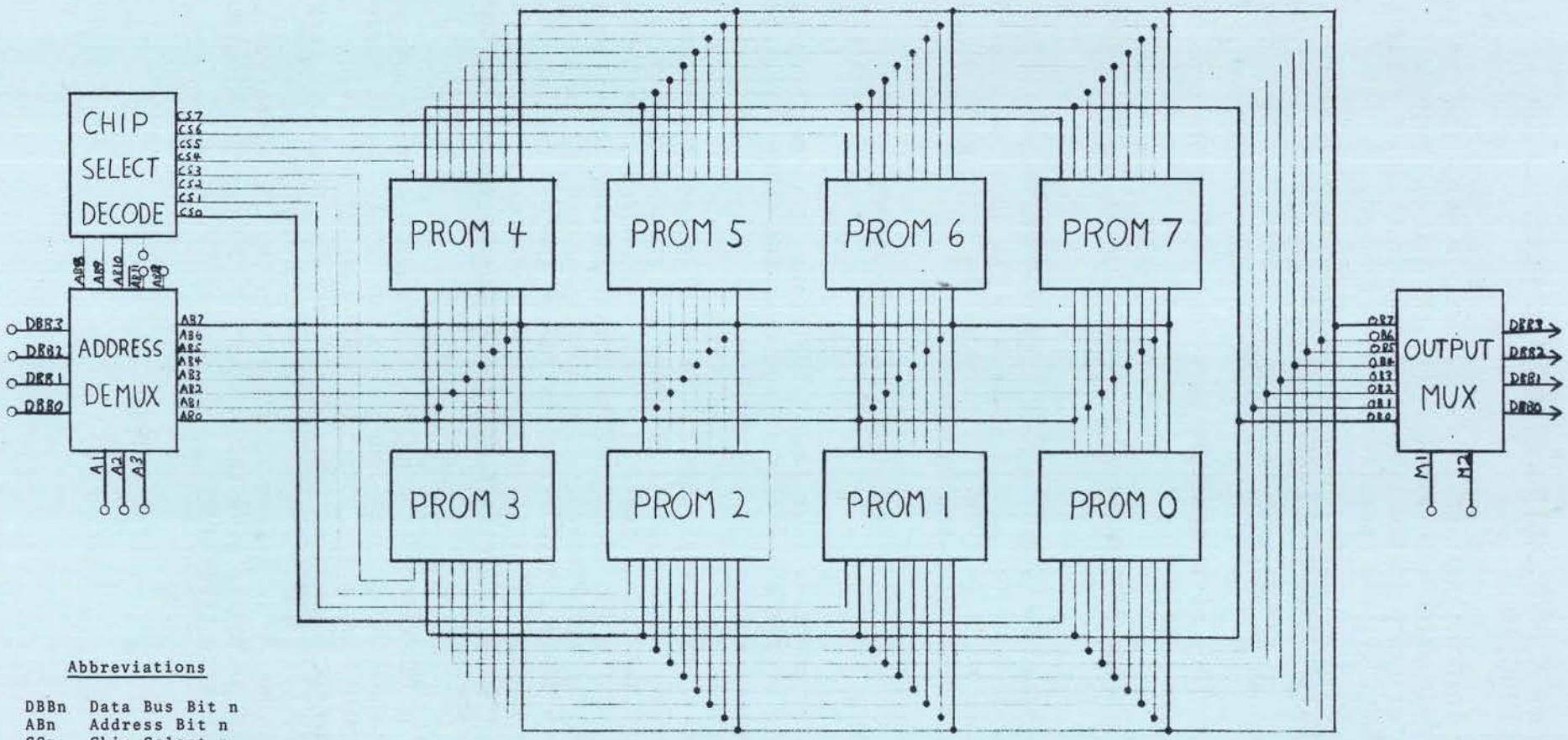


Figure 4 PROM CARD

Abbreviations

DBBn	Data Bus Bit n
ABn	Address Bit n
CSn	Chip Select n
OBn	Output Bit n
A1	Machine Subcycles (See Figure 2)
A2	
A3	
M1	
M2	

1024 x 8 BIT PROM CARD

The PROM card stores the program for the system. In addition, tables of constants can be kept in PROM for use by the program.

The PROM card is configured as shown in Figure 4. It may contain up to eight 256 x 8 bit PROM chips.

During A_1, A_2, and A_3, the PROM card accepts and decodes an address from the CPU. The chip select logic enables one of the eight chips on the card, and then during M_1 and M_2 the demultiplexer puts the data from the PROM onto the data bus.

640 x 4 BIT RAM CARD WITH OUTPUT PORTS

The RAM card contains up to 8 RAM chips. Each RAM chip performs two functions. As a RAM it stores 320 bits arranged in 4 registers of twenty 4-bit characters each (16 main memory characters and 4 status characters). As a vehicle of communication with peripheral devices, it is provided with 4 output lines and associated control logic to perform output operations. (The block diagram is shown in Figure 5)

In the RAM mode, the operation is as follows: when the CPU receives an SRC instruction it will send out the content of the designated index register during X_2 and X_3 and will activate one CM-RAM line at X_2 for the previously selected RAM bank.

The status character locations (0 through 3) are selected by the OPA portions of the RAM instructions.

The twenty 4-bit characters for each RAM register are arranged as follows:

1. 16 characters addressable by the SRC instruction: four 16-character registers constitute the "main" memory.

2. 4 characters addressable by the OPA of the I/O instruction: four 4-character registers constitute the "status character" memory.

Bank switching is accomplished by the CPU after receiving a "DCL" (designate command line) instruction. Prior to execution of the DCL instruction the desired CM-RAM code has been stored in the accumulator (for example, through an LDM instruction). During DCL the CM-RAM code is transferred from the accumulator to the CM-RAM register. The RAM bank is then selected starting with the next instruction.

Two separate X decoders switch between main and status character memories.

When an I/O or RAM instruction is received by the CPU, the CPU will activate one CM-RAM line during M_2, in time for the RAM to receive the OPA (2nd part of the instruction), which will specify the I/O or RAM operation to be performed.

The I/O and RAM operations are divided into Read operations (IOR) and Write operations (IOW). The state of D_3 will determine if the operation is a read or write. $D_3 = 0$ for IOW.

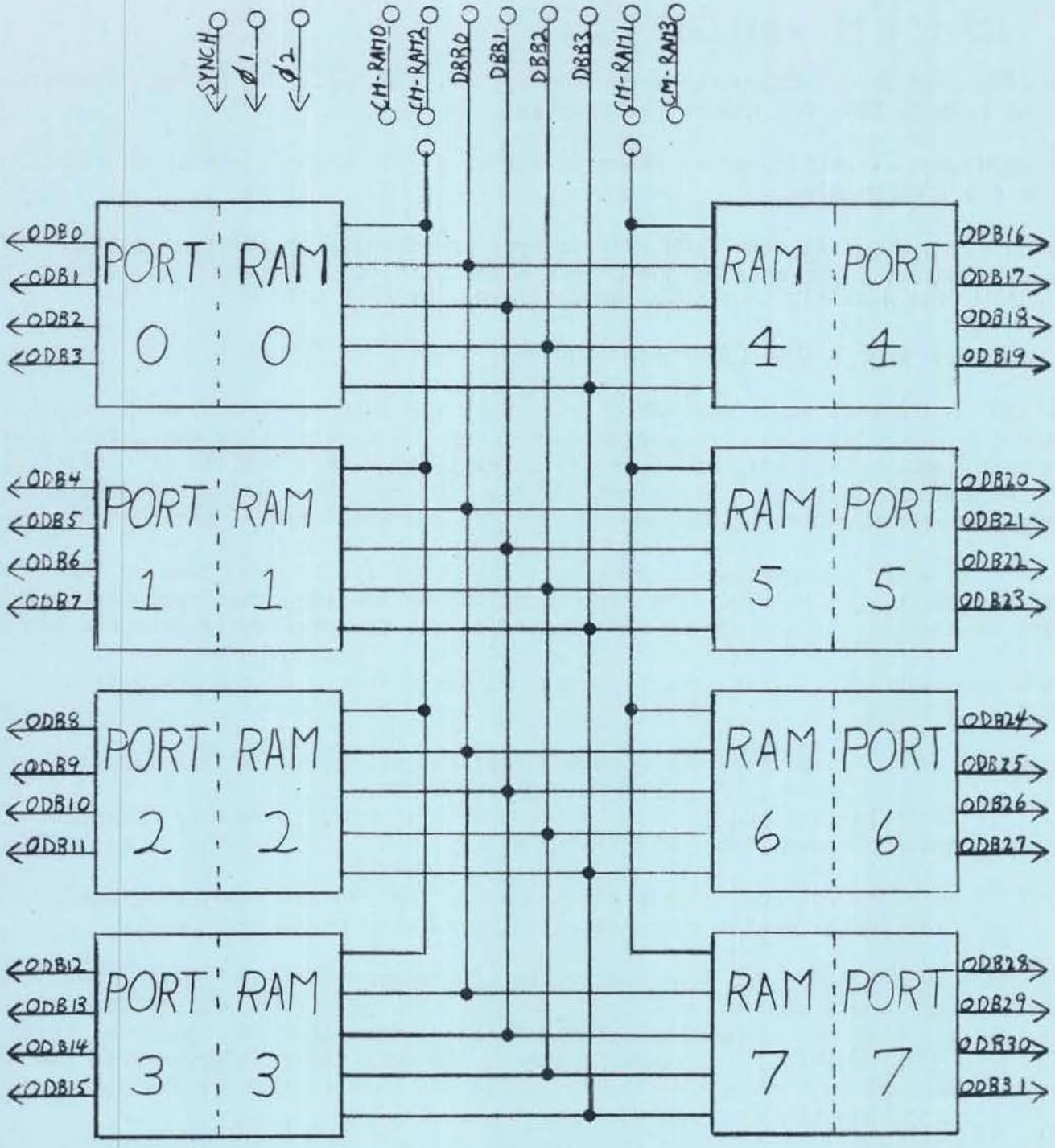


Figure 5 RAM Card Block Diagram

Abbreviations

DBBn	Data Bus Bit n
ODBn	Output Data Bit n
Synch	CPU Synch Signal
Ø1	Clock Phase 1
Ø2	Clock Phase 2
CM - RAMn	RAM Command Line n

In the I/O mode of operation, the selected RAM chip (by SRC), after receiving the OPA of an I/O instruction (CM-RAM activated at M_2), will decode the instruction.

If the instruction is WMP, the data present on the data bus during X will set the output flip-flops associated with the I/O pins. That information will be available until next WMP for the same address.

In addition to the RAM chips, the RAM card includes drivers for all the RAM outputs.

16 INPUT/16 OUTPUT I/O CARD

The I/O card ties the system to external devices, both inputs and outputs. Each card has 16 latching inputs and 16 latching outputs, organized in groups of four inputs and four outputs for each I/O address.

When the CPU sends out a LOAD command, during X_2, indicating execution of an SRC, the I/O card accepts an address from the CPU. This address is then decoded. If the address is on the card, one set of four inputs and four outputs is selected for subsequent I/O operations.

When the CPU receives an input or output instruction, it sends an input enable or output enable command, which causes the I/O card to transfer data between the bus and the selected port during X_2.

When the I/O card receives a reset command, which the CPU sends after an input instruction, the selected input latches are reset.

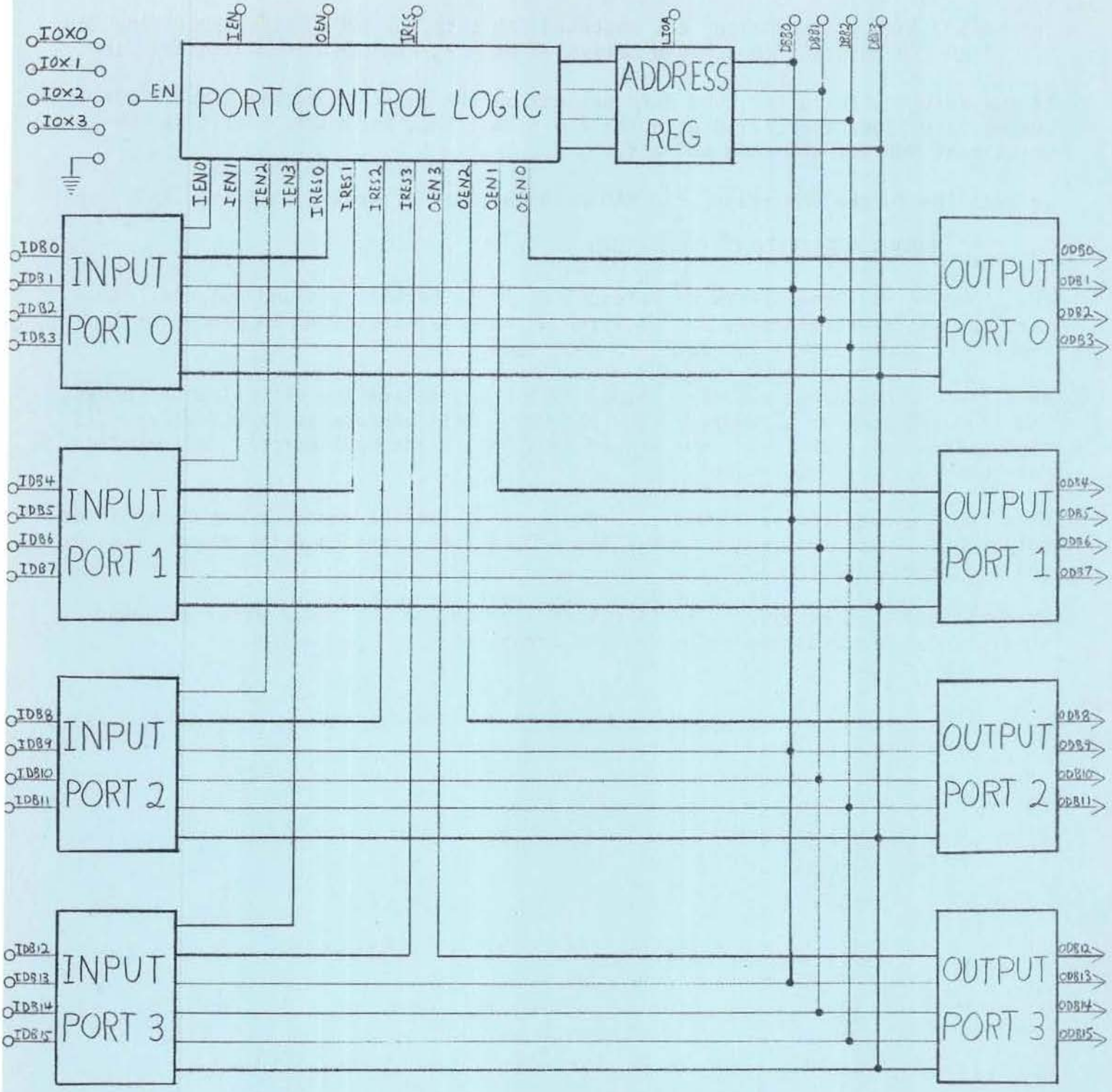


Figure 6 I/O Card Block Diagram

Abbreviations

IDBn	Input Data Bit n
ODBn	Output Data Bit n
IOXn	I/O Expand Line n
IEN	Input Enable
OEN	Output Enable
IRES	Input Reset
DBBn	Data Bus Bit n
LIOA	Load I/O Address
EN	Card Enable

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