VOICE PROCESSOR MANUAL
(Preliminary)

NOTE

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the Installation Guide, may cause interference to radio communications. The equipment has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, which users may be required to correct at their own expense.

Specifications Subject to Change.

Preliminary Edition (March 1985) A-09-00912-00-A

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LIST OF FIGURES

LIST OF TABLES

RELATED DOCUMENTATION

The documentation described below provides additional information related to the contents of this manual. For a complete list of Convergent Technologies documentation, see the "Guide to Technical Documentation" in the Executive Manual or similar command-line interpreter manual for your operating system.

CONVERGENT TECHNOLOGIES DOCUMENTATION

Introductory
- Installation Guide (NGEN)
- Operator's Guide (NGEN)

Software
- Debugger Manual
- Voice/Data Services Manual

Hardware
- Processor Manuals
- Diagnostics Manual

The Installation Guide describes the procedure for unpacking, assembling, cabling, and powering up a workstation.

The Operator's Guide is a link between the operator, the workstation, and the workstation's documentation. The Operator's Guide describes the operator controls and the use of the floppy disk drives, as well as how to use software release notices.

The Debugger Manual describes the Debugger, which is designed for use at the symbolic instruction level. It can be used in debugging C, FORTRAN, Pascal, and assembly-language programs. (COBOL and BASIC, in contrast, are more conveniently debugged using special facilities described in their respective manuals.)

The Voice/Data Services Manual describes the Voice/Data Services, which consists of a device driver that provides a request and procedural interface between the software and hardware components in the Voice Processor Module.

The Processor Manuals describe the respective Processor Modules. Each manual (a two-volume set) covers one processor model and details the architecture and theory of operation of the printed circuit boards, external interfaces, and memory expansion, as well as abridged X-Bus specifications.

The Diagnostics Manual describes the tests used to verify proper operation of the modules in your workstation. Individual tests for individual modules are covered along with bootstrap procedures and customization programs.

VENDOR DOCUMENTATION

The boards that make up the Telephone Manager Module are heavily dependent upon programmable large-scale integration (LSI) circuitry to perform their functions. Since hardware functions and software interfaces of the LSI circuitry are only summarized in this manual, users can find additional information in the following manufacturers' literature:

Intel Corporation. Intel Component Data Catalog. Santa Clara, Cal.: Intel Corporation, 1980.

Intel Corporation. Intel Microprocessor and Peripheral Handbook. Santa Clara, Cal.: Intel Corporation, 1980.

Mitel Corporation. Mitel Semiconductor. Microelectronic Products for Telecommunications. Issue 3. Kanata, Ontario, Canada: Mitel, 1982. 9161-952-001-NA.

MT8804A 8 X 4 Analog Switch Array. April 1983.

MT8870A Integrated DTMF Receiver. Preliminary. April 1983.

Mostek Corporation. Telecommunications Products Data Book. Carrollton, Tex.: Mostek, 1981.

MK5089 (N/P/J) Integrated Tone Dialer. Preliminary.

National Semiconductor Corporation. Linear Databook. Santa Clara: National Semiconductor, 1982.

LM3915 Dot/Bar Display Driver.

TP3040/
TP3040A PCM Monolithic Filter.

Oki Semiconductor, Inc. Santa Clara.

MSM5204RS 8 Bit Analog-to-Digital Converter. Preliminary. October 1982.

MSM5218RS ADPCM Speech Analysis/Synthesis IC. Preliminary. October 1982.

CONVENTIONS

NUMBERS

Numbers used in this manual are written in decimal unless suffixed with "h" for hexadecimal. For example, 10h = 16 and 0FFh = 255.

SIGNAL NAMES

Signal names used in this manual are suffixed with plus (+) and minus (-) to distinguish active-high from active-low, respectively. An example of a RD (Read) signal is as follows:

Signal Name	Logical State	Voltage Level
RD-	0 (active)	Low
	1 (inactive)	High
RD+	0 (inactive)	Low
	1 (active)	High

In addition, signals can be asserted (activated) or deasserted (deactivated) as follows:

Signal Name	Logical State	Voltage Level
RD-	0 (asserted)	Low
	1 (deasserted)	High
RD+	0 (deasserted)	Low
	1 (asserted)	High

X-BUS

In this manual, the "X-Bus master" denotes any device or module capable of controlling the X-Bus command lines.

An explanation of the system capabilities and the system bus, designated as the X-Bus, is found in the Processor Manual for the system.

DOWNSTREAM/UPSTREAM

In this manual, "downstream" signifies any X-Bus module that is to the right of the referenced module. For example, downstream from the Voice Processor Module signifies any module to the right of it.

In addition, "upstream" signifies any module to the left of the referenced module.

SYSTEM CONTROLLER

The system controller consists of the leftmost X-Bus module that provides bus clocks, DMA mode arbitration, and power-up signals.

1 OVERVIEW

INTRODUCTION TO THE MANUAL

This manual serves as a reference for the engineer who tests or services the Voice Processor Module electronics, or who writes or modifies applicable software for use with the workstation. This manual does not, however, support modifications to existing hardware. The manual is divided into the following sections:

- Overview
- Architecture
- Theory of Operation
- External Interfaces
- Troubleshooting Quick Reference Card

This section, "Overview," describes the capabilities of the Voice Processor Module, as well as its major components.

The second section, "Architecture," covers the Voice Processor Module in terms of its applicable software interfaces to hardware components. Applicable command and status registers for the module are defined. In addition, the X-Bus identification scheme and X-Bus DMA mode 3 operation are summarized.

Section 3, "Theory of Operation," details the component-level circuit descriptions of the Voice Processor Module. In addition, an interconnect wire list is provided.

The last section, "External Interfaces," provides a collection of both hardware and software interface information for cable requirements.

In addition, Appendix A contains the Voice Processor Module specifications, Appendix B contains the Modem board specifications, and Appendix C contains the schematic diagram, wire list and other drawings.

A troubleshooting quick reference card points to sections within the manual for troubleshooting the Voice Processor Module.

A glossary of technical terms is located at the end of the manual.

INTRODUCTION TO THE MODULE

GENERAL

The Voice Processor Module, shown in Figure 1-1, provides a fully integrated voice and data interface between a workstation and the switched telephone network or commonly used private automatic branch exchange (PABX) system (supporting Tip and Ring connection). When used with a digital PABX system, all signals and transmission between the Voice Processor Module and the PABX occur via analog techniques.

The Voice Processor Module is an X-Bus module containing two printed-circuit boards. The first board contains a Bell 212A-compatible modem.

The second board contains the following:

- modular jacks for two telephone line interfaces (FCC, part 68, registered)
- additional modular jack (FCC, part 68, registered) that allows connection to any standard voice unit (telephone set)
- analog crosspoint switch allowing any device to connect to either line under software control
- Dual-Tone Multifrequency (DTMF) touch-tone auto-dialer
- DTMF touch-tone decoder that permits numeric data entry via remote voice unit touch pad
- call progress tone detector
- voice amplifier

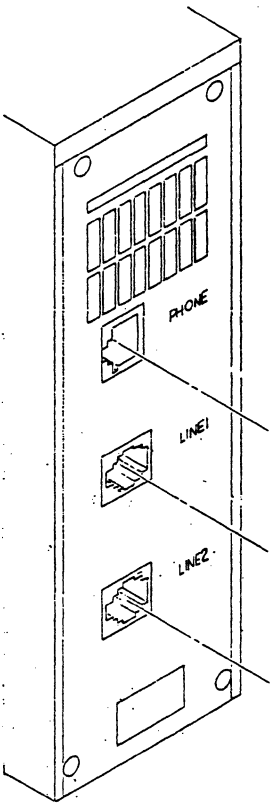

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Figure 1-1. Voice Processor Module.

- Adaptive Pulse Code Modulation (ADPCM) CODEC (Coder/Decoder) for support of digitized voice communications at speeds far less than the normal 64Kbps

- 8051 microprocessor to control all module activities

MODEM BOARD

The Modem board can be used in both originate and answer modes and supports full-duplex transmission (asynchronous mode) over ordinary two-wire telephone circuits. It is compatible with the Western Electric 212A series at 1200 baud and the Bell 103/113 series at 300 baud. Dibit encoded phase-shift keying (PSK) is used for high-speed operation, and frequency-shift keying (FSK) is used for low-speed operation.

CONTROLLER BOARD

Modular Jacks

Three modular jacks are provided at the rear panel of the Voice Processor Module, under a removable cover. The jack labeled "Phone" connects to a standard telephone or speakerphone (voice unit). The jacks labeled "Line 1" and "Line 2" connect to the central office of a telephone company or PABX switch line. When the workstation is powered down or a power failure exists, a normally closed relay connects the "Line 1" jack to the "Phone" jack, permitting manual operation of the voice unit.

Analog Crosspoint Switch Array

All devices are connected to an analog crosspoint switch array, which allows, under software control, either telephone line to be connected to the voice unit, the modem, the CODEC, or the DTMF tone decoder.

DTMF Tone Generator

The DTMF tone generator generates all 16 DTMF digits (Ø through 9, *, #, and ØAh through ØDh) under software control and is normally used in auto-dial applications. The DTMF tone generator can also be programmed to transmit various key sequences to activate specific features of PABXs.

The DTMF tone generator can also generate single tones.

DTMF Tone Receiver

The DTMF tone receiver decodes incoming DTMF tones as digits for applications software. For example, numeric information can be input via the telephone touch pad to programs supporting voice mail or voice response capabilities.

Call Progress Tone Detector

The call progress tone detector consists of analog circuitry that, in conjunction with software, detects busy tone, dial tone, reorder tone, and answer (ringback) tone.

Voice Amplifier

The voice amplifier amplifies voice signals along the voice unit-to-central office/PABX connection through the analog crosspoint switch array.

CODEC

Using the CODEC and ADPCM (Adaptive Pulse Code Modulation) technique, the Voice Processor Module encodes or digitizes analog (voice) signals for storage and decodes or converts digitized voice information back from storage into an analog form for transmission. The CODEC operates at either 6-kHz or 8-kHz sampling rates, generating data at either 24Kbps or 32Kbps, respectively. Therefore, high quality voice can be transmitted at the 8-kHz sampling rate, or the 6-kHz rate can be used for applications where storage and transmission costs are more important than voice quality.

The digital output of the CODEC can be stored on the local system hard disk or can be transmitted via the 1.8Mbps RS-422 cluster communications line to a disk at the master workstation.

Microprocessor

All devices within the Voice Processor Module are controlled by an 8051 microprocessor.

SOFTWARE SUPPORT

Software support includes CT-MAIL, CT-Net, and "Operator" software, which is specially tailored for the Voice Processor Module as follows:

- Telephone directory management, which has the ability to add, delete, modify, and look up entries in a disk-based telephone directory, and automatically establish calls using the information in the directory. Menus provide assistance in accessing special functions used by PABXs.

- Voice digitization, which allows the operator to use the CODEC to record and play back calls or messages. This capability enhances CT-MAIL, where it is used for voice annotation of written documents, as well as the inclusion of voice attachments to textual mail.

- Telephone answering, which allows an unattended system to automatically answer the telephone and perform a variety of user-selectable operations ranging from simple message playback/recording to input of numeric data from a telephone touch-tone pad.

MAJOR COMPONENTS

All functions of the Voice Processor Module are controlled by a dedicated 8051 microprocessor, which includes 4K bytes of on-chip ROM and 128 bytes of on-chip RAM, a serial port used to interface to the modem, and an 8-bit parallel port used for several input signals from the modem and X-Bus interface.

Most devices, however, are accessed as external RAM locations to the 8051 microprocessor. These include a stacker/destacker used to pass 4-bit data to/from the CODEC, the DTMF tone detector, the DTMF tone generator, crosspoint switch control, and a series of address and data latches used for communicating with the X-Bus as a DMA mode 3 master. (See the "DMA Transfer Mode 3" subsection in section 2, "Architecture.")

A socket for a 2732 EPROM provides instructions for the 8031 ROM-less microprocessor rather than the 8751 EPROM version.

The CODEC consists of an Oki 5218 ADPCM speech analyzer/synthesizer. A data rate of 32Kbps is standard (8 kHz ADPCM sampling frequency), while 24Kbps (6 kHz) is available as a programmable option (for applications where voice quality is of less importance than storage costs).

The major components of the Voice Processor Module include the following:

- the enclosure, which houses the module components
- the motherboard, which lies against the bottom of the enclosure
- the Modem board, which is mounted vertically along the left side of the enclosure
- the Controller board, which is mounted vertically along the right side of the enclosure
- one dc/dc converter that plugs into the motherboard, supplying +5 Vdc and -5Vdc

Major components located on the Controller board include the following:

- 8051 microprocessor
- 2732 EPROM
- MSM5204 8-bit analog-to-digital converter

- MSM5218 ADPCM speech analysis/synthesis IC
- MK5089 integrated tone dialer
- MT8870 integrated DTMF receiver
- MT8804 8X4 analog switch array
- LM3915 dot/bar display driver
- TP3040/TP3040A PCM monolithic filter

Printed circuit assemblies showing component locations for the Controller board and Motherboard are provided in Appendix C. In addition, the Modem board specifications are provided in Appendix B.

2 ARCHITECTURE

INTRODUCTION

This section provides information for the systems programmer who needs to understand the Voice Processor Module hardware at a functional block level. It includes information for programming the large-scale integration (LSI) devices within the Voice Processor Module.

A functional block diagram of the Voice Processor Module is shown in Figure 2-1. Each block is described in this section in relation to the programmable LSI device or devices performing the applicable function in the workstation. Each subsection describes the nature of the function and how it is implemented. In addition, specific status and command registers are examined.

The following subjects are detailed:

- X-Bus interface
- changing module base I/O address
- X-Bus mode 3 DMA transfer interface
- 8051 microprocessor internal ports
- 8051 microprocessor external devices
- 8051 microprocessor firmware
- buffer management
- error reporting
- call progress tone detection
- pause detection
- interrupt status
- external RAM address summary

X-BUS INTERFACE

Upon either a power-up or manual reset, the bootstrap ROM program in the Processor Module assigns a unique base I/O address to each module that is physically attached to the X-Bus. The operating system also has the ability to change the base I/O address of any module at any time. A description for changing the module base address through the operating system is included in the "Changing Module Base I/O Address" subsection, in the "Bootstrap ROM and Debugger" section of the Processor Manual for the system.

The Processor Module uses the base I/O address to initialize, identify, or interrupt the Voice Processor Module. These are described in the applicable subsections.

MODULE IDENTIFICATION

A power-up, manual reset, or a specific I/O operation within the Processor Module, resets all X-Bus modules, except the Processor Module. Only the module immediately to the right of the Processor Module is enabled. This module identifies itself by placing a type/state word on the data bus when port Ø is read by the Processor Module.

The Processor Module writes to port Ø a base I/O address. Writing to port Ø also causes the module to reenable the X-Bus connection to the next module and to ignore subsequent reads and writes to and from port Ø. This allows the Processor Module to repeat the process for each module, beginning at the module adjacent to the Processor Module and repeating the process for each module to the right.

A ready timeout, signaled by a nonmaskable interrupt (NMI) when accessing port Ø, signifies that no additional modules are available.

To Be Supplied

Figure 2-1. Voice Processor Module Functional Block Diagram.

IMPLEMENTATION

The module identification scheme is implemented by hardware as follows:

- All modules on the X-Bus are assigned an input signal line (XPIN) and are required to generate an output signal line (XPOUT). The input signal will always enter a module on the module's left side, and the output signal will always exit the module on the module's right side.

- During power up, all modules reset an internal flip-flop to drive XPOUT low.

- The XPIN line of the module closest to the Processor Module is controlled by the Processor Module; when XPIN is low, the I/O register clears.

- When a module's XPIN is high and its XPOUT is low, the base I/O address of the module is zero.

- The Processor Module reads port Ø to identify the peripheral (for example, the Voice Processor Module). This write also enables the XPOUT line in the module, which allows the next module on the right to undergo the same operation.

The Processor Module is always referred to as module Ø, and the first module to the right of the Processor Module is referred to as module 1, and so on. The bootstrap ROM always writes this module number to the low-order byte of port Ø when it performs the identification polling sequence. The bootstrap ROM also builds an array of the module type/state words returned by each module and stores this table in memory for the system.

CHANGING MODULE BASE I/O ADDRESS

As described in the "X-Bus Interface" subsection, during power-up or manual reset, the Processor Module assigns a base I/O address to each module connected to it on the X-Bus. The first module to the right of the Processor Module is assigned a base I/O address of ØlXXh, the second module Ø2XXh, and so on.

The base I/O address of any module except the Processor Module can be programmed to be any number from ØlXXh to FFXXh (in lXXh address increments). Two facilities are available for changing the base I/O address of the modules: the panel Debugger routine in the Processor Module's bootstrap ROM program and the software Debugger.

Using either Debugger, each module on the X-Bus must first be reset to clear the addresses previously set by the Processor Module. Also, each module on the X-Bus must be assigned a new base I/O address number.

See the Processor Manual or Debugger Manual for the system for instructions using the panel Debugger or software Debugger routine, respectively.

DMA TRANSFER MODE 3

DIRECT MEMORY ACCESS

Direct memory access (DMA) transfer operations are bus operations that access data differently than the conventional master/slave I/O or memory operations. DMA transfer operations allow other bus masters besides the system controller to independently access the buses and support data transfers without direct program control. Bus masters can retain the bus for more than one cycle at a time. The X-Bus has four DMA transfer modes, mode Ø through mode 3. The Voice Processor Module uses mode 3; therefore, only mode 3 will be described. For information about modes Ø through 2, see the Processor Manual for the system.

MODE 3

During a mode 3 transfer, the system controller only provides the arbitration for bus acquisition signals. The requesting module, which must be a master, generates the control and addresses. Mode 3 is only valid on DMA channels 1 through 3 of the system controller; however, more than one mode 3 master may share the same data transfer channel. The Voice Processor uses DMA channel 1.

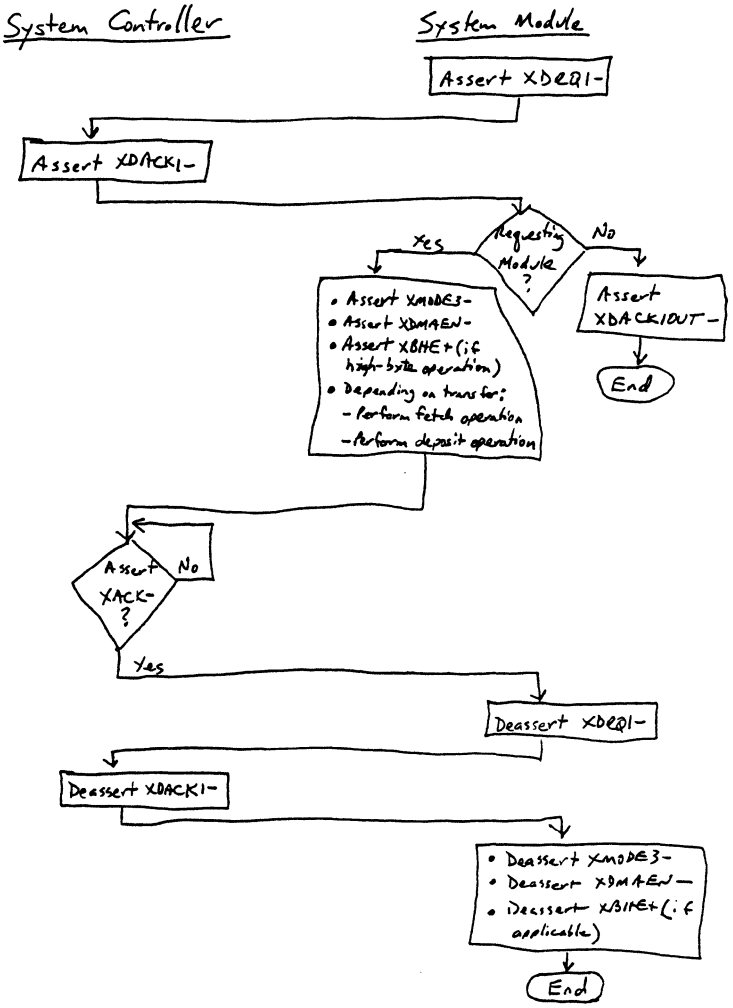


Figure 2-2. Mode 3 DMA Transfer Flow Diagram.

The data requests and the acknowledge is daisy chained through priority arbitration logic. When the system controller asserts XDACK- (X-Bus DMA Acknowledge), each mode 3 module will determine if it has a valid request. If the applicable mode 3 module has asserted XDRQ- (X-Bus DMA Request), then it controls the channel and inhibits XDACK- (X-Bus DMA Acknowledge) for the next X-Bus mode 3 master module, downstream. If no request is pending for the applicable module, the mode 3 master module asserts XDACK- for the next module on the X-Bus. A flow diagram for a mode 3 DMA transfer is shown in Figure 1-2.

For a detailed description of X-Bus specifications and DMA transfer mode information, see the technical specification X-Bus: NGEN High Speed Inter-Module Bus or the Processor Manual for the system.

X-BUS INTERFACE REGISTERS

The X-Bus interface consists of five registers, which appear at the following 8051 microprocessor external RAM locations:

Address (h)	Function	Access
20	Data register	R/W
40	High Byte Address register	W
50	Middle Byte Address register	W
60	Low Byte Address register	W
70	Control register	W

Each of these is described below.

DATA REGISTER (ADDRESS 20h)

This read/write register holds a byte of data during read or write operations. The 8051 microprocessor reads this register to receive data from memory via the X-Bus and writes to this register to transmit data to memory via the X-Bus.

Note that the local data byte is identical to the X-Bus data byte. The register acts only as an interface.

The Voice Processor Module performs byte transfers, and therefore chooses whether to transmit or receive data on the high byte or the low byte of the data bus. Before each transfer, the 8051 microprocessor latches in three separate bytes of addresses as described for the following registers.

HIGH BYTE ADDRESS REGISTER (ADDRESS 40h)

Since the X-Bus consists of a 24-bit address bus, the 8051 microprocessor, which contains an 8-bit data bus, latches each of the three X-Bus address bytes separately.

This register generates the high-order address byte (that is, XADR10- through XADR17-) during write operations. Data bit functions are as follows:

Data Bit	Function
0	X-Bus address 10h
1	X-Bus address 11h
2	X-Bus address 12h
3	X-Bus address 13h
4	X-Bus address 14h
5	X-Bus address 15h
6	X-Bus address 16h
7	X-Bus address 17h

MIDDLE BYTE ADDRESS REGISTER (ADDRESS 50h)

Since the X-Bus consists of a 24-bit address bus, the 8051 microprocessor, which contains an 8-bit data bus, latches each of the three X-Bus address bytes separately.

This register generates the middle address byte (that is, XADR8- through XADRF-) during write operations. Data bit functions are as follows:

Data Bit	Function
0	X-Bus address 8h
1	X-Bus address 9h
2	X-Bus address 0Ah
3	X-Bus address 0Bh
4	X-Bus address 0Ch
5	X-Bus address 0Dh
6	X-Bus address 0Eh
7	X-Bus address 0Fh

LOW BYTE ADDRESS REGISTER (ADDRESS 60h)

Since the X-Bus consists of a 24-bit address bus, the 8051 microprocessor, which contains an 8-bit data bus, latches each of the three X-Bus address bytes separately.

This register generates the low-order address byte during write operations. Data bit functions are as follows:

Data Bit	Function
0	X-Bus address 0
1	X-Bus address 1
2	X-Bus address 2
3	X-Bus address 3
4	X-Bus address 4
5	X-Bus address 5
6	X-Bus address 6
7	X-Bus address 7

CONTROL REGISTER (ADDRESS 70h)

The data-bit functions of this write-only register are as follows:

Data Bit	Function
0	X-Bus Memory Write: When set, a mode 3 master DMA request (that is, XDRQ1-) is issued over the X-Bus to the system controller; one DMA byte is written.
1	X-Bus Memory Read: When set, a mode 3 master DMA request (that is, XDRQ1-) is issued over the X-Bus to the system controller; one DMA byte is read.
2	X-Bus High Byte Disable: When reset, disables the high data byte.
3	X-Bus Interrupt Request: When set, an X-Bus level 4 interrupt request (that is, XINTR4-) is issued to the system controller.

The DMA request (that is, XDRQ1-) deasserts upon receipt of XACK- (Transfer Acknowledge). The interrupt request (that is, XINTR4-) deasserts when the Processor Module reads any I/O port within the Voice Processor Module's assigned range. When the Processor Module writes to any I/O port within the Voice Processor Module's assigned range, a Module Attention request is generated to the 8051 microprocessor. (That is, bit 4 of internal port 1 of the 8051 microprocessor is asserted.) The interrupt is cleared whenever the 8051 microprocessor resets a Clear Module Attention bit (that is, bit 6 of internal port 1 of the 8051 microprocessor). Bit 6 must be set after the clear to allow the next attention request.

See the "8051 Microprocessor Internal Ports" subsection, below, for port information.

8Ø51 MICROPROCESSOR INTERNAL PORTS

Ports Ø and 2 of the 8Ø51 microprocessor are used for internal bus control, while ports 1 and 3 are used for control functions. Each of these ports is described below.

PORT Ø

Port Ø functions as follows:

Port Bit	Function
Ø	Address/data line Ø
1	Address/data line 1
2	Address/data line 2
3	Address/data line 3
4	Address/data line 4
5	Address/data line 5
6	Address/data line 6
7	Address/data line 7

PORT 1

Port 1 is an 8-bit quasi-bidirectional I/O port. Data bit functions for port 1, which can sink/source one TTL load, are as follows:

Port Bit	Function
Ø	Hold 1: When reset, this output causes telephone line 1 to go on hold
1	Hold 2: When reset, this output causes telephone line 2 to go on hold
2	X-Bus Memory Busy: Active-low input that signifies that the X-Bus memory is busy; in other words, the Voice Processor Module has generated a DMA request
3	X-Bus Interrupt Pending: Input that signifies that an X-Bus interrupt has been generated to the system controller
4	Module Attention Pending: Input that signifies an interrupt from the Processor Module
5	Voice Unit Off-Hook: Active-low input signifying that the voice unit (telephone set) is off-hook
6	Clear Module Attention: Active-low output that clears the X-Bus master attention bit (that is, bit 4); this bit must then be set to allow the next Module Attention Pending input
7	Modem Reset: Active-low output that resets the modem

PORT 2

Port 2 functions as follows:

Port Bit	Function
Ø	Address line 8h
1	Address line 9h
2	Address line ØAh
3	Address line ØBh
4 - 7	Unused

PORT 3

Data bit functions of port 3 are as follows:

Port Bit	Function
Ø	Receive data from modem
1	Transmit data to modem
2	CODEC interrupt input signifying that a byte of voice information has been encoded by the CODEC and is ready to be transferred to memory, or a byte of voice information has been transferred from memory to the CODEC for decoding
3	FSK carrier detect from 3ØØ-baud modem (used to control data call setup)
4	PSK carrier detect from 12ØØ-baud modem (used to control data call setup)
5	Set by firmware to adjust the gain for the call screening function of the answering machine; normally reset to zero
6	Write data to internal bus
7	Read data from internal bus

8051 MICROPROCESSOR EXTERNAL DEVICES

The following registers appear at the following 8051 microprocessor external RAM locations:

Address (h)*	Function	Access
00	Tone Detector register	R
10	CODEC stacker/ destacker	R/W
30	Loudness Level register	R
80 - 87	Analog crosspoint matrix control	W
90	DTMF Generator register	W
A0	Line Control register	W
B0	Modem Control register	W

*

TONE DETECTOR REGISTER (ADDRESS 00h)

Data bit functions of the read-only Tone Dectector register, which appears as external RAM location 00h, are as follows:

Data Bit	Function
0 - 3	Encoded DTMF Digit (see below)
4	Ring Detect 1: When set, ring detected for line 1
5	Ring Detect 2: When set, ring detected for line 2
6	Call Progress Tone Detected: When set, call progress tone detected
7	DTMF Digit Detected: When reset, signifies that a received pair-tone has been detected

DTMF Encoding

Data Bits

3	2	1	Ø	Digit
Ø	Ø	Ø	Ø	ØDh
Ø	Ø	Ø	1	1
Ø	Ø	1	Ø	2
Ø	Ø	1	1	3
Ø	1	Ø	Ø	4
Ø	1	Ø	1	5
Ø	1	1	Ø	6
Ø	1	1	1	7
1	Ø	Ø	Ø	8
1	Ø	Ø	1	9
1	Ø	1	Ø	Ø
1	Ø	1	1	*
1	1	Ø	Ø	#
1	1	Ø	1	ØAh
1	1	1	Ø	ØBh
1	1	1	1	ØCh

CODEC STACKER/DESTACKER (ADDRESS 10h)

The CODEC stacker/destacker appears as 8051 microprocessor external RAM location 10h (read/write) and is used to pass data to/from the CODEC in 4-bit increments. The stacker/destacker generates an interrupt to bit 2 of internal port 3 of the 8051 microprocessor for every character (that is, every byte). In other words, the interrupt is generated when a byte of voice information has been encoded by the CODEC and is ready to be transferred to memory, or a byte of voice information has been transferred from memory to the CODEC for decoding.

LOUDNESS LEVEL REGISTER (ADDRESS 30h)

The read-only Loudness Level register, which appears as external RAM location 30h, contains the encoded loudness level reaching the CODEC. There are only five discrete values that can be generated. From lowest to highest volume, they are as follows:

Digit (h)	Volume
01	Silence level
00	Volume detected
02	Next highest volume
06	Next highest volume
0E	Highest volume

CROSSPOINT SWITCH (ADDRESSES 80h THROUGH 87h)

An analog crosspoint switch array occupies external RAM locations 80h through 87h, corresponding to line numbers Ø through 7, respectively. Each data bit of the low-order nibble corresponds to a junctor to which the line is connected when the bit is set. Line numbers are assigned as follows:

Line No.	Address (h)	Device
Ø	80	Voice unit interface (no extra attenuation)
1	81	Modem
2	82	DTMF generator
3	83	DTMF receiver/call progress tone detector
4	84	Voice amplifier
5	85	CODEC encoder
6	86	CODEC decoder
7	87	Voice unit interface (path adding attenuation)

Junctor numbers are assigned to the following devices:

Junctor No.	Device
Ø	Telephone Line 1
1	Telephone Line 2
2	Indirect connection to analog ground
3	Not connected (used for indirect connections)

Each line can be connected to any of the junctors via the data bits. In other words, each of four data bits (DØ+ through D3+) corresponds to each of four junctors (JØ+ through J3+).

For example, when all data bits are low, no junctors are connected to the addressed line. When all data bits are high, all junctors are connected to the addressed line. If D2+ and D3+ are high while DØ+ and D1+ are low, the addressed line connects to junctors 2 and 3. These examples are shown as follows:

Input Data				Junctors Connected			
D3+	D2+	D1+	DØ+	J3+	J2+	J1+	JØ+
Ø	Ø	Ø	Ø	-	-	-	-
1	1	Ø	Ø	*	*	-	-
1	1	1	1	*	*	*	*

*Signifies connection between junctor and addressed line

-Indicates no connection.

For instance, when line Ø (address 8Øh) connects to junctor 1 (data nibble equals ØØ1Ø binary), the voice unit interface is connected to telephone line 2.

DTMF GENERATOR REGISTER (ADDRESS 90h)

The write-only DTMF Generator register appears as external RAM location 90h. Data bits Ø through 3 disable rows 1 through 4, and data bits 4 through 7 disable columns 1 through 4, respectively. The 16 possible DTMF digits are generated as follows:

Data Byte Value (h)	Digit	Row	Column
D7	Ø	4	2
EE	1	1	1
DE	2	1	2
BE	3	1	3
ED	4	2	1
DD	5	2	2
BD	6	2	3
EB	7	3	1
DB	8	3	2
BB	9	3	3
E7	*	4	1
B7	#	4	3
7E	A	1	4
7D	B	2	4
7B	C	3	4
77	D	4	4
FF	None		

Digits A through D do not appear on a standard telephone set.

LINE CONTROL REGISTER (AØh)

The write-only Line Control register appears as external RAM location AØh. Data bit functions are as follows:

Data Bit	Function
Ø	Off Hook 1: When set, signifies line 1 is off hook
1	Off Hook 2: When set, signifies line 2 is off hook
2	Crossover Relay 1 Enable (see below)
3	Originate/Answer: When set, places modem in originate mode; when reset, places modem in answer mode
4	Encode to CODEC: Set to encode voice; reset to decode voice
5	Halt to CODEC: Set to halt CODEC; reset to run CODEC
6	CODEC Sampling Rate Select: Set to sample at 8 kHz; reset to sample at 6 kHz
7	Crossover Relay 2 Enable (see below)

Crossover Relay 2	Crossover Relay 7	Connection
Ø	Ø	Voice unit across line 1 (power-up default)
Ø	1	Voice unit across line 2 (used to save power)
1	Ø	Voice unit not across either line
1	1	Voice unit across line 2 (not used)

MODEM CONTROL REGISTER (ADDRESS BØh)

The write-only Modem Control register appears as external RAM location BØh. Data bit functions are as follows:

Data Bit	Function
Ø	Mode Select: When set, selects V.22 mode; when reset, selects 1Ø3/212 mode
1	Digital Loopback: When set, sets the local modem to digital loopback mode so that data transmitted from a remote modem to the local modem will be looped back to the remote modem for diagnostics
2	Remote Digital Loopback: When set, causes the local modem to perform a command sequence to place a remote modem in digital loopback for diagnostics
3	Remote Digital Loopback Enable: When set, enables the local modem to be placed into digital loopback from a remote modem for diagnostics
4	Analog Loopback: When set, sets an internal modem to analog loopback mode so that data transmitted from the 8Ø51 microprocessor to the modem will be transmitted back to the 8Ø51 microprocessor for diagnostics
5	Unused
6	Enable PSK: When set, enables modem for PSK at 12ØØ baud
7	Enable FSK: When set, enables modem for FSK at 3ØØ baud

8Ø51 MICROPROCESSOR FIRMWARE

The 8Ø51 microprocessor firmware controls all operations of the Voice Processor Module through

commands that are fetched from the Processor Module main memory over the X-Bus. The root of all data structures used to control the Voice Processor Module is the Voice Processor Control Block (TMCB). The TMCB address is obtained from main memory locations 401 through 403 when the first Module Attention request is issued. The TMCB address is given in the form of a 24-bit absolute address, instead of a selector:offset pair. When fetching the TMCB address, the Voice Processor Module ensures that the device code of the Voice Processor Module (byte 400) is set to 32h, and that the signature word at offset 00 of the TMCB is set to 8459h as a validity check. The format of the TMCB is as follows:

Offset (h)	Contents
0, 1	Signature word (must be 8459h)
2	Firmware version
3	Command byte
4	Voice unit status
5	Crosspoint line (device) number
6	Crosspoint junctor number
7	Parameter byte 0
8	Parameter byte 1
9	Telephone line 1 status
A	Telephone line 2 status
B - 12	Dialer character list
13 - 16	DTMF generator character list
17 - 1E	DTMF Receiver data
1F - 26	Modem receive Character Queue Control Block (CQCB)
27 - 2E	Modem transmit CQCB
2F - 36	CODEC Character Queue Control Block

Offset (h)	Contents
37 - 38	CODEC status
39 - 3A	Modem line status
3B	Count call progress tone low
3C	Count call progress tone high
3D	Interrupt status
3E - 45	Map of crosspoint switch

COMMANDS

The Processor Module issues a command to the Voice Processor Module by writing a nonzero command byte to byte Ø of the TMCB and then issuing an I/O write to any location in the Voice Processor Module address space. The Voice Processor Module examines and executes the command, zeros the command byte, and raises a level 4 interrupt (that is XINTR4-) to the Processor Module. The commands performed by the Voice Processor Module are as follows:

Value (h)	Command
1	Crosspoint state (connect/ disconnect)
2	Off-hook
3	On-hook (hang up)
4	Unused
5	Hold
6	Start data transfer
7	Halt data transfer
8	Pulse dial
9	X-Bus DMA test
ØA	Ringthrough mode
ØB	Modem parameter change
ØC	Mimic voice unit pulse dialing
ØFF	No operation

The crosspoint line and junctor numbers, and the two parameter bytes, are obtained from bytes 5, 6, 7, and 8 of the TMCB, as appropriate to each command.

Command Notes

Each of the commands above is described in the following subsections. Parameter bytes Ø and 1 are also described.

Crosspoint State (Value 1). All devices (lines) are connected as commanded. The devices are placed into various stages of operation as follows:

Device	Parameter
Voice unit	None required
Modem	ParamØ (parity), Paraml (mode, test modes, originate/answer, line speed if originating, interrupt mode)
DTMF generator	ParamØ (length of time between digits), Paraml (length of time in 1Ø-millisecond intervals to generate digit)
DTMF receiver/ call progress tone detector	None required
Voice amplifier	None required
CODEC encoder	ParamØ (sampling rate)
CODEC decoder	ParamØ (sampling rate)
Voice unit attenuator	None required

Off-Hook, On-Hook, and Hold (Values 2, 3, and 5). In regard to off-hook, on-hook, and hold commands, junctor 1 equals line 1 and junctor 2 equals line 2.

Start Data Transfer (Value 6). When using the modem line (line 1), ParamØ equals Ø for both transmit and receive; ParamØ equals 1 for transmit only; and ParamØ equals 2 for receive only.

When using the DTMF receive and call progress tone detector line (line 3), ParamØ equals Ø for DTMR receive, and ParamØ equals ØFFh for call progress tone detector.

Halt Data Transfer (Value 7). When using the modem line (line 1), ParamØ equals Ø for both transmit and receive; ParamØ equals 1 for transmit only; and ParamØ equals 2 for receive only.

Pulse Dial (Value 8). If the junctor number is ØFFh during the pulse dial command, the pulse dial action will stop and the telephone line will be taken off hook.

X-Bus DMA Test (Value 9). ParamØ consists of the data to be used for the test. During the firmware test, the data is read and written back to the call progress tone detector low/high bytes in the TMCB. Note that two writes are performed to the TMCB to ensure both a low- and high-byte DMA access.

Ringthrough (Value ØAh). The junctor equals Ø for ringthrough off; equals 1 for ringthrough via line 1; and equals 2 for ringthrough via line 2.

Modem Parameter Change (Value ØBh). ParamØ is as follows: parity, interrupt mode.

Mimic Voice Unit Pulse Dialing (Value ØCh). When using junctor Ø, the mimic is off; when using junctor 1, the mimic is on for line 1; and when using junctor 2, the mimic is on for line 2.

Parameter Byte Ø (ParamØ)

This parameter byte is interpreted as follows:

Data Bit	Function
Ø - 2	Parity (see below)
3, 4	Unused
5, 6	Modem Data Notification (Interrupt) Mode (see below)
7	CODEC Sampling Rate Select: Set to sample at 8 kHz; reset to sample at 6 kHz

Parameter Bits

2	1	Ø	Parity
Ø	Ø	Ø	None
Ø	Ø	1	Zero
Ø	1	1	One
1	Ø	1	Even
1	1	1	Odd

Modem Data Notification Bits

6	5	Function
Ø	Ø	No special notification
Ø	1	Notification (interrupt) on XON, XOFF
1	Ø	Notification on each character
1	1	Unused

No parity implies eight data bits; all other parity settings imply seven data bits.

Note the following for paramØ during the Crosspoint Connection command: When the DTMF generator is the target during start of data transfer, ParamØ is the interdigit interval (that is, the time between digits where the unit is equal to 1Ø-millisecond periods).

An error (for example, overflow) notification will take place as usual no matter which mode is used. Both parity and modem data notification modes must be correct when changing either.

When the command is 'SDT CODEC Encode', bit 6 above is set to 1 to suppress the firmware silence detection.

Parameter Byte 1 (Paraml)

This parameter byte is interpreted as follows:

Data Bit	Function
Ø	Modem Mode: Set to use modes V.21/V.22; reset to use modes 103/212
1	Digital Loopback: When set, signifies digital loopback
2	Remote Digital Loopback: When set, signifies remote digital loopback
3	Remote Digital Loopback Enable: When set, enables remote digital loopback
4	Analog Loopback: When set, signifies analog loopback
5	Line Speed: Set to use 12ØØ baud; reset to use 3ØØ baud (line speed is only interpreted when originating a call)
6	Originate/Answer: When set, modem is in originate mode; when reset, modem is in answer mode
7	Unused

Note the following for Paraml when using the Crosspoint Connection command: When the DTMF generator is the target, Paraml is the digit length (that is, the duration of digits where the unit is equal to 1Ø-millisecond periods).

In addition, when connecting the call progress tone detector, Paraml equals ØFFh for the firmware to look only for the first occurrence of a mark (high) call progress signal. When the signal is detected, the Interrupt Status equals 4 (for call progress tone timing), the Count Call Progress Tone low-order byte in the TMCB equals Ø, and the Count Call Progress Tone high-order byte equals ØFFh.

TELEPHONE LINE STATES

A separate state byte is maintained in the TMCB for each telephone line. A level 4 interrupt (that is, XINTR4-) is issued to the Processor Module whenever the Voice Processor Module detects a change in state on either line. These state codes are interpreted as follows:

Value	Function
Ø	Idle (On Hook)
1	Ringing
2	Modem Not Ready (Data Call Connected)
3	Modem Ready FSK (1Ø3)
4	Modem Ready PSK (212)
5	Off-Hook (No Modem Connected)

The voice unit status has the following values:

Value	Function
Ø	Voice unit on hook
1	Voice unit off hook

INTERRUPT STATUS

Whenever the Voice Processor Module firmware interrupts the Telephone Server, it provides an interrupt status byte to inform the Telephone Server of the reason for interruption. The status is defined as follows:

Value (h)	Function
Ø	Acknowledge receipt of command (if the command involved a connect/disconnect from the crosspoint switch, the map in the TMCB is updated just before this interrupt)
1	Telephone line state change (includes voice unit changes)
2	Unused
3	Finished DTMF digit generation
4	Have call progress tone timing
5	CODEC status change
6	Modem status change
7	Finished pulse dial
8	No action taken on last command
9	Acknowledge receipt of command and telephone line state change
ØA	TMCB is valid
ØB	DTMF character received

BUFFER MANAGEMENT

Two general buffer management techniques are used in the Voice Processor Module: character lists and character queues. Character lists are used for dialing and DTMF generation, and character queues are used for data communications (modem) and voice digitization (CODEC).

CHARACTER LISTS

A character list is a static list of characters used to perform pulse dialing and DTMF generation. Character lists have the following format:

Offset	Contents
Ø	Buffer Size (bytes)
1 - 3	Buffer Address

The firmware assumes that the list will be filled (that is, the buffer size will be the actual number of characters in the list).

The data format in the pulse dial list will be the actual digit (Ø through 9) to be dialed. The format of the data in the DTMF generator list will conform to the list of hexadecimal codes found in the "DTMF Generator Register" part of the "8Ø51 Microprocessor External Devices" subsection, above.

CHARACTER QUEUES

A character queue is a unidirectional, circular buffer used for character-oriented data transfer between a producer and a consumer process. This buffer is controlled by a data structure called a Character Queue Control Block (CQCB). The format of the CQCB is as follows:

Offset	Contents
Ø	Buffer Size (256 bytes)
1 - 3	Buffer Address
4 - 5	Producer Offset
6 - 7	Consumer Offset

Byte Ø contains the size of the data buffer, in units of 256 bytes. Bytes 1 through 3 contain the 24-bit absolute memory address of the data buffer. The word at offset 4 of the CQCB contains the offset of the next byte to be entered into the buffer by the producer process. Offset 6 contains the offset of the next byte to be removed from the buffer by the consumer process.

For CODEC application of the character queue, the firmware in the Voice Processor Module updates the consumer/product offset (whichever is appropriate) after each 256 characters transmitted. This saves time during the firmware CODEC interrupt routine.

DTMF RECEIVER CHARACTER DATA SLOT

The DTMF receiver reports each character as it is received. The character is placed into its data slot, and a level 4 interrupt (XINTR4-) is issued to the Processor Module. (It is assumed that the Processor Module has had time to read the previous byte; therefore, no check is performed.)

ERROR REPORTING

Fatal errors such as buffer overruns or loss of carriers are reported in the CODEC or Modem Line Error Code fields in the TMCB. Parity errors from the modem will be reported immediately to the Telephone Server. The last character in the queue is the errored character and is presented exactly as received.

CALL PROGRESS TONE DETECTION

The algorithms for decoding the various call progress tones is executed by the Telephone Server. After two signal transitions (low to high, or high to low), the Voice Processor Module firmware will report the number of 10-millisecond periods that the signal was low and then high. The Telephone Server will use this on-off timing to determine the call progress tone (for example, 500 milliseconds on, 500 milliseconds off equals busy). See the Telephone Server Manual.

PAUSE DETECTION

When the CODEC is in encoding mode, the 8051 microprocessor monitors the volume level received by the CODEC at every interrupt. When a volume level of 0 is detected, the corresponding ADPCM code from the CODEC will be set to 8 before generating to the Processor Module.

EXTERNAL RAM ADDRESS SUMMARY

A summary of the 8051 microprocessor external RAM locations defined for the Voice Processor Module is provided in Table 2-1. Addresses, associated logic, input information, and output information are listed.

Table 2-1. External RAM Address Summary. (Page 1 of 2)

Address (h)	Associated Logic	Read	Write
00	MT8870 integrated DTMF receiver, analog tone detection	Tone Detector register	---
10	MSM5218 ADPCM speech analysis/synthesis IC	CODEC stacker/ destacker	CODEC stacker/ destacker
20	X-Bus interface	Data register	Data register
30	LM3915 dot/ bar display driver	Loudness Level register	---
40	X-Bus interface	---	High Byte Address register
50	X-Bus interface	---	Middle Byte Address register
60	X-Bus interface	---	Low Byte Address register
70	X-Bus interface	---	Control register

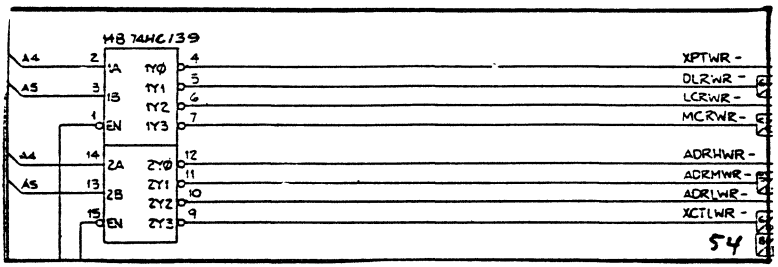
Table 2-1. External RAM Address Summary. (Page 2 of 2)

Address (h)	Associated Logic	Read	Write
8Ø - 87	MT88Ø4 analog crosspoint switch array		Crosspoint switch matrix
9Ø	MT5Ø89 integrated tone dialer		DTMF Generator register
AØ	Telephone lines, modem, CODEC encode/ decode		Line Control register
BØ	Modem board		Modem Control register

INTRODUCTION

This section provides detailed component-level descriptions of the hardware incorporated on the Controller board in the Voice Processor Module and is directed to the engineer who needs to understand the Voice Processor Module at the component level. Each functional block shown in Figure 3-1 is described in relation to the logic that performs the function. In addition, schematic drawings are provided in Appendix C (Figure C-1), and schematic windows are provided on each applicable page to supplement the text.

Each schematic window represents an applicable portion of the schematic diagram. The page of the schematic diagram and location (coordinate) within that page is provided below each window. An example is as follows:



(From Figure C-1, Page 4, Coordinate 3C)

This window comes from page 4 of the schematic drawing in Figure C-1 (Appendix C). The exact location of the window is at coordinate 3C.

Printed circuit board assembly drawings and Voice Processor Module assembly drawings are provided in Appendix C.

The Modem board specifications are given in Appendix B.

As shown in Figure 3-1, the analog crosspoint switch array logic, which is controlled by the 8051 microprocessor, allows switching among the various functional blocks. Each functional block, including the analog crosspoint switch array and the 8051 microprocessor, is described in the

following paragraphs. In addition, an example call setup to line 1 is described at the end of this subsection.

8051 MICROPROCESSOR

The 8051 microprocessor has access to all functional blocks shown in Figure 3-1 via its address and reads from or writes to applicable functional blocks via its 8-bit data bus. The 8051 microprocessor also contains the necessary command signals to control each functional block.

ANALOG CROSSPOINT SWITCH ARRAY

The analog crosspoint switch array, under control of the 8051 microprocessor, switches and connects the various functional blocks to their appropriate states at the appropriate times. As shown in Figure 3-1, J0 (Junctor 0) connects the applicable functional blocks to the line 1 interface, which is used to communicate with the central office or PABX station.

In addition, J1 (Junctor 1) connects the applicable functional blocks to the line 2 interface, which communicates with the central office or PABX station.

The following functional blocks can be connected to J0 or J1 via the analog crosspoint switch array:

- voice unit interface
- 212/103 modem board
- DTMF generator
- DTMF receiver/call progress tone detector
- voice amplifier
- ADPCM encoder
- ADPCM decoder

As shown, the 8051 microprocessor communicates with the analog crosspoint switch array via its address/data bus.

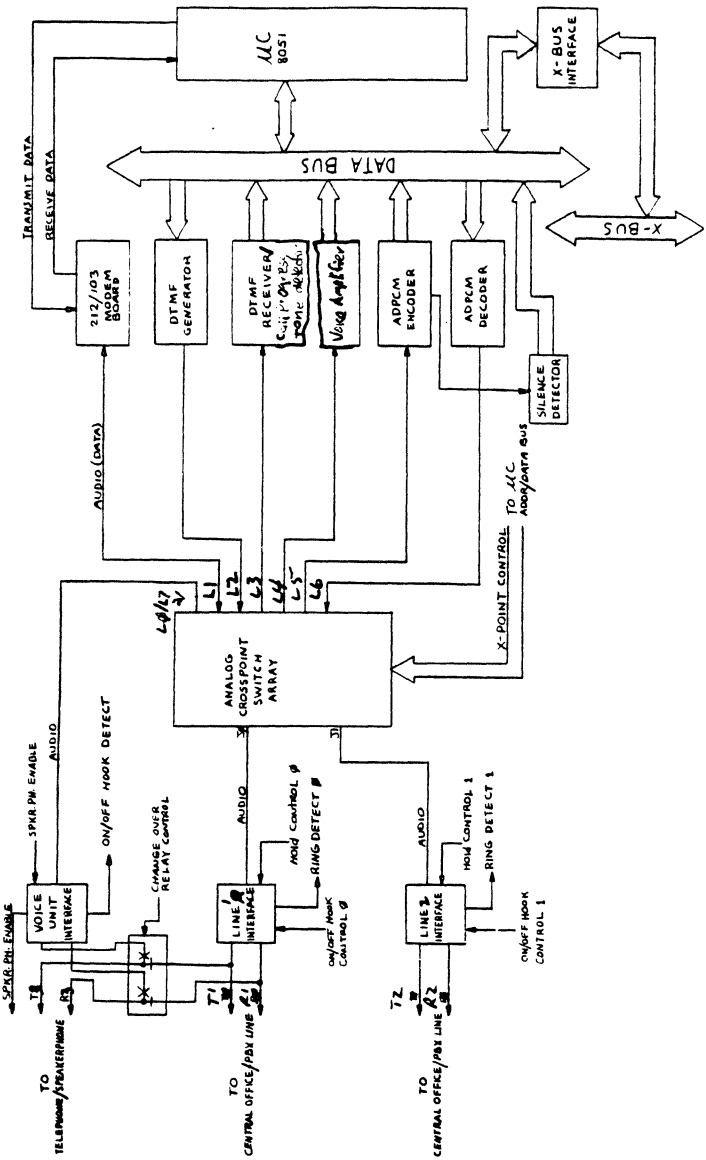


Figure 3-1. Controller Board Logic Functional Block Diagram.

VOICE UNIT INTERFACE

The voice unit interface connects a voice unit (telephone, speakerphone, etc.) to either line interface 1 or line interface 2, or to neither (for example, dictation), depending upon commands from the 8051 microprocessor. The voice unit interface, when enabled, sends its on/off hook status back to the 8051 microprocessor.

Note that the change over relay control is enabled by the 8051 microprocessor to connect the voice unit to either line 1, line 2, or neither.

Also note that the 8051 microprocessor controls the following:

- o on/off hook control (line 1 and line 2)
- o hold control (line 1 and line 2)

A ring detect from line 1 or line 2 informs the 8051 microprocessor of a ring for the respective line.

212/103 MODEM BOARD

The Modem board connects to the Controller board via the Motherboard and contains a Bell-compatible 300/1200 baud modem. The modem provides voice-band data transmission, operates in both originate and answer mode, and supports full-duplex transmission.

The modem can be used for high-speed operation using phase-shift keying (PSK) or low-speed operation using frequency-shift keying (FSK).

DTMF GENERATOR

The DTMF generator allows for automatic dialing across either line 1 or line 2. One of 16 tones can be generated at any time, depending upon the binary value set by the 8051 microprocessor.

DTMF RECEIVER/CALL PROGRESS TONE DETECTOR

The DTMF receiver detects touch tones and can be connected across either line 1 or line 2, or directly to the DTMF generator.

Call progress tone detection, which consists of analog circuits, detects dial tone, reorder tone, busy tone, and answer (ringback) tone.

VOICE AMPLIFIER

The voice amplifier is used to amplify voice signals along the voice unit-to-central office/PABX connection through the analog crosspoint switch array.

ADPCM ENCODER

A speech analyzer/synthesizer, known as a CODEC (Encoder/Decoder), uses the Adaptive Differential Pulse Code Modulation (ADPCM) method of data compression to compress 4-bit parallel voice data, which is generated to a stacker/destacker.

The stacker/destacker, under 8051 microprocessor control, converts two nibbles of encoded voice information from the CODEC to a byte of data that can be transferred to memory via the 8-bit data bus.

Silence detection circuitry detects voice.

ADPCM DECODER

To decode voice information from memory, the data is generated to the stacker/destacker via the 8-bit data bus. The stacker/destacker, under 8051 microprocessor control, generates 4-bit nibbles to the CODEC for decoding.

X-BUS INTERFACE AND MODE 3 DMA TRANSFER

Data transfers are performed via mode 3 DMA transfers over the X-Bus, which is controlled by the X-Bus interface signals issued by the 8051 microprocessor and associated logic.

Note that the Voice Processor Module is a mode 3 DMA master, signifying that it requests use of the X-Bus from the system controller and then performs the DMA logic necessary for the transfer.

CALL SETUP TO LINE 1 EXAMPLE

To perform an automatic call setup to line 1, the line must first go off hook via the line 1 interface circuitry. The line 1 interface circuitry makes a continuous path between T1 (Tip 1) and R1 (Ring 1). This indicates to the central telephone office/PABX that the module is requesting service. The central office/PABX then detects loop current and sends a dial tone back to signify that the module can begin dialing.

The Voice Processor Module goes off hook via the on/off hook control logic, which is controlled by the 8051 microprocessor, while connecting the call progress tone detection circuitry via the analog crosspoint switch array logic.

The call progress tone detection logic detects the dial tone, and the dial tone is reported to the system. In response, the system changes the connection by taking the call progress tone detection logic off of J0 and connecting the dual-tone multifrequency (DTMF) generator to start driving the applicable digits via an 8-bit write register. At the same time, the digits are generated in an attenuated form (that is, as a pacifier tone) to the voice unit interface circuitry. In other words, since the transmission level of the telephone line is much higher than the transmission level at the telephone, the digits need attenuation.

The DTMF receiver is used for remote control of the Voice Processor Module. This allows the module to be controlled by other Voice Processor Modules or remote telephones via DTMF signaling. The DTMF receiver detects DTMF digits, which are received by the 8051 microprocessor, allowing the system to respond to the digits. (In other words, the system expects a certain sequence of digits to operate properly.)

The ADPCM encoder logic allows voice storage. The ADPCM encoder acts as an answering machine for the telephone line. In other words, the ADPCM encoder records the incoming messages to memory.

If the ADPCM encoder detects no voice, the silence detector circuitry will report this to the system, which will not store data at that time. Therefore, the silence detector circuitry saves disk space.

The ADPCM decoder logic is used to decode the digital data back to the line interface circuitry via the analog crosspoint switch array. In other words, a message from memory can be played back to the telephone line or to the voice unit (telephone).

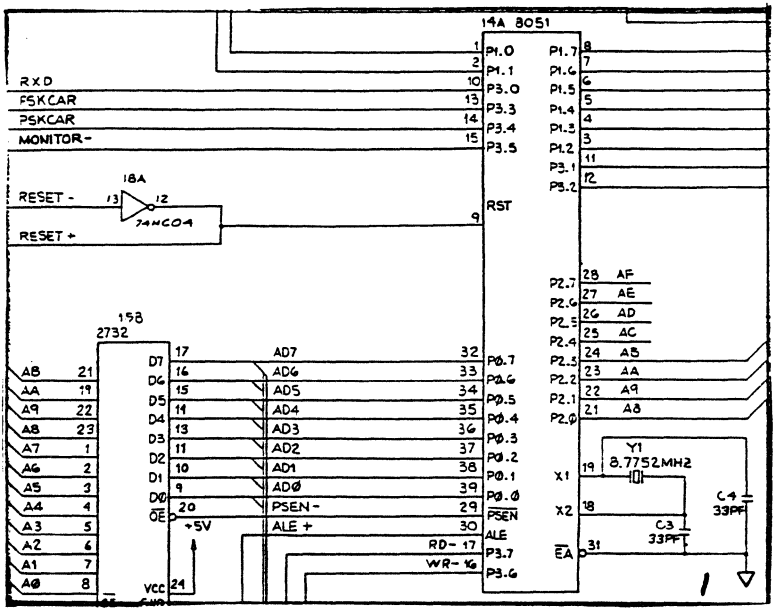
The change-over relay control allows connection of the voice unit to either the voice unit interface, line 1, or line 2.

If system power fails, the telephone will continue to operate. The default line during a power failure connects the voice unit through line 1, allowing the connection to continue.

CIRCUIT DESCRIPTIONS

Detailed component-level circuit descriptions are given for each of the following functions:

- clock generation logic
- processing unit logic
- X-Bus module initialization/identification
- X-Bus mode 3 master logic
- address bus interface logic
- data bus interface logic
- read-only memory
- device decoding
- crosspoint matrix control
- pulse code modulation filtering
- voice amplifier
- analog-to-digital conversion
- CODEC logic
- stacker/destacker logic
- silence detection and volume control
- tone dialing



(From Figure C-1, Page 4, Coordinate 5C)

- tone detection
- call progress tone detection
- line and voice unit interface relays
- line interface circuitry
- voice unit interface circuitry
- line 1 or 2 in parallel with voice unit interface
- DC-to-DC power conversion

CLOCK GENERATION LOGIC

An 8.7752-MHz crystal oscillator (Y1), shown above, provides the 8051 microprocessor with the necessary clock pulses at pins 18 and 19, which connect to an internal oscillator.

PROCESSING UNIT LOGIC

8051 MICROPROCESSOR

The 8051 microprocessor controls all functions of the Voice Processor Module. The 8051 microprocessor contains the following:

- 4K bytes of nonvolatile ROM
- 128 bytes of volatile RAM
- 32 I/O lines
- two 16-bit timers
- one five-source, two-priority level, nested interrupt structure
- serial I/O port used to interface to the modem
- 8-bit parallel port used for input signals from the modem and X-Bus interface
- oscillator and clock circuitry

The pin assignments and functions for the 8051 microprocessor are listed in Table 3-1.

Table 3-1. 8051 Microprocessor 13A Pin Assignments and Functions. (Page 1 of 4)

Pin	Function
1 - 8	**Port 1 (P1.0 Through P1.7).** Eight-bit quasi-bidirectional I/O port. Individual pin functions are as follows:
1	**Hold Line 1 (HOLD1-).** When low, terminates line 1 for the hold function.
2	**Hold Line 2 (HOLD2-).** When low, terminates line 2 for the hold function.

Table 3-1. 8051 Microprocessor 13A Pin Assignments and Functions. (Page 2 of 4)

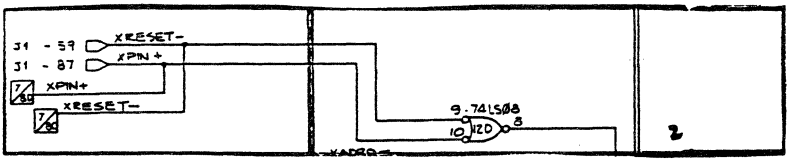
Pin	Function
3	**X-Bus Memory Busy (XMEMBSY-).** Input signifying that the Voice Processor Module has generated a local DMA request. After the cycle has completed, XACK- clears the command lines, including this bit, signifying that the cycle has completed. (Another DMA request cannot be generated until this bit becomes inactive.)
4	**X-Bus Interrupt Pending (XINTPND+).** Input signifying that an interrupt request (that is, XINTR4-) has been generated to the system controller.
5	**Module Attention Pending (NGATTN+).** Active-high input that signifies an interrupt from the Processor Module to the Voice Processor Module.
6	**Voice Unit Off-Hook (VUOH-).** Active-low input that signifies that the voice unit is off hook.
7	**Clear Module Attention (CLRATTN-).** Active-low output that clears the Module Attention Pending bit (pin 5).
8	**Modem Reset (MODEMRST-).** Output that resets the modem.
9	**Reset/Standby Power (RST+).** A low-to-high transition resets 13A.
10 - 17	**Port 3 (P3.0 Through P3.5).** Eight-bit quasi-bidirectional I/O port. Individual pin functions are as follows:
10	**Receiver Data (RXD+).** Receives asynchronous data from the modem via the telephone line.

Table 3-1. 8051 Microprocessor 13A Pin Assignments and Functions. (Page 3 of 4)

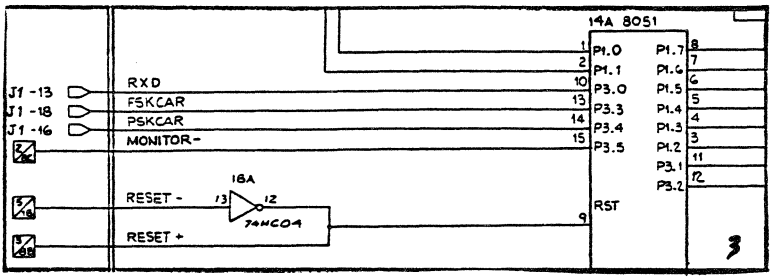
Pin	Function
11	**Transmit Data (TXD+).** Transmits asynchronous data to the modem via the telephone line.
12	**CODEC Interrupt (CODECINT-).** Interrupt Ø input from the CODEC signifying that a byte of voice information has been encoded by the CODEC and is ready to be transferred to memory, or a byte of voice information has been transferred from memory to the CODEC for decoding.
13	**Frequency Shift Keying Carrier Detect (FSKCAR+).** FSK carrier detect interrupt from the 3ØØ baud modem. (Used to control the data call setup.)
14	**Phase Shift Keying Carrier Detect (PSKCAR+).** PSK carrier detect interrupt from the 12ØØ baud modem. (Used to control the data call setup.)
15	**Monitor (MONITOR-).** Output set by firmware to adjust the gain for the call screening (monitoring) function of the answering machine (that is, adjust the gain of the receive part of the TP3Ø4Ø filter).
16	**Write (WR-).** Latches data byte from port Ø into the external data RAM.
17	**Read (RD-).** Enables external data RAM to port Ø.

Table 3-1. 8051 Microprocessor 13A Pin Assignments and Functions. (Page 4 of 4)

Pin	Function
18, 19	**Crystal Oscillator Input/Output.** (X1 and X2). Input to and output from the internal oscillator's high gain amplifier; connected to 8.7752-MHz crystal.
20	**Negative Power Supply (VSS-).** Tied to ground.
21 - 28	**Port 2 (P2.0 Through P2.7).** Eight-bit quasi-bidirectional I/O port that generates the high-order address nibble (that is, A8+ through AB+) when accessing external ROM.
29	**Program Store Enable (PSEN-).** Output that enables external ROM.
30	**Address Latch Enable (ALE+).** Output that clocks address latch.
31	**Enable Address (EA-).** Tied to ground so 13A fetches all instructions from external program ROM.
32 - 39	**Port 0 (P0.0 Through P0.7).** Eight-bit bidirectional I/O port that multiplexes the low-order address and data bus (that is, AD0+ through AD7+).
40	**Positive Power Supply (VCC+).** Strapped to +5 V.



(From Figure C-1, Page 5, Coordinate 8C)



(From Figure C-1, Page 4, Coordinate 7D)

INITIALIZATION LOGIC

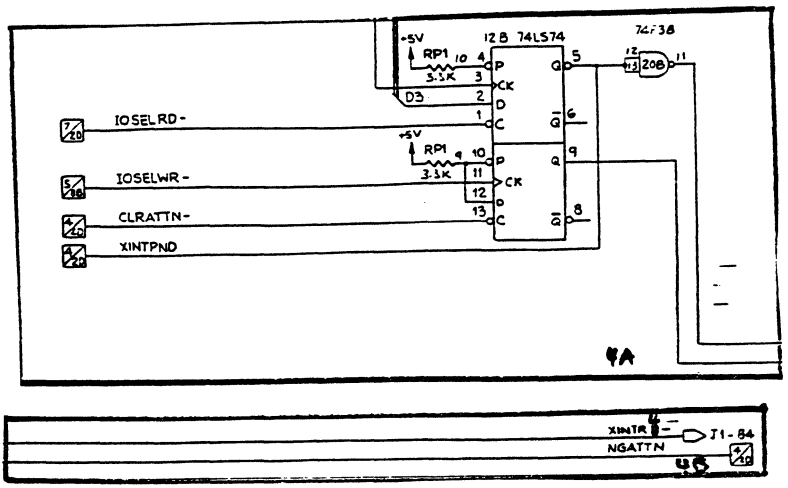
The 8051 microprocessor is initialized at pin 9 during a power up or manual reset or when the Processor Module suspends all activity on the X-Bus for the Voice Processor Module (during X-Bus module initialization, described below).

As shown in the top window above, during a power-up or manual reset, or during suspension of the X-Bus, XRESET- (X-Bus Reset) or a low XPIN+ (X-Bus Priority Input) is generated to the Voice Processor Module via connector J1, pin 59 or 87. XRESET- or the low XPIN- is logically NORed at AND gate 12D, and RESET- (Reset) is generated from pin 8 to 18A (shown in the bottom window).

As shown, RESET- is inverted at gate 18A (pin 12), to reset the 8051 microprocessor at pin 9.

INTERRUPT LOGIC

An interrupt can be generated either by the Voice Processor Module to the Processor Module, or by the Processor Module to the Voice Processor Module. Each is described below.



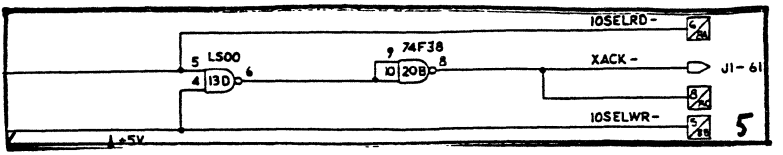
(From Figure C-1, Page 6, Coordinates 6B and 3A)

Voice Processor Module Interrupt Generation

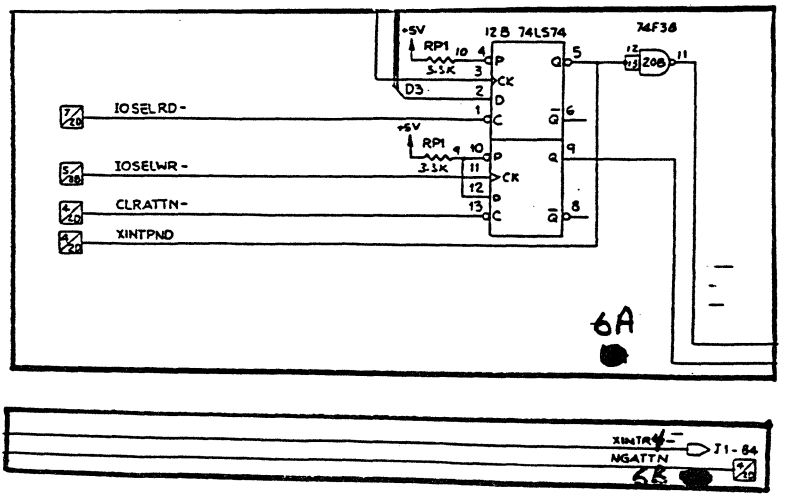
During a Voice Processor Module interrupt generation, the 8051 microprocessor writes data into memory and then sets bit 3 of X-Bus Interface Control register 12B, shown in the top portion of the split window above. This causes a high signal at pin 5, which is inverted at NAND gate 20B (pin 11), as XINTR4- (X-Bus Interrupt, Priority 4). As shown in the bottom portion of the split window above, XINTR4- connects to the Processor Module via connector J1, pin 84. Note that the high signal at pin 5 of 12B is also connected to the 8051 microprocessor as XINTPND+ (X-Bus Interrupt Pending), signifying that an X-Bus request has been generated to the Processor Module.

The Processor Module then reads the data that the Voice Processor Module has written into memory, and issues IOSELRD-.

IOSELRD- clears data bit 3 of X-Bus Interface Control register 12B (pin 1), shown in the top portion of the split window above. In other words, the X-Bus interrupt is deasserted when the Processor Module reads data bit 3 of address 70h. Note that XINTPND+ is also deasserted.



(From Figure C-1, Page 7, Coordinate 2D)



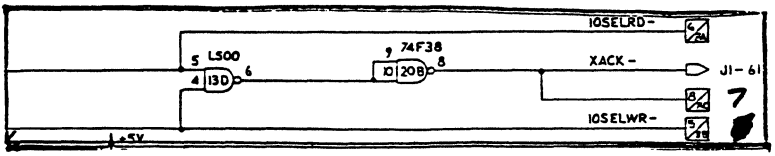
(From Figure C-1, Page 6, Coordinates 6A and 3A)

In addition, IOSELRD- is inverted at 13D (pin 6) and 20B (pin 8), to generate XACK- back to the Processor Module, as shown in the top window, above.

Processor Module Interrupt Generation

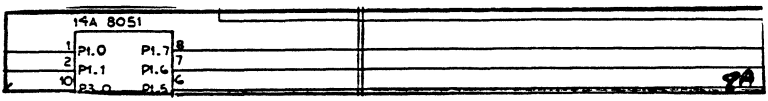
During a Processor Module interrupt generation, the Processor Module writes data into memory, and then interrupts the Voice Processor Module. In response, the Voice Processor Module reads the data from memory.

During a Processor Module write, IOSELWR- clocks 12B (pin 11), shown in the top portion of the bottom window, which forces NGATTN+ (Module Attention) from pin 9, shown in the bottom window. NGATTN+ connects to the 8051 microprocessor at pin 5, signifying an I/O write to the Voice Processor Module from the Processor Module.

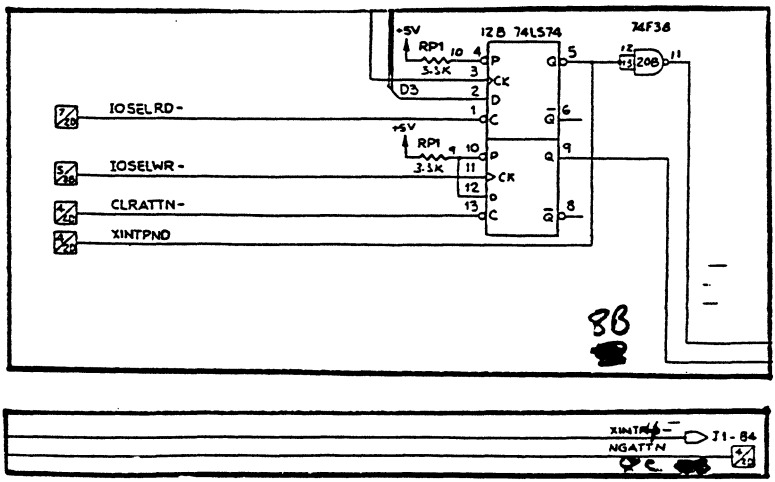


(From Figure C-1, Page 7, Coordinate 2D)

In addition, IOSELWR- is inverted at 13D (pin 6) and 20B (pin 8), to generate XACK- back to the Processor Module.

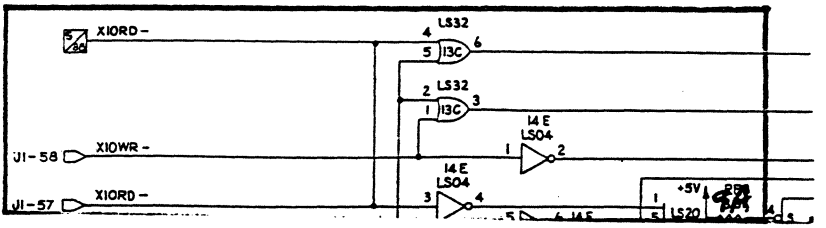


(From Figure C-1, Page 4, Coordinate 5D)

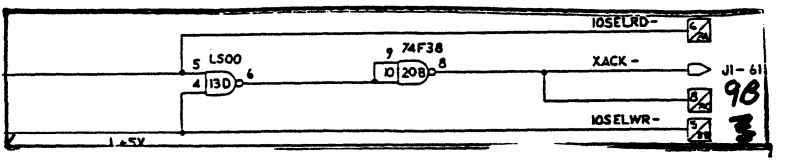


(From Figure C-1, Page 6, Coordinates 6B and 3A)

Note that after the 8051 microprocessor has read from memory, it issues CLRATTN- (Clear Attention) from pin 7 (shown in the top window) to pin 13 of 12B (shown in the bottom window). CLRATTN- clears the module attention bit that had signified the I/O write from the Processor Module. In other words, NGATTN+ becomes low at pin 9 (bottom window).



(From Figure C-1, Page 7, Coordinate 7D)



(From Figure C-1, Page 7, Coordinate 3D)

The Processor Module also interrupts the Voice Processor Module when it reads or writes to port Ø1ØØh, Ø2ØØh, or whichever base I/O address is assigned to the Voice Processor Module during module initialization/identification. (See the "X-Bus Module Initialization/Identification Logic" subsection, below.) Either IOSELRD- (I/O Select Read) or IOSELWR- (I/O Select Write) is generated at OR gate 13C (pin 6 or 3, respectively), shown in the above window. IOSELRD- clears the X-Bus interrupt, and IOSELWR- asserts the X-Bus interrupt.

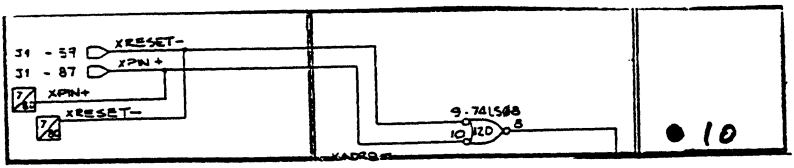
X-BUS MODULE INITIALIZATION/IDENTIFICATION LOGIC

INITIALIZATION

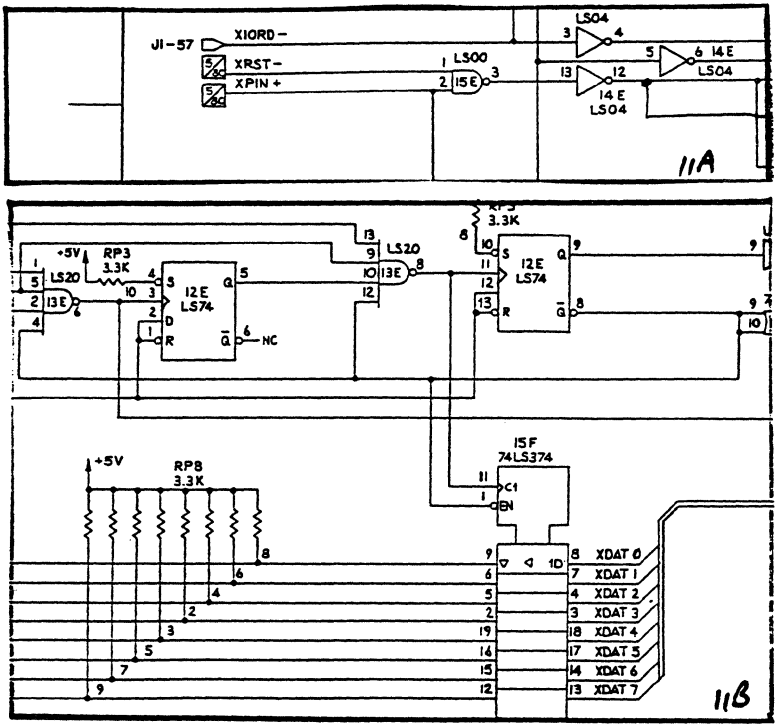
The Processor Module interrupts the Voice Processor Module through the X-Bus interface, as described in the following paragraphs and in Figure 3-2, "X-Bus Initialization/Interrupt Timing." The interrupt address is assigned by the Processor Module when a power-up or manual reset occurs on the X-Bus as XRESET- (X-Bus Reset), or when XPIN+ (X-Bus Priority Input) is reset low, signifying that activity on the X-Bus for the Voice Processor Module has been suspended.

To Be Supplied

Figure 3-2. X-Bus Initialization/Interrupt Timing.

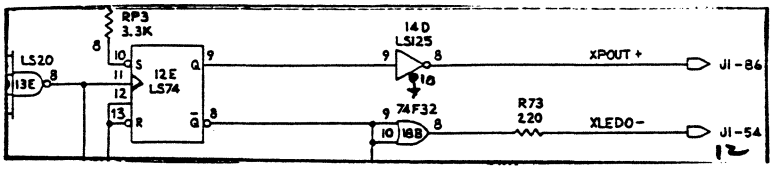


(From Figure C-1, Page 5, Coordinate 8C)



(From Figure C-1, Page 7, Coordinates 7D and 4D)

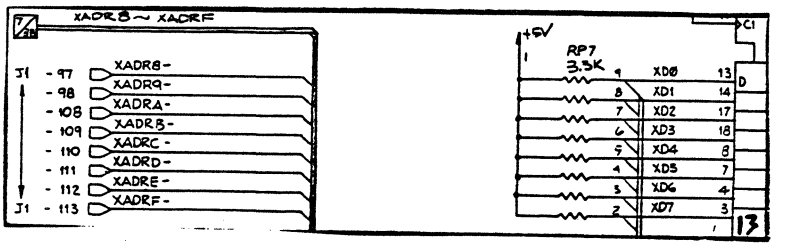
As shown in the top window above, XRESET-, connecting from J1, pin 59, is driven to NAND gate 15E (pin 1), shown in the bottom window. A low XPIN+ connecting from J1, pin 87, also connects to 15E (pin 2). In either case (that is, a reset or a low X-Bus Priority Input), a high signal is generated from 15E (pin 3), inverted at 14E (pin 12), and driven to D flip-flop 12E (pin 13), causing a high signal at pin 8 (bottom portion of the window). This high signal inhibits the output of Base I/O Address register 15F (pin 1).



(From Figure C-1, Page 7, Coordinate 2D)

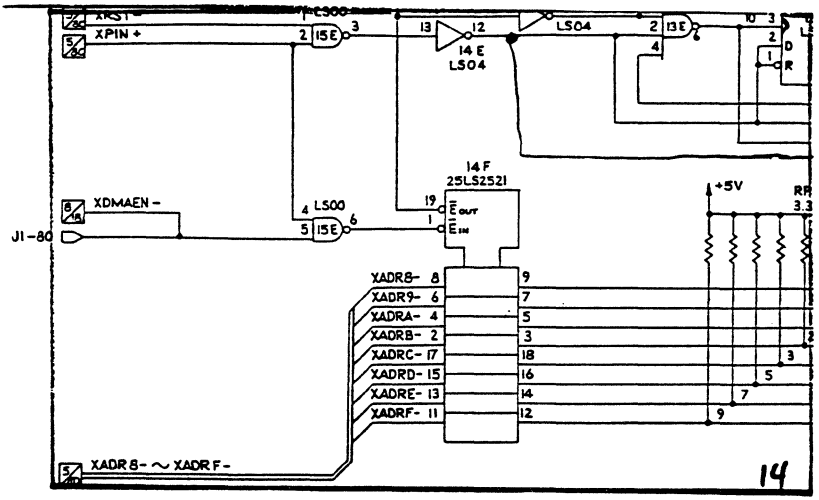
Since 12E is reset at pin 13, a low signal is generated from pin 9, forcing XPOUT+ (X-Bus Priority Output) low at pin 8 of 14D. (Note that 14D is always enabled since pin 1Ø is tied to ground.) This suspends all X-Bus activity for modules farther down the X-Bus (that is, to the right of the Voice Processor Module) via connector J1, pin 86.

XPIN+ then becomes low to signify that the Processor Module wishes to identify the Voice Processor Module (that is, assign the module a base I/O address).



(From Figure C-1, Page 5, Coordinate 8D)

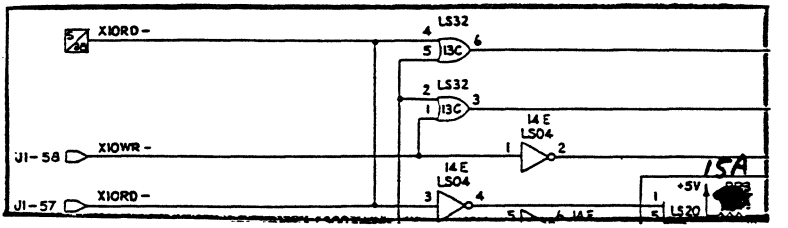
The Processor Module reads I/O address ØØ from lines XADR8- through XADRF- (X-Bus Address Lines 8 through ØFh) via connector J1, pins 97, 98, and 1Ø8 through 113), shown above. This high-order address byte, which represents port Ø, is generated to the A-side inputs of comparator 14F (shown in the window below).



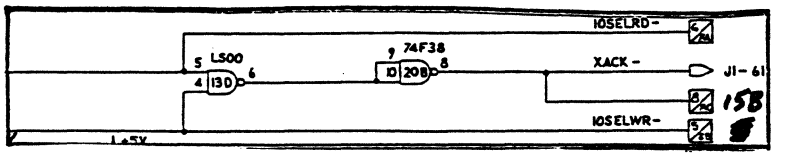
(From Figure C-1, Page 7, Coordinate 6C)

Note that XPIN+ is NANDed with an inactive XDMAEN- (X-Bus DMA Enable) at 15E (pins 4 and 5, respectively), to generate a low signal at pin 6, enabling comparator 14F at pin 1. XDMAEN- indicates that a DMA cycle is in progress, causing comparator 6E to become disabled at pin 1. During a DMA cycle, the XADR8- through XADRF- lines can contain memory address data not to be mistaken for a module base I/O address.

Since Base I/O Address register 15F was previously disabled at pin 1, the B-side inputs of comparator 14F also connect to eight high bits (pulled high by the 33-kohm resistors at RP8), and therefore compare as equal with the A-side inputs, causing a low signal to generate from pin 19 of 14F.

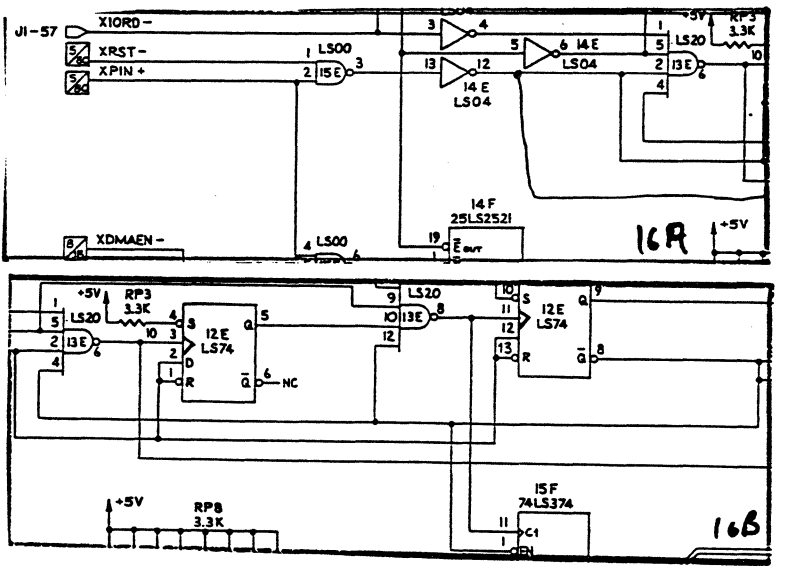


(From Figure C-1, Page 7, Coordinate 7D)



(From Figure C-1, Page 7, Coordinate 3D)

This low signal is driven at OR gate 13C (pins 5 and 2), forcing pin 6 of NAND gate 13D high, which causes NAND gate 20B to generate XACK- (Transfer Acknowledge) back to the Processor Module via connector J1, pin 61.

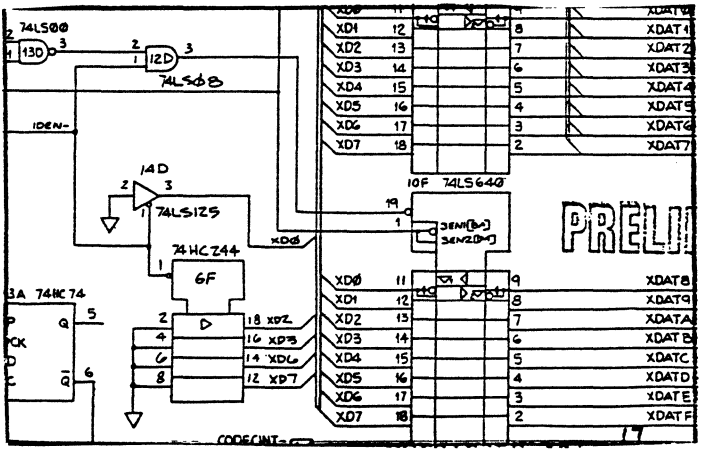


(From Figure C-1, Page 7, Coordinate 7D and 4D)

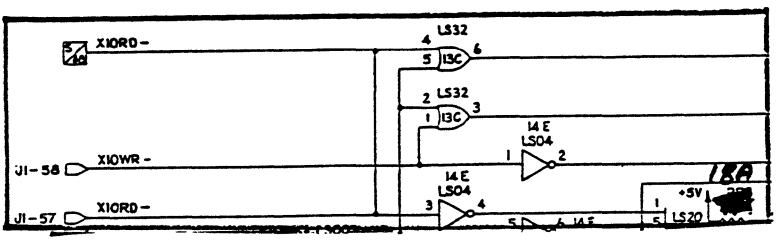
IDENTIFICATION

During XIORD- (X-Bus I/O Read) at connector J1, pin 57 (shown in the above window), XIORD- is inverted at 14E (pin 4) and NANDed at 13E (pin 1) with the following at pins 5, 4, and 2, respectively:

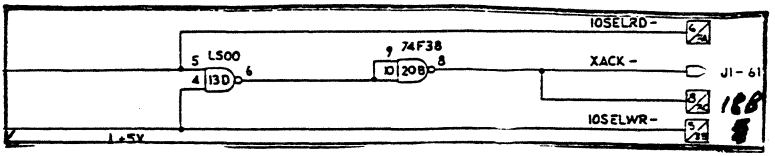
- o the complement of the low signal generated from 14F (pin 19), which signifies that the two sides of the comparator inputs are equal
- o the high signal from pin 8 of 12E, which disabled Base I/O Address register 15F
- o the high signal from pin 12 of 14E, which signifies that either a reset or low X-Bus priority input has been issued



(From Figure C-1, Page 5, Coordinate 3A)

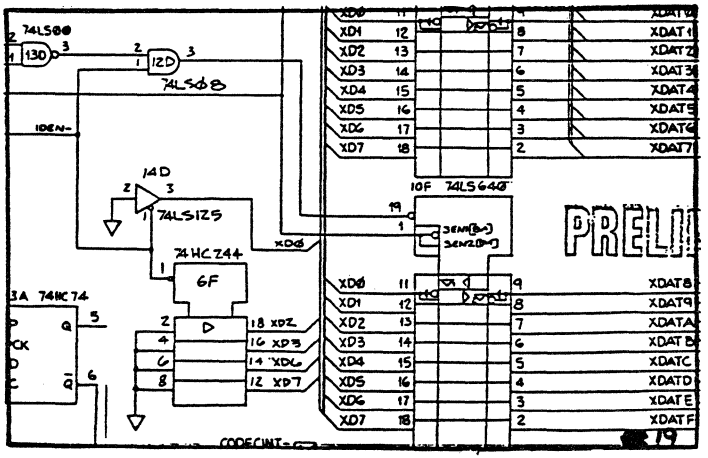


(From Figure C-1, Page 7, Coordinate 7D)

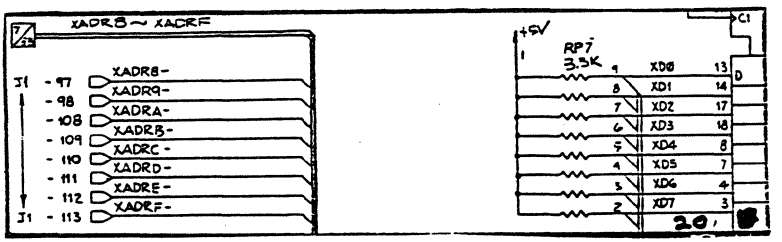


(From Figure C-1, Page 7, Coordinate 3D)

This forces IDEN- (Identification) at pin 6 of 13E. IDEN- enables hard-wired buffers 14D and 6F, shown in the top window above. In addition, XIORD- forces a high signal at 13D (pin 6), which is inverted and driven at 20B back to the Processor Module as XACK-, shown in the bottom window above.



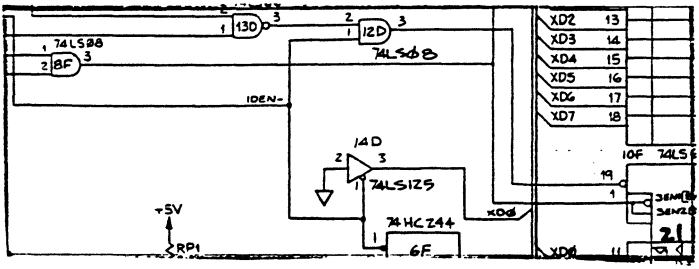
(From Figure C-1, Page 5, Coordinate 3A)



(From Figure C-1, Page 5, Coordinates 8D and 6D)

the module has been suspended and the Processor Module issues an XIORD- command to port 0. These conditions produce four high signals at the input of NAND gate 13E. A low signal is, therefore, generated, enabling hard-wired buffers 14D and 6F, shown in the top window (signifying that an I/O read of port 0 has occurred), which generates the assigned identifier number.

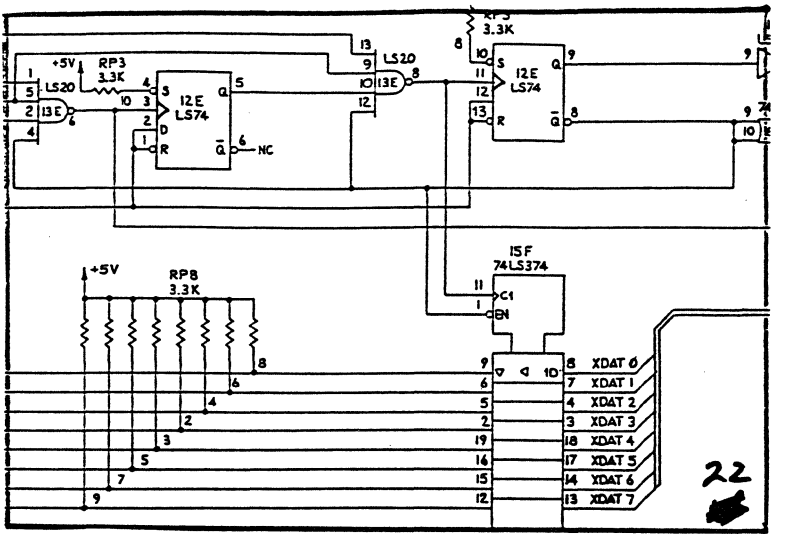
Since 14D and 6F are hard-wired, low-order module data lines XD0 through XD7 (Module Data Lines 0 through 7) are assigned identifying bits of 32h. That is, 32h is the identifying code for the Telephone Manager Module. Note that XD0, XD2, XD3, XD6, and XD7 are tied to ground while the remaining bits are strapped to +5 V via 3.3-kohm resistors at RP7.



(From Figure C-1, Page 5, Coordinate 3B)

Note also that IDEN- forces AND gate 12D low at pin 3, to enable data transceiver 10F (pin 19) for access to the X-Bus. Since XIORD- is active, a low signal is generated from pin 3 of AND gate 8F to pin 1 of 10F, and data is directed from XD0 through XD7 to XDAT0- through XDATF-.

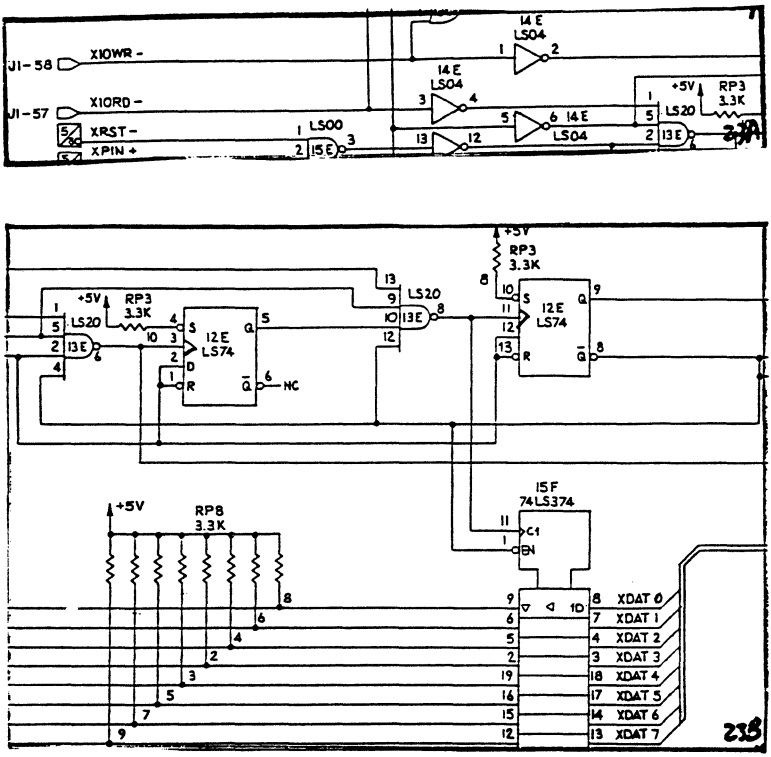
In summary, during the I/O read of port 0, the Telephone Manager Module identifier, 32h, is generated to the Processor Module via the X-Bus data lines.



(From Figure C-1, Page 7, Coordinate 4D)

Once the Processor Module receives the 32h Voice Processor Module identifier code, it writes the base I/O address for the module into I/O Address register 15F.

This I/O address defines the interrupt (base I/O) address reserved for the Voice Processor Module. The Processor Module issues an I/O address via low-order data lines XDATØ- through XDAT7-, and that becomes the high-order eight bits of the interrupt address, Ø1XXh, Ø2XXh, etc., depending upon the physical location of the Voice Processor Module. During the identification polling sequence, the module adjacent to the Processor Module uses addresses Ø100h through Ø1FFh, the next module uses Ø200h through Ø2FFh, and so on. The module identifier is stored in a memory table for use by the system. (See the "X-Bus Interface" subsection in Section 2, "Architecture.")



(From Figure C-1, Page 7, Coordinates 8D and 4D)

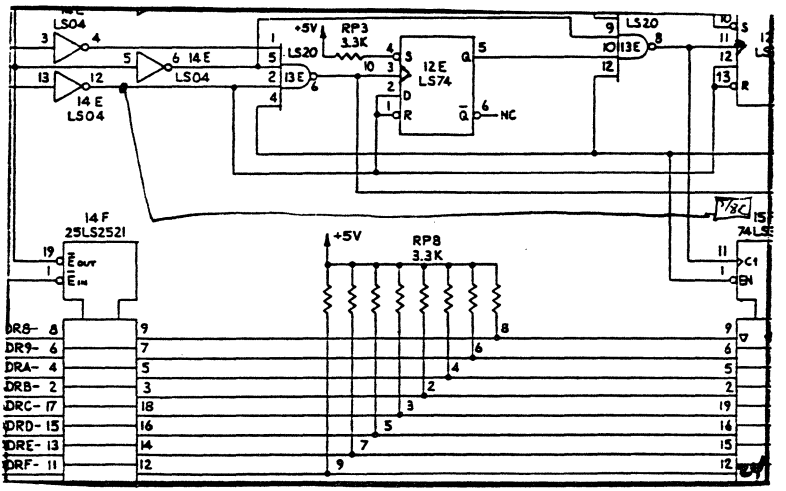
When the Processor Module writes the base I/O address to the Voice Processor Module, XIOWR- (X-Bus I/O Write), which connects at J1, pin 58, is inverted at 14E, pin 2 (upper window), and NANDed at 13E, pin 13 (lower window), with the following at pins 1Ø, 9, and 12, respectively:

- o the high signal from pin 12 of 14E (upper window), which signifies that either a reset or low X-Bus priority input has been issued; note that this high signal connects to the pin 2 input of D flip-flop 12E (lower window), causing the high to generate from pin 5 to 13E (pin 1Ø)

- a high signal from pin 6 of 14E (upper window), which represents the complement of the low signal generated from comparator 14F (pin 19) that signifies that the two sides of the comparator inputs are equal

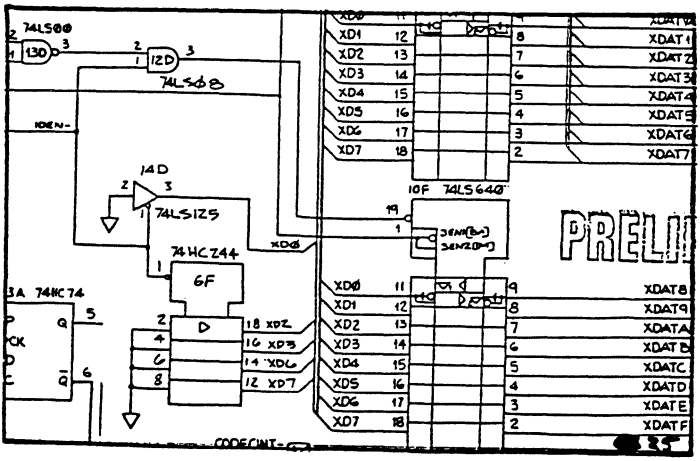
- the high signal from pin 8 of 12E, which disabled Base I/O Address register 15F (pin 1)

A low signal is, therefore, generated from 13E (pin 8), clocking Base I/O Address register 15F (pin 11), which is loaded with the base I/O address sent by the Processor Module.



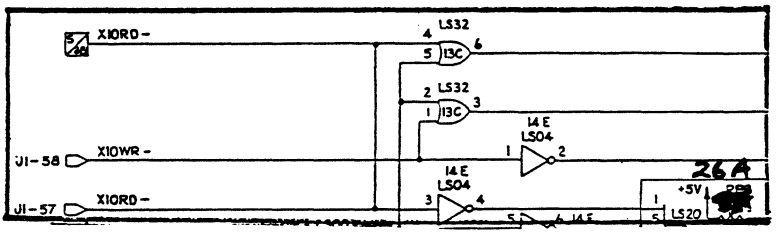
(From C-1, Page 7, Coordinate 5C)

Since the inputs at 15F consist of the module base I/O address, the outputs of 15F do not compare with the active XADR8- through XADRF- at comparator 14F. Therefore, a high signal is generated from 14F (pin 19), shown in the window. This high signal is inverted at 14E (pin 6), forcing IDEN- to its inactive state at pin 6 of 13E.

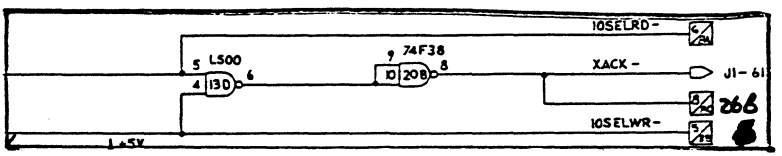


(From Figure C-1, Page 5, Coordinate 3A)

Therefore, module identifier buffers 14D and 6F are disabled at pin 1, shown above.

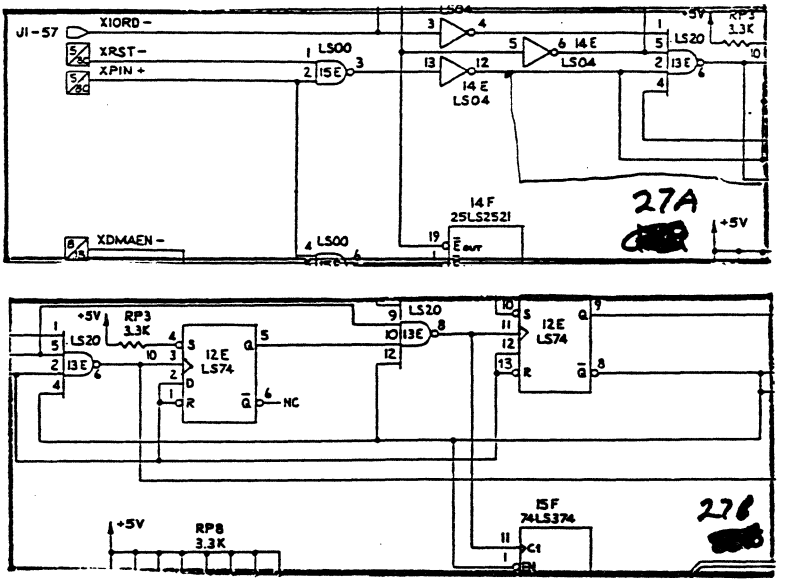


(From Figure C-1, Page 7, Coordinate 7D)



(From Figure C-1, Page 7, Coordinate 3D)

In addition, just as with XIORD-, XIOWR- asserts XACK- at NAND gate 20B (pin 8) to the Processor Module via connector J1, pin 61.

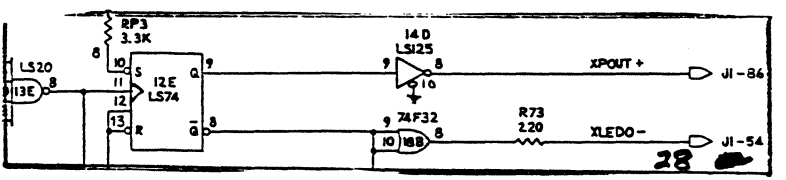


(From Figure C-1, Page 7, Coordinates 7D and 4D)

Note that by this time, XRST- is at its inactive state, and is NANDed with XPIN+, forcing a low signal at 15E (pin 3), which is inverted at 14E (pin 12) and driven to pin 12 of D flip-flop 12E.

The high signal that is generated from 13E (pin 8) clocks 12E (pin 11), and XPOUT+ is therefore generated from 14D (pin 8), which is always enabled since pin 1Ø is tied to ground.

A low signal from pin 8 of 12E ensures that both NAND gates at 13E are disabled at pins 4 and 12 (upper and lower window, respectively), and only the address written into Base I/O Address register 15F (bottom window) causes the module to respond to the interrupt from the Processor Module.



(From Figure C-1, Page 7, Coordinate 2D)

In addition, a low signal from pin 8 of 12E is driven at OR gate 18B through 220-ohm resistor R73 as XLED0- (X-Bus LED 0), signifying that the module has been identified via connector J1, pin 54.

To summarize, I/O reads or writes from or to the 8051 microprocessor (that is, interrupts) within the Voice Processor Module are performed when the Processor Module places a base I/O address for the Voice Processor Module (such as 01XXh, 02XXh, and so on) on the XADR8- through XADRF- address lines and issues an XIORD- or XIOWR-.

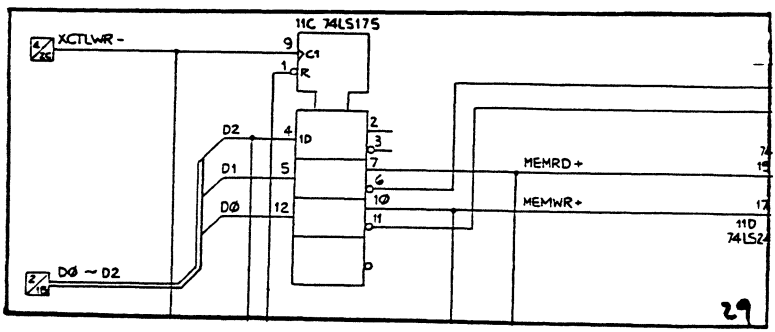
X-BUS MODE 3 MASTER LOGIC

CONTROL ARBITRATION

The 8051 microprocessor operates asynchronously to the system controller processor and performs reads or writes at any time. The system controller responds to the Voice Processor Module with an acknowledge (XACK-) after each transfer. Timing during mode 3 DMA transfers is shown in Figure 3-3.

When the 8051 microprocessor performs an X-Bus read or write, it loads the contents of the X-Bus Interface Control register with the following information:

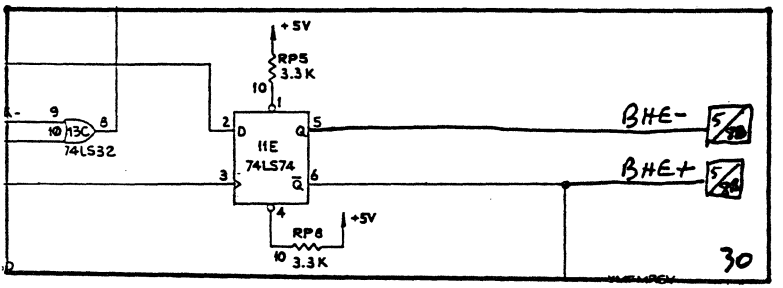
- o X-Bus read or write control
- o high byte or low byte transfer control



(From Figure C-1, Page 8, Coordinate 7D)

As shown in the above window, the 8051 microprocessor loads X-Bus Interface Control register 11C by writing to external RAM location 70h as described in the "Device Decoding" subsection, below. This causes XCTLWR- (X-Bus Interface Control Write) to generate to 11C (pin 9), clocking in data bits D0+ through D2+ as follows:

Data Bit	Pin	Function
D0+	12	When set, X-Bus write operation via mode 3 master DMA
D1+	5	When set, X-Bus read operation via mode 3 master DMA



(From Figure C-1, Page 8, Coordinate 3C)

As shown in the above window, D2+ connects to X-Bus Interface Control register 11E (pin 2), which is clocked by XCTLWR- (pin 3). When D2+ is set, the high data byte is enbaled; when D2+ is reset, the high data byte is disabled.

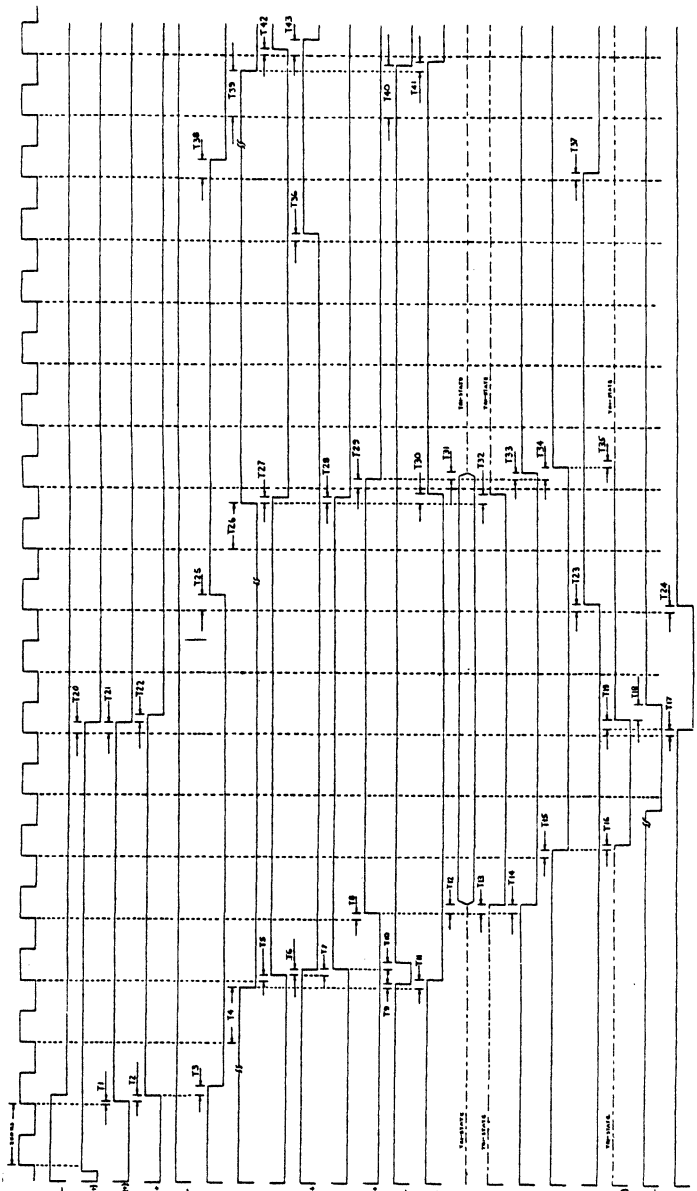
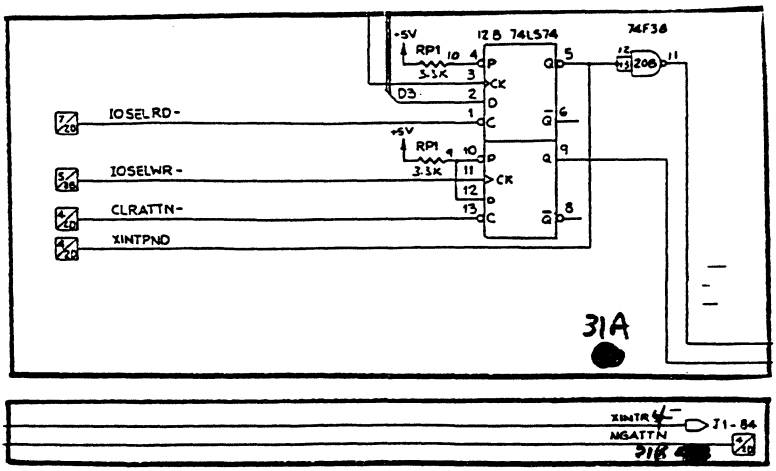


Figure 3-3. X-Bus Mode 3 DMA Timing.



(From Figure C-1, Page 6, Coordinates 6A and 3A)

As shown in the above window, when D3+ is set at X-Bus Interface Control register 12B, an X-Bus level 4 interrupt request (that is, XINTR4-) is issued to the system controller.

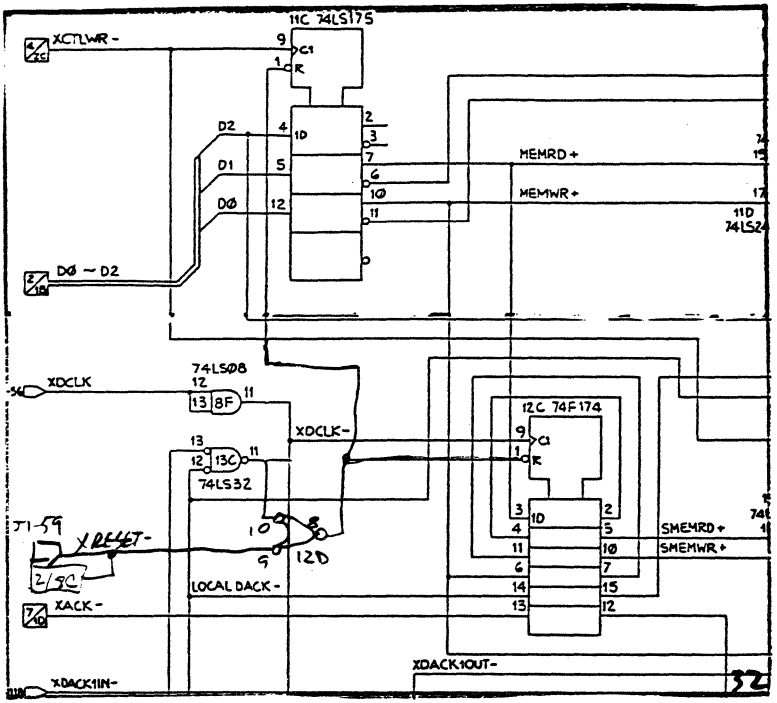
After a read or write is generated from the X-Bus Interface Control register, shown in the top window below as 11C, the Voice Processor Module operates according to the X-Bus mode 3 master DMA protocol.

During a read or write cycle, MEMRD+ or MEMWR+ is generated at 11C (pin 7 or 10) and is synchronized at 12C by XDCLK- (connector J1, pin 56), which is generated from the DMA controller in the Processor Module (that is, the system controller).

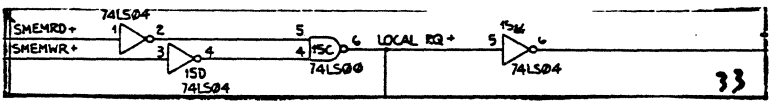
Note that MEMRD+ or MEMWR+ is synchronized to avoid metastable states in which the XDCLK- edge occurs simultaneously with MEMRD+ or MEMWR+.

Two XDCLK- pulses later, either SMEMRD+ (Synchronized Memory Read) or SMEMWR+ (Synchronized Memory Write) is generated. As shown in the bottom window below, SMEMRD+ or SMEMWR+ is inverted at 15D (pin 2 or 4) before connecting to AND gate 15C (pin 5 or 4). As a result, LOCAL RQ+ (Local Request) is generated from pin 6 of 15C.

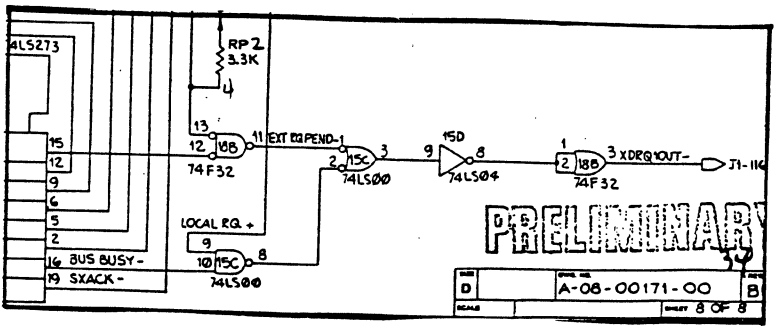
LOCAL RQ+ is used to generate the X-Bus DMA request to the system controller if the X-Bus is not busy. If the X-Bus is busy, the Voice Processor Module must wait until the bus becomes free before generating the X-Bus DMA request.



(From Figure C-1, Page 8, Coordinate 6C)



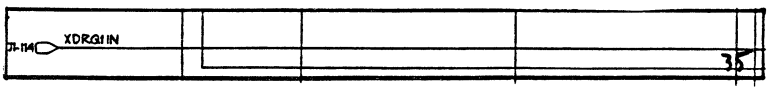
(From Figure C-1, Page 8, Coordinate 4C)



(From Figure C-1, Page 8, Coordinate 3A)

If the X-Bus is not busy, LOCAL RQ+ is generated to pin 9 of 15C, where it is NANDed with an inactive BUS BUSY- (Bus Busy) at pin 10. This causes a low signal to generate from pin 8 of 15C to pin 2 of 15C, forcing a high signal at pin 3. This high signal is inverted at 15D (pin 8) and driven by OR gate 18B (pin 3) as XDRQ1OUT- (X-Bus DMA Request, Channel 1, Output) to connector J1, pin 116, where it generates to the system controller.

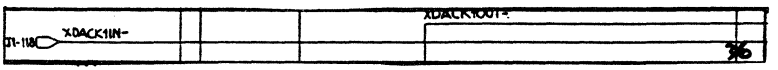
Note that EXT RQ PEND- (External Request Pending) at pin 1 of NAND gate 15C signifies that another X-Bus mode 3 master module downstream on the X-Bus has issued a DMA request via channel 1. Therefore, it also causes XDRQ1OUT-. In this case, the mode 3 master module closest to the system controller will gain access to the X-Bus.



(From Figure C-1, Page 8, Coordinate 8B)

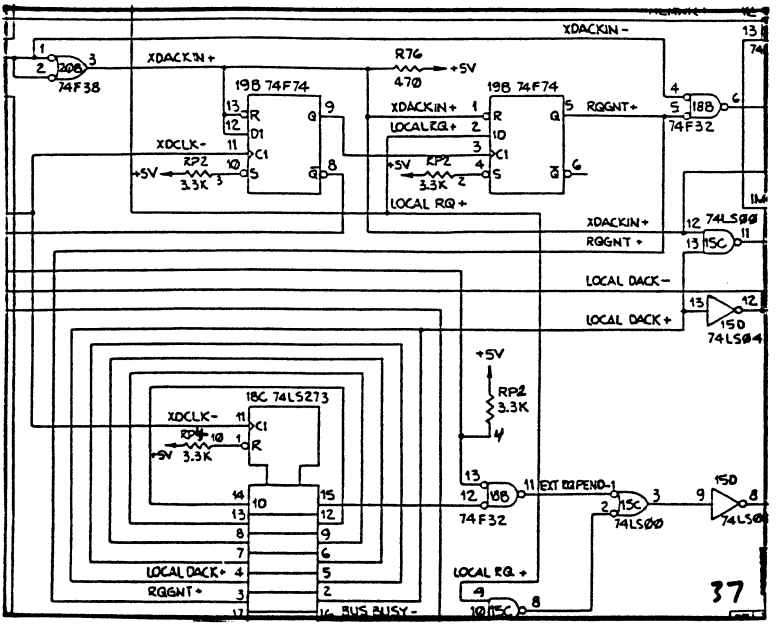
In other words, when another X-Bus mode 3 master module issues a DMA request, XDRQ1IN- (X-Bus DMA Request, Channel 1, Input) is generated to the Voice Processor Module at connector J1, pin 114. XDRQ1IN- is then logically NANDed at pin 13 of OR gate 18B (shown in the previous window) with a low signal at pin 12, which signifies the absence of a local DMA request. This causes EXTRQPEND- (pin 11), which is inverted at 15C (pin 3) and 15D (pin 8) before being driven as XDRQ1OUT- at 18B (pin 3).

LOCAL RQ+ is also inverted at 15D (pin 6) to generate XMEMBSY- (X-Bus Memory Busy), which is generated to the 8051 microprocessor at pin 3. XMEMBSY- signifies to the 8051 microprocessor that an X-Bus mode 3 master DMA cycle is in progress. (See the "Bus Interface Logic" subsection below for data read and write operations.)



(From Figure C-1, Page 8, Coordinate 8B)

In response, the system controller asserts XDACK1IN- (X-Bus DMA Acknowledge, Channel 1, Input) to connector J1, pin 118, which signifies that the Voice Processor Module has been granted the request. Therefore, the Voice Processor Module must ensure that the acknowledge is for it and then disable the next modules downstream on the X-Bus.

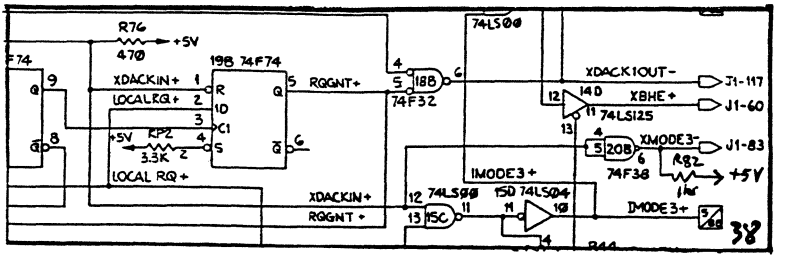


(From Figure C-1, Page 8, Coordinate 3B)

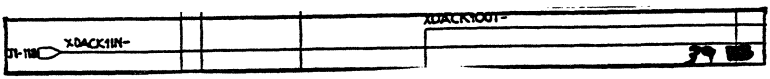
In other words, LOCAL RQ+, which was generated from pin 6 of NAND gate 15C in response to a read or write, is latched at D flip-flop 19B (pin 2) and will generate from pin 5 of 19B as RQGNT+ (Request Granted) when pin 3 of 19B is clocked by a high signal generated from pin 9 of 19B.

This occurs when XDACK1IN- is inverted at NAND gate 20B as XDACKIN+ (X-Bus DMA Acknowledge Input). XDACKIN+ connects to pin 12 of 19B, where it is synchronized by XDCLK- (pin 11), to generate the high signal at pin 9.

Note that LOCAL DACK+ signifies that the Voice Processor Module has access to the X-Bus. As shown in the above window, RQGNT+ is clocked by XDCLK- at 18C to generate LOCAL DACK+ (Local DMA Acknowledge) from pin 2, signifying that the arbitration is complete.



(From Figure C-1, Page 8, Coordinate 2B)



(From Figure C-1, Page 8, Coordinate 8B)

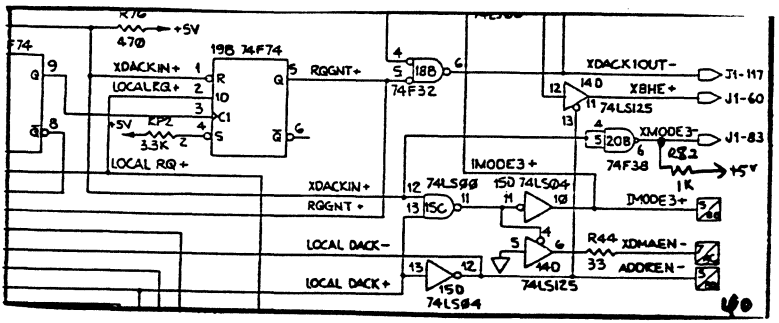
Since all modules on the X-Bus receive RQGNT+, the closest mode 3 master module to the system controller deasserts the DMA acknowledge. In other words, RQGNT+ forces XDACK1OUT- to its inactive state at OR gate 18B (pin 6). In addition, the other modules will never receive LOCAL DACK+ at NAND gate 15C. As shown in the bottom window, the inactive XDACK1OUT- appears to the next module as an inactive XDACK1IN- at connector J1, pin 118. As shown in the previous window, this inactive high signal is inverted at NAND gate 20B (pin 3), to reset D flip-flop 19B at pin 1. This causes RQGNT+ to become inactive at pin 3 of 18C and, therefore, LOCAL DACK+ becomes inactive.

In other words, RQGNT+ forces XDACK1OUT- high at NAND gate 18B (pin 6). This disables the next module on the X-Bus, and acknowledges the request of the Voice Processor Module. Note that when RQGNT+ is deasserted, signifying that the Voice Processor Module had not requested a DMA cycle, the inactive RQGNT+ is logically NANDed at 18B with XDACK1IN-, enabling XDACK1OUT- and the next module on the X-Bus.

The Voice Processor Module then gains control of the X-Bus.

In summary, the Voice Processor Module generates a DMA request output to the system controller, recieves a DMA acknowledge input from the system controller, ensures that the request is for itself, disables the next X-Bus module, and is ready to perform a DMA transfer.

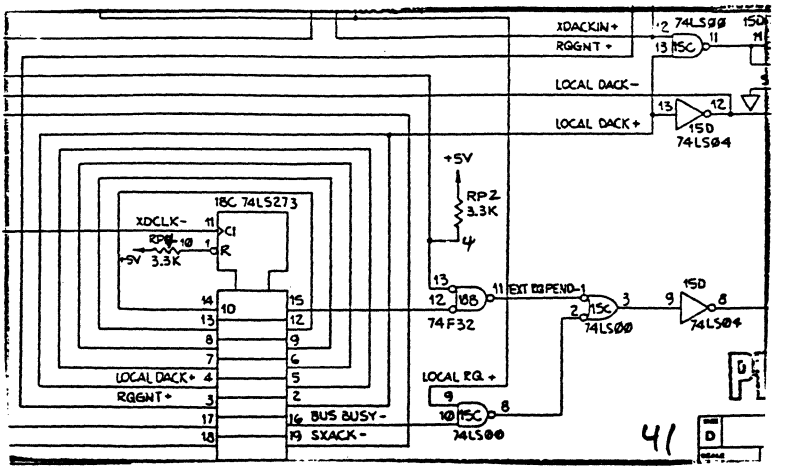
CONTROL SIGNALS



(From Figure C-1, Page 8, Coordinate 1B)

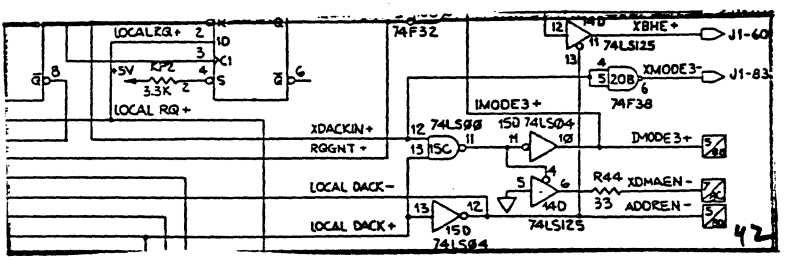
The Voice Processor Module uses the following control signals for the DMA transfer:

- ADDEN- (Address Enable), which enables the address bus for accessing the 24-bit X-Bus address of the location in memory that will be read from or written to
- XBHE- (X-Bus Byte High Enable), which signifies either a high byte enable (when set) or high byte disable (when reset), depending upon the data transfer
- IMODE3+ (Internal Mode 3 Control), which signifies that a mode 3 master transfer is occurring
- XDMAEN- (X-Bus DMA Enable), which enables the X-Bus DMA transfer
- XMODE3- (X-Bus Mode 3), which signifies to the system controller that an X-Bus mode 3 DMA transfer is occurring



(From Figure C-1, Page 8, Coordinate 3A)

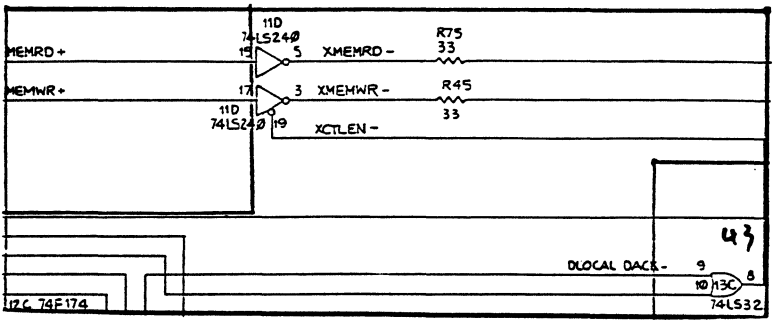
When RQGNT+ is generated from 19B (pin 5), it is synchronized at 18C (pin 3) by XDCLK- before generating as LOCAL DACK+ (Local DMA Acknowledge) at pin 2. LOCAL DACK+ is then NANDed at 15C with XDACKIN+ (pins 13 and 12, respectively). XDACKIN+ was generated as XDACK1IN- at connector J1, pin 118, signifying that the Telephone Manager Module DMA request had been granted.



(From Figure C-1, Page 8, Coordinate 1B)

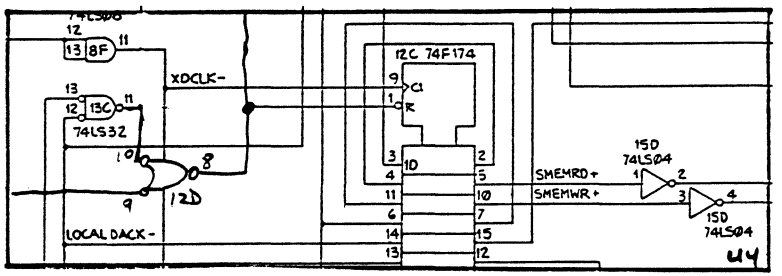
A low signal is, therefore, generated from 15C (pin 11) to 14D (pin 4), enabling XDMAEN-, which connects to the X-Bus via connector J1, pin 8Ø.

In addition, the low signal from 15C (pin 11) is inverted at 15D (pin 10) as IMODE3+ (Internal Mode 3), which is used within the Voice Processor Module for DMA transfer control. IMODE3+ is also inverted at NAND gate 20B and driven as XMODE3- to the system controller via the X-Bus (connector J1, pin 83).



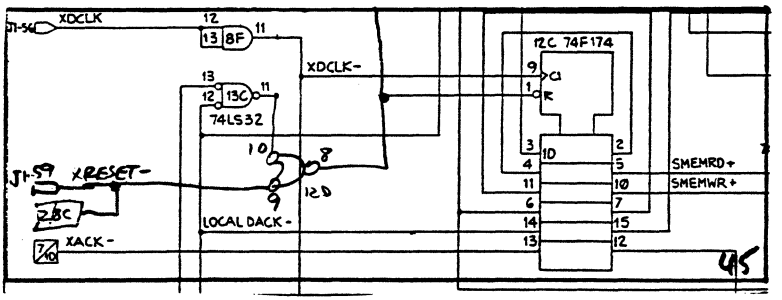
(From Figure C-1, Page 8, Coordinate 5D)

The correct setup time must be generated between the address signals and the read or write command signals at X-Bus Interface Control register 11C. In other words, a 40-nanosecond address setup time is required before the read or write command is generated. The Voice Processor Module, therefore, delays the command lines by a minimum of 250 nanoseconds and a maximum of 500 nanoseconds at buffers at 11D.

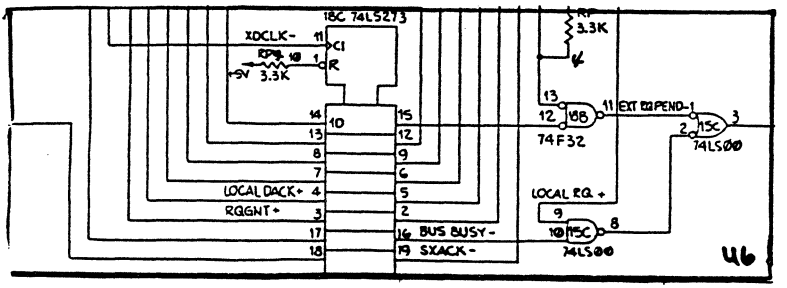


(From Figure C-1, Page 8, Coordinate 6C)

Either LOCAL DACK- or a delayed LOCAL DACK- enables the X-Bus memory read or write signal. As shown, LOCAL DACK- is delayed at 12C by XDCLK- before generating as DLOCAL DACK- (Delayed Local DMA Acknowledge) at pin 15. As shown in the previous window, DLOCAL DACK- is ORed at 13C and driven as XCTLEN- (X-Bus Control Enable) at pin 8. XCTLEN- enables the buffers at 11D (pin 19), which generate either XMEMRD- (X-Bus Memory Read) or XMEMWR- (X-Bus Memory Write) at pin 5 or 3 to the system controller via connector J1, pin 82 or 81, respectively. (Note that LOCAL DACK- also connects directly to pin 10 of 13C, enabling 11D.)



(From Figure C-1, Page 8, Coordinate 6C)

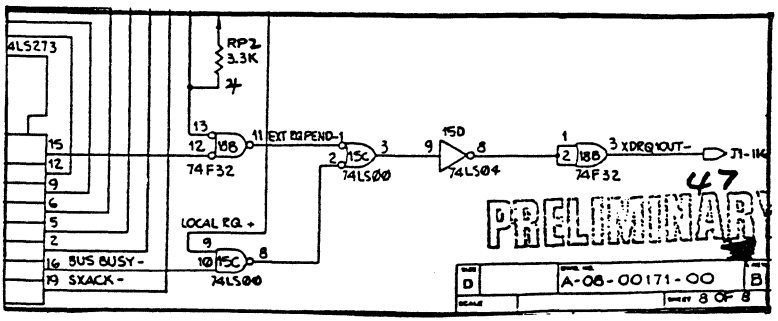


(From Figure C-1, Page 8, Coordinate 3A)

After the read or write is performed, the system contoller issues XACK- (top window), which is asynchronous to XDCLK-. Therefore, XACK- is synchronized and delayed by 250 nanoseconds by XDCLK- at 12C (pin 13) and again at 18C (pin 18)

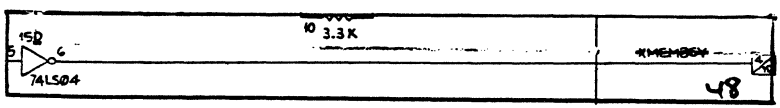
shown in the bottom window, to produce SXACK- (Synchronized Transfer Acknowledge) at pin 19 of 18C.

SXACK- is then generated to OR gate 13C (pin 13) as shown in the previous window, where it is logically NANDed with active-low LOCAL DACK- (pin 12). This causes a low signal at pin 11 that clears the SMEMRD- or SMEMWR- signals, which caused LOCAL RQ+. In addition, the low signal clears the MEMRD+ or MEMWR+ signal that was generated from X-Bus Interface Control register 11C. The data is then accessed via the X-Bus.



From Figure C-1, Page 8, Coordinate 3A)

Since SMEMRD+ or SMEMWR+ is cleared and LOCAL RQ+ becomes inactive, a high signal is generated from pin 8 of NAND gate 15C to pin 2 of 15C. Assuming that another mode 3 master module has not asserted EXTRQPEND- at pin 1 of 15C, a low signal is generated from pin 3 of 15C and inverted at pin 8 of 15D, to deassert XDRQ1OUT- at connector J1, pin 116.

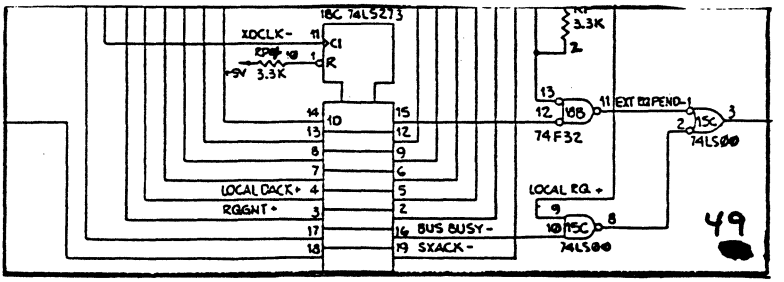


(From Figure C-1, Page 8, Coordinate 3C)

In addition, XMEMBSY- becomes inactive at 15D (pin 6), and generates to pin 3 of the 8051 microprocessor, signifiying the end of the mode 3

master DMA transfer. (See the "Bus Interface Logic" subsection, below, for data read and write operations.)

After the mode 3 master DMA transfer has completed, the Voice Processor Module prevents itself and any other mode 3 master module from accessing the X-Bus. This allows modules that have lower X-Bus priorities to access the X-Bus. This is accomplished by forcing XDRQ1OUT- at connector J1, pin 116, to its inactive state for five DMA clock cycles.



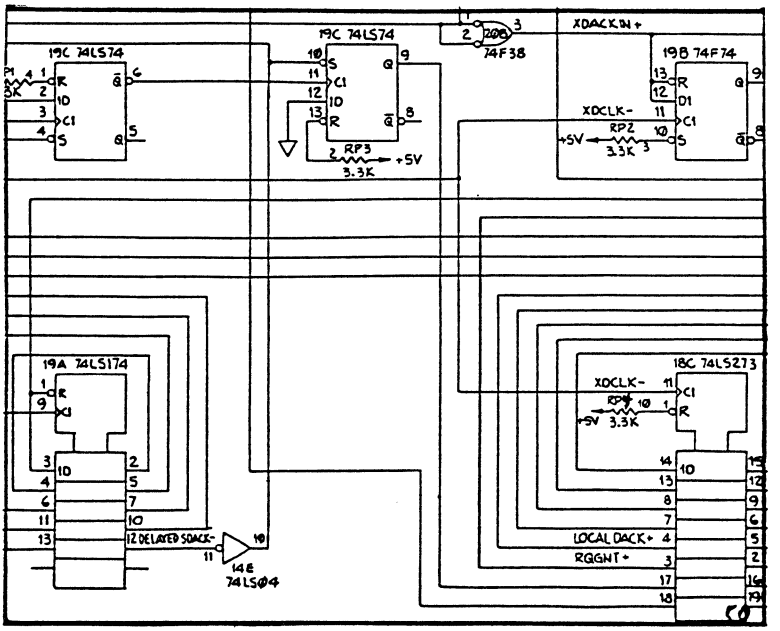
(From Figure C-1, Page 8, Coordinate 4A)

As shown, LOCAL DACK+ is generated to pin 4 of 18C, where it is delayed for five XDCLK- cycles before generating to OR gate 18B. This forces EXTRQPEND- to its inactive state at pin 1. This inactive high signal is logically ORed at NAND gate 15C (pin 1).

Note that the LOCAL DACK+ input at 18C causes EXTRQPEND- to become inactive for six XDCLK- cycles after XDACK1IN- becomes inactive since an inactive RQGNT+ at 18C (pin 3) has to delay the same amount of time as LOCAL DACK+ at 18C.

The Voice Processor Module must also be disabled from the X-Bus for the same amount of time. Therefore, a high signal must be generated to pin 2 of 15C at the same time EXTRQPEND- becomes inactive at pin 1 of 15C.

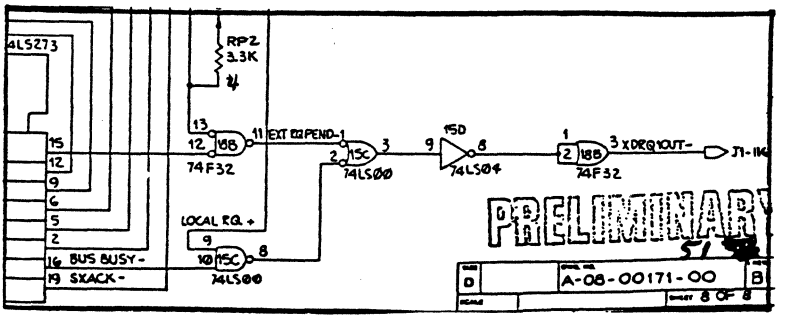
In other words, BUSBSY- (X-Bus Busy) must be asserted at 18C (pin 16), to force a high signal at pin 8 of 15C and, therefore, pin 2 of 15C. This is described in the following paragraphs.



(From Figure C-1, Page 8, Coordinate 5B)

When XDACK1IN- is active, a low signal is generated from pin 8 of D flip-flop 19B to reset 19A at pin 1. Therefore, DELAYEDSDACK- (Delayed Synchronized DMA Acknowledge) is continuously generated from pin 12 of 19A to 14E, where it is inverted (pin 10) and driven to pins 4 and 10 of 19C. Since it is a high signal, it does not affect 19C. Therefore, XDCLK- causes a high signal to generate from pin 6 of 19C, to clock the pin 9 output of 19C (pin 11).

Since pin 12 of 19C is tied to ground, a low signal is generated from pin 9 to 18C (pin 17). At the next XDCLK-, BUS BUSY- is generated from pin 16 of 18C (shown in the window below). This causes the high signal at pin 2 of 15C.



(From Figure C-1, Page 8, Coordinate 3A)

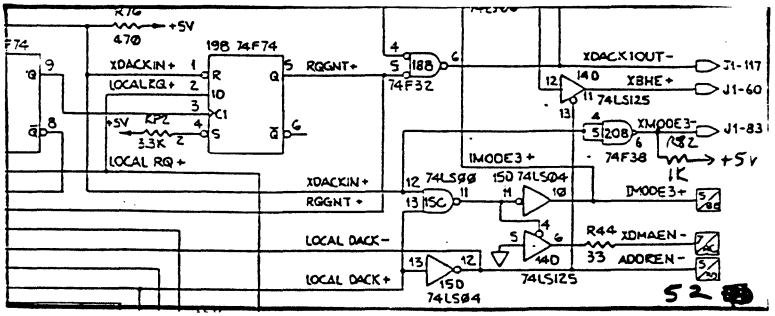
Therefore, a low signal is generated from 15C (pin 3), assuming that EXTRQPEND- is inactive as descrbied in the above paragraphs. This low signal is inverted at 15D (pin 8) and driven at OR gate 18B as an inactive XDRQ1OUT- via connector J1, pin 116.

Because XDRQ1OUT- is inactive, no other X-Bus mode 3 master modules downstream and including the Voice Processor Module can access the X-Bus, allowing other modules with lower DMA priorities access.

Note that when XDACK1IN- becomes inactive, a high signal is generated from pin 8 of 19B (shown in the previous window) to pin 3 of 19A. This high signal is delayed for five XDCLK- cycles before deasserting DELAYEDSACK- at pin 12. Therefore, XDRQ1OUT- remains inactive for five clock cycles.

At the next XDCLK-, a low signal is generated from pin 1Ø of 14E to pins 4 and 1Ø of the D flip-flops at 19C. Therefore, a high signal is generated from pin 9 of 19C to pin 17 of 18C. At the next XDCLK-, BUS BUSY- becomes inactive at pin 16 and the Voice Processor Module can again access the X-Bus.

ADDRESS BUS INTERFACE LOGIC

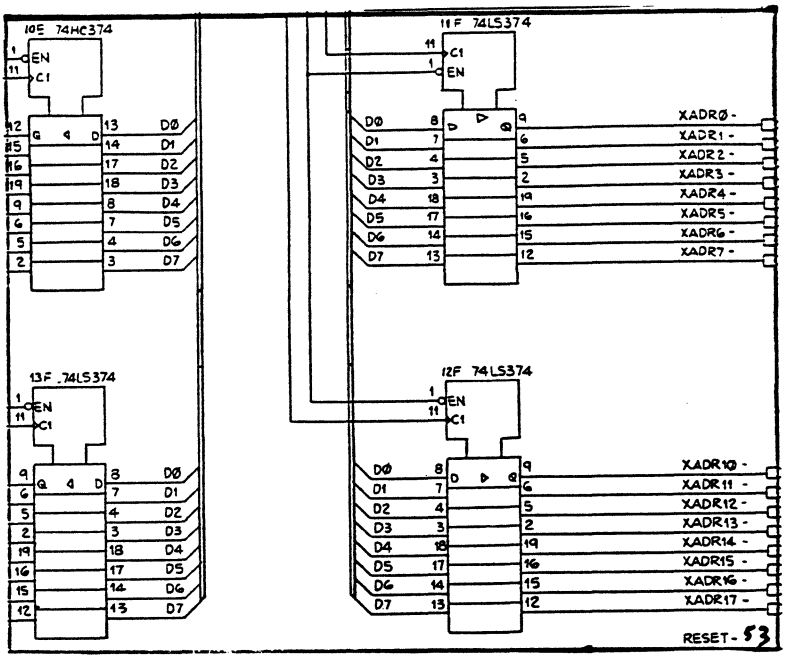


(From Figure C-1, Page 8, Coordinate 2B)

X-BUS/LOCAL ADDRESS BUS

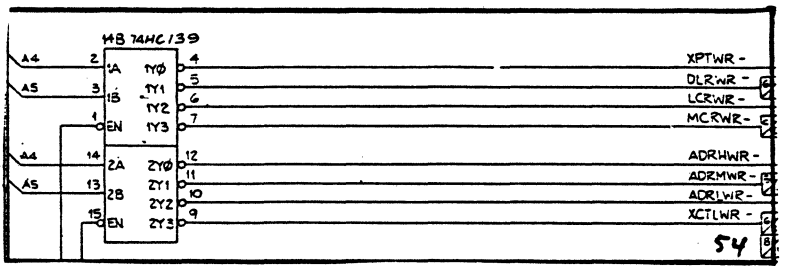
As shown above, LOCAL DACK+ is inverted at 15D (pin 12) as ADDREN- (Address Enable). ADDREN- enables the three X-Bus interface address registers (11F, 13F, and 12F), at pin 1 (shown below). The 8051 microprocessor then writes data to each individual register as described in the "Device Decoding" subsection, below.

See Figure 3-4 for X-Bus read/write timing.

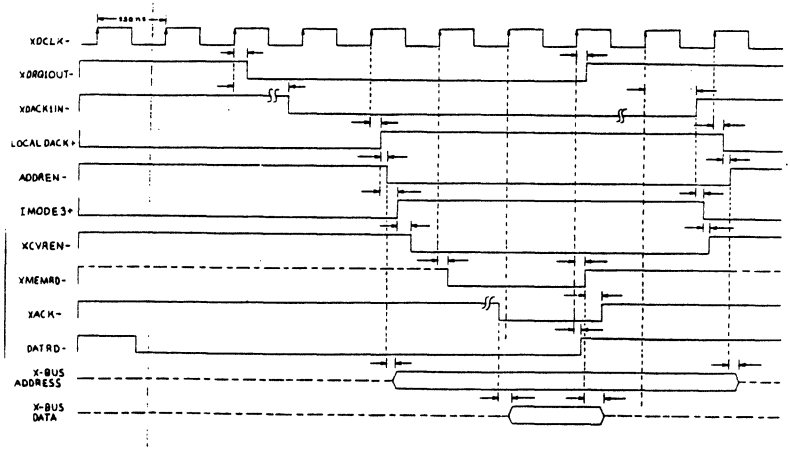


(From Figure C-1, Page 5, Coordinate 3C)

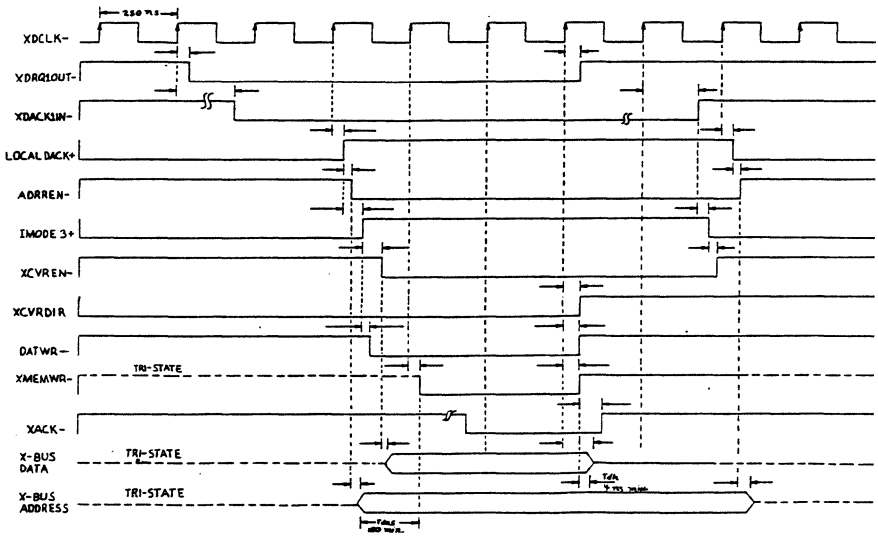
In other words, at the start of the DMA transfer, the applicable 24-bit address must be present on the address bus. Since the 8051 microprocessor contains an 8-bit address bus, it latches each byte separately using the respective external RAM address.



(From Figure C-1, Page 4, Coordinate 3C)



Read



Write

Figure 3-4. X-Bus Read/Write Timing.

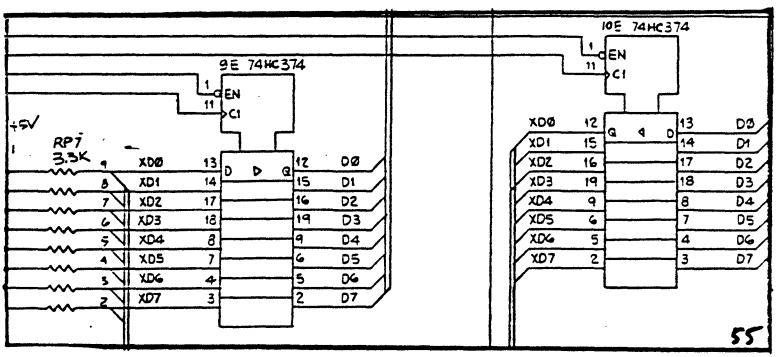
As shown in the above window, 1-of-4 decoder 14B generates the appropriate signal to latch each address byte as follows:

Port (h)	Pin	Signal	Function
60	10	ADRLWR-	Address Low Write: Latches low-byte address at 11F
50	11	ADRMWR-	Address Middle Write: Latches middle-byte address at 13F
40	12	ADRHWR-	Address High Write: Latches high-byte address at 12F

See the "Device Decoding" subsection, below, for decoding logic.

The command lines are summarized as follows:

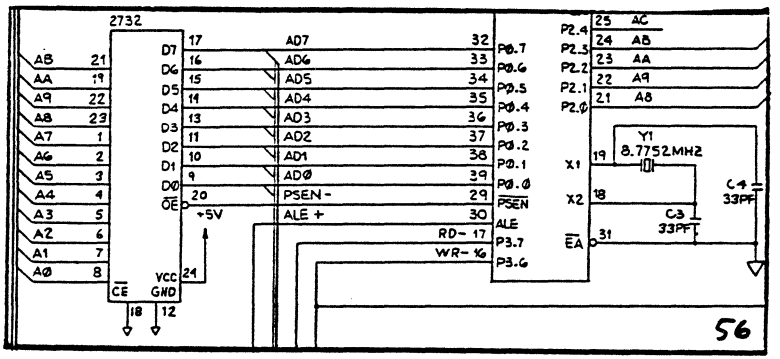
- ADRLWR- places the address on the XADR0- through XADR7- lines via data lines D0+ through D7+
- ADRMWR- places the address on the XADR8- through XADRF- lines via data lines D0+ through D7+
- ADRHWR- places the address on the XADR10- through XADR17- lines via data lines D0+ through D7+



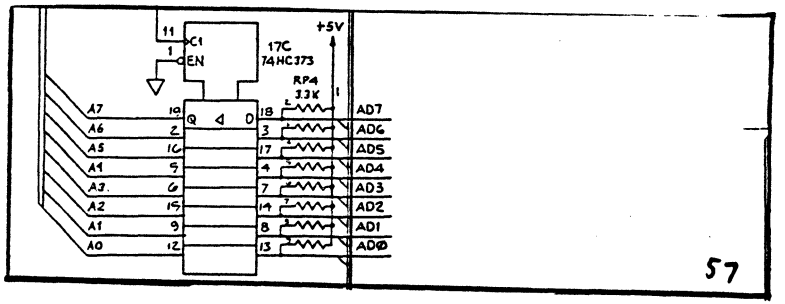
(From Figure C-1, Page 5, Coordinate 5D)

After the three address bytes have been latched, the data byte must be latched at either register 9E or register 10E, depending on whether the data transfer is from memory or to memory, respectively.

8051 MICROPROCESSOR ADDRESS BUS



(From Figure C-1, Page 4, Coordinate 7C)



(From Figure C-1, Page 4, Coordinate 7A)

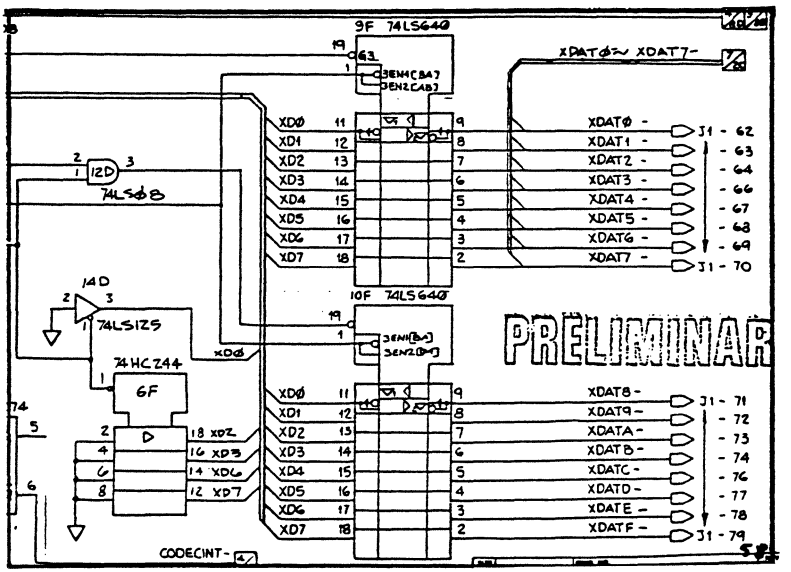
Eight address lines (AD0+ through AD7+) are multiplexed with data lines by the 8051 microprocessor (14A), as shown in the above window. At the beginning of a new machine cycle, indicated by an active ALE+ (Address Latch Enable) at pin 30 of the 8051 microprocessor and pin 11 of address latch 17C (shown in the upper and lower window, respectively), AD0+ through AD7+ stabilize.

At the trailing edge of ALE+, 17C latches the address lines as the local address bus lines AØ+ through A7+.

Note that address lines A8+ through AB+ are generated directly from the 8Ø51 microprocessor.

DATA BUS INTERFACE LOGIC

The Voice Processor Module performs data byte transfers, and therefore chooses whether to transmit or receive data on the high byte or the low byte of the data bus.

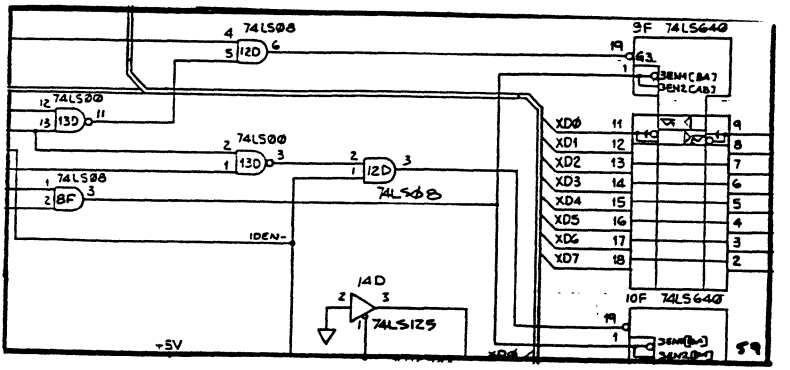


(From Figure C-1, Page 5, Coordinate 2B)

See Figure 3-4, above, for X-Bus read/write timing.

As shown in the above window, transceivers 9F and 1ØF are used as the interface between X-Bus data lines XDATØ- through XDATF- and the internal X-Bus data lines XDØ through XD7.

Note that transceiver 9F interfaces to the low-order data byte, and transceiver 1ØF interfaces to the high-order data byte. Therefore, the X-Bus data word is equivalent to two X-Bus internal data bytes.



(From Figure C-1, Page 5, Coordinate 3B)

As shown in the above window, transceiver 9F is enabled when the following conditions are met:

- BHE- is inactive at NAND gate 13D (pin 12), signifying that the low-order data byte will be transferred.

- IMODE3+ is active at NAND gate 13D (pin 13), signifying that the Voice Processor Module is performing an X-Bus mode 3 DMA transfer.

If the above conditions are met, a low signal is generated from pin 11 of 13D to pin 5 of 12D, forcing a low signal from pin 6 of 12D to pin 19 of 9F, to enable 9F.

Note that IOSELWR- (I/O Select Write) is inactive at 12D (pin 4), signifying that an I/O cycle is not in progress. Therefore, if the low-order byte were not selected, a high signal would be generated from 12D (pin 6), disabling 9F so that the high-order byte could be accessed via 1ØF.

Transceiver 10F is enabled when the following conditions are met:

- IMODE3+ is active at NAND gate 13D (pin 2), signifying that the Telephone Manager Module is performing an X-Bus mode 3 DMA transfer.

- BHE+ is active at NAND gate 13D (pin 1), signifying that the high-order data byte will be transferred.

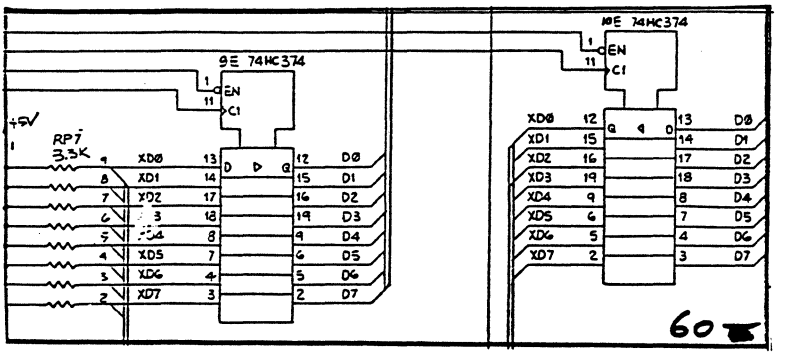
If the above conditions are met, a low signal is generated from pin 3 of 13D to pin 2 of AND gate 12D, forcing a low signal from pin 3 of 12D to enable 10F at pin 19.

Note that during the X-Bus module identification operation, IDEN- (Identification) is generated to AND gate 12D, to enable 10F so the Telephone Manager Module can generate the proper identification number to the Processor Module. (See the "X-Bus Module Identification" subsection, above.)

The direction of data is determined at pin 1 of 9F and 10F, which connect to pin 3 of AND gate 8F. Since an I/O operation is not occurring, XIORD- (X-Bus I/O Read) is inactive at pin 1 of 8F.

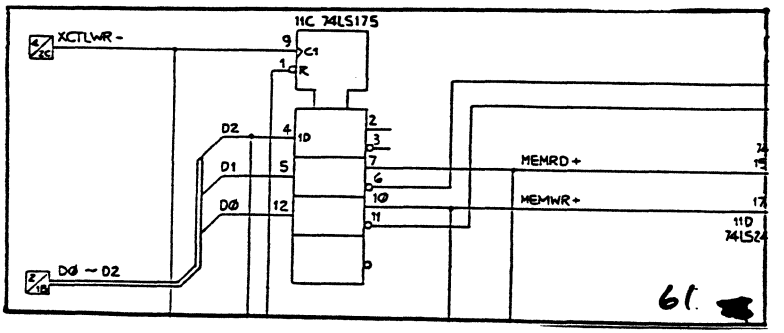
During read cycles, therefore, MEMWR- (Memory Write) is inactive at pin 2 of 8F, and a high signal is generated to pin 1 of 9F and 10F, directing the XDAT0- through XDATF- X-Bus data lines to the XD0 through XD7 module data lines.

During write cycles, MEMWR- forces 8F to generate a low signal to pin 1 of 9F and 10F, directing XD0 through XD7 module data lines to the XDAT0- through XDATF- X-Bus data lines.



(From Figure C-1, Page 5, Coordinage 5D)

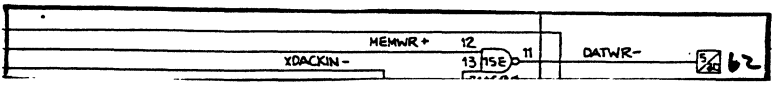
The applicable data byte is latched at buffers 9E and 10E, for read or write cycles, respectively.



(From Figure C-1, Page 8, Coordinate 7D)

Note that 9E is clocked at pin 11 by DATRD- (Data Read), which was generated from pin 6 of X-Bus Interface Control register 11C (shown in the above window) when MEMRD+ is asserted by XCTLWR- as described in the "Control Signals" subsection, above. In addition, 9E is enabled at pin 1 by DATLRD-, which is generated when the 8051 microprocessor reads external address 20h.

During write operations, 10E is clocked at pin 11 by DATLWR-, which is generated when the 8051 microprocessor writes to external address 20h. In addition, 10E is enabled at pin 1 by DATWR- (Data Write), which is generated when MEMWR+ is asserted from 11C as described in the "Control Signals" subsection, above.

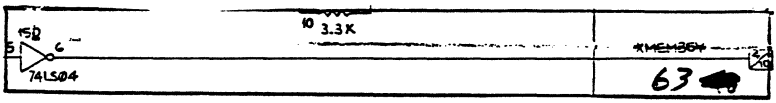


(From Figure C-1, Page 8, Coordinate 2C)

MEMWR+ is NANDed at 15E with IMODE3+, which signifies that the memory write cycle consists of an X-Bus mode 3 DMA transfer. As a result, DATWR- is generated from pin 11 of 15E.

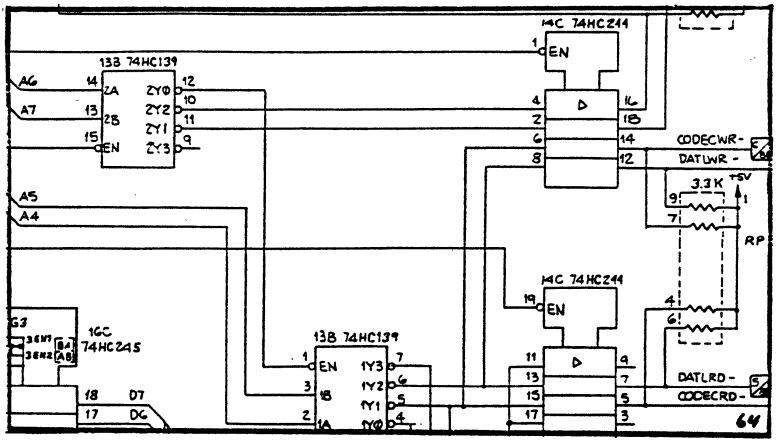
Read Data Latch

Once the data is latched at read register 9E, the data must be generated to the local data lines.



(From Figure C-1, Page 8, Coordinate 3C)

After XMEMRD- becomes inactive, XMEMBSY- also becomes inactive at 15D (pin 6). An inactive XMEMBSY- is, therefore, generated to the 8051 microprocessor at pin 3, signifying that the DMA transfer has been completed, and data is valid at the read register. The 8051 microprocessor then reads address 20h as described in the "Device Decoding" subsection, below.



(From Figure C-1, Page 4, Coordinate 3A)

As shown above, this causes DATLRD- (Data Latch Read) to generate from pin 7 of buffer 14C to read data latch 9E, which enables the data lines. Therefore, internal X-Bus data lines XDØ through XD7 are driven by 9E to local data lines DØ+ through D7+.

In other words, during a read from memory, RD- (Read) is generated from the 8Ø51 microprocessor (pin 17) to enable buffer 14C (pin 19), which drives DATLRD- (Data Latch Read) from pin 7. DATLRD- enables the internal X-Bus data lines onto the local data lines.

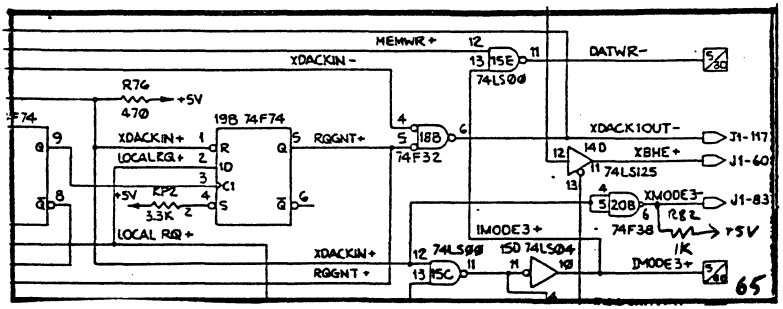
Write Data Latch

Once the data is latched at write register 1ØE, shown in the data must be generated to the X-Bus internal data lines for the DMA transfer.

The 8Ø51 microprocessor latches the data by writing to external RAM address 2Øh as described in the "Device Decoding" subsection, below.

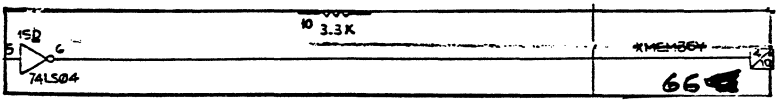
During a write to memory, WR- (Write) is generated from the 8Ø51 microprocessor (pin 16) to enable buffer 14C (pin 1) shown in the above window. This drives DATLWR- (Data Latch Write) from pin 12, to clock the data into 1ØE.

Local data lines D0+ through D7+ are driven by 10E to module data lines XD0 through XD7 when MEMWR+ is generated from X-Bus Interface Control register 11C.



(From Figure C-1, Page 8, Coordinate 2B)

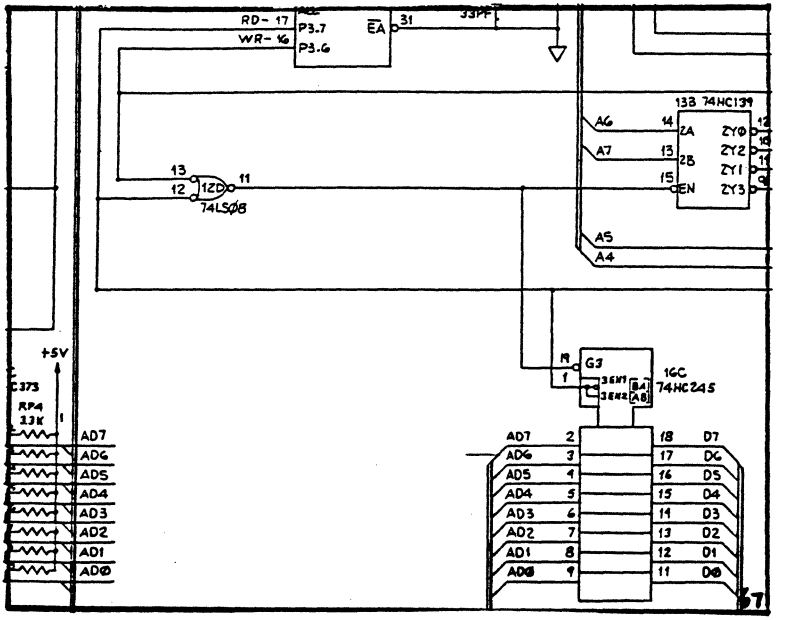
As shown in the above window, MEMWR+ is NANDed at 15E with IMODE3+, which indicates an internal mode 3 master DMA transfer. This causes DATWR- (Data Write) to generate from pin 11 of NAND gate 15E to write data latch 10E, which enables the data lines.



(From Figure C-1, Page 8, Coordinate 3C)

At the end of the DMA transfer, XMEMBSY- becomes inactive at pin 6 of inverter 15D. The inactive XMEMBSY- is generated to pin 3 of the 8051 microprocessor to signify that the mode 3 master DMA transfer has been completed.

8051 MICROPROCESSOR DATA BUS



(From Figure C-1, Page 4, Coordinate 6B)

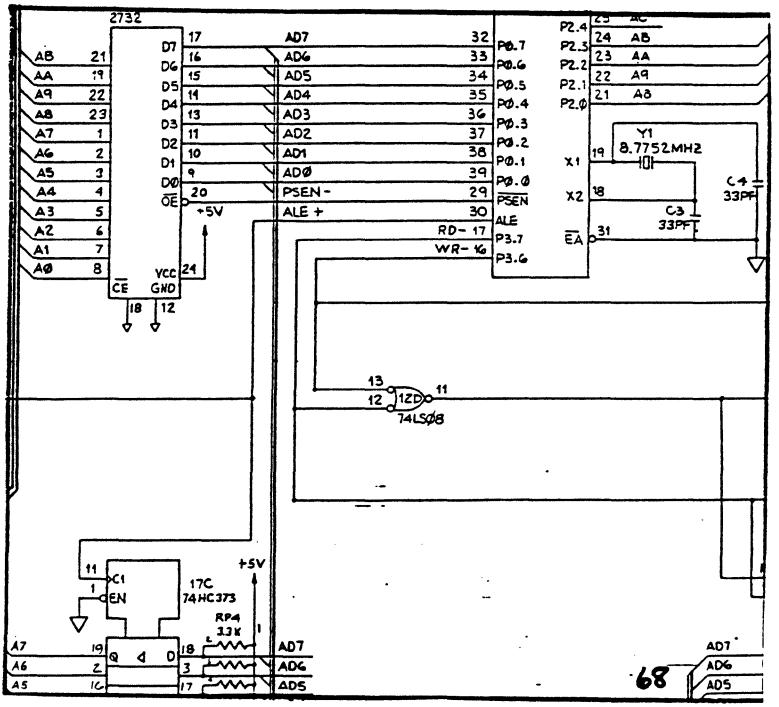
Address/data lines AD0+ through AD7+ are buffered by data transceiver 16C, which generates local data bus lines D0+ through D7+. In other words, data transceiver 16C is used as the interface between local data lines D0+ through D7+ and the 8051 microprocessor data lines AD0+ through AD7+.

As shown above, 16C is enabled at pin 19 when the 8051 microprocessor issues either RD- (Read) or WR- (Write) from pin 17 or 16, respectively.

As shown, RD- or WR- is logically NORed at AND gate 12D (pin 12 or 13, respectively), forcing a low signal at pin 11, and enabling 16C.

Data is directed at pin 1 of 16C. During a read cycle, RD- is active at pin 17 of the 8051 microprocessor and pin 1 of 16C, directing D0+ through D7+ to AD0+ through AD7+. During a write cycle, RD- is inactive and data is directed from AD0+ through AD7+ to D0+ through D7+.

READ-ONLY MEMORY



(From Figure C-1, Page 4, Coordinate 7C)

After an 8051 microprocessor reset condition, local ROM (Read-Only Memory) bootstrapping and self-testing is provided by 2732 EPROM (Erasable Programmable ROM) 15B, as shown in the above window.

Multiplexed address/data bus AD0+ through AD7+ and A8+ through AB+ are used to latch in the addresses of the instructions at the 2732 EPROM.

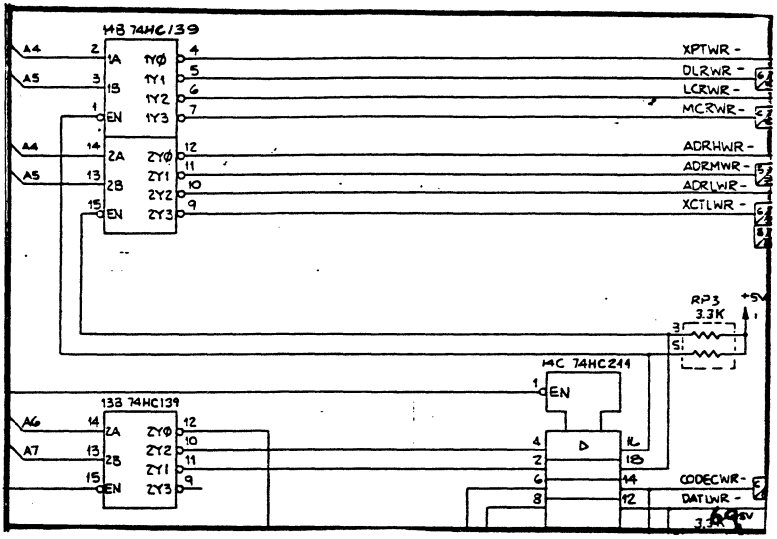
Address lines AD0+ through AD7+ are latched in at buffer 17C, when ALE+ (Address Latch Enable) is generated from the 8051 microprocessor. (Note that the output of 17C is always enabled since pin 1 is tied to ground.)

Simultaneously, address bits A8+ through AB+ are generated from the 8051 microprocessor (pins 21 through 24). Therefore, A0+ through AB+ are all generated to 15B. Then, the 8051 microprocessor asserts PSEN- (Program Store Enable), which enables the output of 15B, allowing the content of the respective address (that is , the instruction) onto the AD0+ through AD7+ data bus to the 8051 microprocessor. Note that EA- (External Address) is tied to ground at pin 31 of the 8051 microprocessor, signifying that the 8051 microprocessor is to fetch instructions at an external ROM.

To summarize, 15B receives the address of an instruction, and then generates the contents of that address to the 8051 microprocessor.

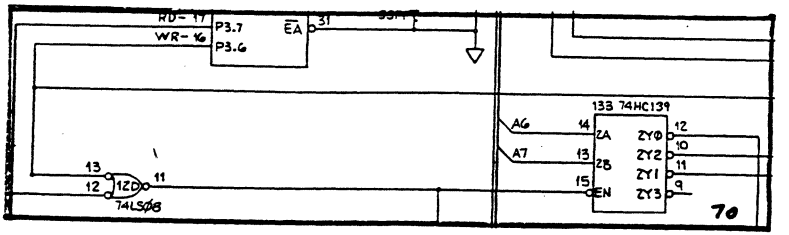
Note that each instruction is generated onto the AD0+ through AD7+ address/data bus at the falling edge of PSEN- and the 8051 microprocessor decodes the instruction on the rising edge of PSEN-.

DEVICE DECODING

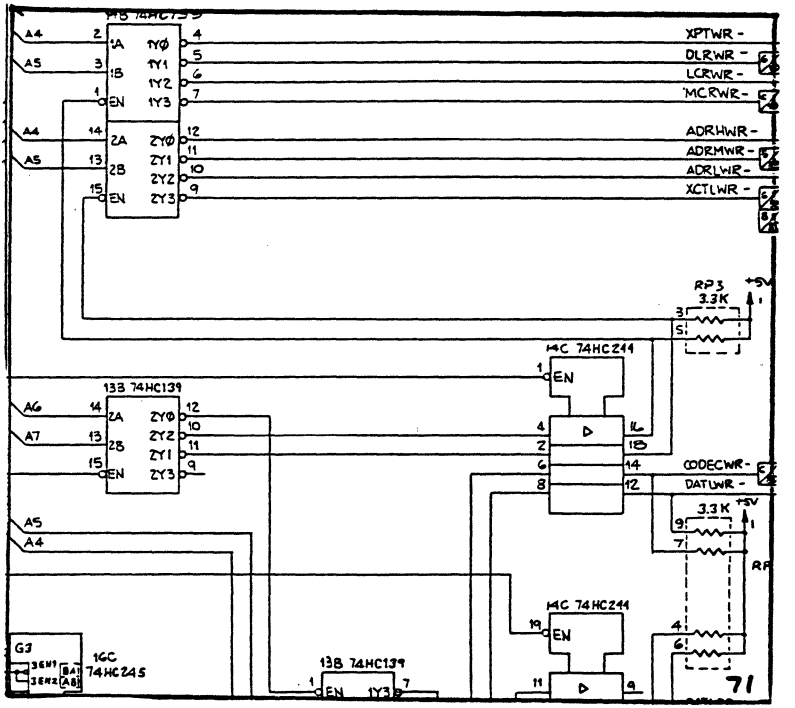


(From Figure C-1, Page 4, Coordinate 4C)

To generate the applicable control and status lines in the Voice Processor Module, the 8Ø51 microprocessor writes or reads the respective external RAM locations via 1-of-4 decoders 14B and 13B, shown in the above window.



(From Figure C-1, Page 4, Coordinate 5B)



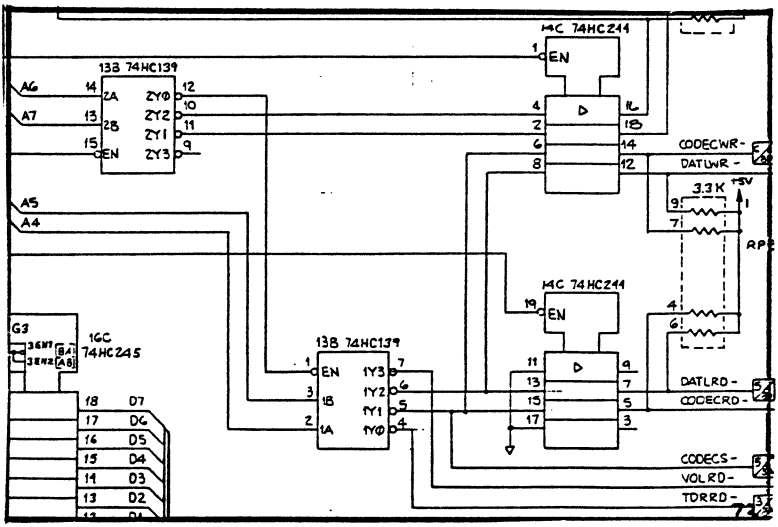
(From Figure C-1, Page 4, Coordinate 4C)

As shown in the top window, the 8051 microprocessor issues a read or write from pin 17 or 16, respectively, which is logically NORed at AND gate 12D at pin 12 or 13, respectively. This

causes a low signal at pin 11 of 12D, which enables 1-of-4 decoder 13B at pin 15. As shown in the bottom window, address lines A6+ and A7+ drive 13B as follows:

A7+	A6+	Function
0	0	Enables pin 1 of 13B (addresses 00h through 30h)
0	1	Enables pin 15 of 14B (addresses 40h through 70h)
1	0	Enables pin 1 of 14B (addresses 80h through 0B0h)
1	1	Unused

Each of these is described in the following paragraphs.



(From Figure C-1, Page 4, Coordinate 4B)

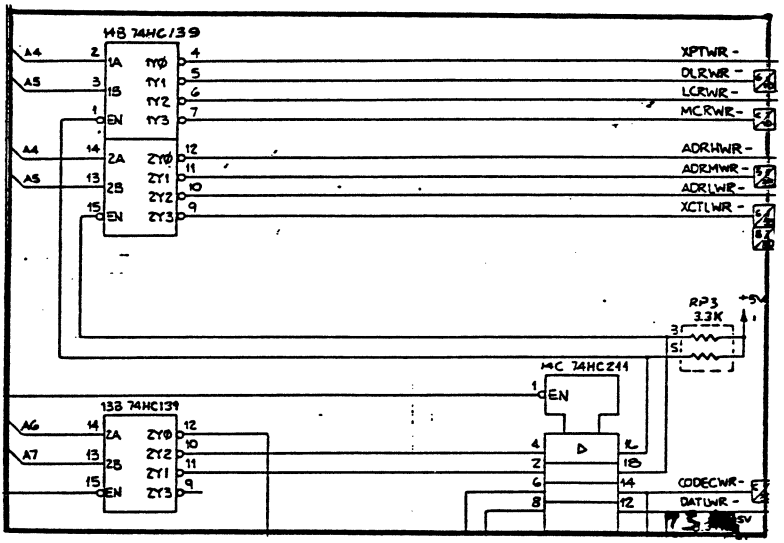
When both A6+ and A7+ are low, 13B is enabled at pin 1, allowing address lines A4+ and A5+ to drive the following:

A5+	A4+	Address (h)	Pin	Function
0	0	00	4	TDRRD- (Tone Detector Register Read): Enables contents of the Tone Detector register onto the 8051 microprocessor data bus
0	1	10	5	CODECS- (CODEC Select): Clears CODEC interrupt to 8051 microprocessor, and acknowledges byte of voice data
1	0	20	6	Clocks read/write data latches, which act as the interface between internal X-Bus data lines and local data lines
1	1	30	7	VOLRD- (Volume Read): Enables contents of the Loudness Level register onto the 8051 microprocessor data bus

Note that CODECS- is also buffered at 14C (pin 15 or 6), to generate CODECRD- or CODECWR-, which enables the CODEC stacker/destacker for 4-bit transfers between the CODEC and the 8051 microprocessor. CODECS-, CODECRD-, and CODECWR- are all described in the "CODEC Logic" and "Stacker/Destacker Logic" subsections, below.

The other registers can be found in the the following subsections:

- The Tone Detector register is described in the "General 8051 Microprocessor External RAM Registers" subsection, below.
- The read/write data latches are described in the "Data Bus Interface Logic" subsection, above.
- The Loudness Level register is described in the "Silence Detection and Volume Control" subsection, below.



(From Figure C-1, Page 4, Coordinate 4C)

When A6+ is active and A7+ is inactive, 14B is enabled at pin 15, allowing address lines A4+ and A5+ to drive the following:

A5+	A4+	Address (h)	Pin	Function
Ø	Ø	4Ø	12	ADRHWR- (Address High Byte Write): Clocks the X-Bus Interface High Byte Address register
Ø	1	5Ø	11	ADRMWR- (Address Middle Byte Write): Clocks the X-Bus Interface Middle Byte Address register
1	Ø	6Ø	1Ø	ADRLWR- (Address Low Byte Write): Clocks the X-Bus Interface Low Byte Address register
1	1	7Ø	9	XCTLWR- (X-Bus Control Load Write): Clocks the X-Bus Interface Control register

These registers can be found in the following subsections:

- All of the X-Bus interface address registers are described in the "Address Bus Interface Logic" subsection, above.
- The X-Bus Interface Control register is described in the "X-Bus Mode 3 Master Logic" subsection, above.

When A6+ is inactive and A7+ is active, 14B is enabled at pin 1 (shown in the above window), allowing address lines A4+ and A5+ to drive the following:

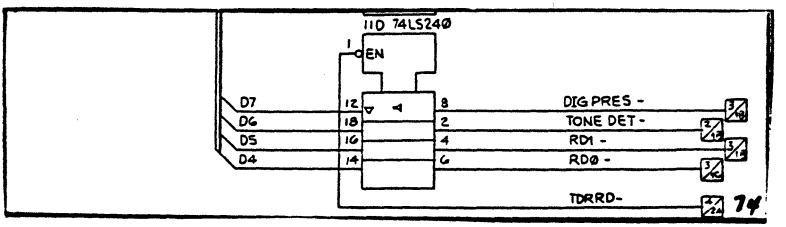
A5+	A4+	Address (h)	Pin	Function
Ø	Ø	8Ø	4	XPTWR- (Crosspoint Write): Clocks crosspoint line and junctor connections
Ø	1	9Ø	5	DLRWR- (DTMF Load Register Write): Clocks DTMF Generator register
1	Ø	ØAØ	6	LCRWR- (Line Control Register Write): Clocks Line Control register
1	1	ØBØ	7	MCRWR- (Modem Control Register Write): Clocks Modem Control register

Each of these can be found in the following subsections:

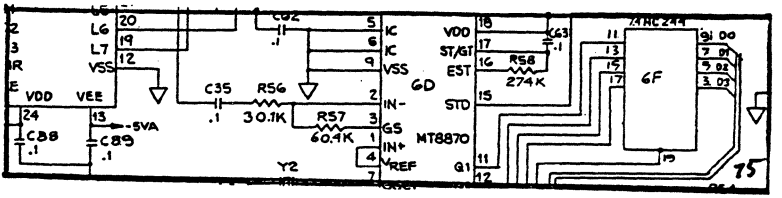
- The crosspoint line and junctor connections are described in the "Crosspoint Matrix Control" subsection, below.
- The remaining registers are described in the "General 8051 Microprocessor External RAM Registers" subsection, below.

GENERAL 8051 MICROPROCESSOR EXTERNAL RAM REGISTERS

Tone Detector Register (Address 00h)



(From Figure C-1, Page 6, Coordinate 2B)



(From Figure C-1, Page 3, Coordinate 3A)

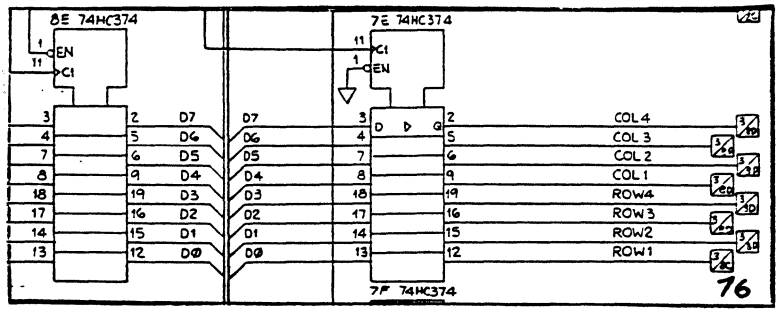
The Tone Detector register, shown in the top window as 11D, and in the bottom window as 6F, is located at external RAM location ØØh and contains the status of the following:

Data Bit	Pin	Function
DØ+ - D3+	5	DTMF Encoding: Contains the encoded DTMF digit from the DTMF receiver (see below)
D4+		RD1- (Ring Detect 1): When set, ring detected for line 1
D5+		RD2- (Ring Detect 2): When set, ring detected for line 2
D6+		TONE DET- (Tone Detect): When set, call progress tone detected (for example, dial tone, busy signal, etc.)
D7+		DIGPRES- (Digit Present): When reset, signifies that a received tone-pair has been detected

DTMF Encoding

Data Bits				
3	2	1	Ø	Digit
Ø	Ø	Ø	Ø	D
Ø	Ø	Ø	1	1
Ø	Ø	1	Ø	2
Ø	Ø	1	1	3
Ø	1	Ø	Ø	4
Ø	1	Ø	1	5
Ø	1	1	Ø	6
Ø	1	1	1	7
1	Ø	Ø	Ø	8
1	Ø	Ø	1	9
1	Ø	1	Ø	Ø
1	Ø	1	1	*
1	1	Ø	Ø	#
1	1	Ø	1	A
1	1	1	Ø	B
1	1	1	1	C

DTMF Generator Register (Address 90h)



(From Figure C-1, Page 6, Coordinate 2C)

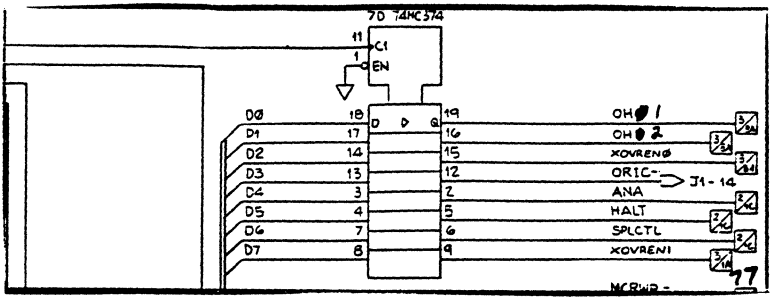
The DTMF Generator register (7E), shown above, is located at external RAM location 90h. The DTMF Generator register is used to input the row and column information to the DTMF generator, which then generates the proper digit. Note that the rows and columns of the register are identical to the rows and columns of a telephone keypad. For example, row 1, column 1 consists of the digit 1, and row 4, column 2, consists of the digit 0.

Digits that correspond to the row and column outputs at pins 2, 5, 6, 9, 12, 15, 16, and 19 of 7E are as follows:

	COL1- (D4+)	COL2- (D5+)	COL3- (D6+)	COL4- (D7+)
ROW1- (D0+)	1	2	3	0Ah
ROW2- (D1+)	4	5	6	0Bh
ROW3- (D2+)	7	8	9	0Ch
ROW4- (D3+)	*	0	#	0Dh

The data bit inputs to 7E are shown above in parentheses. Note that the column 4 digits (that is 0Ah through 0Dh) do not appear on a standard telephone set.

Line Control Register (Address ØAØh)



(From Figure C-1, Page 6, Coordinate 2D)

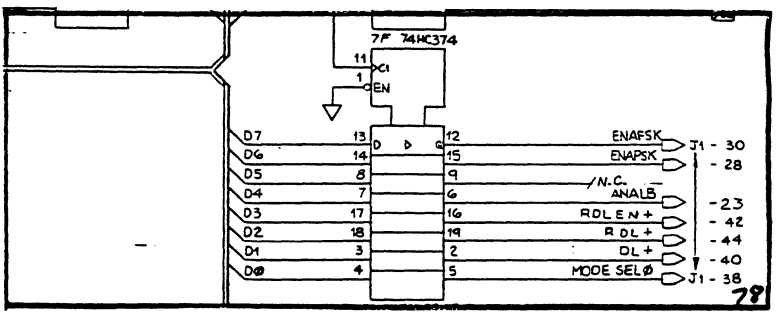
The Line Control register (7D), shown above, is located at external RAM location ØAØh and controls the following:

Data Bit	Pin	Function
DØ+	19	OH1+ (Off-Hook Relay 1): Set to place line 1 off hook
D1+	16	OH2+ (Off-Hook Relay 2): Set to place line 2 off hook
D2+	15	XOVRENØ- (Crossover Enable Ø): See below
D3+	12	ORIG- (Originate/Answer): When reset, places modem in originate mode via connector J1, pin 14; when set, places modem in answer mode via connector J1, pin 14
D4+	2	ANA+ (Analyze/Synthesize): When set, encodes voice via the CODEC; when reset, decodes voice via the CODEC
D5+	5	HALT+ (Halt): When set, halts CODEC; when reset, enables CODEC to run

Data Bit	Pin	Function
D6+	6	SPCTL- (Sample Control): When set, CODEC is sampled at 8 kHz; when reset, CODEC is sampled at 6 kHz
D7+	9	XOVREN1- (Crossover Enable 1): See below

D2+	D7+	Function
Ø	Ø	Enables voice unit across line 1 (power-up default)
Ø	1	Enables voice unit across line 2 (used to save power)
1	Ø	Disables voice unit across both lines
1	1	Enables voice unit across line 2 (not used)

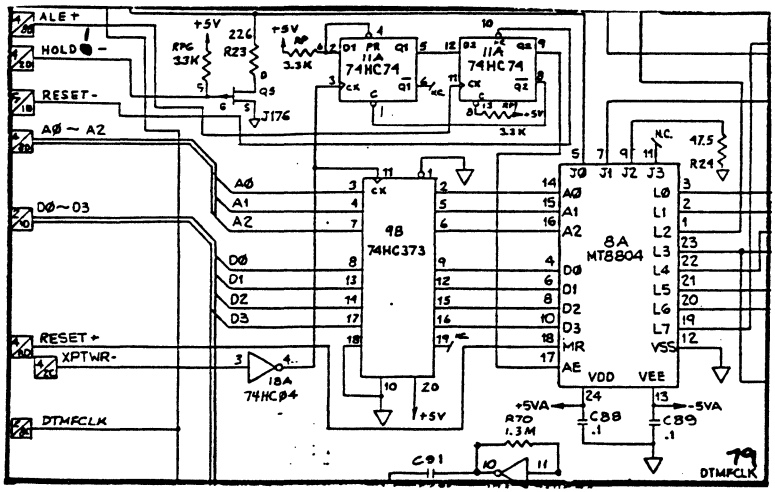
Modem Control Register (Address ØBØh)



(From Figure C-1, Page 6, Coordinate 2B)

The Modem Control register (7F), shown above, is located at external RAM location ØBØh and controls the following:

Data Bit	Pin	Function
DØ+	5	MODE SELØ+ (Mode Select Ø): When set, selects V.22 mode; when reset, selects 1Ø3 (212-A) mode
D1+	2	DL+ (Digital Loopback): When set, sets the local modem to digital loopback mode so that data transmitted from a remote modem to the local modem will be looped back to the remote modem for diagnostics
D2+	19	RDL+ (Remote Digital Loopback): When set, causes the local modem to perform a command sequence to place the remote modem in digital loopback
D3+	16	RDLEN+ (Remote Digital Loopback Enable): When set, enables the local modem to be placed into digital loopback from a remote modem
D4+	6	ANALB+ (Analog Loopback): When set, sets the modem on the Modem board to analog loopback mode so that data transmitted from the 8Ø51 microprocessor to the modem will be transmitted back to the 8Ø51 microprocessor for diagnostics
D5+	9	Not connected
D6+	15	ENAPSK+ (Enable PSK): When set, enables modem for PSK at 12ØØ baud
D7+	12	ENAFSK+ (Enable FSK): When set, enables modem for FSK at 3ØØ baud



(From Figure C-1, Page 3, Coordinate 6B)

The heart of the analog circuitry consists of an MT8804 8 by 4 analog crosspoint switch array. Under control of the 8051 microprocessor, the analog crosspoint switch array switches and connects the various analog functional blocks to their appropriate states at the appropriate times.

The MT8804 8 by 4 analog crosspoint switch array, shown in previous window, allows the connection to either telephone line.

The pin assignments and functions for the MT8804 8 by 4 analog crosspoint switch array are listed in Table 3-2. Timing for the analog crosspoint switch is shown in Figure 3-5.

As shown above, the analog switch array is arranged in eight rows and four columns. The row input/outputs are signified as lines (that is, L0+ through L7+) and the column inputs/outputs are signified as junctors (that is, J0+ through J3+). The lines and junctors interconnect when turned on.

Table 3-2. MT8804 8 By 4 Analog Switch Array 8A Pin Assignments and Functions. (Page 1 of 2)

Pin	Function
1	**Input/Output Line 2 (L2+)** Used as the row input/output for the DTMF generator.
2	**Input/Output Line 1 (L1+)** Used as the row input/output for the modem.
3	**Input/Output Line Ø (LØ+)** Used as the row input/output for the voice unit interface (no extra attenuation).
4, 6, 8, 10	**Control Memory Data Lines (DØ+ Through D3+).** Data bus inputs that determine which junctors will connect to the lines.
5, 7 9, 11	**Input/Output Junctor (JØ+ Through J3+).** Used as the column input/outputs as follows: o JØ used as telephone line 1. o J1 used as telephone line 2. o J2 connects to analog ground. o J3 used for indirect connection (not connected).
12	**Negative Digital Power Supply (VSS-).** Tied to ground.
13	**Negative Analog Power Supply (VEE-).** Tied to -5 VA.
14 - 16	**Control Memory Address Inputs (AØ+ Through A2+).** Used to select the applicable lines.
17	**Control Memory Address Enable (AE+).** Input strobe that enables the RAM.

Table 3-2. MT8804 8 By 4 Analog Switch Array 8A Pin Assignments and Functions. (Page 2 of 2)

Pin	Function
18	**Master Reset (MR+).** Used to initialize 8A; forces all memory locations to their low states and turns off all crosspoint switches.
19	**Input/Output Line 7 (L7+)** Used as the row input/output for the voice unit interface (path adding attenuation).
20	**Input/Output Line 6 (L6+)** Used as the row input/output for the CODEC decoder.
21	**Input/Output Line 5 (L5+)** Used as the row input/output for the CODEC encoder.
22	**Input/Output Line 4 (L4+)** Used as the row input/output for the voice amplifier.
23	**Input/Output Line 3 (L3+)** Used as the row input/output for the DTMF receiver and the call progress tone detector.
24	**Positive Analog/Digital Power Supply (VDD).** Strapped to +5 VA.

The control memory consists of an 8-word by 4-bit RAM. The eight words are selected by A0+ through A2+ (Address Lines 0 Through 2) via an internal address decoder. At the positive edge of AE+ (Address Enable) at pin 17, A0+ through A2+ are latched at the analog crosspoint switch array (8A). The information contained on the A0+ through A2+ lines address one of the L0+ through L7+ lines described above.

Data lines are accessed at D0+ through D3+ (Data Lines 0 Through 3) and are asynchronously written into the control memory when AE+ becomes low at pin 17. The data lines determine which junctors (that is, J0+ through J3+) will connect to the

line. A high level written into a memory cell turns the corresponding crosspoint switch on and a low level turns the crosspoint switch off. Any combination of lines and junctors can be interconnected.

When data is written into control memory, only the crosspoint switches corresponding to the addressed memory words are affected; the remaining crosspoint switches remain in their previous states.

Input/Output lines (LØ+ through L7+) are addressed as follows:

A2+	A1+	AØ+	Addressed Line	Device
Ø	Ø	Ø	LØ+	Voice unit interface no extra attenuation)
Ø	Ø	1	L1+	Modem
Ø	1	Ø	L2+	DTMF generator
Ø	1	1	L3+	DTMF receiver/call progress tone detector
1	Ø	Ø	L4+	voice amplifier
1	Ø	1	L5+	CODEC encoder
1	1	Ø	L6+	CODEC decoder
1	1	1	L7+	Voice unit interface (path adding attenuation)

The addressed lines connect with junctor lines, which are dedicated as follows:

Junctor No.	Device
Ø	Telephone line 1
1	Telephone line 2
2	Direct connection to analog ground
3	Not connected; used for indirect connections

Each of the addressed lines (LØ+ through L7+) can have 16 different combinations of the above junctors connected to it by inputing data to the control memory as follows:

Input Data				Junctors Connected			
D3+	D2+	D1+	DØ+	J3+	J2+	J1+	JØ+
Ø	Ø	Ø	Ø	-	-	-	-
Ø	Ø	Ø	1	-	-	-	*
Ø	Ø	1	Ø	-	-	*	-
Ø	Ø	1	1	-	-	*	*
Ø	1	Ø	Ø	-	*	-	-
Ø	1	Ø	1	-	*	-	*
Ø	1	1	Ø	-	*	*	-
Ø	1	1	1	-	*	*	*
1	Ø	Ø	Ø	*	-	-	-
1	Ø	Ø	1	*	-	-	*
1	Ø	1	Ø	*	-	*	-
1	Ø	1	1	*	-	*	*
1	1	Ø	Ø	*	*	-	-
1	1	Ø	1	*	*	-	*
1	1	1	Ø	*	*	*	-
1	1	1	1	*	*	*	*

*Signifies connection between junctor and addressed line

-Indicates no connection.

Latches 9B and 11A provide the proper setup and hold times for the address and data lines, and the address enable line connecting to 8A.

Since the 8051 microprocessor operates faster than 8A, the latches are used to hold the address lines A0+ through A3+ and data lines D0+ through D3+, and address enable AE+ until 8A is ready to accept them. Therefore, the 8051 microprocessor can continue with its next instruction without waiting for 8A.

The address and data lines, and the address enable, are clocked into 9B and 11A when the 8051 microprocessor writes to external RAM location 80h as described in the "Device Decoding" subsection, above, to generate XPTWR- (Crosspoint Write). XPTWR- is inverted at 18A (pin 4), to clock 9B and 11A.

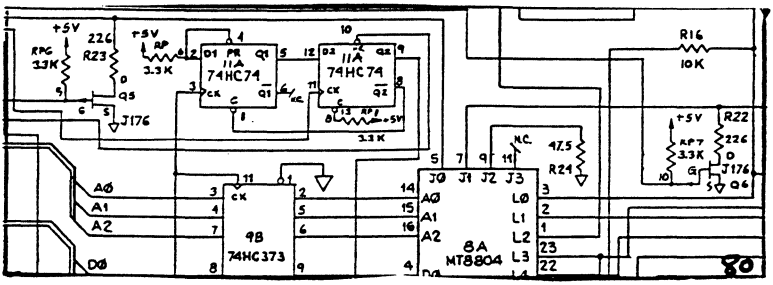
Since pin 1 of 9B is tied to ground, 9B is always enabled.

Note that 11A is strapped to +5 V through 3.3-kilohm resistor RP so that a high signal is generated from pin 5 when clocked at pin 3. This high signal is delayed at pin 12 of 11A until ALE+ is generated from pin 30 of the 8051 microprocessor to pin 11 of 11A. Then AE+ is generated from pin 9 of 11A to pin 17 of 8A, to enable the address lines.

Note that the complement of AE+ is generated from pin 8 of 11A to pin 1 of 11A, clearing AE+ until the next crosspoint write from the 8051 microprocessor.

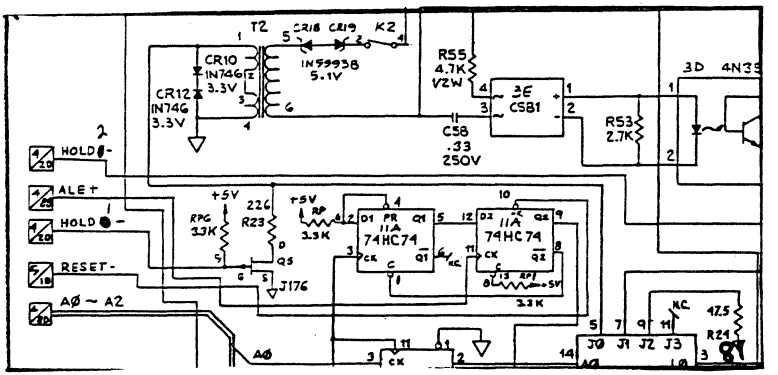
During a power-up or manual reset, or when activity on the X-Bus for the Voice Processor Module has been suspended, as described in the "X-Bus Module Initialization/Identification Logic" subection, above, RESET+, which connects at pin 18 of 8A, resets 8A (that is, disconnects all connections).

ON-HOLD OPERATION

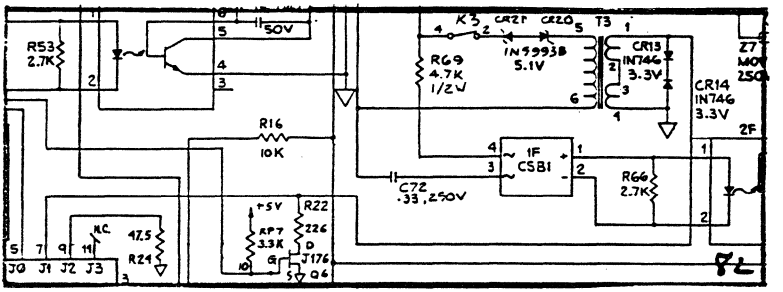


(From Figure C-1, Page 3, Coordinate 6B)

Hold operations occur via 8A and p-channel JFETs Q5 and Q6, which provide proper termination for the secondary of either transformer T2 or T3, depending upon which line is in use. Each line must remain active at all times.



(From Figure C-1, Page 3, Coordinate 7C)



(From Figure C-1, Page 3, Coordinate 4C)

In other words, either relay K2 (upper window) or K3 (lower window), for line 1 or line 2, must remain energized even though the line will be placed on hold. Each line is described below.

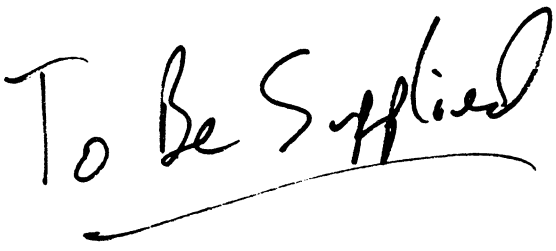
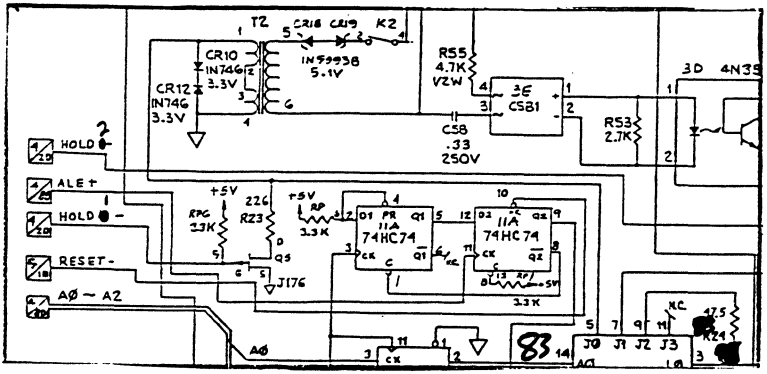


Figure 3-5. Analog Crosspoint Switch Timing.

Line 1 On Hold



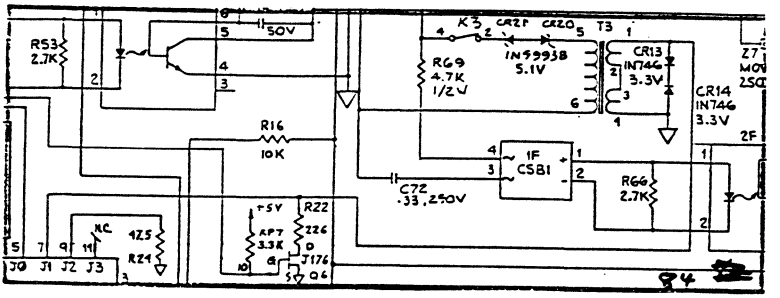
(From Figure C-1, Page 3, Coordinate 7C)

To place line 1 on hold, the voice unit must be disconnected from 8A. For example, if JØ+ at pin 5 of 8A is connected to LØ+ at pin 3 of 8A (signifying that the voice unit interface is connected to line 1), the system must disconnect JØ+ from LØ+. This disconnection, however, causes the wrong termination for the line, and an incorrect AC impedance is reflected.

In other words, pin 1 of T2 floats. Therefore, Q5 is used for proper termination. As shown, HOLD1- (Hold Line 1), which is generated from the 8Ø51 microprocessor as described in the "Processing Unit Logic" subsection, above, turns Q5 on at pin 5 and terminates the line with the 226-ohm resistor at R23, plus a negligible resistance from Q5.

Line 1, which is still active, therefore contains no voice activity.

Line 2 On Hold



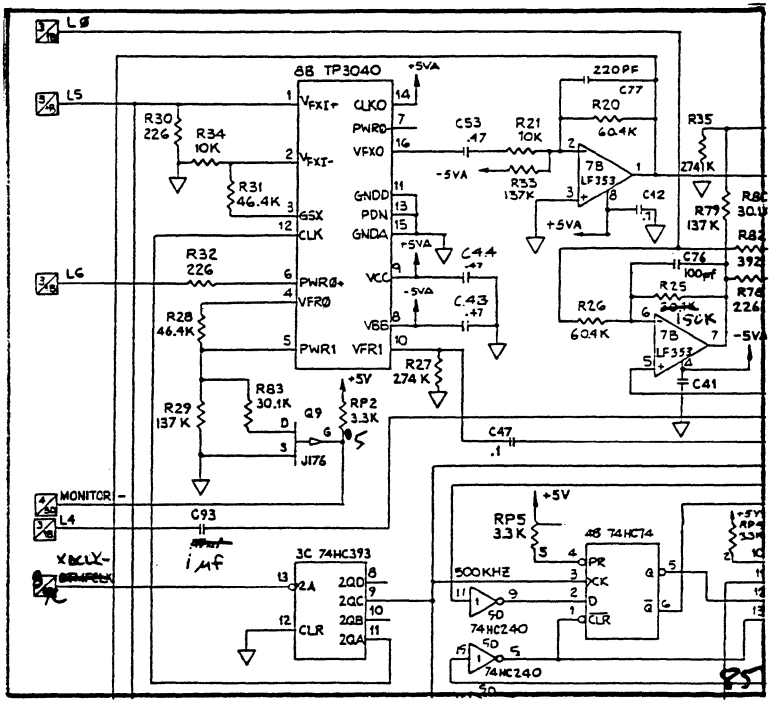
(From Figure C-1, Page 3, Coordinate 4C)

To place line 2 on hold, the voice unit must be disconnected from 8A. For example, if J1+ at pin 7 of 8A is connected to LØ+ at pin 3 of 8A (signifying that the voice unit interface is connected to line 2), the system must disconnect J1+ from LØ+. This disconnection, however, causes the wrong termination for the line, and an incorrect AC impedance is reflected.

In other words, pin 1 of T3 floats. Therefore, Q6 is used for proper termination. As shown, HOLD2- (Hold Line 2), which is generated from the 8Ø51 microprocessor as described in the "Processing Unit Logic" subsection, above, turns Q6 on at pin 1Ø and terminates the line with the 226-ohm resistor at R22, plus a negligible resistance from Q6.

Line 2, which is still active, therefore contains no voice activity.

PULSE CODE MODULATION FILTERING



(From Figure C-1, Page 2, Coordinate 7D)

The TP3040 monolithic filter (8B), shown in the top window, band-limits voice input for CODEC encoding and also filters the decoded CODEC output.

As shown, 8B operates at 1.8-MHz. XDCLK- enables 4-bit binary counter 3C at pin 13 (shown in the above window), which asserts a 1.8-MHz pulse at pin 11. This pulse connects to 8B at pin 12.

The pin assignments and functions for the TP3040 PCM monolithic filter are listed in Table 3-3.

Table 3-3. TP3040 PCM Monolithic Filter 8B Pin Assignments and Functions. (Page 1 of 2)

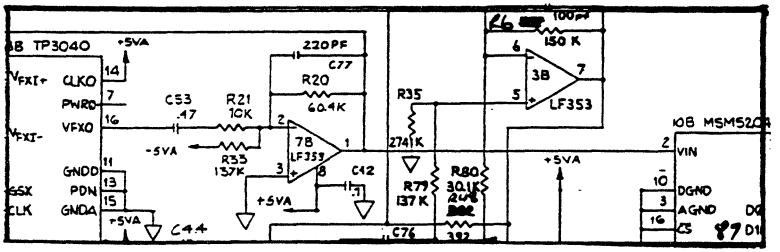
Pin	Function
1	**Noninverting Filter Input (VFXI+).** Noninverting input to the transmit filter stage.
2	**Inverting Filter Input (VFXI-).** Inverting input to the transmit filter stage.
3	**Gain Adjustment (GSX).** Output used for gain adjustments of the transmit filter.
4	**Receiver Filter Output (VFRO).** Receive filter output that drives pin 5.
5	**Power Input (PWRI).** Input to the receive filter differential power amplifier.
6	**Noninverting Power Output (PWRO+).** Noninverting output of the receive filter differential power amplifier.
7	Unused.
8	**Negative Power Supply (VBB-).** Strapped to -5 V.

Table 3-3. TP3040 PCM Monolithic Filter 8B Pin Assignments and Functions. (Page 2 of 2)

Pin	Function
9	**Positive Power Supply (VCC+).** Strapped to +5 V.
10	**Receive Filter Input (VFRI).** Input for the receive filter stage.
11	**Digital Ground (GNDD).** Input to which all digital signals are referenced; tied to ground.
12	**Clock (CLK).** 1.8-MHz input clock.
13	**Power Down (PDN).** Unused; tied to ground.
14	**Clock Select (CLK0).** Strapped to +5 V to select internal counter of 2048 kHz.
15	**Analog Ground (GNDA).** Input to which all analog signals are referenced; tied to ground.
16	**Transmit Filter Output (VFXO).** Output of the transmit filter stage.

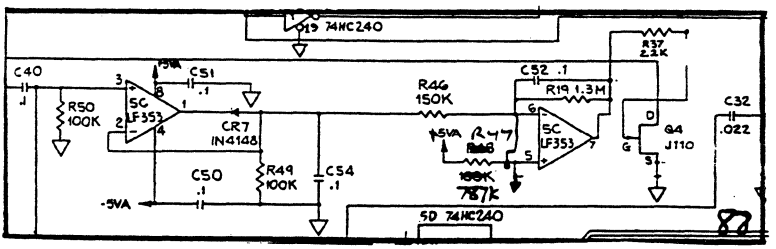
VOICE ENCODING

During voice encoding, voice information is generated from analog crosspoint switch array 8A at pin 21 of L5+ to pin 1 of 8B, where it is filtered and limited. All frequencies below 200 Hz and above 3.2 kHz are attenuated so only frequencies within this pass band can pass through.



(From Figure C-1, Page 2, Coordinate 6D)

Since 8B operates at +5 V and -5 V, the output at pin 16 varies about 0 V. The input of MSM5204 analog-to-digital converter 10B, however, operates from power supplies consisting of 0V to +5 V. Therefore, the input of 10B must be shifted to a midpoint equal to about 2.2 V. This is accomplished by operational amplifier 7B, which is connected in an inverting configuration. Operational amplifier 7B amplifies and provides level shifting between the output of 8B and the input of 10B. The 137-kilohm resistor at R33 biases the output of 7B at pin 1 to about 2.2 V. In addition, 0.47-microfarad capacitor C53 isolates DC voltage.



(From Figure C-1, Page 2, Coordinate 6B)

Note that an automatic gain control (AGC) circuit, which provides feedback and loop control, is built around two operational amplifiers at 5C and an N-channel JFET at Q4.

The input to analog-to-digital converter 10B (pin 2) is sampled by the AGC circuitry and a DC-controlled voltage is generated at the gate of Q4 to control the resistance of Q4. In other words, Q4 acts as a voltage-controlled resistor and appears in parallel with the 226-ohm resistor at R30. Note that R30 connects to the voice input of 8B that will be encoded.

If the signal level is high at operational amplifier 7B (pin 1), the resistance of Q4, which is in parallel with R30, becomes low to attenuate the signal.

If the signal level is low at 7B (pin 1), the resistance of Q4 becomes high, and the circuit does not attenuate. In other words, Q4 looks like an open circuit in parallel with R30.

The first half of operational amplifier 5C acts as a negative-peak detector. In other words, the output at pin 1 follows the negative peaks of the input signals to detect amplitude. Note that the 0.1-microfarad capacitor at C54 and the 100-kilohm resistor at R49 ensure that the circuit detects low-level negative peaks as well as high-level negative peaks.

When the signal at pin 1 of 5C consists of a negative voltage, diode CR7 turns on to allow C54 to charge and store the sample. When the signal at pin 1 of 5C consists of a positive voltage, CR7 turns off, and C54 discharges through R49. This leakage allows the circuit to follow variations in low-level AC signals.

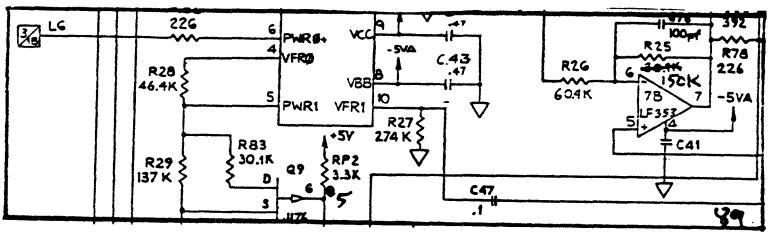
The second half of 5C, which consists of an inverting differential amplifier, adds gain to the circuit and filters DC voltage.

The 1.3-Megohm resistor at R19 and the 150-kilohm resistor at R46 determine the gain. The combination of 0.1-microfarad capacitor at C52, and R19, filter the voltage for a smoother signal that is used as a DC-controlled voltage at the gate of Q4.

The 1ØØ-kilohm resistor at R47 provides a negative DC offset of -4 V at the output of 5C (pin 7). When the signal from pin 1 of 7B is low, Q4 is turned off by the -4 V. As the signal amplitude increases, the output of 5C (pin 7) increases from -4 V toward Ø V. When the voltage reaches Ø V, Q4 is completely turned on and, therefore, Q4 provides a low resistance (about 12 ohms).

Note that 2.2-kilohm resistor at R37 is in series with the gate of Q4 to add linearity to the device.

VOICE DECODING

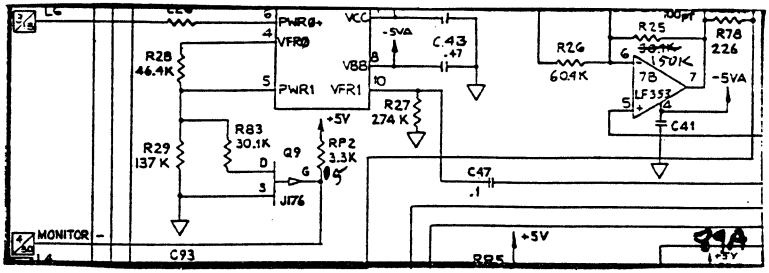


(From Figure C-1, Page 2, Coordinate 7C)

During voice decoding, voice information is generated from the CODEC at pin 18 to 8B (pin 1Ø), where the stairstep waveform is internally filtered and smoothed before generating from the noninverting power output of 8B (pin 6) as L6+. Note that L6+ is generated to the analog crosspoint switch array where it can be switched to any junctor. (See the "Crosspoint Matrix Control" subsection.)

The Ø.1-microfarad capacitor at C47 isolates DC voltage and couples AC voltage to 8B.

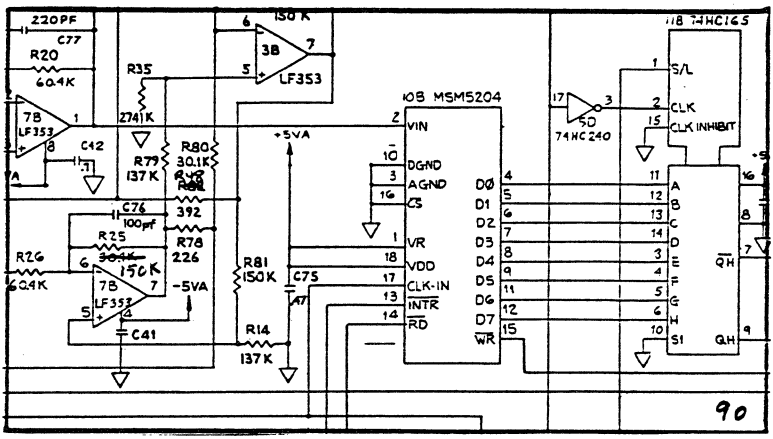
VOICE SCREENING (MONITORING)



(From Figure C-1, Page 2, Coordinate 7C)

When the call screening (monitor) function of the answering machine is used, p-channel JFET Q9 adjusts the gain of the receive filter of 8B. To accomplish this, the 8051 microprocessor generates MONITOR- (Monitor) from pin 15 to the gate of Q9 (pin 9), which appears in parallel with the 137-kilohm resistor at R29. This reduces the gain of the receive filter for proper operation of the monitor function.

ANALOG-TO-DIGITAL CONVERSION



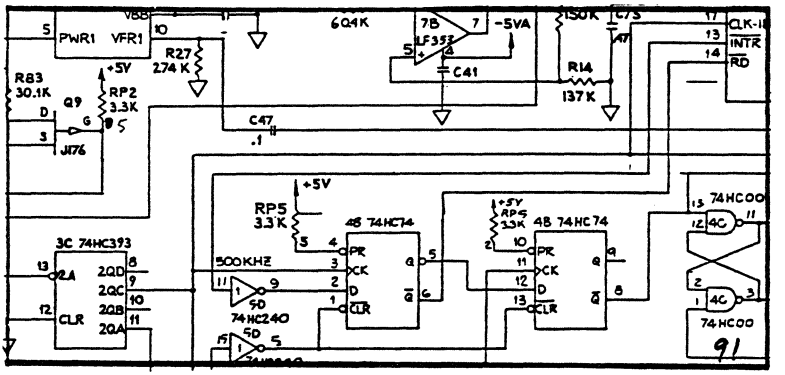
(From Figure C-1, Page 2, Coordinate 4D)

During the voice encoding process, the MSM5204 analog-to-digital converter (10B), shown in the above window, converts an analog signal to a digital byte.

The pin assignments and functions for the MSM5204 8-bit analog-to-digital converter are listed in Table 3-4.

The filtered amplified output at pin 1 of operational amplifier 7B (described in the "Pulse Code Modulation Filtering Logic" subsection, above) generates to pin 2 of 10B, which contains an internal sample and hold circuit in addition to the analog-to-digital converter.

The internal sample and hold circuit samples the signal and holds it for a certain period of time so the analog-to-digital converter has enough time to convert the sample to an 8-bit output at pins 4 through 9, 11, and 12. Without the internal sample and hold circuit, the voice signal would change before the analog-to-digital conversion since voice signals constantly change in amplitude.

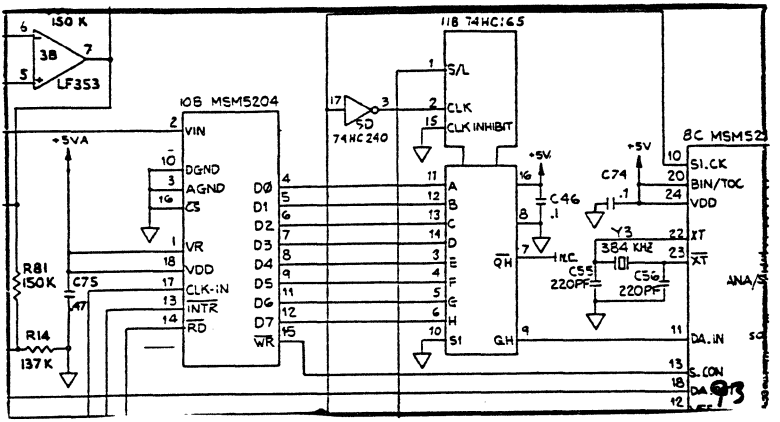


(From Figure C-1, Page 2, Coordinate 6C)

Note that 10B is referenced by a 447-kHz signal (pin 17), which is generated from 4-bit binary counter 3C (pin 9). Note that 3C is enabled at pin 13 by XDCLK-.

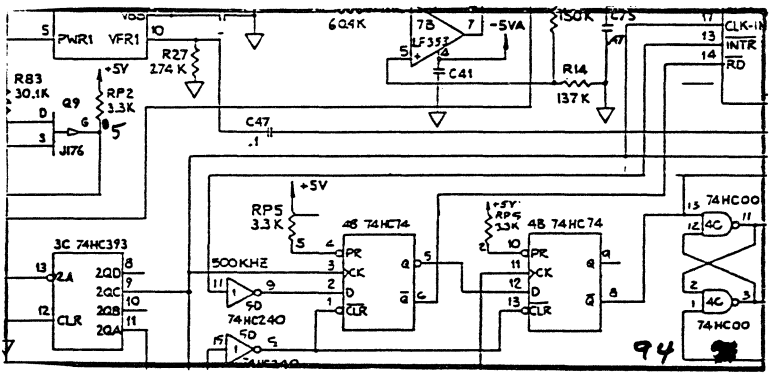
Table 3-4. MSM52Ø4 8-Bit Analog-to-Digital Converter 1ØB Pin Assignments and Functions.

Pin	Function
1	**Reference Supply (VR+).** Strapped to +5 V.
2	**Analog Input (VIN).** Analog input signal.
3	**Analog Ground (AGND-).** Tied to ground.
4 - 9, 11, 12	**Data Lines (DØ+ Through D7+).** Tristate output of converted data.
1Ø	**Digital Ground (DGND-).** Tied to ground.
13	**Interrupt (INTR-).** Active-low output that signifies the end of the conversion; indirectly causes pin 1 of 11B to become low so the data byte can be shifted to the CODEC.
14	**Read (RD-).** Active-low input that accesses the data byte via DØ+ through D7+.
15	**Write (WR-).** Active-low input that starts the conversion; connected to the CODEC.
16	**Chip Select (CS-).** Tied to ground to enable 1ØB.
17	**Clock In (CLKIN+).** 447-kHz clock input.
18	**Power Supply (VDD+).** Strapped to +5 V.



(From Figure C-1, Page 2, Coordinate 4D)

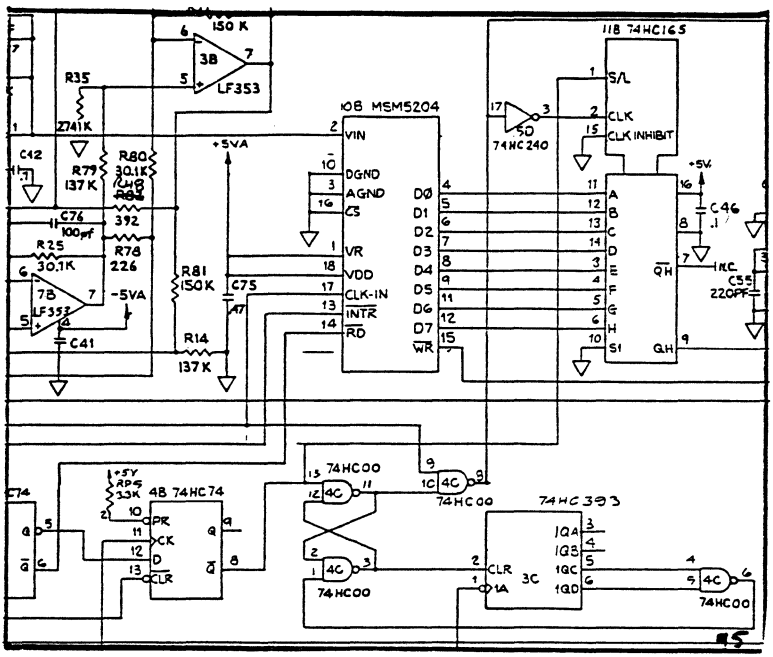
To start the conversion, a low signal is generated from pin 13 of the CODEC (8C) to the WR- (Write) input of 10B (pin 15).



(From Figure C-1, Page 2, Coordinate 6C)

At the end of conversion, a low signal is generated from the INTR- (Interrupt) output of 1ØB (pin 13), signifying the end of conversion. This low signal is inverted at 5D (pin 9) and driven to D flip-flop 4B (pin 2), where it is delayed one clock cycle to give 1ØB enough time to present the encoded analog signal at the output. Therefore,

one clock cycle later, a low signal is generated from pin 6 of 4B to the RD- (Read) input of 10B (pin 14), which allows access of the data byte that has been converted via the D0+ through D7+ lines.



(From Figure C-1, Page 2, Coordinate 4D)

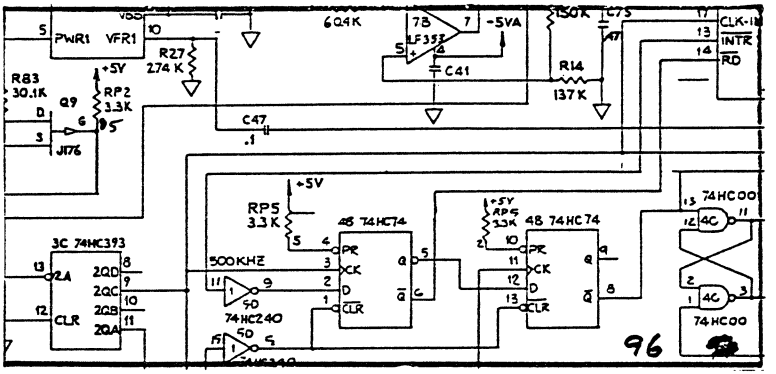
In addition, a high signal is generated from pin 5 of 4B to pin 12 of 4B causing a low signal to generate from pin 8. This low signal is generted to 11B (pin 1), to enable the load of 11B.

An 8-bit binary output is then generated to shift register 11B, which acts a parallel-to-serial converter. Each bit, starting with D7+ and ending with D0+, is serially shifted out of 11B at pin 9 to the CODEC.

After 11B is loaded, a high signal at pin 8 of 4B is generated to 11B (pin 1), causing 11B to start shifting as per the CLK input at pin 2.

Note that the CLK input is referenced to a 447-kHz pulse that connects to NAND gate 4C (pin 9). The pin 1Ø input of 4C determines the state of the clock. When pin 1Ø is active at 4C, the clock generates from pin 8 of 4C to gate 5D, where it is inverted (pin 3) and driven to 11B (pin 2). When pin 1Ø is inactive, the clock input is disabled.

Four-bit binary counter 3C and the other NAND gates at 4C are configured to allow the 447-kHz clock for 12 states for compatibility with the CODEC. In other words, after the byte of data is generated from 11B to the CODEC, four low bits are generated from 11B to the CODEC. This is described in the following subsection.



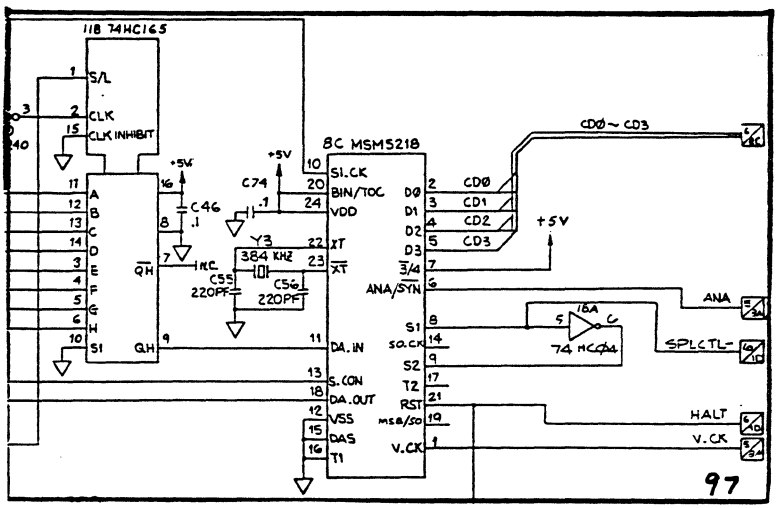
(From Figure C-1, Page 2, Coordinate 6B)

Note that the D flip-flops at 4B clear when the 8Ø51 microprocessor sets the HALT+ (Halt) data bit (that is, D5+) of the Line Control register at 7D located at external RAM location ØAØh as described in the "Device Decoding" subsection, above. As shown in the window above, HALT+ is inverted at 5D (pin 5), to clear 4B (pins 1 and 13), which disables the RD- input of 1ØB (pin 14). In addition, HALT+ resets the CODEC at pin 1.

CODEC LOGIC

The CODEC consists of an MSM5218 speech analyzer/synthesizer featuring the Adaptive Differential Pulse Code Modulation (ADPCM) method of data compression. During the analysis (encoding) stage, serial PCM data compresses to 4-bit parallel ADPCM data. In addition, during the synthesis (decoding) stage, PCM data is synthesized from ADPCM data. The PCM data is output via an internal 10-bit digital-to-analog converter for an analog output signal.

The pin assignments and functions for the MSM5218 ADPCM speech analysis/synthesis IC are listed in Table 3-5. ADPCM CODEC timing is shown in Figure 3-6.



(From Figure C-1, Page 2, Coordinate 2D)

Note that the CODEC (8C) resets when the 8051 microprocessor sets the HALT+ (Halt) data bit (that is, D5+) of the Line Control reigster located at external RAM location 0A0h, as described in the "Device Decoding" subsection, above. As shown in the above window, HALT+ connects to 8C at pin 21. In addition, HALT+ is inverted at 5D (pin 5), to clear D flip-flops at 4B (pins 1 and 13), which disables the RD- input of the analog-to-digital converter (pin 14) as described in the previous subsection.

Table 3-5. MSM5218 ADPCM Speech Analysis/Synthesis IC 8C Pin Assignments and Functions. (Page 1 of 2)

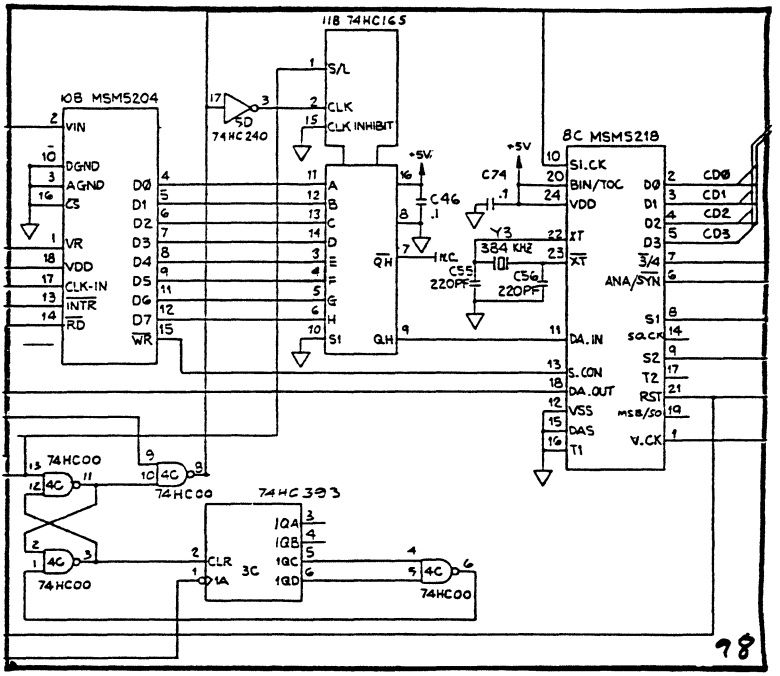
Pin	Function
1	**Variable Clock (V.CK).** An 8-kHz or 6-kHz output, depending upon the sampling frequency selected by the S1 and S2 inputs (pins 8 and 9); used to synchronize the stacker/destacker to 8C.
2 - 5	**CODEC Data Lines (CDØ+ Through CD3+).** Bidirectional ADPCM data port; connects to the stacker/destacker.
6	**Analyze/Synthesize (ANA+/SYN-).** When set, this input selects the analysis function (encode); when reset, selects the synthesis function (that is, decode).
7	**3-Bit/4-Bit Data (3-/4+).** Strapped to +5 V to use 4-bit ADPCM data.
8, 9	**Status Lines 1 and 2 (S1 and S2).** Inputs used to select the sampling frequency or external mode as follows: S1 S2 Sampling Frequency Ø 1 6 kHz 1 Ø 8 kHz Note that the lower frequency signifies a lower bit-rate representation to lessen the storage requirement of memory
1Ø	**Serial Input Clock (SI.CK).** Clock input used for clocking serial PCM data from an external analog-to-digital converter into an internal 12-bit shift register.
11	**Data In (DA.IN).** Serial PCM data input.

Table 3-5. MSM5218 ADPCM Speech Analysis/Synthesis IC 8C Pin Assignments and Functions. (Page 2 of 2)

Pin	Function
12	**Ground (VSS-).** Tied to ground.
13	**Start of Conversion (S.CON-).** Output that signifies the start of conversion.
14	Unused.
15	**Data Selector (DAS).** Tied to ground to select an analog signal output.
16	**Test 1 (T1).** Unused; tied to ground.
17	**Test 2 (T2).** Unused; open.
18	**Data Out (DA.OUT).** Analog signal output.
19	Unused.
20	**Binary/Two's Complement (BIN+/TOC-).** Strapped to +5 V for binary operations.
21	**Reset (RST+).** Active-high input that initializes the internal circuitry.
22, 23	**Oscillator Inputs (XT+ and XT-).** Inputs from 384-kHz crystal oscillator that provide the reference clock.
24	**Power Supply (VDD+).** Strapped to +5 V (nominal).

VOICE ANALYSIS (ENCODING)

The input at pin 11 of the MSM5218 ADPCM speech analysis/synthesis IC (8C) must consist of 12 serial bits. Note that only eight bits are generated from the analog-to-digital converter, via pin 9 of shift register 11B, to represent voice information. Since 8C expects 12 bits, four additional low bits are generated from pin 9 of 11B.



(From Figure C-1, Page 2, Coordinate 4C)

These four low bits are caused by four-bit binary counter 3C and the NAND gates at 4C, which are configured to allow a 447-kHz clock at pin 8 of 4C for 12 states. Note that the pin 8 output of gate 4C is connected to both the CLK input of 11B and the SI.CK (Serial Input Clock) input of 8C (pin 10).

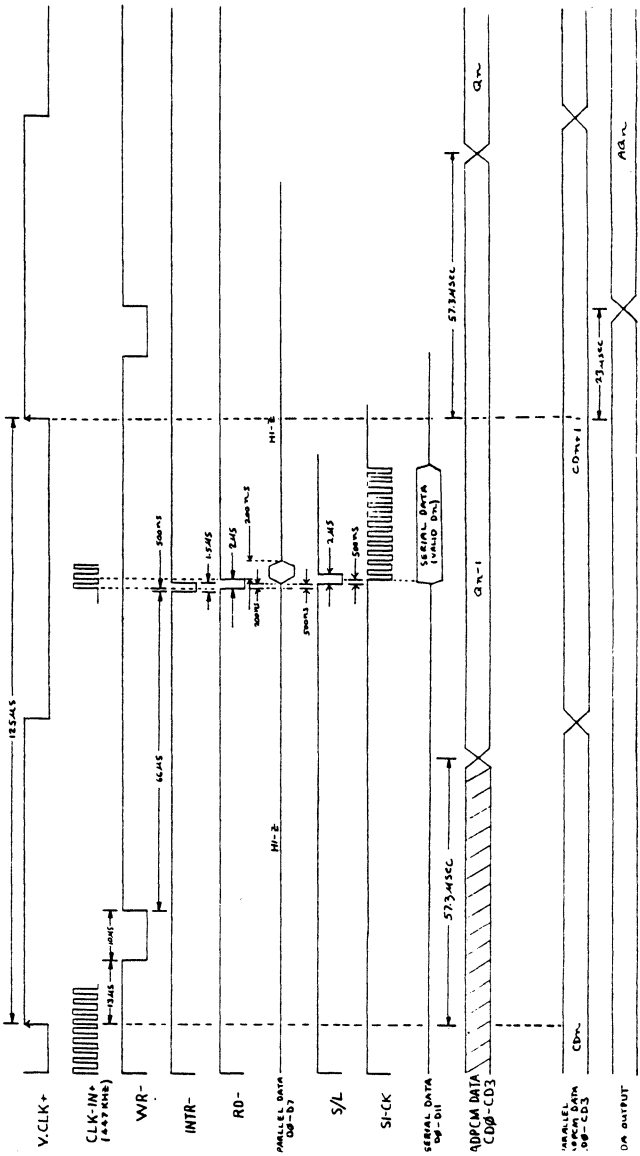
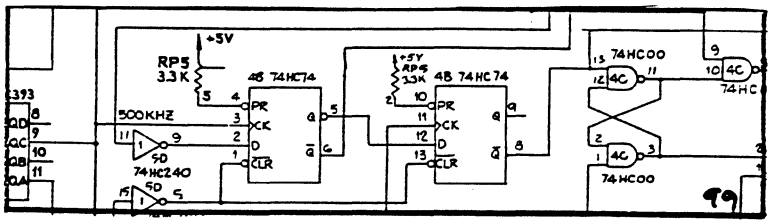


Figure 3-6. ADPCM CODEC Timing.



(From Figure C-1, Page 2, Coordinate 6C)

As shown in the above window, the 447-kHz pulse from pin 9 of 3C connects to NAND gate 4C (pin 9). As shown in the previous window, the pin 10 input of 4C determines the state of the clock. When pin 10 is active at 4C, the clock generates from pin 8 of 4C to gate 5D, where it is inverted (pin 3) and driven to 11B (pin 2). When pin 10 is inactive, the clock input is disabled.

Four-bit binary counter 3C, which is enabled at pin 1 by the 447-kHz signal from pin 9 of 3C, is configured to count from 0 to 11 before pins 5 and 6 become high. That is, when the binary digits of 3C equal 1100 (12 decimal), two high signals are generated from pins 5 and 6 to cause a low signal at pin 6 of 4C.

This low signal causes pin 3 of 4C to become high and, therefore, pin 11 of 4C to become low since pin 8 of 4B is high. (Note that pin 8 of 4B went high to start the shift register as described in the previous subsection.) The low signal at pin 11 of 4C disables the clock at pin 8 of 4C.

After the 12 bits are shifted, 8C generates a 4-bit representation of the 12-bit sample to the stacker/destacker via the CD0+ through CD3+ lines at pins 2 through 5. The stacker/destacker combines two consecutive nibbles of data from 8C, to generate a byte of data to memory. (See the "Stacker/Destacker Logic" subsection, below.)

VOICE SYNTHESIS (DECODING)

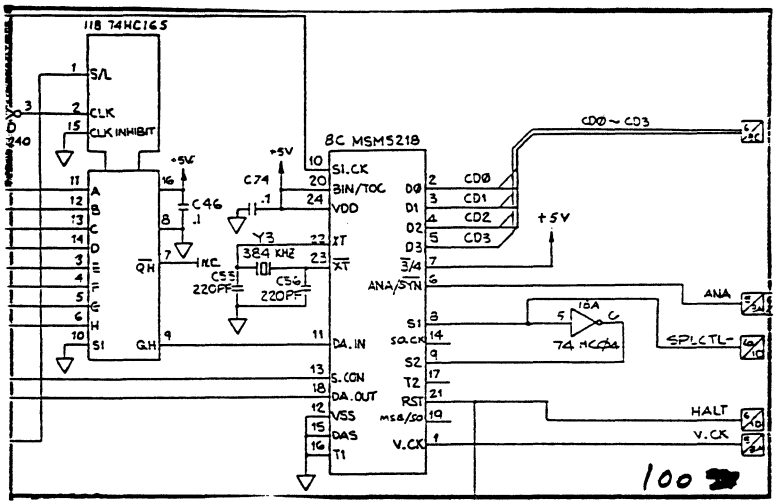
During voice decoding, 4-bit nibbles are generated from memory via the stacker/destacker (described in the following subsection) to 8C. To output an analog signal, 8C performs a 10-bit digital-to-analog conversion of the data.

The analog signal is then generated from pin 18 of 8C to pin 10 of the PCM filter, where it is filtered as described in the "Pulse Code Modulation Filtering Logic" subsection, above.

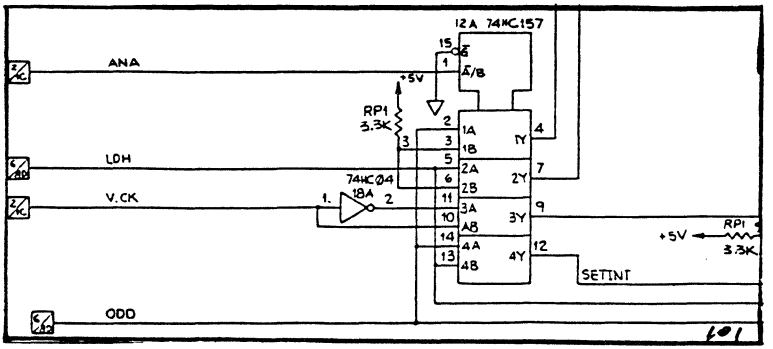
STACKER/DESTACKER LOGIC

The stacker/destacker consists of two sets of latches that are controlled by the CODEC clock (V.CK) and is used to latch in either a byte of data from the 8051 microprocessor or two separate nibbles of data from the CODEC. In other words, the stacker/destacker provides the necessary interface between the 8051 microprocessor 8-bit data bus and the CODEC 4-bit data bus during either encoding of voice or decoding of voice to or from memory.

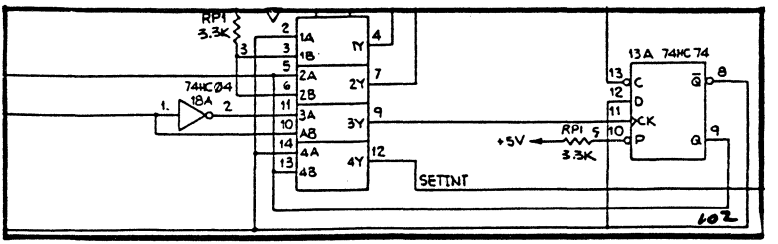
ENCODING VOICE TO MEMORY



(From Figure C-1, Page 2, Coordinate 1C)

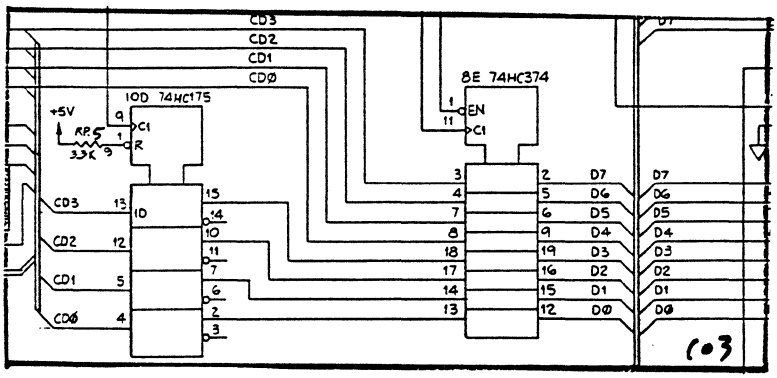


(From Figure C-1, Page 5, Coordinate 6A)



(From Figure C-1, Page 5, Coordinate 5A)

As shown in the top window, V.CK+ is generated from the CODEC (8C) at pin 1 to data multiplexer 12A (pin 1Ø), shown in the middle window. Since the CODEC is encoding the voice, ANA+ (shown in top window) is also generated from 8C (pin 6) to 12A (pin 1), enabling the pin 1Ø input of 12A. Therefore, a high signal is generated from pin 9 of 12A (shown in bottom window) to D flip-flop 13A (pin 11), to clock ODD+ (Odd) from pin 8.



(From Figure C-1, Page 6, Coordinate 4C)

See Figure 3-7 for CODEC stacker/destacker timing during the analysis (encoding) mode.

As shown in the above window, ODD+ clocks data latch 1ØD at pin 9, to enable CDØ+ through CD3+ (CODEC Data Lines Ø through 3) to generate to data latch 8E (pins 13, 14, 17, and 18).

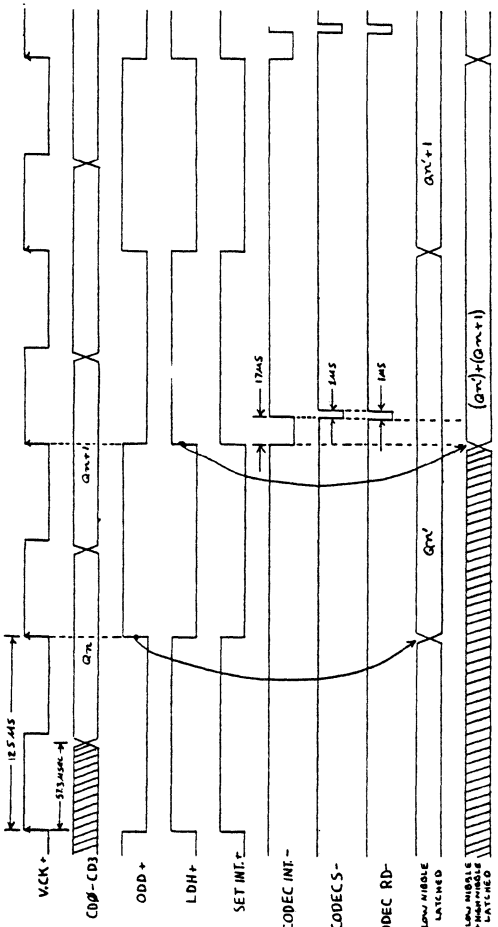


Figure 3-7. CODEC Stacker/Destacker Timing - Analysis Mode.

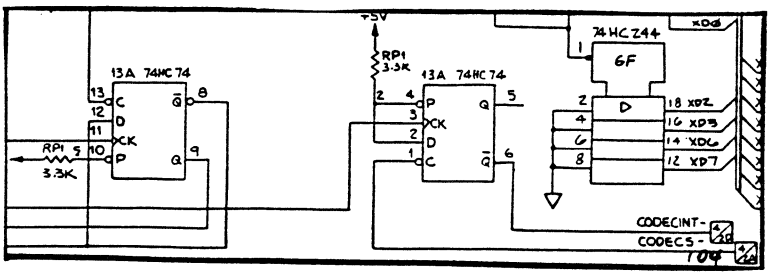
Simultaneously, the second nibble appears on the CDØ+ through CD3+ bus and is also latched at 8E (pins 3, 4, 7, and 8).

Note that 8E is clocked at pin 11 by LDH+ (Load Data High), which is generated from pin 9 of D flip-flop 13A (shown in the bottom and middle windows, respectively of previous set of windows). (Note that after ODD+ was generated from pin 8 of 13A, the D- input of 13A became high. At the next V.CK at pin 11, LDH+ is generated from pin 9 of 13A, to clock 8E at pin 1.)

Then, 8E is enabled at pin 1 during the operation by CODECRD-, which is generated when the 8051 microprocessor reads external RAM location 10h as described in the "Device Decoding" subsection, above.

Therefore, a data byte is generated to the 8051 microprocessor via DØ+ through D7+. Finally, a mode 3 DMA transfer occurs, and the data is placed in memory. (See the "X-Bus Mode 3 Control" subsection, above.)

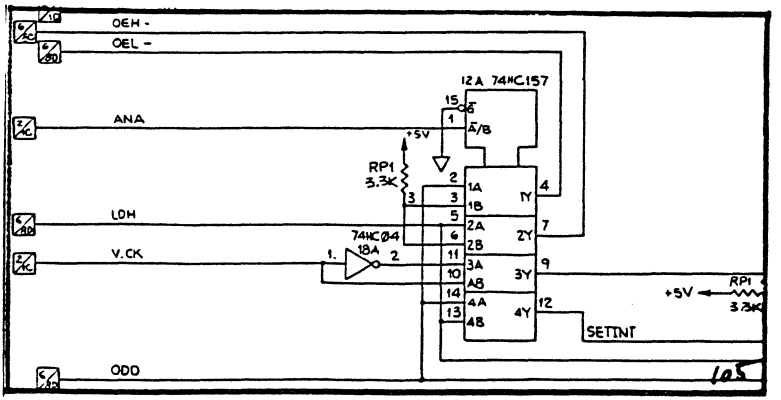
Note that when LDH- is generated from pin 9 of D flip-flop 13A, it also connects to the pin 13 input of data multiplexer 12A, causing SETINT- (Set Interrupt) at pin 12 of 12A. As shown in the window below, SETINT- clocks D flip-flop 13A (pin 3). Since pin 2 of 13A is strapped to +5 V via a 3.3-kohm resistor at RP1, CODECINT- (CODEC Interrupt) is generated from pin 6 to the 8051 microprocessor at pin 12. CODECINT- signifies to the 8051 microprocessor that a byte of voice information is ready to be transferred to memory.



(From Figure C-1, Page 5, Coordinate 4A)

After the transfer, the 8051 microprocessor writes to external RAM address 10h as described in the "Device Decoding" subsection, above, to generate CODECS- (CODEC Select), which clears the interrupt to the 8051 microprocessor, and acknowledges the byte of voice data.

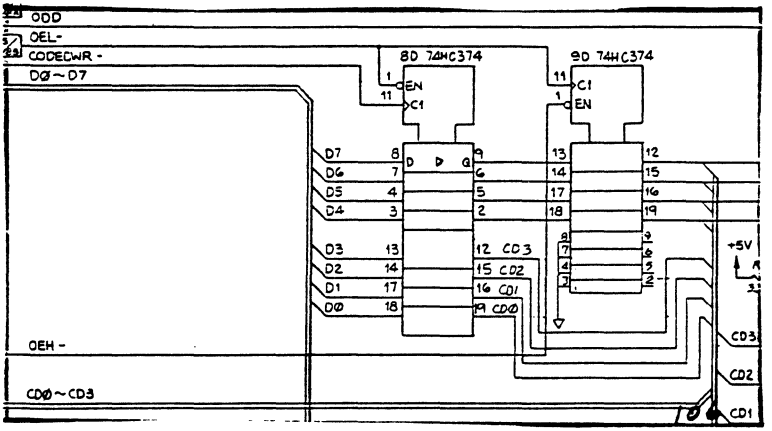
As shown in above, CODECS- clears 13A at pin 1, disabling CODECINT-.



(From Figure C-1, Page 5, Coordinate 6A)

Note also that the pin 3 and 6 inputs of 12A are strapped to +5 V via a 3.3-kohm resistor at RP1 to ensure that only the applicable data latches are enabled.

DECODING VOICE FROM MEMORY



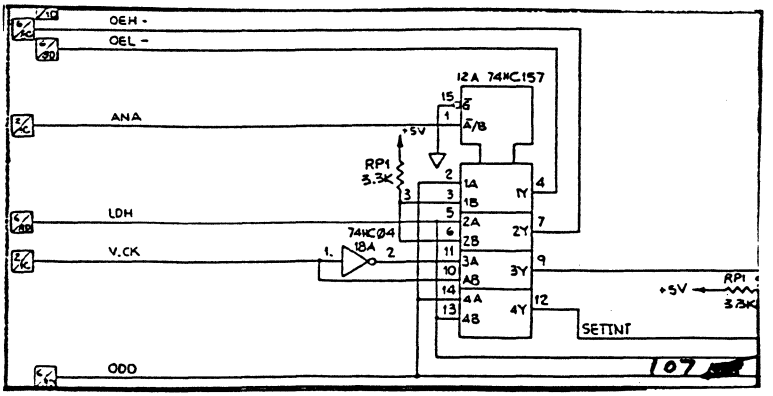
(From Figure C-1, Page 6, Coordinate 6C)

To decode the data from memory, a memory transfer occurs, which generates a byte of data from memory to data latch 8D (shown above) via 8051 microprocessor data lines D0+ through D7+.

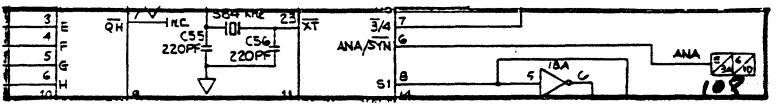
See Figure 3-8 for CODEC stacker/destacker timing during the synthesis (decoding) mode.

Note that the data is latched at 8D when the 8051 microprocessor performs a write to external RAM location 10h as described in the "Device Decoding" subsection, above, to generate CODECWR- to 8D (pin 11).

Next, 8D is enabled at pin 1 by OEL- (Output Enable Low). As shown in the top window below, OEL- is generated from data multiplexer 12A (pin 4). Since the CODEC is decoding the data, an inactive ANA+ is generated from the CODEC (pin 6), shown in the bottom window below, to 12A (pin 1). This enables the pin 2 input, which is connected to a low ODD+, and therefore, OEL- is generated from pin 4 of 12A to enable 8D at pin 1 (shown in the above window).



(From Figure C-1, Page 5, Coordinate 6A)



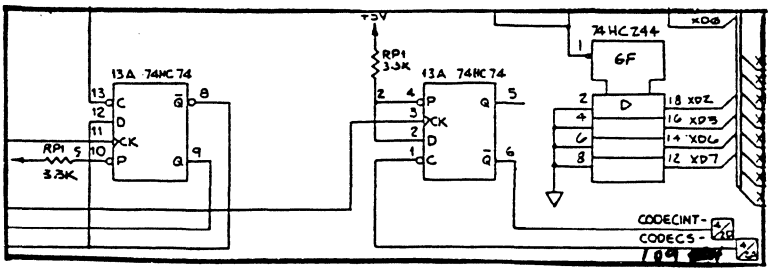
(From Figure C-1, Page 2, Coordinate 1C)

Therefore, CDØ+ through CD3+ is generated from pins 12, 15, 16, and 19 of 8D to the CODEC. The upper nibble, however, is latched into 9D by OEL- (pin 11).

Note that the low ODD+ also connects at pin 14 of 12A, causing SETINT- at pin 12 of 12A shown in the top window above. SETINT- clocks D flip-flop 13A (pin 3) shown in window below. Since pin 2 of 13A is strapped to +5 V via a 3.3-kohm resistor at RP1, CODECINT- (CODEC Interrupt) is generated from pin 6 to the 8051 microprocessor at pin 12. CODECINT- signifies to the 8051 microprocessor that a byte of voice information has been encoded by the CODEC and is ready to be transferred to memory, or a byte of voice information has been transferred from memory to the CODEC for decoding.

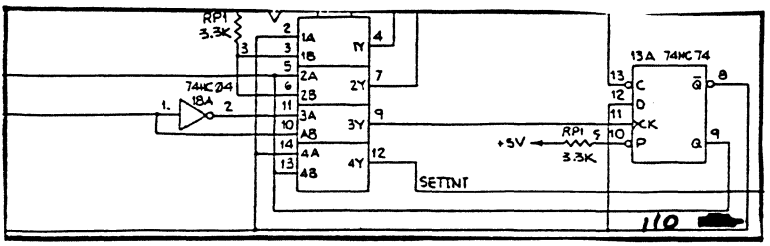
To Be Supplied

Figure 3-8. CODEC Stacker/Destacker Timing - Synthesis Mode.



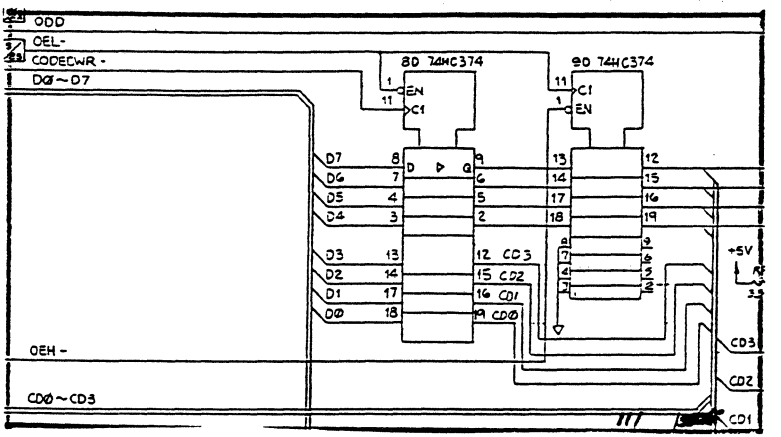
(From Figure C-1, Page 5, Coordinate 4A)

Then, as shown in the top window of the previous set of windows, OEH- (Output Enable High) is generated from data multiplexer 12A (pin 7). This occurs since the low ODD+ in the last cycle causes a low signal to generate from D flip-flop 13A (pin 9) at the next V.CK, shown in the window below. This low signal is input to 12A at pin 5.



(From Figure C-1, Page 5, Coordinate 5A)

OEH- is generated from pin 7 of 12A to pin 1 of 9D (shown below), enabling CD0+ through CD3+ to generate to the CODEC as the upper nibble.

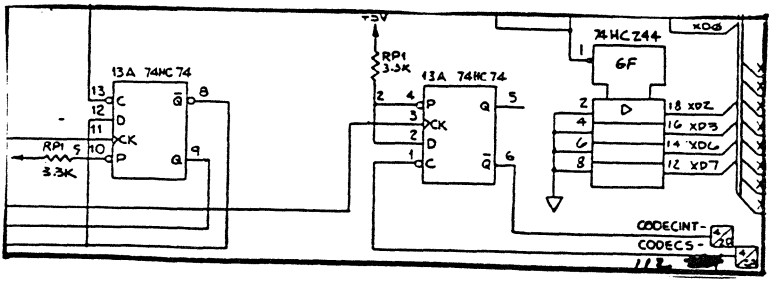


(From Figure C-1, Page 6, Coordinate 6C)

Note in the previous window, that pins 3 and 6 of 12A are strapped to +5 V via 3.3-kohm resistors at RP1 during the analysis mode (that is, during voice encoding described above).

This ensures that data latches 8D and 9D remain disabled during voice encoding.

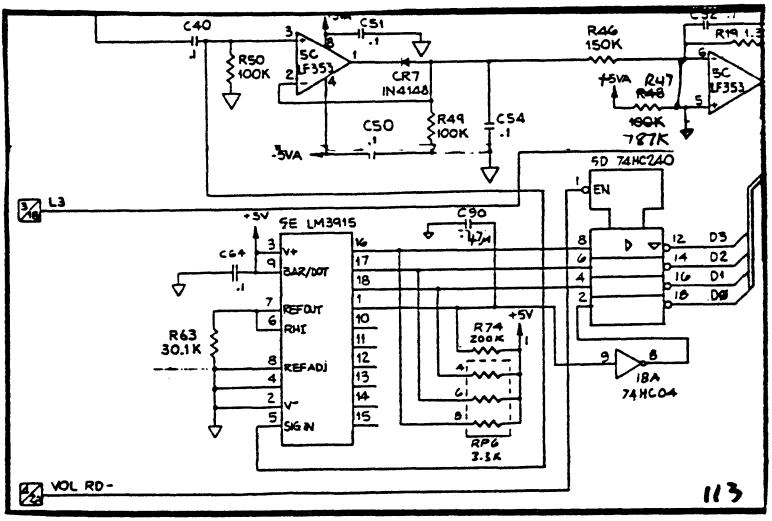
The 8051 microprocessor writes to external RAM address 10h as described in the "Device Decoding" subsection, above, to generate CODECS- (CODEC Select), which clears the interrupt to the 8051 microprocessor, and acknowledges the byte of voice data.



(From Figure C-1, Page 5, Coordinate 4A)

As shown in the above window, CODECS- clears 13A at pin 1, disabling CODECINT-.

SILENCE DETECTION AND VOLUME STATUS



(From Figure C-1, Page 2, Coordinate 7A)

Silence detection and volume control are built around the LM3915 dot/bar display driver (5E), which provides for a 3-dB/step analog signal suitable for a wide dynamic audio level range. It contains an adjustable voltage reference and an accurate 10-step voltage divider. In addition, it contains comparators that can detect extremely low amplitudes.

The pin assignments and functions for the LM3915 dot/bar display driver are listed in Table 3-6.

Table 3-6. LM3915 Dot/Bar Display Driver 5E Pin Assignments and Functions. (Page 1 of 2)

Pin	Function
1	**Output 1.** Output used to signify volume level; used with pins 16 through 18 (see below).
2	**Negative Power Supply (V-).** Tied to ground.
3	**Positive Power Supply (V+).** Strapped to +5V.
4	**Divider, Low End.** Tied to ground.
5	**Signal Input (SIG IN).** Input signal that is detected.
6	**Divider, High End.** Connected to pin 7.
7	**Reference Output (REFOUT).** Reference to pin 8.
8	**Reference Adjust (REFADJ).** Reference adjustment to pin 7 (nominally 1.25 V).
9	**Mode Select (BAR+/DOT-).** Strapped to +5 V to use bar graph mode for driving the signal.
10 - 15	Unused.

Table 3-6. LM3915 Dot/Bar Display Driver 5E Pin Assignments and Functions. (Page 2 of 2)

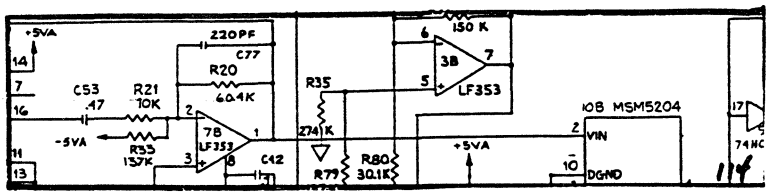
Pin	Function
16 - 18	**Outputs 2 Through 4.** Outputs used to signify volume level; used with pin 1 (see below).

Volume Level*

Pins				
16	17	18	1	Level
1	1	1	1	Silence
1	1	1	Ø	Volume detected
1	1	Ø	Ø	Next highest volume
1	Ø	Ø	Ø	Next highest volume
Ø	Ø	Ø	Ø	Highest volume

*Only the above five discrete values can be generated.

In conjunction with 5E, buffer 5D is used as the Loudness Control register.



(From Figure C-1, Page 2, Coordinate 6D)

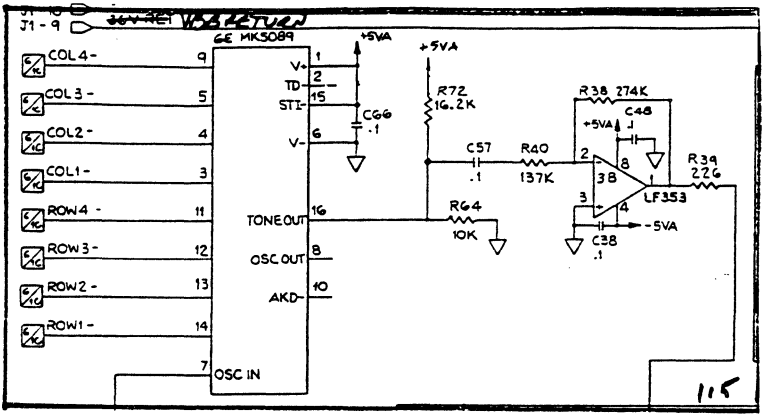
The amplified analog input to analog-to-digital converter 10B is tapped off between operational amplifier 7B (pin 1) and 10B (pin 2), and is coupled by the 0.1-microfarad capacitor at C40 to the SIG IN (Signal Input) of 5E (pin 5), as shown in the previous window.

A series of comparators within 5E can activate pins 1, 18, 17, and 16, depending upon the size of the incoming signal. Note that pin 1 becomes active first. Then pins 1 and 18 become active, and so on.

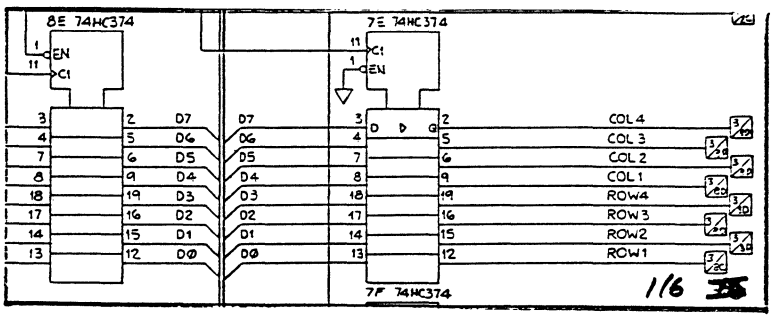
If a signal is detected, the pin 1 output is always inverted at 18A (pin 8) and driven to 5D (pin 2). The 8051 microprocessor enables 5D at pin 1 by reading external RAM location 30h as described in the "Device Decoding" subsection, above.

Note that the signal at pin 5 of 5E is half-wave rectified. Since 5E operates between 0 V and +5 V, only the top half of the AC waveform is detected by 5E. This waveform is filtered and averaged at the pin 1 output by the 200-kilohm resistor at R74 and the 0.1-microfarad capacitor at C90, to allow voice detection. The other three pins (that is, pins 18, 17, and 16) can be used to signify increases in volume. Each pin represents 3-dB amplitude increments with pin 1 as the lowest volume and pin 16 as the highest volume.

TONE DIALING



(From Figure C-1, Page 3, Coordinate 7D)



(From Figure C-1, Page 6, Coordinate 2C)

The DTMF generator (shown in top window) consists of an MK5089 integrated tone dialer, which interfaces to the DTMF Generator register (7E), shown in the bottom window.

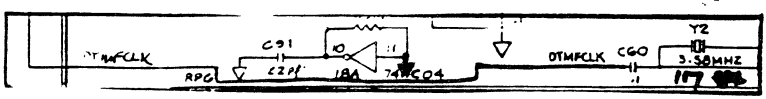
The pin assignments and functions for the MK5089 integrated tone dialer are listed in Table 3-7.

Table 3-7. MK5089 Integrated Tone Dialer 6E Pin Assignments and Functions.

Pin	Function
1	**Positive Power Supply (V+).** Strapped to +5 VA.
2	Unused.
3 - 5, 9	**Column Inputs (COL1- Through COL4-).** Applicable input connected for respective desired tone; used in conjunction with the row inputs.
6	**Negative Power Supply (V-).** Tied to ground.
7	**Oscillator Input (OSCIN+).** 3.58-MHz pulse.
8, 10	Unused.
11 - 14	**Row Inputs (ROW1- Through ROW4-).** Applicable input connected for respective desired tone; used in conjunction with the column inputs.
15	**Single Tone Inhibit (STI-).** Floated to cause any input that would normally result in a single tone to result in no tone; all other functions operate as normal.
16	**Tone Output (TONEOUT+).** Output of tone after an internal operational amplifier mixes the row and column tones.

To perform an automatic dial, the 8051 microprocessor writes to the DTMF Generator register at external RAM location 90h as described in the "Device Decoding" subsection, above, to input the row and column information into the DTMF generator (6E).

In response, 6E generates a tone that is dependent upon the binary value of the eight row and column inputs from the DTMF Generator register. Therefore, a tone, which represents a digit from 0 through 15, is generated from pin 16 of 6E.



(From Figure C-1, Page 3, Coordinate 5A)

Note that the row and column inputs create a divide ratio that causes the required two audio frequencies from a 3.58-MHz reference oscillator (Y2), which connects to 6E at pin 7 as DTMFCLK+ (DTMF Clock).

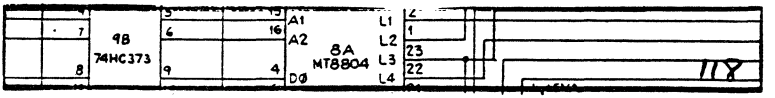
Digital-to-analog conversion is performed within 6E, to output a tone in a stairstep approximation to a sine wave at pin 16.

The 10-kilohm resistor at R64 converts the current from pin 16 into a voltage potential. In conjunction with R64, 16.2-kilohm resistor at R72 biases the signal to about 1.65 Vdc. The 0.1-microfarad capacitor at C57 provides DC isolation since operational amplifier 3B operates at about 0 Vdc (that is, 3B is powered by +5 VA and -5 VA).

Operational amplifier 3B provides a gain for transmission over the line interface (that is, line 1 or line 2), which occurs via the analog crosspoint switch array (8A) shown below. The combination of 274-kilohm resistor at R38 and 137-kilohm resistor at R40 set the gain. The 220-picofarad capacitor at C37 and R38 filter the signal from the DTMF generator, which synthesizes the sine waves, causing distortion.

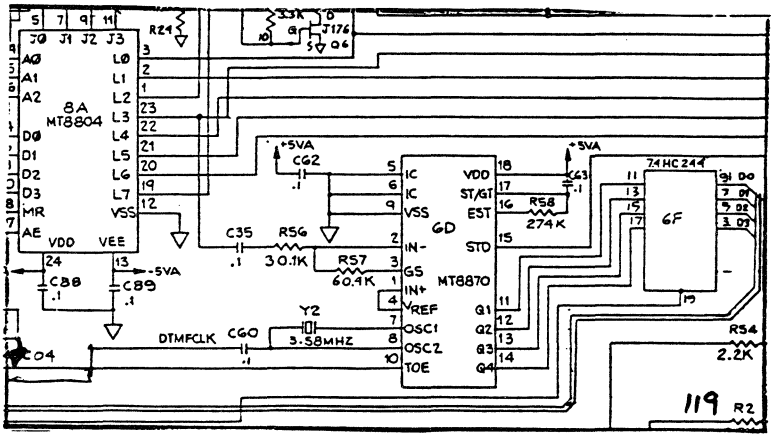
The 226-ohm resistor at R39 provides the proper termination for the secondary of transformer T2 or T3, depending on which line is used.

The signal, therefore, connects to the L2+ input of 8A (pin 1), where it is switched to either J0+ or J1+ (pin 5 or 7) for line 1 or line 2, respectively.



(From Figure C-1, Page 3, Coordinate 6B)

TONE DETECTION



(From Figure C-1, Page 3, Coordinate 4A)

The MT8870 DTMF receiver (6D) is used to detect touch tone, and can be connected to either line 1 or line 2, or the DTMF generator, via the analog crosspoint switch array (8A) at the L3+ output (pin 23).

The pin assignments and functions for the MT8870 integrated DTMF receiver are listed in Table 3-8. For output information, see the "Tone Detector Register" subsection in Section 2, "Architecture."

Table 3-8. MT8870 Integrated DTMF Receiver 6D Pin Assignments and Functions. (Page 1 of 2)

Pin	Function
1	**Noninverting Input (IN+).** Connects to an internal front-end differential operational amplifier.
2	**Inverting Input (IN-).** Connects to an internal front-end differential operational amplifier.
3	**Gain Select (GS+).** Output connected to pin 2 via resistors R56 and R57 for a gain of 2.
4	**Reference Voltage (VREF+).** Reference voltage output, which is nominally VDD+ divided by two; used to bias the input (pin 1) at midrail.
5, 6	**Internal Connection (IC+).** Must be tied to pin 9.
7	**Clock Input (OSC1+).** Clock input used in conjunction with pin 8 for internal oscillator; connected to 3.58-MHz crystal.
8	**Clock Output (OSC2+).** Clock output used in conjunction with pin 7 for internal oscillator; connected to 3.58-MHz crystal.
9	**Negative Power Supply (VSS-).** Tied to ground.
10	**Tristate Output Enable (TOE+).** Input that enables the Q1 through Q4 outputs; strapped to +5 V.
11 - 14	**Tristate Data Outputs (Q1 Through Q4).** When enabled, provides the code corresponding to the last valid tone-pair received.

Table 3-8. MT8870 Integrated DTMF Receiver 6D Pin Assignments and Functions. (Page 2 of 2)

Pin	Function
15	**Steering Delay Output (STD+).** Becomes high when a received pair-tone has been registered and the output latch has been updated; returns to its low state when the voltage of ST/GT+ (pin 17) falls below the steering threshold voltage (about 2.45 V)
16	**Early Steering Output (EST+).** Becomes high when the digital algorithm detects a recognizable tone-pair (that is, signal condition), and returns to its low state during any momentary loss of signal condition; tied to pin 17.
17	**Steering Input/Guard Time Output (ST/GT+).** When the ST voltage of this bidirectional pin is greater than the steering threshold voltage (about 2.45 V), 5D registers the detected tone-pair and updates the output latch (a voltage less than the steering threshold voltage allows 5D to accept a new tone-pair); the GT output resets the external steering time constant (its state is a function of pin 16 and the voltage of ST).
18	**Positive Power Supply (VDD+).** Strapped to +5 V.

As shown, 6D receives the DTMF touch-tone signal at pin 2 and, in response, outputs a 4-bit binary number (pins 11 through 14) that identifies the tone (that is, digits from Ø through 15).

Note that 6D contains an uncommitted operational amplifier. Therefore, 3Ø.1-kilohm resistor at R56 and 6Ø.4-kilohm resistor at R57 set the gain of the operational amplifier.

The Ø.1-microfarad capacitor at C35 couples AC signals and isolates DC signals from 8A to 6D. Note that 8A operates about Ø Vac and 6D operates about 2.45 Vac (midpoint reference).

The frequency reference for 6D is provided by 3.58-MHz crystal Y2.

Note that 6D contains a bandsplit filter that separates the high and low tones of a received pair, and a digital counter that verifies the frequency and duration (that is, validation) of the received tones before passing the corresponding code to the outputs (pins 11 through 14).

Low-group and high-group tone separation is accomplished within the DTMF receiver by applying the inputs of two ninth-order switched-capacitor bandpass filters. Each filter output is followed by a single-order switched-capacitor that smooths the signals before limiting, which is performed by high-gain comparators. The output of the comparators provide fullrail logic swings at the frequencies of the incoming tones.

An internal decoder counts to determine the frequencies of the limited tones and to verify that the tones correspond to standard DTMF frequencies. In addition, the decoder protects against extraneous tone simulation (for example, voice).

When the detector recognizes two simultaneous valid tones (that is, a signal condition), it asserts EST+ (Early Steering Output) at pin 16, and will deassert EST+ upon any subsequent loss of signal condition.

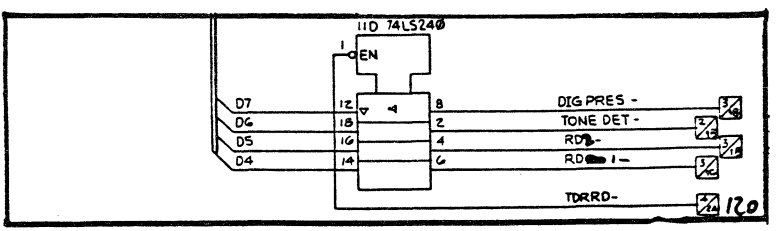
The Ø.1-microfarad capacitor at C63 and the 274-kilohm resistor at R58 provide an RC time constant that determines the validation time of 6D. The DTMF signal must be valid for 4Ø msec before 6D will output the value. This time delay allows 6D to filter out the extraneous sources of noise such as voice that, for an instant, have the characteristics of a DTMF signal.

In other words, before registering the decoded tone-pair, 6D checks for a valid signal duration via the external RC time-constant driven by EST+. When EST+ is high, the capacitor voltage rises as C63 discharges. If the signal-condition is stable (that is, EST+ remains high) for the validation period (approximately Ø.67 X R58 X C63), the capacitor voltage reaches the threshold voltage (about 2.45 V) of the steering logic to register the tone-pair, latching its corresponding 4-bit code into the output latch. (See the "Tone Detector Register" subsection in Section 2, "Architecture," for code information.)

The GT+ ouput at pin 17 then asserts and drives the capacitor voltage to VDD+ (pin 18). In addition, GT+ continues to drive as long as EST+ remains high. Finally, after a short delay to allow the output latch to stabilize, STD+ becomes high at pin 15, signaling that a received tone-pair has registered.

The contents of the output latch are available at the Q1 through Q4 outputs (pins 11 through 14) since TOE+ is strapped to +5 V.

The steering circuitry works in reverse to validate the interdigit pause between signals. Therefore, 6D rejects signals too short to be valid and will tolerate signal interruptions too short to be considered as a valid pauses.



(From Figure C-1, Page 6, Coordinate 2B)

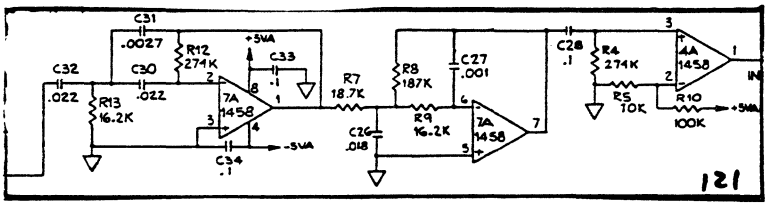
As described above, the validation signal, in effect, is generated from pin 15 of 6D as DIGPRES+ (Digit Present). DIGPRES+ connects to the Tone Detector register at 11D (shown in the above window), where it is read by the 8051 microprocessor at external RAM location 00h, as described in the "Device Decoding" subsection, above.

Simultaneously, the 8051 microprocessor reads the lower nibble of the Tone Detector register at 6F (shown in the previous window) for the value of the tone.

CALL PROGRESS TONE DETECTION

The call progress tone detection circuitry detects dial tone, busy tone, reorder tone, and answer (ringback) tone and consists of the following:

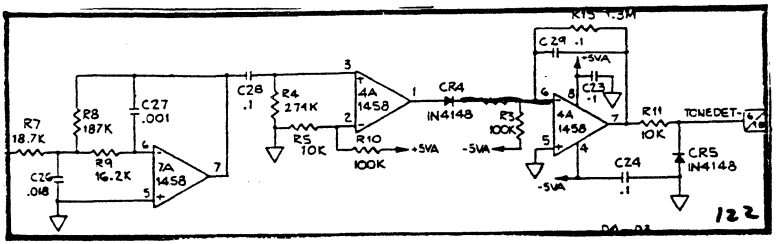
- filter circuitry
- detection circuitry that produces a TTL output



(From Figure C-1, Page 2, Coordinate 3B)

The first section consists of operational amplifier 7A, which acts as a band-pass filter with a pass band between 300 Hz and 750 Hz. Call progress tones are always within this pass band. All signals outside of the pass band (for example, voice signals) are attenuated.

The 0.1-microfarad capacitor at C28 couples the AC output of 7A (pin 7) to the input of 4A.



(From Figure C-1, Page 2, Coordinate 2B)

The second half of the circuitry consists of operational amplifiers at 4A. The first one of these acts as a comparator. A sensitivity threshold turns on the comparator when the signal exceeds a certain level.

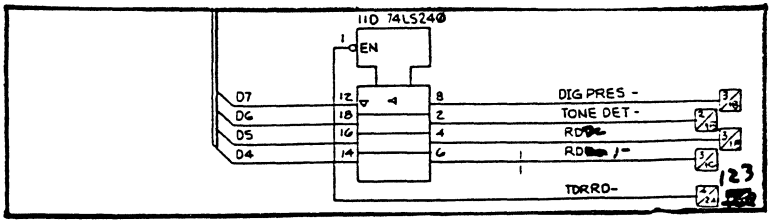
The comparator and diode CR4 half-wave rectify the AC signal generating out of the filter to produce pulses at the pin 6 input of 4A. The 10-kilohm resistor at R5 and the 100-kilohm resistor at R10 provide the reference voltage for the comparator.

These pulses from the comparator portion of 4A are integrated and filtered at pin 6 of 4A, to produce a constant TTL signal at the output of 10-kilohm resistor R11 as TONEDET- (Tone Detected).

In other words, the second half of 4A acts as an inverting lossy integrator and filters the pulses appearing at pin 1.

As described above, diode CR4 ensures that only positive output pulses from comparator at 4A (pin 1) appear at the pin 6 input of 4A. These pusles are then filtered and inverted before generating as active-low TTL TONEDET-.

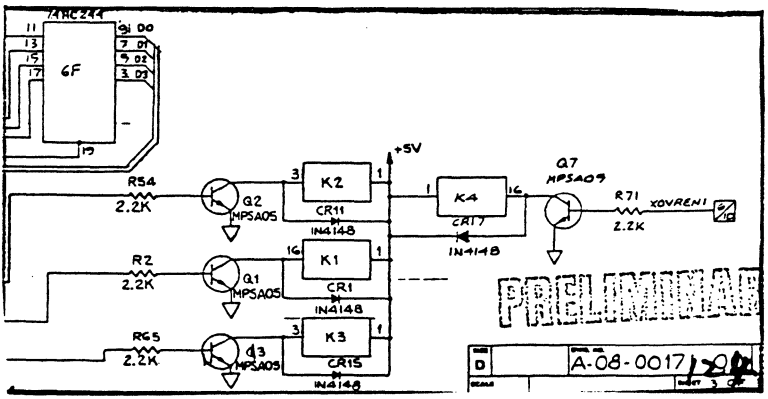
Note that the 100-kilohm resistor at R3 discharges the 0.1-microfarad capacitor at C29 to allow 4A to closely follow the input that is below ground so the comparator can act as a switch and turn off and on where applicable.



(From Figure C-1, Page 6, Coordinate 2B)

TONEDET- is generated to Tone Detector register 11D, signifying that a call progress tone has been detected. The 8051 microprocessor reads this bit (that is, D6+) by reading from external RAM location 00h, as described in the "Device Decoding" subsection, above.

LINE AND VOICE UNIT INTERFACE RELAYS



(From Figure C-1, Page 3, Coordinate 2A)

As shown in the above window, transistors Q1, Q2, Q3, and Q7 drive relays K1, K2, K3, and K4, respectively, which are used for both the line interfaces and voice unit interface for the Voice Processor Module. (These interfaces are detailed in the following subsections.)

The following signals turn on the transistors when the 8051 microprocessor writes to the Line Control register at external RAM location 0A0h as described in the "Device Decoding" subsection, above:

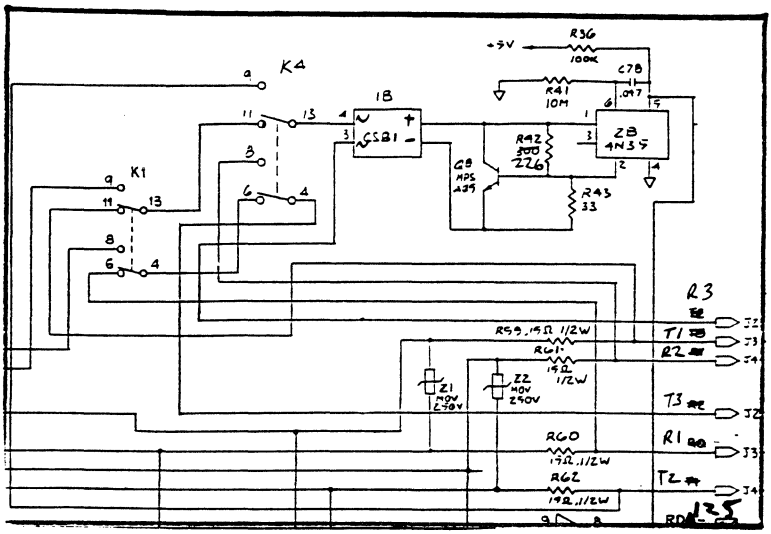
Signal	Transistor	Function
XOVREN0+	Q1	Crossover Enable 0: See below
OH1+	Q2	Off-Hook 1: Places line 1 off hook
OH2+	Q3	Off-Hook 2: Places line 2 off hook
XOVREN1+	Q4	Crossover Enable 1: See below

The crossover relay enables function as follows:

XOVREN0+	XOVREN1+	Function
0	0	Enables voice unit across line 1 (power-up default)
0	1	Enables voice unit across line 2 (used to save power)
1	0	Disables voice unit across both lines
1	1	Enables voice unit across line 2

When the applicable transistor turns on, its collector draws a current from +5 V and therefore energizes the relay coil, which sets up a magnetic field to close the relay switch.

The 2.2-kilohm resistors (R2, R54, R65, and R71) connected to the bases of the transistors act as current limiting resistors. In addition, diodes CR1, CR11, CR15, and CR17 protect the transistor against reverse fields produced by the relay coil during switching.



(From Figure C-1, Page 3, Coordinate 2D)

When both XOVRENØ+ and XOVREN1+ are inactive, both relays K1 and K4 are off, enabling the voice unit across line 1 at the voice unit interface as follows:

K1, Pin 13 Connection	K1, Pin 4 Connection	K4, Pin 13 Connection	K4, Pin 4 Connection
T1+ (pin 11)	R1+ (pin 6)	T1+ (pin 11)	R1+ (pin 6)

Note that R3+ connects to pin 3 of bridge rectifier 1B, and T1+ connects to pin 4 of 1B during this configuration. (See the "Voice Unit Interface" subsection, below.)

When XOVRENØ+ is inactive and XOVREN1+ is active, relay K1 is off and relay K4 is on, enabling the voice unit across line 2 at the voice unit interface as follows:

K1, Pin 13 Connection	K1, Pin 4 Connection	K4, Pin 13 Connection	K4, Pin 4 Connection
Unused	Unused	T2+ (pin 9)	R2+ (pin 8)

Note that R3+ connects to pin 3 of bridge rectifier 1B, and T2+ connects to pin 4 of 1B during this configuration. Also, relay K1 is not used since relay K4 is on. (See the "Voice Unit Interface" subsection, below.)

When XOVREN0+ is active and XOVREN1+ is inactive, relay K1 is on and relay K4 is off, disabling the voice unit across both lines at the voice unit interface as follows:

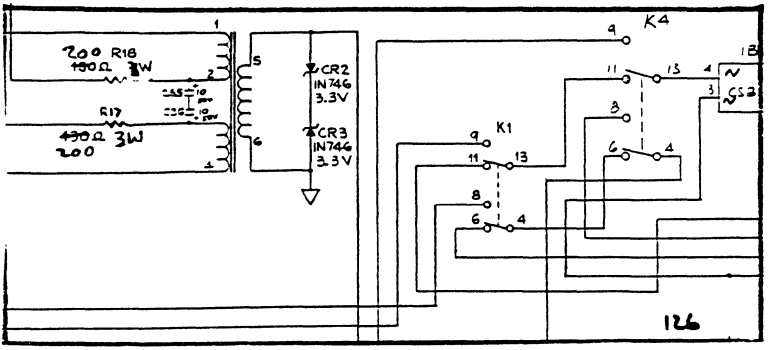
K1, Pin 13 Connection	K1, Pin 4 Connection	K4, Pin 13 Connection	K4, Pin 4 Connection
VBB (pin 9)	VBB RETURN (pin 8)	VBB (pin 11)	VBB RETURN (pin 6)

Note that R3+ connects to pin 3 of bridge rectifier 1B, and VBB connects to pin 4 of 1B during this configuration as shown in the window below. (See the "Voice Unit Interface" subsection, below.)

When both XOVREN0+ and XOVREN1+ are active, both relay K1 and relay K4 are on, enabling the voice unit across line 2 at the voice unit interface as follows:

K1, Pin 13 Connection	K1, Pin 4 Connection	K4, Pin 13 Connection	K4, Pin 4 Connection
Unused	Unused	T2+ (pin 9)	R2+ (pin 8)

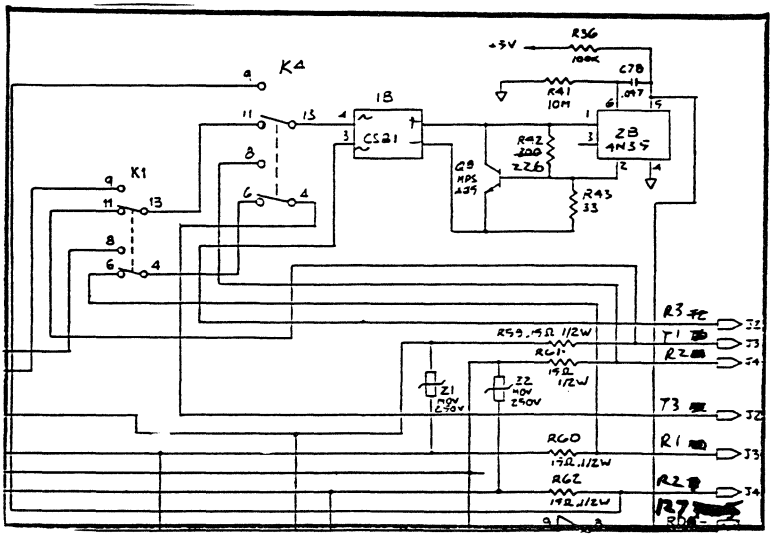
Note that R3+ connects to pin 3 of bridge rectifier 1B, and T2+ connects to pin 4 of 1B during this configuration. In addition, this configuration is identical to when XOVREN0+ is inactive and XOVREN1+ is active because relay K1 is not used since relay K4 is on. (See the "Voice Unit Interface" subsection, below.)



(From Figure C-1, Page 3, Coordinate 4D)

LINE INTERFACE CIRCUITRY

TIP AND RING SIGNALS

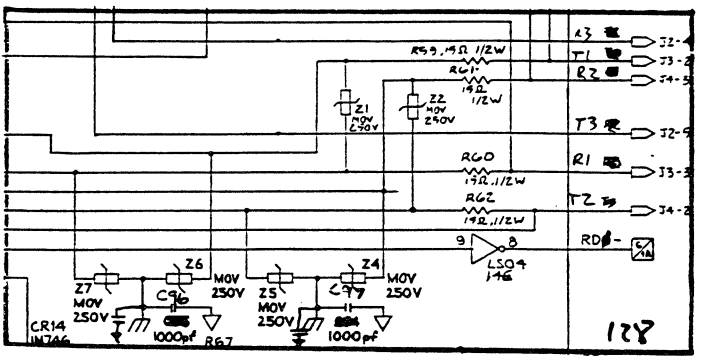


(From Figure C-1, Page 3, Coordinate 2D)

Each telephone line has a pair of tip and ring signals with tip as the more positive and ring as the more negative of the two signals. As shown in the above window, T1 (Tip 1) and R1 (Ring 1) at connector J3, pins 2 and 3, and T2 (Tip 2) and R2 (Ring 2) at connector J4, pins 2 and 3, are used as the line interfaces to the central office/PABX.

Each line interface is described in the following subsections.

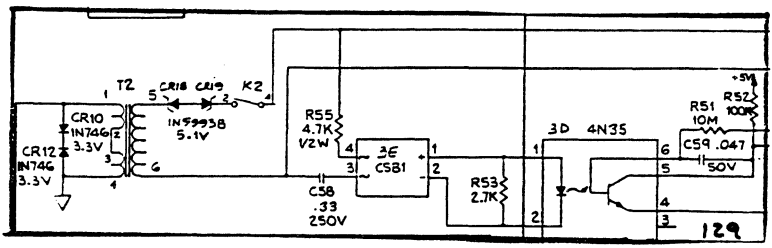
LINE 1 INTERFACE



(From Figure C-1, Page 3, Coordinate 2C)

Both T1 and R1 connect through 15-ohm resistors at R59 and R60, respectively, which protect against current surges. In other words, these carbon-composition resistors absorb large amounts of energy (for example, surges caused by lightning) to protect the line interface circuitry. For example, the resistors protect the Controller board traces, which tend to burn otherwise.

In addition to the resistors, 250-V metal-oxide varistor Z1 acts as a switch between T1 and R1. If more than about 300 V is impressed across Z1, it will short between T1 and R1 and, therefore, shunt the surge current around the line interface circuitry (that is, the relays, transformers, etc.) for protection. Varistors Z6 and Z7 protect surges to chassis ground through the 1000-picoFarad capacitor at C96.



(From Figure C-1, Page 3, Coordinate 7C)

During normal operation, T1 and R1 generate to the line 1 interface, which consists of the following:

- o coupling transformer T2
- o relay K2
- o ring detector

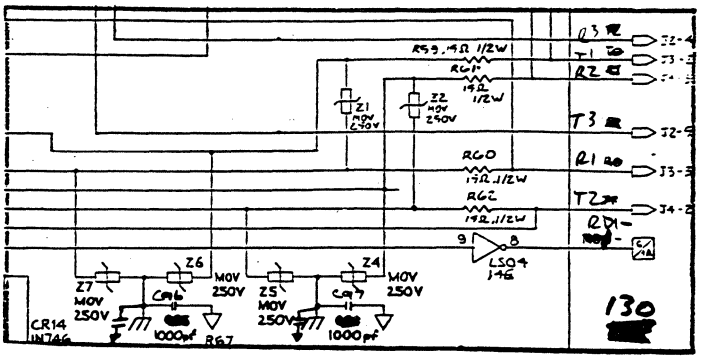
Transformer T2 provides DC isolation and couples the voice signals to the central office/PABX line from the Voice Processor Module or from the central office/PABX line to the Voice Processor Module, depending on which way the signals are transmitted.

Diodes CR1Ø and CR12, which are connected to the secondary of T2, protect the circuitry from large voltage spikes (that is, transient voltage) that generate through T2. In other words, the diodes clamp the large spikes to about +4 V or -4 V, to protect the secondary circuitry, which consists of many CMOS devices that are powered by +5 V.

Relay K2 provides the off-hook/on-hook relay switch, which is similar to the off-hook/on-hook of a telephone hook switch. (See the "Line and Voice Unit Interface Relays" subsection, above.)

When the Voice Processor Module goes off-hook, K2 closes, and loop current from the central office/PABX flows through transformer T2, causing the central office/PABX to detect off-hook. In response, the central office/PABX returns dial tone. The Voice Processor Module detects the dial tone via the Call Progress Tone Detector and, therefore, acknowledges that the central office/PABX is ready to receive digits. (See the "Call Progress Tone Detection" subsection, above.)

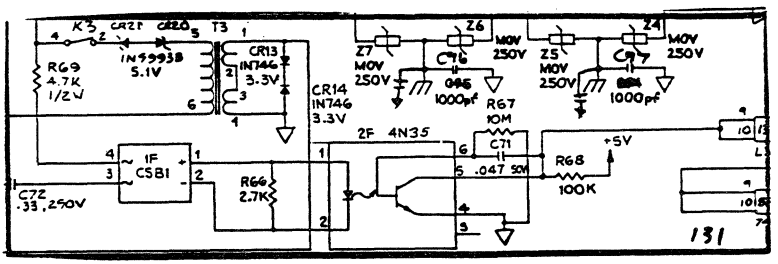
LINE 2 INTERFACE



(From Figure C-1, Page 3, Coordinate 2C)

Both T2 and R2 connect through 15-ohm resistors at R62 and R61, respectively, which protect against current surges. In other words, these carbon-composition resistors absorb large amounts of energy (for example, surges caused by lightning) to protect the line interface circuitry. For example, the resistors protect the Controller board traces, which tend to burn otherwise.

In addition to the resistors, 250-V metal-oxide varistor Z2 acts as a switch between T2 and R2. If more than about 300 V is impressed across Z2, it will short between T2 and R2 and, therefore, shunt the surge current around the line interface circuitry (that is, the relays, transformers, etc.) for protection. Varistors Z4 and Z5 protect surges to chassis ground through the 1000-picoFarad capacitor at C97.



(From Figure C-1, Page 3, Coordinate 4C)

During normal operation, T2 and R2 generate to the line 2 interface, which consists of the following:

- coupling transformer T3
- relay K3
- ring detector

Transformer T3 provides DC isolation and couples the voice signals to the central office/PABX line from the Voice Processor Module or from the central office/PABX line to the Voice Processor Module, depending on which way the signals are transmitted.

Diodes CR13 and CR14, which are connected to the secondary of T3, protect the circuitry from large voltage spikes (that is, transient voltage) that generate through T3. In other words, the diodes clamp the large spikes to about +4 V or - 4 V, to protect the secondary circuitry, which consists of many CMOS devices that are powered by +5 V.

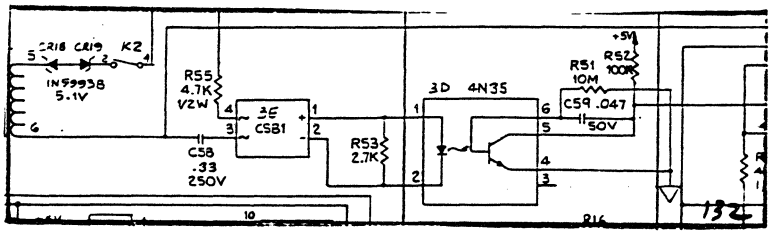
Relay K3 provides the off-hook/on-hook relay switch, which is similar to the off-hook/on-hook of a telephone hook switch. (See the "Line and Voice Unit Interface Relays" subsection, above.)

When the Voice Processor Module goes off-hook, K3 closes, and loop current from the central office/PABX flows through transformer T3, causing the central office/PABX to detect off-hook. In response, the central office/PABX returns dial tone. The Voice Processor Module detects the dial tone via the Call Progress Tone Detector and, therefore, acknowledges that the central office/PABX is ready to receive digits. (See the "Call Progress Tone Detection" subsection, above.)

LINE INTERFACE RING DETECTION

The ring detection circuitry for both lines is described in the following subsections.

Line 1



(From Figure C-1, Page 3, Coordinate 6C)

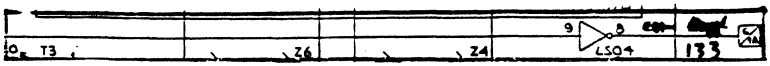
The ring detection circuitry for line 1 consists of bridge rectifier 3E, optocoupler 3D, associated resistors and capacitors, and an inverter at 14E (not shown in the window).

Bridge rectifier 3E rectifies the ringing current in both directions. The 4.7-kilohm resistor at R55 and Ø.33-microfarad capacitor at C58 provide the proper ringer impedance to the central office/PABX.

Resistor R55 and capacitor C58 also couple the ringing signal to optocoupler 3D. After the ringing voltage is full-wave rectified by 3E (pins 1 and 2), the pulses are generated to optocoupler 3D (pins 1 and 2), which contains an internal LED that turns on at about 1.2 V, causing an internal phototransistor to turn on. Therefore, the bottom of 1ØØ-kilohm resistor R52 (that is, pin 5 of 3D) is pulled to ground (that is, about Ø.25 V).

Note that R52 and Ø.Ø47-microfarad capacitor C59 form an integrator to filter the output pulses of 3D and keep pin 5 of 3D near ground potential.

In summary, 3D provides isolation, detects the ringing pulses, and couples the pulses to an internal phototransistor that turns on and continues to remain on as long as ringing is present because of the integrator action of R52 and C59.



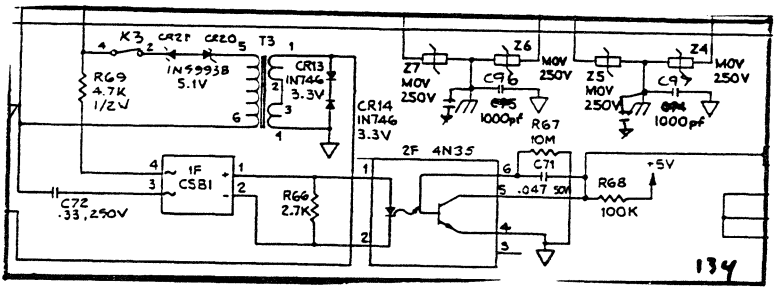
(From Figure C-1, Page 3, Coordinate 2C)

The low signal at pin 5 of 3D is then inverted at 14E (pin 8) and driven as RD1+ (Ring Detect 1) to the Tone Detector register at external RAM location ØØh as described in the "Device Decoding" subsection, above. A high RD1- signifies that a ring has been detected on line 1.

Note in the previous window that 2.7-kilohm resistor R53 sets a threshold and shunts some of the current around the internal LED of 3D, and, therefore, allows more current to generate from 3E. This desensitizes the ring detector to dial pulses that are generated by the Voice Processor Module. In other words, when relay K2 out-pulses digits, pulses also generate to the ring detector. Therefore, R53 desensitizes the ring detector to these dial pulses.

If the ring detector were not desensitized to dial pulses, false ring detection would occur while dial pulses were generated.

Line 2



(From Figure C-1, Page 3, Coordinate 4C)

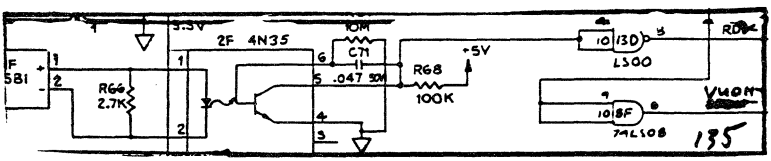
The ring detection circuitry for line 2 consists of bridge rectifier 1F, optocoupler 2F, associated resistors and capacitors, and an inverter at 13D (not shown in the window).

Bridge rectifier 1F rectifies the ringing current in both directions. The 4.7-kilohm resistor at R69 and Ø.33-microfarad capacitor at C72 provide the proper ringer impedance to the central office/PABX.

Resistor R69 and capacitor C72 also couple the ringing signal to optocoupler 2F. After the ringing voltage is full-wave rectified by 1F (pins 1 and 2), the pulses are generated to optocoupler 2F (pins 1 and 2), which contains an internal LED that turns on at about 1.2 V, causing an internal phototransistor to turn on. Therefore, the bottom of 1ØØ-kilohm R68 (that is, pin 5 of 2F) is pulled to ground (that is, about Ø.25 V).

Note that R68 and Ø.Ø47-microfarad capacitor C71 form an integrator to filter the output pulses of 2F and keep pin 5 of 2F near ground potential.

In summary, 2F provides isolation, detects the ringing pulses, and couples the pulses to an internal phototransistor that turns on and stays as long as ringing is present because of the integrator action of R68 and C71.



(From Figure C-1, Page 3, Coordinate 2B)

The low signal at pin 5 of 2F is then inverted at 13D (pin 8) and driven as RD2+ (Ring Detect 2) to the Tone Detector register at external RAM location ØØh as described in the "Device Decoding" subsection, above. A high RD2- signifies that a ring has been detected on line 2.

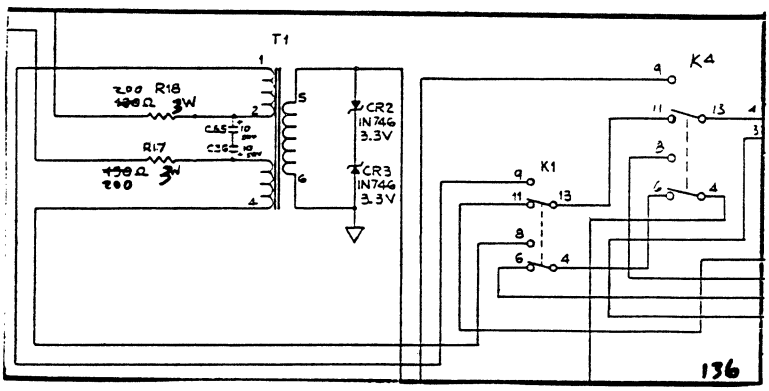
Note in the previous window that 2.7-kilohm resistor R66 sets a threshold and shunts some of the current around the internal LED of 2F, and, therefore, allows more current to be generated from 1F. This desensitizes the ring detector to dial pulses that are generated by the Voice Processor Module. In other words, when relay K3 out-pulses digits, pulses also generate to the

ring detector. Therefore, R66 desensitizes the ring detector to these dial pulses.

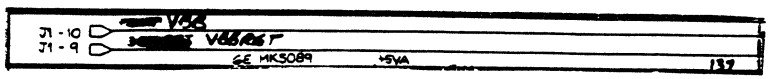
If the ring detector were not desensitized to dial pulses, false ring detection would occur while dial pulses were generated.

VOICE UNIT INTERFACE CIRCUITRY

The Voice Processor Module must power the voice unit (telephone set), which can be connected across the voice unit interface or across either line 1 or line 2. When the voice unit connects across either line 1 or line 2, it cannot be connected to the voice unit interface. In other words, the voice unit can only be connected across one interface at any time.



(From Figure C-1, Page 3, Coordinate 4D)



(From Figure C-1, Page 3, Coordinate 7D)

As shown in the top window, the voice unit interface provides power to the voice unit via 200-ohm battery feed resistors R17 and R18 and the primary of transformer T1. As shown in the bottom window, power generates via connector J1, pins 10 and 9, as VBB and VBB RETURN (VBB Return), respectively.

Current flows from the VBB supply at connector J1, pin 10, through R18 and pins 1 and 2 of T1 (top window), where it generates through the voice unit via relay K1 and K4. Then, the current flows back through K4 and K1, through pins 4 and 3 of T1, and through R17 to connector J1, pin 9 (bottom window).

In addition, T1 provides AC impedance that matches the voice unit, which consists of 600 ohms for a maximum power transfer. The 10-microfarad capacitors at C65 and C36, and the 0.022-microfarad capacitor at C25, provide an AC short between pins 2 and 3 of T1 for the 600-ohm impedance. (Note that the DC impedance consists of the impedance of T1 and the 200-ohm resistors at R17 and R18, which equals about 973 ohms.)

Zener diodes CR2 and CR3 are provided for transient protection against the CMOS devices in the circuit.

When the voice unit is connected across the voice unit interface, the following applications can occur:

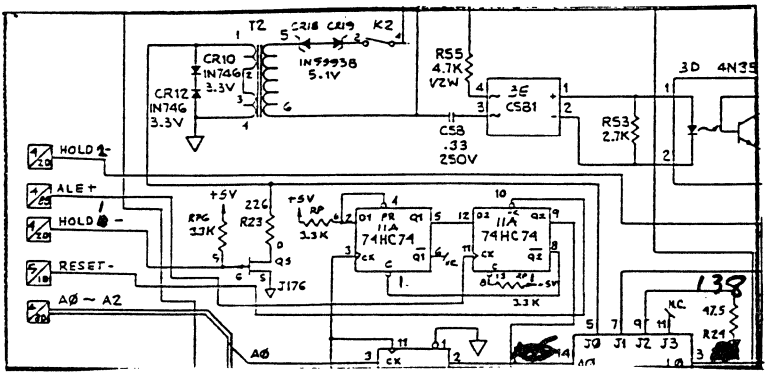
- encoding of voice (that is, voice dictation)
- decoding of voice (that is, receiving messages)
- call placement (via the analog crosspoint switch array) to the telephone line interface (line 1 or line 2)

Depending upon the state of relays K1 and K4 as described in the "Line and Voice Unit Interface Relays" subsection, above, the voice unit can switch to either line 1 or line 2.

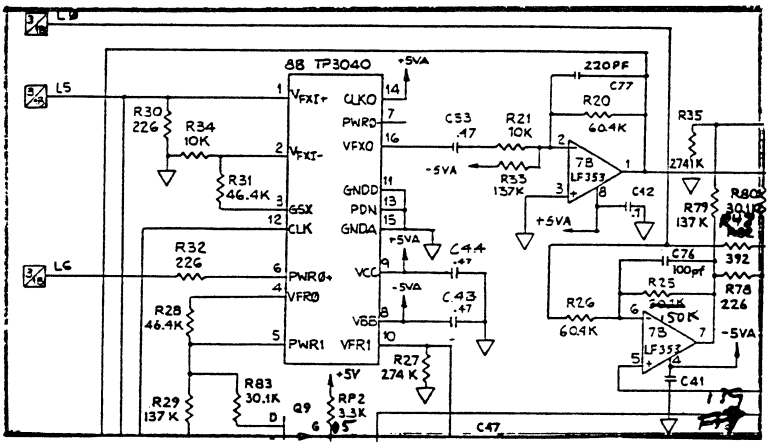
CALL PLACEMENT TO TELEPHONE LINE INTERFACE

Calls may be placed across either line 1 or line 2 via the analog crosspoint switch. Each line is described in the following subsections.

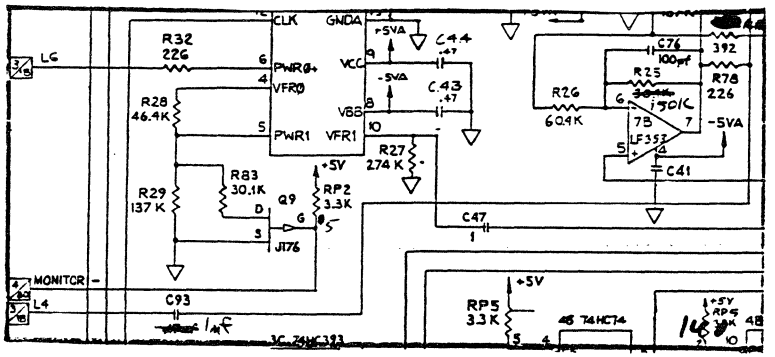
Line 1



(From Figure C-1, Page 3, Coordinate 7C)

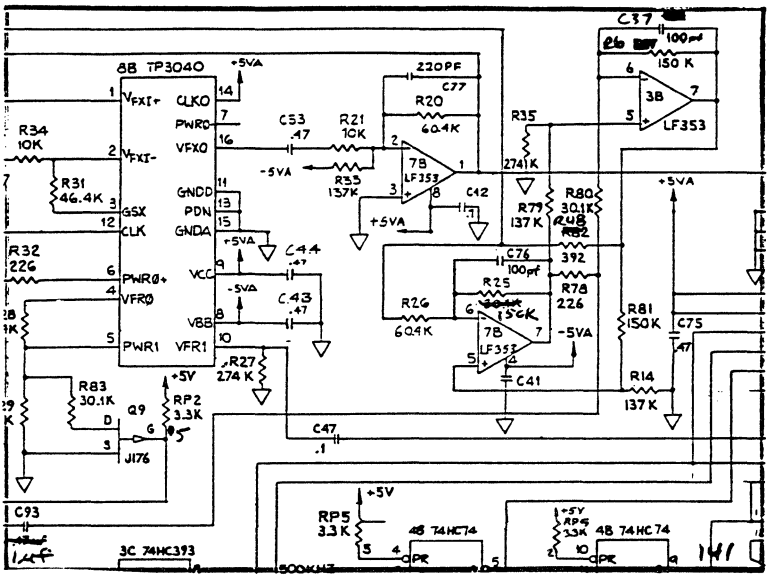


(From Figure C-1, Page 2, Coordinate 7D)



(From Figure C-1, Page 2, Coordinate 6C)

Calls From Voice Unit to Line 1. When the voice unit becomes off hook, loop current flows and the loop-current detection notifies the 8051 microprocessor that the voice unit has gone off hook. In response, the 8051 microprocessor closes relay K2, which connects to J0 (Junctor 0) of the analog crosspoint switch array (8A), shown in the top window. The voice signal generates from the T1 transformer secondary of the voice unit interface via L0 (Line 0) to the voice amplifier circuitry, shown in the middle window. After the voice signal is amplified, it generates to 8A via L4 (Line 4), shown in the bottom window, and is connected to J0 of 8A.



(From Figure C-1, Page 2, Coordinate 6D)

The voice signal from the T1 transformer secondary generates to operational amplifier 7B (pin 6) via the 60.4-kilohm resistor at R26. A gain of 2.5 can be calculated by dividing the 150-kilohm resistor at R25 by R26. The 100-picoFarad capacitor at C76, which is in parallel with R25, attenuates any high frequencies (that is, noise) and prevents oscillations.

The output of 7B (pin 7) generates through the 226-ohm resistor at R78 and the 1-microFarad capacitor at C93 to the analog crosspoint switch array (8A) via L4.

Then, 8A connects the voice signal to J0, and the voice signal then generates through the T2 secondary, to the Tip and Ring connectors, and finally to the central office/PABX.

Note that the output of 7B also generates to a resistor divider consisting of the 137-kilohm resistor at R79 and the 247-kilohm resistor at R35, located at the positive terminal of operational amplifier 3B (pin 5), and to the 30.1-kilohm resistor at R80, located at the negative terminal of 3B (pin 6). The resistor

divider ensures that the voltages at pins 6 and 5 of 3B are equal. This inhibits oscillations by cancellation. (The 392-ohm resistor at R48 provides another resistor divider with the T1 secondary.)

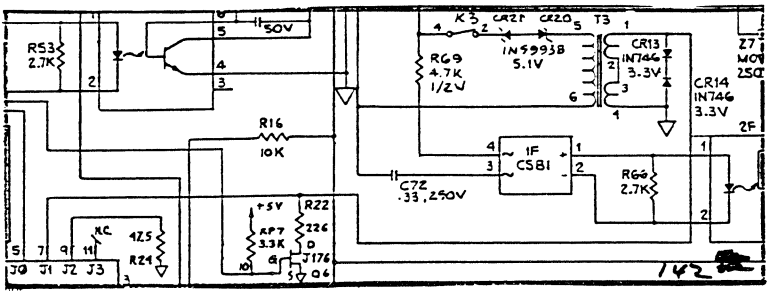
Calls From Line 1 to Voice Unit. When the voice signal originates from the central office/PABX, the voice signal generates through the Tip and Ring connectors to the secondary of T2 and the JØ input of 8A. Then, 8A connects the voice signal to the voice amplifier via L4+.

At the voice amplifier, the voice signal is coupled to pin 6 of operational amplifier 3B (via C93) where it is amplified. The signal amplification can be determined by dividing the 150-kilohm resistor at R6 by the 30.1-kilohm resistor at R80. The 100-picoFarad capacitor at C37, which is in parallel with R6, attenuates any high frequencies (that is, noise) and prevents oscillations.

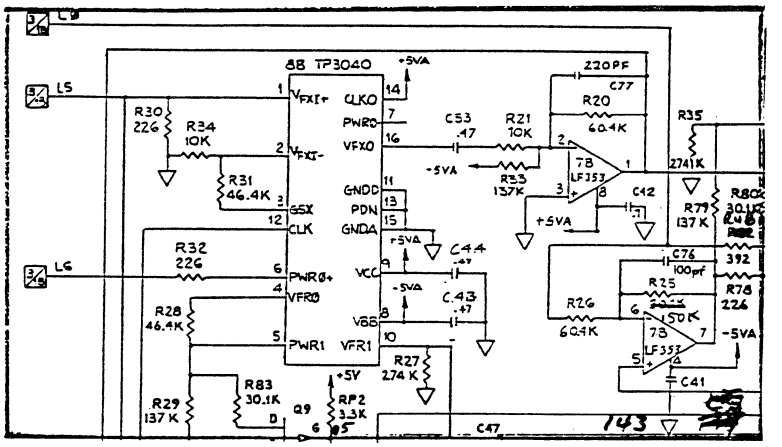
The output at 3B (pin 7) then generates through the 392-ohm resistor at R48 to the T1 secondary transformer via LØ+.

Note that the output of 3B also generates to a resistor divider consisting of the 150-kilohm resistor at R81 and the 137-kilohm resistor at R14, located at the positive terminal of operational amplifier 7B (pin 5), and to the 60.4-kilohm resistor at R26, located at the negative terminal of 7B (pin 6). The resistor divider ensures that the voltages at pins 6 and 5 of 7B are equal. This inhibits oscillations by cancellation. (The 392-ohm resistor at R48 provides another resistor divider with the T1 secondary.)

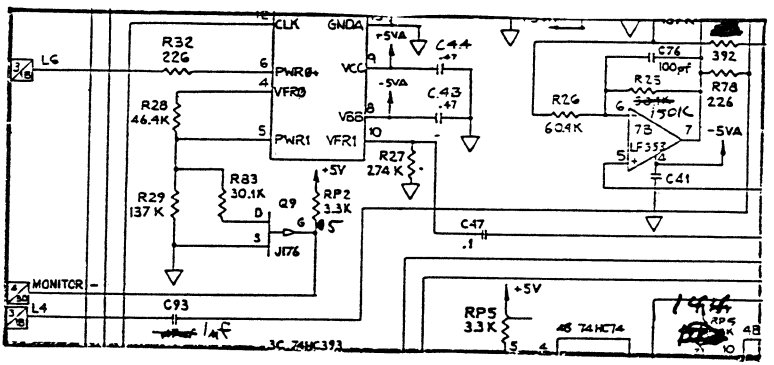
Line 2



(From Figure C-1, Page 3, Coordinate 4C)

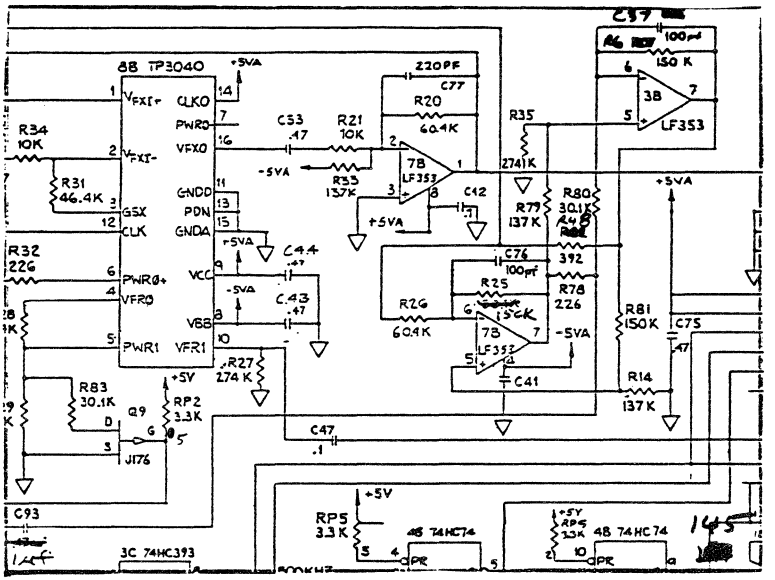


(From Figure C-1, Page 2, Coordinate 7D)



(From Figure C-1, Page 2, Coordinate 6C)

Calls From Voice Unit to Line 2. When the voice unit becomes off hook, loop current flows and the loop-current detection notifies the 8051 microprocessor that the voice unit has gone off hook. In response, the 8051 microprocessor closes relay K3, which connects to J1 (Junctor 1) of the analog crosspoint switch array (8A), shown in the top window. The voice signal generates from the T1 transformer secondary of the voice unit interface via L0 (Line 0) to the voice amplifier circuitry, shown in the middle window. After the voice signal is amplified, it generates to 8A via L4 (Line 4), shown in the bottom window, and is connected to J1 of 8A.



(From Figure C-1, Page 2, Coordinate 6D)

The voice signal from the T1 transformer secondary generates to operational amplifier 7B (pin 6) via the 60.4-kilohm resistor at R26. A gain of 2.5 can be calculated by dividing the 150-kilohm resistor at R25 by R26. The 100-picoFarad capacitor at C76, which is in parallel with R25, attenuates any high frequencies (that is, noise) and prevents oscillations.

The output of 7B (pin 7) generates through the 226-ohm resistor at R78 and the 1-microFarad capacitor at C93 to the analog crosspoint switch array (8A) via L4.

Then, 8A connects the voice signal to J1, and the voice signal then generates through the T3 secondary, to the Tip and Ring connectors, and finally to the central office/PABX.

Note that the output of 7B also generates to a resistor divider consisting of the 137-kilohm resistor at R79 and the 247-kilohm resistor at R35, located at the positive terminal of operational amplifier 3B (pin 5), and to the 30.1-kilohm resistor at R80, located at the negative terminal of 3B (pin 6). The resistor divider ensures that the voltages at pins 6 and 5 of 3B are equal. This inhibits oscillations by cancellation. (The 392-ohm resistor at R48 provides another resistor divider with the T1 secondary.)

Calls From Line 2 to Voice Unit. When the voice signal originates from the central office/PABX, the voice signal generates through the Tip and Ring connectors to the secondary of T3 and the J1 input of 8A. Then, 8A connects the voice signal to the voice amplifier via L4+.

At the voice amplifier, the voice signal is coupled to pin 6 of operational amplifier 3B (via C93) where it is amplified. The signal amplification can be determined by dividing the 150-kilohm resistor at R6 by the 30.-kilohm resistor at R80. The 100-picoFarad capacitor at C37, which is in parallel with R6, attenuates any high frequencies (that is, noise) and prevents oscillations.

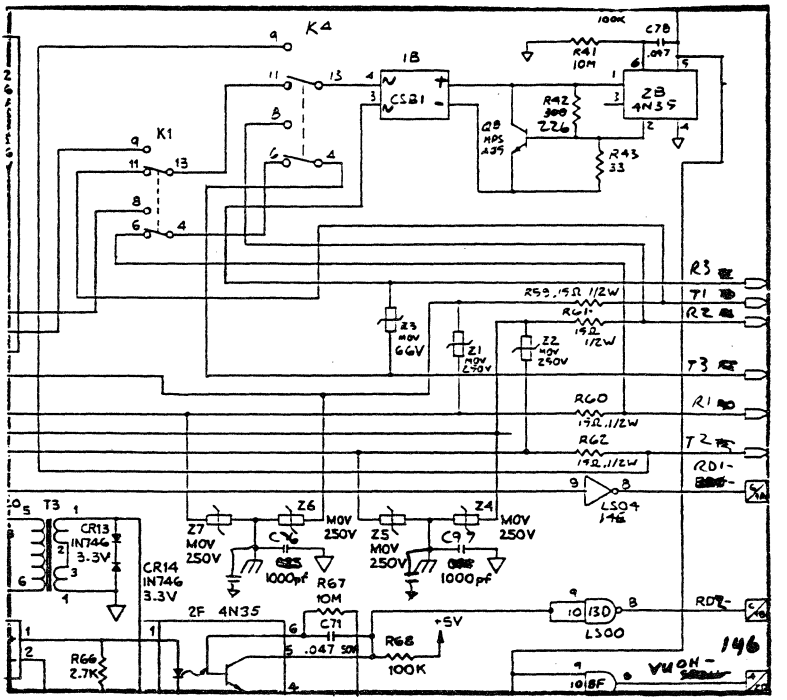
The output at 3B (pin 7) then generates through the 392-ohm resistor at R48 to the T1 secondary transformer via L0+.

Note that the output of 3B also generates to a resistor divider consisting of the 150-kilohm resistor at R81 and the 137-kilohm resistor at R14, located at the positive terminal of operational amplifier 7B (pin 5), and to the 60.4-kilohm resistor at R26, located at the

negative terminal of 7B (pin 6). The resistor divider ensures that the voltages at pins 6 and 5 of 7B are equal. This inhibits oscillations by cancellation. (The 392-ohm resistor at R48 provides another resistor divider with the T1 secondary.)

OFF-HOOK DETECTION

To detect the off-hook status of the voice unit, an off-hook detector connects in series with the voice unit at all times. In addition, the voice unit can be connected to either of the interfaces (that is, the voice unit interface or the line interface) and the off-hook detector will still continue to operate.



(From Figure C-1, Page 3, Coordinate 2D)

As shown in the above window, bridge rectifier 1B, which has a low AC impedance, allows DC current to flow in either direction. For example, when current flows into 1B at pin 3 and out of 1B at pin 4, the current also flows out of 1B at pin 1 and into 1B at pin 2.

When the current flows out of 1B at pin 1, a voltage is impressed across pins 1 and 2 of optocoupler 2B. This causes an internal LED to turn on, which in turn causes an internal phototransistor to turn on. Therefore, an active-low signal is generated from pin 5 of 2B to pins 9 and 10 of AND gate 8F, where it is driven as VUOH- (Voice Unit Off-Hook) to the 8051 microprocessor, signifying that the voice unit is off hook.

Note that various amounts of current can flow in the voice unit loop, depending upon the proximity of the voice unit and the central office/PABX. Short loops consist of high current, and long loops consist of low current.

In the case of a short loop containing high current, the internal LED of 2B, which is rated at 60 mA of current, must be protected. In other words, with short loops, the current can be much greater than the 60 mA rating, causing the LED to burn out.

Therefore, when the current becomes larger than 20 mA, 33-ohm resistor R43 develops about 0.7 V across it that biases transistor Q8, causing Q8 to turn on. Transistor Q8 protects the LED by shunting current around it.

(Note that 226-ohm resistor R42 provides a 5-mA threshold to shunt current around the internal LED at pins 1 and 2 of 2B.)

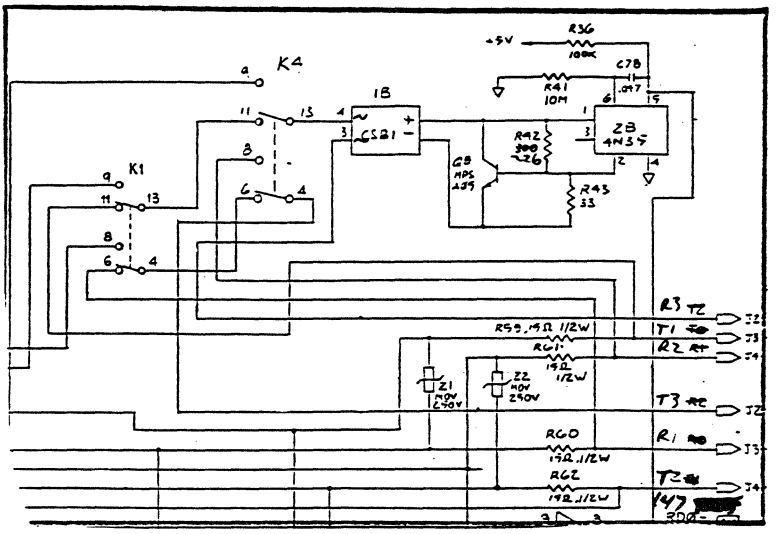
The 100-kilohm resistor at R36 and the 0.047-microfarad capacitor at C78 integrate the signal to filter variations in the loop current.

The 10-Megohm resistor at R41 connects to the base of the internal phototransistor to drain transistor leakage current, which would otherwise charge C78 and turn on the phototransistor.

LINE 1 OR 2 IN PARALLEL WITH VOICE UNIT INTERFACE

The voice unit interface can be placed in parallel with line 1 or line 2. Each of these is described in the following subsections by giving an example of voice recording.

VOICE RECORDING LINE 1

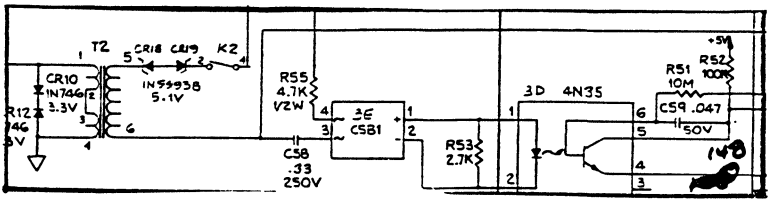


(From Figure C-1, Page 3, Coordinate 1C)

As shown in the above window, T3 (Tip 3) and R3 (Ring 3) are connected directly to the voice unit interface via connector J2, pins 5 and 4.

When recording a voice call, the following must occur:

- the recoder must be turned on
- the voice unit must be in parallel with line 1



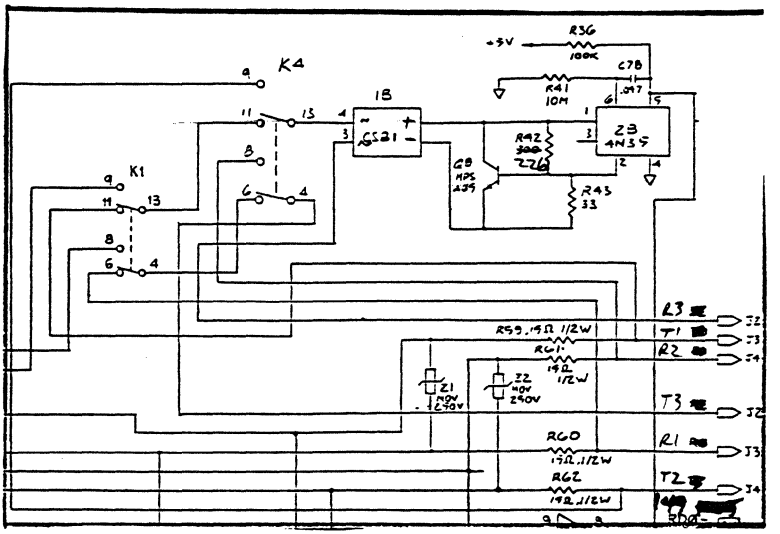
(From Figure C-1, Page 3, Coordinate 7C)

The above condition enures that the recorder can record both the near-end (that is, local) voice and the far-end voice. Both the near- and far-end voice are coupled into the encoder via T2, and directed to the CODEC encoder (that is, recorder).

Note that back-to-back zener diodes CR18 and CR19 turn on when loop current is present, to provide about 6 V across T1 and R1. This voltage is used to operate the telephone set that is across T1 and R1.

Telephones are voltage-sensitive as well as current-sensitive and need between 3 V and 5 V to operate properly. Therefore, CR18 and CR19 provide the voltage source necessary for the telephone to operate when the telephone is in parallel with line 1.

VOICE RECORDING LINE 2

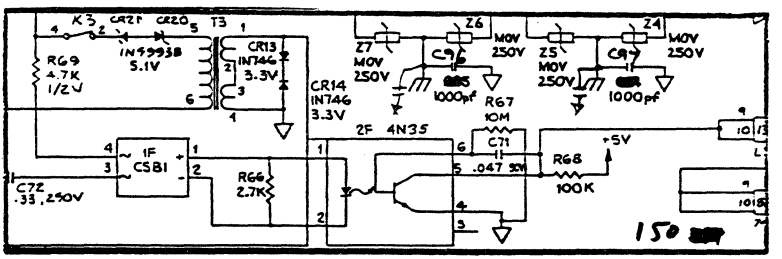


(From Figure C-1, Page 3, Coordinate 1C)

As shown in the above window, T3 (Tip 3) and R3 (Ring 3) are connected directly to the voice unit interface via connector J2, pins 4 and 5.

When recording a voice call, the following must occur:

- the recoder must be turned on
- the voice unit must be in parallel with line 2



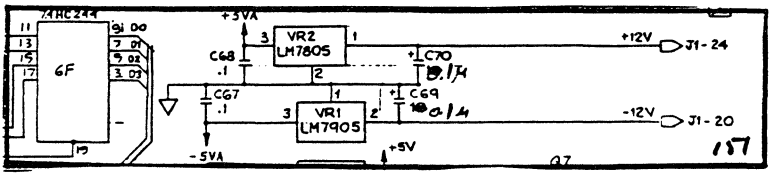
(From Figure C-1, Page 3, Coordinate 4C)

The above condition enures that the recorder can record both the near-end (that is, local) voice and the far-end voice. Both the near- and far-end voice are coupled into the encoder via T3, and directed to the CODEC encoder (that is, recorder).

Note that back-to-back zener diodes CR2Ø and CR21 turn on when loop current is present, to provide about 6 V across T2 and R2. This voltage is used to operate the telephone set that is across T2 and R2.

Telephones are voltage-sensitive as well as current-sensitive and need between 3 V and 5 V to operate properly. Therefore, CR2Ø and CR21 provide the voltage source necessary for the telephone to operate when the telephone is in parallel with line 2.

DC-TO-DC POWER CONVERSION



(From Figure C-1, Page 3, Coordinate 2A)

As shown in the above window, voltage regulator VR2 and VR1 provide the +5VA (+5 V) and -5VA (-5 V) ouputs for the analog circuitry on the Controller board.

The inputs of VR2 and VR1 are connected to +12V and -12V, repsectively, from the Modem board via connector J1, pin 24 and 2Ø.

Note that the Modem board also contains a DC-to-DC converter, which converts +36 V from the X-Bus power supply to +12V and -12V.

4 EXTERNAL INTERFACES

INTRODUCTION

This section defines specific hardware characteristics of the applicable Voice Processor Module interfaces. It illustrates the following external interfaces:

- Voice Processor Module voice unit phoneset line cord/plug
- Voice Processor Module standard modular line cord/plug
- Voice Processor Module loopback cord connector

Each subsection includes a description and diagram for connecting the Voice Processor Module to an external device.

VOICE UNIT PHONESET LINE CORD/PLUG

The voice unit phoneset line cord/plug is the interface between the Voice Processor Module and the voice unit (telephone).

The Voice Processor Module end of the cord consists of a customized plug while the other end consists of a standard RJ11 plug, as shown in the cabling drawing, below..

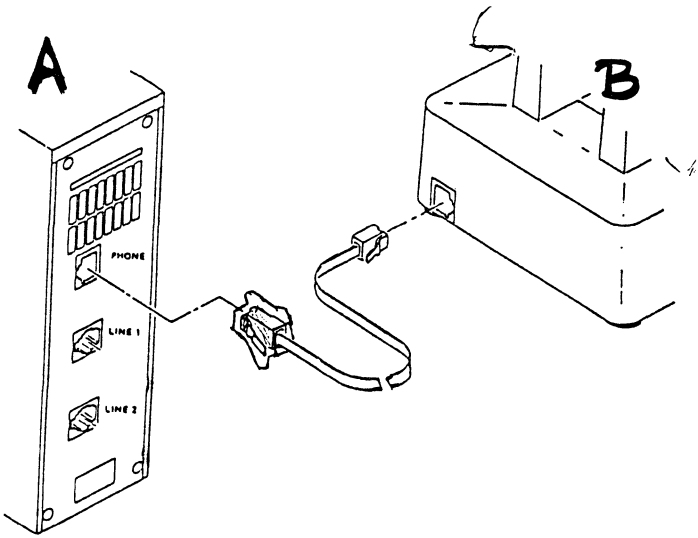
VOICE UNIT PHONESET CABLING

This section details the cable assembly for the voice unit phoneset interface.

Assembly: Voice Unit Phoneset Line Cord/Plug

Function: Used to connect the Voice Processor Module to a voice unit (telephone)

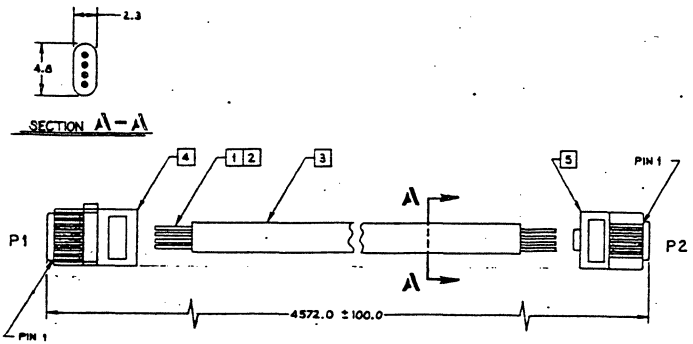
Connection:



Pin Assignments:

A Voice Processor	B Voice Unit	Color	Assignment
3	5	Black	A
4	4	Red	Tip
5	3	Green	Ring
6	2	Yellow	Al

Construction:



Notes:

1. Conductors (4 each) consist of 28 AWG (7 by 36) stranded tinned copper.

2. Insulation consists of Ø.3-mm thick (nominal) PVC or equivalent.

3. Jacket consists of black Ø.8-mm thick (nominal) PVC with a matte finish.

4. Part number A-41-ØØ3Ø7-ØØ.

5. Plug consists of 6-position/4-contact RJ11 modular line cord plug.

6. Conductors are laid in parallel.

7. Bag and tag with part number and revision.

MODULAR LINE CORD/PLUG

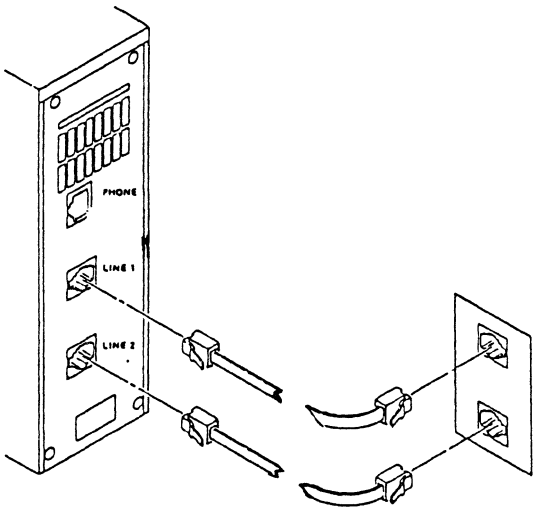
The modular line cord/plug consists of a standard RJ11 modular line cord and plug assembly, obtainable from most consumer electrical supply stores.

Pin assignments are not necessary for the modular line cord/plug.

Assembly: Modular Line Cord/Plug

Function: Used to connect the Voice Processor Module to a telephone line (central office/PABX)

Connection:



LOOPBACK CORD/CONNECTOR

The Voice Processor Module loopback cord/connector consists of a modular duplex jack, RJA2X (also known as an answering machine connector), and standard RJ11 modular line cord/plugs, which are easily obtainable from most consumer electrical supply stores.

The loopback cord/connector is used in conjunction with the phoneset line cord/plug and the RJ11 modular line cord/plug to perform the external loopback portion of the diagnostics.

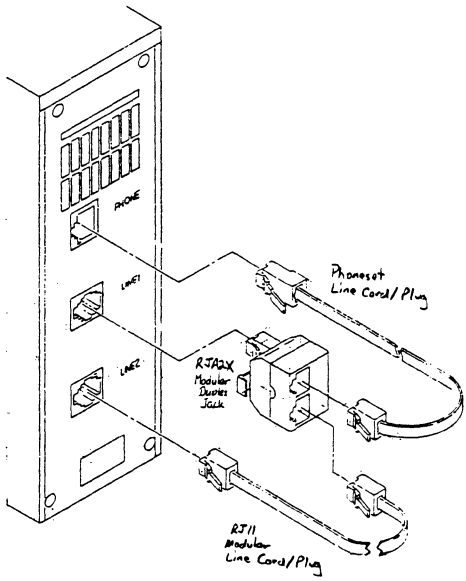
Construction of the phoneset line cord/plug and modular line cord/plug are described in the above sections.

Pin assignments are not necessary for the loopback cord/connector.

Assembly: Loopback Cord/Connector

Function: Used to run the Voice Processor Module external loopback portion of the diagnostics

Connection:



908-007

APPENDIX A: MODULE SPECIFICATIONS

POWER MODULE REQUIREMENTS

Power Code: 1 (7 W)

MODEM SPECIFICATIONS

SPEED

1200 baud, full duplex

300 baud, full duplex

COMPATIBILITY

Bell 212-A

Bell 103/113

MODULATION

High speed: PSK

Low speed: FSK

OPERATING MODES

Originate/answer

Full duplex

Asynchronous transmission

CHARACTER FORMAT

1 start bit/8 data bits/1 stop bit

VOICE OPERATIONS

24 Kbps/6 kHz sampling

32 Kbps/8 kHz sampling

PHYSICAL DIMENSIONS

HEIGHT

8 in. (203.2 mm)

WIDTH

2.52 in. (64 mm)

LENGTH

12 in. (304.8 mm)

WEIGHT

4.5 lb (2.05 kg)

ENVIRONMENTAL, SAFETY, AND REGULATORY

ALTITUDE

15,000 ft ASL (operating)

25,000 ft ASL (nonoperating)

TEMPERATURE/HUMIDITY

Operating: 0 to 40 degrees ^{o}C (32 to 104 ^{o}F); 90 percent RH at 65 degrees ^{o}C for 12 hr

Nonoperating: -40 to 75 ^{o}C (-40 to 167 ^{o}F); 90 percent RH at 65 degrees ^{o}C for 12 hr

ESD

5 kV:	No observable effect
12 kV:	Errors corrected via software intervention
17.5 kV:	Errors corrected via operator intervention
25 kV:	No permanent damage

SAFETY

Meets UL 478 (EDP) and 114 (office equipment)

Meets CSA 154 (EDP) and 143 (office equipment)

EMISSIONS

Meets FCC, part 15, subpart J for class A emissions

TELEPHONY

Registered for direct connection to the Public Telephone Network, under part 68 of the FCC rules

APPENDIX B: MODEM BOARD SPECIFICATIONS

INTRODUCTION

The Modem board functions as a nonintelligent 1200/300 bps modem, fully compatible with both the Western Electric 212A and CCITT recommendation V.22. This board interfaces to a 100-pin montherboard connector and does not have to be FCC, part 68, registered.

Connector pinouts are provided in Table B-1.

Table B-1. Modem Board Connector Pinouts. (Page 1 of 3)

Pin	Signal	Pin	Signal
1		2	
3	DGnd	4	DGnd
5		6	
7		8	
9		10	
11	DGnd	12	Transmit Data
13	Receive Data	14	Originate
15		16	PSK Carrier
17	DGnd	18	FSK Carrier
19	+12VDC	20	-12VDC
21	DGnd	22	
23	Analog Loopback	24	
25		26	
27		28	Enable PSK

Table B-1. Modem Board Connector Pinouts. (Page 2 of 3)

Pin	Signal	Pin	Signal
29		30	Enable FSK
31	DGnd	32	
33		34	
35		36	
37	Reset	38	Mode Select Ø
39	DGnd	40	Mode Select 1
41	AGnd	42	Mode Select 2
43	Audio	44	Mode Select 3
45	AGnd	46	
47		48	+5VDC
49	AGnd	50	+5VDC
51	DGnd	52	+5VDC
53		54	+36VDC
55		56	+36VDC
57		58	+36V Return
59	DGnd	60	+36V Return
61		62	
63		64	
65	DGnd	66	
67		68	
69		70	

Table B-1. Modem Board Connector Pinouts. (Page 3 of 3)

Pin	Signal	Pin	Signal
71	DGnd	72	
73		74	
75		76	
77	DGnd	78	
79		8Ø	
81		82	
83	DGnd	84	
85		86	
87		88	
89	DGnd	9Ø	
91		92	
93		94	DGnd
95		96	DGnd
97	DGnd	98	DGnd

ANALOG INTERFACE

As shown in Table B-1, pin 43 is dedicated for the 2-wire audio frequency signal. Specifications for this signal are given in the following subsections.

MODULATION

High Speed: PSK, dibit encoded

Low Speed: FSK

COMPATIBILITY

Western Electric 212A, including 300 bps operation with 103 and 113 series; CCITT recommendation V.22, alternative C

OPERATING MODES

Originate/answer, full duplex

PERFORMANCE CHARACTERISTICS

Transmit level: -11 dBm (at tip and ring)

Receive sensitivity: -43 dBm

Bit error rate: $1X10^{-5}$ for a signal-to-noise ratio of 12 dB with 300 to 3400 Hz Gaussian noise over a receive level range of 3 dB above the carrier detect threshold back-to-back (-40 dBm)

Maximum frequency offset (error free): 7 Hz measured with a -11 dBm transmit level and a -30 dBm receive level

Maximum phase jitter (error free): 20 degrees peak-to-peak (50 to 300 Hz) measured with a -11 dBm transmit level and a -30 dBm receive level

Error free region with phase hits: +/-20 degrees; 1 Hz rates with -11 dBm transmit level and a -30 dBm receive level

Error free region with sudden changes in amplitude: 1 Hz rate, 10 dB variation, transmit level at -4 dBm, receive level at -20 dBm

Error free region with impulsive noise: 1-sec rate, 0 to 1 millisec duration with a -11 dBm transmit level and a -30 dBm receive level

DIGITAL INTERFACE

All remaining connector signals are TTL/CMOS compatible, positive high (that is, high = 1 = +5 V; low = Ø = Ø V), with ouputs capable of driving two, and inputs presenting a load of one standard LSTTL gate. The following signals are provided:

- Transmit Data
- Receive Data
- Originate
- FSK Carrier Detect
- PSK Carrier Detect
- Enable PSK
- Enable FSK
- Analog Loopback
- Mode Select (4 bits)
- Reset

TRANSMIT AND RECEIVE DATA

When using 212 mode, these signals contain asynchronous digital data at a rate of 12ØØ bps (+1 percent -2.5 percent).

When using 1Ø3 mode, these signals contain asynchronous digital data at a rate of Ø to 3ØØ bps.

When using V.22 mode, these signals contain asynchronous digital data at a rate of 12ØØ bps (+1 percent - 2.5 percent).

ORIGINATE/ANSWER MODE

When driven by the system high, this signal indicates that the modem will operate in originate mode; when driven by the system low, this signal indicates that the modem will operate in answer mode.

FSK/PSK CARRIER DETECT

These signals are raised by the modem to indicate that a valid carrier signal is being received over the line, and that a data transfer can occur.

ENABLE FSK/PSK

When in originate mode, one of these signals is raised by the system to indicate that the appropriate modem section should be enabled.

When in answer mode, the enable PSK signal is raised and the enable FSK signal is lowered. When the modem responds with a carrier detect, the system will respond by raising the appropriate enable. (For example, the system sets the enable PSK, and resets the enable FSK and originate/answer. The modem will attempt to answer with PSK. If it is able to answer, the modem sets PSK carrier detect. The system will respond by setting the enable PSK, which is already set, and resetting the enable FSK, which is already reset. If the modem is unable to answer with PSK, it will attempt to answer with FSK. If it is able to answer, the modem will set the FSK carrier detect and the system will respond by setting the enable FSK and resetting the enable PSK.)

CHARACTER LENGTH

Characters are defined as 10 bits: 1 start (active low), 8 data/parity, and 1 stop (active high).

ANALOG LOOPBACK

This signal is raised by the system to cause the modem to enter an analog loopback test mode. It will not be changed by the system when the Reset signal is high.

MODE SELECT

Mode select Ø is the only mode selector currently used. It is low to indicate 103/212 and is high to indicate V.22.

These signals will not be changed by the system when the Reset signal is high.

RESET

The system drives this signal low to reset the modem electronics.

POWER REQUIREMENTS

The sytem provides the following voltages to the Modem board:

- o +5 VDC (500 mA)
- o +36 VDC, unregulated (400 mA)

The modem supplies the following voltages to the sytem:

- o +12 VDC (60 mA)
- o -12 VDC (50 mA)

EMI/EDS REQUIREMENTS

The Voice Processor Module meets FCC, class B, approval in regard to spurious emissions. The system also meets the following levels of electronic discharge susceptibility:

- o 10 kV - no effect
- o 15 kV - no hard errors
- o 25 kV - no permanent damage

For this reason, all unused board area (including the component side) is covered by a crosshatched ground grid, and the effective aspect ratio of component distance from the connector is equal to or less than 1:1.

ENVIRONMENTAL

Operating environment: Temperature, Ø to 7Ø degrees C (32 to 158 degrees F); 1Ø to 9Ø percent relative humidity, noncondensing

Storage temperature: -3Ø to +7Ø degrees C (-22 to 158 degrees F)

Operating/storage altitude pressure requirements: 86Ø to 1Ø6Ø mBar

APPENDIX C: DRAWINGS

This appendix contains the following drawings for the Voice Processor Module:

Figure	Drawing
C-1	Controller Board Schematic Diagram
C-2	Motherboard Wire List
C-3	Controller Board Printed Circuit Assembly
C-4	Motherboard Printed Circuit Assembly
C-5	Voice Processor Module Assembly
C-6	Voice Processor Module Chassis

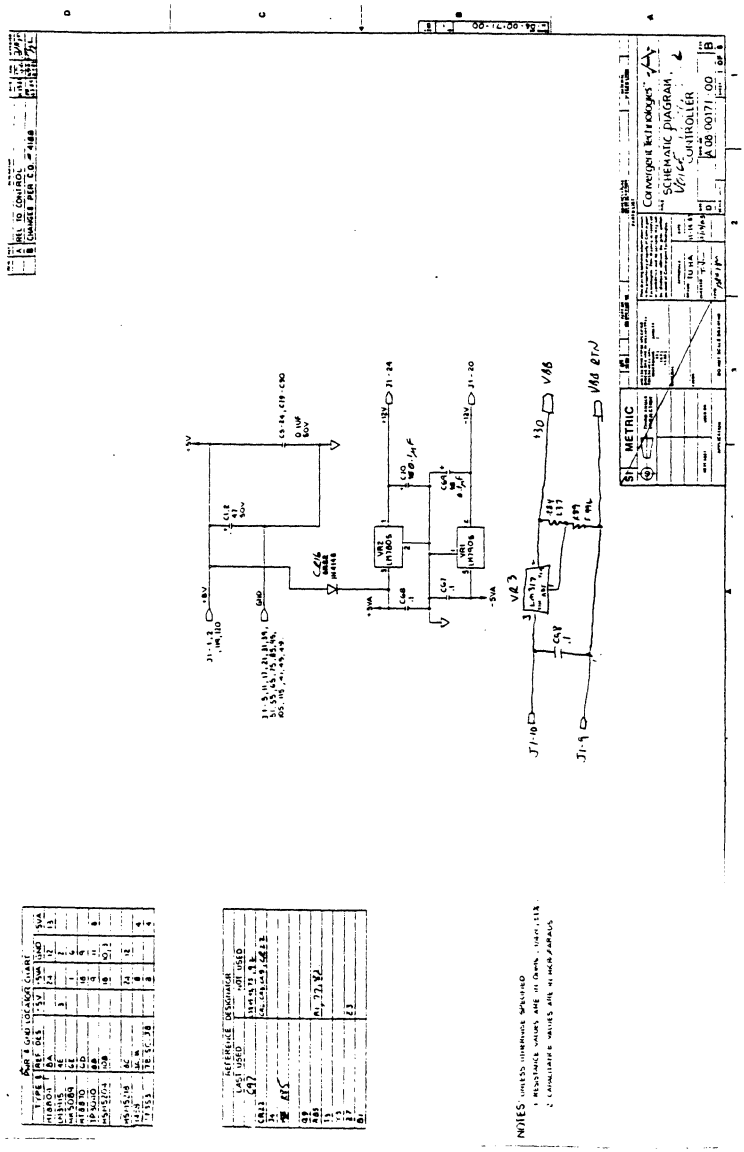


Figure C-1. Controller Board Schematic Diagram. (Page 1 of 8)

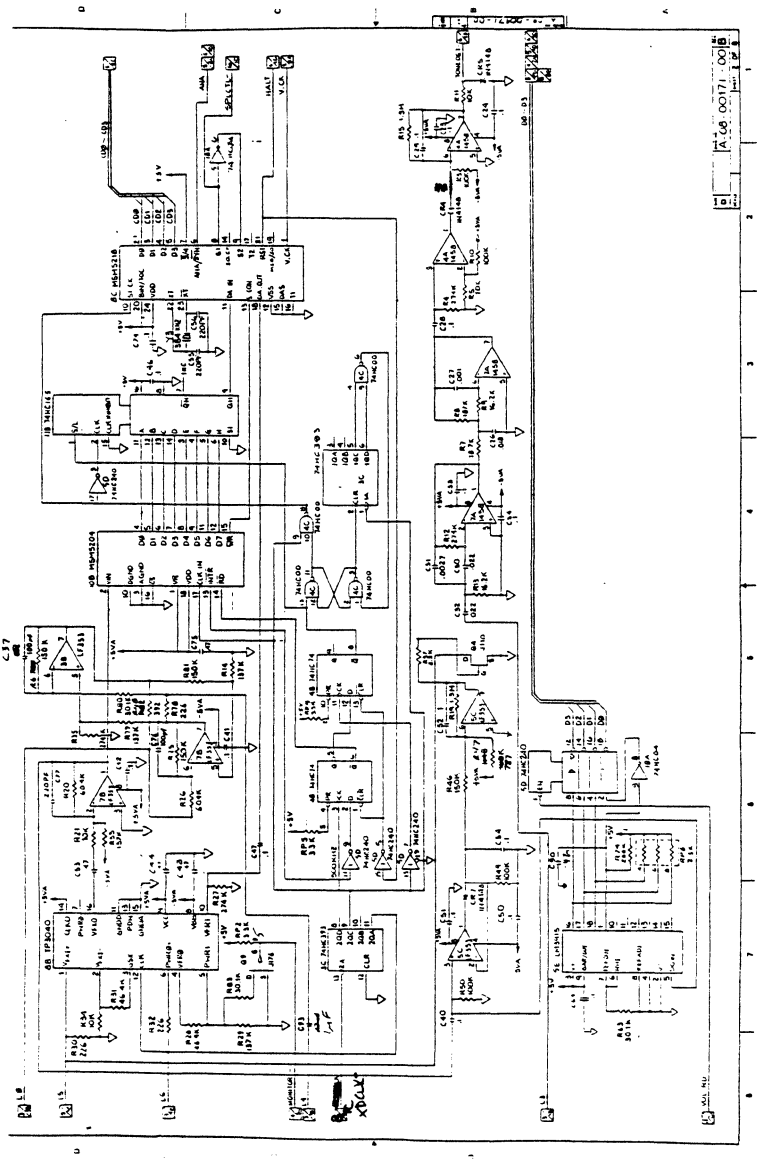


Figure C-1. Controller Board Schematic Diagram. (Page 2 of 8)

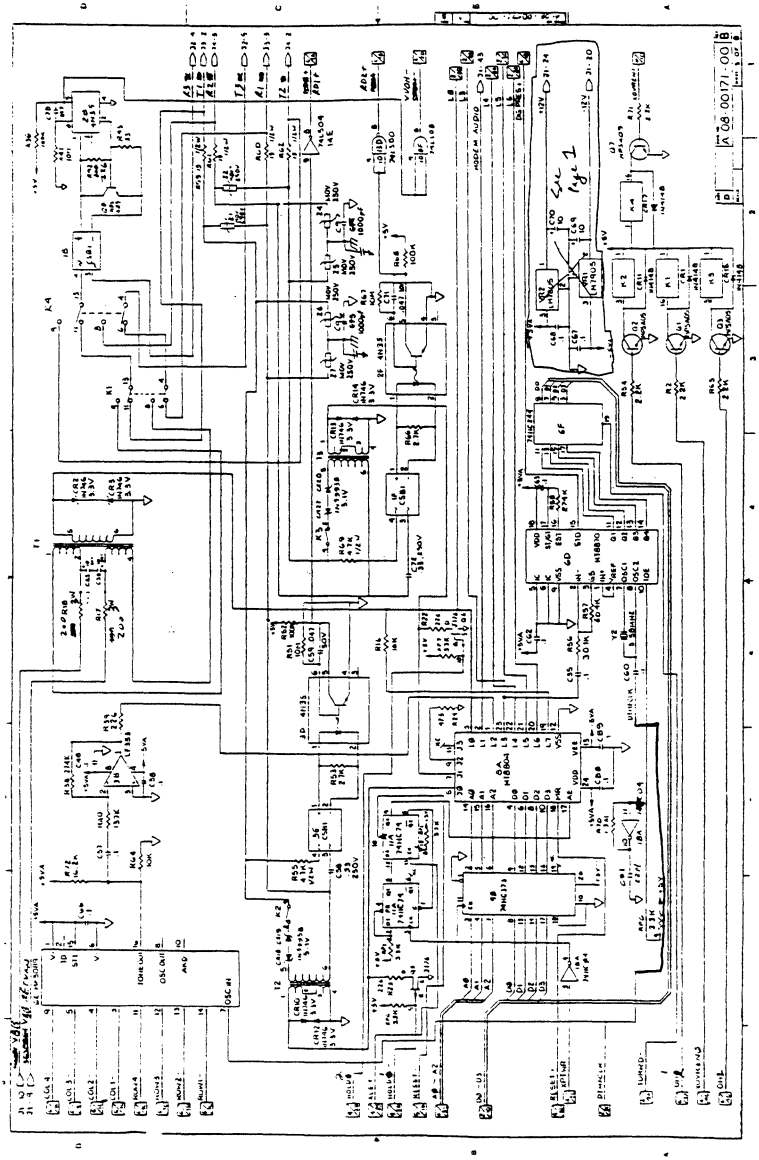


Figure C-1. Controller Board Schematic Diagram. (Page 3 of 8)

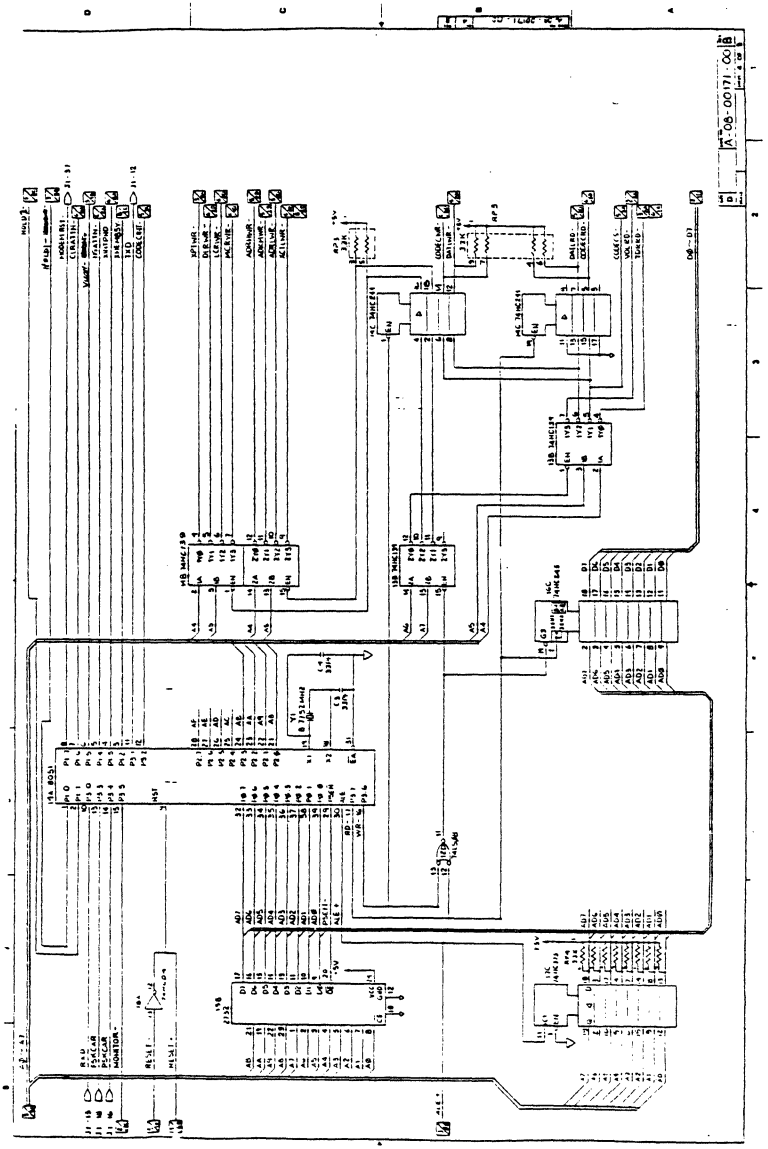


Figure C-1. Controller Board Schematic Diagram. (Page 4 of 8)

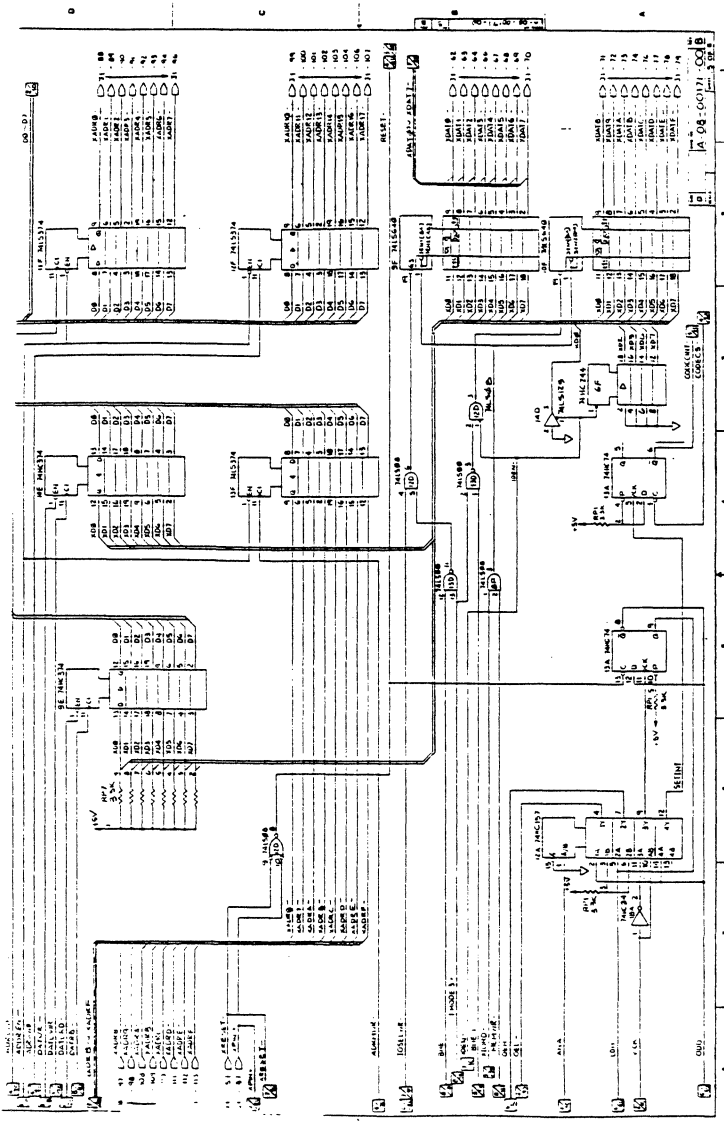


Figure C-1. Controller Board Schematic Diagram. Page 5 of 8)

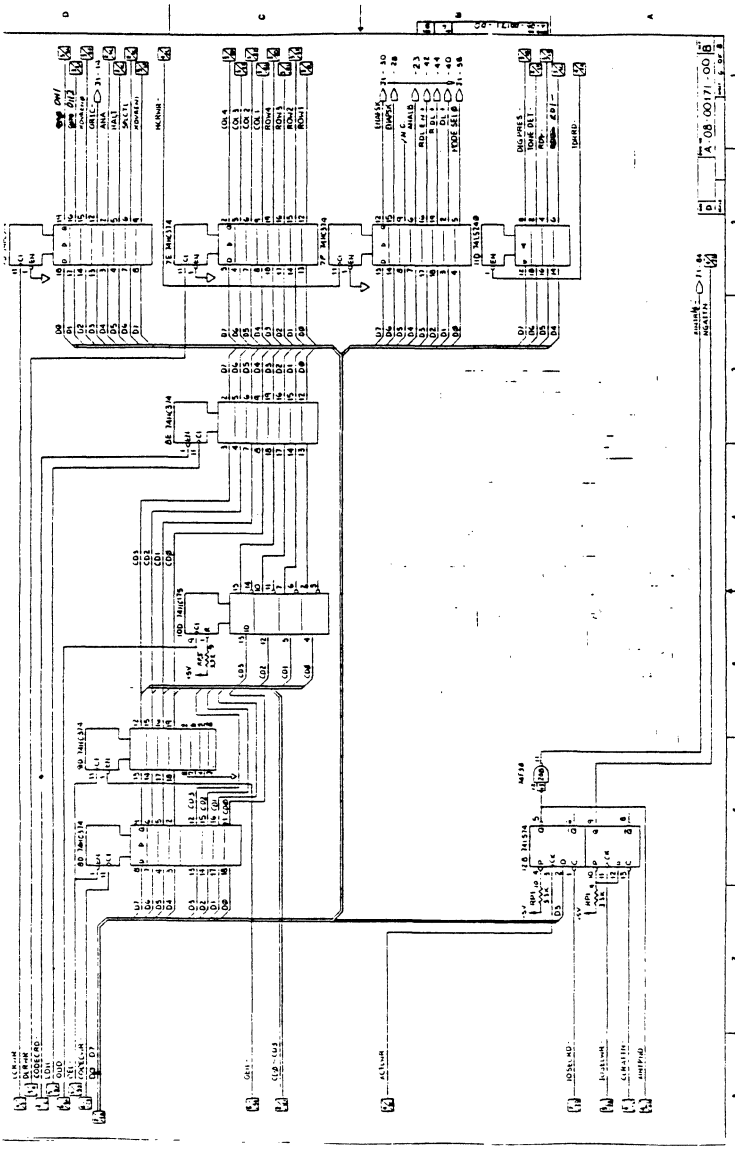


Figure C-1. Controller Board Schematic Diagram. (Page 6 of 8)

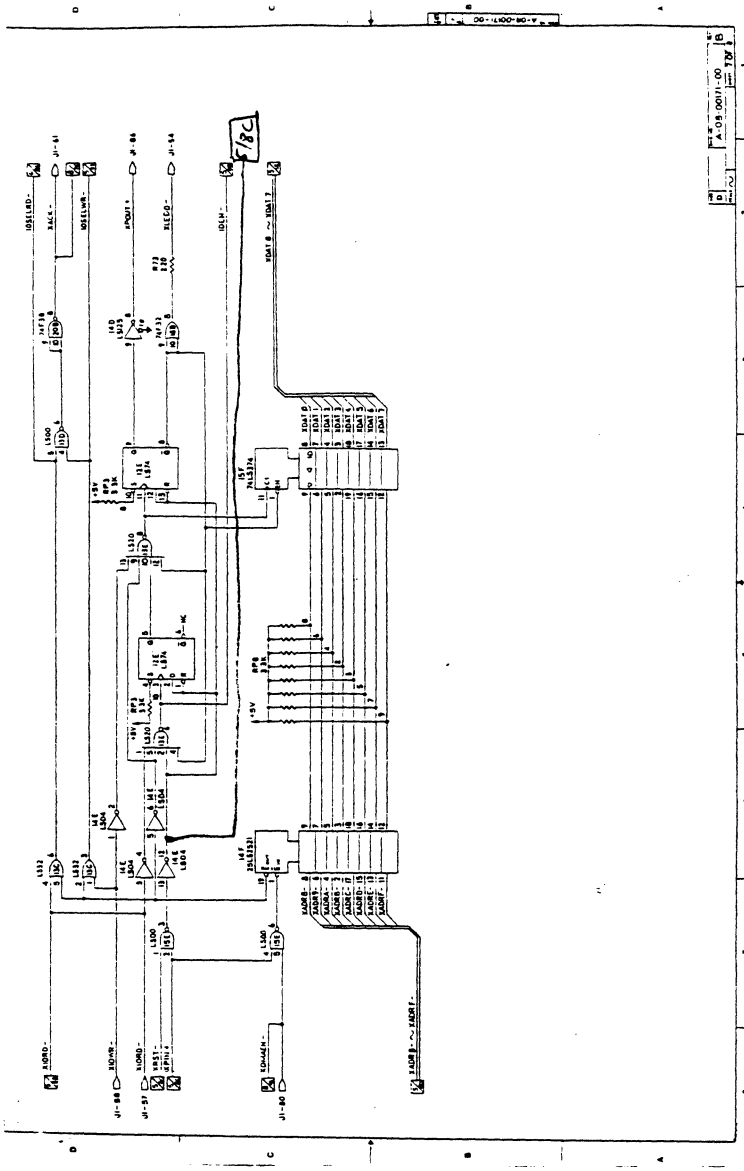


Figure C-1. Controller Board Schematic Diagram. (Page 7 of 8)

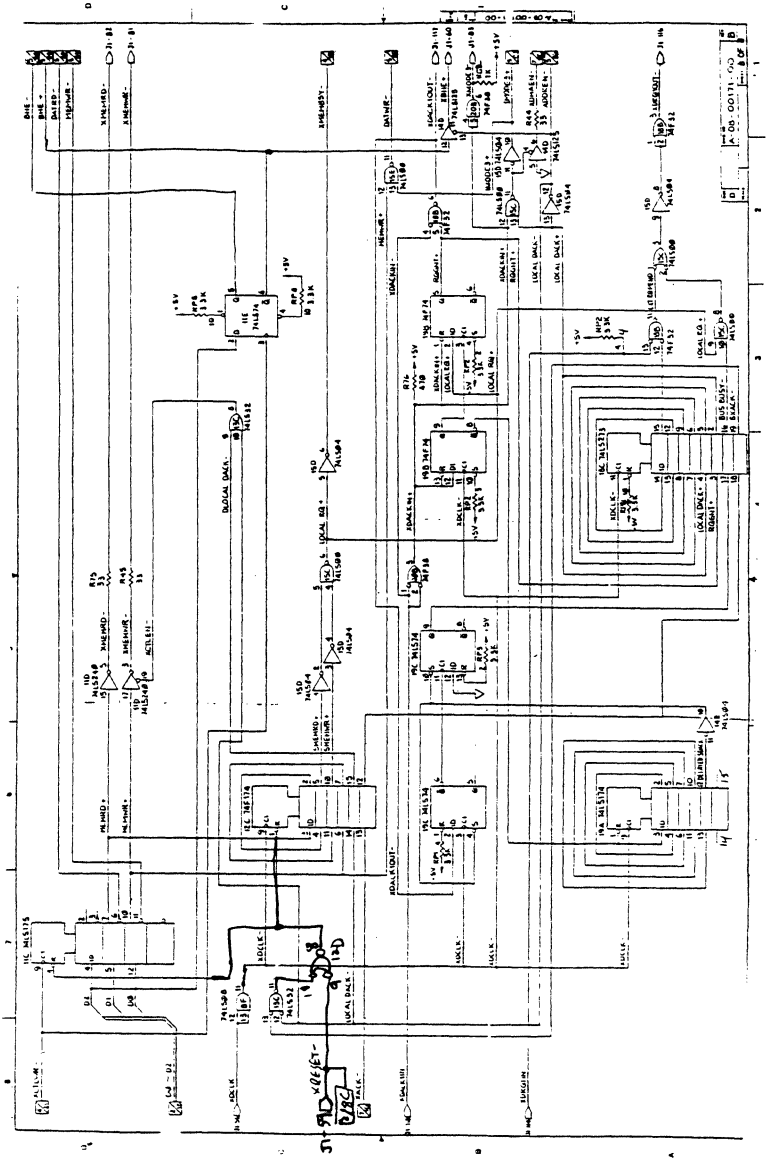
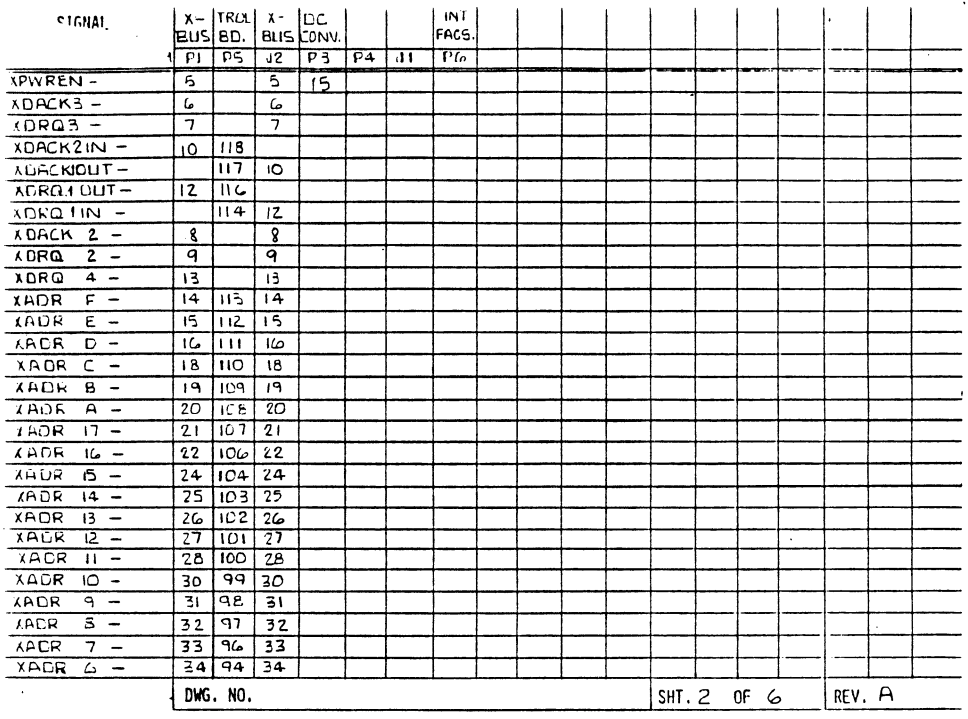


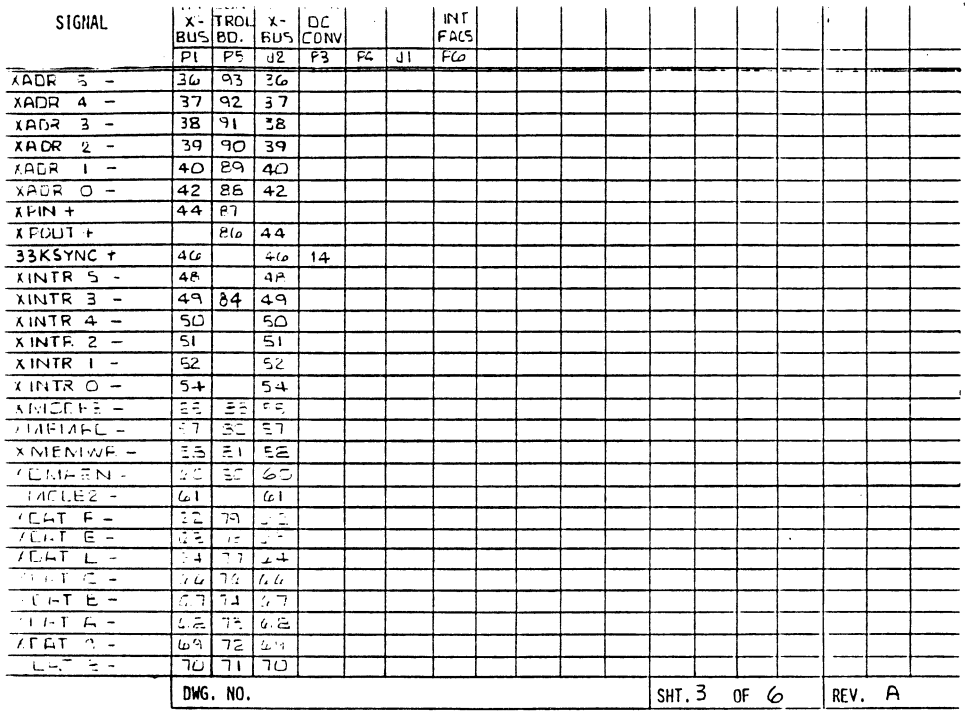
Figure C-1. Controller Board Schematic Diagram. (Page 8 of 8)

Figure C-2. Motherboard Wire List. (Page 1 of 6)



SIGNAL	X-BUS	TRCL BD.	X-BUS	DC CONV.			INT FACS.											
	P1	P5	J2	P3	P4	J1	P6											
XPWREN -	5		5	15														
XDACK3 -	6		6															
XDRQ3 -	7		7															
XDACK2IN -	10	118																
XDACKIOUT -		117	10															
XDRQ1 OUT -	12	116																
XDRQ1IN -		114	12															
XDACK 2 -	8		8															
XDRQ 2 -	9		9															
XDRQ 4 -	13		13															
XADR F -	14	113	14															
XADR E -	15	112	15															
XADR D -	16	111	16															
XADR C -	18	110	18															
XADR B -	19	109	19															
XADR A -	20	108	20															
XADR 17 -	21	107	21															
XADR 16 -	22	106	22															
XADR 15 -	24	104	24															
XADR 14 -	25	103	25															
XADR 13 -	26	102	26															
XADR 12 -	27	101	27															
XADR 11 -	28	100	28															
XADR 10 -	30	99	30															
XADR 9 -	31	98	31															
XADR 8 -	32	97	32															
XADR 7 -	33	96	33															
XADR 6 -	34	94	34															
	DWG. NO.													SHT. 2 OF 6			REV. A	

Figure C-2. Motherboard Wire List. (Page 2 of 6)



SIGNAL	X-BUS P1	TROL BD. P5	X-BUS J2	DC CONV P3	P4	J1	INT FACS P6
XADR 5 -	36	93	36				
XADR 4 -	37	92	37				
XADR 3 -	38	91	38				
XADR 2 -	39	90	39				
XADR 1 -	40	89	40				
XADR 0 -	42	86	42				
XPIN +	44	87					
XPOUT +		86	44				
33KSYNC +	46		46	14			
XINTR 5 -	48		48				
XINTR 3 -	49	84	49				
XINTR 4 -	50		50				
XINTR 2 -	51		51				
XINTR 1 -	52		52				
XINTR 0 -	54		54				
XMEMRE -	58	85	58				
XMEMWE -	57	80	57				
XMEMWR -	55	81	56				
XDMAEN -	60	80	60				
XCLK2 -	61		61				
XDAT F -	62	79	62				
XDAT E -	63	78	63				
XDAT D -	64	77	64				
XDAT C -	66	76	66				
XDAT B -	67	74	67				
XDAT A -	68	75	68				
XDAT 9 -	69	72	69				
XDAT 8 -	70	71	70				
	DWG. NO.						

SHT. 3 OF 6

REV. A

Figure C-2. Motherboard Wire List. (Page 3 of 6)

SIGNAL	X-BUS	TROL BD	X-BUS	DC CONV			INT FACE										
	P1	P5	J2	P3	P4	J1	P6										
XDAT 7 -	72	70	72														
XDAT 6 -	73	69	73														
XDAT 5 -	74	68	74														
XDAT 4 -	75	67	75														
XDAT 3 -	76	66	76														
XDAT 2 -	78	64	78														
XDAT 1 -	79	63	79														
XDAT 0 -	80	62	80														
XTRK -	81		81														
XACK -	82	61	82														
RESERVED1	84		84														
XBHE +	85	60	85														
XRESET -	86	59	86														
XIOWR -	91	58	91														
XIORD -	92	57	92														
XPCLK +	93		93														
XDCLK -	95	56	95														
XKBDRST -																	
XLED0 -		54															
XEOP -	87		87														
TXDATA		12					12										
RXDATA		13					13										
DRIG		14					14										
XDACK4 -	88		88														
PSKCAR		16					16										
FSKCAR		18					18										
ANALB		23					23										
PSKEN		28					28										
	DWG. NO.											SHT. 4 OF 6				REV. A	

Figure C-2. Motherboard Wire List. (Page 4 of 6)

SIGNAL	X+ BUS	TROL BD	X- BUS	DC CONV			INT FACS
	P1	P5	J2	P3	P4	J1	P6
FSKEN		30					30
MODEMRESET-		37					37
MODESEL 0		38					38
DL+		40					40
RDLEN +		42					42
RDL +		44					44
MODEM[illegible]		43					43
RESERVED2	90		90				
+5VDC		1		3			48
		2		4			50
		119		5			52
		120		6			
				7			
A GND		41					41
		45					45
		49					49
+12		24					19
-12		20					20
	DWG. NO.						SHT. 5 OF 6

REV. A

Figure C-2. Motherboard Wire List. (Page 5 of 6)

SIGNAL	X-BUS	TKUL BD	X-BUS	DC CONV			INT FACS
	P1	P5	J2	P3	P4	J1	P6
+36V RTN	109	9	109	2			58
	111		111				60
	113		113				
	115		115				
	117		117				
	119		119				
+36V DC A	110						
	112						
	114						
	116						
	118						
	120						
+36V DC B		10	110	1		1	54
			112			3	56
			114			5	
			116			7	
			118				
			120				

Figure C-2. Motherboard Wire List. (Page 6 of 6)

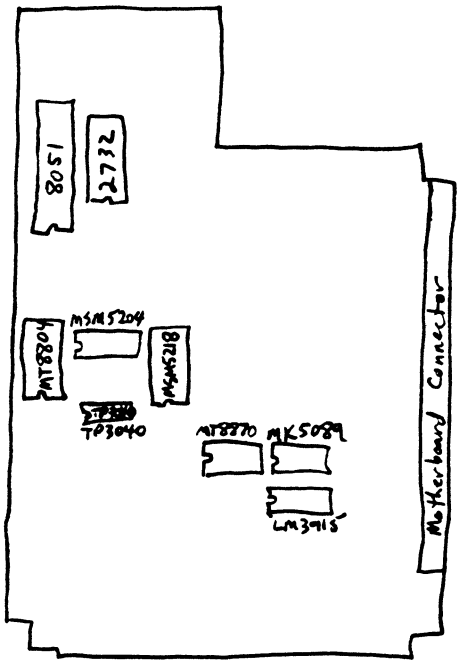


Figure C-3. Controller Board Printed Circuit Assembly.

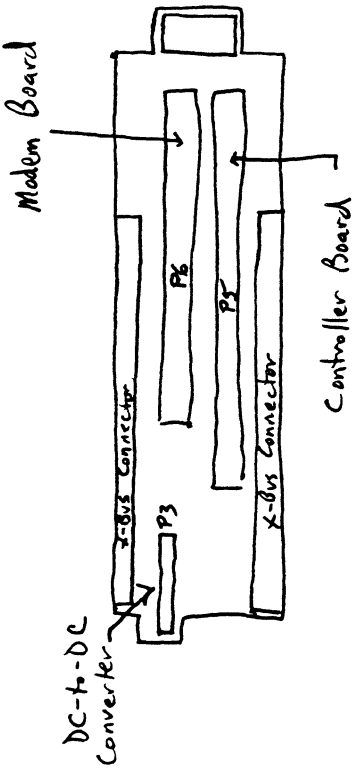


Figure C-4. Motherboard Printed Circuit Assembly.

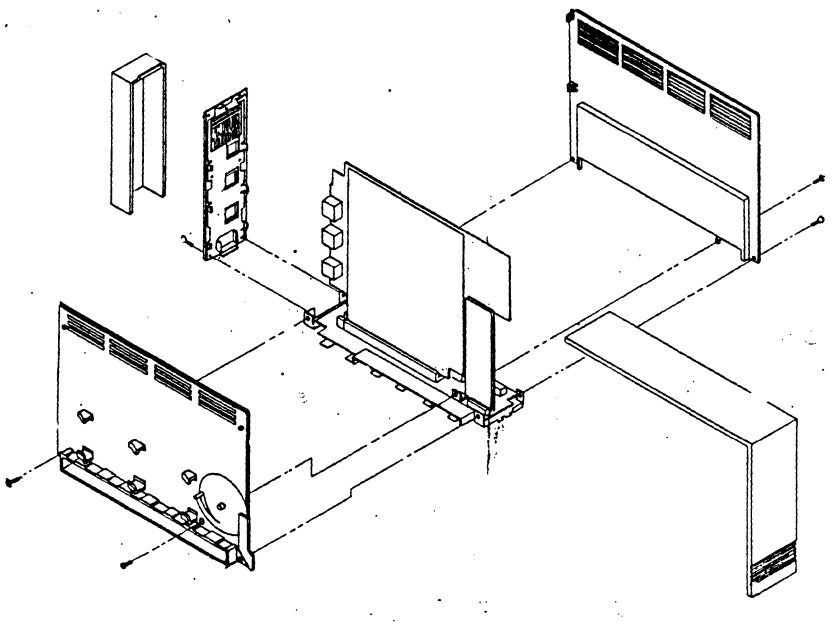


Figure C-5. Voice Processor Module Assembly.

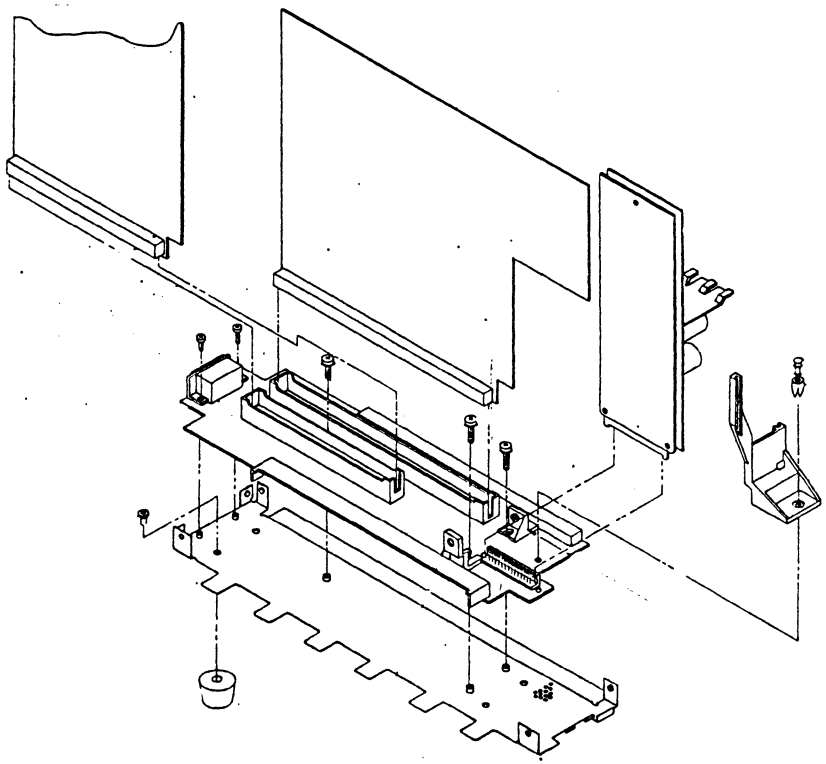


Figure C-6. Voice Processor Module Chassis.

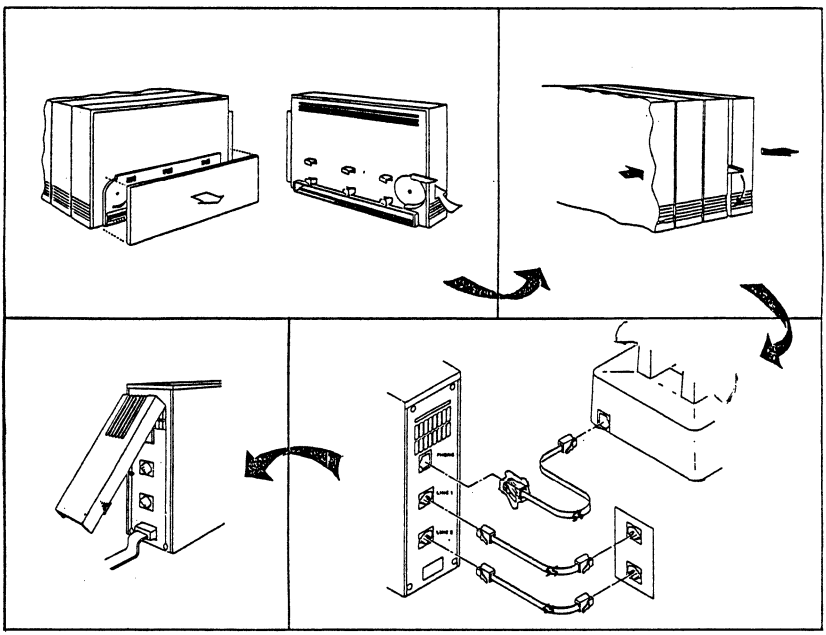
TROUBLESHOOTING QUICK REFERENCE CARD

Symptom	Possible Causes	See Section
Cannot dial out from keyboard Modem doesn't work No tone detection No CODEC functions No dial tone when off hook	Analog crosspoint switch (MT8804) malfunctioning	"Crosspoint Matrix Control"
	dc-to-dc converter on No tone Modem board malfunctioning	"DC-to-DC Power Conversion"
	DTMF generator (MK5089) or other CMOS chip latched up	"Tone Dialing"
	5V regulators not operating properly	"DC-to-DC Power Conversion"
	Address/data latch to the Analog crosspoint switch (MT8804) malfunctioning	"Crosspoint Matrix Control"
Cannot dial out from keyboard	DTMF generator (MK5089) malfunctioning	"Tone Dialing"
	One or more inputs to the DTMF generator (MK5089) not functioning properly	"General 8051 Microprocessor External RAM Registers"
	DTMF generator (MK5089) driving operational amplifier and corresponding circuitry not functioning properly	"Tone Dialing"
	DTMF generator (MK5089) latched up	"Tone Dialing"
	DTMF oscillator clock not from keyboard operating properly	"Tone Dialing"

Symptom	Possible Causes	See Section
No dial tone	Off-hook bridge rectifier, phototransistor, and associated circuitry not functioning properly	"Off-Hook" subsection in "Voice Unit Interface Circuitry"
	Line Ø relay or line 1 relay not working	"Line Interface Circuitry" and "Voice Unit Interface Circuitry"
	Relay drives not funtioning properly	"Line and Voice Unit Interface Relays"
No ringing; can dial out, but other party cannot dial in	Line interface Ø bridge rectifier, phototransistor,and other associated circuitry not functioning properly	"Line Interface Ring Detection" subsection in "Line Interface Circuitry"
	Line interface 1 bridge rectifier, phototransistor, and associated circuitry not functioning properly	"Line Interface Ring Detection" subsection in "Line Interface Circuitry"
Distortion when off-hook	Voice amplifier circuitry off-hook not functioning properly	"Call Placement to Telephone Line Interface" subsection in "Voice Unit Interface Circuitry"

Symptom	Possible Causes	See Section
Faint or no dial tone	Voice amplifier circuitry not functioning properly	"Call Placement to Telephone Line Interface" subsection in "Voice Unit Interface Circuitry"
Distorted dial tone	Voice amplifier circuitry not functioning properly	"Call Placement to Telephone Line Interface" subsection in "Voice Unit Interface Circuitry"
Cannot record voice	Silence detection circuitry not functioning properly	"Silence Detection and Volume Status"
	PCM filter (TP3040) input not functioning properly	"Pulse Code Modulation Filtering"
	Analog-to-digital converter (MSM5204) input not functioning properly	"Analog-to-Digital Conversion"
	Bitstream between shift register and CODEC (MSM5218) inaccurate	"Analog-to-Digital Conversion" and "CODEC logic"
	Input to CODEC (MSM5218) inaccurate	"CODEC Logic"
	Inaccurate clock input to devices	"CODEC Logic"

Symptom	Possible Causes	See Section
Beginning of words clipped off	Silence detection driver (LM3915) malfunctioning	"Silence Detection and Volume Status"
	RC network at output of Silence detection driver (pin 1) not operating properly	"Silence Detection and Volume Status"
Voice Processor Module does not recognize dial tone	Call progress tone detection filter network circuitry not functioning properly	"Call Progress Tone Detection"
	Call progress tone detection comparator circuitry not functioning properly	"Call Progress Tone Detection"
Voice recording too loud or distorted	AGC circuitry not functioning properly	"Pulse Code Modulation Filtering"
LED does not light	X-Bus address or data lines are not accurate	"X-Bus Mode 3 Master Logic," "Address Bus Interface Logic," and "Data Bus Interface Logic"
	Improper base I/O address generated from Processor Module	"X-Bus Initialization/Identification Logic"



Place this Installation sheet in your Installation Guide