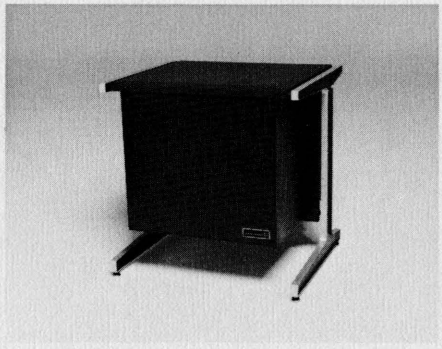
DATAPOINT CORPORATION
Product Specification

Channel Adapter
9426



The 9426 Channel Adapter (also available in a console mount.)

August 7, 1979 Document no. 60829

1.0 General Description

The 9426 Channel Adapter interfaces with an IBM System 360/370 by emulating with hardware and software certain IBM I/O devices found on a byte multiplexor channel -- most commonly unit record devices such as card readers, card punches, and line printers.

The Adapter is compatible with the Datapoint 5500 and 6600 I/O busses. It has 4K of data buffers, organized into 16 pages of 256 bytes per page, plus control memory consisting of 16 pages or buffers of 16 bytes each. A microprocessor controls all data transfer and IBM I/O interface activity; firmware resides in a PROM. The Adapter monitors IBM Channel sequences and steps the microprocessor through them.

The Channel Adapter is used as part of three different but similar Datapoint software products: DASP™, DCIO, and MLCI.

DASP -- Datapoint Attached Support Processor -- is a combination hardware and software product used in conjunction with the Channel Adapter to enable Batch Telecommunications with an IBM System 360, Model 30 (equivalent or above) mainframe. A description of this system product is given in the DASP Product Specification, Document no. 60673.

DCIO -- Direct Channel Interface Option -- is a combined hardware/software product used in conjunction with the Channel Adapter to enable an IBM mainframe to access the resources of a Datapoint ARC™ system in a manner analogous to that of a Datapoint Attached Processor. This system product is described in the DCIO Product Specification, Document no. 60674.

MLCI -- MULTILINK™ Channel Interface -- a software product used in conjunction with the Channel Adapter to enable ON-LINE interactive inquiry into the database of an IBM System 360/370 from terminals of a Datapoint DATASHARE® system. The MLCI Product Specification, Document no. 60641, describes this system product.

The software component of each of these systems executes in a Datapoint processor connected to the 9426/9427 Channel Adapter. This controlling software is referred to hereafter as the Datapoint processor software program, or software driver.

2.0 System Requirements

The Channel Adapter is compatible with the Datapoint 5500 and 6600 I/O interfaces. On the IBM side, the Adapter will be connected to the Byte Multiplexor Channel.

3.0 Technical Description

3.1 Channel Adapter Components

The Adapter consists of the following major components:

-Interface I Logic Card (Datapoint Interface and Control Logic
-Memory Logic Card (Control and Data Buffers)
-Microprocessor Logic Card
-Sequencer Logic Card (IBM I/O Interface Control)
-Interface II (IBM compatible Drivers and Receivers)
-Power Supply

(See figure 3-1 for a block diagram of the Adapter.)

3.1.1 Interface I Logic Card

The Interface I Logic Card provides the necessary logic to implement a standard Datapoint I/O interface. It is compatible with the Datapoint 5500 and 6600 I/O Busses. In addition to providing an interface for the Adapter it furnishes the Adapter a built-in Channel sequence Simulator (for test purposes) controlled from the connecting Datapoint Processor.

3.1.2 Interface II Logic Card

The Interface II Logic Card contains the necessary line drivers and receivers for the IBM I/O interface as well as the Power On/Power Off sequence relays. Other major components on the card include the Select Out/Hold Out latch, the Select Out propagation circuitry, and the Power On Reset (POR) circuitry for the Channel Adapter.

3.1.3 Memory Logic Card

The Memory Card provides 4K (4096) bytes of data buffers organized into 16 pages of 256 bytes each, as well as a 64 byte deep Activity queue (a First-In, First-Out memory) and control buffers organized in 16 pages of 16 bytes. It also contains the control logic necessary to provide dual port access (between the microprocessor and the Datapoint 5500/6600) to both the Control and Data Buffers.

3.1.4 Microprocessor Card

The microprocessor and microprogram are the major control components of the Adapter. Through the microprocessor, the microprogram (which resides in the PROM on the card) controls and monitors all data transmissions and IBM I/O interface activity, except for the Control Unit Busy Sequence.

3.1.5 Sequencer Card

The Sequencer Card monitors the IBM Channel sequences and steps the

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microprocessor through them. It also provides address decoding logic for the IBM Channel Interface, and logic for the short Control Unit Busy sequence.

3.1.6 Power Supply

The power supply, a switching regulator type similar to the Version III power supply in the Datapoint 6600 processor, is contained in a module located at the rear of the unit. It provides all necessary logic power for Adapter operaton, and the power interlock circuitry.

3.2 Operation and Programming Definitions

The Datapoint Channel Adapter together with its associated Datapoint processor and software performs the function of an IBM System 360/370 control unit, accomplishing data transfer through emulation. The devices it emulates may vary with software changes, but the most common ones are unit record type I/O devices (Card Readers, Card Punches, and Line Printers).

The Datapoint hardware and software can also emulate an IBM 1052 Printer-Keyboard, using the Datapoint processor's CRT and keyboard for control of the System 360/370.

3.2.1 Structure of IBM Control Units

Nearly all I/O devices which attach to an IBM System 360/370 do so through a control unit, which may be integrated into the device or be a separate, stand-alone item. Such control units are attached to the Channel through a standard I/O interface: a group of connecting lines that carry data and control information between the control unit and the Channel, which is a device that controls the transmission of data between the IBM Central Processing Unit and the I/O devices, or from these components to main storage.

3.2.2 Control of the Channel Adapter

Control of the Adapter relies upon a very few external switches and indicators. Most operational control is done by the software program in the Datapoint processor. The user does not need to know how the software program works in order to make it perform.

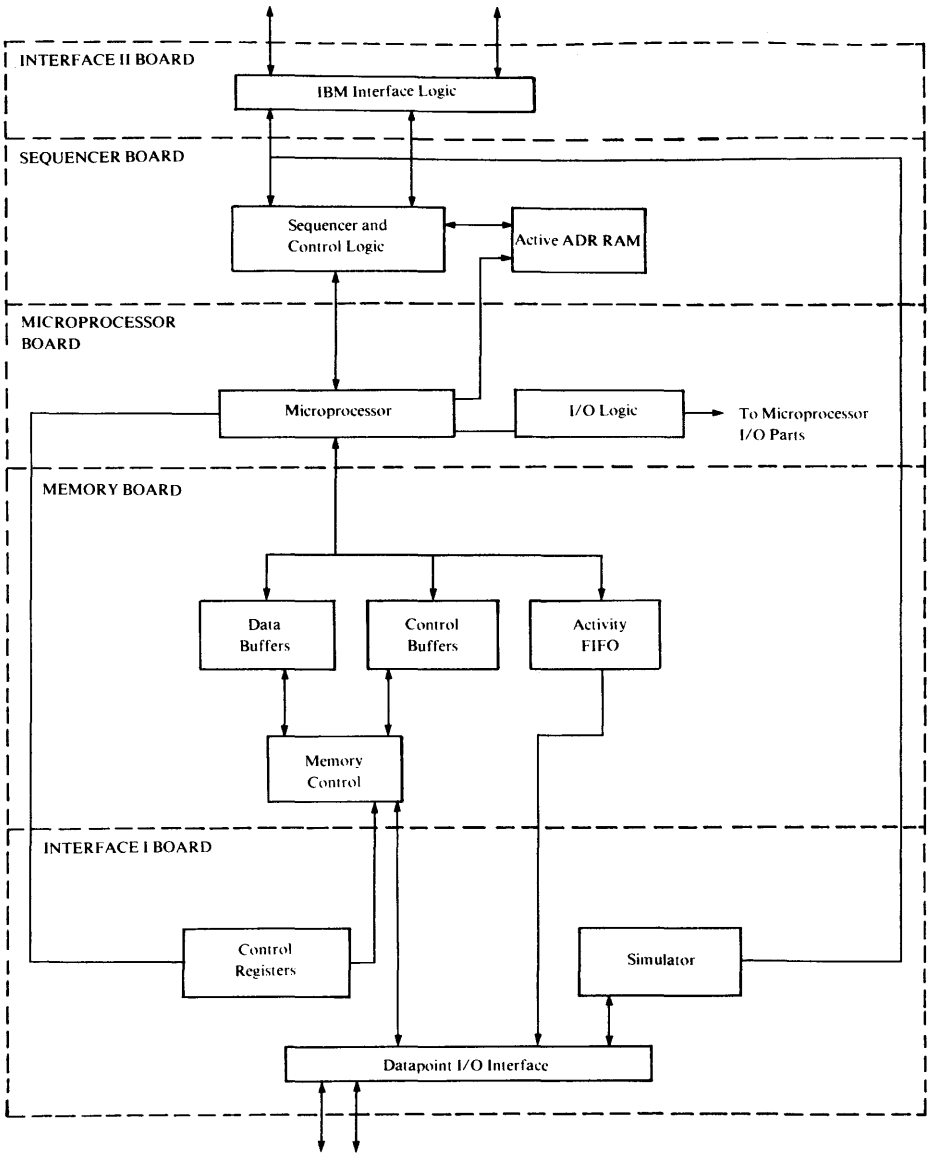


Figure 3-1 Adapter Block Diagram

He need know only how to instruct it, by entering responses at the processor keyboard to questions displayed on the processor screen, to carry out certain built-in functions.

For example, many different devices may be emulated merely by changing selected parameters of the software control program.

3.2.3 Operator Controls and Indicators

Operator controls consist of three switches and three indicators located on both the front and rear panels of the Adapter.

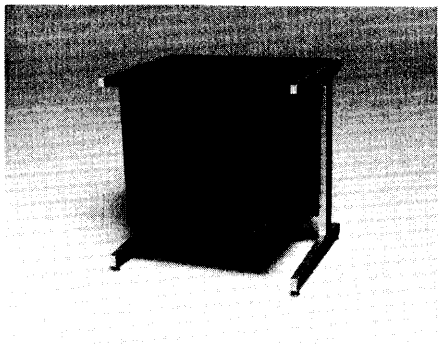
Front panel controls are as follows:
- On Indicator Light
- On-Line Indicator Light
- Operate Indicator Light
- Controlled Power On/Off Switch

ON Indicator-The ON indicator lights when power has been applied. The following conditions must be met before this indicator will light or the Channel Adapter will work:

Both the Main Power On/Off switch and the Controlled Power On/Off Switch must be in their "on" positions and the Adapter must sense the +12VDC I/O power available from the connecting Datapoint processor -- which means the processor must also be "on" and its I/O cable connected to the Adapter. The operate/test switch should be in the operate position.

ON-LINE Indicator-The ON-LINE Indicator lights when the Adapter is brought "on-line" to either the IBM System 360/370 Channel or the built-in Channel Simulator. It does not light when the Adapter is "off-line" to either the Channel or the Simulator.

OPERATE Indicator-The Operate indicator



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lights when the Adapter is in the "Operate" mode.

CONTROLLED POWER ON/OFF SWITCH-

A double-throw switch is used to apply power to the Adapter. The switch will apply power only

- when it is moved to its "on" position
- the connecting Datapoint processor is also powered on
- Adapter Main Power On/Off Switch is "on," and AC Power present at the Adapter

Note that the Datapoint processor must be powered up before the Adapter is powered up.

Once turned on, the Controlled Power On/Off switch is only active when the following conditions have been met:

- The Adapter is not ON-LINE to either the IBM System 360/370 Channel or to the built-in Simulator.

In other words, when the Adapter is ON-LINE to the Channel or the Simulator, the Controlled Power On/Off Switch cannot be operated. (Note that moving the switch from its "on" to its "off" position while the ON-LINE indicator is lit will not result in powering down the Adapter. The Controlled Power On/Off Switch may, however, be over-ridden by the Main Power On/Off switch (located at the rear of the Adapter) during emergencies.

Rear panel controls consist of two switches:

- Main Power On/Off Switch
- Operate/Test Switch

Main Power ON/OFF Switch-Controls the main AC power into the Adapter and is the main AC circuit breaker, rated at 5.0 AMP. It is independent of all interlocks and, when thrown open, immediately cuts AC power to the Adapter.

Normally this switch should not be used to power off the Adapter, as it may cause disturbances to the System 360/370 I/O interface. However, it should be in the Off position whenever the Adapter is to be serviced.

Should an overload condition open the circuit breaker, always have qualified maintenance personnel investigate and correct the cause of the overload before resetting the circuit breaker by moving the switch to the "ON" position. Otherwise, the same condition may open the breaker again, with possibly disastrous results.

OPERATE/TEST Switch-This switch is used to control the operating mode of the Adapter when it is brought ON-LINE. It should be set to the Operate position except when the Adapter is being serviced by field maintenance personnel. With the Operate/Test switch in Test position, the Adapter will be brought up ON-LINE to the built-in Simulator; it cannot be brought on-line to the host multiplexor Channel. However, once the Adapter is brought ON-LINE by the driver software, the mode of operation will not be changed by moving the switch. The Operate/Test Switch is only effective when the Adapter is OFF- Line to both the Channel and the built-in Simulator.

3.2.4 Datapoint Software Control Definitions

This section sets forth all control sequences, status, and command formats which may be issued by the Datapoint processor to the Channel Adapter.

3.2.4.1 EX ADR

The Adapter is addressed by executing an EX ADR instruction with the correct device address in the processor's A register. The factory-strapped address is an octal 0215. (This address may be changed in the field by modifying the address strapping on the Interface I Logic Card.)

Executing an EX ADR sets status bit 0 of the Adapter status byte and places the Adapter in the status mode.

3.2.4.2 Status Byte

Execution of either an EX ADR or an EX STATUS instruction makes the Adapter status byte in the Status Register available to the software during the subsequent execution of an INPUT instruction. Either an EX ADR or an EX STATUS places the Adapter into its Status mode.

Care should be taken when examining the contents of the Adapter status register because it is only updated after an EX ADR, EX STATUS, or INPUT instruction is executed. To be certain that the current status is being accessed, use an EX STATUS instruction immediately before an INPUT instruction.

The Adapter status byte has the following format and bit definitions:

Bit

0 - .....Adapter Addressed
1 - .....ON-LINE & Configured
2 - .....Address Available
0 = FIFO Buffer Empty
1 = FIFO Buffer Full
3 - .....Adapter BUSY
4 - .....System RESET
5 - .....Illegal Operation
6 - .....Status Modifier
7 - .....Reserved

Bit 0 - Adapter Address -This bit is a logical 1 whenever the Adapter is addressed by the Datapoint processor.

Bit 1 - On-Line and Configured - This bit is a logical 1 whenever the Adapter is ON-LINE. It is a software duplication of the ON-LINE indicator located on the Adapter's front panel. This bit will remain on until the Adapter has gone OFF-LINE, following an OFF- LINE EX COM1 instruction.

Bit 2 - Address Available -This bit is a logical 1 whenever the Adapter has placed a Logical Buffer Address into the Activity FIFO memory. It remains on until the contents of the FIFO memory have been exhausted by the driver software. That is, the bit is off whenever the FIFO memory is empty.

Bit 3 - Adapter Busy -This bit is a logical 1 whenever the Adapter cannot execute or is executing the previous EX COM1 instruction. It is turned on upon receipt of an EX COM1, and is not reset until the Adapter has either completed execution of the EX COM1 or acknowledged receipt of the EX COM1. (See definitions of EX COM1 instruction.) The driver software should not attempt to execute another EX COM1 instruction until this bit is reset.

Bit 4 - System Reset Received This bit is set upon receipt by the Adapter from the IBM Channel of a System Reset. It is reset when a

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System Clear is executed by the Adapter in response to a System Clear EX COM1 instruction.

Bit 5 - Illegal Operation on Last EX COM1 This bit is set whenever the last received EX COM1 instruction was detected as an invalid command. It is reset upon receipt of the next valid EX COM1 instruction.

Bit 6 - Status Modifier - This bit is set when the last received EX COM1 instruction was a New Sequence EX COM1, and was detected as an invalid instruction. It is reset upon receipt of the next valid EX COM1 instruction.

3.2.4.3 EX COM1

An EX COM1 instruction is the means whereby the driver software responds to Adapter requests for service, or issues instructions to the Adapter. When an EX COM1 instruction is executed by the Datapoint processor, the contents of its A-register are loaded into the COM1 register on the Interface I logic card. In addition, the contents of the COM3 register are loaded into the Auxiliary Logical Address register on the Interface I logic card. Execution of an EX COM1 sets status bit 3. An EX COM1 should not be executed while status bit 3 is set.

The EX COM1 instruction byte has the following bit definitions:

0 - .....Master Clear
1 - .....Configure System
2 - .....System Clear
3 - .....On-Line
4 - .....Off-Line
5 - .....Initiate Sequence
6 - .....Send Asynchronous Status
7 - .....Reserved

Bit 0 - Master Clear - If set True, this resets the sixteen control buffers and the active address RAM to zero. It also clears the Activity FIFO memory and the status register. Upon execution of the Master Clear EX COM1, the Busy bit (bit 3 of status register) will be set until the Adapter has completed execution of the Master Clear.

Bit 1 - Configure System - This commands the microprogram to configure the active address RAM for ON-LINE operation. The microprogram scans the control buffers for a Active Bit being set, indicating that the control buffer is to be an active logical buffer and that byte zero of the buffer contains the Channel Address to be used in configuring the active address RAM. Both the Active Bit and the Channel Address must be set up in the control buffers by the software before issuing the Configure System command. The Busy bit (status bit 3) is set until the Adapter acknowledges receipt of the command.

Bit 2 - System Clear - This resets the sixteen control buffers, except byte zero and the Active bit of byte seven. It also clears the Activity FIFO memory and the status register. A System Clear instruction should only be issued to the Adapter in response to a System Reset indication when the Adapter is ON-LINE. The Busy bit is set until the Adapter acknowledges receipt of the command.

Bit 3 - On-Line - Setting this bit True commands the Adapter to go ON-LINE to either the IBM Channel or the built-in Simulator -- depending on the position of the OPERATE/TEST switch. The ON-LINE EX COM1 instruction should only be issued to the Adapter when bit 1 of the status byte is not set -- that is, the Adapter is OFF-LINE. The busy bit (status bit 3) is set until the Adapter has successfully gone ON-LINE to either the IBM Channel or the built-in Simulator.

Note, however, that this will not happen until a SYSTEM/WAIT transition occurs.

Bit 4 - Off-Line - Setting this bit True commands the Adapter to go OFF- LINE to either the IBM Channel or the built-in Simulator -- depending on the position of the OPERATE/TEST switch. An Off-Line EX COM1 instruction should only be issued when the Adapter is in the ON-LINE state (Status bit 1 is set). The Busy bit (status bit 3) is set upon receipt of the command and remains set until the Adapter has acknowledged receipt of the instruction. Note that this command may not result in immediate execution, depending upon the current state of the Adapter. The Adapter must be completely idle before its microprogram will allow it to go off-line.

If an OFF-LINE EX COM1 is issued when the Adapter is not in an idle state, the microprogram will "store" it until the Adapter can successfully execute it. Once the Adapter has achieved the off-line state, bit 1 of the status byte is set low (logical zero). The idle state is defined as:

- No current outstanding Channel commands are awaiting completion.
- The Adapter is not currently engaged in receiving a new incoming command.
- The Adapter is not engaged in sending Asynchronous Status.

Until the above conditions exist, the Adapter will continue to function as if the OFF-LINE command had not been sent.

Bit 5 - Initiate Sequence - Setting this bit True commands the Adapter to begin execution of a new sequence as specified in byte three of the control buffer (see control buffer definitions). The address of the specific control buffer (logical buffer address - LBA) is loaded into the Adapter's COM3 register before the execution of the EX COM1. (Upon receipt of an EX COM1 the Adapter loads the LBA into its Auxiliary Logical Address Register.)

Status bit 3 (Busy) will be set upon receipt of the Initiate Sequence command and will remain set until the Adapter's microprogram acknowledges the receipt of the command.

The Initiate Sequence instruction is only sent to the Adapter in response to a service request made by the Adapter through the Activity FIFO memory and the control buffers. The Adapter has asked the software for futher instructions to complete execution of a Channel command for a particular logical buffer address (LBA). The instructions are loaded into control buffer byte 3 and the Initiate Sequence EX COM1 is sent to notify the Adapter that the instructions are available in the control buffer of the particular LBA.

Bit 6 - Send Asynchronous Status - This COM1 instruction commands the Adapter to begin an asynchronous status transfer to the Channel, to the LBA set in the COM3 Register. The status to be sent to the Channel must have been previously loaded into byte 8 of the specified LBA's control buffer before the EX COM1 instruction is sent to the Adapter. Again, the LBA must be available in the COM3 Register before the instruction is sent. The Busy bit (bit 3) of the Adapter's status register will remain set until the Adapter's microprogram acknowledges receipt of the instruction.

The asynchronous status transfer is conditional, i.e., the status may or may not be sent, depending upon Channel activity with the specified LBA. If the LBA (device) was idle (no Channel command execution pending), the status will be sent and the software notified of the fact through the Status Transfer Complete mechanism. If the status could not be sent because of an incoming Channel command, the software will be notified though the use of the Activity FIFO memory and the control buffer.

NOTE: Asynchronous status should not be sent when software is working on completion of a Channel command. A command execution is not considered to have been completed until Device End status has been sent to and accepted by the Channel and indicated to the software through a Status Transfer Complete with the Activity FIFO memory.

3.2.4.4 EX COM2

Execution of an EX COM2 instruction to the

Adapter causes the next logical buffer address in the Activity FIFO memory to be available in the COM2 Register for reading by the software with a subsequent INPUT instruction. Execution of an EX COM2 instruction is under the control of status bit 2 (Address Available). If the FIFO memory has any logical buffer address stored, bit 2 of the status register will be set. Once the contents of the Activity FIFO memory are exhausted, the Address Available bit is reset.

Additional logical buffer addresses (if available as indicated by status bit 2) may be read from the Activity FIFO memory by issuing additional INPUT instructions to the Adapter.

The contents of the COM2 register are updated after each INPUT instruction. That is, each subsequent INPUT instruction will load the next Logical Buffer Address from the FIFO memory into the COM2 register.

Bit 2 of the status register and the Activity FIFO memory provide a means for the Adapter microprogram to signal the Datapoint processor driver software that activity has occurred with the Channel which requires its attention. (The Status bit indicates that the activity occurred, while the contents of the Activity FIFO memory indicate which logical buffer requires attention.)

The Logical Buffer Address has the following format:

3 2 1 0 ... specifies one of the 16 logical buffers within the Adapter
6 5 4 ..... reserved for buffer expansion
7 ..... used to indicate completion of a status transfer (when set to 1)

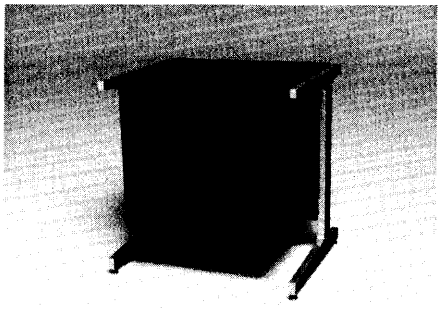
3.2.4.5 EX COM3

Execution of an EX COM3 instruction to the Adapter causes the information on the A-OUT bus to be loaded into the COM3 register. This has two purposes: to specify which logical buffer is to be used for buffer reads and writes, and which Logical Buffer Address an EX COM1 Initiate Sequence or Send Asynchronous Status command is directed to.

When used for buffer access, the content of the COM3 register has the following format:

3 2 1 0 ..... Logical Buffer Address
6 5 4 ..... Reserved for Address Expansion
7 ..... Which Buffer
0 = Data Buffer
1 = Control Buffer

When used in conjunction with an EX COM1, bit 7 is not significant.



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3.2.4.6 Auxiliary Logical Address Register

This eight-bit register stores Logical Buffer Addresses for access by the microprogam. It is loaded from the contents of the COM3 register upon execution of any EX COM1. Note that the contents of the Auxiliary Logical Address Register are used by the microprogram only if the EX COM1 instruction was an Initiate Sequence or a Send Asynchronous Status command. For all other EX COM1 instructions, the microprogram ignores the contents of this register.

3.2.4.7 EX COM4

The COM4 register stores the byte address, within a logical buffer, for use during buffer reads and writes. Execution of an EX COM4 instruction loads the COM4 register with the information on the A-OUT bus. If the Adapter is in Data mode (see 3.2.4.9), execution of an EX COM4 instruction also causes a buffer read; COM3 register contents specify which buffer is to be read.

The Adapter uses only the first four low-order bits of the COM4 register for control buffer access. (The control buffers are sixteen bytes deep.) It uses all eight bits of the register for addressing byte locations within a buffer. (The data buffers are 256 bytes deep.)

3.2.4.8 EX WRITE

If the Adapter is not in Data mode, an EX WRITE instruction causes the information on the A-OUT bus to be written into a buffer location (as specified by the contents of the COM3 and COM4 registers). An EX WRITE does not change the existing Status/Data mode of the Adapter. Data to be written into a buffer must be loaded into the A register (of the Datapoint processor) before execution of the EX WRITE.

3.2.4.9 EX DATA

An EX DATA instruction places the Adapter in its Data mode, in which execution of an EX COM4 instruction will cause a buffer read to occur (buffer and byte address specified by the contents of the COM3 and COM4 registers). Thus the "Data" mode allows the Datapoint processor driver software to read from one of the sixteen control buffers or one of the sixteen data buffers. Execution of an EX ADR, EX STATUS, or EX COM2 changes the Adapter's mode from Data to either the Status mode (EX ADR and EX STATUS) or the FIFO memory mode (EX COM2).

3.2.4.10 EX STATUS

An EX STATUS instruction places the Adapter in Status mode, as will execution of an EX ADR instruction with proper address and parity on the AOUT bus, making the contents of the status register available during subsequent execution of an INPUT instruction. Execution of an EX DATA or an EX COM2 will change the Adapter mode from Status to either Data mode or FIFO memory mode.

3.3 Control and Data Buffer Format

The Adapter has sixteen control buffers and sixteen data buffers. Each logical buffer address (LBA) has both a control and a data buffer associated with it. There are sixteen logical buffer addresses (000-017) corresponding to the sixteen control and sixteen data buffers. In addition, each LBA may be associated with a device address used by the IBM Channel.

The control buffers contain status and control information required for communication between the microprogram and the adapter-driver software. The data buffers are used to buffer data to or from the Channel.

Data stored in the data buffer may be in IBM EBCDIC code or be binary; data for transmission via the I/O interface is normally EBCDIC. The driver software must provide a translation process for converting EBCDIC coded data to ASCII coded data for use within the Datapoint system. Data to be transferred to the IBM System 360/370 must be translated by the driver software from ASCII code to IBM EBCDIC code.

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3.3.1 Control Buffer Format

3.3.1.1 Byte 0 - Channel Address

This byte contains the eight-bit IBM device address assigned to the logical buffer during system configuration. The Channel uses it to address one of the Adapter's logical buffers.

3.3.1.2 Byte 1 - Channel Command

This byte contains the command received from the Channel during an initial selection sequence. Bit 0 of byte 5 is set (Command Received), when a command is stored. All commands with valid parity are stored, except for the Test I/O and No-Operational Control commands. Command decoding is done by the adapter-driver software.

3.3.1.3 Byte 2 - Initial Selection Byte

This byte contains the eight-bit status that is returned to the Channel during an initial selection sequence. The status byte has the following format:

Bit 0 = Unit Exception
Bit 1 = Unit Check
Bit 2 = Device End
Bit 3 = Channel End
Bit 4 = Busy
Bit 5 = Control Unit End
Bit 6 = Status Modifier
Bit 7 = Attention

When a device goes from Ready to Not Ready state, the driver software sets the Unit Check bit (Bit 1) before ending status is sent. This is the only case in which the adapter-driver software will write to the initial selection status byte.

3.3.1.4 Byte 3 - Datapoint Control

This byte contains the Adapter control information by which adapter-driver software controls the Adapter. It has the following format:

Bit 0 = Reserved
Bit 1 = Execute Read Data Transfer
Bit 2 = Execute Write Data Transfer
Bit 3 = Excute Ending Procedure
Bit 4 = Selective Reset Acknowledged
Bit 5 = Reserved
Bit 6 -7 = Reserved

These control bits have the following effects on the Adapter when an Initiate Sequence COM1 instruction is issued to it:

Bit 1 - Execute Read Data Transfer - Causes the Adapter to initiate a read data transfer with the Channel, in response to either a sense or read command from the Channel during initial selection. Data from the data buffer is sent to the Channel until either the number of data bytes transferred to the Channel equals the count in byte 4 of the control buffer or the Channel halts data transfer by one of the following means: Stop data transfer, Halt I/O, Selective Reset, or a System Reset.

Bit 2 - Execute Write Data Transfer - Causes the Adapter to initiate a write data transfer with the Channel, in response to a write command from the Channel during an initial selection. Data from the Channel is written into the data buffer until either the number of data bytes transferred equals the count in byte 4 of the control buffer or the Channel stops data transfer by one of the following means: stop data transfer, Halt I/O, Selective Reset, or a System Reset.

Bit 3 - Execute Ending Procedure - Causes the Adapter to initiate an ending status transfer to the Channel, in response to one of the following conditions:

1 - Control Command Received from the Channel.

2 - Normal End on Read/Write.

3 - Halt I/O Received.

4 - Stop Received on Read/Write.

5 - Channel Parity Error/Command Received.

6 - Status Transfer Complete (Only if Device End status was not presented in the previous ending procedure.)

The Adapter uses the status byte from byte 8 of the control buffer. Before issuing an ending procedure command to the Adapter, the adapter-driver software must write the proper ending status into byte 8 of the control buffer. Upon successful transfer of the status byte, the Adapter will signal "Status Transfer Completed" by using the Activity FIFO memory. The logical address of the control buffer will be placed into the FIFO memory with the high order bit (bit 7) set.

Bit 4 - Selective Reset Acknowledged - Causes the Adapter to complete the selective reset procedure on a selected device. This command is used for interlocking purposes. It is issued to the Adapter in response to a selective reset indication.

Bit 5 - Reserved - This bit is reserved.

3.3.1.5 Byte 4 - Initial Byte Count

This byte of the control buffer contains the number of bytes (1-256, where 0 represents 256), to be transferred to or from the Channel in response to a read, sense, or write command. The byte count must be written into the control buffer by the driver software before an Initiate Sequence EX COM1, specifying a read or write data transfer (see Datapoint Control), is sent to the Channel Adapter.

3.3.1.6 Byte 5 - IBM Control

This byte contains control information for the driver software. It specifies the type of activity that has occurred with the logical buffer. Whenever information in the IBM Control byte changes (due to activity with the Channel), the adapter-driver software is flagged through the activity FIFO memory. (The address of the logical buffer is placed into the FIFO memory. This causes the Address Available status bit to be set.) The IBM Control Byte has the following format:

Bit 0 = Command Received
Bit 1 = Halt I/O Received
Bit 2 = Selective Reset
Bit 3 = Normal End on Read/Write
Bit 4 = Stop Received on Read/Write
Bit 5 = Reserved
Bit 6 = Reserved
Bit 7 = Channel Parity Error

Note that bit 7 may be set in combination with the bits 0 - 4. Bits 0 -- 4 will only have one bit set at a time.

The control bits have the following meaning:

Bit 0 - Command Received - This bit is set after the Adapter has received a command from the Channel other than a Test I/O or No-Operational Control command. The command that was sent during the initial selection is available in byte 6 of the control buffer.

Bit 1 - Halt I/O Received - This bit is set after the Adapter has received a Halt I/O (Interface Disconnect) indication from the Channel. If a data transfer was in progress at the time of the Halt I/O indication, the actual number of bytes transferred is contained in byte 6 of the control buffer.

Bit 2 - Selective Reset - This bit is set after the Adapter has received a Selective Reset indication from the Channel. The logical buffer will appear as a busy I/O device to the Channel until the adapter-driver software responds with a Selective Reset Acknowledged, Initiate Sequence EX COM1.

Bit 3 - Normal End on Read/Write - This bit is set when the Adapter is transferring data and the number of bytes transferred reaches the initial byte count (byte 4 of the control buffer).

The ending byte count in byte 6 is stored and is equal to the initial byte count in byte 4.

Bit 4 - Stop Received on Read/Write - This is set after the Adapter has received a stop indication from the Channel during a data transfer. The actual number of bytes transferred is stored in the ending byte count (Byte 6).

Bit 5 - This bit is reserved.

Bit 7 - Channel Parity Error - This bit is set whenever the Adapter has detected invalid parity on Bus Out. If the parity error was detected during a data transfer, the error will not be indicated until the transfer is terminated. Whenever the Channel Parity Error bit is set, the adapter-driver software should respond with a Unit Check status ending procedure.

3.3.1.7 Byte 6 - Ending Byte Count

This byte specifies the actual number of bytes (1 to 256), where 0 represents 256 bytes transferred during a data transfer. If the data transfer ends normally, the ending count will equal the initial byte count in byte 4. If a Stop or Halt I/O was received, the ending count will be less than the initial count.

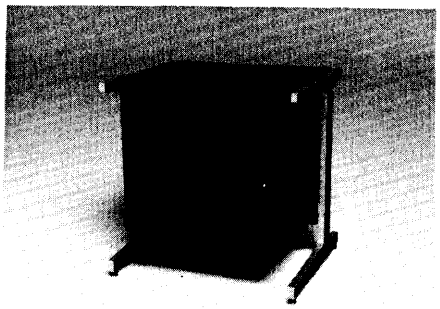
3.3.1.8 Byte 7 - Device Flag Word

This byte contains internal flags for the microprogram. Only bit 7 of the Device Flag is used for communication between the microprogram and the adapter-driver software. Bit 7 is set by the driver software, before system configuration, if the logical buffer is to be used. Once system configuration has been performed, the contents of the Device Flag Word should be ignored by the adapter-driver software.

3.3.1.9 Byte 8 - Ending and Asynchronous Status Byte

This byte contains the eight-bit status that is sent to the Channel during either an ending procedure, or during an asynchronous status transfer, as specified by an EX COM1 instruction and the contents of byte 3 of the control buffer. The status byte has the following format:

Bit 0 = Unit Exception
Bit 1 = Unit Check
Bit 2 = Device End
Bit 3 = Channel End
Bit 4 = Busy
Bit 5 = Control Unit End
Bit 6 = Status Modifier
Bit 7 = Attention



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3.3.1.10 Bytes 9 through 15

Bytes 9 through 15 of the control buffer are reserved for use by the microprogram.

3.3.2 Data Buffer Format

There are sixteen data buffers in the Channel Adapter. Each data buffer is associated with a control buffer that has the same logical buffer address. The data buffers are used to store data during read and write data transfers.

3.4 Off-line Procedures

Before the Channel Adapter can communicate with the IBM Byte Multiplexor Channel, it must be initialized and brought on line, a procedure in which both the driver software in the Datapoint processor and the microprogram in the Channel Adapter take part.

Initialization consists of clearing Adapter control buffers and then configuring them with the device addresses to be used by the Channel to identify these buffers.

3.4.1 Power-up Procedure

Turn on power to the Datapoint processor first, because even though the Channel Adapter has an independent On/Off switch, it does nothing unless I/O power from the Datapoint processor is present.

After the Datapoint processor is on, turn on the Main Power On/Off Switch located on the rear of the Channel Adapter. This switch should be left on unless the Adapter is being serviced.

Now, use the Controlled Power On/Off Switch on the Adapter's front panel to turn on its power; the Adapter will immediately execute an automatic power-on reset cycle during which all Adapter logic -- except for the control buffers, data buffers, and the active address RAM -- is brought to its initial state, and the Adapter status registers and activity FIFO buffer are cleared. Also, the IBM interface logic is switched from bypassing the Select Out signal to logically propagating it.

3.4.2 Power-down Procedure

Normally, use the Adapter Controlled Power On/Off Switch to power down, because this sequence, too, is under microprogram control which will not allow the Adapter to power down until it has been taken off-line to the IBM Channel by the driver software in the Datapoint processor.

Once the Adapter is off-line to the Channel, the power down sequence switches the IBM interface logic from propagating the Select Out signal to bypassing it; cuts off the output signals from the Adapter to both the Datapoint and IBM interfaces.

In an emergency, power down the Adapter by turning off the Main Power On/Off Switch on the rear panel, but understand that such an action ignores all control interlocks and will almost certainly cause unpredictable errors on the IBM Channel.

3.4.3 System configuration

Three system configuration tasks must be done to make the Adapter operational, in this sequence:

- Master Clear
- Configure System
- Go ON-LINE

3.4.3.1 Master Clear

Master Clear, initiated by the Datapoint processor driver software and performed by the Adapter microprogram, clears all sixteen control buffers in the Adapter. The driver software initiates Master Clear by addressing the Adapter and issuing a Master Clear EX COM1.

When this has been done, the busy bit of the Adapter's status byte will be set and remain set until the microprogram completes the Master Clear, at which time it will be reset.

Continued....

3.4.3.2 Configure System

Upon completion of the Master Clear, the Adapter microprogram resets its busy bit and the Datapoint processor adapter-driver software configures the Adapter control buffers for on line usage, by placing the address to be used by the IBM Byte Multiplexor Channel in byte 0 of each control buffer that is required to be active.

Each logical buffer corresponds to one IBM I/O device address, thus each address assigned to a control buffer must be uniquely different than all other addresses used by other control buffers and other control units on the Channel.

See IBM System 360 and System 370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information, GA22-6974-4, or Principles of Operation Manual for further addressing restrictions in relationship to the IBM System.

As each desired address is written into byte 0 of a control buffer, the Datapoint processor driver software must set the high-order bit (bit 7) of the control buffer byte 7 (Device Flag Word).

This bit serves as a flag to the Adapter microprogram; when set (to a logical 1), the control buffer is considered to be an active buffer. The bit is set by writing an octal 0200 to byte 7 of the desired control buffer.

Special Note: All models of the IBM System 360/370 carry I/O device addressing restrictions. To avoid possible Channel errors, users should consult the IBM Functional Characteristics manual for the particular model number of System 360/370 and the Principles of Operation manual in use before assigning device addresses to Adapter logical buffers.

After it has configured the Adapter control buffers, the Datapoint processor driver software issues a Configure System EX COM1 to the Adapter, causing the Adapter microprogram to branch to a configuration routine in which it scans all the control buffers, checking each control buffer's Device Flag Word (byte 7) for the status of its high-order bit.

If the high-order bit is not set, the microprogram moves on to scan the next buffer; if the bit is set, it reads the device address from buffer byte 0, and uses it to access the active address RAM on the sequencer logic card. At that address location in the RAM the microprogram writes the logical address of the control buffer together with an active indication bit.

(Recall that active address RAM locations were cleared to all zero values during Master Clear execution.)

After placing the logical buffer address into the RAM location specified by the device address, the Adapter microprogram continues to scan any remaining control buffers. The Adapter microprogram follows acknowledgement of receipt of the Configure System EX COM1 by resetting the busy bit in its status register.

3.4.4 Going ON-LINE

At completion of Configure System execution, the Adapter is ready to go ON-LINE. Its microprogram will try to place the Adapter on-line when it receives an ON-LINE EX COM1 from the Datapoint processor driver software.

Before the Adapter can go ON-LINE, however, proper conditions must exist, either on the IBM Channel interface -- if the Adapter is in OPERATE mode -- or on the Adapter's Simulator -- if the Adapter is in TEST mode.

The proper condition on the IBM Channel interface is that the IBM CPU is in the stop or wait state. Refer to the Simulator operation, Section 3.6.10, for comparable conditions in TEST mode.

When the Adapter goes ON-LINE, the ON-LINE and Configured bit (bit 1) of its status byte is set. When the microprogram acknowledges receipt of the ON-LINE EX COM1 instruction, it resets its busy bit. Once ON-LINE, the Adapter is ready to communicate with the IBM Channel; it signals this condition by lighting the ON-LINE indicator.

3.4.5 Going OFF-LINE

The Datapoint processor adapter-driver software should issue an OFF-LINE EX COM1 instruction only when the Adapter is ON-LINE, and in an idle state, i.e., no current Channel operations in progress. An interlock in the microprogram manages the asynchronous conditions that exist between the Channel, the Adapter, and the driver software; it prevents the Adapter from going OFF-LINE until all its logical buffers are idle. It is possible, therefore, that the Adapter may not go OFF-LINE immediately after the execution of an OFF-LINE EX COM1, and the driver software must take this possibility into account. The Adapter's microprogram stores the fact that an OFF-LINE command was received, and allows the Adapter to comply with that command as soon as conditions permit.

3.5 ON-LINE Operation

Once the Adapter has been configured and brought ON-LINE, various interface sequences take place, in response to requests initiated by either the Datapoint processor or the IBM System 360/370.

3.5.1 Channel Sequence Definition

On the IBM Byte Multiplexor Channel data transfer proceeds through three phases: Initial Selection, Data Transfers, and Ending Sequence.

For a more detailed discussion of this operation, refer to IBM System 360 Principles of Operation, G22-6281, IBM System Principles of Operation GA22-7000, IBM System 360 and System 370 Interface Channel to Control Original Equipment Manufacturer Information, GA22-6974-4.

Initial Selection- During Initial Selection the IBM System 360/370 Channel addresses the Adapter and issues a command. A Selective Reset or Halt I/O can also be issued in this way.

Data Transfer- The Adapter requests service from the Channel and after being selected, effects the transfer of data to or from the Channel.

Ending Sequence- After the entire data block has been transferred, the Adapter requests service from the Channel and, after being addressed, transfers the status byte to the Channel.

3.5.2 Microprogram Polling Scheme

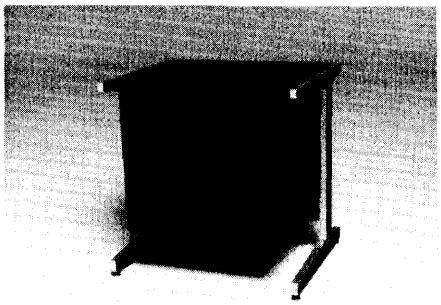
A polling routine in the Adapter microprogram controls all activity between the logical buffers and the Channel, with a view to preventing any one logical buffer from monopolizing the resources of the Adapter, and making all active logical buffers work multiplex fashion.

On a Byte Multiplexor Channel, multiplexing between logical buffers requiring service occurs once for every four data bytes transferred. Multiplexing on this kind of Channel also occurs between initial selection sequences and between ending (status transfer) sequences.

(Note that the hardware may be strapped for either one-byte or four-byte mode of operation.)

When a command is received from the Channel during an initial selection sequence, a logical buffer is placed in a queue. It remains in the queue until either a System Reset occurs or the Adapter presents Device End status to the Channel and the Channel accepts it.

Continued...



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A logical buffer may exist in four states:

- NOT ACTIVE -- not configured during Adapter configuration
- ACTIVE-- configured, but in an idle state
- ACTIVE, SERVICE REQUIRED -- waiting instructions from Adapter driver software
- ACTIVITY OCCURRING -- executing an instruction received from adapter-driver software

When a logical buffer changes from the ACTIVE state to the ACTIVE, SERVICE REQUIRED state the Datapoint processor driver software is informed of the change by use of the Activity FIFO. Bit 2 of the Adapter's status byte is set and the logical buffer's address is placed in the FIFO. Bit 0 of byte 5 of the control buffer is also set. This transition occurs when a new command is received from the Channel.

Transition from the ACTIVE, SERVICE REQUIRED state to the ACTIVITY OCCURRING state takes place when the Datapoint software control program responds to the service requirements made by the Adapter activity FIFO and control buffer. Response from the software may vary, depending on what the command from the Channel requires of it and the Adapter. In all cases, however, the driver software issues an Initiate Sequence EX COM1 to the Adapter. Additional information required by the Adapter microprogram for execution of the sequence is contained in byte 3 of the control buffer.

Upon completion of the sequence, the Adapter logical buffer may return either to the ACTIVE, SERVICE REQUIRED state or to the ACTIVE state. Transition is to the ACTIVE state only if the last sequence executed was an Ending Procedure and the Ending Status contained Device End status, or if a System Reset occurred.

3.5.3 Initial Selection Sequence

The IBM System 360/370 initiates I/O operations by the START I/O (SIO) instruction. The operand of the SIO instruction specifies both the Channel and the I/O device for which I/O is required. The Channel specified by the operand fetches the first Channel Command Word (CCW) from main storage using the address stored in the Channel Address Word (CAW), which is always stored in location 72 of the main storage.

The CCW specifies the command to be given to the I/O device, data address, and the number of data bytes to be transferred. It also uses a number of flag bits to modify the I/O operation.

To initiate an I/O operation, the Channel places the address from the SIO operand of the desired I/O device on BUS OUT and raises ADDRESS OUT. Each control unit connected to the Channel attempts to decode the address on the bus, but I/O addresses are uniquely assigned, so only one finds itself addressed. To be acceptable, the address must exhibit correct parity.

The Channel Adapter uses the Active Address RAM on the sequencer logic card for address decoding. The logical buffer addresses for all active device addresses, up to the maximum of sixteen possible, are contained in this RAM.

The Adapter uses the address from the IBM BUS OUT to address the RAM. If the address on BUS OUT matches one of the active addresses assigned to the Adapter -- established during System Configuration while OFF-LINE -- the logical buffer address (LBA) assigned to the address will appear on the output of the RAM, and the high-order bit (bit 7) of the LBA will be set, indicating that a match has been made.

The next action of the Channel is to issue a SELECT OUT (along with HOLD OUT). When the incoming SELECT OUT -- or SELECT IN, depending on control unit priority strapping -- appears, the Adapter does not allow it to propagate, and the Adapter microprogram raises the OPERATIONAL IN line.

If the address on BUS OUT did not match an address assigned to the Adapter, the sequencer propagates SELECT OUT (or SELECT IN, as noted above) and the microprogram is not disturbed.

When the IBM Channel senses the rise of OPERATIONAL IN, it responds by dropping ADDRESS OUT. If none of the control units attached to the Channel recognize the address, the Channel will receive the SELECT IN signal and an error will be flagged.

After the Channel drops ADDRESS OUT, the Adapter responds by placing the device address -- taken from control buffer byte zero, using the LBA from the active address RAM -- on BUS IN, and then raises the ADDRESS IN tag line.

For a Byte Multiplex operation the Channel drops HOLD OUT and SELECT OUT at this time. The Channel then compares the address on BUS IN with the address from the SIO operand; if they match, the Channel places the command byte (from the CCW) on BUS OUT and raises the COMMAND OUT tag line.

If the address on BUS IN does not match the one from the SIO operand an error is flagged and the control unit may be released by placing a TEST I/O command on BUS OUT and signalling COMMAND OUT.

When the Channel raises COMMAND OUT, the Adapter takes the command from BUS OUT. Neither a TEST I/O nor a NO-OPERATION control command will be placed in the Adapter control buffer. All other commands are stored in the control buffer (byte one), after which the Adapter signals the Channel by dropping ADDRESS IN, and the Channel responds by allowing COMMAND OUT to fall. When COMMAND OUT falls, the Adapter places status -- obtained from the Initial Status Byte of the control buffer -- on BUS IN.

If the command was a NO-OPERATION control command, the Adapter generates CHANNEL END, DEVICE END status and places it on BUS IN, then raises the STATUS IN tag line.

If the Channel accepts this status condition, it responds with the SERVICE OUT line, which allows STATUS IN to fall, thus completing the initial selection sequence. If SELECT OUT is down at this time, the Adapter drops STATUS IN and then OPERATIONAL IN. Bit one of byte 5 (Command Received bit of the IBM control word) is set and the Datapoint processor adapter-driver software is notified by the placing of the LBA into the activity FIFO, which results in the setting of the ADDRESS AVAILABLE status bit.

If the Adapter raises STATUS IN, a COMMAND OUT response from the Channel in-

Continued....

dicates that it cannot currently accept the initial status and the status is stacked, whereupon the Adapter drops STATUS IN and then OPERATIONAL IN (if SELECT OUT is down at this time). The Adapter does not notify the driver software until the initial status byte is accepted by the Channel, either through a reselection or through the use of a TEST I/O command during a Channel-initiated initial selection sequence.

If SELECT OUT is active at the time STATUS IN falls, the driver software is notified by the setting of the SELECT OUT bit along with the COMMAND received bit in the IBM CONTROL WORD of the selected control buffer. This indicates that the Byte Multiplexor Channel is forcing burst mode.

Note that the Channel will not stack an initial status byte of zero, unless the command presented to the Adapter was a TEST I/O.

3.5.4 Control Unit Busy Sequence

If the microprogram cannot currently execute an initial selection sequence because of outstanding housekeeping requirements, the sequencer will execute a short Control Unit Busy Sequence to the Channel. This short sequence is handled entirely by the sequencer hardware, allowing the microprogram to continue its housekeeping uninterrupted.

The control-unit-busy sequence begins when the Channel places the I/O device address on BUS OUT and raises ADDRESS OUT, followed by SELECT OUT. Each control unit attached to the Channel's interface attempts to decode the address on BUS OUT.

When the Channel Adapter detects SELECT OUT -- and only if the address on BUS OUT matches one of the addresses assigned to one of its logical buffers -- the sequencer will not allow propagation of the signal. Instead, it places control unit busy status -- BUSY, STATUS MODIFIER, and CONTROL UNIT END bits set -- on BUS IN, then raises STATUS IN, but does not raise OPERATIONAL IN.

After accepting the status byte, the Channel drops SELECT OUT, to which the Adapter responds by dropping STATUS IN and logically disconnecting from the interface. The Channel keeps ADDRESS OUT up until STATUS IN drops, thus completing the control-unit-busy-sequence.

NOTE: The short control-unit-busy sequence implies that the Adapter is only temporarily busy. A busy condition may be considered temporary if it lasts less than approximately 2 milliseconds.

3.5.5. Address Available Responses

When the Datapoint processor software recognizes the Address Available status from the Adapter, it reads the logical buffer address (LBA) from the Activity FIFO and uses that to point to the control buffer requiring its attention. Control information is contained in byte 5 of the buffer; its source is the IBM Control Word.

If the Channel just performed an Initial Selection Sequence and the command sent to the Adapter was neither a TEST I/O or a NO-OP, the COMMAND RECEIVED bit (bit 0) will be set in the control word. Two other bits may be set along with the COMMAND RECEIVED bit: SELECT OUT (bit 5) or CHANNEL PARITY ERROR (bit 7) or both.

The SELECT OUT bit indicates that the Datapoint processor software should immediately respond to the service request from the LBA, suspending multiplexing on other LBAs currently active. It means that the Byte Multiplexor Channel is forcing burst mode.

If the Multiplexor Channel is forcing burst mode, the Datapoint processor software must respond in less than 500 milliseconds to avoid possible error conditions. The Channel should not indicate a malfunction unless a delay of interface activity exceeds approximately 30 seconds; however, possible data overrun conditions can come to exist on non-buffered I/O devices if the delay is excessive.

Four other bits in the IBM Control Word may be set when an Address Available status indication is given to the driver software:

3.5.5.1 HALT I/O RECEIVED (Bit 1)

When the Channel issues a Halt I/O sequence to the Logical Buffer Address this bit is set. In response to it, the Datapoint processor software normally generates an ending status, provided that the LBA was executing a Channel command, i.e., was not in the ACTIVE ONLY state.

3.5.5.2 Selective Reset (Bit 2)

This bit is set when the Channel issues a Selective Reset to the LBA. The driver software should respond to it by setting the SELECTIVE RESET ACKNOWLEDGED bit (bit 4) in the Datapoint Control Word (DPCW, byte 3) of the control buffer, then issuing an Initiate Sequence EX COM1 to the Adapter.

A Selective Reset cancels all previous activity required by the LBA. The LBA goes to the ACTIVE ONLY state and all incomplete Channel sequences are halted. A response of INITIATE SEQUENCE causes the Adapter microprogram to clear the control buffer except for the Channel address byte (byte 0) and the Active bit in byte 7.

Because of the asynchronous nature of the Selective Reset, an interlock in the Adapter microprogram prevents any other activity from taking place with a Logical Buffer Address until the Datapoint driver software returns a SELECTIVE RESET ACKNOWLEDGE to the Adapter.

3.5.5.3 Normal End on READ/WRITE (Bit 3)

After the Datapoint processor software has instructed the Adapter to execute a READ or WRITE data transfer with the Logical Buffer Address, the setting of this bit indicates that the data transfer has equalled the specified number of bytes to be transferred, i.e., the Ending Byte Count -- Byte 6 of the control buffer -- is equal to the Initial Byte Count in Byte 4.

If the LBA in use is emulating a unit record I/O device such as a card reader or line printer the Initial Byte Count will contain the UNIT RECORD LENGTH -- for example, 80 bytes for a card reader; when NORMAL END occurs the driver software should respond by executing an ending procedure set up. However, if the LBA is emulating a tape control unit, additional data transfers may be necessary, and a data transfer set up should be executed by the driver software.

3.5.5.4 Stop Received on READ/WRITE (Bit 4)

If set, this bit indicates the Channel has stopped a data transfer in progress on the LBA by issuing a COMMAND OUT response to the SERVICE IN tag. The Ending Byte Count (Byte 6 of the control buffer) contains the actual number of bytes that were transferred. The driver software should respond with an ending procedure set up.

3.5.6 Command Decoding

Following a Channel initiated Initial Selection Sequence, the Adapter notifies the Datapoint processor software control program that a command has been received from the Channel. If there has been no parity error, the driver software must decode this command and take action on it. The Channel command is stored in byte 1 of the control buffer following the initial selection sequence. It will have one of the following formats.

Continued...

Command Type:	*Bit Position (Datapoint Convention)*							
	7	6	5	4	3	2	1	0
Test I/O*	0	0	0	0	0	0	0	0
Sense	M	M	M	M	M	1	0	0
Read Background	M	M	M	M	1	1	0	0
Write	M	M	M	M	M	M	0	1
Read	M	M	M	M	M	M	1	0
Control	M	M	M	M	M	M	1	1
Basic Sense	0	0	0	0	0	1	0	0
No-Operation Control*	0	0	0	0	0	0	1	1

M = Modifier Bit

* The Test I/O and No-Operation Control commands are handled by the microprogram and do not require any action from the software control program.

The modifier bits (symbolized by M) are used to modify the basic command codes and make them dependent upon the I/O device type. More information about this feature is available in the IBM System Reference Library publications for specific I/O devices. For command information on the following IBM unit record equipment consult Section 6.0:

IBM 2501 CARD READER
IBM 1403 LINE PRINTER
IBM 1052 KEYBOARD - PRINTER
IBM 2540 CARD - READER PUNCH
IBM 1443 LINE PRINTER

3.5.6.1 Command Reject

If the command byte does not match the list of valid commands for the I/O device being emulated, the Datapoint processor software program must reject it.

The Adapter indicates command rejection to the Channel by use of an ending procedure. Unit Check status is placed into the Ending/Asynchronous status byte of the LBA's buffer (byte 8), and an Execute Ending Procedure Datapoint Control Word is then written into byte 3 of the control buffer. Then an Initiate Sequence EX COM 1 is issued to the Adapter.

Note that before the EX COM1 instruction is attempted, the software program must ensure that the proper LBA has been loaded into the Auxiliary Register.

After this, the Adapter will attempt to present the Unit Check status to the Channel by initiating a Control Unit Initial Selection Sequence. The Adapter raises the REQUEST IN tag to the Channel, a signal which will force the Channel to conduct a polling sequence as soon as it is free to do so. The next time SELECT OUT rises at the Adapter and no I/O selection is being attempted by the Channel (ADDRESS OUT is down), the Adapter will not propagate the SELECT OUT signal but will capture the interface by raising the OPERATIONAL IN tag.

At that, the Adapter places the device address corresponding to the LBA rejecting the command on BUS IN; when the Channel recognizes the address, it sends COMMAND OUT to the Adapter as a signal to proceed. When it sees COMMAND OUT, the Adapter drops ADDRESS IN; the Channel responds by dropping COMMAND OUT. The Adapter then places the status from byte 8 of the control buffer on BUS IN and raises the STATUS IN tag.

The Channel may accept or reject status. If it accepts the STATUS, the Channel raises SERVICE OUT, which allows the Adapter to drop STATUS IN and OPERATIONAL IN.

After dropping these tags and clearing the interface the Adapter microprogram informs the Datapoint processor driver software that status has been sent to and acknowledged by the Channel during another Control Unit-initiated Initial Selection Sequence, or during a Channel-initated Initial Selecton Sequence with a Test I/O command.

Once the stacked status has been accepted by the Channel, the Adapter informs the driver software through use of the Activity FIFO and the Ending Procedure Complete bit.

When the Channel receives Unit Check status it will normally respond by issuing a SENSE command to the I/O device that sent Unit Check. The software driver must have SENSE data available for the Channel once a command is rejected. The first six bits of the first sense data byte -- sense byte 0 -- are common to all I/O devices having this type of information; these bits are:

IBM Bit

7.....Command Reject
6.....Intervention Required
5.....Bus-Out Check
4.....Equipment Check
3.....Data Check
2 1 0.....Overrun

Datapoint Bit

0.....Command Reject
1.....Intervention Required
2.....But-Out Check
3.....Equipment Check
4.....Data Check
5 6 7.....Overrun

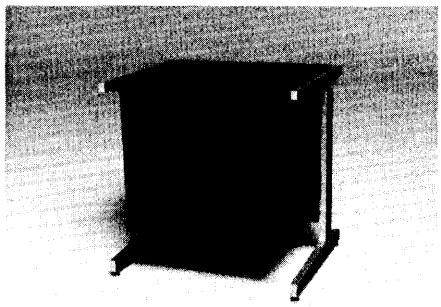
The SENSE command begins like all other Channel-initiated initial selection sequences. At the end of it the COMMAND RECEIVED bit is set and the LBA is placed into the Activity FIFO memory. The software program must then supply the proper sense data (Command Reject Bit set) to the LBA's data buffer. Next, the initial byte count (byte 4) of the control buffer is set to the number of sense bytes that are to be transferred to the Channel. Finally, the Execute Read Data Transfer bit is set in byte 3 (DPCW) of the Control buffer, and an Initiate Sequence EX COM1 is sent to the Adapter.

The software program must always ensure that the proper LBA is loaded into the COM3 register before issuing an Initiate Sequence EX COM1.

The rest of the sense operation resembles a Read Data transfer. Once the sense data has been sent to the Channel the driver software should reset its sense byte to ensure that the same information is not retransmitted at the next sense inquiry.

3.5.6.2 Normal Command Procedures

The Channel issues three kinds of "normal" commands to the Adapter: Read, Write, and Control.



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Unless an error has been detected -- such as Command Reject -- Read and Write commands always result in a Data Transfer sequence. The Sense command is essentially a Read command except that it has a different data source. Control Commands are immediate-type commands, i.e., ending status is immediately presented to the Channel following the initial selection sequence.

The Datapoint software driver responds to both Read and Write commands in similar fashion. It decodes the command and checks for validity. If a Read, data is loaded into the data buffer. Note that the data must first be translated from ASCII to EBCDIC.

For both Read and Write commands, the Initial Byte Count (control buffer byte 4) is set to the desired record length. (An Initial Byte Count of zero is assumed to mean a 256 byte data transfer.)

Next, the correct Datapoint Control Word (DPCW) must be written into control buffer byte 3. If a Read, the Execute Read Data Transfer bit (bit 1) of the DPCW is set; if a Write, the Execute Write Data Transfer bit.

Finally, an Initiate Sequence EX COM1 instruction is sent to the Adapter ending the software response sequence. These activities will cause the Adapter to begin a Control Unit Initiated Sequence.

Note that Read and Write commands may contain control information such as stacker select information for a card reader. This control information may be ignored if the emulated I/O device is not a physical device, i.e., if it is a disk file. Such information usually does not effect the data transfer unless the device is in a state that inhibits total execution of a command.

Control commands require an Ending Procedure response by the software. Ending status -- usually CHANNEL END, DEVICE END -- is written into byte 8 (ENDING/ ASYNCHRONOUS STATUS BYTE) of the control buffer. The Execute Ending Procedure bit is set in the DPCW (byte 3) of the control buffer, and an Initiate Sequence EX COM1 is issued to the Adapter, which in turn begins a Control Unit Initiated Sequence to present the status to the Channel.

3.5.6.3 Parity Error on Command Received

If the CHANNEL PARITY ERROR bit in the IBM CONTROL WORD is set with the COMMAND RECEIVED bit, a parity error has occurred during the initial selection sequence. The validity of the command byte in the control buffer is questionable, therefore the Datapoint processor driver software should not attempt to decode it. The error condition must be signalled to the Channel in the same manner as a Command Reject condition.

The software program instructs the Adapter to send a Unit Check status byte to the Channel, using the Ending Procedure sequence. However, the sense data to be retained by the software should reflect the parity error condition by the setting of the BUS OUT check bit. The rest of this procedure is identical to that of the Command Reject procedure.

3.5.7 Control-Unit-Initiated Sequence

When the Adapter requires service from the Channel, it raises REQUEST IN to the Channel. Thereafter, the next time SELECT IN rises at the Adapter and no I/O selection is being attempted by the Channel (ADDRESS OUT is down) the Adapter raises OPERATIONAL IN and places the address of the I/O device -- Channel address associated with the LBA requiring service -- on BUS IN.

The Adapter signals ADDRESS IN to inform the Channel that the information on BUS IN is the address; the Channel sends COMMAND OUT to the Adapter to indicate that it should proceed. The Adapter thereupon drops ADDRESS IN, to which the Channel in turn responds by dropping COMMAND OUT.

If the service request is for data, the sequence then proceeds as in DATA TRANSFER. The control-unit-initiated selection for data transfer occurs in Byte Multiplex mode.

If the service request is for status information the sequence proceeds as defined for the status cycle in the ending procedure.

3.5.7.1 Data Transfers

To transmit data to the Channel (Read Data Transfer), the Adapter places a data byte on BUS IN and raises SERVICE IN. It maintains the validity of BUS IN until an OUT TAG (see 3.6.6) from the Channel is raised in response.

To request data from the Channel (Write Data Transfer), the Adapter raises SERVICE IN and the Channel places the data byte on BUS OUT and signals by raising SERVICE OUT. The Channel maintains the validity of BUS OUT until the Adapter drops SERVICE IN, after which the Channel responds by dropping SERVICE OUT.

Duration of data transfer is controlled by both the Channel and the Adapter. To give the Channel a method of controlling connection duration, a control unit cannot disconnect from the interface before SELECT OUT (or HOLD OUT) falls. However, the Adapter, by holding up OPERATIONAL IN, may preserve its logical connection after the Channel, with SELECT OUT (or HOLD OUT), has permitted it to disconnect. The Adapter may in this way force burst mode.

Either Byte Multiplexor or Burst mode is established by the duration of the connection. These modes are established so the program can schedule concurrent execution of multiple I/O operations.

If OPERATIONAL IN remains up for longer than the byte multiplexing time-out limit of 32 microseconds, selection is in burst mode; selection times less than this limit are in byte multiplex mode.

The Adapter normally transfers data in byte multiplex mode; up to four data bytes during a Data Transfer sequence. It will keep requesting service from the Channel until either the Channel stops the transfer or until the ending byte count -- in byte 6 of the control buffer -- equals the initial byte count in byte 4, transferring four data bytes at a time until the residue count is less than four bytes.

If more than one Logical Buffer Address (I/O device) has data transfer service requirements, the Adapter interleaves data transfer requests, multiplex fashion. Each data transfer sequence begins with a control-unit-initiated sequence and the address of the I/O device is always given to the Channel.

3.5.7.2 Burst Mode

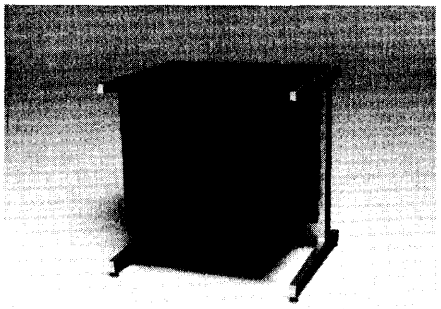
The Adapter will force burst mode on the Channel if the FORCE BURST MODE bit in the Datapoint Control Word (DPCW -- control buffer-byte 3) was set when the software driver program issued an Initiate Sequence EX COM1. The Adapter will request service from the Channel with the normal control-unit-initiated sequence, then, once it gains connection to the interface, will keep the OPERATIONAL IN tag up until either the data byte count is exhausted or the Channel stops the transfer.

NOTE: This method of data transfer is not recommended, since overrun conditions may occur.

3.5.7.3 Ending Data Transfer

One of three situations may exist at the termination of Data Transfer.

1. The Channel recognizes the end of the operation before the Adapter reaches the initial byte count number of data bytes to be



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transferred. When the Adapter requires service again, it raises the SERVICE IN line, to which the Channel responds with COMMAND OUT, indicating STOP. The Adapter thereupon drops SERVICE IN and OPERATIONAL IN (if SELECT OUT is down) and informs the software program of the situation.

2. The Channel and the Adapter recognize the end of an operation at the same time. The number of bytes specified by the Initial Byte Count in the control buffer has been transferred.

3. The Adapter recognizes the end of the operation before the Channel reaches the end of the operation. Again, the specified number of bytes to be transferred has in fact been transferred.

In situations 2 and 3, the Normal End On Read/Write bit is set in the IBM Control Word (Control buffer - byte 5). The Ending Byte Count is equal to the Initial Byte Count and both are available in the control buffer. The Logical Buffer Address of the I/O device is placed into the Activity FIFO and the Address Available status bit is set on the Interface I logic card.

In situation 1, the Stop Received On READ/WRITE bit is set in the IBM Control Word. The Ending Byte count will be less than the Initial Byte Count. The LBA of the I/O device is placed into the Activity FIFO, setting the Address Available status bit.

3.5.7.4 Parity Errors During Data Transfers

If a parity error occurs on BUS OUT during a Write Data Transfer the CHANNEL PARITY ERROR bit will be set in the IBM Control Word when data transfer ends. Note that this bit may be on with either the Normal End or Stop Received bits. The Datapoint processor software program should respond with a Unit Check status Ending Procedure and make ready BUS OUT CHECK sense data.

3.5.8 Ending Procedure and Asynchronous Status

The Ending Procedure transfers ending status conditions to the Channel at the end of an I/O operation. Ending Procedures may be single or multiple. Note that the Ending Procedure may be used to transfer status to the Channel until Device End status is transferred; after Device End has been sent and accepted any additional status transfers must be made using the Asynchronous status transfer procedure.

Asynchronous status conditions are not related to any commands previously initiated by System 360/370 programs. One of these conditions is ATTENTION, which is generated by the IBM 1052 console. Another is DEVICE END, generated when the corresponding I/O device goes from a not-ready to a ready state.

3.5.8.1 Normal Ending Procedure

An Ending Procedure must be initiated by the software program after one of the following events occurs:

1. Normal End On Read/Write
2. Stop Received on Read/Write
3. Command Received (Control Command)
4. Command Received (Channel Parity Error)*
5. Command Received (Command Reject)*
6. Channel Parity Error at Normal End/Stop Received
7. Status Transfer Completion (Other than DEVICE END)

* *NOTE:* Channel End, Device End Status must be sent along with the Unit Check indication.

To initiate an Ending Procedure, the software program places the ending status byte into byte 8 (Ending/Asynchronous Status Byte) of the desired control buffer. Next the Execute Ending Procedure bit is set in the Datapoint Control Word (control buffer byte 3) and an Initiate Sequence EX COM1 instruction is issued to the Adapter.

When the turn of that Logical Buffer Address comes up in the queue, the Adapter will attempt a Control-Unit-Initiated sequence. Once the Adapter has been selected by the Channel it will present the ending status byte by placing it on BUS IN and raising STATUS IN. If the Channel accepts this status byte it will respond by raising SERVICE OUT, which allows the Adapter to let STATUS IN and OPERATIONAL IN fall, completing the Ending Procedure sequence.

The Channel may also stack the ending status by responding with COMMAND OUT, which also allows STATUS IN and OPERATIONAL IN to fall; in this case the Adapter will hold the stacked status until another opportunity arises to present it.

Once the status has been accepted by the Channel, the Adapter signals status transfer completion to the software driver program by placing the Logical Buffer Address into the Activity FIFO with the high-order (bit 7) bit set. The status completion indication allows for Multiple Ending Procedures. The Datapoint processor software should not initiate a second Ending Procedure until the first has completed.

3.5.8.2 Asynchronous Status Presentation

The Asynchronous Status Procedure is used to present to the Channel status not associated with any previous command, i.e., the LBA is in the ACTIVE ONLY state. To accomplish this, the software program places the status into byte 8 of the control buffer, then issues an Asynchronous Status EX COM1 instruction. The Adapter will attempt to present this status to the Channel using the Control-Unit-Initiated sequence.

The asynchronous status presentation will be aborted if it is interrupted by a Channel-initiated selection sequence directed to the LBA that is attempting the status transfer. If this happens, the Adapter will accept the command, place it in byte 1 of the control buffer, set the COMMAND RECEIVED bit in the IBM Control Word, and then place the LBA in the Activity FIFO to notify the software program that its status transfer was preempted.

If the asynchronous status is accepted by the Channel, the Adapter will signal status transfer completion to the driver software. If the Channel stacks the status, the Adapter will retry presentation at the first opportunity. Note that once the status has been stacked, any commands from the Channel for the LBA holding status will be rejected by a DEVICE BUSY initial status byte.

Continued....

3.5.9 Device Busy Status

Whenever an I/O device -- identified with a Logical Buffer Address -- cannot accept a command during an Initial Selection sequence the command is rejected by presentation of a BUSY initial status byte. Busy is indicated whenever one of the following conditions exist:

1. A previous command is being executed by the LBA (DEVICE END status has not yet been presented to the Channel).

2. Stacked status is being held by the LBA -- except that if the command is a TEST I/O the stacked status will be presented after all.

3. The LBA is waiting on a Selective Reset Acknowledgement from the driver software program.

3.5.10 Attention Status

ATTENTION is generated when some asynchronous condition occurs in the I/O device identified with a Logical Buffer Address which is not associated with the initiation, execution, or termination of any I/O operation. ATTENTION should only be presented to the Channel through the use of an Asynchronous Status Transfer Sequence.

ATTENTION is used when a Logical Buffer Address is to be identified with, and emulate, an IBM 1052 Printer-Keyboard.

3.5.11 Device End Status

Device End Status occurs for either of two reasons:

1. The completion of an I/O operation at the I/O device identified with an LBA.

Device End Status is presented with the use of an Ending Procedure Sequence, which signals to the Channel that the I/O device (LBA) has completed execution of the command previously issued by it. Each I/O operation causes only one Device End condition; it is generated either simultaneously with the Channel-End condition or later -- in which case Multiple Ending Procedures are required. Once Device End has been accepted by the Channel, the Adapter's microprogram clears bytes 1, 3, and 5 of the control buffer, and resets all bits of byte 7 except for the Active bit (bit 7).

2. The transition of an I/O device (LBA) from not-ready to ready status.
Device End Status is signalled to the Channel during an Asynchronous Status transfer, indicating that an I/O device identified with an LBA has gone from a not-ready to a ready state. Acceptance of the Asynchronous Device End Status clears any Unit Check status that previously existed in the initial status byte. Transition in the opposite direction, from ready to not-ready, is done by the software program's setting the initial status byte of the control buffer to Unit Check; this must be done before Device End status is presented to the Channel during an Ending Procedure following an I/O operation. The asynchronous Device End presentation resets the Unit Check initial status.

3.5.12 Command Chaining

Command chaining means that another command for the I/O device in operation will immediately follow the presentation of Device End status -- provided that no unusual conditions were encountered during execution of the current operation.

If SUPPRESS OUT is active when SERVICE OUT is raised in response to STATUS IN during an Ending Procedure status presentation, it means command chaining follows. The Adapter microprogram responds by making the Adapter wait on the Channel to either start the next I/O operation or drop the command chaining indication by taking down SUPPRESS OUT before an Initial Selection Sequence begins.

3.5.13 Data Suppression

Operations whose rate of data transfer can be adjusted without overrunning are subject to suppression of data by SUPPRESS OUT. Completely buffered I/O devices, start-stop devices, and operations that transfer data for the basic sense command may fall into this category, and be treated as follows:

1. SUPPRESS OUT is ignored for the first data byte following any selection sequence unless the data transfer immediately follows the initial selection, with no deselection-reselection in between.

2. When SUPPRESS OUT is raised at the control unit and the operation is in burst mode -- whether because SELECT OUT is up or because the control unit is forcing burst mode -- the control unit must not raise SERVICE IN for subsequent suppressible data.

3.5.14 Channel End

The completion of a portion of an I/O operation involving transfer of data or control information between an I/O device and the Channel causes Channel End; each I/O operation causes the Channel End condition for an operation.

Channel End is not generated when programming errors or equipment malfunctions are detected during initiation of an operation, but operations that do not cause any data to be transferred can provide the Channel End condition during initial selection. A Channel End condition pending in a control unit causes that unit to appear busy for initiation of new operations.

3.5.15 Unit Check

Unit Check indicates that the I/O device or control unit has detected an unusual condition -- perhaps a programming error or an equipment malfunction -- and details are available on receipt of a sense command.

An error condition causes the Unit Check indication only when it happens during execution of a command or Test I/O, or during some activity associated with an I/O operation. If during the initial selection sequence an I/O device detects that its command cannot be executed, Unit Check is presented to the Channel without Channel End, Unit End, or Device End; it means that no action has been taken at the device in response to the command. Any errors associated with an operation which are detected after Device End has been cleared are indicated by signalling Unit Check with ATTENTION.

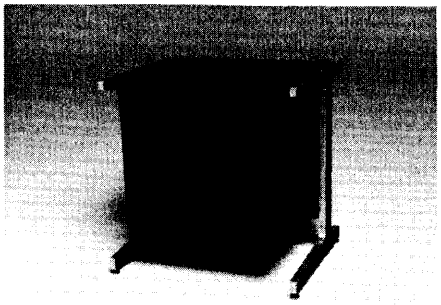
3.5.16 Halt I/O

This instruction causes the current operation at the addressed Channel or subchannel to be terminated. If the Channel is operating in burst mode a Halt I/O is issued regardless of the current activity in the Channel and on the interface. If the Channel is involved in the data transfer portion of an operation, data transfer is immediately terminated and the device is disconnected from the Channel.

3.5.17 Selective Reset

Selective Reset is issued only as a result of a malfunction detected at the Channel or a time-out by the Channel. Provided the I/O device is not presently in an operating mode all command sense and status information is reset. If the device is operating when Selective Reset occurs all sense and status information except for Busy is reset. When the device comes to a normal stopping point Device End is turned on. Once the Channel accepts Device End the Busy bit is reset.

Continued...



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3.5.18 System Reset

Whenever Operational Out and Suppress Out are low and the I/O device is in an On-Line mode, a System Reset is indicated. Once Operational In falls, the Adapter resets all buffers to zero except for byte 0 (device address) and byte 7 (active bit), so that a System Reconfigure is not necessary. The Adapter gives the system a Control Unit Busy status until all buffers have been reset to zero, and then goes into an idle mode waiting routine.

3.6 Channel Simulation

The Channel Adapter is equipped with an integral Channel Simulator which makes on-site self-testing simple and easy. The Simulator is selected by the Adapter's OPERATE/TEST switch, and controlled by a diagnostic program which executes in the Datapoint processor.

The Simulator may be operated without disconnecting the Adapter from the Channel I/O interface.

3.6.1 Simulator Logic

The Simulator consists of a group of registers which are either read from or written to by the Datapoint processor diagnostic program. The Simulator shares with the Adapter some of its interfacing facilities: both Adapter and Simulator use the same AOUT bus, COM receivers and AIN bus drivers; however, the addressing of the Simulator is separate from that of the Adapter. The Simulator is strapped at the factory with an address of 0216.

The Simulator logic uses the following command strobes from the Datapoint processor: EX ADR, EX STATUS, EX DATA, EX WRITE, EX COM1, EX COM2, EX COM3, EX COM4.

These strobes are used to address the Simulator and read and write from registers which control and monitor the bus and tag signals to the Adapter logic, as follows:

3.6.2 EX ADR

If the Simulator address (0216 octal) is on the AOUT bus and the AOUT bus has correct parity, an EX ADR command addresses it. The Simulator must be addressed before any other command strobes can be issued, and if the Datapoint processor addresses any other peripheral, including the Adapter, that causes the Simulator to be deaddressed.

When the Simulator is addressed, bit 0 of the status register is set. An EX ADR puts the Simulator into status mode, i.e., the status register is logically connected to the AIN bus.

3.6.3 EX STATUS

An EX STATUS command places the Simulator into status mode. If the Datapoint processor then executes an INPUT instruction, the contents of the Simulator's status register become available for inspection.

3.6.4 EX WRITE

EX WRITE causes the contents of the AOUT bus to be written into the BUS OUT is generated by the Simulator.

3.6.5 EX DATA

This command places the Simulator in DATA mode, by logically connecting the output of the BUS IN register to the AIN bus. If the Datapoint processor follows with an INPUT instruction, it gains access to the contents of the BUS IN register.

3.6.6 EX COM1

EX COM1 controls the OUT TAGS from the Simulator to the Adapter. The contents of the AOUT bus are loaded into the TAG OUT register.

Consult 3.6.10.3 for the format of the TAG OUT register. Control of the OUT TAGS is done in the manner described in the IBM System 360/370 I/O Interface Channel To Control Unit Original Equipment Manufacturer's Information; GA22-6974-0.

3.6.7 EX COM2

An EX COM2 command inverts BUS OUT PARITY. This feature allows the Simulator software to create parity errors and then check the response of the Adapter to them.

The COM2 strobe loads the COM2 register, of which only the high-order bit (bit 7) is used. When bit 7 on the AOUT bus is high during execution of an EX COM2 instruction the parity of BUS OUT will be even (invalid) parity, and will continue so until reset by the execution of an EX COM2 instruction with all zeros on the AOUT bus, after which BUS OUT PARITY will function correctly.

3.6.8 EX COM3

An EX COM3 command to the Simulator reads the IN TAGS from the Adapter.

An EX COM3 instruction logically connects the output of the TAG IN register to the AIN BUS. When the Datapoint processor diagnostic program executes an INPUT instruction the contents of this register are read. Consult 3.6.10.4 for the format of the TAG IN register.

3.6.9 EX COM4

The EX COM4 command logically connects the output of the COM4 register to the AIN BUS. Only the high-order bit (bit 7) of the COM4 register is used; if set, it indicates invalid parity on BUS IN.

3.6.10 Simulator Register Descriptions

3.6.10.1 BUS OUT Register

Data written into the BUS OUT register appears to the Adapter to be on the Channel's BUS OUT. Parity for this register is generated by the Simulator under the control of the COM2 register's Bus-Out Parity bit.

3.6.10.2 BUS IN Register

This register represents the Adapter's BUS IN. The diagnostic program may examine it by executing an EX DATA instruction followed by an INPUT instruction. Simulator logic checks parity on BUS IN; parity information is available in the COM4 register.

Note that data on BUS IN is only valid when an appropriate TAG IN tag has been raised.

Continued....

3.6.10.3 TAG OUT Register

This register controls the TAG OUT lines to the Adapter. It has the following format:

0.....Operational Out (Opl Out)
1.....Hold Out (Hld Out)
2.....Select Out (Sel Out)
3.....Suppress Out (Supp Out)
4.....Address Out (Adr Out)
5.....Command Out (Cmd Out)
6.....Service Out (Srv Out)
7.....Not used

An EX COM1 instruction executed by the diagnostic software writes data from the A OUT bus into the TAG OUT register. TAG OUT tags are raised or lowered by varying the data on the A OUT bus and executing successive EX COM1 instructions.

3.6.10.4 TAG IN Register

This register represents the TAG IN lines to the Adapter. It has the following format:

0.....Operation In (Opl In)
1.....Not used
2.....Not used
3.....Request In (Req In)
4.....Address In (Adr In)
5.....Status In (Sta In)
6.....Service In (Srv In)
7.....Not used

The Datapoint processor's diagnostic program may examine the TAG IN tags by executing an EX COM3 instruction followed by an INPUT instruction. If any bit of the TAG IN register is high or set when read, the tag corresponding to that bit is high or set.

NOTE: All sequences involving use of the TAG IN and TAG OUT registers must conform to the Channel sequences described in lthe IBM System 360/370 I/O Interface Channel To Control Unit Original Equipment Manufacturer's Information; GA22-6974-0.

3.6.10.5 COM2 Register

The COM2 register is used to create invalid parity on the Simulator's BUS OUT, by setting bit 7 -- the only bit used in the register -- high. When bit 7 is low, normal (odd) parity exists on BUS OUT. The Datapoint diagnostic program loads the COM2 register by placing the desired bit pattern in the processor's A register, addressing the Simulator, and issuing an EX COM2 instruction.

3.6.10.6 COM4 Register

Bit 7 -- the high-order bit -- of this register is an indication of the Adapter's BUS IN parity; if high, it signifies even (invalid) parity, if low, normal (odd) parity. The diagnostic program reads it by issuing first an EX COM4, then an INPUT instruction.

Note that parity on BUS IN need be valid and should be checked only when one of the following TAG IN tags is high: SERVICE IN, STATUS IN, or ADDRESS IN.

3.6.11 Simulator Operation

The Channel Simulator is addressed when the Adapter is in OFF-LINE mode and the Operate/Test switch on the rear of the chassis is in TEST position. Switching from Operate to TEST logically disconnects the Adapter from the IBM Channel interface, and connects it to the simulated Channel interface.

NOTE: The Operate/Test switch is only effective if the Adapter is in OFF-LINE mode. Once commanded to go ON-LINE, the Adapter remains in whichever mode was set by the switch while last OFF-LINE.

With the Adapter in TEST, the Simulator's registers must be initialized, by causing the diagnostic program to write all zero bytes into BUS OUT, TAG OUT, and EX COM2 registers. After that, the Operational Out bit (bit 0) in the TAG OUT register must be set, to avoid an immediate System Reset indication from the Adapter when it is commanded to go ON-LINE. Thereafter, the diagnostic program may begin to exercise the Adapter's functional operation.

To end testing, the diagnostic program commands the Adapter to go OFF-LINE, after which the Operate/Test switch may be moved to OPERATE, logically reconnecting the Adapter to the IBM Channel interface again.

4.0 Physical Description

The Adapter is packaged in a free standing equipment cabinet separate from the processor and disk drives, or in a console on which sits the Datapoint processor.

9426 Adapter - Console

Width	36.0 in. (91.44 cm)
Depth	53.0 in. (134.58 cm)
Height	28.5 in. (72.39 cm)
Weight	180 lbs. (81.37 kg)

9427 Adapter - Freestanding

Width	36.0 in. (91.44 cm)
Depth	28.5 in. (72.39 cm)
Height	28.5 in. (72.39 cm)
Weight	120 lbs (54.18 kg)

See Figure 4-1

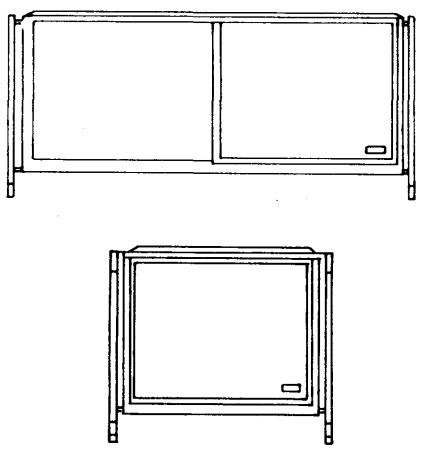


Figure 4-1 Channel Adapter

5.0 Environmental Requirements

	Minimum	*Maximum*
Temperature	10 degrees C 50 degrees F	38 degrees C 80 degrees F
Relative Humidity	20%	80%
Primary Power	100 VAC ±10% 120 VAC ±10% 220 VAC ±10% 230 VAC ±10% 240 VAC ±10%	
Line Frequency	50 Hz or 60 Hz ± 1 Hz	
Input Current	100/120 VAC - rated 3.0 AMPS 220/230/240 VAC - rated 1.5 AMPS	
Power	225 Watts	
Heat Dissipation	770 BTU 172.04 Kcal 812.20 KJ	

Continued...

6.0 Interface Requirements

6.1 Datapoint Processor

The 9426/9427 Adapter is connected to the Datapoint processor using a standard Datapoint I/O Cable. In the daisy chain of devices attached to the I/O bus, the Channel Adapter must precede any device which does not pass parity down the bus.

Connection to the IBM Channel is via standard IBM cables.

6.2 IBM Channel Command Formats

IBM System 360/370 command byte formats given below are for the most common unit record I/O devices.

6.2.1 IBM 2501 Card Reader

Commands		*Bit Patterns*
	Datapoint	7 6 5 4 3 2 1 0
	IBM	0 1 2 3 4 5 6 7
Read		0 0 0 0 0 0 1 0
Read Card Image		0 0 1 0 0 0 1 0
Sense		0 0 0 0 0 1 0 0
Control (No-op)		0 0 0 0 0 0 1 1
Read (2501 compatibility)*		0 0 0 1 0 0 1 0
Test I/O		0 0 0 0 0 0 0 0

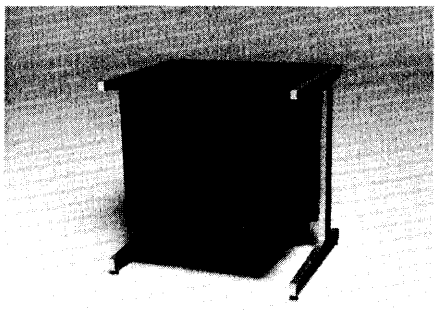
*This command is used when the IBM System 360/370 is processing data while emulating a 1401 or a 1620 Data Processing System.

6.2.1.1 Read

READ commands the card reader to read the next card in its hopper. As the card passes the read station, its data bytes are transferred to the Channel as they are read. The IBM 2501 transfers data to the Channel one byte at a time, i.e., each data byte sent requires a selection sequence initiated by the control unit. Emulation of the 2501 by the Adaptor, however, transfers four data bytes per selection. The Unit Exception status bit is presented to the Channel at initial selection of the READ command which follows reading of the last card.

6.2.1.2 Read Card Image

READ CARD IMAGE commands the card reader to read the next card in its hopper, but read the data in column binary code -- a special feature of the 2501. Each column read in a card image read is transferred to the Channel using two data bytes. The first byte from each column occupies the odd byte of a pair of bytes in the processing unit's storage; the second half of the column goes to the next higher even byte. READ CARD IMAGE may accept any combination of punches in a single card column.



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6.2.1.3 Sense

A SENSE command transfers bytes containing the sense information of the 2501 and any unusual condition detected during the previous operation. The transmitted sense byte has the following bit assignments:

Datapoint

7.....Command Reject
6.....Intervention Required
5.....Bus Out Check
4.....Equipment Check
3.....Data Check
2.....Overrun
1.....Not used
0.....Not used

IBM

0.....Command Reject
1.....Intervention Required
2.....Bus Out Check
3.....Equipment Check
4.....Data Check
5.....Overrun
6.....Not used
7.....Not used

Command Reject indicates an invalid command. It also occurs when a Read Data Mode 2 command was issued but the Card Image feature is not installed. An invalid command will not be executed.

Intervention Required means operator attention is needed to empty the card stacker, fill the input hopper, press End-Of-File, clear the transport, close the cover, or restore Ready status.

Bus Out Check means the 2501 has detected a parity error in the command received. Execution of the command will not be attempted.

Equipment Check indicates that the two successive readings of a punched column did not agree, or that the read station failed before reading began.

Data Check indicates that the 2501 detected an invalid card column, consisting of more than one punch in rows 1 through 7, while in Data Mode 1.

Overrun indicates that the Channel failed to accept a data byte from the 2501 before the next byte was ready.

6.2.1.4 Control (NO-OP)

The NO-OP command is an immediate command. Channel End and Device End are presented to the Channel during the initial selection sequence for a NO-OP command. During the Control NO-OP command no transmission of data is involved.

6.2.1.5 Read, 2501 Compatibility

This command is identical to the READ command except that the Unit Exception status is presented with the Channel End for the last card read.

6.2.1.6 Test I/O

The Test I/O command is initiated by the CPU; it places an 8-bit unit address on the unit address bus out line. Upon receiving this address the 2501 places its current status on the bus. The status byte has the following bit assignments:

Datapoint

7.....Not used
6.....Not used
5.....Not used
4.....Busy
3.....Channel End
2.....Device End
1.....Unit Check
0.....Unit Exception

IBM

0.....Not used
1.....Not used
2.....Not used
3.....Busy
4.....Channel End
5.....Device End
6.....Unit Check
7.....Unit Exception

Continued....

Busy indicates that the 2501 is operating and has no Channel End to report.

Channel End means all data has been sent from the 2501 to the program.

Device End means that a point has been reached in mechanical operation at which the 2501 can accept a new command.

Unit Check means the program should issue a SENSE command to determine the nature of the exception condition and the action necessary.

Unit Exception is sent in response to Initial Selection for the first read command after the last card has been read and stacked. When the 2501 is operating in 2501 compatibility mode, Unit Exception accompanies Channel End for the last card.

6.2.2 IBM 1403 Printer

Commands	*Bit Patterns*
Datapoint	7 6 5 4 3 2 1 0
IBM	0 1 2 3 4 5 6 7
Read for diagnostic purpose	0 0 0 0 0 0 1 0
Write	0 0 0 0 0 0 0 1
Control (No-Op)	0 0 0 0 0 0 1 1
Sense	0 0 0 0 0 1 0 0
Test I/O	0 0 0 0 0 0 0 0

6.2.2.1 Read, Diagnostic Data

READ, DIAGNOSTIC DATA, performs a data transfer from the data buffer to the Channel. This command usually follows a diagnostic write. The data returned to the Channel should compare, bit for bit, with the data sent. In multiplex mode a diagnostic read data transfer is in two-byte bursts. Buffer bits corresponding to data bytes read are as follows:

Buffer	C B A 8 4 2 1
Byte Bit Position:	1 2 3 4 5 6 7

6.2.2.2 Write

The WRITE command causes the printer to print the contents of the data buffer. The three low-order bits of the write command sent over the Channel do not cause any automatic carriage operation. In order to provide for carriage operation, modifier bits accompany the write command to accomplish spacing from one to three lines or selecting a new Channel, as follows:

IBM	*Datapoint*	
	0 1 2 3 4 5 6 7	7 6 5 4 3 2 1 0	
	0 0 0 0 0 0 0 1	Write (no automatic space)
	0 0 0 0 1 0 0 1	Write; space 1 line after print
	0 0 0 1 0 0 0 1	Write; space 2 lines after print
	0 0 0 1 1 0 0 1	Write; space 3 lines after print
	1 0 0 0 1 0 0 1	Write; skip to Channel 1 after
	1 0 0 1 0 0 0 1	Write; skip to Channel 2 after
	1 0 0 1 1 0 0 1	Write; skip to Channel 3 after
	1 0 1 0 0 0 0 1	Write; skip to Channel 4 after
	1 0 1 0 1 0 0 1	Write; skip to Channel 5 after
	1 0 1 1 0 0 0 1	Write; skip to Channel 6 after
	1 0 1 1 1 0 0 1	Write; skip to Channel 7 after
	1 1 0 0 0 0 0 1	Write; skip to Channel 8 after
	1 1 0 0 1 0 0 1	Write; skip to Channel 9 after
	1 1 0 1 0 0 0 1	Write; skip to Channel 10 after
	1 1 0 1 1 0 0 1	Write; skip to Channel 11 after
	1 1 1 0 0 0 0 1	Write; skip to Channel 12 after
	0 0 0 0 0 1 0 0	Sense

6.2.3 IBM 2540 Card Reader-Punch

Commands:	*Datapoint*	7 6 5 4 3 2 1 0
	IBM	0 1 2 3 4 5 6 7
Read Feed and Select Stacker		
Stacker R1		0 0 C 0 0 0 1 0
Stacker R2		0 1 C 0 0 0 1 0
Stacker RP3		1 0 C 0 0 0 1 0
Read and No Feed or Stacker Select		1 1 C 0 0 0 1 0
Read, Feed, and No Stacker Select (compatibility)		1 1 C 1 0 0 1 0
Write Feed and Select Stacker		
Stacker P1		0 0 C 0 0 0 0 1
Stacker P2		0 1 C 0 0 0 0 1
Stacker P3		1 0 C 0 0 0 0 1
Sense		0 0 0 0 0 1 0 0
No-Op		0 0 0 0 0 0 1 1
Test I/O		0 0 0 0 0 0 0 0

C = 0 in Data Mode 1; C = 1 in Data Mode 2

6.2.3.1 Read, Feed, and Select Stacker

The 2540 reads the next card in the hopper and transfers the data to the Read-buffer, from whence it goes on the Channel to main storage. After the card is read it is fed to the specified stacker and the next card is read.

6.2.3.2 Read and No Feed or Stacker Select

The 2540 reads a card from the hopper, and sends the data to main storage or Punch Feed Read (PFR) -- a special feature which allows the punch to be used for card reading with or without card punching, concurrently with card reading in the read feed. Subsequently, no more cards are fed; the 2540 waits for a new command.

In PFR, data read from the Punch Feed Read and data sent to the punch both pass through a common buffer. To avoid loss of read data, when a read is to be done in the punch feed a read must be given to the punch unit before a punch cycle is initiated by a write command.

Continued...

6.2.3.3 Read, Feed and No Stacker Select (compatibility)

Read-buffer data is sent to the Channel; after data transfer is complete, Channel End and Device End are presented to the Channel. ATTENTION (Status Bit 0) is returned at Initial Selection for a sense command. At this time a Feed and Select Stacker instruction can be issued to specify which stacker to put the card in. Device End is returned to the Channel after the automatic feed has taken place or the feed initiated by a Feed and Select Stacker command. If such a command has been neither issued nor accepted, the card is put in stacker R1.

6.2.3.4 Feed and Select Stacker

The card stacked is the one whose data was sent to the Channel on the preceding read command. The data from the card passing the read station is read into the read buffer.

6.2.3.5 PFR Write, Feed, and Select Stacker

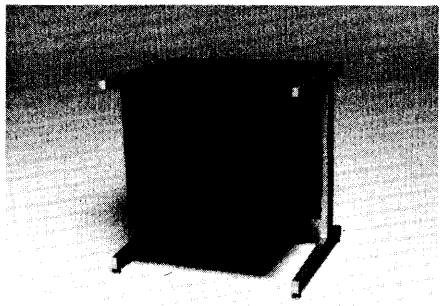
The 2540 feeds in a card and data is sent from the Channel to the punch buffer. This data is also punched into the card at the punch station. Any stacker slection specified by this command pertains to the card being punched. The stacker select information is retained so that on the next feed cycle the card is stacked in the selected stacker. If this command is not used as the first command after initial run-in the data read at the punch check station will be compared with the total hole count from the data punched and the data read at the PRF brushes; if the quantities do not match that card is stacked into P1.

6.2.3.6 Write, Feed and Select Stacker

This mode of operation resembles PRF Write, Feed and Select Stacker except that card data is not read by the PRF brushes.

Data Mode 1 -- used when translating the Extended Binary Coded Digital Card Code to and from the 8-bit EBCDIC.

Data Mode 2 -- In this mode the 12 bits from each card column are expressed as two (2) 8-bit bytes, composed of two zeroes (bits 0 and 1) and 6 bits from the card image buffer column as follows:



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Card Row Bit	*Interface Bit*
12	2 Odd Byte
11	3 Odd Byte
0	4 Odd Byte
1	5 Odd Byte
2	6 Odd Byte
3	7 Odd Byte
4	2 Even Byte
5	3 Even Byte
6	4 Even Byte
7	5 Even Byte
8	6 Even Byte
9	7 Even Byte

This mode allows transmitting any punched hole appearing in the card. For punching in column binary, the bytes sent from main storage are acted upon in the folowing manner.

- Bits 0 and 1 are not valid but are used for parity checking calculated on that particular byte.
- Bits 2 through 7 are transferred to the punch.

6.2.4 IBM 1052 Printer/Keyboard Console Emulation

Like any other System 360/370 I/O device, the 1052 and its associated control unit are controlled by I/O instructions and commands issued by the supervisor program. The valid commands are:

Commands		*Bit Patterns*
	Datapoint	7 6 5 4 3 2 1 0
	IBM	0 1 2 3 4 5 6 7
Sense		0 0 0 0 0 1 0 0
Control (No-Op)		0 0 0 0 0 0 1 1
Control (Alarm)		0 0 0 0 1 0 1 1
Write (Auto Carrier Return)		0 0 0 0 1 0 0 1
Write (Inhibit Carrier Return		0 0 0 0 0 0 0 1
Read Inquiry (Or Read)		0 0 0 0 1 0 1 0

6.2.4.1 Control (NO-OP)

This command is a control immediate and Channel End and Device End are both signalled in the unit status response to the Channel. This command is handled by the Adapter's microprogram. The command is not indicated to the Datapoint software control program.

6.2.4.2 Control (Alarm)

This makes the 1052 audible alarm sound for 2 seconds. The alarm may be emulated by the Datapoint processor software control program either with EX BEEP or EX CLICK. If more than one EX BEEP or EX CLICK is issued in succession, only one alarm cycle will result.

6.2.4.3 Read (Read Inquiry)

Depressing the request key on the 1502 keyboard causes an I/O interrupt to the CPU (asynchronous status transfer), to which the program normally responds by sending a read inquiry command to the 1052. Acceptance and execution of this command lights the PROCEED light on the 1052, after which the operator may key in any characters; they will be sent to the Channel one at a time. Characters may be keyed in until the command is terminated in one of the following ways:

1. By depressing and holding the alternate coding key and then depressing the numeric 5 key (End Of Block -- EOB -- with alternate coding) which sends an end of transmission signal to the 1052's control unit. The messages previously keyed in will be transferred to main storage.

2. By depressing and holding the alternate coding key and then depressing the numeric 0 key, which sends a cancel signal to the control unit, indicating an operator error in the message and requiring the entire to be retransmitted.

3. By a Channel-initiated stop signal procedure.

Continued....

6.2.4.4 Sense

This Channel-initiated command transfers a byte of sense information from the 1052 to the Channel and thence to the byte location in main storage specified by the sense command. The sense byte in the 1052 is reset to zeros on initiation of a 1052 read, write, or control command.

The format of the 1052 sense byte is as follows:

Datapoint

Bit Position	*Bit Definition*
0	Not used
1	Not used
2	Not used
3	Not used
4	Equipment Check
5	Bus-Out Check
6	Intervention Required
7	Command Reject

IBM

7	Not used
6	Not used
5	Not used
4	Not used
3	Equipment Check
2	Bus-Out Check
1	Intervention Required
0	Command Reject

Equipment Check is set when a malfunction is detected in the 1052 or its associated control unit.

Bus-Out Check indicates that the console control unit has received a command code or a data byte with invalid parity over the I/O interface. It is set when one of the following conditions occurs:

1. When a command code with invalid parity is detected at the console control unit during a Channel-initiated command selection, or when the console control unit is not in a busy condition.

2. When invalid parity is detected on a data byte transfer during a write operation.

Intervention Required signifies a not ready condition of the 1052 and its associated control unit; it is set if any of the following conditions occur:

1. When the not ready key is depressed while the console control unit is not engaged in a Channel-initiated command selection, or when it is not in a busy condition.

2. When the printer runs out of forms and the console control unit is not in a busy condition or when it is not engaged in a Channel-initiated command selection.

Command Reject is set during Channel-initiated command selection if the command sent to the control unit cannot be executed because it is not defined for control unit.

6.2.4.5 Write

Two write commands are available: write (auto carriage return) and write (inhibit carriage return). The first automatically returns the carriage at the end of a message; the second does not.

The format of status byte for this command is as follows:

Datapoint

Bit Position	*Definition*
0	Unit Exception
1	Unit Check
2	Device End
3	Channel End
4	Busy
5	Not used
6	Not used
7	Attention

IBM

7	Unit Exception
6	Unit Check
5	Device End
4	Channel End
3	Busy
2	Not used
1	Not used
0	Attention

Status bits 7, 4, 3, 2, 1, and 0 are reset by any one of the following:

System Reset
Selective Reset
Acceptance of the status bit by the Channel

Unit Exception -- This status bit is sent to the Channel during Channel End time in a read operation if Channel End has been initiated by a cancel from the keyboard.

Unit Check -- This status bit is set when any of the sense bits are set except Intervention Required, but it is also set if Intervention Required is detected during Channel-initiated command selection of a valid read or write command. If Unit Check is present, the read or write command is not initiated.

Unit Check status may be sent during a Channel-initiated command selection sequence or when Channel End or Device End is sent.

At Channel-initiated command selection time the Command Reject, Bus-Out Check, and Intervention Required sense bits may be set.

At Channel End or Device End, Bus-Out Check and Equipment Check may be set.

Device End -- When set, this bit indicates that the 1052 and its console control unit have completed an operation or that the 1052 has gone from not-ready to read status.

Execution of a Control No-Op or a Control Alarm operation sets Device End and sends it to the Channel during a Channel-initiated command selection.

Execution of a sense operation sets Device End and sends it to the Channel after transfer of one data byte from the sense register. A read or write operation sets Device End and sends it to the Channel upon completion of the mechanical cycle of the printer.

Channel End -- This bit indicates to the Channel that the console control unit may be disconnected from this I/O interface, even though the device may be completing an operation. Execution of a Control No-Op or Control Alarm operations sets Channel End and sends it to the Channel during a Channel-initiated command selection.

A sense operation sets Channel End and sends it to the Channel after transfer of one data byte from the sense register. A write operation sets Channel End and sends it to the Channel after one of the following conditions:

1. After receipt of a stop signal sequence from the Channel indicating the end of data transfer.

2. After an end-of-block (EOB) indication from the keyboard.

3. After a cancel indication from the keyboard.

Busy -- This bit is set:

1. After a Channel-initiated selection for a read, write, or sense operation.

2. At the time the Attention status bit is set.

3. When the 1052 goes from a not-ready to a ready status.

4. Whenever status bits are stacked by the Channel this bit is reset:

a. After acceptance of the status byte by the Channel.

Continued...

b. After acceptance of the Device End status bit by the Channel.

c. After a system reset.

d. After a selective reset.

A Busy condition on the 1052 makes the console control unit send a Busy status bit to the Channel during a Channel-initiated command selection if any of the following conditions occur:

1. New Commands (except Text I/O):

a. After Channel End has been stacked in the console control unit.

b. After Device End has been generated at the console control unit but either has not been sent to the Channel or has been stacked in the console control unit.

c. After Attention has been generated in the console control unit but either has not been sent to the Channel or has been stacked in the console control unit.

2. New Commands (including Test I/O).

a. After a previous Channel-initiated command selection and before Channel End has been generated.

b. After Channel End has been sent and accepted by the Channel but Device End has not been generated.

Attention -- This bit is set when the Request key is depressed and all the following conditions exist:

1. The console control unit is not Busy.

2. The console control unit is not engaged in a Channel-initiated selection.

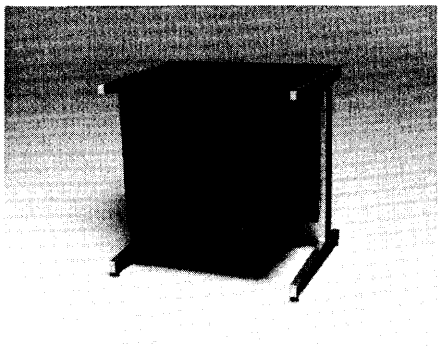
3. Command chaining is not in progress.

After Attention status has been set the console control unit and the 1052 become Busy. Any new commands -- except the Test I/O -- issued at this time will not be initiated by the console control unit. The initial status byte will contain Busy and Attention status bits. The console control unit will remain Busy with the Attention status bit set until the Attention bit is accepted by the Channel.

In the case of Test I/O, the Attention bit will be sent alone during initial status.

6.2.4.6 Special Key Functions

1. Ready Key -- Pressing this key causes the 1052 to become ready.



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2. Request Key -- Causes the 1052 to set the Attention status bit.

3. Not Ready Key -- Causes the 1052 to become Not Ready, thereby prohibiting read or write operations.

4. Alternate Coding Key-- Allows dual output coding from the numeric row of keys. The dual coded keys are the 5 and 0.

5. EOB -- Generates an End-Of-Block code when the 5 key and the Altn. Coding Key are pressed simultaneously.

6. Cancel -- Generates a cancel code when pressed simultaneously with the 0 key and the Altn. Coding Key.

7.0 Options

9427 - Freestanding cabinet

The 9427 Channel Adapter in a freestanding cabinet is optionally available with a 230 VAC power supply.

The 9427 Channel Adapter in a freestanding cabinet is optionally available with either an 8-foot or a 5-foot length of Datapoint I/O cable for connection to the Datapoint processor.

IBM Bus/Tag cables are used, and are available from Datapoint.

9426 - Console cabinet

The 9426 Channel Adapter in a Datapoint console is optionally available with either an 18-inch or a 42-inch length of Datapoint I/O cable for connection to the Datapoint processor.

IBM Bus/Tag cables are used, and are available from Datapoint.

The 9426/9427 Channel Adapter is available in either 1-byte or 4-byte mode strapping, and with either High or Low Priority strapping.

8.0 Shipping List

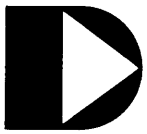
The following items are shipped with each Channel Adapter:

Quantity	*Item*	*Model Code/Part Number*
1	Cable, Assembly, External Device	11-1055-001
1	Cable, Assembly, IBM Channel	(nr. on request)
1	Product Specification	60641

NOTE: This shiping list is for information only; the appropriate Datapoint Shipping List prevails in all cases.

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

DATAPOINT CORPORATION



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