ETA Systems ETA10 Series

PRODUCT DESCRIPTION

As part of an all-out assault on the minisupercomputer and Cray supercomputer markets, ETA Systems introduced two low-end ETA10 machines that are said to pack the punch of a "true supercomputer" at a starting price of less than $1 million. The new ETA10 Models P and Q, one-to-two processor systems announced in October 1987, have a peak performance of 750 of floating points per second (MFLOPS) and 947 MFLOPS, respectively. The models are meant to fill a price/performance gap between minisupers from Alliant Computer Systems and Convex Computer Corporation and more powerful supercomputers from Cray Research and Japanese supercomputer manufacturers. The Model P became available last October; the Model Q will become available during March 1988.

The ETA low-end additions bring the ETA10 line up to four processors. The other two systems are the Model E, a one-to-four processor system first delivered to Florida State University in 1986, and the top-end Model G, a two-to-eight processor system scheduled to be delivered this year. With the availability of four processors, users can now choose from 44 possible configurations over a performance range of 27 to 1, according to ETA.

To provide these price/performance possibilities, ETA offers a range of CPU cycle times and main memory configurations. CPU cycle times are 7 nanoseconds for the Model G, 10.5 nanoseconds for the Model E, 19 nanoseconds for the Model Q, and 24 nanoseconds for the Model P. Additionally, the two low-end models can be configured with up to 512 megabytes of shared memory, while the Model E can have up to one gigabyte of shared memory and the Model G up to 2 shared gigabytes. The heart of all ETA systems is a single 44-layer board containing

PRODUCT ANNOUNCED: ETA10 Models P, Q, E, and G.

COMPETITION: Cray-2 and X-MP Series, Honeywell-NEC Supercomputers, Amdahl Vector Series, Alliant FX Series, Convex C1 XL and C1 XP, and Scientific Computer-40.

DATE ANNOUNCED: Model E, March 1987; and Model G, April 1987; Models P and Q, October 1987.

SCHEDULED DELIVERY: Model E, shipped third-quarter 1987; Model G, available 1988; Model P, shipped October 1987; Model Q, available March 1988.

BASIC SPECIFICATIONS

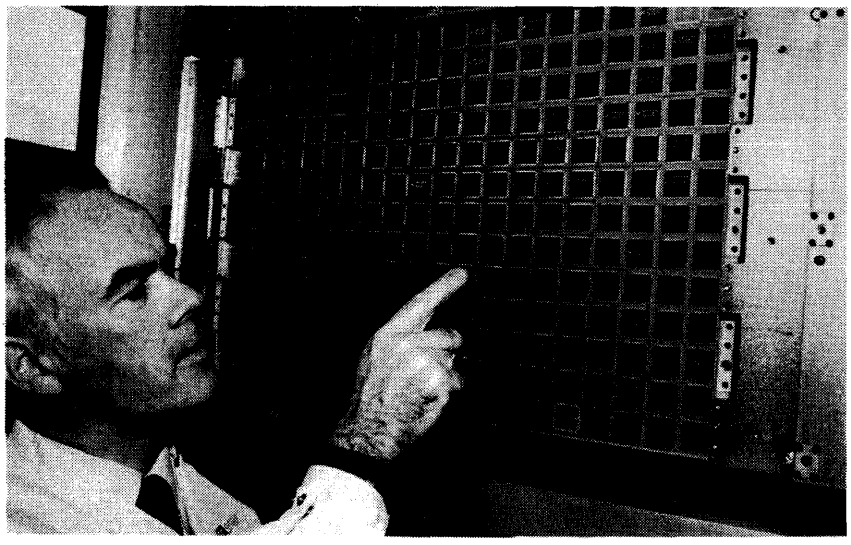
MANUFACTURER: ETA Systems Inc., a Control Data Corporation subsidiary, 1450 Energy Park Drive, St. Paul, Minnesota 55108. Telephone (612) 642-3408.

MODELS: Model P, one or two processors; Model Q, one or two processors; Model E, one to four processors; Model G, two to eight processors.

CONFIGURATION: The entry-level Model P can be configured with one or two processors, 64 megabytes to 512 megabytes of shared memory, 32 megabytes of local CPU memory, and four input/output (I/O) units.

The Model Q can be configured with one to two processors, 64 to 512 megabytes of shared memory, 32 megabytes of local CPU memory, and four I/O units.

The Model E can be configured with one to four processors, 256 megabytes to 1 gigabyte of shared memory, 32 megabytes of local CPU memory, and nine I/O units.



This 44-layer board containing 240 semiconductor devices is the heart of a typical ETA10 supercomputer. The ETA10 line now includes four supercomputer models that can include from one to eight processors and from 64 megabytes to 2 gigabytes of main memory. Peak performance ranges from 750 million floating points per second to 10 billion floating points per second.

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complementary metal oxide semiconductor (CMOS) chips. Up to 240 chips are placed on a single board.

In the operating system software area, ETA machines operate under both EOS (ETA Operating System), a proprietary operating system, and an implementation of AT&T's UNIX System V, which will become available during third-quarter 1988.

UNIX is particularly strategic to ETA. UNIX implementations have become quite popular among vendors selling minisupercomputers and related products designed for numeric-intensive computing. UNIX supports an abundance of existing third-party applications and presents scientific users with an operating environment with which they are already familiar.

In addition to these advantages, ETA plans to use the UNIX option to provide a common link between ETA10 systems and the Control Data Cyber mainframe line, which operates under NOS/VE. The Cyber 910 scientific workstation already operates under UNIX. Under current plans, Cyber users operating under the Cyber NOS/VE operating system will be able to initiate jobs on the standard Control Data mainframe line and then process them on an ETA10.

ETA Systems, a CDC spin-off formed in 1983, designed, built, and began testing the first ETA supercomputers in little more than three years. The first model, now designated the ETA Model E, underwent beta testing at Florida State University in 1986 and 1987. Additional machines have since been installed at the John Von Neumann Center in Princeton, New Jersey, the German Weather Service, the Minnesota Supercomputer Center in Minneapolis, the Tokyo Institute of Technology, and the NASA-Ames Research Center in California.

In addition to these sites, ETA officials announced they have orders or letters of intent for their newest low-end systems. New orders have come from the Canadian Atmospheric Environment Service of Montreal, Canada, the University of Western Ontario, the Mid-America Research Institute of Oklahoma, and the University of Georgia.

RELATIONSHIP TO CURRENT PRODUCT LINE: ETA, Control Data's young offspring, is now positioned to carry on CDC's supercomputer efforts at the extreme high end of the market. In addition to the introduction of four supercomputer models within the last year, ETA now supports CDC Cyber 205 supercomputers, which can only be obtained on an "as available" basis. CDC shifted Cyber 205 marketing responsibility to ETA in January 1987. To protect the software investment of CDC's 30 Cyber 205 customers and to encourage 205 users to migrate to the new ETA systems, the company has made the ETA10 operating system compatible with the Cyber 205 Virtual Storage Operating System (VSOS) environment. Cyber 205 systems first became available in March 1981.

The Model G can be configured with two to eight processors, 512 megabytes to 2 gigabytes of shared memory, 32 megabytes of local CPU memory, and 18 I/O units.

Each ETA system can be configured with a DSU10-1, 1.4-gigabyte capacity disk or DSU12-1, 1.2-gigabyte capacity disk. The DSU10-1 unit has a transfer rate of 12 megabytes per second, and the DSU12-1 unit has a transfer rate of 3 megabytes per second. Up to 32 DSU10-1 drives and up to 16 DSU12-1 drives can be attached to an I/O unit. In addition, the ETA10 supports 1600/6250 bit-per-inch, nine-track tape units with a transfer rate of 200 inches per second. Systems are also compatible with Ethernet, the Control Data Loosely Coupled Network (LCN), and HYPERchannel.

CENTRAL PROCESSOR AND MEMORY: ETA10 systems are designed around complementary metal oxide semiconductor (CMOS) technology obtained from Honeywell Inc., which manufactures the CMOS-based gate array chips for ETA. A single chip contains 20,000 logic gates. Up to 240 chips are placed on a single 44-layer board that measures 16 inches by 22 inches. The processor board, common to all the models, uses dense packaging to enhance cycle time and throughput. To achieve different price/performance levels, ETA has varied CPU cycle times. Top-end Model G cycle time is 7 nanoseconds, the Model E is 10.5 nanoseconds, the Model Q is 19 nanoseconds, and the Model P is 24 nanoseconds.

Architecturally, an ETA10 supercomputer can contain up to eight central processing units (CPUs). Each CPU contains a scalar processor, vector processor, and local memory. Each processor is connected to a larger shared memory, a communications buffer, a service unit, and input/output units.

The CPU scalar unit processes tasks that can best be handled sequentially. The scalar unit contains a 256-word element, high-speed register file, and a 64-word instruction stack.

The vector unit handles closely related data elements expressed in the form of arrays or tables. The vector unit operates in parallel with the scalar unit and I/O channels. The unit handles single- or double-stream input vectors from memory and returns them to memory in a single stream.

In addition to processing units, ETA systems employ a three-tiered memory structure consisting of local memory, shared memory, and a special communications buffer. Each CPU in any ETA system contains 32 megabytes of local memory. Local memory is a kind of buffer area that helps the CPU sustain transfers from scalar/vector units and high-speed memory without producing memory conflicts. Shared memory on ETA systems ranges from 64 megabytes to 2 gigabytes. The memory bandwidth is high enough to support up to eight CPUs and up to 18 I/O units simultaneously. The communications buffer provides a high-speed memory that is common to both CPUs and I/O units. The buffer reduces the processing burden of the other processors to maintain parallel operations.

The service unit provides the systems with an operator and maintenance interface.

PHYSICAL CHARACTERISTICS: The Models P and Q are five feet high, two feet wide, and seven feet deep. A single-processor Model P or Model Q requires a 120 V AC, three-phase, 60 Amp power source. Both models are air cooled and don't require any special cooling or the raised floor characteristic of a computer room environment.

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Besides providing a migration path for Cyber users, the ETA line is designed to provide a smoother growth path for departmental scientific/engineering users who will eventually need to migrate to larger systems as their computing requirements expand. This has become a key ETA marketing strategy. The ETA10 Models P and Q lower the ETA10 entry point and ostensibly make supercomputing more affordable to a larger number of users. Additionally, the new models extend the supercomputing performance range and the upgrade growth path. Prices range from $850,000, for an entry-level Model P with a peak performance of 750 MFLOPS, to $22 million for an eight-processor Model G with a peak performance of 10 billion floating points per second (GFLOPS). Relative performance of the four systems ranges from 1.0 for a minimally configured Model P to 6.9 for a minimally configured Model G. Relative performance for fully configured systems ranges from 2.0 for a Model P to 27.4 for a Model G.

COMPETITIVE POSITION: For more than a decade, supercomputing has been synonymous with Cray Research, Inc. and for good reason. In 11 years, Cray has installed more than 180 multimillion dollar supercomputers worldwide and now owns more than 70 percent of the market. Invariably, as new players enter the field, they compare their price/performance against Cray. ETA Systems is no exception.

ETA top executives are now claiming their top-end systems are more powerful than Cray offerings and their two entry-level systems have better price/performance than Cray entry-level systems and minisupercomputers from Alliant, Convex, and Scientific Computers. For the time being at least, competitors may have a hard time challenging these claims.

The low-end Models P and Q are said to fill a price/performance gap between minisuper offerings and true supercomputers. The Model P, for instance, has a starting price of $850,000 and a peak performance of 750 MFLOPS. A fully configured Model P, featuring one CPU, 64 megabytes of shared memory, I/O units, disk drives, operating system software, a Fortran compiler, and programming tools, comes in at $995,000, the price of a supermini. The more powerful Model Q, which has a peak performance of 947 MFLOPS, starts at $1.2 million for a single-processor version. By comparison, an Alliant FX/8, which can be configured with two-to-eight computational processors, has a peak performance of 94.4 MFLOPS. Prices range from $185,000 to $1 million. A Convex C1 XP, configured with four processors, has a peak performance of 160 MFLOPS. An entry-level configuration sells for $475,000.

In response to new competitive pressures, Cray has made pricing adjustments and has also introduced a new entry-level supercomputer, the X-MP/14se, which has a starting price of $2,500,000. It replaced the X-MP/11 and X-MP/12, which sold for $4,000,000 and $5,000,000, respectively. Despite these substantial price adjustments, the new Cray model still comes in higher than the aggressively priced ETA entry-level machine priced for less than $1 million. The aggressive ETA pricing took many observers by surprise. Interestingly, the Cray X-MP/14se became available during the third quarter of 1987, about the same time ETA announced its lower-priced entry models. The ETA Model P became available when announced in October, while the Model Q is scheduled for shipment early this year.

At the high end of the performance spectrum, ETA hopes to overtake Cray with the delivery of the Model G, a two-to-eight processor system that has a peak performance of 10 GFLOPS and a starting price of $8.9 million. The Model E, a one-to-four processor system with a peak performance of 3.4 GFLOPS and a starting price of $5.5 million, was first delivered last year. By comparison, Cray

The Models E and G are cooled in liquid nitrogen to maximize the conductivity of the circuitry.

A Model E configured with one processor has a total footprint of 129 inches by 197 inches. A Model G configured with two processors has a total footprint of 187 inches by 197 inches, and a Model G configured with eight processors has a footprint of 187 inches by 249 inches. Heat dissipation for a single-processor system is 35,000 Btu. Power requirements range from 21.1kVAs for a single-processor system to 102.7kVAs for a full eight-processor system.

INPUT/OUTPUT SUBSYSTEM: ETA systems feature from 1 to 18 I/O units, depending on model. Maximum transfer rate between shared memory and each I/O unit is 440 megabits per second.

SOFTWARE: ETA machines run under the ETA operating system (EOS), an environment compatible with the Virtual Storage Operating System (VSOS) that runs on Control Data Cyber 205 supercomputers. The compatible operating systems make it possible for Cyber 205 users to migrate applications to an ETA operating environment.

In addition to EOS, the machines will also operate under an implementation of AT&T's UNIX System V, which will become available during third-quarter 1988. The UNIX option will provide a common link between ETA10 systems and the existing Cyber mainframe line, which operates under NOS/VE, and the Cyber 910 scientific workstation, which operates under UNIX. Under current plans, Cyber users working under the Cyber NOS/VE operating system will be able to initiate jobs on the standard Control Data mainframe line and then process them on an ETA10. Besides providing a common link, UNIX makes many existing UNIX applications available to ETA program developers.

In the connectivity area, Cyber and ETA10 systems will also be linked through Ethernet, TCP/IP, and the Control Data Loosely Coupled Network, which provides file transfer capabilities.

Pricing and Support: ETA supercomputers can be purchased or leased. The company offers either a one-year or three-year lease plan and a maintenance program. Detailed lease and maintenance pricing was not available at press time; however, the following price list does include base purchase prices.

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peak performance ranges from 160 MFLOPS for the X-MP/14se to 2.1 GFLOPS for the Cray-2S Series, according to *Computerworld* estimates.

In addition to peak performance ratings, ETA has published benchmarks for a variety of supercomputer models based on the Linpack 100 by 100 matrix at 64-bit full precision. Based on the Linpack benchmarks, ETA claims its top-end Models E and G are now the most powerful supercomputers on the planet. The Linpack benchmark attempts to measure how supercomputers would actually perform doing real jobs, which is considered a better gauge of performance than more theoretical peak performance ratings. To derive the benchmarks, supercomputers configured with one CPU solved a series of linear equations in the form of a 100 by 100 matrix. According to ETA, its Model G achieved 84 MFLOPS, and the Model E achieved 56 MFLOPS. The NEC SX-2 came in third at 43 MFLOPS, and the Cray X-MP-4, running just one CPU, came in fourth at 39 MFLOPS. The Cray X-MP-2 came in ninth at 24 MFLOPS, and the Cray-2 placed eleventh at 18 MFLOPS.

Cray is expected to respond to new price/performance challenges from ETA and Japanese supercomputer vendors selling through American partners with the introduction of the Y-MP Series, a follow-on to the X-MP Series, and the Cray-3, a follow-on to the Cray-2 Series. The Y-MP is expected to have a peak performance within the 8-to-10 gigaflop range, while the Cray-3 is expected to have a peak performance within the 16-to-20 gigaflop range. The Y-MP Series should appear during the first half of this year, while the Cray-3, incorporating new gallium arsenide chip technology, is expected to appear late in 1989.

In addition to price/performance, supercomputer vendors including ETA recognize the importance of third-party engineering/scientific applications. In this category, Cray emerges as the clear winner. At the moment, more than 500 proprietary and third-party applications packages can be run on Cray machines. ETA and other Cray competitors must play catch-up in this area. So far, ETA has agreements with more than 30 software vendors and remains in negotiation with about 30 more. Also, more than 100 applications that run on the Cyber 205 can also run on ETA systems, since the product lines use compatible operating systems. □

EQUIPMENT PRICES

		Purchase Price ($)
ETA10 Processors		
Model P	Processor Complex; features one processor, expandable to two, 64 megabytes of shared memory, 32 megabytes of local CPU memory, and four input/output (I/O) channels	850,000
Model Q	Processor Complex; includes one processor, expandable to two, 64 megabytes of shared memory, 32 megabytes of local CPU memory, and four I/O channels	1,200,000
Model E	Processor Complex; includes one processor, expandable to four, 256 megabytes of shared memory, 32 megabytes of local CPU memory, and nine I/O channels	5,500,000
Model G	Processor Complex; includes two processors, expandable to eight, 512 megabytes of shared memory, 32 megabytes of CPU memory, and 18 I/O channels ■	8,900,000