

SECTION 1

INTRODUCTION AND DESCRIPTION

DECtape provides the flexibility, speed, and storage capabilities of magnetic tape while maintaining the convenience of paper tape. Its size and portability, in addition to the reliability obtained by the tape format and track head arrangement, render its integration into overall systems an easily accomplished task. The 550 Control together with the DECtape Transport is used with either a PDP-1, -4, or -7 to provide a fast, convenient input-output device.

This manual will emphasize the operation of the 550 control since a complete description of the transport is available in the 555 DECtape Dual Transport manual (H-555).

DECTAPE CONTROL TYPE 550

The DECtape Control Unit 550 is a program break control. That is, it allows the transfer of information word by word between the computer and the DECtape Transport. Since the control does not deal with blocks of information from the tape, words can be individually read and written within certain general limits. Since the computer is required to attend to the needs of the control on a word by word basis, however, more of its time is spent in handling the needs of the control than would be the case if the control were of the block transfer type.

The DECtape Control Unit 550 contains electronic circuitry necessary for performing the logical and timing functions essential to the operation of the system; the transport unit contains the tape handling elements, the drive mechanism, and relays for switching the tape heads onto a master bus system.

Operation of the DECtape transport is, normally, controlled by an associated computer. However, manual control is also afforded, by means of the controls located on the front panel of the unit.

A maximum of four tape transport units (eight drivers) may be controlled by the Type 550 Control unit by means of the mark track, which gives format information to the control, and the

program interrupt facility of the PDP-7, -4, or -1. The computer is permitted to do computation in the main program during tape operations. Information is transferred with programmed checking by means of the subroutines supplied, but these routines do not allow simultaneous computation during word transfers since these programs are general purpose and take most of the computer's time for their operations.

USES OF DECTAPE

DECTape is particularly suitable for certain applications. Some of these are covered briefly below.

Storage

The first application is simply as a storage device for programs and data. Since the tape handling is extremely simple, it is easy, and in fact desirable, to store the program on DECTape and simply carry it to the computer when needed. To carry the same amount of data on either cards or paper tape would be unwieldy to say the least. Different library tapes can be changed easily, if necessary, and retrieval of any portion of the tape is relatively fast.

Editing

If modifications to the programs are necessary, the tape need not be either rewritten entirely to preserve the order, or added to at the end. The program can be read in, modified, and rewritten in the same location on the tape if its block length is not changed. This indicates also that many programs can be written utilizing a minimum number of drives.

On-Line System Data Handling

On an on-line system, use of individual DECTapes to store information keyed in by individual users provides a cheap and efficient way of handling data. The ability to multiprogram during searching (which requires, by far, the greatest amount of time) means that more than one individual can have access to the computer without appreciably affecting internal processing, and without causing an inordinate amount of waiting time for the user. An extension of this is discussed in the next application.

Since the DECtape reel is only 3-1/2 inches in diameter, and the system can read or write in both directions, random access to any point on the reel is relatively fast. A fairly large amount of data can be stored, however. For example, one tape can hold more than 28 complete 4K memories. In a real-time, multiple-user, random access system, many tapes can be moving simultaneously even though data can be transferred on only one tape at a time. For example, take a system with several remote Teletypes, each of which requires random access to information stored on several DECtapes. When the first request occurs, the program can place the appropriate tape in search mode and begin searching for the block. If another request occurs, the program can note approximate position of the first tape in relation to the block requested, select the new tape (leaving the old tape moving), and start searching for the new block. A programmed clocking device or timing loop can be used to determine when to reselect the first tape, check for the correct block, and transfer the data. As new inquiries enter the system, a queue can be formed with the request for the nearest information and the time needed to reach it at the top of the queue. As information is found, the clock is reset to the time necessary to reach the next request and so on:

In this way, multiple requests for information on a single tape can be easily handled if both records can be found by searching in the same direction. There are times, of course, when data is reached on more than one tape simultaneously. In this case, the tape searching for the later request can either be stopped before the record is reached or can be turned around if the record has been bypassed. In terms of overall time to the user, very little difference will be noticed. Of course if two separate DECtape controls are used, data can actually be transferred on more than one tape simultaneously, if the program is fast enough to react to the various flags.

Sampling of Data

A fourth type of application involves the continuous movement of the tape. In many instances it is desirable to store sampled data on a tape for future analysis by other programs. Memory fills up rapidly, however; and during the time information is transferred onto the tape, sampling is usually stopped to avoid synchronization problems. Thus, the information stored usually consists of data relating to many relatively short samples. With DECtape, one whole tape can be written with one command, and therefore an extremely long sample of fairly rapid

data can be achieved. If desired, the entire tape can be considered as one long block of information. Storing of information from an analog-to-digital converter would be a logical use of such a system.

SPECIFICATIONS

Listed below are the characteristics of the 550 DECTape Control. All values are approximate.

WORD TRANSFER RATE	One 18-bit word each 200 (± 10) μ sec. Bit rate is constant when moving forward. Although velocity varies slightly, bit density changes serve to maintain a constant bit rate due to the constant rate timing tack. In reverse direction the variation in time between words becomes $\pm 30\%$ depending on location along the tape.
BLOCK SIZE	Arbitrary segments of any length determined by format control tracks.
POWER REQUIREMENTS	115 v, 60 cps, 1.5 amp
WRITE CURRENT	180 ma
READ SIGNAL	5 mv, p-p, minimum

FEATURES

The general features incorporated in the DECTape system are: bidirectional reading and writing; Manchester type polarity sensing; prerecorded mark and timing tracks; pretested subroutines; individually addressable blocks; and in the sense explained elsewhere in this manual, individually addressable words.

Recording Technique

Most of the above features are the result of the type of recording technique used in the system (Manchester, or polarity sensed). Briefly, this technique utilizes a change in magnetic flux for every data bit on the tape. Of importance in this technique is the direction of each flux

change. A "negative-going" change represents a 1; a "positive-going" change is 0. The polarity of the voltage generated by these flux changes is sensed to determine the type of bit written at a particular location on tape. A timing track is recorded on the tape for purposes of strobing the data tracks. The timing strobe is issued to coincide with the maximum rate of change in flux of a data bit, thus at the point of maximum read voltage.

Preprogrammed Subroutines

Information is transferred with programmed checking by means of the subroutines which may be obtained from Digital. There are three types of subroutines currently available. The first is a basic set of subroutines for searching, reading, and writing. The second, called Microtog, is a set of maintenance and diagnostic programs entirely under control of toggle switches on the main computer console. The third, called Microtrieve, is a routine which permits the saving of programs or data on DECTape, with a quick retrieval feature using toggle switches. A more detailed description of these programs is included at the end of Section 4.

FORMAT

DECTape uses a ten track recording head to read and write five duplexed channels. The five tracks actually written consist of the timing track, used to strobe the other tracks; the mark track, used to raise flags in the program, create sequence breaks, detect block mark numbers, and protect control portions of the tape; and three data tracks. An 18-bit word therefore uses six lines of three bits each on the tape.

Tape Skew

Some tape systems strobe on the first bit of a slot, then impose some arbitrary delay after which all signals present are read. This produces problems since differences may occur in the two directions. Variations in tape speed between write time and read time would result in non-compensated changes in the necessary delay. In the DECTape system the redundant heads are placed in a relationship to each other which eliminates most of the cross-talk between the most important tracks. This relationship also places the timing tracks at the edges of the tape so that strobing on the analog sum of the timing track signals guarantees that the data tracks are read when they are in the most favorable position. The data tracks are placed in the middle of the tape where the effect of skew is at a minimum.

The actual mark track, which is written on the tape (see Figure 2) was selected after careful consideration and provides many functions not readily discernible at a casual glance. Some of these are listed below

Program synchronization

Block end detection

Error checking and prevention

Protection of control information

Block and word addressability

Automatic bidirectional compatibility

End of tape detection

Variable block format

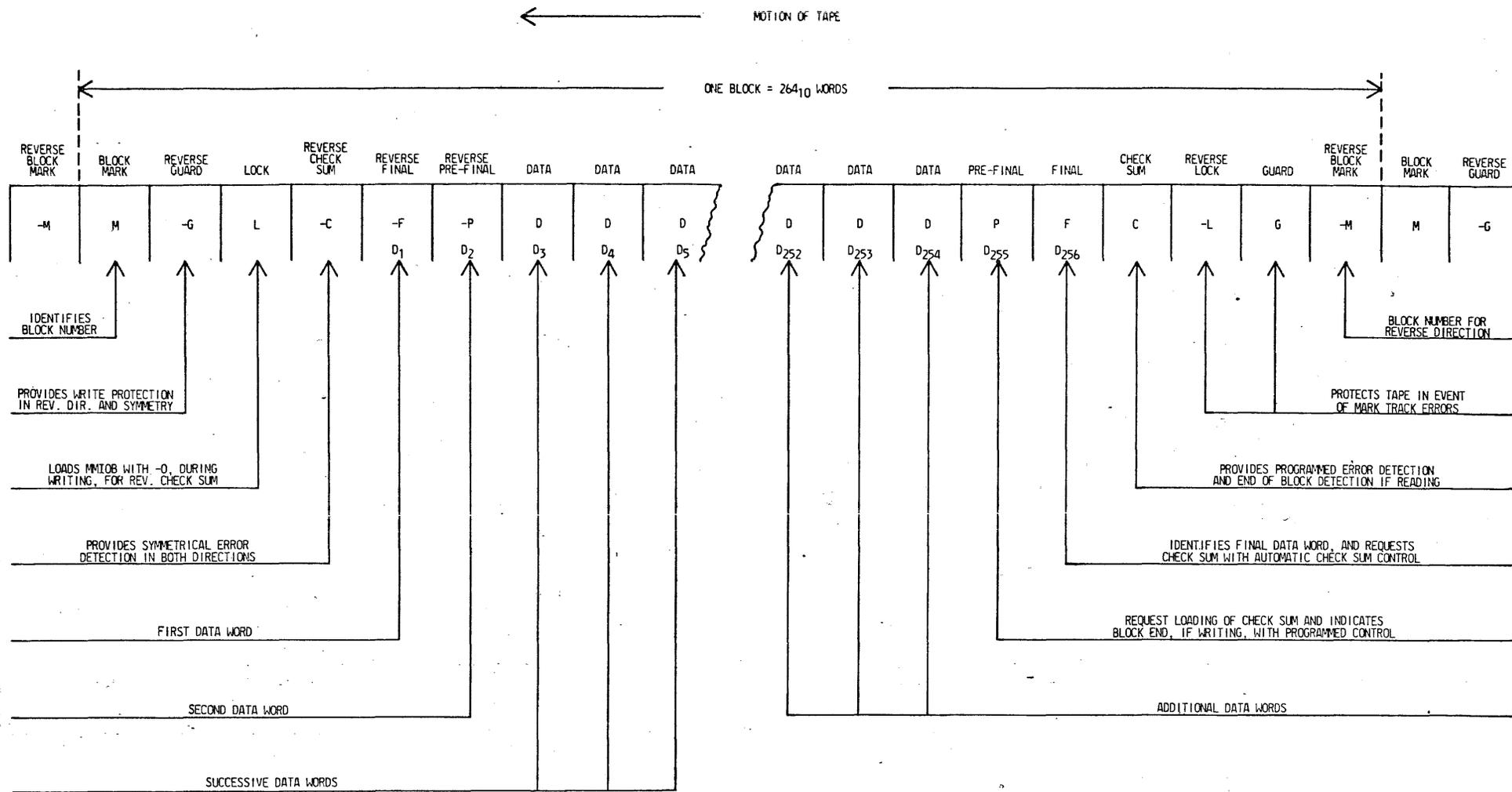
Inclusion of marks to allow expansion for more automatic systems of the future.

For complete understanding of the questions of program synchronization and block end detection, Figures 2 through 6 should be studied closely, using the explanation which follows to clarify certain main points.

Modes of Operation

There are three main programmed modes of operation which require that the user either provide information to the DECTape system or accept information from the DECTape system. These are the search, read, and write modes. A fourth mode, move simply moves the tape without supplying or requesting information. In order to indicate to the programmer that the system is ready to transfer information, certain flags are raised. When these occur, the programmer must either load new information to be written, or unload information just read, and must do so within a specified time to prevent loss of information and error indications. If the program interrupt mode is being used, the raising of any of the flags mentioned also causes a break in which the individual flags must be interrogated.

In order to produce these flags, the mark track is read by passing the bits through an 8-bit "moving window" which shifts bit by bit as the tape moves. A decoder associated with the window interprets the pattern present, and raises the appropriate flags, if necessary. An 8-bit window is used, even though each mark is six bits long, to provide greater reliability, since



NOTE: END MARKS WHICH IDENTIFY THE PHYSICAL ENDS OF THE TAPE, ARE THE ONLY MARKS NOT SHOWN.

Figure 2 DECtape Mark Track Format
(Assumes 256₁₀ Data Words Per Block)

a mark will not be recognized as legitimate unless the last two bits of the previous mark were legitimate. This is one of the reasons which requires ordering of the marks on the tape. Note that whether the program is reading or writing, the mark and timing tracks are always being read.

Search Mode

In the search mode the data flag is raised only when a block mark is read (see Figure 3). The program must unload the buffer within 53 msec, and bits 6-17 contain the block mark number.

Write Mode

In write mode, the DECtape system automatically writes the reverse check sum and raises data flags when it requires information to be written on the tape (see Figure 5). The first data flag requests the first data word of the block, and the last data flag requests the last data word of the block; therefore there are a total of 256 data flags for a 256 word block. Note that the program loads each data word as the DECtape system is writing the previous one; thus a flag is raised requesting a data word when it has just passed the place on the tape two words ahead of where the word is to be written. Compare this with read mode discussed below. Time between data flags is approximately 200 μ sec. When the prefinal mark is detected, a block-end flag is raised which accomplishes two things. First it is a request for the program to load the calculated check sum (normally the complement of the 18-bit ring sum of the reverse check sum and the data words); and second, it allows the program to detect that a block has been completed without the use of any programmed counters. After the check sum is written, the writers are turned off to avoid any possibility of destroying the control portion of the block. Approximately 1.2 msec are available to switch to search mode if a check of the next block mark number is desired. If the control remains in write mode, the DECtape system writes the next reverse check sum and raises the next data flag after approximately 1.6 msec.

Read Mode

In the read mode the first data flag is raised when the reverse check sum has been read (see Figure 4). The reason for this becomes obvious since a block may be read in either direction independent of the direction in which it may have been written. The first word read, therefore,

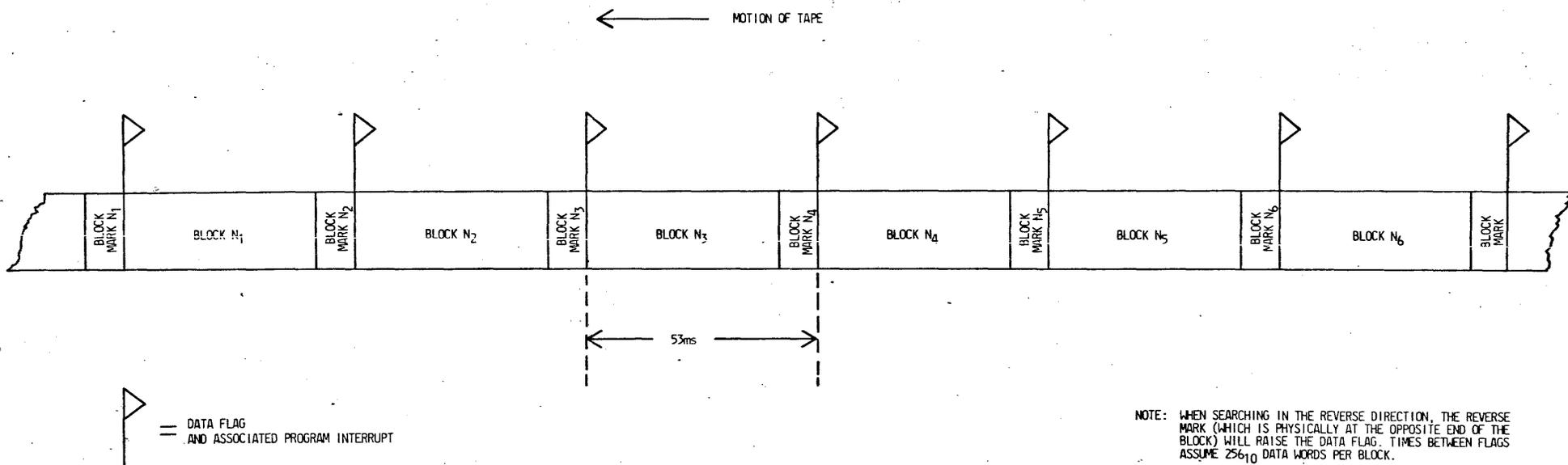
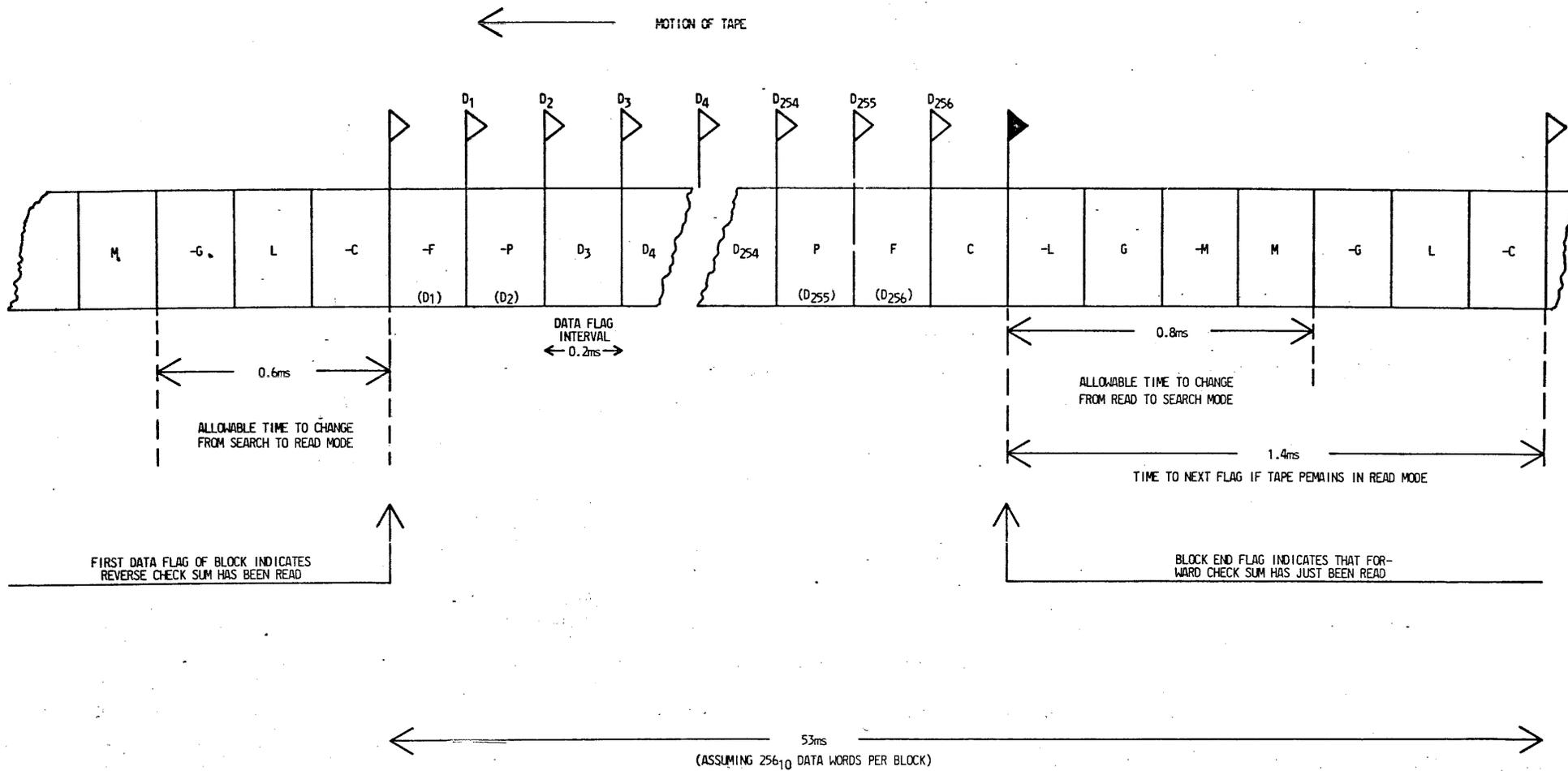


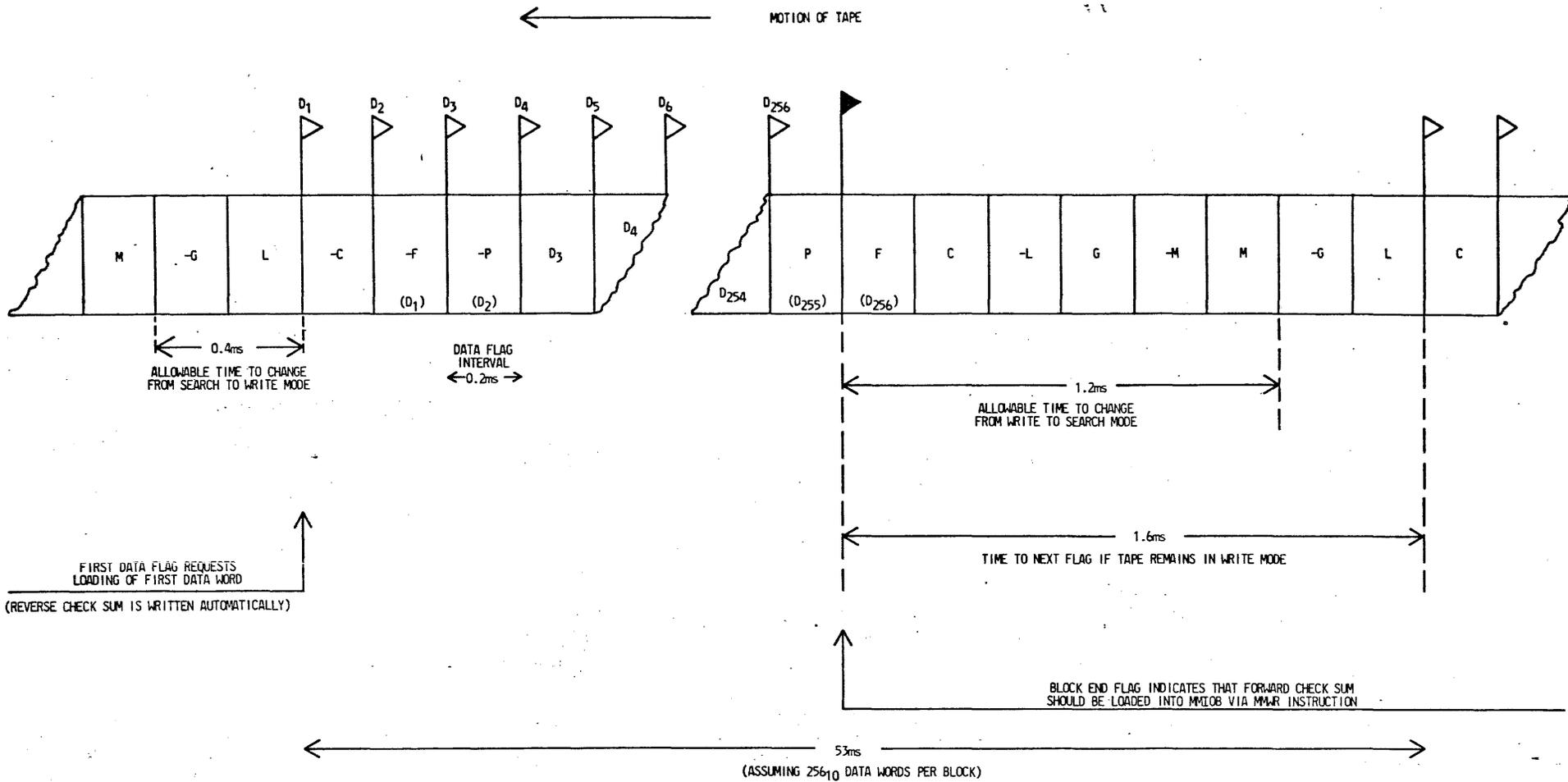
Figure 3 Flag Raising, Search Mode



- = DATA FLAG AND ASSOCIATED PROGRAM INTERRUPT (NUMBERS OVER FLAGS INDICATE NUMBER OF DATA WORD JUST READ INTO MMIOB)
- = BLOCK END FLAG AND ASSOCIATED PROGRAM INTERRUPT

NOTE: FLAGS ARE SYMMETRICAL IF READING IN THE REVERSE DIRECTION.

Figure 4 Flag Raising — Read Mode



- = DATA FLAG AND ASSOCIATED PROGRAM INTERRUPT (NUMBERS OVER FLAG INDICATE NUMBER OF DATA WORD WHICH MUST BE LOADED INTO MMIOB)
- = BLOCK END FLAG AND ASSOCIATED PROGRAM INTERRUPT

NOTE: FLAGS ARE SYMMETRICAL IF WRITING IN THE REVERSE DIRECTION.

Figure 5 Flag Raising — Write Mode

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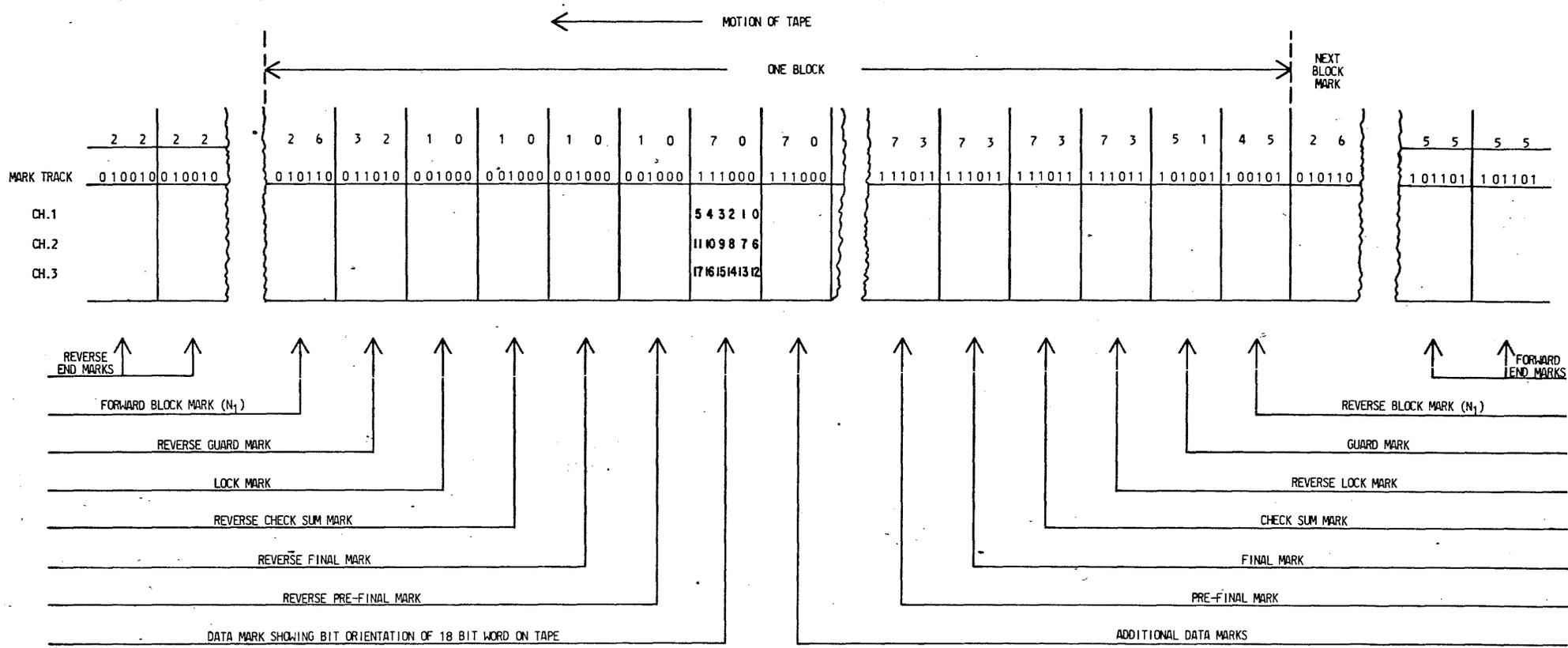


Figure 6 Mark and Information Track Bit Format

of the window or if a legitimate mark is not found after each six shifts of the window. These combinations of checks make it virtually impossible to misinterpret the mark track and thereby destroy information.

Nothing in the system prohibits the changing of modes at any time during the movement of the tape. However, care should be taken to include the difference in counting words when switching from read to write or from write to read, the recovery of the read amplifiers after writing (about two word times), and the fact that writing in various locations in the block invalidates the check sum at end of the block. Within those limits almost any combination of modes can be used; and because of the polarity sensed recording technique, even individual words can be replaced.

Complement Obverses

One other unique feature of the mark track is that the six control marks before the data marks are "complement obverses" of the six control marks after the data marks. The complement obverse of a word is defined as the complement of a word with the bits read in the reverse direction, for example:

010110 (26) and 100101 (45)
001000 (10) and 111011 (73)

The data mark is the complement obverse of itself. When reading in the reverse direction, the flux reversals on the tape are opposite to those when reading forward and the bits are read in the reverse order. Therefore, the mark track window sees exactly the same thing in both directions.

Bidirectional Ability

With one exception, no special logic is required to distinguish the format of the tape in either direction. The one exception involves the shifting of information into the DECTape buffer. Since the assembling of the 18-bit word is done by the hardware, it is necessary to shift the buffer in opposite directions for opposite movement of the tape in order to present words to the computer as they were originally written. This means that if a record is read opposite to the way in which it was written, each 18-bit word appears in the buffer exactly as it originally appeared in memory; however, the last word written would be the first one read, etc.

The end marks on either end of the tape illustrate this bidirectional ability even better. As the end marks are complement obverses of each other, only recognized is that end of tape which will physically come off the reel if further movement continues. Again, no special hardware is needed for opposite ends of the tape, and there is no harm in coasting into or turning around in the end zones. Errors are indicated only if attempting to go further into the end zone. The particular bit structure of the end marks is a repetitive one, so that any shift of three bits in the window appears as another end mark. This makes it virtually impossible to pull the tape off the reel in any of the normal modes. Sensing of the appropriate end mark stops the tape and raises the error flag if the tape is in any of the normal modes.

There are only two "abnormal" modes. One is the write timing and mark track mode, mentioned previously, in which no marks can be detected since they are being written. The other is the case where a tape has been left moving but not connected to the control (deselected). In this case, only the marks on the actually selected tape are recognized. In only these two circumstances can the tape be pulled off the reel.

Block Size

Although the blocks are structurally alike in terms of the types of marks on the mark track, they need not contain the same number of data words. Indeed every block on the tape can be of different length, if such a format was created originally. The system will operate in the manner outlined no matter what the length of the block. One other feature exists which may prove useful, especially in the future designs. If for any reason the distance between blocks must be lengthened, it can be done simply by adding "01" codes between the reverse block mark of block N and the forward mark of block N+1 (see Figure 6). Since the pattern "01010101" already appears at the junction of the two marks, it may be continued indefinitely without harm.

PERTINENT DOCUMENTS

Publications

The following documents serve as source material and complement the information in this manual. These publications may be obtained from the nearest Digital office or from:

Customer Relations Department
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts

Digital Module Catalog, C-1105 contains information pertaining to the function and specifications for the basic modules and accessories comprising the DECTape Control Type 550.

DECTape brochure, F-03-550 presents a general description of the DECTape system.

PDP-4 Reference Manual, F-75 contains programming information pertinent to DECTape when used with a PDP-7

PDP-4 Handbook, F-45A gives programming information for DECTape used with the PDP-4.

PDP-1 Handbook, F-15D gives basic IOT programming information.

Library Programs

The following programming brochures are available now and may be ordered from the Digital Program Library at the address given above.

PDP-4/7 Programs

Microtrieve, 4-29-IO allows the programmer to save areas of memory on DECTape and quickly retrieve such information using the toggle switches on the PDP-4/7.

Microtog, 4-46-IO describes various programs to detect any errors in the DECTape control.

DECTape Subroutines, 4-45-IO are programs which allow the programmer to read, write, or search the DECTape using prewritten and tested subroutines.

PDP-1 Programs

DECtape Control PGM, 1-26-IO is a subroutine which transfers data to or from DECTape.

DECtape Format Pack, 1-127-IO writes the mark track, timing track, and block numbers from 0 to 1077₈ on tape. It also allows the operator to check the tape after it is written.

Data Transfer Test, 1-128-IO enables the operator to check data transfer to and from the computer and the DECTape control. This program also indicates which flags are being detected during the test.

DECtape Rocker Program, 1-129-IO allows the user to oscillate tape over a desired area for debugging purposes.

DECtape Exerciser, 1-130-IO evaluates the performance of DECTape and determines the nature of any errors that might occur.

DECtape Dump and Retrieve, 1-130-IO allows the operator to store data on DECTape or retrieve data from DECTape using the TEST WORD switches.

Error Message, 1-132-IO functions with a DECTape control to type out errors on the on-line typewriter.

SECTION 2

THEORY OF OPERATION

ENGINEERING DRAWINGS

All the DECTape prints are fully cross referenced. The numbers shown at the inputs or outputs of the logic blocks on the block diagram refer to the block schematic print numbers and geographical references as follows: The first two characters (EM, IN, C2, C1, etc.) indicate the mnemonic title of the appropriate block schematic, and the second two characters (B4, C2, etc.) indicate to which zone on the print the reference is made. The letter indicates the vertical dimension, which is shown on the right and left hand margins; and the number indicates the horizontal direction, which is shown across the top or across the bottom. The destinations (or origins) of all signals are shown within the block schematics. If a given signal goes two places, both at the same geometrical print location, this location is indicated twice. In this way a section of the wiring list can be built up for purposes of detailed troubleshooting or corrections to the hardware. Wiring lists are not maintained once the machinery is shipped. Refer to Appendix 1 for a detailed explanation of DEC symbology as well as reduced copies of the engineering drawings.

DECTAPE SYSTEM

The basic block diagram of the DECTape system is shown in D-550-0-BD. At the top of this diagram, a horizontal line representing information and control plugs 0J1 and 0J2 serves to separate the computer (above) from the DECTape system (below). Another horizontal line located at the bottom of the diagram, representing the information bus plugs at C21, 22 and the control bus at B3, 4, serves to separate the tape drive mechanism (below) from the control system above it. The purpose of this diagram is to depict the inter-relationship of major signals utilized in the DECTape system. Some of these signals are shown as input-output transfers (IOT's). These are located at the top of the diagram, and are designated as being relevant to either the PDP-1 or PDP-4/7 computer. Input-output transfers without such designations are common to both computers. Thus, the IOT MMRD as shown is common to both computers; whereas the IOT MMEF is relevant only to the PDP-4/7.

Data Transfers

Information transfers are routed to or from the accumulator (AC) if a PDP-4/7 is used, or to or from the input-output buffer (I/O) if a PDP-1 is used.

Data transfers between computer and tape are via the in-out register and the shift register in the control unit, as shown at the left of the diagram (D-550-0-BD). From the AC or I/O of the computer, information flows to the tape through 18 lines which connect the AC or I/O to the in-out register. These lines are one-directional only; a binary 1 is indicated by a ground on a line.

Information from the tape is forwarded to the AC or I/O from the in-out register of the control unit by means of another set of 18 lines; a 1 is indicated by -3 on a line.

A transfer of information between the in-out register of the control unit and the shift register is accomplished by a double set of 18 lines. Information flow between these registers is accomplished by simultaneously pulsing their in gates by means of an interchange pulse. During writing, the contents of the shift register are transferred to the tape through the write amplifiers and tape heads; during reading, information is transferred from the tape through the read amplifiers to the shift register. A detailed discussion of the shift register, in-out register, and read and write amplifiers is included later in this section.

CONTROL FUNCTIONS

The basic control functions of the control unit are listed below. The titles of the block schematics which contain the indicated circuitry are shown in parentheses.

Reading of timing track. The bits on the timing track are read and transformed into timing pulses which control the sequence of DECTape operation. (TM).

Reading of mark track. The mark track is read and decoded to obtain flag signals, sequence breaks, mark numbers, and block ends. (W).

Transfer of information. Signals are generated to denote the direction of information exchange between the computer and DECTape. Information to or from the computer is transferred in parallel form; information to or from the tape itself is transferred in serial form (IN).

Generation of control responses. The timing pulses (TP), the marks, and the mode of operation (read, write, search, etc.) are used to generate proper control responses (flags, shift signals, interchange pulses, etc.). (C62, TM). Memory of mode, selection, and motion commands of the program are shown in (C1).

Reading of Timing Track

The basic timing pulses (TP1 and TP0) are derived from the timing tracks of the tape. Refer to the TM print. TP1 is generated during the negative-going zero-crossings of the timing track voltages picked up by the tape head, and TP0 is generated from the positive-going zero-crossings. Tape head voltages appear as sign waves. The zero-crossings of the voltages picked up by the head are transformed by the read amplifier of the 4523 module into square waves, the transitions of which occur in synchronism with the zero-crossings of the original head voltages. The read amplifiers, which have high and uncontrolled gain, saturate at any input signal over $100\mu\text{v}$, p-p.

Timing pulse TP1 marks the time the change in direction of flux of the data or mark bits is at maximum, and therefore ready for transfer to storage registers. During writing it is used to write the flux reverse which represents the bit. Timing pulse TP0 denotes between-bit time, i.e., the appropriate time to shift into the writers the next bits that are to be written. In effect, TP0 designates the time that the head is passing through the boundary region between bit locations on the tape.

Another timing pulse designated as TP2 is obtained by delaying TP1 approximately $4.5\ \mu\text{sec}$. TP2 is used to check mark track information picked up by the TP1 preceding it. The time interval between TP1 and TP2 is sufficient to allow the CD gates to set up. In effect, TP2 commands an inspection of the control word (if any). TP0 is sometimes used to accomplish the same thing.

Relay Timing and Mark Signal

The relay timing and mark signal (RELTM) functions to suppress timing pulses picked up from the tape during this mode of operation. In addition, the RELTM signal enables the timing and mark track writers and physically connects them to the TT and MT. It also starts the WRTM (write timing and mark MODE) clock. In addition to the above, the RELTM signal lights a red lamp on the drivers.

Figure 2-1 Method of Writing on DECtape

2-4

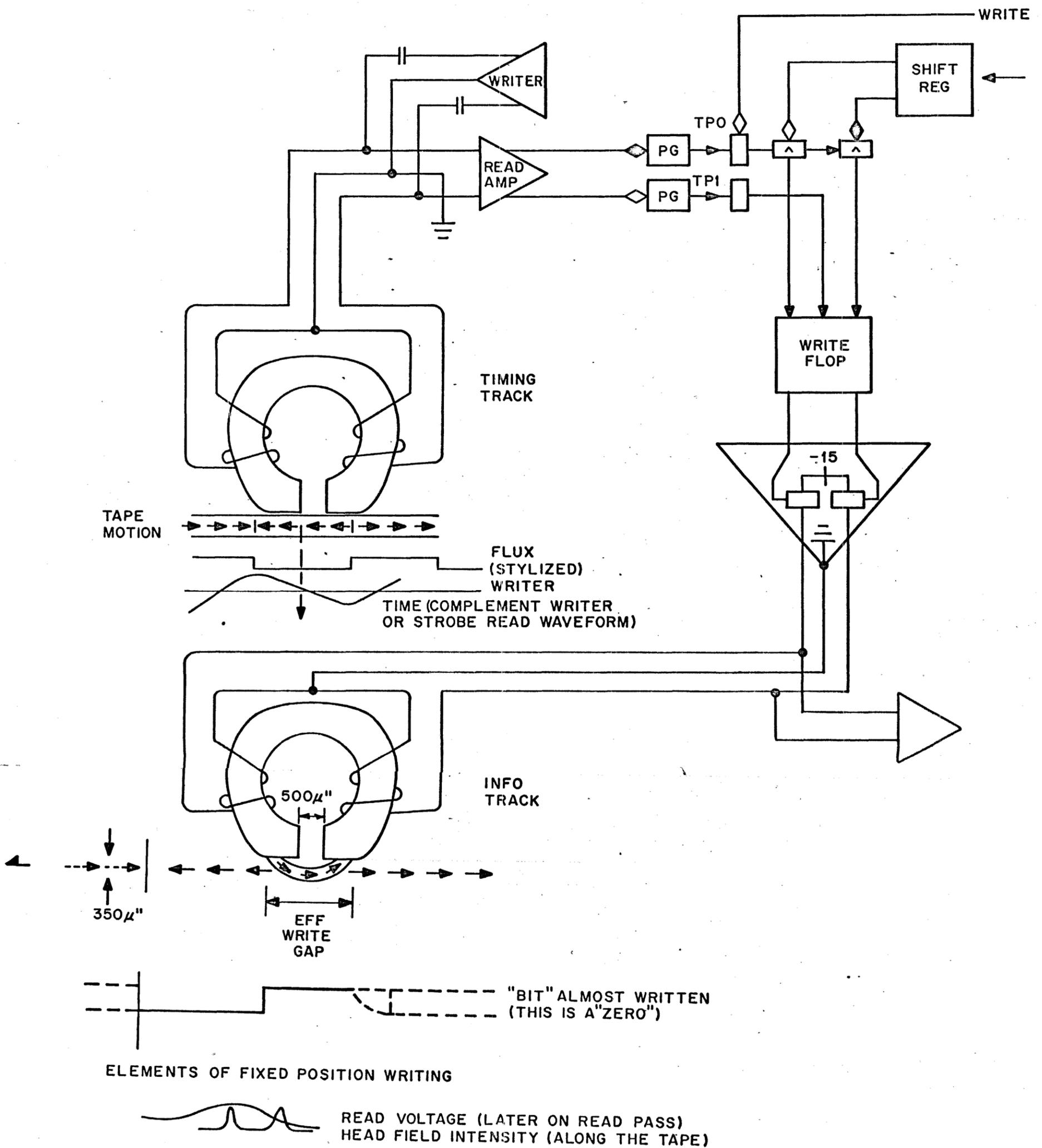


Fig 2-1 D. 2-4

Figure 2-1 shows the physical position of the heads at time T after a timing track voltage zero crossing has passed under center of the TT read head, eg., the zero crossing produced a TP1 which complemented the writer. The field around the head has just completed switching and the bit just written will be centered under the zero crossing if the tape has moved 1/2 of an effective write gap in the time T taken to complete the switch of the head.

The clock mentioned in the paragraph above drives a gray code counter which, in turn, drives the track writers and generates quadrature phase TP pulses by means of the same pulse amplifiers which normally buffer the timing pulses. It should be noted that the TT writers are switches at times which are in quadrature with the timing pulses. This ensures the preservation of the relationship between the negative-going, zero-crossing of a timing signal and the coincidence of the flux reversal of the data or mark bit.

Reading the Mark Track

The mark track is read in the same manner as are the information or data tracks. That is, timing pulse TP1 loads the first flip-flop of a shift register from the (push-pull) outputs of the read amplifier. This occurs at the time of maximum flux reversal of a data or mark bit passing under the head. This same flux reversal was previously written on the tape during an earlier writing operation by means of the same TP1. Since the head senses maximum flux reversal at TP1, an accurate output is obtained from the associated read amplifier. The direction of the flux change determines the polarity of the read amplifier output, hence the kind of bit being read 1 or 0. Figure 2-2 shows the relationship between flux directions and binary value as recorded on the tape.

Unlike the data words, which are routed as described above between tape and computer, the mark track bits are routed only to the control unit. In the control unit, the mark track bits are shifted into the window register. This 8-bit register always holds the last eight bits read from the mark track. Each new reading of a new mark track bit shifts the register so that the new bit is shifted in, and the old eighth bit shifted out. Since mark track bits are read in succession, there is a succession of shiftings of the window register. After each shift, however, the window register accurately reflects the last eight bits read from the mark track.

Note that time displacement, \mathcal{T} , indicated does not result in a displacement of bits since the bit is "written" at the trailing edge of gap and "read" at the center of the gap. The physical displacement (LAG) tends to cancel the effect of time displacement (LAG).

Figure 2-2 Writing

Window Register

The outputs of the flip-flops of the window register are fed to a group of AND circuits. Refer to print W. The function of these latter circuits is to detect particular patterns as they appear in the register. Any particular pattern of bits in the register remains the same only for a period

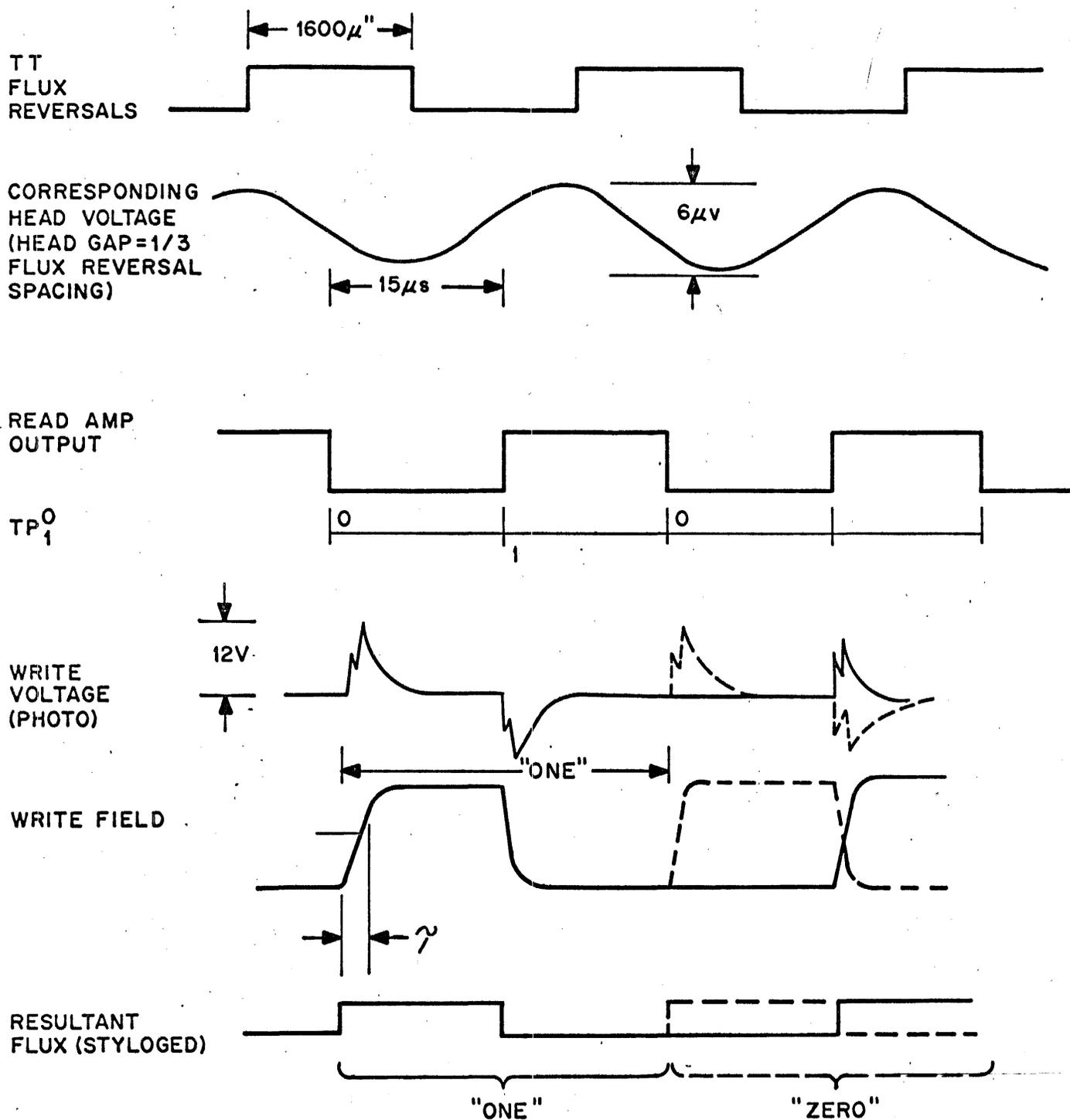


Figure 2-2 p-2-6

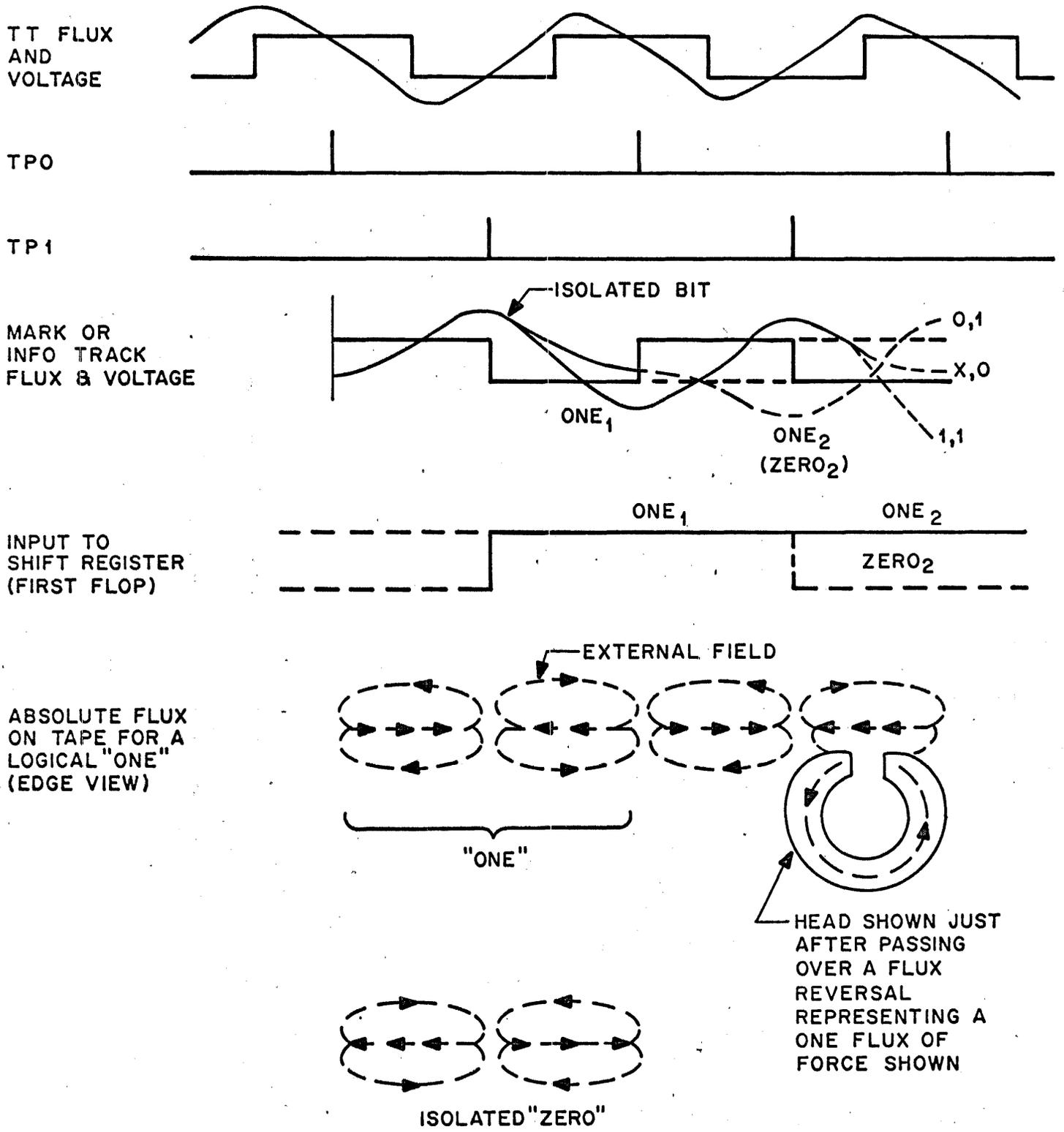
TITLE WRITING
 FIG. NO. 9
 JOB NO. 599-105217 DATE 2/5/65
 DYN BY Joel White CHKD BY _____

8090

FIGURE 4 WRITING

of approximately 33 μ sec; at the end of this time, the next TP1 pulse shifts the register to create (possibly) a new pattern. Accordingly, the AND circuit outputs can be asserted only for 33 μ sec. Thus, after the mark track heads read into the window register a particular pattern as created by the last bit read, the AND circuits, fed by the register, are allotted a time interval of 33 μ sec in which to recognize the pattern and produce the appropriate responses.

Figure 2-3 Reading



7.UG
 FIG. NO. 10
 DATE 2/5/65
 CHKD BY

Figure 2-7 p.2-7

80%

FIGURE READING

The AND circuits are comprised of diodes which drive inverters. The circuits are arranged so that any particular inverter output is at ground whenever its associated flip-flop in the register is enabled. (During the writing of timing and mark tracks, the RELTM signal is used to inhibit the shifting of the window register to prevent the accidental detection of marks during this process.)

Although referred to as an 8-bit register above, the window register stores a ninth bit which, although not part of the pattern fed into the AND gates, serves to control the accurate reading of marks during starting or when switching to a running transport. Bit 9 is set into the register on a shift pulse only if bit 8 is a 1. Bit 9 is cleared by the clear window pulse, which clears all other flip-flops in the register. When not present, bit 9 prohibits operation of the AND circuits into which the window register feeds. When present, bit 9 enables these circuits.

The importance of bit 9 resides in its power to prohibit the reading of mark track patterns until the proper conditions are met. Thus, at the start of the mark track reading process, after clearing of the window register, a one from the mark track must be shifted through the window register, to position nine in the register in order that a pattern (bit arrangement) in the register may be detected by the AND circuitry mentioned above. In this way, bit 9 prevents partial patterns from being erroneously detected. (Other circuits also function to prevent erroneous detection; these circuits clear the entire window register when activated.)

The patterns or bit arrangements presented by the window register to the AND gates for detection are six bits long. The window register itself holds eight bits. The ninth bit, although forming a part of the register, is in no way utilized by it in the pattern detection process. Because of this circuit configuration, the window register is capable of providing 8-bit patterns; the order of code patterns is fixed in the shift register patterns. The 8-bit pattern capability utilizes the last two bits of the preceding pattern.

MSY Register

The window register and the associated decoding circuitry do not completely decode the mark track patterns. To achieve complete decoding, the MSY register circuit is used. The function of this MSY register is to decode the four blockstart marks (LOCK, REV CHECK, D1, and D2), and the four block end marks (prefinal, final, check, and spare).

The MSY register is loaded when a block mark is detected. Loading of a MSY register consists of inserting the binary arrangement 1000 into the register. Each time a block start mark is detected, a shift in the MSY register occurs. This shift causes the initial 1 to travel down through the register as other ones follow it. Thus, the first shift would cause the register to read 1000; the second, 1100; the third, 1110; and the fourth, 1111. The MSY register states are ANDed with detected block start marks to obtain the initial four marks mentioned above.

The four block-end marks also cause four shifts of the MSY register. However, zeros rather than ones are propagated or shifted down the register. In this case, the initial state of the register is 1111. At the first shift, the state of the register is 0111; at the second, 0011; the third, 0001; and the fourth, 0000. This last, or fourth, state is decoded during troubleshooting procedures.

The shifting of the MSY register occurs at TP2. The block start and block end marks are detected between one TP1 and the next. As a consequence of this, the useful output of the mark detection circuitry considered as a whole occurs at TP2.

Writing the Mark Channel

Mark track words furnished by the computer are written on the mark track of the tape when the DECtape system is in the RELTM mode. The WRTM command (a result of the computer-issued MMLC instruction) must also be issued to effect mark track writing. Normally, the writing of the mark track is initiated when the DECtape system is in the stop condition. This permits the delay inherent in start up, at which time the DIP signal is effective, to render the timing pulses from the local clock ineffective. In this way, flags normally raised by the timing pulses are kept absent.

Word Counter

After start up, data flags are raised automatically at each word time. These flags are raised by the EK (or word counter) circuit. This circuit consists of a ring arrangement of six flip-flops in which a single one is caused to circulate. At the issuance of each data flag, the computer loads the word to be written on the mark track into the IOB. The word remains in the IOB until issuance of the next flag request, at which time the word is shifted into the shift register. From

the shift register it is transferred through the write amplifiers and tape heads to the mark track. Since the shift register is logically divided into three sections, the writing of a mark channel is accompanied by an identical writing of data channel number one.

Mark Track Errors

Mark track errors are detected, if present, as follows. There are specific marks which occur each sixth time the window register is shifted. By using these specific marks, an error check procedure based on verifying the passage of six timing pulses between each such specific mark is effected. Utilized for this procedure is the EK (word counter) used also in the mark track writing process.

The EK is present at the same time that a block mark is detected (at TP2). The EK is rotated by TPO's. After six such rotations, caused by six successive TPO's, the EK is returned to its initial condition. As each initial position is reached, a new specific block mark should also be present. Thus, assuming no error, the initial condition of the EK and the detection of a specific block mark should exist concurrently. Should the two not exist concurrently, an error has occurred.

Since the EK is shifted at TPO, and since the window register is shifted at TP1, the concurrency of the initial state of the EK and the existence of the specific block mark are valid only after TP1 is issued and only before the following TPO is issued. Because of this, the concurrency is checked, or strobed (since it is in gate form) at TP2.

It should be noted that there are particular times during DECTape operation when any error checking procedure is superfluous. For instance, during search, errors obtained from portions of the tape not yet read or written are irrelevant. Similarly, in the WRTM mode and the MOVE any MTE is also irrelevant.

For the above reasons, the negative (for error) output of the error detecting circuitry is clamped to ground and rendered inoperative unless a particular mode such as write, read, write all, or read all, unclamps it.

Figure 2-4 EK Waveforms

Indications resembling errors, but not errors as such, are eliminated by clearing the window register during their "presence." In this respect, the two areas on the mark track located near the block mark errors are suppressed.

During the interval of time which elapses between the start of tape operation and the attainment of proper tape speed, the synchronization signals for the EK are nonexistent. Thus, error-detection cannot be performed. The BMF flag is set by the block mark and is used to gate out MTE's detected during this period. The tape system, when in this condition, would normally be in the search mode, rendering error detection superfluous, as described above. However, when in this condition, the tape system may be in the read mode. The BMF flag is then cleared by the clear window pulses.

Transfer of Information

In addition to furnishing information for, or receiving information from, the tape, the AC or I/O can also forward a portion of its contents to the control unit for purposes of control only.

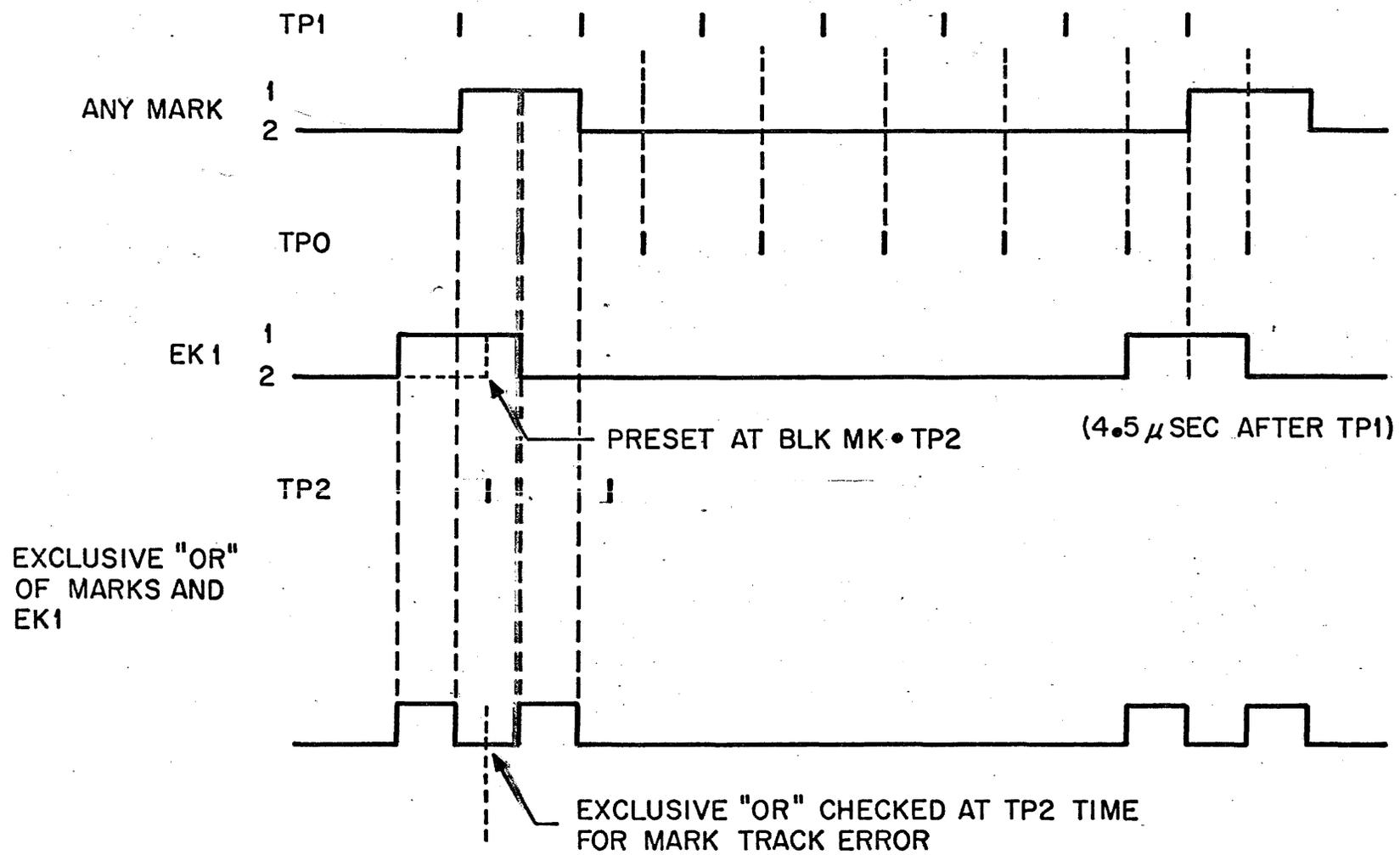


Figure 2-1 8-2-11

By means of IOT instructions, the computer is able to select a tape unit (1 out of a possible 8 plus zero, or no unit), direct the motion of the tape, and command one of several possible modes. The selection of a tape unit is controlled by the arrangement of bits 2 through 5 in the AC or I/O. These bits are loaded into the selection register by the MMSE instruction. A ground on any of these lines indicates a binary 1.

Load Control Instruction

The MMLC instruction, or load control instruction, is formed by the arrangement of bits 12 through 17 in the AC or I/O. These bits are transferred by means of six lines to the command logic circuitry and the motion control circuitry. This circuitry then translates the bit arrangement into a specific tape direction and a specific equipment mode (move, search, read, write, WRTM, read all, write all, and readin mode). A ground on any of these six lines represents a binary 1. There are eight possible modes which can be commanded by the command to the logic circuitry.

Timing Pulses and Mark Track Information

Like the accumulator or I/O, the tape can furnish information to the control unit for control purposes only. This information comes from the mark and timing tracks and is not passed through to the computer as data information. Instead, it is routed to the timing pulse generator circuitry and mark detection network (and window register). The information so routed consists of the timing pulses and mark track information derived from the tape.

The timing bits from the tape are picked up from the bus which is connected to a particular timing track head by the selection circuits, fed through a read amplifier and forwarded to the timing pulse generator. This generates three timing pulses: TP1, TP2, and TP0. These timing pulses are forwarded to other circuits in the control unit.

Mark track information, picked up by the mark track heads, is forwarded to the mark detection network circuitry. In accordance with the information received, the mark detection network circuitry issues signals signifying that one of the various mark codes written on the mark track has just passed over the head.

Operating in conjunction with the timing pulse generator is the WRTM clock circuitry. The purpose of this circuitry is to write timing track information on the tape. Information is forwarded from the clock to the tape through a write amplifier.

Read Status Instruction

The DECTape control unit transfers nondata information into the AC or I/O by means of the MMRS instruction. Although the bits constituting this instruction are temporarily stored in the AC or I/O, they do not represent any part of the data work or words. As shown on the overall block diagram (D-550-0-BD), the six leads composing the MMRS consist of REV, GO, UNABLE MK TK ERROR, MISS, and END. The MMRS command also reads the three flag levels into bits 0-2.

Flags

Another major group of signal leads of importance in DECTape system operation are those generated by the flag response net circuitry. This circuit issues to the computer the data flag, block end flag, and error flag signals. In the PDP-4/7, these signals are used to produce a program break request, enable the skip logic, and are sent to the AC on a MMRS.

In the PDP-1, the data flag signal (MMDF) is an indication to the computer that a particular data word being read or written is assembled and ready for transfer. The block-end flag (MMBF) indicates to the computer to unload the check sum if reading, or to load the calculated check sum if writing—indications to which the computer can respond by issuing a MMRD instruction or a MMWR instruction. An error flag (MMEF) indicates to the computer that one of four error conditions has occurred; accompanying this error flag signal is the MMRS format (described above) stipulating the type of error responsible for issuance of error flag.

Generation of Control Responses

In general, the timing relationships between the computer and the DECTape system are governed by the ordinary program break control function. That is, the computer selects the mode of DECTape system operation by furnishing it with a MMLC instruction; this instruction directs the DECTape system to search, read, or write. The DECTape system, in accordance with mode

generates the flags appropriate to the mode. The generation of flags and other responses continues until the tape is stopped by command, the mode is changed, or the tape end is reached.

The DECTape system control is in large part based on actions caused by reading of the mark track. These actions consist in the main of the initiating flag signals. A block mark is detected each time the tape heads encounter the boundary between data words. Depending upon the type of mark detected, and the mode of operation, a flag signal is issued. For example, in the search mode, the data flag is issued if the block mark is detected at TP2. The block mark and the TP2 signal and its attendant flag cause issuance of the interchange pulse, which shifts data between the shift register and the in-out register.

Searching

In the search mode, block number codes as read from the tape are forwarded to the computer for comparison purposes. Such forwarding is accomplished by means of the interchange pulses which transfer the block number codes from tape to the in-out register. During search, such transfers occur every 53 msec (for a 256-word block). Each block number code so transferred is accompanied by the data flag. Should the computer fail to recognize the data flag before the next raise data flag pulse is issued, an error flag signal is issued. This flag signal is generated by a CD gate which has as inputs the RDF signal and DF signal. The output of this gate sets the miss flip-flop to the 1 state. The encountering of an end mark automatically sets the END flip-flop, and the GO flip-flop is reset, stopping the tape.

Writing

The commanding of the write mode by the computer results in the issuance of a data flag by the control unit to the computer. The purpose of this flag is to indicate to the computer that the in-out register is prepared to accept a word from the computer for writing on the tape. The computer then transfers the word to be written to the in-out register by means of a MMWR command. The MMWR command extinguishes the data flag. (The WDA level results from a ORing of the block start and data marks. This level appears when the write data flags are to be raised.) During write, after the computer has transferred a word into the in-out register, the word is then interchanged and shifted. This process requires between 140 and 480 μ sec, depending on speed and program timing. During this time, neither the stop mode nor the read mode can be commanded.

Should the computer direct the writing of information exceeding a block length, the DECtape system responds by shifting to the reading mode (in the block end area), writing the reverse check sum, and raising the first flags; the DECtape system then reverts to the write mode and utilizes TPO's for shifting purposes in writing.

Since the command to stop writing is inhibited in the boundary region between the last data word and the check sum, any read command given during this time is temporarily held in abeyance. At the raising of the block flag (read mode), a minimum delay of 240 additional μsec is necessary in order that a stop command be carried out.

Reading

Entry into the read mode is accompanied by the issuance of data flags signifying readiness of words for transfer to the computer. The data flags are generated by the RDA signals and the TP2 pulses. The RDA signals, in turn, are generated by the OR formed by combining the third and fourth block start marks, data mark, prefinal, and final signals.

Data flags are lowered by the computer-issued MMRD signals. The MMRD signal strobes the word in the in-out register into the computer.

Switching from Write to Read Mode

In the read mode, any switching to the write mode within a particular block cause the following to occur. The data flag (read mode), signifying the readiness of the word in the in-out register for transfer to the computer, is lowered by an MMRD. Assuming an MMLC (write) is issued just prior to the transfer, the first word to be written in the new write mode is written in the third word space following the word space from which the last word was read. Switching from read to write within a block necessitates the loss of two word spaces, which are neither written into nor read from. The first data flag raised after the switchover indicates that the last word read has been transferred to the computer, and that the second word to be written can be released by the computer.

There is an exception to the above: if the first word to be written after switchover occupies the last data word space in the block, an RBF is raised. Also, if the first word so written falls into the check sum word space, no flag is immediately raised; instead the next flag is issued at the start of the next block.

Any switching from write to read occurs in the boundary region following the last word loaded for writing. In this boundary region, a dummy flag signal is issued. However, this flag signal corresponds to no special action; this flag is lowered when the first flag for read is raised. Because of the switchover, no validity check of the first three or four words read is possible.

Selection (Refer to print C1)

Complementary inputs formed via inverters tied to AC bits (or I/O) 2 through 5 are connected to the CD gate level inputs of four Type 4218 Flip-Flops. The CD gate pulse input is generated by a select command from the computer (see DECtape Instruction List).

This instruction code loads the contents of the AC into the 4218 Flip-Flops. A 4671 Octal to Decimal Decoder then decodes the FF outputs and pulls the example selected line to approximately -3v from a more negative voltage. The selection lines are connected to a selection relay located in the 555 Transport, one side of which is tied to -15vdc. Selecting a transport connects the motion control and data bus from the 550 Control to the selected transport.

Motion Control (Refer to print C1)

Complementary inputs are formed via inverters tied to AC bits 12 and 13. The outputs from the inverter on AC bit 12 are tied to CD gates wired to the GO flip-flop. These same lines are combined with the complementary ACB13 input through two negative AND gates. The AND gates enable the CD gate set input to the Rev flip-flop and are provided to inhibit a change of direction command at the same time a stop command is given.

The GO and REV flip-flops are used directly for control functions as well as for motion commands to the DECtape transport. Solenoid drivers Type 4608 are used to buffer the motion commands to the transport since 100 ma from -15vdc is required to drive the relays in the transport. Additional buffering for control function is provided by standard inverters.

The pulse input to the CD gates comes from a 4606 Pulse Amplifier, which initiates a pulse when the computer instruction to load control is given. Thus, if ACB 12 and ACB 13 are set to a 1 and the load control instruction is issued, the CONTROL MOTION flip-flop will be set to command GO in reverse to both the transport and control.

Function Control

AC bits 15, 16, and 17 are used in conjunction with the load control instruction to load the control with the function commands. This is accomplished by forming complementary inputs with 4102 Inverters and sending them to the level inputs of the CD gates of a 4218 Flip-Flop. The 4218 acts as a buffer which returns the function commands given when load control instructions are issued. These flip-flop outputs are then decoded by a 4151 Binary to Octal Decoder. The functions provided are MOVE, SEARCH, READ, WRITE, RDALL, WRALL, and WRTM. Refer to the Instruction List for details.

Pin D of the function decoder is connected to the output of an inverter whose input is from the GO flip-flop. Therefore, no asserted level (gnd) is issued from the decoder until the GO command is given to the control.

All Halt

The ALL HALT feature stops all moving transports whenever the computer programs stops. This feature is provided by two paralleled 4680 Solenoid Drivers which provide a ground to the go relay latching circuit in the transport when the computer RUN flip-flop is in a 1 state. In addition, an inverter is connected to the GO flip-flop from the RUN input in such a manner that when the RUN state is 0, the GO flip-flop is pulled to a 0 state, thereby stopping the motion of the selected transport.

Delay in Progress (DIP)

The delay in progress circuitry places the control in a timed state of abeyance whenever the transport is commanded to start or turnaround.

This allows the tape to attain a reliable operating speed before normal control functions are permitted to resume. Two separate 4303 Delays are OR combined to form the DIP state.

One delay accounts for the time required for a transport to reverse direction (TA delay) and one allows the transport to reach full speed from a stop condition (start delay). The start delay is inhibited via the CD gate input whenever the tape moves into an end zone. This is necessary when searching for the first or last block on tape since the detection of an end mark automatically

sets the GO flip-flop to 0. The computer would quickly reverse the direction of tape, and if not inhibited in the above manner, this GO flip-flop would initiate the start delay, thus causing the transport to miss the first block on tape.

Write Interlock Circuits (WR-Interlock)

The write interlock circuit enables the 4523 Read-Write to write only when the WRITE LOCK switch is in WRITE position. Although somewhat redundant, the NR-interlock circuit shown on print C1 location A1-4 has been included for reasons of clarity. Basically, the interlock circuit originates in the transport with the WRITE LOCK switch and a contact on one of the selection relays. With the interlock open, the resistor-diode network shown at C1B5 places 25vdc across the contacts (for contact reliability) and places a negative level at the 4141 2-Input Positive AND Circuit. When the interlock circuit is closed, the resistor-diode network places a gnd level on one input to the AND circuit. The second input is gnd when the write enable (WREN) flip-flop is a 1.

To insure switches speed and reliability the output from the 4141 is inverted then buffered with three parallel inverters. The buffered output is tied directly to the enabling level of the information channel writer amplifiers. The timing and mark channels writer amplifiers, however, are enabled via the RELTM relay only when the RELTM switch is on. This switch is used only when timing and mark information must be written on the tape. Further protection against failures which could cause the timing and mark track to be destroyed is afforded through contacts on the RELTM relay which completely disconnect the write amplifiers from the timing and mark channel.

It is therefore impossible to write in the timing (TT) and mark channel (MT) unless the RELTM switch located on panel A of the control logic is turned on.

A red indicator lamp on each transport and a white indicator lamp next to the filter switch warns the operator that the TT and MT writers will be enabled if the command to write is given.

Clear Inputs

Refer to print C1 unless otherwise noted. When the system is turned on, POWER CLEAR pulses for the computer are sent to a 4606 Power Clear pulse amplifier and to one of the preset inputs

of the EK counter (W). The output from the power clear pulse amplifier clears the selection, motion, function and WREN flip-flops (C2). In addition this power clear pulse is connected to a PA which clears the ERROR STATUS flip-flop which in turn clears the data flag and block flag via a third pulse amplifier.

Timing Control

The output of the 4523 Read Amplifier is sent to a 4410 Pulse Generator which standardizes transitions from the read amplifier to DEC 400-nsec pulses (see the TM print). The negative output of both 4410 Pulse Generators are combined with the number of conditional inputs via a 4117 Negative AND Gate. One such enabling level is the delay in progress (DIP) signal which was previously discussed. In addition, an enabling level from a cross talk delay is used to reduce the effect of cross talk during writing. This writing introduces an 8- μ sec delay after actual origination of any TP signal mentioned above. After writing (or before writing) the time lapse between TP1 and TP0 or between TP0 and TP1 is $16\frac{2}{3}$ μ sec. The OFF level occurs whenever the GO flip-flop is cleared provided the write enable flip-flop (WREN) is in the 0 state. This AND function of the WRITE ENABLE signal allows the timing pulses to continue even though the GO signal may be absent. Finally a RELTM level is used to inhibit the pulses from the pulse generator during write timing and mark track mode since in this mode the time pulses are generated directly from this CK counter.

The output from each AND gate is then sent to a pulse amplifier for buffering. It is the output from each of these PAs, TP1, and TP0, which is used for timing throughout the control. During write timing and mark track mode, the time pulses are generated by the CK counter via the CD gate input to the buffer pulse amplifiers mentioned above. A third time pulse, TP2, is derived from time pulse 1 by using time pulse 1 to strobe a 4.5 μ sec delay. The output of this delay is a pulse which is then buffered by a 4606 Pulse Amplifier, the output of which becomes TP2. Reference is made to TP2A which is nothing more than the unbuffered TP2 directly from the output of the 4301 Delay. For all practical purposes both TP2 and TP2A occur at the same time.

Decoding the Mark Track

With the knowledge of how the computer selects the unit, transfers motion and function commands to the control, and knowing how time pulses are generated, it is now possible to describe in detail

the decoding of the mark track. Refer to the print designated Timing Diagram (TD). This print outlines the sequence in which the bits appear in the mark track. As may be seen, a flag is raised every sixth IOT. Each complete block on tape is organized in the following manner. The block begins with a block mark flag followed by a reverse guard; this is followed by four block starts, N number of data words, four block N's, and a guard and reverse block mark. To allow for expansion of the block number, two code 25's are placed between the reverse block mark and the forward block mark. Code 25's are not decoded by the mark track decoder, therefore they do not interfere with normal operation. The block starts are further sub-divided into a lock, a reverse check, and data word 1 and data word 2. The block ends are subdivided into prefinal, final, check, and spare. The octal number which defines the sequence of bits as decoded by the mark track decoder is found written just above each of the previously mentioned six slots or six bit words on the mark track. This sequence as outlined remains the same no matter in which direction the tape is moving.

Mark Track Decoding

Refer now to Print W, Mark Track Decoding Error. Since the mark track is a single channel, the bits are read serially. Location D2 on Print W shows a representation of the head. The signals read from the head are sent to 4532 Read Amplifier. Only one output of this amplifier is used; that is Pin Z. This output is sent to a 9-bit shift register or window as was previously described. Only when the series of bits shifted into this window form a pattern shown in the block just above the shift register will there be flags raised as indicated. These flags will be at a ground level. The one mark that was not previously described is the end mark. This comes up whenever the tape reaches an end zone.

The window is shifted by a circuit which comprises TP1 and \overline{RELTM} located a C6 on Print W. A second input, clear window input to the shift register, is found at location D2. Please note that the output from the clear window PA is produced for both beginning and end of the delay in progress (DIP) for a block mark present at TP0, a guard mark present at TP0, and whenever the GO flip-flop goes to a 1 or POWER CLEAR pulses are present. The period of time for which the window is nonoperative or the window is cleared is shown as a "window shut" period indicated on print TD or Timing Diagram. Please note that the "window shut" condition remains for one slot more when initiated by the block mark than when initiated by the guard mark.

This is due to the fact that the code following the block mark is a 32 which has a 0 bit in the first slot after the block mark whereas the reverse mark has a 1 in the first slot after the guard mark.

Referring again to Print W, the block ends and block starts are subdivided by a second decoder, a 4261. This decoder has somewhat of a window also. It is a 4-bit register which is filled or cleared with ones at specific times in the shift process. The shift register flip-flops are designated MSY_1 through MSY_4 . These flip-flops are preset to a 1000 with the condition of a block mark and TP0. A somewhat more complicated gate allows the shift register to shift at TP2 only with either block starts or block ends. However shifting of ones is done exclusively with block starts, and shifting of zeros is done with block ends. Block ends actually load at the MSY_1 flip-flop with zeros; therefore after four TP2's and block ends, the MSY register is cleared.

This register in conjunction with block ends, block starts, and data marks produces the outputs indicated in the block just above the MSY register. For example, the preset condition in conjunction with the first block start produces what is called a lock output at pin X. As a further example, please note that the read data (RDA) output is available with either data or block starts or block ends and the MSY shift register, containing ones in the MSY_2 and MSY_3 flip-flops. The inverters to the right of the 4261 Decoder are used primarily for inversion and buffering of the outputs from the two decoders.

The presence or absence of a mark from the mark track decoder is checked through the use of an EK counter located on Print W at location C2. This EK counter is a 6-bit register which is wired to shift a single one sequentially through each of the six registers. Thus looking at an output from any one of the flip-flops in the register, a change in state of the output would occur for $33\frac{1}{3}$ μ sec out of 200 μ sec essentially duplicating the pattern shown on the timing diagram. The counter is preset when power is turned on with POWER CLEAR pulses and by a signal from the computer. During normal read and write functions, the EK counter is preset to 100000 at TZA time whenever a block mark is decoded by the mark track decoder. This puts the EK counter in synchronism with the marks from the mark track. Error checking of the mark track is accomplished through an exclusive OR circuit which checks for both the absence and presence of a mark. The exclusive OR circuit is located at D5 on Print W. The guard mark, block mark, block ends, block starts,

and data marks are ORed together in a 4117. The output of this gate is sent directly to one input of a 2-input AND gate, then inverted and sent to one input of a second 2-input AND gate. The second input to both AND gates is EK_1^0 and EK_1^1 respectively. The ORed outputs of both the AND gates thus form the exclusive OR of the EK counter and the marks as decoded from the mark track. This output is sent to a 3-input AND gate which enables the mark track error to occur only when the window is open and a block mark is found.

The block mark found or BMF input is derived from a flip-flop located at C3 on Print W. This flip-flop is zeroed at TP2A time when a check mark is decoded as well for all conditions of clear window except block mark. The BLOCK MARK FOUND flip-flop is set to a 1 at TP2A time only when a block mark is found. Referring once again to the mark track error output located at C6 on Print W, the 3-input AND circuit inhibits mark track error detection within each block in the inter block zone. A 4-input OR circuit is tied to the output of the mark track error detection circuit. This gate inhibits mark track errors for all modes except read, write, read all, and write all. In essence, mark track errors can occur only in the data portion of a block and only in the read, write, read all and write all modes. The output from the mark track error circuit enters a CD gate on Print C2 entitled "flag response data control outputs." It is strobed at TP2 time to set the MTE or mark track error flip-flop to a 1. The output of the MTE flip-flop is inverted and sent to control plug D1 where it is made available to the computer AC input as a status bit. The MTE output also goes to an OR circuit located at A5 on Print C2. This OR circuit forms the OR of all error conditions which will be explained in detail later. The output of the OR circuit is inverted and is also made available to the AC through data control plug D1.

Data Transfer

Data transfer to and from the control is handled through 4228 modules. These modules were especially designed for use in the DECtape controls and consist of an input/output buffer and shift register combination. Each package or module is capable of handling three bits. Refer to the print entitled information handling (IN). Note that the 550 Control is an 18-bit machine and six 4228 packages are required. Further, since there are three information channels, two 4228 packages are wired to each channel. To write information on tape, data is accepted from the computer through information plug D2. It is strobed into the input/output buffer (IOB) with

an MMWR pulse or load pulse. This is tied to Pin Y, print location A1. The data in the IOB is then transferred to the shift register via a pulse labeled B → SR entering Pin W, print location B1. From here the data is shifted serially into the 4523 Write Amplifier. The shift pulses are either shift right or shift left, Pin Z and U respectively of the 4228, depending upon tape direction.

The data transfer from the input/output buffer to the shift register is a parallel transfer handled internally by the 4228 modules. To read information from the tape data is read by the head, amplified by the 4523 Read Amplifier, and assembled bit by bit by the shift register until six bits are assembled. The shift right and shift left pulses actually load the output of the reader into the shift registers. When six bits have been assembled, in each of the three information channels, a pulse labeled SR → IOB transfers the information from the shift register into the input/output buffer. All 18 bits are then available to the computer via information plug D2. Note that the pulses B → SR and SR → IOB are one and the same pulse. Thus this single pulse has become known as an interchange pulse which does just that. It exchanges the data in the input/output buffer with the data in the shift register.

Operation of the Control in Search Modes

In search mode the control raises a data flag every time it passes over a block mark. Refer to print C2, location C4. A 1011 AND Gate is used to combine the search mode with a block mark track input to enable a CD gate. This CD gate is strobed at TP2 time and if enabled, pulses the input to a pulse amplifier located at B2. The output of this pulse amplifier is sent to the base input of an inverter located at B5. The output of this inverter then sets the DATA FLAG flip-flop, print location plug D1. The raise data flag pulse or RDF pulse is also sent to the pulse input of a CD gate input to the interchange PA located on PM print, print location A6. Thus whenever a block mark is found an interchange takes place which transfers the data from the shift register into the IOB. The data in this mode is the block number. As mentioned before the shift right and shift left pulses shift the data in the shift register to the right or to the left depending upon the direction of tape. However, in the search mode information is shifted right only. This may be seen by referring to print TM location B5. Two 4606 PA's are used for the shift right and shift left pulses. Pin N input to the shift right pulse amplifier comes from a 4127 CD Gate whose pulse input is TP1. The level input comes from a 1011 AND Gate whose

whose inputs consist of SEARCH and WREN^B₀. Thus, if in search mode and not writing, the shift register is shifted right at TP1.

This is the only mode in which shifting is not dependent upon the direction of tape. The reason for this is that the reverse block mark is written as the complement obverse. Therefore rearrangement of the bits is not necessary.

Operation of the Control in Read Mode

In read mode the control raises a data flag for each 18-bit data word just assembled and transferred to the IOB or input/output buffer. Refer to location C4, print C2 entitled "flag response data control outputs." A 2-input AND gate whose inputs consist of read and RDA is used to enable a CD gate which is pulsed at TP2. The output of the CD gate pulses the raise data flag amplifier and the same sequence of events takes place as was described for the conditions of search. The RDA input to the 2-input AND gate originates from the 4261 module shown on Print W entitled "mark track decoding error" at location A5. The RDA output is formed by the jumpering of Pins S and W thus referring also to print TD or timing diagram. Note that the RDA flags consist of the reverse check flag, the last two block start flags, all the data flags, the prefinal flag, and the final flag.

The first 18-bit data word transferred in this mode is the reverse check word. This word is combined by the computer with the rest of the data and the check sum word at the end of the block to determine if the data transfer was done correctly. The check word is the last word transferred when reading a block. Since the block length could be variable, it is necessary to indicate to the computer when the last word is read. This is accomplished by raising what is known as a block flag. Refer once again to print C2, location C5. A 2-input AND gate whose inputs consist of both READ and CHECK enables a CD gate whose output strobes the raise block flag PA at TP2. The block flag pulse amplifier is located at B1. The output of this PA enters the base of an inverter located at B6. This inverter in turn sets the BLOCK FLAG flip-flop located at B4 to a 1. The output of the block flag then is inverted and made available to the computer through a control plug D1. Thus, in read mode the check flag signals the computer that the end of the block has been reached and that the data should be checked for errors. Refer to Print TM, location A6. Note that interchange pulses occur each time the data flag or a block flag is raised.

In read mode the shift register is shifted either right or left depending upon the direction of the tape when the data transfer occurs. The logic necessary to do this is located on Print TM, Print location C5. A 3-input AND gate, whose inputs consist of $REVB^0$, $WRENB^0$, and \overline{WRITE} mode, enables the CD gate input to a 4606 Pulse Amplifier. The pulse input to this CD gate is TP1. The output of this PA causes the shift register located on the IN print to shift right and is identified as SHIFT MMSR RT. The output of this PA is therefore available at TP1 time when the tape is going forward when not in write mode and the writers are not on. Just below this gate there is a 4-input AND gate whose inputs consist of $\overline{WRITE} REVB^1$, $WRENB^0$, and \overline{SEARCH} . The output enables the CD gate input to a 4606 Pulse Amplifier. The pulse input again is TP1. The output from this PA is designated SHIFT MMSR LT. Thus when moving in reverse the control is not in the write or search mode, the writers are not on and the shift register is shifted left at TP1 time.

Operation of the Control in Write Mode

In write mode once again the computer is signaled via the data flag and the block flag. However, the signal in this mode requests the computer to load the input/output buffer. The control then transfers the contents of the IOB to the shift register and from there to the write amplifier to be written on tape. Refer to print C2, location C5. A 2-input AND gate, whose inputs consist of $WRITE$ and WDA , enables a CD gate which pulses the RBF pulse amplifier at TP2 time. The WDA 's or write data flags come from the 4261 Decoder on print W. The WDA flags consist of all the block start flags plus all data flags. Note that the first data flag to be raised occurs with the first block start flag. The computer responds to this data flag by loading the input/output buffer. On the next block start flag a data flag is again raised. This time the contents of the input/output buffer are interchanged with the shift register where they are immediately shifted and written on the tape. Refer to the print entitled timing diagram. Note that the actual position that data was written on tape is indeed in the area where the first data word is read in the read mode. Thus, if data is to be written in a particular location on tape, the input/output buffer must be loaded two mark flags before the desired position on tape.

During write mode the reverse sum check is automatically written on tape by the control. This is accomplished by a network located at A5 on print TM entitled "control pulses." A 3-input AND gate whose inputs consist of $LOCK$, $RDALL$, and $WRTALL$ enable the CD gate input to

a 4606 PA. The pulse input is TP2. The negative output of this PA is sent to the CLEAR input of the shift register. This same pulse is sent to the positive input of a 4606 Pulse Amplifier. Note that it is a positive overshoot of a pulse amplifier which triggers the 4604. The output of this PA then complements the shift register. The net result of these two pulses causes all ones to be written as the reverse check word at the beginning of the block. In general, if the control is not in RDALL or WRTALL mode, the block flag causes all ones to be written as the reverse check word. Note the negative overshoot of the 4604 is used to complement the shift register.

In order to preserve all ones in the shift register at this time the interchange pulse must be inhibited. This is done via a 3-input positive NOR gate located at B5 on print TM. The three inputs consist of $\overline{\text{LOCK}}$, $\overline{\text{RDALL}}$, and $\overline{\text{WRTALL}}$. The output enables the CD gate input to the interchange PA. The pulse input to the CD gate is the RDF pulse. Thus, if the control is not in RDALL or WRTALL mode, interchange pulses are produced for every RDF except the one that occurs with the lock flag. Also, if the control is in either RDALL or WRTALL mode, interchange pulses will occur for every RDF pulse.

When the end of the block is reached the prefinal flag is ANDed with the write mode to cause a block flag to be raised at TP2. This tells the computer to load the IOB with the computed check sum. Once loaded the control then takes over and writes the check-sum word in its proper position on tape. The ANDing of the prefinal flag with the write mode may be checked on print C2 location C5.

Thus far the description has covered the transfer of data from the computer to the IOB, then to the shift register in response to a data or block flag. Now consider the actual process involved in writing information on tape.

In the read mode, shifting of the shift register was determined by the direction of tape and occurred at TP1. However in the write mode shifting occurs at TP0 time. Refer now to location A7, print TM entitled "control pulses." The PA which produces shift writer left (SLW) pulses has two inputs; the first consists of a CD gate whose enabling level is produced by a 2-input AND gate and whose pulse input is TP0. The two inputs to the AND gate are WRENB^1 and REVB^1 . Thus with this logic connection, when the tape is moving in reverse and the write enable flip-flop is on, SLW pulses are produced at TP0. The second input to the PA is through

its own CD gate, whose enabling level is produced by $REVB^1$, and whose pulse input is the transition of the WREN flip-flop to a 1. The actual input is $WRENC^1$ which is the buffered output of the WRITE ENABLE flip-flop. The inverted output of this particular PA is designated as SLWB. The pulse caused by the transition of the WRITE ENABLE flip-flop is necessary to load the write buffers in the write amplifiers with the first bit from the shift register. This transition also occurs at TPO.

As the tape moves in the forward direction during write mode, shiftwriters right (SRW) pulses are produced by a circuit similar to the one described above with the exception that direction input is $REVB^0$, which indicates that the tape is moving in a forward direction. The output from the SLW PA is sent to the shift MMSR rt PA located at B5. The SRW PA is sent to the shift MMSR Lt PA located at C5. Thus the shift register is shifted right or left depending upon the direction of tape at TPO when in write mode.

Refer now to print IN entitled "information handling." At the same time that the shift register is shifted, its contents are being loaded into the write amplifier word buffer via the SRWB or the SLWB pulses. Once the write amplifier word buffer has been loaded with the contents of the shift register, the actual writing of the bit takes place whenever the word buffer is complemented. The complement input originates on TM print at location B7. The mnemonic for the output of this PA is CPWR or complement the information writers. This pulse is present at TP1 when the WRITE ENABLE flip-flop is a 1. With all the previous conditions met, it is still impossible to write on a tape unless the write amplifier is enabled. Enabling the write amplifier is done via the right interlock line which was discussed when the C1 or control print was described.

The WRITE ENABLE flip-flop is controlled by a number of inputs. Refer to print C2 at location D3. WDA flags and RDA flags enter a 2-input OR gate, the output of which is sent to a 3-input AND gate located at C3. The other two inputs to this AND gate are WRITE MODE and UNABLE. The unable condition will be discussed under error responses. The output of the 3-input AND gate then enables a CD gate located at B3. The pulse input to this CD gate is TPO and the output is tied to the WRITE ENABLE flip-flop. Thus the WRITE ENABLE flip-flop may be turned on at TPO time only if the control is in write mode, the transport is not unabled, and WDA or RDA block flags are present. The WRITE ENABLE flip-flop is turned off at TP2.

via CD gate whose enabling level comes from a 4-input AND gate located at C2. The 4 inputs are $\overline{\text{WRITE}}$, $\overline{\text{WRTMR}}$, $\overline{\text{WRTALL}}$, and the output of a 4-input OR circuit located at D1. The four inputs to this OR circuit are WDA flags, the condition of RELTM, the prefinal flag, and the output of a 2-input AND gate also located at D1. The RELTM input is a contact closure to ground whenever the RELTM switch is turned on thus causing the 1802 Relay to be energized. For this combination refer to print C1, location A2. The inputs to the 2-input AND gate are EK1B and NOT FINAL.

The main purpose of this entire network is to guarantee that the WRITE ENABLE flip-flop will not be turned off unless enough time has been allowed to write the complete word. When in write mode the condition of WDA, prefinal, or EK1B, at a time other than when a final mark is decoded, determines if the write enable flip-flop will be turned on. In effort to protect the block numbers a second circuit located at C1 is used to turn the WRITE ENABLE flip-flop off whenever a check flag is raised or as double protection when a guard flag is raised except when in WRTALL mode. Note the 2-input AND gates which combine CHECK and $\overline{\text{WRTALL}}$ to turn the WRITE ENABLE flip-flop off at TP2 or TP0 and combine a guard flag and $\overline{\text{WRTALL}}$ to turn the WRITE ENABLE flip-flop off at TP0. Thus if the computer commanded the control to write more than one block, the WRITE ENABLE flip-flop would be turned on with the check flag, and then would be turned on again when the first block start flag of the next block was raised.

Operation of the Control in Read All Mode (RDALL)

In this mode of operation the interblock zones are ignored. Therefore a data flag is raised for every 6 lines on tape or every 200 μsec . The data transfer in this mode is similar to the read mode. The readall mode is used to read unusual tape format which is not compatible with the read mode. Refer to print C2, location C6. A 2-input AND gate is used to combine EK1B with either read all or write all to enable a CD gate to raise a data flag at TP2. Raising the data flag in this mode causes the computer to respond in the same way as it did for other modes. However it may be noted on print TM that the interchange pulses take place for every RDF since the control is in the RDALL mode.

Operation of the Control in Write All Mode (WRTALL)

As in the RDALL mode, the WRTALL mode ignores all interblock zones thus allowing the operator to write information in any position on tape. This mode is similar to the read all mode for writing. Refer once again to print C2, location C6. Again the data flag is raised as in the RDALL mode except that the asserted level to the second input to the 2-input positive NOR gate is caused by the WRTALL mode. The WRITE ENABLE flip-flop is turned on through the use of a 4-input positive NOR gate located at A1 in print C2. The four inputs are TP0, EK1B, WRITE ALL, and NOT ENABLE. Therefore, the WRITE ENABLE flip-flop is turned on at TP0 when EK1B is present in the WRTALL mode and the transport is not in an unable condition. The WRITE ENABLE flip-flop is turned off when the $\overline{\text{WRTALL}}$ condition occurs at the 4-input AND gate located on print C2 at location C2, entitled "operation of the control in the WRTM or write timing and mark track mode."

In order to write timing and mark track on tape it is first necessary to turn the RELTM switch on. This, in turn, energizes a relay whose contacts are in series with the write amplifier inputs to the head on both the timing and mark track. In addition, the relay energizes a clock which, in turn, drives the CK counter located on print TM, location A2. The CK counters generate the timing necessary for the control during this mode and load the write buffer in the timing track write amplifier as shown at location C1. The mark track word buffer located at C1 on print W is loaded from the shift register associated with information channel 1.

Loading occurs depending upon directions by either the SRWM or the SLWM input. Refer to print TM, location B7. SRWM or SLWM pulses are available only in the write timing and mark track (WRTM) modes. This is because the level input to the CD gates driving these PA's is $\overline{\text{WRTMR}}$. The WRTMR input originates from the WRTM mode through a relay contact as both the WRTM mode and the RELTM. Relay must be on in order to have this level (Refer to location A2, print C1). The pulse input which produces the SRWM is the SRW pulse. Similarly the SLWM output is produced by the SLW pulse. Therefore, loading of the mark track word buffer occurs at TP0. Writing the bit, as in the information channel writers, is done when the word buffer in the mark track writer is complemented.

Timing and mark track information on tape is written only when the enabling level to the timing and mark track writers is present. This level is designated WT-INTERLOCK R and is nothing

more than the WT interlock line wired through a series contact of the RELTM relay.

Refer now to location C3 on print C2. Note the 2-input AND gate whose inputs consist of WRTMR and EK6 enables two CD gates. One gate pulsed at TP0 time sets the WRITE ENABLE flip-flop to a 1. The other gate pulsed at TP2 raises the data flag. Therefore, when in WRTM mode with the RELTM relay closed, the occurrence of EK6 and TP2 raises the data flag thereby indicating to the computer that the control is ready to transfer an 18-bit word. Since in this mode the timing originates from an internal clock, the data flag is raised at regular 200- μ sec intervals. When the computer is finished writing the timing and mark track, the WRITE ENABLE flip-flop is turned off by the 4-input AND gate located at C2 of print C2.

ERROR RESPONSES

There are four error conditions, unable, misindication, off end, and mark track error. Flip-flops for these conditions are shown on print C2 in location B5.

Unable Condition

The unable condition is set by three separate inputs, refer to location C7. Note the 2-input AND gate, whose inputs consist of INFORMATION WRITE level and WREN¹. If the WREN flip-flop is a 1 and the INFORMATION WRITE level is not present, the output of this AND gate will be negative. This negative input is applied to a 2-input negative OR gate located at B8. Any input being negative causes the UNABLE flip-flop to be set to a 1 state. The output of this UNABLE flip-flop is inverted and made available to the control plug D1 as the unable status bit.

The second source of an unable error comes from a 3-input AND gate located at C7 of print C2. The three inputs are WREN¹, $\overline{\text{WT Interlock R}}$, and WRTM mode. Thus, if the WRITE ENABLE flip-flop is a 1, the control is in write timing and mark track mode, and the timing and mark track writers are not enabled, an unable condition exists. (Note: The unable condition which occurs when the control is requested to write on tape is caused by the WRITE LOCK switch on the transport not being in WRITE position.)

The third unable error is caused when a single transport is not selected. Refer to location C8 of print C2. Two sections of a 1501 Level Standardizer monitor the current through the ground

return of the 4671 Decoder used in selecting the drives. If less than one or more than one drive is selected, the voltage developed across the 5-ohm resistor causes the output of the 1501 to be negative. This negative level enables the CD gate, located at B8, to be strobed on the transition of \overline{DIP} or the end of the delay in progress. If the level input is true, the output of this CD gate sets the UNABLE flip-flop to a 1 thus causing an unabled error condition. As a matter of information, the reference voltages developed for the inputs of the 1501 are -0.3 v at the junction of the 150-, 270-ohm resistors and -0.7 v at the junction of the 270-, 6800-ohm resistors. The current to pin D for a single drive is approximately 100 ma; thus -0.5 v developed across the 5-ohm resistor when a single drive is selected.

Misindication

The next error condition is MISIND error and is caused whenever the data flag or the block flag from a previous data transfer has not been cleared before the control requests another transfer. Refer to print C2 location B7. Two CD gates are used to set the MISS-flip-flop; one CD gate is pulsed by the RDF pulse and the level input is in a condition of assertion when the DATA FLAG flip-flop is in a 1 state. The second CD gate is pulsed by the RBF pulse and by the same token is enabled by the BLOCK FLAG flip-flop. The inverted output of the MISS-flip-flop is available to the control plug D1 as a status indication.

End Error

The third error condition which can exist is the end error. This flip-flop is set at TP2 whenever the tape enters an end zone. (Refer to location B8.) When the mark track decoder detects that it is an end zone, two CD gates are enabled: one sets the END flip-flop and the other zeros the GO flip-flop, thus stopping all control functions. The output from the END flip-flop is inverted and made available to the control plug D1 as a status indication.

Mark Track Error

The fourth and final error is a mark track error. This flip-flop is set whenever there is a mark track error at TP2. The details concerning the detection of a mark track error are found in the description of the mark track decoder. The output of the mark track error flip-flop is also inverted and made available to the control plug D1 as a status indication.

All four error conditions are ORed together through a negative diode NOR gate located at A5. The output of the NOR gate is inverted and made available to the control plug D1 as a status indication. Whenever an error exists, the WRITE ENABLE flip-flop is set to 0 via the D003 Diode shown at the output of this OR gate. This prevents the control from writing once an error condition has been discovered.

CHAPTER 3

INTERFACE

All logic levels between the computers and DECtape are either standard DEC logic levels or standard DEC pulses. A standard DEC logic level is either ground (0 to -0.3 v) indicated by an open diamond (\diamond), or -3 v (-2.5 to -3.5 v), indicated by a solid diamond (\blacklozenge). Dual-polarity level logic is used; therefore the particular voltage-logic state relationships are defined by individual usage. Logic levels that are applied to the conditioning level input of capacitor-diode gates must be present for 1 μ sec before an input triggering signal is applied to the gate. The standard DEC negative pulse is indicated by a solid triangle (\blacktriangleright) and goes from ground to -2.7 (-2.3 to -3.5 v). The standard DEC positive pulse, indicated by an open triangle (\blacktriangleleft), goes from ground to +2.7 v (+2.3 to +3.2 v). The width of the standard pulse used in this equipment is 400 nsec.

Two 50 pin cables are used to connect the 550 Control to either a PDP-1 or PDP4/7. The connection points for interface signals at these two I/O connectors, D1 and D2, are listed in the table.

TABLE 3-1 CONTROL CONNECTOR D1

Signal	Symbol	Terminal	Direction (With Respect to Control)
MMEF-MMDF	-----*	1	
MMEF-MMDF	----- \blacktriangleright	2	in (PDP-4/7 only)
MMRD	-----*	3	
MMRD	----- \blacktriangleright	4	in
MMWR	-----	5	
MMWR	----- \blacktriangleright	6	in
MMSE-MMLC	-----	9	

*Ground side of pulse transformer secondary winding

TABLE 3-1 CONTROL CONNECTOR D1 (continued)

Signal	Symbol	Terminal	Direction (With Respect to Control)
MMSE-MMLC	→	10	in (PDP-4/7 only)
MMDF	----	11	
MMDF	→	12	out (PDP-4/7 only)
MMEF	----	13	
MMEF	→	14	out (PDP-4/7 only)
Power Clear	----	15	
Power Clear	→	16	in
RUN	◆	19	in
MMSE	----	20	
MMSE	→	21	in (PDP-1 only)
MMLC	----	22	
MMLC	→	23	in (PDP-1 only)
MMB	----	24	
MMB	→	25	out (PDP-1 only)
DATA FLAG	◆	26	
BLOCK FLAG	◆	27	
ERROR FLAG	→	28	
END	→	29	
MISS TIMING	→	30	
REV	→	31	
GO	→	32	
MTE	→	33	
UNABLE (selection error)	----	34	
-15v marginal check		43	
voltage from computer		44	
-15 v remote power control		49	
GND		50	

TABLE 3-2 INFORMATION CONNECTOR D2

Signal	(PDP-1, -4, -7)	Symbol	Terminal	Direction (Reference to Control)
IM/MMIO	0	→	1	out
IM/MMIO	1	→	2	out
IM/MMIO	2	→	3	out
IM/MMIO	3	→	4	out
IM/MMIO	4	→	5	out
IM/MMIO	5	→	6	out
IM/MMIO	6	→	7	out
IM/MMIO	7	→	8	out
IM/MMIO	8	→	9	out
IM/MMIO	9	→	10	out
IM/MMIO	10	→	11	out
IM/MMIO	11	→	12	out
IM/MMIO	12	→	13	out
IM/MMIO	13	→	14	out
IM/MMIO	14	→	15	out
IM/MMIO	15	→	16	out
IM/MMIO	16	→	17	out
IM/MMIO	17	→	18	out
IO/ACB	0	→	19	in
IO/ACB	1	→	20	in
↓	↓	↓	↓	↓
IO/ACB	17	→	36	in
MBB12 ¹		→	37	in (PDP-4/7 only)
MBB12 ⁰		→	38	in (PDP-4/7 only)
GND			50	

*Ground side of pulse transformer secondary winding

INTERFACE DESCRIPTION

<u>MMEF-MMDF</u>	ERROR FLAG and DATA FLAG. This pulse, used only for the PDP-4/7 is available to the DECtape control when the instruction 75 x 1 is issued. The control combines the pulse with memory buffer bit 12 to form two separate IOT's, MMEF or MMDF, which are returned to the computer skip logic.
<u>MMRD</u>	READ. Refer to the DECtape instruction list.
<u>MMWR</u>	WRITE. Refer to the DECtape instruction list.
<u>MMSE-MMLC</u>	SELECT and LOAD CONTROL pulse, used only on the PDP-4/7, is sent to the DECtape control when the instruction 76 4 is issued. The control combines this pulse with memory buffer bit 12 to form two separate IOT's, MMSE or MMLC, which are separately used by the control.
<u>MMDF</u>	DATA FLAG skip pulse causes a skip when the data flag from the control is set.
<u>MMEF</u>	ERROR FLAG skip pulse causes a skip when the error flag in the control is set.
<u>Power Clear</u>	Clears the selection, motion, function, mark track windows, error status, data and block flags, and the write enable flip-flops. It also presets the EK counter.
<u>RUN</u>	RUN in a zero state stops all drives in motion.
<u>MMSE</u>	SELECT. Refer to the DECtape instruction list.
<u>MMLC</u>	LOAD Control. Refer to the DECtape instruction list.
<u>MMB</u>	PDP-1 break request.

DATA FLAG

Status level sent to computer-set during search when a block number is assembled in the MMIOB (control data buffer) or during read or write functions when the control is ready for data transfer. This level is also connected to the interrupt and skip logic in the PDP-4/7.

ERROR FLAG

Status level sent to the computer whenever any one of the following errors occurs:

1. Tape has reached an end zone.
2. A block flag or data flag was not cleared before another occurred.
3. A Mark Track Error.
4. The transport is not conditioned to perform the desired task, either because the WRITE LOCK switch was not in WRITE position when the control was commanded to write, or a single transport was not selected. This level is also connected to the interrupt and skip logic with PDP-4/7.

BLOCK FLAG

Status level sent to the computer during read or write mode when the control is ready for transfer of the check sum. This level is also connected to the PDP-4/7 interrupt and skip logic.

END

Status level indicating that the tape has moved into an end zone.

MISS TIMING

Status level set when the computer raises a data flag or block flag before the computer is able to clear them.

REV

Status level indicating the state of the reverse flip-flop (CI); therefore, the direction in which the tape was or will be moving.

GO

Status level indicating the state of the go flip-flop (CI); therefore, the state of the transport when status is read.

MTE

Status level set when an error occurs either in the timing or mark track.

UNABLE

Status level indicating that either the WRITE LOCK switch is not in WRITE position or a single transport is not selected.

IM/MMIO-0→17

Information transfer lines from the control.

IO/ACB-0→17

Information transfer lines from the input-output register of the PDP-1 and the accumulator of the PDP-4/7.

MBB12¹

The "one" signal from the PDP-4/7 memory buffer which is used in conjunction with the MMSE--MMLC and MMEF--MMDF pulses to produce separate MMSE, MMLC, MMEF, and MMDF IOT's.

MBB12⁰

Same as MBB12¹ except the "zero" signal.

CHAPTER 4

OPERATING INSTRUCTIONS AND PROGRAMMING

The operating instructions for the DECTape system consist, basically, of tape loading and manual switching operations. Each is described below. Following them is a subsection devoted to programming information.

LOADING THE PROGRAM

There are no special instructions other than the ones for using the computer. There are, however, some standard pitfalls. First be sure the program is the correct one for the computer as well as for the desired operation. Insert the paper tape in its proper orientation. There is one correct way out of four. If the program does not load (in the case of a PDP-4 or -7), check the loader instructions. Remember that if it is an 8K machine, add 010000 to all instructions other than IOT's. Then follow the written program closely.

Certified Tape

DECTape systems give the user, for the first time, a means of marginal checking his own tape. Checking is done by recording a pattern on tape, reducing the signal read from the head by a factor of five, and making sure that the tape still works. This process assures that, for the conditions at the time of the test, there was an amplitude margin of at least five to one for the signal from the tape. The attenuation is accomplished by replacing a jumper plug on the back panel of the control (at C19 and C24) with another which has a resistor attenuator on it. The module number of the jumper plug is 1033.

DEC can provide certified tape. This tape has written on it a mark track, a timing track, and a pattern of 577 blocks each 256 words long. It is checked as above with the further refinement that read amplifiers of average gain margins are used; the signal is attenuated to an average of 1.6 mv, p-p, and the writing is done on a skew corrected head.

SWITCH FUNCTIONS

There is only one switch on the 550 Control, the WRTMR switch located just below plug A22. Its function is to turn on the clock which is used only when writing the timing and mark track on the tape.

Turning Off Unit

Ordinarily, the DECtape system is controlled by an associated computer which turns the system off. When off, the tape should be checked for excess slack, and corrected, if necessary, by using the AC switches which control the individual drives. If computer control is not provided, the DECtape unit can be turned off by simply throwing the power switch.

PROGRAMMING

Included at the end of this subsection are IOT's of relevance when the DECtape system is used in conjunction with a PDP-1, PDP-4, or PDP-7 computer.

Preprogrammed Subroutines

As mentioned earlier in this manual, three types of program subroutines are furnished with, or can be obtained for use with, the DECtape system. The first is a basic set of subroutines for searching, reading, and writing. The second, Microtog, is a set of maintenance and diagnostic programs which can accomplish combinations of DECtape functions using the toggle switches on the console. The third, Microtrieve, is a routine which saves programs or data on DECtape and permits quick retrieval by means of toggle switches on the computer console. Microtog and Microtrieve both employ the basic read, write, and search subroutines described above. These latter subroutines, with small differences are basically the same for the PDP-1, PDP-4, and the PDP-7.

Subroutines for PDP-1

For the PDP-1, the basic subroutines are designed to read or write one block of information in either direction, depending on the position of the tape and the direction in which the tape is searched. Searching in the reverse direction results in a transfer of data, the start of which

coincides with the end of the block in core storage. In the forward direction, data is transferred upon encountering the beginning of the block in question. Thus, the direction of reading is independent of the direction of writing, and memory words are preserved. In searching, the appropriate unit designation, the block number, and the error return are used as parameters. The read and write subroutines both require a unit designation, block number starting address, and error return as parameters. The read and write subroutines automatically enter the search subroutine to find the request block.

After completion of the subroutines mentioned above, the tape is not stopped, but allowed to run if so programmed.

Subroutines for PDP-4 and -7

Subroutines applicable to the PDP-4 and -7 permit specification of the total number of words for transfer regardless of block format. Searching is permitted in both the forward and reverse directions; however, both reading and writing are permitted only in the forward direction. Should the number of words specified for transfer result in use of only a portion of some block, the remainder of the block would be filled in with zeros (if writing) or the remainder of the block would be read (if reading) even though the words so read are not utilized in any manner. The purpose of this latter action is to permit the check sum to be calculated or checked. It should be noted that the program interrupt mode of operation constitutes the basis for the above discussion, and that one auto-index is defined by the main program. The instruction "dismiss" is defined as a jmp to the instructions which dismiss the interrupt. Instruction to check the appropriate flags are also included in the interrupt sequence.

For the PDP-4 and -7, the search subroutine requires a unit designation, block number, and error return as parameters. Searching terminates with either a stop, or a running in either the forward or reverse direction, according to the subroutine entrance used. As soon as searching is started, a return is made to the main program to allow simultaneous multiprogramming.

For the read and write subroutines, the unit designation, block number, starting and ending core addresses, and error return are required as parameters. These routines cause automatic entry into the search mode to position the tape. During data transfers, no multiprogramming

is permitted. After completion of transfer, the tape is stopped. Errors are detected, coded numerically, saved in status bits, and indicated by a special return. The coding of the error type may be followed by continuance of the desired program.

Microtog

The Microtog subroutines are applicable for use with either the PDP-1, PDP-4, or PDP-7. These subroutines consist of a number of short programs which check out the various DECtape functions under control of the console toggle switches. Some of these short programs are: creating the mark track as individual block format; reading or writing specific portions of the tape; writing a clear tape in either direction; sum-checking specified modes for indicated times or distances; generation of specified types of data block; and exercising the tape by writing, reading, and sum-checking in both directions. Errors are analyzed and indicated by typeout. The typeout includes the block causing the error and the exact status of the DECtape at the time of the error.

Microtrieve

The Microtrieve subroutine permits, by use of toggle switches on the main console, the storing or retrieving of data in specified locations. During storing, a search is made for the block indicated; then the indicated area of memory is written on the tape, accompanied by an identification designation into control words. Upon completion of the storage process, a typeout is executed. The typeout lists the starting and ending block numbers used for the storage and a number representing the total check sum of the entire area so written.

During retrieving, a portion of data information on the tape is stored in core memory. Its location is indicated by the status of the toggle switches. For retrieving, the unit designation and block number must be specified; the control words on the tape indicate the starting address and length of information in memory. In this subroutine, the check is made to insure that the block specified is actually the start of the storage area. Upon completion of retrieval, a typeout is effected which lists the starting and ending block numbers and the total check sum. These items can be checked against the typein data as a verification of the retrieval. Errors are analyzed as noted above under Microtog.

Instructions

Input-output transfer instructions for use when DECTape is employed with a PDP-1, PDP-4, or PDP-7 are given in Table 4-1. Table 4-2 gives a sample of DECTape operation with a PDP-4 or -7.

TABLE 4-1 DECTAPE INSTRUCTION LIST

PDP-1 Mnemonic	PDP-1 Binary	PDP-4 or -7 Mnemonic	PDP-4 or -7 Binary	Function
MRD	720501	MMRD	707512	READ. Clears I/O or AC and transfers one word from MMIOB to bits 0-17 of I/O (PDP-1) or AC (PDP-4 or -7).
MWR	72061	MMWR	707504	WRITE. Transfers one word from bits 0-17 of I/O (PDP-1) or AC (PDP-4 or -7) to MMIOB.
MSE	720301	MMSE	707644	SELECT. Connects the unit designated in bits 2-5 of the I/O (PDP-1) or AC (PDP-4 or -7) to the DECTape control.
MLC	720401	MMLC	707604	LOAD CONTROL. Sets the DECTape control to the proper mode and direction from bits 12-17 of the I/O (PDP-1) or AC (PDP-4 or -7), as follows: Bit 12 = Connect (Go) Bit 13 = Reverse Bit 14 = Spare Bit 15-17 = Mode: 0 = Move 1 = Search 2 = Read 3 = Write 4 = Spare 5 = Read through block ends 6 = Write through block ends 7 = Write timing and mark track i.e. 42 = Read forward 62 = Read reverse 43 = Write forward 41 = Search forward 61 = Search reverse

TABLE 4-1 DECTAPE INSTRUCTION LIST (continued)

PDP-1 Mnemonic	PDP-1 Binary	PDP-4 or -7 Mnemonic	PDP-4 or -7 Binary	Function
MRS	720701	MMRS	707612	<p>READ STATUS. Clears the I/O or AC and transfers the DECTape status conditions into bits 0-8 of the I/O (PDP-1) or AC (PDP-4 or -7) as follows:</p> <ul style="list-style-type: none"> Bit 0 = Data flag Bit 1 = Block end flag Bit 2 = Error flag Bit 3 = End of tape Bit 4 = Timing error Bit 5 = Reverse Bit 6 = Go Bit 7 = Mark track error Bit 8 = Tape unable
		MMDF	707501	<p>Skip on DECTape data flag.</p> <p>In search mode: Block mark number should be unloaded via (M) MRD instruction.</p> <p>In read mode: Data or reverse check sum should be unloaded via (M) MRS instruction.</p> <p>In write mode: Data should be loaded via (M) MWR instruction.</p>
		MMBF	707601	<p>Skip on DECTape block end flag.</p> <p>In read mode: Unload forward check sum via (M) MRD instruction.</p> <p>In write mode: Load calculated forward check sum via (M) MWR instruction.</p>
		MMEF	707541	<p>Skip on DECTape error flag. Timing error, mark track error, end tape, or tape unable condition has occurred. Use (M) MRS instruction to detect specific error.</p>

NOTE: MMSE and MMLC clear the error flag; and MMSE, MMLC, MMRD, and MMWR clear the data and block end flags.

TABLE 4-2 DECTAPE OPERATION CHART (PDP-4 AND -7)***

FLAG	MOVE MODE	SEARCH MODE
Data flag cleared on MMRD MMWR MMLC MMSE This flag causes interrupt.	No data flags raised. Tape motion is continuous until end marks are sensed at far end of tape.	Data flag means that the MMIOB contains a block number. Write mode may be specified within 400 μ sec to transfer the block. Read mode may be specified within 600 μ sec.* Any other mode (including stop), may be commanded at any time. Transfer of block number must be completed before the next block to avoid a MISS.**
Block Flag cleared on MMRD MMWR MMLC MMSE This flag causes interrupt.	Should not occur.	Should not occur.
Error flag cleared on MMSE MMCL (also clears MISS, END, MTE This flag causes interrupt.	Error flag means that an error has occurred. An MMRS command will load AC bits 0-8 with status information. (END is only possible error.) End status bit is set when tape reaches for end. Error flag is raised. Tape stops.	Error flag means that an error has occurred. An MMRS command will load AC bits 0-8 with status information. (END, and MISS are only possible errors.) End status bit is set when tape reaches far end. Error flag is raised. Tape stops. Miss Status bit is set when a data or block flag has not been cleared from previous use.

* All times are nominal for forward direction. In reverse direction add $\pm 20\%$.

** MISS indicates a programmed timing error; i.e., information will be lost (missed) because the routine is taking too long to transfer data to or from the buffer.

*** Operation for the PDP-1 is similar except that the I/O is referenced rather than the AC.

TABLE 4-2 DECTAPE OPERATION CHART PDP-4 (continued)

FLAG	READ MODE	WRITE MODE
<p>Data flag cleared on</p> <p>MMRD MMWR MMLC MMSE</p> <p>This flag causes interrupt.</p>	<p>Data flag means that MMIOB contains a data word. An MMRD must be given within 200 μsec for data transfer.</p> <p>First data flag in block indicates reverse check sum. Change to other modes possible within 200 μsec. If write mode is desired, a 1-word delay occurs after MMWR is given.</p>	<p>Data flag means that MMIOB is ready for data word. An MMWR must be given within 200 μsec for data transfer. Initial (-0) check sum is written automatically. First flag in block is a request for first data word. Change of mode possible within 200 μsec. Since tape system is bidirectional, the initial check sum written must be placed at either forward or reverse check sum location in block, depending only on direction commanded.</p>
<p>Block flag cleared on</p> <p>MMRD MMWR MMLC MMSE</p> <p>This flag causes interrupt.</p>	<p>Block flag means that check sum is in MMIOB. First data flag of next block automatically occurs in 1.4 msec. Change to search mode must be made in next 800 μsec in order to catch next mark. Change to write mode must be made within next 1.2 msec in order to start new block (not recommended - Block number should be checked by search mode).</p>	<p>Block flag means that check sum should be loaded into MMIOB with an MMWR. First data flag of next block occurs in 1.6 msec. Change of mode commanded at last data word (D256) is delayed while check sum is written. Change to search mode must be made within 1.2 msec to read next block number. Preferred method of stopping is to change to search mode, then check succeeding block number for correctness before stopping.</p>
<p>Error flag cleared on</p> <p>MMSE MMLC (also clears MISS, END, MTE)</p> <p>This flag causes interrupt.</p>	<p>Error flag means that an error has occurred. An MMRS command will load AC bits 0-8 with status information. (END, MISS, mark track error (MTE) are only possible errors.)</p> <p>End status bit is set when tape reaches far end. Error flag is raised. Tape stops. Miss status bit is set when a data or block flag has not been cleared from previous use. Mark track error (MTE) status bit is set upon discovery of certain mark track and timing track errors.</p>	

SECTION 5

MAINTENANCE

Maintenance of the DECtape control and transport consists of procedures repeated periodically as preventive maintenance as well as corrective maintenance if equipment should malfunction. Maintenance activities require the items listed below in addition to standard hand tools, cleansers, and test cables and probes.

Test Instruments

Tektronix Scope
Type CA plug in
Type E plug in

Test Programs

Rocker
Exerciser
Microtog

PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the equipment and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks will forestall possible future failure by correcting minor damage and discovering progressive deterioration at an early stage. Data found during the performance of each preventive maintenance task should be recorded in a log book. Analysis of this data will indicate the rate of circuit operation deterioration and provide information to determine when components should be replaced to prevent failure of the equipment.

Cleaning

Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

Visual Inspection

Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC blue tweed paint number 5150-865 or DEC gray enamel number 3277-IR55. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring. Inspect the following for security: switches, knobs, jacks, connectors, transformers, fan, capacitors, lamp assemblies, etc. Tighten or replace as required. Inspect all racks of logic to assure that each module is securely seated in its connector. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors giving these signs of malfunction.

Marginal Checks

Marginal checks are performed to aggravate borderline circuit conditions within the control logic to produce observable faults. Therefore, conditions caused by marginal components can be corrected during scheduled preventive maintenance to forestall possible future equipment failure. These checks can be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors. By recording the level of bias voltage at which circuits fail, progressive deterioration can be plotted and expected failure dates predicted. Therefore, these checks provide a means of planned replacement. The checks are performed by operating the logic circuits from an adjustable external power supply, such as the DEC Type 730 Dual Variable Power Supply.

To perform the checks:

1. Set the switch on the marginal-check power supply to the +10 MC position.
2. Adjust the output of the marginal-check power supply so that the MARGINAL CHECK voltmeter indicates 10 v.

3. Start DECTape operation in a normal program or in a routine which fully utilizes the circuits in the rack to be tested. If no program is suggested by the normal system application, select an appropriate maintenance routine.
4. Set the top normal/marginal switch to the up position on the rack to be checked.
5. Decrease the volt marginal-check power supply output until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced, if desired.
6. Start operation. Then increase the volt marginal-check supply output until normal operation is interrupted, at which point record the marginal-check voltage. Transistors can again be located and replaced.
7. Return the top normal/marginal switch to the down position.
8. Repeat steps 2 through 7 for the center normal/marginal switch on the logic rack being checked.
9. Set the selector switch on the marginal-check power supply to the -15 MC position and adjust the output until the MARGINAL CHECK voltmeter indicates 15 v.
10. Repeat step 3.
11. Set the bottom normal/marginal switch to the up position for the rack to be checked.
12. Repeat steps 5 and 6; then return the bottom normal/marginal switch to the down position.
13. Repeat steps 1 through 12 for each module rack to be tested.
14. Adjust the output of the marginal-check power supply to 0 v and set the selector switch to the OFF position.

Maintenance Programs

Programs are available for detecting errors in the DECTape control and may be used with marginal checking. Microtog, consisting of five subroutines, is used with the PDP-4/7. The DECTape Rocker and Exerciser programs perform similar functions for the PDP-1. See Chapter 4 for a description of the maintenance routines.

Periodic Adjustment of Stop Time

A DECTape unit is commanded to stop by the action of energizing the stop relay. This relay has a single normally closed contact on it which carries the holding current to the go relay. Therefore, (after 15 msec) the go relay drops out followed, after a delay, by the timer relay. The time between go and timer dropping out defines a "stop pulse" which is caused to drive the trailing motor and stop the tape. If this stop pulse is too long, the drive reverses rather than stops, and if it is too short, the drive does not come to rest but coasts to a sluggish stop. The length of the stop pulse is determined by the charge on the capacitor in the filter network and by R2 which is in series with the timer relay coil. If the drive is only partially up to speed, a shorter stop pulse is desired. Otherwise, the long stop pulse will cause a reverse rather than a stop. For this reason, the charging resistor, R1, is included so that the capacitor charges up at approximately the same rate that the drive picks up speed in the first place. The procedure for adjusting R1 and R2 is now outlined.

To perform the adjustment:

1. Run the program which starts the drive and allows it to run for one second or more, and then commands stop, followed by a pause of one second and another run period of one second or more in the opposite direction. This program then causes the tape to rock in one direction, pause, rock in the other direction, etc. It assures that the capacitor across the timer relay has achieved full charge regardless of the setting of R1.
2. With this "long running time" program operating, adjust the appropriate potentiometers (see the DECTape Dual Transport 555 Manual) for a good abrupt stop in either direction over the entire reel.

3. Run the same program, but with the running times changed to 120 msec, to barely get started before commanding a stop (which should last for 1 sec as above), and adjust the appropriate short running time pot for good stop time. Repeat Steps 1 and 2 for checking purposes. The potentiometers are labeled R1 and R2 for the front left drive and R3 and R4 respectively for the front right drive.

CORRECTIVE MAINTENANCE

The equipment is constructed of highly reliable transistorized modules. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment down time due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. For corrective maintenance no special test equipment nor tools are required other than a broad bandwidth oscilloscope and a standard multimeter.

Troubleshooting Random Information Errors

A check for strobe timing is a good first step when troubleshooting random information errors. The position of the TP1 pulse generated from the timing track with respect to the information located on the information tracks determines the margins the system has for skew and amplitude variations. The TP1 (or strobe) should be centered on the information contained in the information channels. Unfortunately, this centering is primarily a function of parameters which are not controlled in the field. The main factors are: the gap width of the head, the velocity of the tape; and the switching time of the head.

To a lesser extent, however, the write current, tape tension, and the delays present in the reader and the writer do affect the strobe time.

For accomplishing this check the following procedure should be followed: Use a scope with a high gain differential preamplifier such as a Tektronix Type D or E. Also needed is a shielded cable with clip leads to connect the preamplifier to the tracks under consideration. Look at any particular information channel and sync on the timing track TP1's, or with a dual beam

scope, look at both the timing track output and this information signal. It is possible to see a bit of noise reflected onto the input of the information amplifiers because of timing pulses occurring at the output. This noise too, gives a good clue as to when the signal is being strobed.

Figure 5-1 Troubleshooting Diagram

Adjust the upper potentiometer of pair (RZ) with a long run time. Adjust the lower potentiometer of the pair for a short run time. Turn all potentiometers clockwise for a longer stop pulse (more abrupt stop).

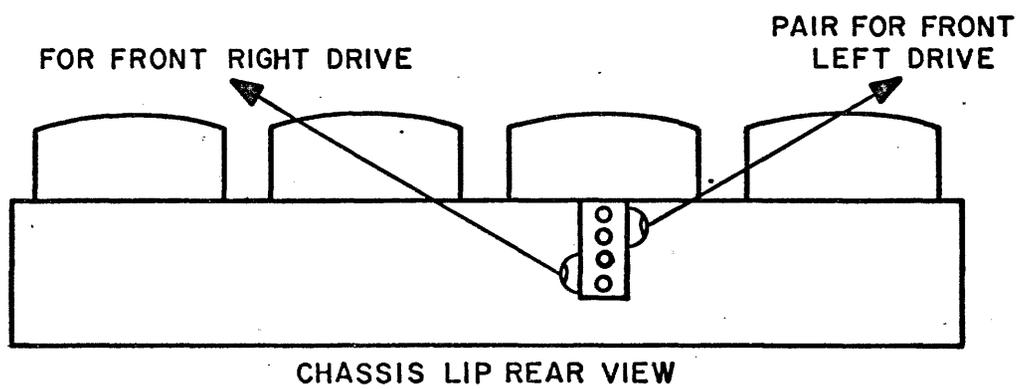
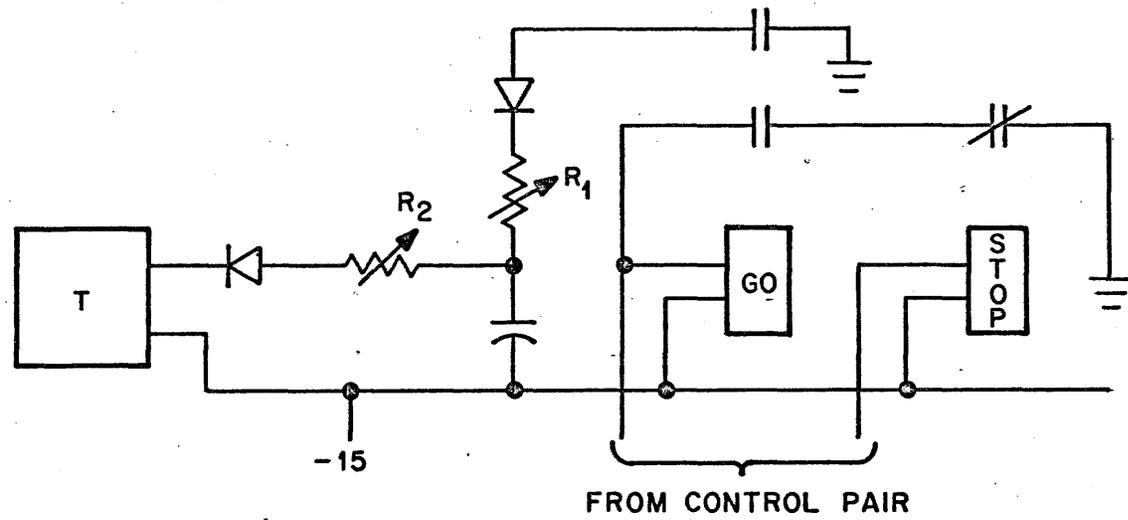


Fig 5-1

10 5-6

At the outset, the delay through the timing track amplifier should be measured and allowed for by checking the zero crossing of the input to the timing track amplifier and those at its output. If the output wave form is not of 50% duty cycle or if the two sides do not switch simultaneously for low level signals (use the attenuation plug to check), the timing track read amplifier knobs may have to be adjusted. It has never been necessary, however, to adjust these in the field. The time delay of the reader amplifier should be subtracted from the time delays observed in the next part of the procedure to achieve an honest appraisal of when the output of the information chart amplifiers will be strobed.

Interpreting the results:

<u>Cause</u>	<u>Result</u>
Strobe late when reading in the same direction as written and strobos early when reading in opposite direction	Write current too large Head response too fast Tape too slow
Strobos late in either direction	Timing track read amplifier delay too large

Circuit Troubleshooting

The procedure followed for troubleshooting and correcting the cause of faults within specific circuits depends upon the down time limitations of equipment use. Where down time must be kept at a minimum, it is suggested that a provisioning parts program be adopted to maintain one spare module or standard component which can be inserted into the cabinet when system troubleshooting procedures have traced the fault to a particular component. Following is a list of this type:

<u>Module No.</u>	<u>Spares Per Control</u>
4606	2
4221	1
4261	1
4523	2
4260	1
4228	2

Bench troubleshooting procedures can then be performed to correct the defective components. Where down time is not critical, the spare parts list can be reduced and signal tracing techniques can be utilized to troubleshoot modules within the equipment. This practice involves module removal by means of a Type 1960 System Module Puller, insertion of a Type 1954 System Module Extender into the logic rack, insertion of the suspect module in the module extender, and oscilloscope signal tracing of the module with the equipment energized and operating.

Static and dynamic circuit troubleshooting procedures may be performed at a bench. Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semi-conductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same, and no parallel paths exist, replace the diodes.

Measure the emitter-collector and emitter-base resistance of transistors. Most catastrophic failures are due to short circuits between the collector and the emitter or are due to an open circuit in the base-emitter path. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse direction. To determine forward and reverse directions a transistor can be considered as two diodes connected back-to-back. In this analogy PNP transistors are considered to have both cathodes connected together to form the base and both the emitter and collector assume the function of an anode. In NPN transistors the base is assumed to be a common-anode connection and both the emitter and collector are assumed to be the cathode.

Multimeter polarity must be checked before measuring resistances since many meters (including the Triplet 630) apply a positive voltage to the common lead when in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. A more reliable indication of diode or transistor malfunction is obtained by using one of the many inexpensive in-circuit testers commercially available.

Damaged or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at the wires or components around the connection, or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short durations, caused by an intermittent connection, can be detected by connecting a 1.5-v flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope while probing the connection.

Dynamic bench testing of modules can be performed through the use of special equipment. A Type 922 Test Power Cable and either a Type 722 or Type 765 Power Supply can be used to energize a system module. These supplies provide both the +10 vdc and -15 vdc operating supply for the module as well as ground and -3 v sources which may be used as signal inputs.

The signal inputs can be connected to any terminal normally supplied by logic level by means of eyelets provided on the power cable. Type 911 Patch Cords may be used to make these connections between eyelets on the plug. In this manner logic operations and voltage measurements can be made. When using the Type 765 Bench Power Supply, marginal checks of an individual module can also be obtained.

Repair

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When soldering semi-conductor devices (transistors, crystal diodes, and metallic rectifiers) which may be damaged by heat, the following special precautions should be taken:

- a. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.
- b. Use a 6-v soldering iron with an isolation transformer. Use the smaller soldering iron adequate for the work.
- c. Perform the soldering operation in the shortest possible time, to prevent damage to the component and delamination of the module etched wiring.

When any part of the equipment is removed for repair and replacement, make sure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective components only with parts of equal or greater quality and equal or lower tolerance.