

Engineering Change C Order Log

DQS11-C

DMA Controller

PROCESSOR TYPE PDP-11 Family

DQS11C-B0001 CODE: F ML: A WL: A

MAR-73 - PROBLEM: Received BCC character is not transferred to memory if it equals the SYNC code, 026 octal.

CORRECTION: OR the BCC enable signal with the negation of STRIP SYNC to enable an input data transfer. The ADD/DELETE's are as follows: DELETE A22D1 to B17F1 and A22B1 to A22D1. ADD A22B1 to A22D1, A22D1 to A18K2, B17E1 to A18H2, and B22M2 to A18J2.

In-plant effectivity -03 retrofit immediately

Field effectivity -Retrofit all DQS11-C's

(Time To Install And Test 1.0 Hour.) (Kit Contents -FCO/Prints)

DQS11C-C0002 CODE: F ML: B WL: B

MAY-73 - PROBLEM: Parity logic is not enabled for SYNC and EOT characters. Half duplex control is not employed within the DQS11-C option. CORRECTION: Incorporate parity on SYNC and EOT characters. Add CLEAR TO SEND and REQUEST TO SEND to control logic. Update prints.

In-plant effectivity -03 retrofit immediately Field effectivity -Retrofit all DQS11-C's

(Time To Install And Test 2.5 Hours.) (Documentation \$ 5.00 , Parts None) The DEC on-site labor charge will be the time required to install and test the FCO at the then current hourly rate. (Kit Contents - FCO/Prints)

DQS11C-E0003 CODE: F ML: C WL: C

NOV-73 - PROBLEM: The DQS11-C can only be initialized by SYSTEM INITIALIZE or a reset instruction.

CORRECTION: This is a product improvement fco; it adds an instruction to initialize the DQS11-C. Bit zero of the RECEIVE STATUS WORD performs a CLEAR AND GO function. Bit 7 of the RECEIVE STATUS WORD performs a RESUME function.

In-plant effectivity -Production break-in, #1708

Field effectivity -Retrofit DQS11-C's only upon customer request

(Time To Install And Test 1.0 Hour.) (Documentation \$ 5.00 , Parts None)

The DEC on-site labor charge will be the time required to install and test the FCO at the then current hourly rate. (Kit Contents -NF1091 -FCO/Prints)