digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

EC DEC-O-LOG Engineering Change Order Log

M8105

KB11-A Timing and Miscellaneous Control

PROCESSOR TYPE PDP-11/45

M8105-00001 CODE: D CS: B ETCH: C
MAR-72 - PROBLEM: Etch errors on revision "B " artwork of M8105.
CORRECTION: Correct etch and digitize board.
In-plant effectivity -02 phase-in

ETCH: D

M8105-00002 CODE: D CS: C
MAY-72 - CORRECTION: Change disable gate in priority arbitration.
In-plant effectivity -03 rework immediately

M8105-B0003 CODE: DF CS: D ETCH: E
AUG-72 - PROBLEM 1: **PIRQ LEV 1** request locks out "T " bit if PSW priority is at **LEV 1** .
CORRECTION 1: Remove **PIR LEV 1** from inhibiting "T " bit by cutting etch from E50 pin 5 to E46 pin 6 and adding jumper from E50 pin 5 to E50 pin 4.
CORRECTION 2: Correct print on TMCF .

NOTE: Existing diagnostics do not test the failing condition; a test program is included in the FCO.
In-plant effectivity -03 rework immediately , 9/11/72
Field effectivity -Rework all M8105's in PDP-11/45 systems.
(Time To Install And Test .8 Hour.) (Kit Contents -FCO/Prints)

M8105-00004 CODE: D CS: E
DEC-72 - PROBLEM: Not necessary to have 74S74-45 in E37.
CORRECTION: Replace E37 with 74S74.
In-plant effectivity -02 phase-in 1/1/73.

M8105-D0005 CODE: F CS: F
MAR-73 - PROBLEM: Parity errors are time consuming to detect through vector 4.
CORRECTION: Make parity trap to 114.

NOTE: The following FCO's must be installed in total to fully implement core parity: M8100-D0003, M8103-D0005, M8105-D0005, M8106-D0007, KB11A-D0015, and M8106-D0008. Each of these related FCO's may be installed separately; each FCO relies upon the others only to fully implement parity. Note that MS11-B/-C semiconductor parity memories with etch revision "B " M8110's will not function properly with the above FCO's installed. A new M8110 is being designed to allow proper operation with the FCO's installed.
In-plant effectivity -02 phase-in to Module Production March 1, 1973. Rework parity machines in Systems Checkout area and parity systems as required.
Field effectivity -Rework all M8105's in core parity PDP-11/45's
(Time To Install And Test 1.5 Hours.) (Kit Contents -FCO/Prints And Parts)

M8105-C0006 CODE: F CS: H
JUN-73 - PROBLEM: References to internal registers cause unnecessary data to be put on the UNIBUS.
CORRECTION: Disable **TMCD XX BYTE EN H** until master sync is asserted. The rework procedure is as follows: Cut etch from E15 pin 2, side 2; cut etch from third plated thru hole left of E05 pin 1, side 1; jumper plated thru hole connected to E09 pin 7 to plated thru hole right of E09 pin 7; jumper plated thru hole connected to E09 pin 1 to E16 pin 2; jumper plated through hole connected to E09 pin 2 to E07 pin 2; jumper E15 pin 2 to E15 pin 5; jumper plated thru hole connected to E09 pin 3 to third plated thru hole left of E01-05 ; insert IC type 74S00 in spare IC slot E9.
In-plant effectivity -03 * -Rework in module production and for test area immediately. Rework basics, systems, and field as needed. All shipments after August 6, 1973 will have this FCO.
Field effectivity -Rework CS revision "F " and earlier M8105's shipped prior to August 6, 1973.
(Time To Install And Test 1.0 Hour.) (Kit Contents -FCO/Prints And Parts)

M8105-C0007 CODE: F CS: J
OCT-73 - PROBLEM: The processor can hang in T2 and pause without **UBCA GET BUS 1 H** . This is because of a glitch on **RACH DIS BUST L** . If it is an MOS or bipolar system, it could get invalid address calculation.
CORRECTION: Create ROM decode of **BUST H** on the M8103 board. Jumper the new source of **BUST H** into M8105 logic. The rework procedure is as follows: Cut etch from E34 pin 08 on side 1. Jumper plated thru hole connected to pin CT2 to plated thru hole connected to pin DU2.

NOTE: This FCO must be installed in conjunction with FCO M8103-C0006.
In-plant effectivity -Rework in Module Production and Basic CPU Line. Rework in systems area and acceptance area only as necessary. Rework all boards in-plant as of November 1, 1973.
Field effectivity -Rework all M8105's in systems with MOS or bipolar memory and in systems that cannot be margined at 140 nsec.
(Time To Install And Test 1.0 Hour.) (Kit Contents -F1072 -FCO/Prints)

M8105-00008 CODE: D CS: K ETCH: F
NOV-73 - PROBLEM: MOS memory systems with KT11-C could pick up bits in MOS memory; the problem only occurs during KT11-C abort traps.
CORRECTION: Issue **TMCE BEND CLRL** to MOS control during the pause ROM cycle.
In-plant effectivity -Do not rework any existing boards. Phase-in change to create new etch revision "F " board by March 4, 1974.