



# INTEROFFICE MEMORANDUM

M1106

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SUBJECT CORE MEMORY EXPANSION FOR THE PDP-1

TO PDP Distribution List FROM Gordon Bell

## Introduction

Two core memory expansion methods are available for PDP-1. The Type 11 Memory System allows a PDP-1 to have a memory of up to 16,384 18-bit words, while the Type 14 system allows a total memory capacity of 32,768 words.

If memory Type 11 Control is used, three Type 12 memory modules may be added to make up the 16,384 words.

If type 14 memory control is incorporated, seven Type 12 memory modules may be added to form the 32,768 words.

Memory Type 11 should be used unless it is necessary to have a storage capacity of over 16,384 words.

## Type 11 Memory Switching

Two 3-bit registers address a memory field. In this case, each memory module contains two 2,048 word fields. Either one of two 3-bit registers; field A register (FA) or field B register (FB) selects one of eight, 2,048 word memory fields to be used. If bit 6 of the memory address register (MA) is a 0 when calling for a memory register, then FA selects the memory field. If MA-6 is a 1, then FB is used to select the memory field. Thus, memory references 0 - 2047 (0 - 3777 octal) come from Field A and references 2048 - 4095 (4000 - 7777 octal) come from Field B.

Two commands modify FA and FB. The first command is jump field, jfd Y, operation code 120000. This command uses the contents of memory register Y as a code word. When jfd Y is given, bits 5-17 of the contents of the memory register Y replace the program counter (PC), bits 0-2 replace FB, and bits 3-5 replace FA.

With jfd Y, the defer bit of the command has a special meaning. If the defer bit is a 0, then the contents of memory register Y replace FB, FA, and PC. If bit 5 is a 1, FB, FA, and PC replace the contents of the accumulator (AC), and the instruction proceeds

as stated above. The instructions, jsp, jda, and cal also place the previous contents of FB, FA, and PC in the accumulator.

The second command, change fields - cfd, has an operation code 72XX74, and requires 5 microseconds. When cfd is given, bits 6-11 of cfd replace the contents of the FB and FA registers, and the program counter is unchanged.

#### Type 11 High Speed Channel and Sequence Break Operation

When high speed channel transfers are involved, the high speed channel specifies a 14-bit address for one of 16,384 words.

When a sequence break interrupt occurs, FB and FA are both set to 0, and the previous contents of FB, FA, and PC are stored in the second register of the registers of the interrupt. The first and third registers of the interrupt receive the contents of the AC and IO, while the next instruction is taken from the fourth register.

A sequence break is terminated by giving jfd Y, where Y is one of the 16 registers holding FB, FA, and PC. FA, of course, must = 0.

#### Type 14 Memory Switching

Two 3-bit registers are incorporated in a PDP-1 for Type 14 switching. These two registers are the Data Field register (DF) and the Instruction Field register (IF). Each of these 3-bit registers address one of eight 4,096 word memory modules. A particular memory location, within a possible 32,768 ( $2^{12} + 3$ ) locations, is selected by using either the IF and Memory Address register (MA), or the DF and MA.

The memory address and the instruction field registers select the core memory register for all instructions. Similarly, if the instruction is deferred, the deferred addresses come from the MA and IF. The operand address (bits 5-17) of an instruction and the DF select the actual operand location in most cases. Only in the case of instructions jda Y, jfd Y, jmp Y and jsp Y is the address formed with the Y portion (MA) and IF.

Two commands are available to the programmer to allow memory field switching. The command, jump field, jfd Y, is the first command for memory switching. This command has an operation code of 120000, and is a two cycle instruction which does the following:

The contents of memory location Y are taken as an 18-bit memory selection code word. The program counter (PC) is reset to bits 5-17 of the code word, bits 0-2 replace the contents of DF, and bits 3-5 replace IF.

The defer bit used with jfd has special meaning. The defer bit specifies that the jfd is to save the previous contents of DF, IF, and PC. Thus, if the defer bit is a 1, the accumulator is cleared and the previous DF, IF, and PC contents are stored in the AC. If the defer bit is a 0, and jfd given, the accumulator is unaffected. Thus, jfd (no defer bit) and jfd (with a defer bit) are analogous to jmp and jsp.

The commands, jda, cal, and jsp, which are normally affected with the AC holding the previous PC contents, also receive DF and IF just as in the jfd (with a defer bit) case.

The second command, change data field - cdf, is used to change the contents of DF. This is a single cycle instruction with an operation code of 720X74. The command, cdf, changes only the data field register (DF) and does not affect the program counter or the IF register. Bits 9-11 of cdf specify the new contents of DF.

#### Type 14 High Speed Channel and Sequence Break System Operation

When high speed channel transfers are involved, the high speed channel specifies a 15 (12 + 3) bit address for one of the 32,768 words.

When a sequence break interrupt occurs, the previous DF and IF states must be stored. In this case, a sequence break to a channel means that the contents of the AC are stored in the first register of the break channel, IF, DF, and PC are stored in the second register, and the IO are stored in the third, and the fourth register contains the next instruction to be executed. The sequence break addresses are always taken from memory module 0. Thus, when a sequence break occurs, both IF and DF are set to 0. A sequence break is terminated by giving the jfd Y command, with IF = 0. Register Y must be one of the 16 registers holding IF, DF, and PC of the interrupt.

#### Example Of Programming

The following subroutines form  $c_i = a_i + b_i$ ,  $i = 1, \dots, n$ . The elements are stored continuously. The number of elements, 3.n, must fit into the available memory in all examples.

Three examples are given, the first assumes no field switching, the second is for Type 11, and the third is for Type 14.

The subroutines are overly general in that the matrices are assumed to be stored in different fields of memory, and may extend from field to field.

Both extra memory routines use subroutines which "fetch" the desired word from a possible  $2^{14}$  or  $2^{15}$  words, and these subroutines are called "setmem".

APPENDIX

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MATRIX ADDITION C(I) = A(I) & B(I).  I= 1,.....,N
, JSP  MATADD ,CALLING SEQUENCE
, R  N ,NUMBER OF ELEMENTS
, R&1 LOC  A ,LOCATION OF 1ST ELEMENT A
, R&2 LOC  B ,LOC B
, R&3 LOC  C ,LOC C
, R&4 ,RETURN
MATADD DAP  MATEND ,DEPOSIT RETURN
LAW  NCOUNT ,DEPOSIT PARAMETERS IN NCOUNT,....,&3
DAP  & & 2
LOOP LAC * MATEND ,BECOMES NCOUNT, A INDEX, B INDEX, C INDEX
DAP  MATEND
IDX  & - 2
SAS  LOOPTEST
JMP  LOOP
LAC  NCOUNT
CMA
DAC  NCOUNT
JMP  & & 2 , # OF ELEMENTS
NCOUNT 0
AINDEX LAC
BINDEX ADD
CINDEX DAC
IDX  AINDEX
IDX  BINDEX
IDX  CINDEX
ISP  NCOUNT
JMP  AINDEX
MATEND JMP
LOOPTEST DAP  NCOUNT & 4

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,MATRIX ADDITION - TYPE 11 - OPERATES IN FIELD B BRINGS DATA TO FIELD A  
 ,REQUIRES SUBROUTINES: CONVERT AND SETMEM

,R	JFD * MATADDW	,MATADDW IS CODE FOR CALLING SUB.
,R&1	LOC CODEA	,14 BIT ADDRESS FIRST ELEMENT OF "A"
,R&2	LOC CODEB	,14 BIT ADDRESS FIRST ELEMENT OF "B"
,R&3	LOC CODEC	,14 BIT ADDRESS FIRST ELEMENT OF "C"
,R&4	- N	,NUMBER OF ELEMENTS IN MATRIX
,MATADD	DAC MATEND	,RETURN
	JDA CONVERT	,RETURN MACHINE STATE
	DAC $\phi$ & 2	,THE FOLLOWING INSTRUCTIONS
	JDA SETMEM	,SETUP THE INITIAL VALUES FOR
	LOC	,INDICES
	LAC * FALOC	
	JDA CONVERT	
	DAC AINDEX	
	IDX FALOC	
	LAC * FALOC	
	JDA CONVERT	
	DAC BINDEX	
	IDX FALOC	
	LAC * FALOC	
	JDA CONVERT	
	DAC CINDEX	
	IDX FALOC	
	LAC * FALOC	
	DAC NCOUNT	,END SETUP
LOOP	JDA SETMEM	
AINDEX	0	
	LAC * FALOC	
	JDA SETMEM	
BINDEX	0	
	ADD * FALOC	
	JDA SETMEM	
CINDEX	0	
	DAC * FALOC	
	IDX AINDEX	
	IDX BINDEX	
	IDX CINDEX	
	ISP NCOUNT	
	JMP LOOP	
	LAW 4	
	ADD MATEND	
	DAC MATEND	
	JFD MATEND	
MATEND	0	,STORAGE FOR RETURN
NCOUNT	0	,NUMBER OF ELEMENTS

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,
,
,R
CONVERT
O
DAP CONEND
LAC CONVERT
RCL S6
SMA
RIR S3
RAL S1
RCR S7
CONEND JMP
,AC HAS 18 BIT CODEWORD FOR MACHINE STATE
,AC HAS 14 BIT CODEWORD FOR THE MEMORY REGISTER
,SELECTS EITHER FA OR FB FOR 3 BITS
,MAKE 11 BITS FROM 12
,AC CONTAINS 14 BITS - MEMORY REGISTER
,
,
,R
,R&1
,"FALOC" CONTAINS A NUMBER LESS THAN 4000 FOR CELL. FA IS SET TO BITS 4-7.
SETMEM
O
DAP SETEND
LAC * SETEND
AND FIELDMASK
DAC FALOC
XOR * SETEND
RAR S5
ADD THISCFD
DAC & 1
..
IDX SETEND
LAC SETMEM
SETEND JMP
THISCFD CFD 2000
FIELDMASK 3777
FALOC 0
,
JMP END.
,

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,MATRIX ADDITION - TYPE 14 -
,
      JFD * MATADD           ,CALLING COMMAND
      LOC A                 ,LOCATION OF 1ST ELEMENT OF MATRIX A
      LOC B
      LOC C
      - N                   ,NUMBER OF ELEMENTS
,REQUIRES SETMEM SUBROUTINE
MATADD      DAC MATEND
           LAW AINDEX
           DAP LOOP1
LOOP        JDA SETMEM           ,MATRIX PARAMETER PICKUP
           LOC MATEND           ,LOCATION OF 15 BIT CODEWORD
           ..                   ,BECOMES CDF
           LAC                 ,BECOMES LAC "ADDRESS"
           CDF x00              ,X IS THE FIELD OF THIS PROGRAM
LOOP1       DAC
           IDX MATEND
           IDX LOOP1
           SAS LOOPTEST
           JMP LOOP
,
LOOPMAT     JDA SETMEM           ,BEGIN MATRIX LOOP
           LOC AINDEX
           ..
           LAC
           CDF x00
           JDA SETMEM
           LOC BINDEX
           ..
           ADD
           CDF x00
           JDA SETMEM
           LOC CINDEX
           ..
           DAC
           CDF x00
           IDX AINDEX
           IDX BINDEX
           IDX CINDEX
           ISP NCOUNT
           JMP LOOPMAT
           JFD MATEND
MATEND      O                 ,STORAGE FOR RETURN
AINDEX      O                 ,LOCATION OF CURRENT ELEMENT
BINDEX      O
CINDEX      O
NCOUNT      O                 ,STORE NO. OF ELEMENTS
LOOPTEST    DAC AINDEX & 4
,
,SETMEM SUBROUTINE
,
      JDA SETMEM           ,AC/10 PRESERVED
,R          LOC CW         ,12 BIT LOCATION OF 15 BIT CODEWORD

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,R&1	..	,BECOMES CDF TO FIELD OF CW
,R&2	LAC	,INSTRUC (E.G. LAC) WHOSE ADDRESS IS CW
,RETURN IS R&1		
SETMEM	0	
	DAP $\phi$ & 1	
PICK	LAC	,PICK UP CODEWORD
	DAP CWPICK	
	IDX PICK	
	DAP SETEND	
	LAC * PICK	
	DAP CDFP	
	IDX PICK	
	LAC * PICK	
	DAP - INSTP	
CWPICK	LAC	
	AND SETM1	
	RAR S6	
	ADD CDFCON	
CDFP	DAC	
	LAC * CWPICK	
	AND SETM2	
INSTP	DAP	
	LAC SETMEM	
SETEND	JMP	
CDFCON	CDF	
SETM1	70000	
SETM2	7777	