

dec

PERMANENT
MEMORANDUM

M 1130

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SUBJECT Instruction Test Programs
TO Technicians, PDP-1 Distribution List

ABSTRACT A series of small diagnostic routines for checking memory reference and augmented instructions. Each routine is written using the program format for PDP-1 maintenance programs (see memo - 1127).

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INTRODUCTION

The following routines are written in sequential order starting with a basic set of instructions, that are assumed working, and branching out into different areas of the machine using these instructions to analyze other instructions.

OPERATING INSTRUCTIONS

To start each test, ss #1 must be off. With ss #2 on, each routine will iterate about itself provided ss #1 is off. SS #2 off, the following routine (in read-in-mode format) on tape, will be read in. All Frap symbols used, are defined in memo - 1127.

,TEST 1

,clear memory

,9/15/61
,G. B. & S. L.

org 7762

be0 szs 10
ph0 hlt
dzm * t1
idx t1
sas p0
jmp be0
f10 rpb
dio p0
spi *
rpb
p0 7762
jmp f10
t1 0
end .

,TEST 2

,skip spa sma szs 1 2 3 hlt cma cla test don't skip uses jmp
,partially tests sza

,9/15/61
,G. B. & S. L.

be1 szs 10
ph0 hlt
cla
sza
er0 hlt *,0 no good
sza * ,0 no good
pl jmp p0
cma
sza

```
650000 ,end sza check
er1      hlt
          cma
          sza
er2      hlt
          spa
er3      hlt
          cma
          spa
650000
er4      hlt
          sma
er5      hlt
          cma
          sma
650000
er6      hlt
fil       szs 20
          jmp be1
          rpb
          dio $ & 3
          spi *
          rpb
          o
          jmp fil
p0       szs 30
ph1       hlt
          jmp pl
end .
```

,TEST 3
,test for all lac dac idx and addl sas also uses jmp hlt
,9/17/61
,G. B. & S. L.

```
be2      szs 10
          hlt
          lac t1
          dac p2
          cla
          dac t3
          dac t4
          jmp p2
p1       idx t4
          lac t3
          add tb3 & 1
          dac t3
          sas t4
eh1      hlt
          sza *
          jmp p3
          sas
p2
```

```
jmp p1
idx p2
jmp p1
t3      0
t4      0
tb3      0
          1
          3
          7
          17

          37
          77
          177
          377
          777
          1777
          3777
          7777
          17777

          37777
          77777
          177777
          377777
          777777
t1      sas tb3
t2      sas tb3 & 2
p3      lac p2

          sas t2
          hlt
f12      szs 20
          jmp be2
          rpb
          dio f & 3
          spi *
          rpb
          0
          jmp f12
end .
```

,TEST 4
,add sub lio dio sas sza lac jmp isp test szo dac hlt idx dap spi
,9/14/61
,G. B. & S. L.

be3 szs 10
 hlt
 law tb5
 dap p5
 dzm t1
 dzm t2
 dzm t3
 dzm t4

p2
dzm t5
dzm t6
lac t7
dac p6 & 1

p3
lac t10
dac p6 & 2
lac t1
add t11
szo *

jmp φ & 3
sas t13
hlt
dac t1
lac t11

add t2
szo *
jmp φ & 3
sas t13
hlt
dac t2
lac t3
sub t12
szo *
jmp φ & 3
sas t13
hlt
dac t3
lio t3
dio t4

t7
idx t5
sas t4
hlt
sas t3
hlt
sas t2
hlt
sas t1

p6
hlt
isp t6

0

p5
0
sas

jmp p3
sza *
~~jmp p13s6~~
~~sas t14~~
~~jmp p7~~
lac t10
dac p6 & 1
lac t7
dac p6 & 2
jmp p11
spi *

p7 jmp p10
 spi *
 jmp p11
 sas t12
 jmp p3
 idx p5
 jmp p2
p11 idx p5
 jmp p3

fi3 szs 20
 jmp be3
 rpb
 dio & 3
 spi *
 rpb
 0
 jmp fi3
t1 0

t2 0
t3 0

t4 0

t5 0
t6 0
t10 jmp p6 & 3
t11 1
t12 777776
t13 400000
t14 377777
tb5 1
 2
 3
 4
 7
 10

 17
 20
 37

 40
 77
 100

 177

 200

 377
 400
 777

1000
1777
2000
3777
4000

7777
10000
17777
20000
37777
40000
77777

100000
177777
200000
377777
400000
777776
000000

end .

,TEST 5
,ior xor & and test

,9/14/61
,G. B. & S. L.

be4 szs 10
 hlt

 law tb1
 dac t1
 law tb2
 dac t2
p0 lac * t1
 ior * t1
 sas * t1
 hlt
 lac * t1
 ior * t2
 cma

 sza
 hlt
 lac * t2
 ior * t1
 cma
 sza
 hlt

 lac * t2
 ior * t2
 sas * t2

hlt
hlt
lac * t1

and * t1
sas * t1

hlt
lac * t1
and * t2
sza

hlt
lac * t2
and * t1

sza
hlt
lac * t2

and * t2
sas * t2

hlt
lac * t1
xor * t1
sza

hlt
lac * t1
xor * t2

cma
sza
hlt
lac * t2
xor * t1
cma
sza
hlt
lac * t2
xor * t2
sza

hlt
idx t1
idx t2
sas t3

fi4
jmp p0
szs 20
jmp be4

rpb
dio & 3
spi *

rpb
0
jmp fi4
t1
0

t2 0
t3 tb2 & 23
tbl 0
1
2
4
10
20
40
100
200
400
1000
2000
4000
10000
20000
40000
100000
200000
400000
tb2 777777
777776
777775
777773
777767
777757
777737
777677
777577
777377
776777
775777
773777
767777
757777
737777
677777
577777
377777
end .

,TEST 6

,jmp jsp jda test

,9/20/61

,G. B. & S. L.

org 7721
be5 szs 10

hlt
dzm t1
law 1
dap t2
lac t2

dac * t1
idx t2
idx t2
idx t1
lac t4
dac * t1
idx t1

lac t2
dac * t1
idx t2
idx t2
idx t1
lac t3

dac * t1
idx t1
sas t5

jmp be5 & 5

jmp p2~~t~~ & 1

p1 0 ~~p2~~ dap p2 ~~.....~~

sas t1

hlt

idx t1
idx t1

sas t5
jmp
law 2
dac t1

p2

fi5 szs 20
jmp be5

rpb
dio & & 3
spi
rpb
0
jmp fi5
t1
t2
t3
t4
t5
be5 - 1
end .

,TEST 7
,cal test
,9/25/61
,G. B. & S. L.
org 100 0
dap p0

sas t1
hlt
sad t2
jmp p4
idx t1
sas t3

p0 jmp
fi6 szs 20
jmp be6
rpb
dio & & 3
spi *

rpb 0
jmp fi6
add t4
dac t1

p4 idx t1
jmp po
szs 10
hlt dzm t1
be6 idx t1
sad t2
jmp p1
sad t3
jmp p3

p2 ior t6
 dac * t1
 jmp p5
p1 add t4
 dac t1
 jmp p2
p3 dzm t1

 idx t1
 idx t1
 lac t5
 dac 77
 jmp 1

t3 7777
t6 160000

t1 0
t2 77
t4 60
t5 jmp 157
end .

,TEST 8
,simple ac & io shift rotate test
,9/21/61
,G. B. & S. L.

be7 szs 10
ph1 hlt
 lac t1
 dac t2

 lio t2
 ril s9
 ral s9

eh1 dio t3
 sas t3
 hlt
 rir s9
 rar s9
 sas t2
eh2 hlt
 dio t3
 sas t3
eh3 hlt
 sal s9

eh4 sil s9
 dio t3
 sas t3
 hlt
 lac t2
 lio t2
 sar s9
 sir s9
 dio t3
 sas t3
eh5 hlt
 idx t1
 sza
 jmp be7
fi7 szs 20
 jmp be7
 rpb
 dio \$ & 3
 spi *
 rpb
 0
 jmp fi7
t1 0
t2 8
t3
end .

,TEST 9
, super rotate test
, 9/20/61
,G. B.
be10 szs 10
p17 hlt
 law 1
 dac p05 , base initialize
p13 law tb2~~base~~
 dap p11
 dap p12 ,setup
p16 cla cma cli ,test that it does move
 rcr s9
 rcl s1
 rcr s1
 ral s2
 rar s1
 rir s9
 ril s1
 dio p06
 sas p06

hlt
rir ,test for zero rotate
rcr
ril
ril
rcr
rar
rcl
ral
ral
dio p06
sas p06
hlt
p11
lac
lio
jda p00
rar
sas * p11
hlt

dio p06
sas p06
hlt ,finish rar
lac * p11

lio * p12
jda p00
ral
sas * p11
hlt
dio p06
sas p06
hlt ,finish ral
lac * p11
lio * p12
jda p00
rir
sas * p11
hlt

dio p06
sas p06 ,rir done

lac * p11
lio * p12
jda p00
ril
sas * p11
hlt
dio p06
sas p06

hlt ,ril done
lac * p11
lio * p12
jda p00
rcr
sas * p11
hlt
dio p06
sas p06 , rcr done
lac * p12
lio * p12
jda p00
rcl
sas * p11
hlt
dio p06
sas p06
hlt ,rcl done
idx p12
idx p11
sas p14
jmp p16
idx p05
sas p15
filo szs 20
jmp bel0
rpb
dio & & 3
spi *
rpb
0
jmp filo
jmp p01 0 ,temp for residue
p05 8 ,base for command
p02 0 ,ac
p00 dap p01 ,return
lac * p01
dac p02
idx p01 p03 ,return
law p03 dap p08 ,to put commands away
law 44 36
p07 dac p06
lac p06
sub p05
spa
jmp p09

dac p06
law p04
add p05
dap & 1

lac
add p02
dac
idx p08

jmp p07
law p04
add p06
dap & 1
lac
add p02
dac * p08
idx p08
lac p10
dac * p08
lac p00
0 46
&
org p03
jmp
0
s1
s2
s3
s4
s5
s6
s7
s8
s9

p15 l2
p14 lac tb2 & 5
tb2 0

- 0
525252

252525
end .

,TEST 10
,shift test law dap isp ior rar idx
,9/22/61
,S. L.
bell szs 10
hlt
law p5

dap p4
law tb1
dap p1

law tb3

dap p5
law tb4

dap p6
law * 3
dac t1
law tb2
dap p2 & 2

p1
law
dap p7
idx p1

isp t1
jmp p2
sad t2
jmp ~~fill~~
sad t12
jmp p14
law p7 - 4
dap p4
law t10
dap p11

p2
dap p12
law * 7
dac t3
lac

dac p10
dac t4
idx p10

idx p2 & 2

p4
isp t3
jmp
jmp p1 - 2

p14
law t11
jmp p2 - 2

p5
law
dap p11

p6
idx p5
law
dap p12
idx p6
law 1
dac t5

	law * 11
	dac t6
p7	lac
	lio * p7
p10	
p11	sas
e_h1	hlt
	dio t7
	lac t7
p12	sas
eh2	hlt
	lac t5
	ral s1
	dac t5
	ior t4
	dac p10
	isp t6
	jmp p7
	jmp p2 & 2
fill	szs 20
	jmp bell
	rpb
	dio φ & 3
	spi *
	rpb
	0
	jmp fill
t1	0
t3	0
t4	0
t5	0
t6	0
t7	0
tb1	252525
	525252
t10	000000
t11	777777
tb2	sal
	sar
	sil
	sir
	scl
	scr
tb3	252525
	525252

252525 252525
 125252
 125252

 652525

 652525

 525252

 525252
 652525
 652525

t2 2
t12 1
tb4 252525
 252525
 125252
 125252
 525252
 525252
 525252
 525252
 652525
 652525
 252525

 252525

end .