EK-MH10-MM-003

MH10 Maintenance Manual

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CHAPTER 1
INTRODUCTION

This chapter contains a general functional description of the MH10 Core Memory. It includes a system level description of the logic, a physical description, and general design specifications.

1.1 GENERAL DESCRIPTION

The MH10 (Figure 1-1) is a coincident-current, ferrite-core, 3-D, 3-wire memory, storing up to 262,144 37-bit words (36 data bits plus 1 parity bit) with a cycle time of 1.2 μs. The MH10-G is the basic system and is capable of storing 64K word locations (65,536 actual locations). The MH10-E option is a 64K expansion unit, which, when installed in a basic MH10-G, yields a 128K MH10-H. Two MH10-E options installed in an MH10-H yield a 256K MH10-L. As many as 16 memory units may be physically connected to the memory bus.

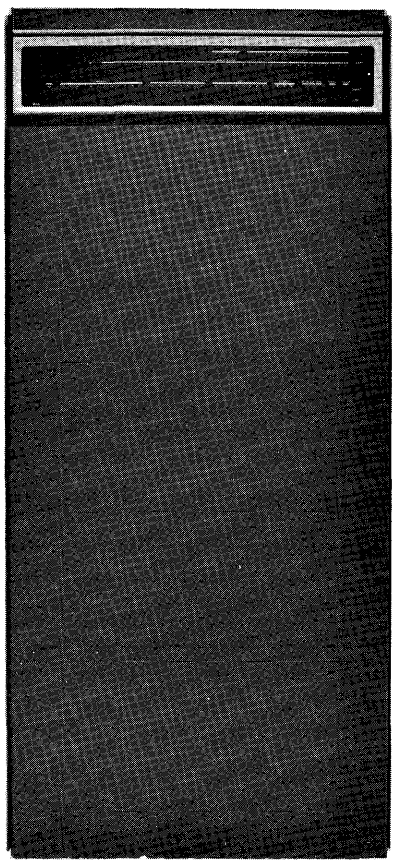


Figure 1-1 MH10 Core Memory

1.2 SYSTEM LEVEL DESCRIPTION

The operation of the MH10 within the DECsystem-10 is asynchronous; that is, access to memory units is governed by a "request/response" system, wherein the processor makes a memory cycle request and waits for a response from a memory unit. Communication between processor and memory units takes place over the memory bus. Each processor in the system has an associated memory bus which is connected to an active port in each memory unit.

A memory unit may contain a maximum of eight access ports; each port is associated with one particular processor, data channel, multiplexor, etc. (Figure 1-2). If an MX10 Memory Data Multiplexor is included in the system, as many as eight DF10 Data Channels may be associated with one memory port. The MC10-G Additional Access Port option provides two additional access ports to MH10 memories that do not utilize all available access ports. Priority logic contained in each memory unit designates the sequence in which the processors are granted access in the event of simultaneous requests.

MH10s are compatible with all DECsystem-10 memories and processors. Two-way interleaving is provided within a single MH10 cabinet, and four-way interleaving is performed between two MH10 cabinets. Each unit, however, must contain equal amounts of storage. Interleaving rotates successive memory cycles between the interleaved memory units if the addressing is sequential. Operation in this mode effectively decreases cycle time, which, in turn, reduces processor idle time.

The MH10 incorporates additional features that allow for smooth degradation of memory performance and ease in checking malfunctions. A select switch is provided for each 64K bank of memory. A deselected bank is logically placed into the highest address range in the cabinet, while other previously higher banks are automatically pushed down, so that no hole appears in the address base within a cabinet. Thus, a core stack malfunction results in less core being available, rather than immediately having to power down the cabinet to replace the malfunctioning stack; the latter can be replaced at the next scheduled maintenance time.

The MH10 contains data parity checking logic for checking data being read out of memory and being written into memory. If a parity error is detected, the address, data, ACTIVE, RD RQ, and WR RQ indicator lights are frozen without affecting regular MH10 operation. If the STOP switch is ON, the particular control with which the error is associated is halted.

1.3 PHYSICAL DESCRIPTION

The MH10 is housed in a standard PDP-10 cabinet (Figures 1-1 and 1-4). The major physical differences in the MH10 and many earlier DECsystem-10 memories are:

1. Higher storage capacity
2. Up to eight access ports available.

The use of Quick Latch bus connectors provides low maintenance and fast, easy attachment of the bus cable to the eight access ports (P0–P7) located at the lower rear of the logic frame (Figure 1-3). Two physical connectors (in/out) are associated with each port. They are wired in parallel, allowing Pn of one unit to be daisy-chained to the respective Pn of the next unit. These ports are the electrical inputs and outputs for the memory bus and the MH10.

The MH10 is divided into two major logic sections: the Core Memory and Control (CMC) section and the Port Control and Core Interface (PCCI) section. The CMC section is further subdivided into two separate controllers (C0 and C1), selected by address bits 20 (0) and 20 (1), respectively. The CMC and PCCI sections are connected by four BC20-D cables, as shown in Figure 1-5.

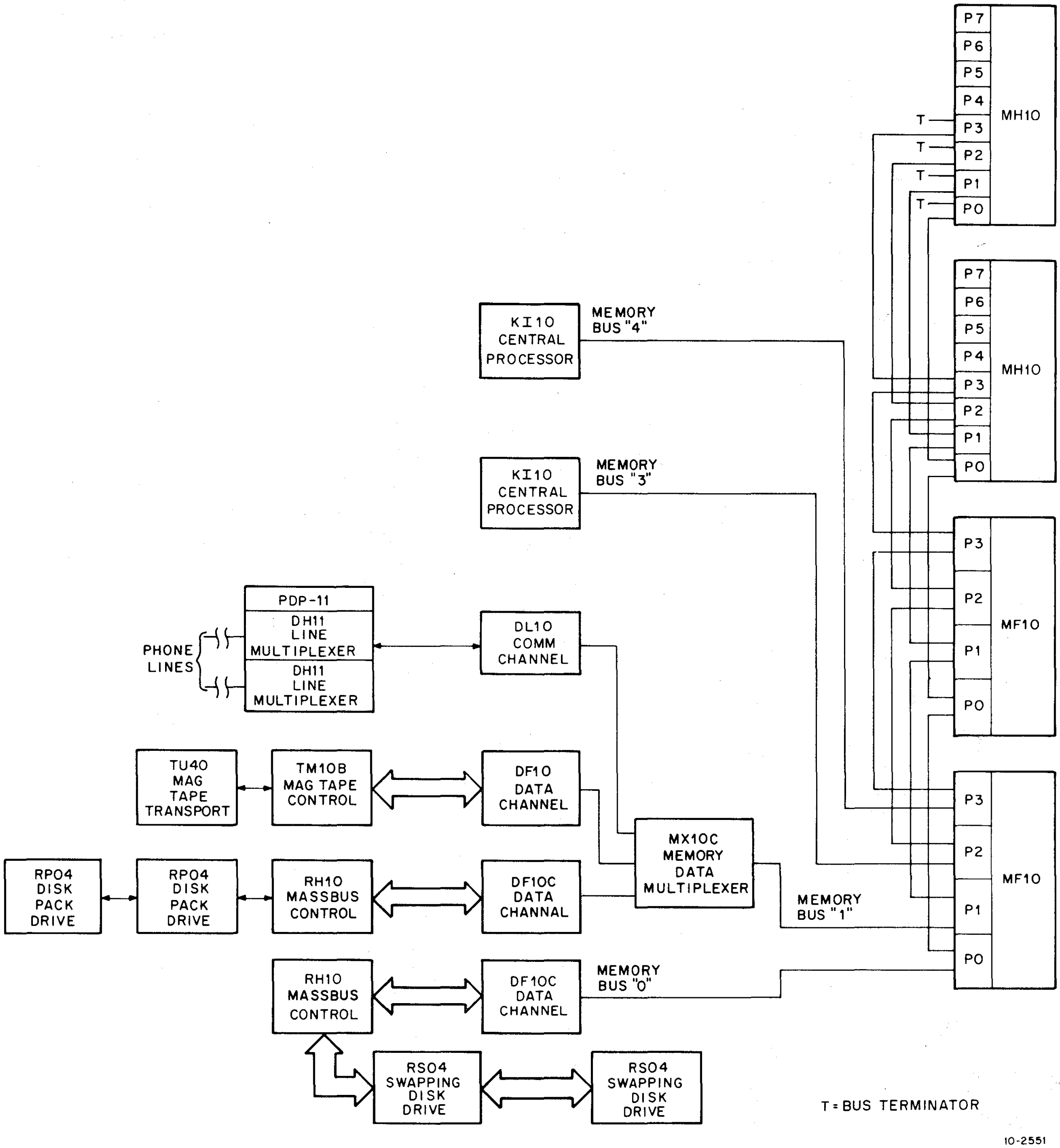


Figure 1-2 Typical System Diagram

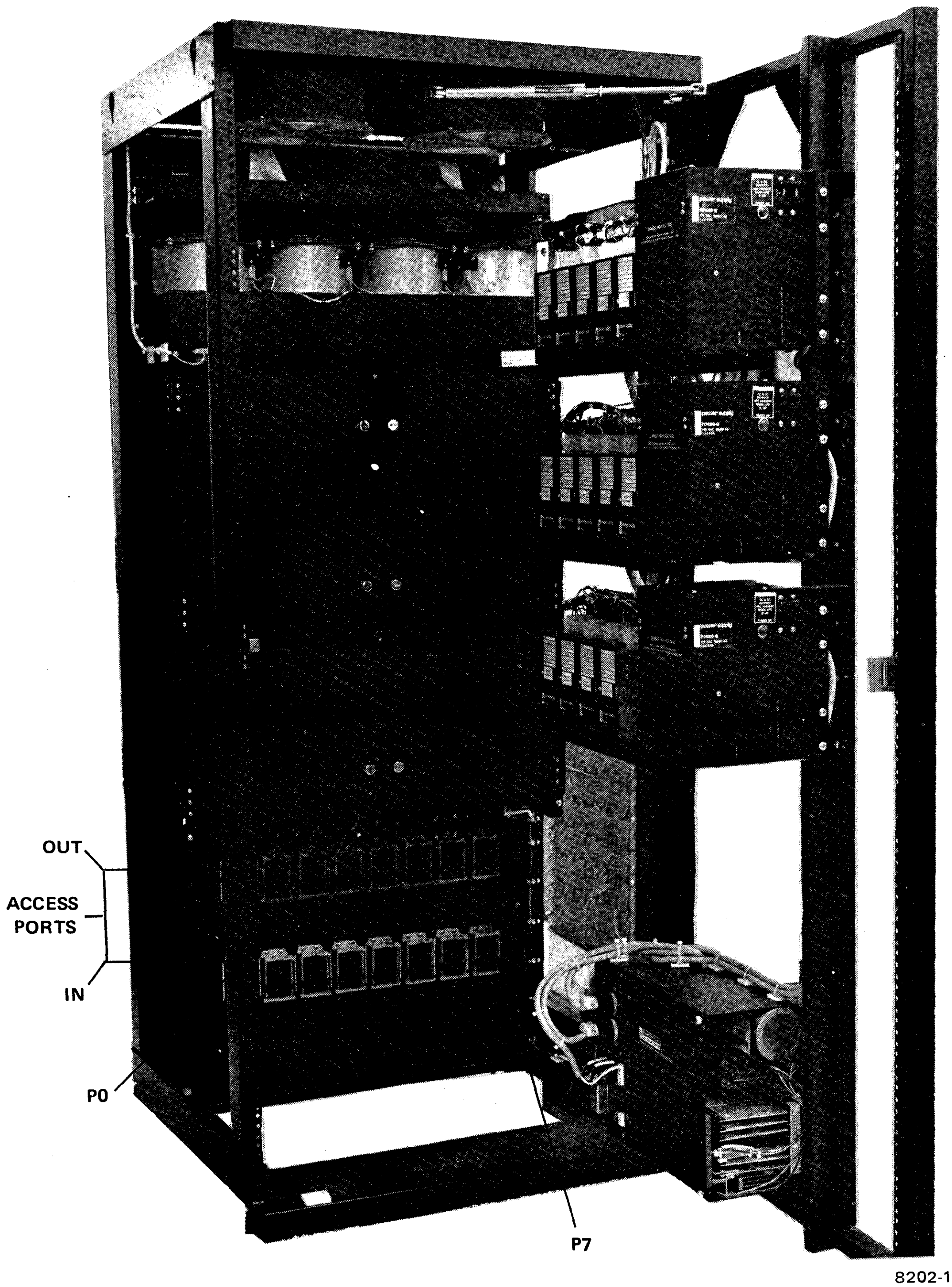


Figure 1-3 MH10 Rear View (Access Ports)

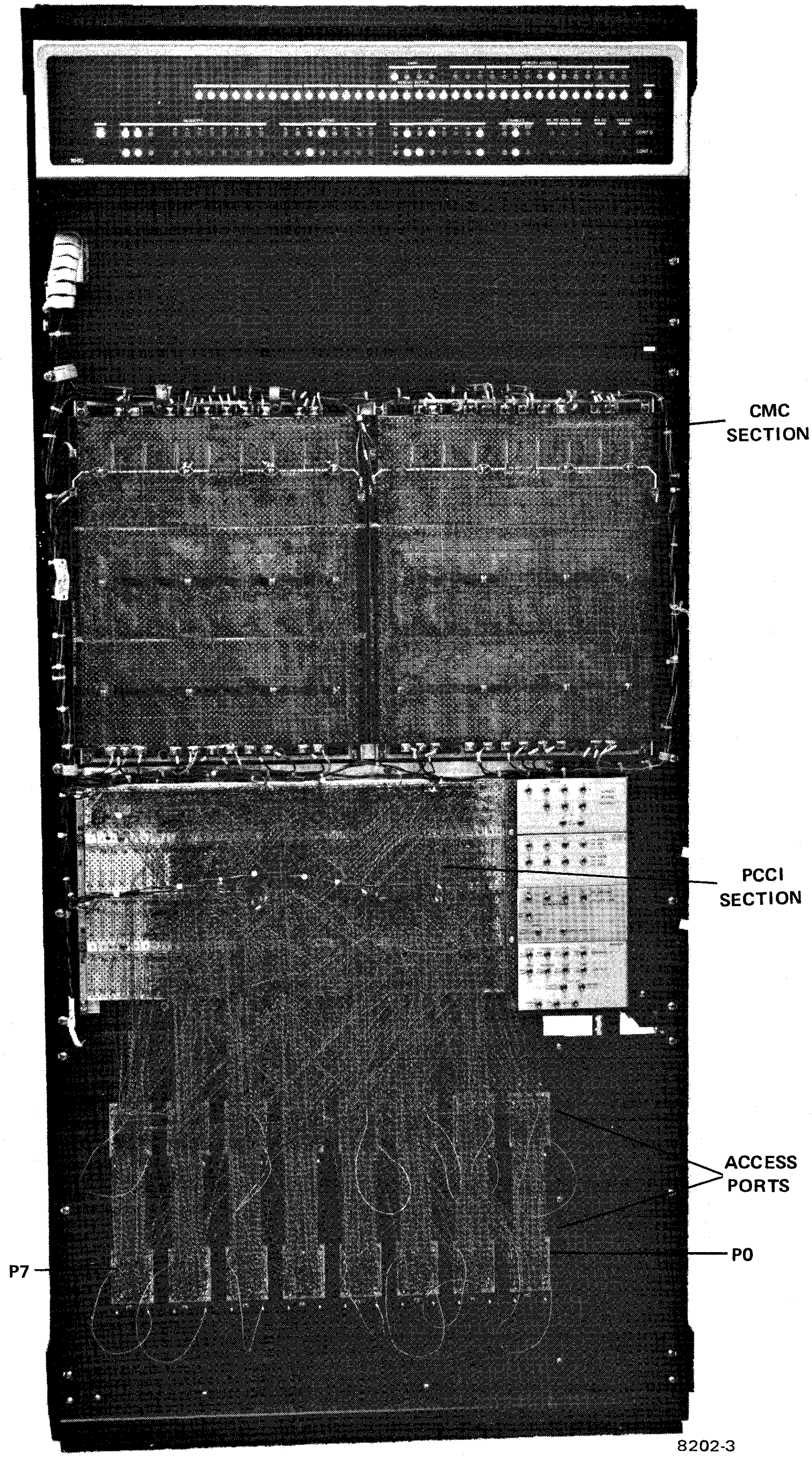


Figure 1-4 MH10 Core Memory, Front View (Door Off)

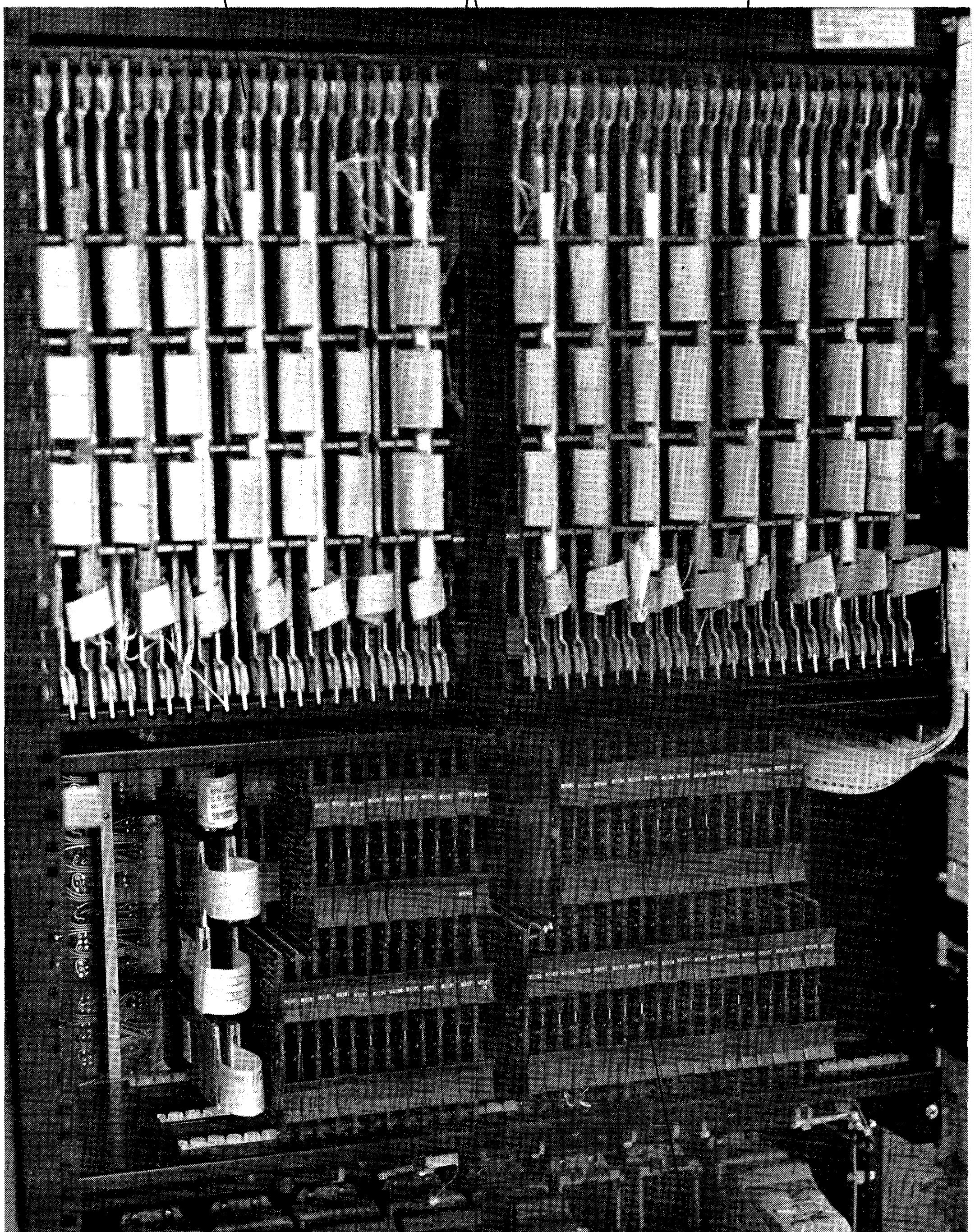


Figure 1-5 MH10 Core Memory, Rear View (Logic Section)

1.4 SPECIFICATIONS

The MH10 Core Memory general specifications are listed in Table 1-1.

Table 1-1 Specifications

Characteristics	Specification
Power Requirements	208Y/120 Vac +6%, -12%, 60 Hz ± 1 Hz 380Y/220 Vac +6%, -12%, 50 Hz ± 1 Hz 416Y/240 Vac +6%, -12%, 50 Hz ± 1 Hz
Line Current, 60 Hz	20 A; 175 A inrush for one cycle
Line Current, 50 Hz	10 A; 90 A inrush for one cycle
Power Dissipation	2400 W
Internal Logic Potentials	
Positive Logic Negative Logic Stack Voltage	0 V to +3 V -3 V to 0 V +5 V, +20 V, and -5 V
Power Interrupt	Up to 20 ms with no effect on operation No loss of stored data at power ON/OFF
Cycle Time	1180 ns
Read Access Time	735 ns maximum, excluding cable delay
Address Acknowledge Time	230 ns maximum, excluding cable delay
Word Length	36 bits plus parity bit
Memory Size	
MH10-G MH10-H MH10-L MH10-E	65,536 words 131,072 words 262,144 words 65,536 words, expansion from MH10-G to MH10-H. Two MH10-E options are required to expand an MH10-H to an MH10-L.
Access Ports	Eight maximum; simultaneous access by any two ports of each memory half. The MC10-G Additional Access Port option provides two additional access ports to MH10 memories that do not utilize all available access ports.
Interleaving	2-way within one cabinet 4-way between two cabinets

Table 1-1 Specifications (Cont)

Characteristics	Specifications
Dimensions	
Height	1.83 m (72 in)
Width	0.84 m (33 in)
Depth	0.76 m (30 in)
Weight	409 kg (900 lb)
Operating Temperature	15° to 35° C (60° to 95° F)
Storage Temperature	5° to 45° C (40° to 110° F)
Relative Humidity	20% to 80%
Heat Dissipation	1960 kcal/hr (7800 Btu/hr)

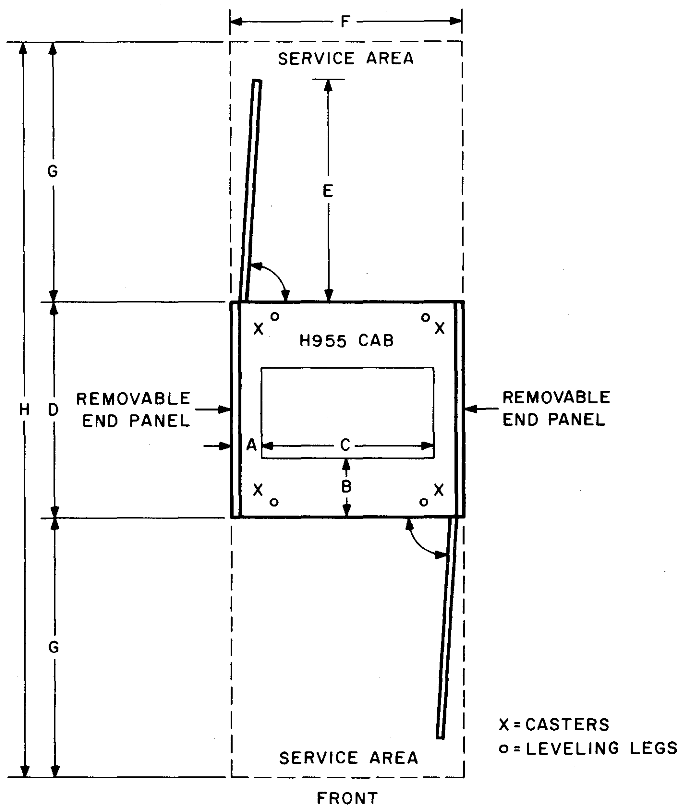
CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter, used with the *PDP-10 Site Preparation Guide* and the engineering drawings provided with each unit, contains the information required for MH10 installation.

2.2 SITE PREPARATION

No special site requirements exist other than those dictated by environmental conditions (Table 1-1) and service clearances (Figure 2-1). Subflooring is not normally required. The units are free standing; up to four units may be bolted together. The memory unit installed closest to the CPU should not be separated from it by more than 0.914 m* (3 ft) or less than 0.635 cm (1/4 inch).



DIMENSIONS	A	B	C	D	E	F	G	H
METERS	0.09	0.19	0.61	0.76	0.79	0.8	0.91	2.6
INCHES	3.7	7.5	24	30	31	31.5	36	102

10-0869

Figure 2-1 MH10 Core Memory Service Clearance

* Speedy, the processor timing program, is written for the standard 10-ft memory bus cable connection between the CPU and the first memory unit. If lengths in excess of 10 ft are used, Speedy timing printouts will not agree with the timing specification.

2.3 INSTALLATION PROCEDURE

After removing the equipment packing material, visually inspect the exterior and interior of the equipment: inspect external surfaces for surface, bezel, switch, and light damage; caved-in doors; or other signs of the damaged equipment. Internally inspect the cabinet for any obvious cable damage; loose or broken modules; fan damage; and loose nuts, bolts, or screws. Ensure that all modules are properly seated.

2.3.1 Cabling

All cables enter or leave the memory unit through an access cutout at the bottom of the cabinet. Figure 2-2 illustrates a system configuration with cabling data.

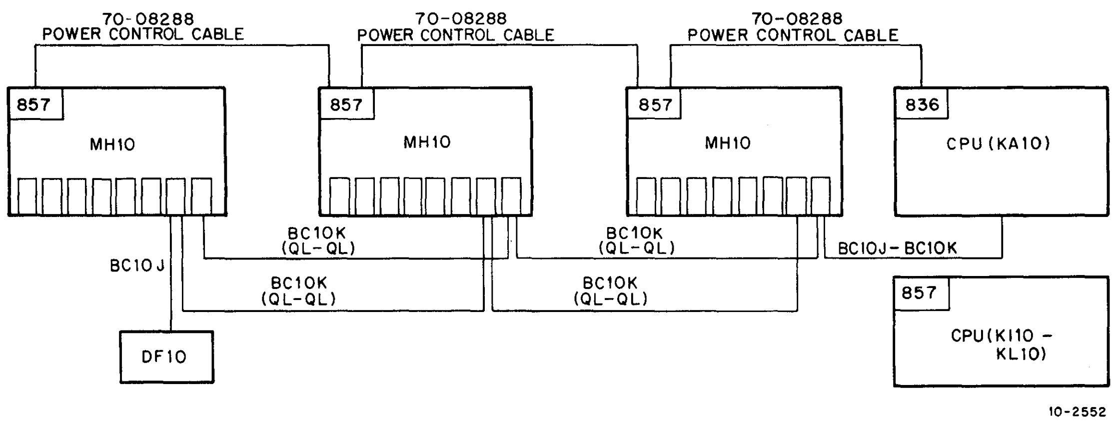


Figure 2-2 MH10 Cabling

2.3.1.1 Memory Bus - One memory bus cable is required to connect the unit to a processor or to another memory unit if more than one unit is included in the system. Two memory bus cables are included for each MC10-G Access Port option (all access ports are optional), with a maximum of eight ports per unit. The maximum allowable physical length of the memory bus is 100 ft, including wire-runs through each memory unit. The memory bus must be terminated in the last memory unit in the system using one H866-type terminator per access port.

CAUTION

Do not force connection when installing memory bus cable with Quick Latch cable connector.

2.3.1.2 AC Power - Each 60-Hz MH10 unit is furnished with a 3-wire ac power cable with the Hubbell 2611 Twist-Lok™ plug to be mated with a Hubbel 2610 receptacle. For 50-Hz users, a Hubbell 2321 Twist-Lok plug is mated with a Hubbell 2320 receptacle. Ensure that the power supplies are jumpered for the appropriate line voltage (115 or 230 Vac). Appropriate jumper configurations are shown on the power supply label.

™ Twist-Lok is a trademark of Harvey Hubbell, Inc.

2..3.1.3 Power Control – The 857 power controls in all cabinets must be interconnected to enable central control of POWER ON/OFF from the PDP-10 console power switch. Three Mate-N-Lok connectors on each 857 power control are used for interconnection via a 3-wire bus (Figure 2-3). One 3-wire bus cable is supplied with each cabinet to connect the 857 power control to the 857 power control in the next cabinet. Because each power control must connect to the power controls in the preceding and following cabinets, two Mate-N-Lok connectors are reserved for the intercabinet bus. A third connector is provided for connection to the cabinet-mounted thermal switches and to the PDP-10 console power switch.

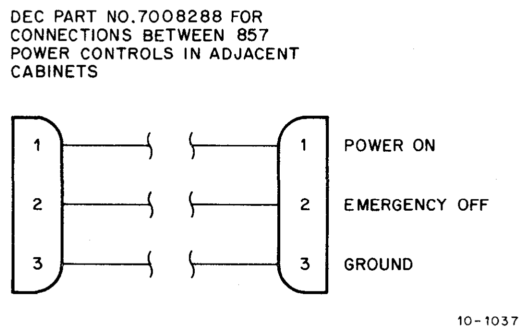


Figure 2-3 Remote Power Control Cable

If remote control is desired, ensure that the REMOTE/LOCAL toggle switch on the 857 power control is in the REMOTE position before operating the MH10 on-line with the processor. Also ensure that the ac line voltage select switch on the 857 power control selects the proper ac line voltage level (115 Vac or 240 Vac position).

2.3.1.4 Ground Mesh Cable – Connect a No. 4 gauge wire from the copper bolt on the bottom of the MH10 cabinet to the adjacent cabinet(s).

2.3.2 Memory Address Switch Settings

The MH10 port address must be established prior to memory operation. The port address is established via the LOWER BOUND ADDRESS toggle switches located on the Memory Maintenance panel. Table 2-1 lists the address switch settings for a typical system having eight 256K MH10-L memories connected to one KI10 or KL10 processor.

NOTE

If the KA10 processor is used, only one MH10-L memory can be connected to the memory bus.

Note that KA10-based memory systems are limited in size. This limitation is dictated by the memory addressing capability of the KA10 (256K word locations). The 3-position PORT SELECTION switch, relative to the KA10 in the system, is placed in the "KA" position. This causes the MH10 to ignore memory address bits 14–17.

When 128K MH10-H memories are connected to the memory bus, a maximum of two memories can be connected to a KA10 processor memory bus due to the KA10 memory size limitation. Table 2-2 lists the address switch settings for a switch having eight 128K MH10-H memories connected to a KI10 memory bus.

Table 2-1 MH10 (256K) Memory Address (Lower Boundary) Switch Settings

Memory Address	MH10-L No.	Memory Address (Lower Boundary) Switch Settings 14	15	16	17	18	19	20
00000000–00777777	0	0	0	0	0	0	0	0
01000000–01777777	1	0	0	0	1	0	0	0
02000000–02777777	2	0	0	1	0	0	0	0
03000000–03777777	3	0	0	1	1	0	0	0
04000000–04777777	4	0	1	0	0	0	0	0
05000000–05777777	5	0	1	0	1	0	0	0
06000000–06777777	6	0	1	1	0	0	0	0
07000000–07777777	7	0	1	1	1	0	0	0

Table 2-2 MH10-H (128K) Memory Address (Lower Boundary) Switch Settings

Memory Address	MH10-H No.	Memory Address (Lower Boundary) Switch Settings 14	15	16	17	18
000000–377777	0	0	0	0	0	0
400000–777777	1	0	0	0	0	1
1000000–1377777	2	0	0	0	1	0
1400000–1777777	3	0	0	0	1	1
2000000–2377777	4	0	0	1	0	0
2400000–2777777	5	0	0	1	0	1
3000000–3377777	6	0	0	1	1	0
3400000–3777777	7	0	0	1	1	1

MH10 memories connected to a KA10 memory bus must have consecutive addresses. If this addressing is not followed, holes are created in the memory address space and the KA10 attempts to address memory that does not exist.

When 64K MH10-G memories are connected to the memory bus, the LOWER BOUND ADDRESS toggle switches are set differently. Only four MH10-G memories can be connected to the KA10 processor memory bus due to the KA10 memory size limitation. Only switches 14 through 19 (instead of 14 through 20) are used. Again, the PORT SELECTION switch relative to the KA10 processor is placed in the center (KA) of three positions, which, in effect, results in ignoring bits 14–17. Table 2-3 lists the address switch settings for a typical system having four 64K MH10-G memories connected to one-KA10 memory bus or eight MH10-G memories connected to KI10 or KL10 memory buses.

NOTE

If the KA10 processor is used, only four 64K MH10-G memories can be connected to the memory bus.

Table 2-3 MH10-G (64K) Memory Address (Lower Boundary) Switch Settings

Memory Address	MH10-H No.	Memory Address (Lower Boundary) Switch Settings					
		14	15	16	17	18	19
000000–177777	0	0	0	0	0	0	0
200000–377777	1	0	0	0	0	0	1
400000–577777	2	0	0	0	0	1	0
600000–777777	3	0	0	0	0	1	1
1000000–1177777	4	0	0	0	1	0	0
1200000–1377777	5	0	0	0	1	0	1
1400000–1577777	6	0	0	0	1	1	0
1600000–1777777	7	0	0	0	1	1	1

2.3.3 Interleave (INTL/NORM) Switch Settings

Interleaving MH10 memories is controlled by two toggle switches located on the Memory Maintenance panel. These switches are used to select normal (non-interleaved) operation, 2-way interleaved operation, and 4-way interleaved operation. Table 2-4 lists switch settings for the various interleaved situations.

NOTE

Only memory units with the same number of memory locations can be interleaved; i.e., a 128K memory cannot be interleaved with a 64K memory (Paragraph 4.3.3).

Table 2-4 Interleave Switch Settings

Mode	Interleave Switches	
	34	35
Normal	NORM	NORM
2-way	NORM	INTL
4-way	INTL	INTL

In 2-way interleaving, address bit MADR 35 is swapped with address bit MADR 20. The result is that all even addresses are accessed through Control 0 (C0) and all odd addresses are accessed through Control 1(C1).

In 4-way interleaving, in addition to swapping MADR 35 for 20, MADR 34 is swapped with either MADR 19, 18, or 17 depending on the memory size in each cabinet. The result is that four consecutive words are obtainable from the four controls in the two cabinets.

2.3.4 Port Selection Switch Settings and Priority

Eight 3-position selection switches (P0–P7) are located on the Maintenance panel. In the down position of a given switch, access to the memory by the port associated with that switch is denied. The middle position is used for accessing the MH10 from KA-type processors only (address bits 14–17 are ignored). The up position is used for accessing the MH10 from KI- or KL-type processors.

In the case of multiple simultaneous requests from all eight ports, the following priority scheme is used:

Port	Priority	Associated Devices
0, 1	Highest; alternates between P0 and P1	Disks, drums, and other high-speed devices
2, 3	Second; alternates between P2 and P3	
4, 5, 6, 7	Lowest; rotates among P4, P5, P6, and P7	CPUs; e.g., KI or KL

If two or more requests are received simultaneously by the MH10, the priority network enables the port that has the highest priority. For example, second priority is shared between ports P2 and P3, such that if P2 were serviced last in the previous memory cycles, then P3 would be given priority over P2, should simultaneous requests occur in those ports. Likewise, the highest priority is shared between ports P0 and P1.

The rotating scheme works differently. Priority goes downward from P4 to P7. For example, if P5 was the last serviced port, for subsequent simultaneous requests to those ports, priority would pass to P6, etc. After P7, the priority "rotates" back to P4.

2.3.5 MEMORY BANK Switch Settings

Automatic selection and deselection of memory banks is provided by the four MEMORY BANK switches located on the Maintenance panel; each MEMORY BANK switch controls 64K of memory. A detailed description of the memory bank selection logic is given in Paragraph 4.4.4.4.1. Table 2-5 lists the memory bank sizing.

Table 2-5 Memory Bank Selection Decoding

MEMORY BANK Switches*				
M0	M1	M2	M3	Memory Size
1	0	0	0	64K
1	1	0	0	128K
1	1	1	1	256K

* 1–Indicates switch in ON LINE position.
0–Indicates switch in OFF LINE position.

2.3.6 Memory Select Switch Setting

The Memory Select (Deselect) switch connects the CROBAR signal line to ground, when in the "Deselect" position, which prevents operation of all the memory in the affected cabinet. This switch must be in the "select" position to permit acccess to the unit.

2.3.7 35-INTL Switch

The 35-INTL switch is not used (currently) in the MH10.

2.3.8 Jumper Configuration and Delay Timing

Refer to drawings D-BS-MH10-0-IS0 and 1 for the correct jumper selection and delay settings in the MH10 control logic.

CHAPTER 3
OPERATION

3.1 INTRODUCTION
The MH10 controls and indicators are grouped on three separate panels: the Maintenance panel, the Indicator panel, and the 857 Power Control panel. The following paragraphs state the purpose of each panel and describe each control and indicator. Figure 3-1 shows the MH10 Maintenance Switch panel. The 857 power control (Figure 3-2) is mounted on the rear cabinet door.

3.2 PANEL OPERATION
Generally, the panels can be described as follows:

1. The 857 Power Control panel controls input power to the MH10.

2. The Maintenance panel controls port addressing, port selection, sizing, and troubleshooting hardware.

3. The Indicator panel provides fault detection and status indicators.

3.2.1 857 Power Control Panel
The 857 Power Control panel (Figure 3-2) performs the following functions:

1. Adapts the MH10 to different ac line voltage inputs.

2. Enables central control of power turn ON/OFF from the PDP-10 console power switch.

3. Initiates power shut-down if any of the memory logic door interlocks or the air flow sense switches are activated (Paragraph 4.4.5.1.4).

4. Enables memory logic door interlocks and air flow sense switch to be overridden for maintenance purposes.

5. Provides circuit breaker protection against overloading.

Tables 3-1 and 3-2 describe the 857 Power Control panel switches and indicators.

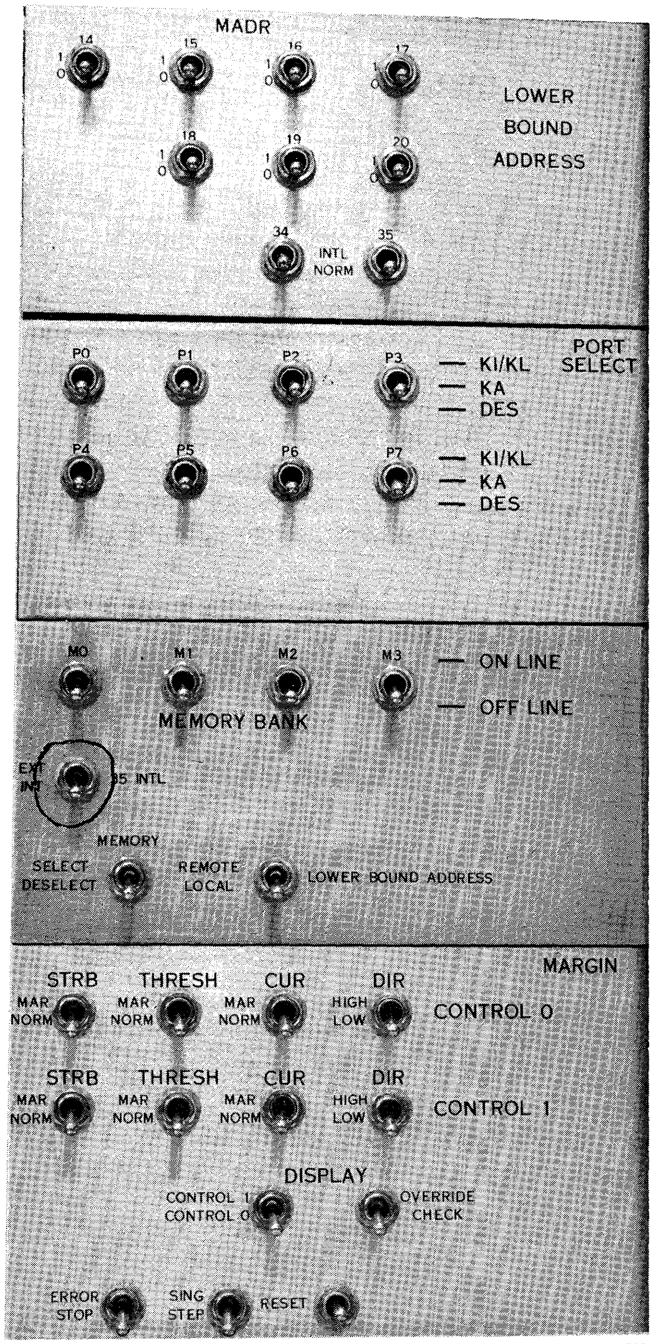


Figure 3-1 MH10 Maintenance Switch Panel

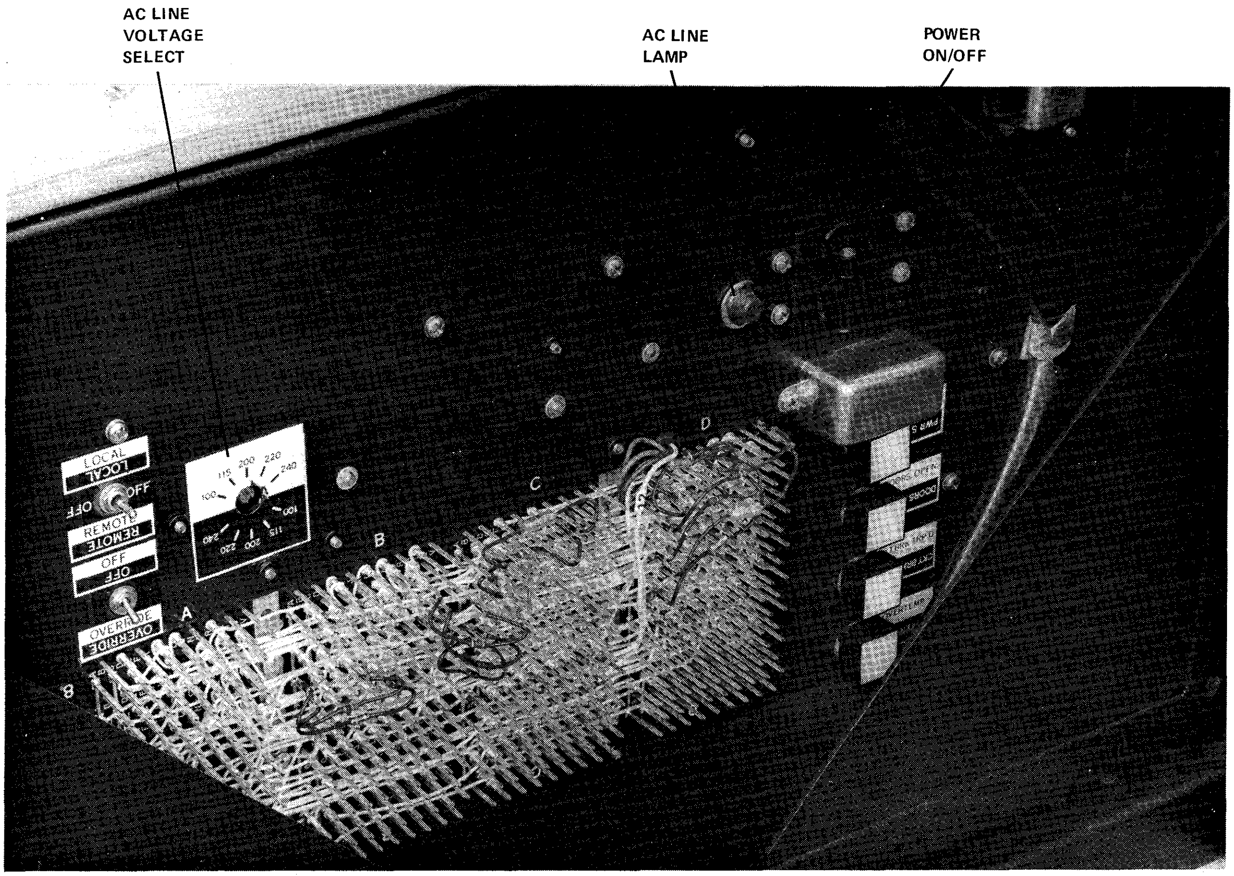


Figure 3-2   857 Power Control Panel

Table 3-1   Power Control Switches

Switch	Function
LOCAL/OFF/REMOTE	Allows power to turn ON/OFF from the CPU (REMOTE) or from the MH10 unit (LOCAL).
OVERRIDE	Overrides the temperature sense switches and door interlock switches.
AC SELECT LINE VOLTAGE	This switch is set for the ac line voltage that is supplied.
POWER ON/OFF	This is the ac input line voltage circuit breaker.

Table 3-2 Power Control Indicators

Indicator	Function
PWR SW ON	Lights when ac power is applied to all power supplies in the memory unit. A flashing light means that the OVERRIDE switch is on.
DOORS OPEN	Lights when either or both of the logic cabinet doors are open.
CKT BRK TRP'D	Not used.
OVERTEMP	Lights when an over-temperature condition exists.
AC LINE LAMP	Lights when ac line voltage is present.

3.2.2 Memory Address Switches

The memory address switches are located in the top section of the Maintenance panel (Figure 3-3) and are labeled LOWER BOUND ADDRESS. These LOWER BOUND ADDRESS switches establish the lowest address in the cabinet.

Also located on the Memory Address Switch panel are the two interleave (INTL/NORM) switches. Refer to Paragraph 2.3.3 for a complete explanation of their operation.

Table 3-3 summarizes the Memory Address Switch panel switches.

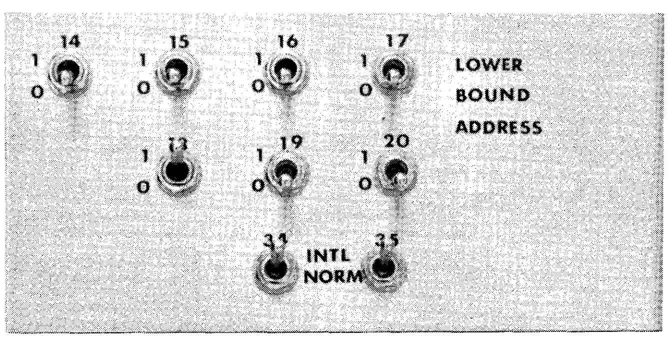


Figure 3-3 Memory Address Switches

Table 3-3 Memory Address Switch Panel

Switch	Function	Engineering Drawing No.
MADR 14-20*	Two-position toggle switches which are set to establish the lower boundary address of the memory unit, allowing memory address bits 14–20 to select a particular unit (Paragraph 2.3.2).	M8592-0-PAD0 M8592-0-PAD1
INTL/NORM (34, 35)	Two-position toggle switches that select 2- or 4-way interleave or normal mode operation. (See Table 2-4 for interleave switch settings.)	M8592-0-PAD0 M8592-0-PAD1

* All ports reflect this address.

3.2.3 Maintenance Panel

The entire Maintenance panel was shown in Figure 3-1. The sections of the panel previously discussed (i.e., memory address, port selection, and memory banks) comprise the three uppermost sections of the panel. The lowest section (Figure 3-4) contains the switches related strictly to maintenance. The top two rows of switches on this section are identical, except each row relates to a different controller (0 and 1).

Table 3-4 lists the Maintenance panel section switch definitions. Definitions for the top two rows of switches are not duplicated, as the functions are identical except for the control section referenced.

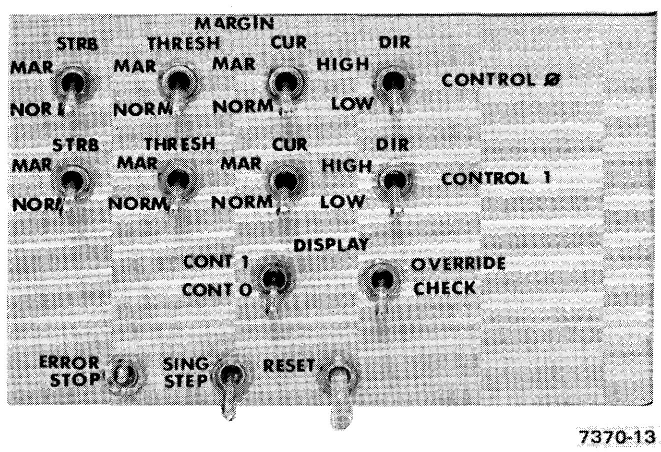


Figure 3-4 Maintenance Panel (Maintenance Section)

Table 3-4 Maintenance Panel Switches

Switch	Position	Function
STRB	MAR	Varies the internal strobe timing pulse ±7 ns, to check for marginal memory bank conditions reflected in marginal core switching speeds.
	NORM	Normal operation.
THRESH	MAR	Varies the sense amplifier threshold amplitude to check for marginal memory bank conditions reflected in marginal core noise or amplitude condition.
	NORM	Normal operation.
CUR	MAR	Varies the X/Y core selection currents by ±7.5% to check for marginal CMC conditions.
	NORM	Normal operation.
DIR	HIGH	Permits the STRB, THRESH, or CUR switches to apply their respective margin values in the high (+) direction.
	LOW	Permits the STRB, THRESH, or CUR switches to apply their respective margin values in the low (–) direction.
DISPLAY	CONT 0	Data and memory address for Control 0 are displayed.
	CONT 1	Data and memory address for Control 1 are displayed.
	OVERRIDE	Data, address, ACTIVE, RD RQ, and WR RQ lights continue displaying MH10 status even if parity error exists.
	CHECK	Data, address, ACTIVE, RD RQ, and WR RQ lights stop (MH10 logic does not stop) at a parity error.
SINGLE STEP*	ON	Prevents the completion of the memory cycle, but allows the completion of one memory cycle each time the RESET switch is activated. (The request and acknowledge portion of the cycle is allowed, but the read/write portion is inhibited.)
ERROR STOP	ON	Causes the STOP indicator to light and prevents further memory cycles when a memory control logic error or data parity error is detected. The STOP condition is cleared with the RESET switch.
RESET	ON	Spring-loaded momentary switch which, when pressed, clears and initializes the memory.

* All 0s are written into memory when SINGLE STEP is used on clear/write cycle.

3.2.4 Indicator Panel

The MH10 Indicator panel (Figure 3-5) provides memory operation status indicators to aid in the maintenance of the MH10. Visual displays indicate memory operation and the contents of the Address and Data registers. When an operation indicator lights, the function identified as active or true; when a register indicator lights, the particular bit position identified contains a binary 1. The register indicators (Table 3-5) are grouped in octal format to facilitate translation of the binary word segments.

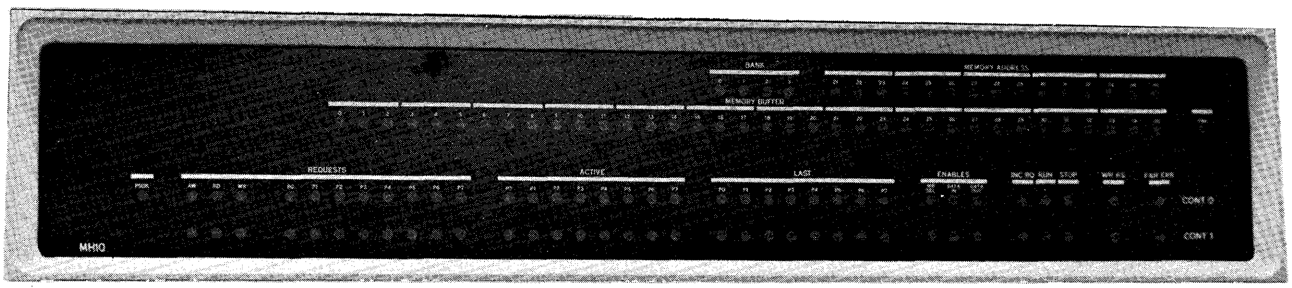


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Figure 3-5 Indicator Panel

Table 3-5 Indicator Panel Lamp Functions

Indicator	Function (When Lighted)
BANK 0–3	Indicates which of the four memory banks is being used.
MEMORY ADDRESS 21–35	Indicates the current Memory Address
MEMORY BUFFER 0–35 and PAR (parity)	Indicates the contents of the Memory Buffer register.
PSOK	Power is applied to the unit and regulated voltages are within tolerances.

Table 3-5 Indicator Panel Lamp Functions (Cont)

Indicator	Function (When Lighted)
REQUESTS	
AW	The memory control is free and waiting processor request for access.
RD	A read request is being processed or was the last memory cycle processed.
WR	A write request is being processed or was the last memory cycle processed.
P0–P7	Indicates which processor port(s) is requesting access
ACTIVE P0–P7	Indicates which port in a given priority level is presently being accessed.
LAST P0–P7	Indicates which port in a given priority level was last granted access.
ENABLES	
MB SEL	The active port memory bus transceivers are enabled to send or receive data to or from the processor.
DATA IN	The data transfer from the PCCI Data register to the CMC data latches is enabled.
DATA OUT	The CMC data bus drivers (on the G116 modules) are enabled to transmit the data from the CMC data latches to the PCCI bus transmitters.
INC RQ	Indicates failure of a cycle completion 20 μs from the start of the memory cycle.
RUN	The memory unit is performing a memory cycle.
STOP	An error was detected while in the error stop mode.
WR RS	The Write Restart signal was received from the processor.
PAR ERR	A parity error was detected during the memory cycle.

CHAPTER 4
PRINCIPLES OF OPERATION

4.1 INTRODUCTION
This chapter contains detailed information on the logical operations of the MH10 Core Memory. To aid the reader, a discussion of drawing conventions and notations introduces the detailed theory.

Two levels of detailed theory are included in this chapter: interface and unit. The interface level of theory discusses all MH10 interfacing in a DECsystem-10 installation. The level of discussion is supported by a block diagram and additional related drawings. The text does not go beyond the level of the diagrams used and mainly describes interfacing logic.

The unit level theory discusses the MH10 logic at a detailed level, referencing block schematics, flow diagrams, and the MH10 print set logic schematics. This section defines how the various memory operations function.

Emphasis here should be placed on referencing the main MH10 flow diagram (located in the print set), which provides the reader with an overall view of the various memory operations. Included in some of the operation descriptions are additional, simplified flows that reflect just the immediate subject.

4.2 CONVENTIONS AND NOTATIONS
Accompanying every MH10 Core Memory is a set of drawings that defines the memory physically, electrically, and functionally. Both the logic drawing and flow diagram conventions and notations are discussed in the following paragraphs.

4.2.1 Logic Drawings
Various drawings (block schematics) show the function and location of every logic element used in the MH10.

Just below the title in the lower right corner of each drawing is the drawing identification written in four boxes. In the left box is a letter indicating the size of the original drawing; a 2-letter code indicating the type of drawing is in the next box. The third box contains the drawing number in three parts: the left part is the identification number of the module, the center digit names the drawing variation number, and the right digit identifies the individual drawing or a mnemonic code appears that identifies both the individual drawing and the material presented on it. For a drawing with several sheets, this mnemonic code runs consecutively (e.g., AR0, AR1). If a drawing is revised after being signed by the project engineer, the revision letter is written in the right box.

Almost all drawings are D size, but are reduced to B size for convenience. Some typical codes for drawing types are block schematic BS, flow diagram FD, circuit schematic CS, and module utilization MU. The modules are described in terms of the drawings that represent the standard production equipment at the time the manual was printed; the print set, however, reflects any later revisions and any special features unique to a given installation. The drawings associated with the text are listed in Table 4-1.

Table 4-1 Signal/Drawing Identification

Signal Prefix*	Title	Module	Drawing
CHK(N)	Parity Check	M8588	CHK0-1
CYT(N)	Cycle Timing	M8566	CYT0-2
PRC(N)	Priority Control	M8590	PRC0-2
ADR(N)	Address Receivers	M8591	ADR0-2
PAD(N)	Port Address Interface	M8592	PAD0-2
DR(N)	MH10 Data Register	M8593	DR0-1
AD(N)	MH10 Address Register	M8593YA	AD0-1
DAT(N)	MH10 Data Transceivers	M8594	DAT0-1
MAT(N)	Memory Timing	M8565	MAT0-2

* (N) refers to the relative sheet number of that particular module drawing.

Standard logic symbols are used throughout the MH10 drawing set. Some of the newer chips used, however, are not familiar to everyone. Therefore, Appendix A is provided to list those unique chips, truth tables, and other pertinent information. Appendix A is a very beneficial supplement to this manual; refer to it when you are unsure of the operation of a particular chip.

Every element on the logic drawings is identified by the reference designation type number. The location of every element on that particular module is listed just below the reference number. Inputs or outputs shown as a plain line represent a high level; a line with a circle at its end represents a low level. For those familiar with traditional DIGITAL logic symbology, the circle is equivalent to a solid diamond or arrowhead; the plain line is equivalent to an open diamond or arrowhead.

Simple gates are combined in a variety of ways to provide the OR and AND functions. The symbol for an exclusive OR gate (XOR) is the OR symbol with an extra line at the back of the arrowhead, as shown (for example) at the upper left in CHK1. Most of the remaining logic elements are represented by boxes that are labeled for the logic functions, such as an adder, a comparator, or a mixer. It is recommended that you go through the MH10 drawings (and Appendix A) and familiarize yourself with all of these logic elements symbols.

Flip-flops are all D-type and (for example) are represented by rectangular symbols as shown on DR0. A single module may have a number of independent flip-flops, or a group that has a common clock, clear, and set inputs. The flip-flops may be drawn horizontally or vertically, but the outputs are always on the top or right side, and the clock and data inputs are below or to the left of the figure.

When drawn horizontally, the clock input and clocked data input are always directly below the "0" and "1" outputs, respectively. When drawn vertically, the same inputs are directly to the left of the corresponding outputs. The unclocked clear and set inputs are always on the 0 and 1 sides, respectively. Note that the output terminals are drawn twice, showing the polarities associated with either state of the flip-flop. The polarities of the output terminals for the 0 state are shown over the 0; for the 1 state, the terminals have the polarities shown over the 1. This agrees with the convention that neither voltage level categorically represents 1 or 0, true or false. A given logic function may have different assertion levels in different places, depending upon gate input requirements. A signal is always regarded as true when it has the polarity shown for the input or output associated with it. In other words, if the signal X appears at an input with a circle, then X is true when low. The very same physical line may appear elsewhere without the circle but with the signal designation -X; this is equivalent, for now a high level on the line indicates that -X is true, i.e., X is false.

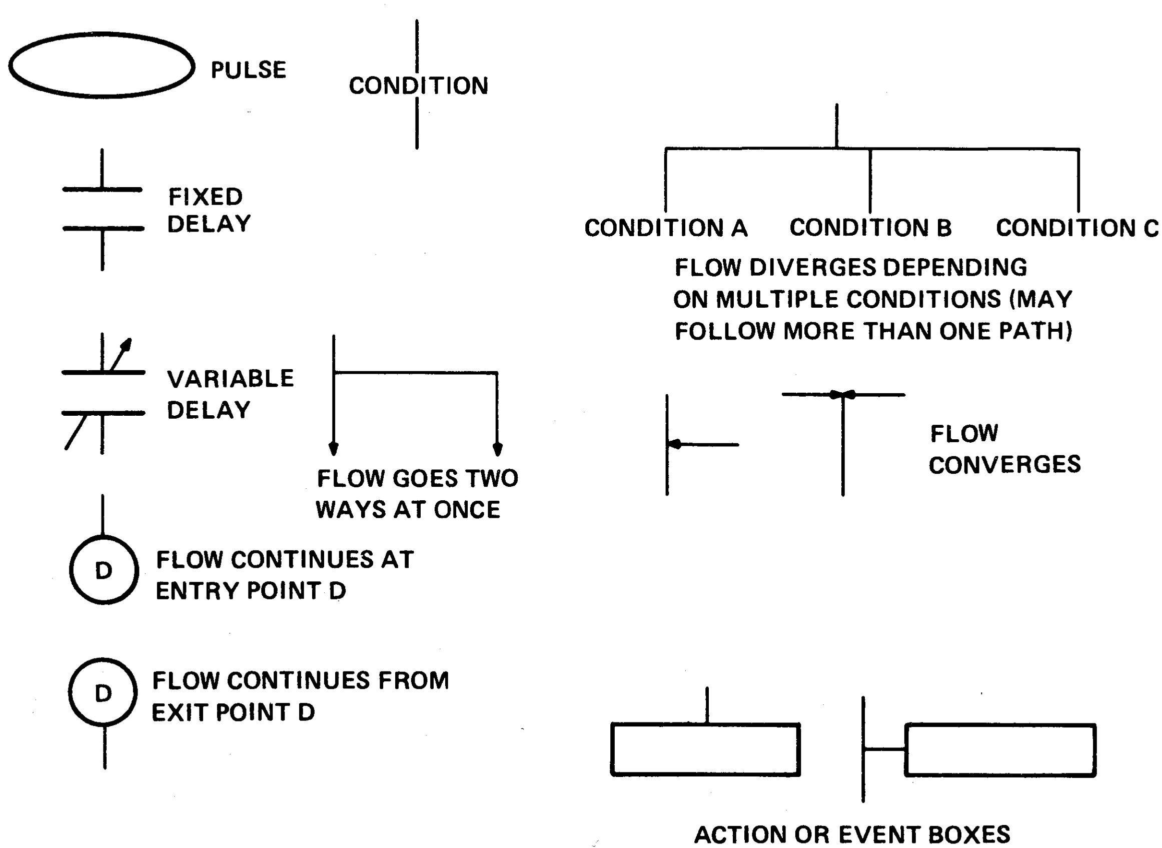
4.2.1.1 Signal Notation – All signal names are mnemonics that indicate both the function of the signal and its source. In almost all cases, signal names are meaningful phrases, although they are sometimes lengthy. Typical mnemonic terms used are IND indicator, PAR parity, CLK clock, STRB strobe, SEL select, CLR clear, EN enable, etc.

The source of any signal can be determined from its first term or its first letters. Each register with associated logic and each control section, whether it occupies several drawings or only part of a drawing, has a mnemonic designation that appears in the drawing number and at the beginning of the name of any signal originating in that part of the logic. This source code may appear naturally as part of the signal name; if not, it is merely prefixed to the name. For example, all signals originated in the parity checking logic have names that begin with CHK.

4.2.2 Flowcharts

The flowcharts show the major MH10 events and the flow of operations in a manner consistent with the actual gating and timing in the hardware, based on a sequence of level changes and timing pulses. In general, flow is downward. Upward flow occurs only upon returning to an earlier part of a sequence (as in a loop) or when going from one flow line to the next when several are on the same drawing; in any case, no conditions or events are ever shown along a rising line. Time pulses are indicated by ellipses. Events are shown in boxes that are at one side of the line unless an event actually is responsible for further movement along the line. If an event occurs only on some conditions, those conditions are written at the left of a colon and the resulting event is written at the right.

FLOW CHART CONVENTIONS



Essentially, there is no passage of time along a continuous line. A break in a line indicates that movement along the line cannot continue beyond that point unless the condition written in the break is satisfied. This does not indicate any passage of time and the condition must be satisfied then; movement cannot restart should the condition later become true. Actual passage of time is indicated by horizontal lines breaking the flow line. A pair of single horizontal lines indicates a fixed delay, with the delay time written between the lines. Variable delay times have an arrow through the horizontal lines with a nominal time indicated.

4.3 INTERFACE LEVEL DESCRIPTION

This section defines the MH10 Core Memory on an interface level. Through the use of a block diagram, figures, and text, an overview of all memory cycles is given and the major logic sections are defined.

4.3.1 Operation Overview

To begin operation, a processor requests access to a memory unit by placing the memory address on the memory bus along with the type of cycle requested (Figure 4-1). The cycle type is established by the Read Request [(Pn) RD RQ] and Write Request [(Pn) WR RQ] signals as follows:

1. Read/Restore Cycle = Pn RD RQ is true *and* Pn WR RQ is false.
2. Clear/Write Cycle = Pn RD RQ is false *and* Pn WR RQ is true.
3. Read/Modify/Write Cycle = Pn RD RQ is true *and* Pn WR RQ is true.

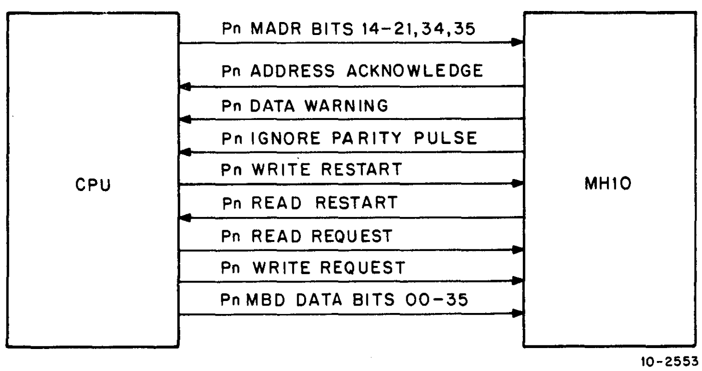


Figure 4-1 Memory Processor Interface

Memory address bits 14–21, 34, and 35 are inputs to the port address interface logic. In the event of simultaneous requests, the memory port priority logic determines the highest priority port request; then, the ADR ACK (Address Acknowledge) pulse is sent to the corresponding processor, signifying acceptance of the request.

4.3.1.1 Read/Restore Cycle – The Read/Restore cycle transfers data from a selected memory location to a requesting processor. During the read portion of this cycle, the memory reads data from the addressed memory location and loads it into the memory data latches (registers). From there, the data is placed on the bus to the requesting processor. If the parity bit is to be ignored (for KA processors only), the IGN PAR (Ignore Parity) pulse is sent to the processor. At the same time as the data is sent, the RD RS (Read Restart) pulse is sent to the processor, indicating that the data requested has been sent. During the restore portion of the cycle, the memory disconnects from the bus and writes the data in the memory data latches back into the addressed memory locations. This last step is necessary because the MH10 is a destructive readout memory.

4.3.1.2 Clear/Write Cycle – The Clear/Write cycle transfers data from a processor to a selected memory location. During the clear portion of the cycle, the memory reads data from the addressed memory location, discards it, and loads the data from the processor into the memory data latches by means of the WR RS (Write Restart) pulse sent by the processor. During the write portion of the cycle, the memory disconnects from the bus and the new data and parity bit contained in the memory data latches are written into the addressed memory location.

4.3.1.3 Read/Modify/Write Cycle – The Read/Modify/Write cycle transfers data from a selected memory location to a processor for modification and then transfers the modified data back to the selected memory location. During the read portion of the cycle, the memory reads the data from the addressed memory location, loads it into the memory data latches, places the data on the bus to the processor, clears the memory data latches, and pauses. While the memory pauses, the processor modifies the data (modify portion) and initiates the write portion of the cycle by placing the modified data on the bus and sending the WR RS pulse. The memory then loads the modified data into the memory data latches and writes it into the same selected memory location.

4.3.2 Major Logic Sections

A brief description of the two major logic sections is presented in the following paragraphs. The PCCI section comprises the request-acknowledge and priority control logic, as well as logic that initiates and controls the interfacing of the two sections. The CMC section comprises the core memory stacks and the addressing and timing control logic for reading and writing the data words. Figure 4-2 shows major control signals and data flow, along with the logic subsection interconnections.

4.3.2.1 Port Control and Core Interface (PCCI) – The PCCI consists of two almost identical control sections: C0 and C1, of which both may be accessed by all eight ports (Figure 4-3). Of the total 256K 37-bit words, C0 controls the left 128K words and C1 controls the right 128K words. In the non-interleave mode, address bit MADR 20 determines which storage section is being accessed. The left 128K is being accessed if MADR 20 is a one. This means that one port may gain access through C0, while another port may simultaneously gain access through C1, resulting in doubling the data transfer rate as compared to earlier models.

Each control consists of the following logic sections:

1. Port Address Interface (PAD) – Consists of the memory address bits and logic for selecting the proper MH10 cabinet (unit).
2. Priority Control (PRC) – Consists of the logic that:
    a. Performs port priority selection in the event of simultaneous requests
    b. Generates strobe to load the Memory Address register
    c. Generates the upper Bound Address bits.
3. Cycle Timing (CYT) – Consists of status logic (e.g., run, stop, etc.), the conditioning logic (e.g., restart, error stop, cycle start, single step, reset, etc.), and Control Timing pulses.
4. Address Receivers (ADR) – Contains the Memory Address receivers and generates the ADR ACK and DATA WARNING pulses.
5. Data Register (DR) – Contains the memory data bits.
6. Address Register (AR) – Contains the memory address bits.
7. Data Transceivers (DAT) – Contains the data receivers that direct the Data pulses to one of the two Data registers. It also contains the drivers for strobing READ data out onto the correct memory bus. All eight ports can access both controls.
8. Parity Check (CHK) – Contains the control logic and registers for storing READ or WRITE data from which parity is checked. It also contains multiplexors for displaying inverted or noninverted inputs (e.g., data input is true LOW, address input is true HIGH).

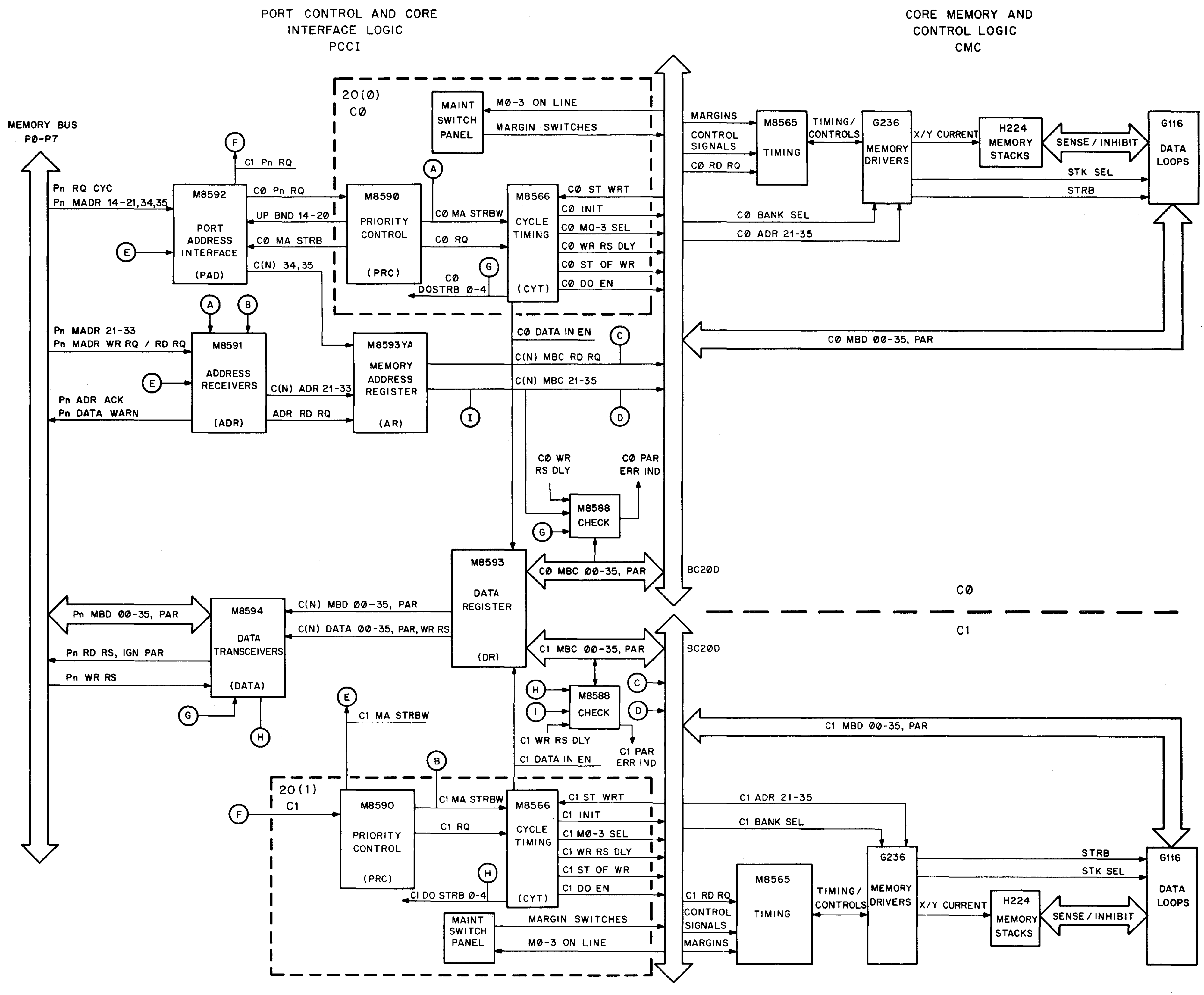


Figure 4-2 MH10 Block Diagram

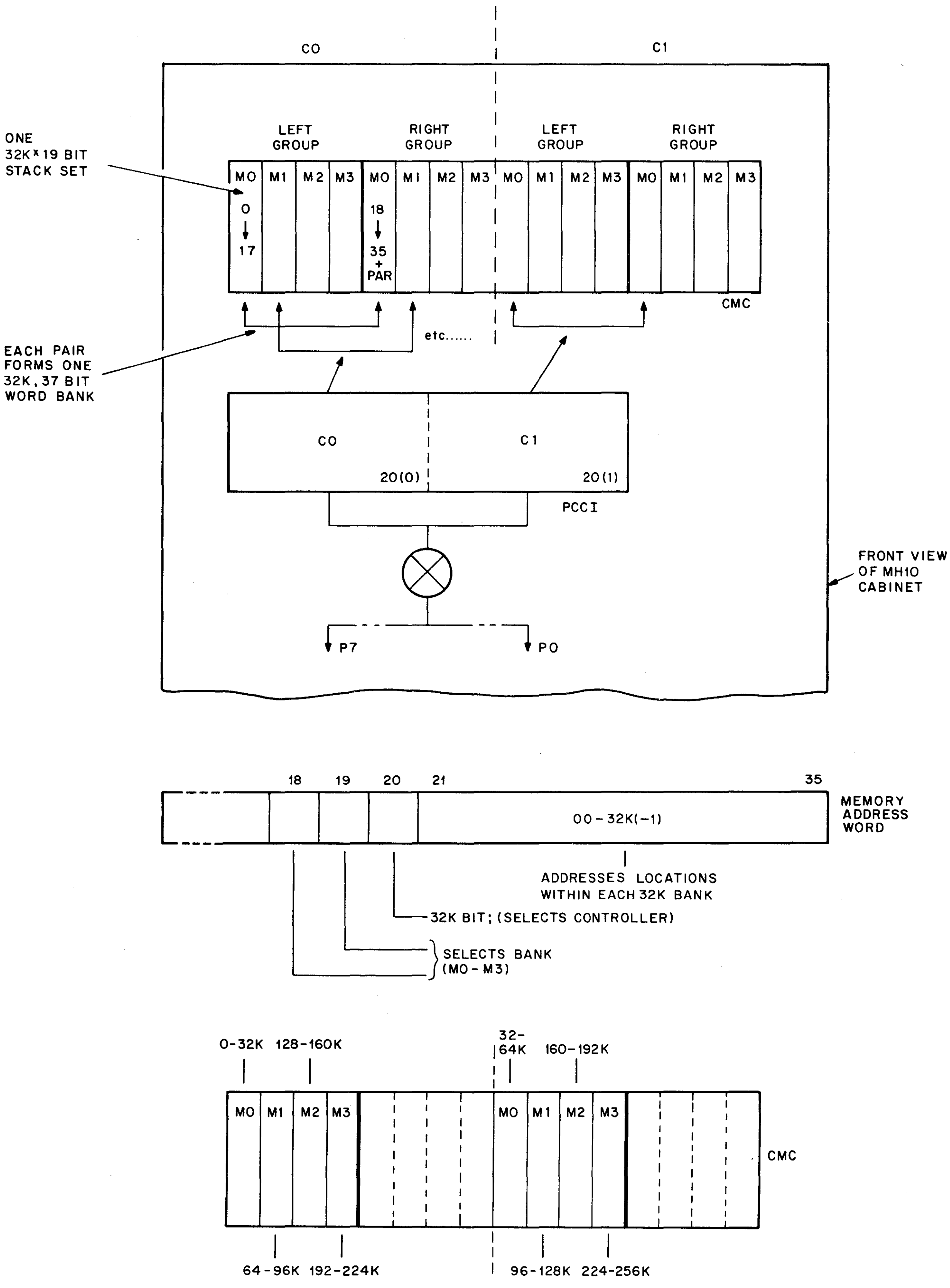


Figure 4-3 CMC/PCCI Format

4.3.2.2 Core Memory and Control Section (CMC) (Figure 4-3) – This storage section is divided into a left half and a right half, with each half capable of storing up to 128K × 37-bit words. The left half is controlled by PCCI Control 0 and the right half is controlled by PCCI Control 1. Each half consists mainly of eight stack sets. The four leftmost stack sets store the low order bits (00–17), and the four rightmost stack sets store the high order bits (18–35, PAR). Each corresponding pair of stack sets is referred to as a memory bank. The four memory banks of each storage half are numbered M0, M1, M2, and M3.

The minimum memory size is 64K, 37-bit words, consisting of 32K, 37-bit word bank M0 in the right-half section and 32K, 37-bit word bank M0 in the left-half section. For ease of reference, each half section is prefixed by the mnemonic for its respective control, i.e., C0 and C1. The three different memory sizes offered are 64K, 128K, and 256K, 37-bit words.

Each 32K, 19-bit stack set consists of three modules: G116 Sense Inhibit (Data Loops), H224 Stack, and G236 Memory Driver.

A bank, therefore, comprises two of each of these three modules. Additionally, for each half section, one M8565 is provided to manage the timing requirements of all the memory banks.

1. M8565 Timing – This module generates the control signals and timing pulses that are required to control the READ and WRITE currents, memory margins, and CROBAR circuitry.

2. G116 Sense Inhibit – This module contains the sense amplifiers, inhibit drivers, and data latches.

3. H224B Stack – This module contains the ferrite core array, X-Y diode matrices, sense/inhibit terminations, stack charge circuit, and a thermistor to provide temperature compensation for the bias circuit.

4. G236 Memory Driver – This module contains the decoders, X and Y drivers and switches, sense strobe control, bias source generator, and current sources.

4.3.3 Interleaving

Interleaving logic allows 64K, 128K, or 256K MH10 Core Memory units to be addressed in a manner that allows consecutive memory addresses to alternate between the two controls in one MH10, or rotate through the four controls in two MH10s.

Only memories of the same size and having consecutive port addresses with an even port address first may be 4-way interleaved. For example, 4-way interleaving can exist between memories 0 and 1, but not between 1 and 2. Interleaving is accomplished by swapping port address bits with word address bits. Functionally, the memory address can be divided into three segments:

Memory Size	Port Address Bits	Segments Bank Select Bits	Word Address Bits
64K	14–19	20	21–35
128K	14–19	19,20	21–35
256K	14–19	18–20	21–35

When 2-way interleaving is selected, bit 20 is swapped with the least significant word address bit, bit 35. In this configuration, should the processor generate consecutive addresses starting at address 0 or MH10 number 0, the subsequent memory cycles would alternate between MH10 Control 0 and Control 1, with all even addresses located through Control 0 and all odd addresses located through Control 1.

In 4-way interleaving, bit 20 is again swapped with bit 35 and bit 34 is swapped with bit 19, 18, or 17, depending on the storage size in each MH10. Thus, memory words would be addressed in the following sequence:

MH10-0 Control 0: 0, 4, 10, etc.
MH10-0 Control 1: 1, 5, 11, etc.
MH10-1 Control 0: 2, 6, 12, etc.
MH10-1 Control 1: 3, 7, 13, etc.

4.4 UNIT LEVEL DESCRIPTION

A block diagram of the MH10 is shown in Figure 4-2, and circuit diagrams and flows are interspersed through this section. Engineering drawings are also referenced where applicable. Note again that the mnemonic prefix portion of signal names shown on the illustrations indicates the signal source. For example, the CYT1 C(N) CYC START H signal is generated on the Cycle Timing 1 logic drawing, D-CS-M8566-0-CYT1.

4.4.1 Initial Conditions

Applying power to the MH10 initializes the memory system and places the MH10 in an idle state ready to respond to access requests from a processor. Refer to Figure 4-4, MH10 Power-Up Flow Diagram, while reading this section.

When power is initially turned on, CAB C(N) CROBAR INPUT (from DC LO of the H7420 power supplies) is temporarily shorted to ground causing CYT2 C(N) CROBAR L to be true. This disables the data and address transceivers and prevents spurious pulses from being sent out on the memory bus. At the same time, CYT2 C(N) CLR AW RQ L clears the CYT0 C(N) AW RQ flip-flops, preventing access to both controls (C0 and C1). Signal CYT2 C(N) CLR AW RQ L is also wired to the PS OK indicator so that the indicator is temporarily not turned on. When DC LO (from the H7420 power supplies) is released to +3 V, the PS OK indicator light is turned on and a CYT2 C(N) PWR RESTART L pulse is generated which, in turn, generates CYT1 C(N) RESET PLSE L and CYT1 C(N) STATE CLR. Thus both controls (C0 and C1) are initialized. Approximately 300 ns later, PRC0 C(N) SET AW RQ L is generated to set the CYT0 C(N) AW RQ flip-flops, indicating that both controls are free to accept memory requests.

4.4.2 Request/Acknowledge

Basic request/acknowledge circuitry must be capable of recognizing an access request from a processor or other device and acknowledging that request when the memory is free to service it. However, the MH10 request/acknowledge circuitry is required to perform tasks in addition to the basic request/acknowledge tasks. Because the MH10 is required to service up to eight separate devices, the priority network allows access to the processor (or device) having highest priority. The priority control logic is shown on the PRC drawings. The following paragraphs explain the request/ acknowledge sequence with reference to the PRC and CYT drawings.

4.4.2.1 Single Access Request – Two Priority Control modules (M8590) are used in each MH10: one for Controller 0 (C0), the other for Controller 1 (C1). Each controller can be accessed by all eight ports. This discussion continues the use of C(N) to represent either controller, as the logic for both is identical.

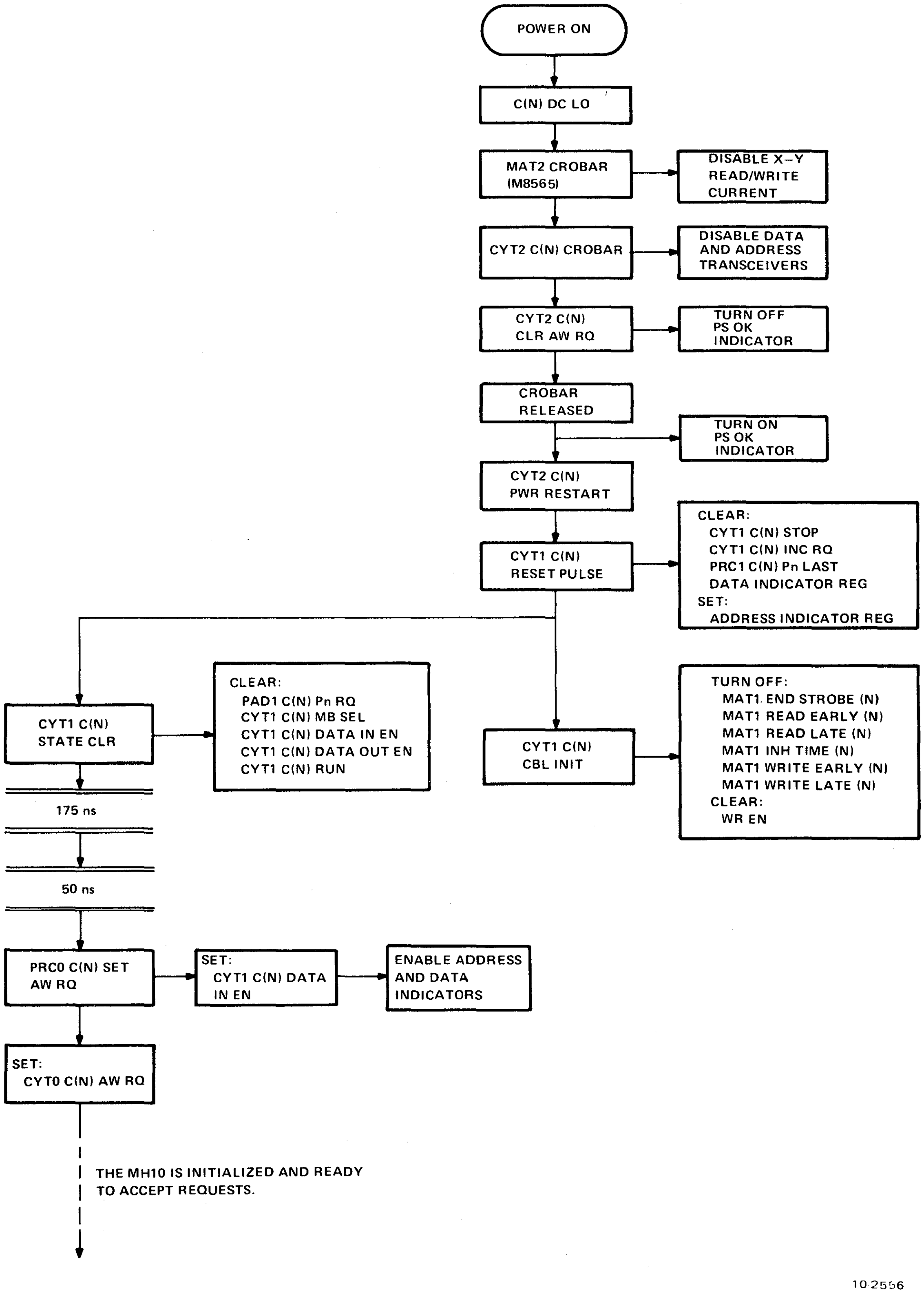


Figure 4-4 MH10 Power-Up Flow Diagram

Assuming the memory is in the idle state, as explained in Paragraph 4.4.1, the sequence is initiated when a processor generates a Pn RQ signal and a memory address that is within the address boundaries of the specific MH10. The address boundaries are determined by the setting of the LOWER BOUND ADDRESS switches and the storage size of the MH10 as determined by the four MEMORY BANK switches.

When this happens, one of the port request (e.g., PAD1 C(N) P0 RQ L) signals asserts and generates signal PRC0 C(N) RQ H. This resets the CYT0 AW RQ flip-flop and generates the CYT0 C(N) MA CLR CLK L and CYT0 C(N) MB CLR CLK L pulses. As long as the CYT0 AW RQ flip-flop is reset, subsequent processor requests are ignored. The CYT0 C(N) MA CLR CLK L clears the Memory Address register, while the CYT0 C(N) MB CLR CLK L clears the Memory Buffer register and the WR RS DISPLAY flip-flop. The registers are now ready to receive the current memory address and data. The same port request (PAD1 C(N) Pn RQ L) that generated the main PRC0 C(N) RQ H signal also inverts and becomes PRC0 C(N) Pn RQ H, notifying the priority control logic that port Pn is requesting access.

After a delay of approximately 60 ns, the PRC0 RQ H signal generates two types of pulses: the 27 ns wide PRC0 C(N) MA STRB 0–3 H pulses are generated, which load the address into the Memory Address register; the second pulse generator outputs the PRC0 C(N) MA STRBW (wide) pulse, which is approximately 107-ns wide. This signal is used to generate the ADR ACK (Address Acknowledge) signal. Signal PRC0 C(N) MA STRBW H (wide) is also used to generate CYT1 C(N) CAB CYC START H after a delay of approximately 65 ns. The latter signal starts the core read cycle.

4.4.2.2 Simultaneous Access Requests – Simultaneous access requests dictate the need for additional priority control. If two or more requests are received simultaneously by the MH10, the priority network enables the port having the highest priority. The priority scheme is as defined in Paragraph 2.3.4.

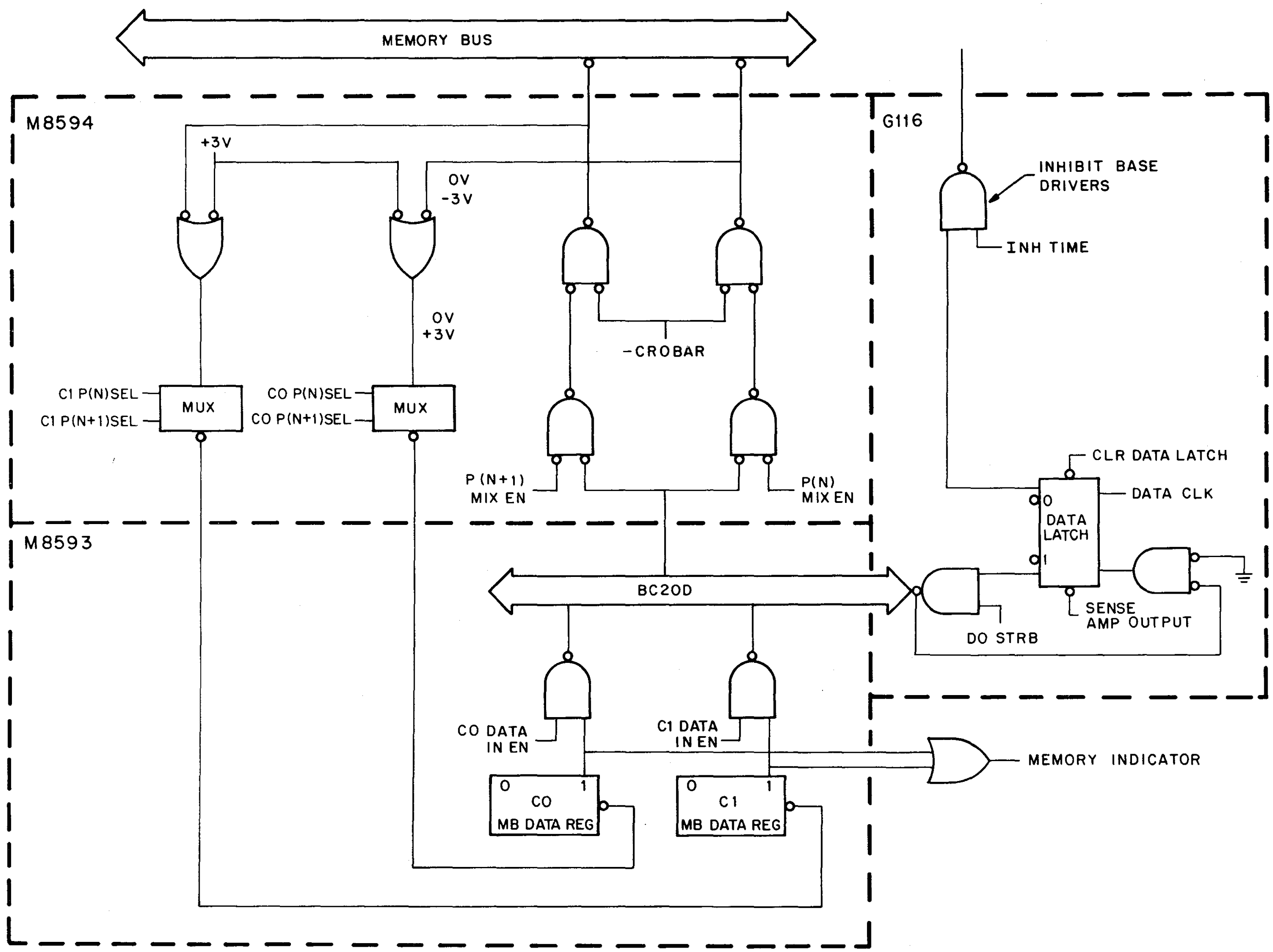
Priority	Port
First	P0 and P1 (Alternating)
Second	P2 and P3 (Alternating)
Third	P4–P7 (Rotating)

Second priority (for example) is alternated between ports P2 and P3 such that if P2 were serviced last in the previous memory cycles, then P3 would be given priority over P2 should simultaneous requests occur on those ports. The rotating priority goes downward from port 4 through 7, then back to 4 again. Priority logic for each control is located on the two M8590 Priority Control modules.

4.4.3 Memory Cycle Timing

As previously stated (Paragraph 4.3.1), data may be read from memory and sent to a processor (Read/Restore cycle); data may be transferred from a processor and written into memory (Clear/Write cycle); or data may be read from memory, sent to a processor, returned to the memory, and written into the memory at the same location from which it was originally read (Read/Modify/Write cycle).

The basic operations of memory cycle timing, the read operation and the write operation are common to the three memory cycles. Figure 4-5 illustrates the data path of information written into and read from memory.



10-2557

Figure 4-5 Data Path Diagram

The following paragraphs describe the various memory cycle operations. The times stated are all approximate. Because the two Memory Controller sections can overlap their operations, timing diagrams are not used. However, flow diagrams readily lend themselves to describe the memory operations. The main MH10 flow diagram should be referenced as an overall guide through each discussion. Where necessary, sectional flows are also provided.

The power-up conditions prepare the memory for receiving requests. The memory may also become initialized (again) after completing an operation. Either way, the memory is idle, waiting for a request.

Assuming a single step request is not being made, the MA STRBW pulse (described in Single Access Request, Paragraph 4.4.2.1), is delayed approximately 65 ns. It causes signal CYT1 C(N) CYC START to be generated. Once a request has been received and acknowledged, this signal commences all memory operations. The following memory cycle operations all begin at this time.

4.4.3.1 Clear/Write Cycle - Refer to Figure 4-6, Clear/ Write Cycle Flow Diagram, while reading this section. The discussion assumes that the MH10 is initialized, CYT0 AW RQ is set, and CYT1 CYC START has been produced.

During a Clear/Write cycle, a read operation is performed first; however, the data is lost because the sense strobe lines are disabled and the data is not strobed from the sense amplifiers. In effect, this is a destructive read operation that clears memory prior to writing new data into memory.

At the beginning of this cycle, the CYT1 C(N) CYC START signal asserts and the CYT1 C(N) RUN flip-flop is set. Signals MAT1 A EARLY, MAT1 INITIATE, and MAT1 READ EARLY begin the destructive read operation. Additionally, setting CYT1 C(N) CYC START asserts CYT1 C(N) SET DIN EN L, which sets the CYT1 C(N) MB SEL and CYT1 C(N) DATA IN EN flip-flops.

The active controller (C0 or C1) signal [C(N) Pn ACT] is ANDed with its respective controller MB SEL signal to produce the PAD0 C(N) Pn SEL H signals. They are then inverted and become the DAT0 C(N) Pn SEL L and DAT0 C(N) Pn+1 SEL L signals, which enable the Memory Buffer receiver multiplexors for the proper ports to receive the data from the processor.

While the core read portion of the Clear/Write cycle is being performed, the processor, after receiving the ADR ACK pulse from the MH10, sends back a Pn WR RS pulse along with the data and parity bits. The data is received from the processor (along with Pn WR RS) and loaded into the Memory Buffer. The selected CYT1 C(N) DATA IN EN level allows the data to be transferred from the Memory Buffer through the BC20D Core Interface cables to the data latches in the CMC section.

When MAT1 READ EARLY is negated, while the MAT1 WR EN flip-flop is set, the WRITE EARLY signal is asserted. This turns on the X and Y write current generators and the X and Y switches on the G236 module.. MAT1 WRITE LATE is asserted 75 ns later followed by MAT1 INH TIME after another 25 ns. MAT1 WRITE LATE turns on the X and Y write drivers. Accordingly, the MAT1 INH TIME signal provides the timing required for turning on the inhibit drivers.

MAT1 MG10 WR EARLY (N) is asserted at the same time as MAT1 INH TIME. The MG10 WR EARLY signal is sent to the controller as CAB C(N) ST OF WR. It is used to set the PRC1 C(N) Pn LAST flip-flop, stating which port is presently being accessed. Additionally, it asserts CYT1 STATE CLEAR, which resets the PAD1 C(N) Pn RQ, CYT1 C(N) MB SEL, DATA IN EN, DATA OUT EN, and RUN flip-flops: this disconnects the memory from the memory bus.

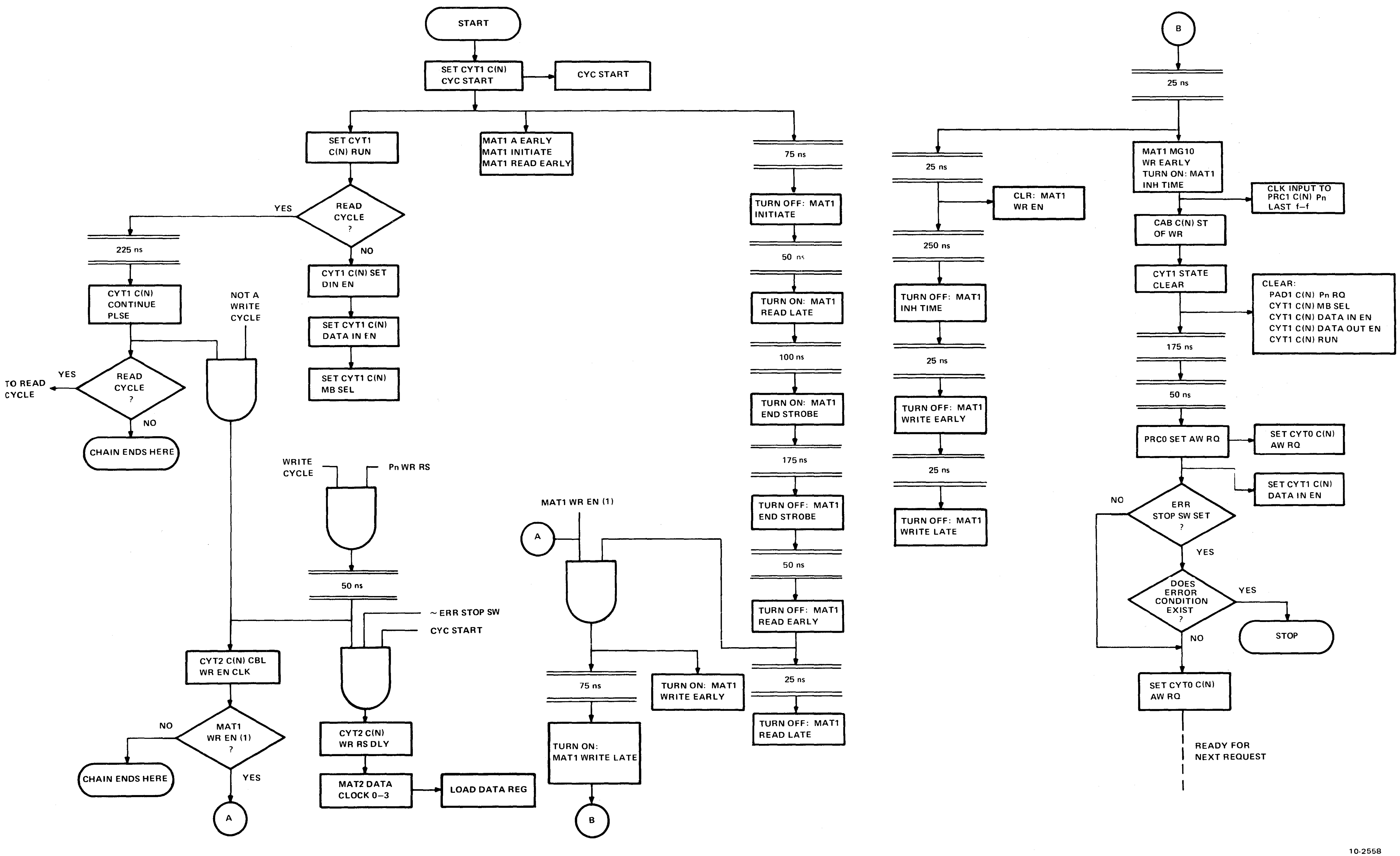


Figure 4-6 Clear Write Timing Flow Diagram

The MAT1 WR EN flip-flop is cleared next (after 25 ns). Another 250-ns delay then times out and negates the MAT1 INH TIME signal, disabling the inhibit drivers. Signal MAT1 WRITE EARLY is negated 25 ns later. This turns off the same current generators (X and Y write) and switches (X and Y) that it had previously turned on. Then, the MAT1 WRITE LATE signal is negated, turning off the X and Y write drivers and signaling the end of the write sequence.

Approximately 300 ns after the start of the write sequence, the PRC0 SET AW RQ signal asserts and sets the CYT0 C(N) AW RQ flip-flop, notifying the processor of the memory's availability for another access request. The CYT1 C(N) DATA IN EN flip-flop is also set at this time to gate out the contents of the Data and Address registers to the indicators.

The Pn WR RS signal, used to initiate the sending of the data and parity bits to the MH10, also triggers the CYT2 C(N) WR RS DLY. When it times out (after approximately 100 ns), it clocks the data into the CHK Data register, where parity is checked. Parity is checked by comparing parity of the 36 data bits with the parity bit. If an even number of ones is detected in the data plus the parity bit, a parity error is displayed. Odd parity is used, meaning that if the number of ones in the data bits is even, the parity bit should be a one.

4.4.3.2 Read/Restore Cycle Timing – Refer to Figure 4-7, Read/Restore Cycle Flow Timing Diagram, while reading this section. The Read/Restore cycle begins with the assertion of the CYT1 C(N) CYC START signal, which generates CYT1 C(N) RUN H and MAT1 A EARLY (N) L. The MAT1 A EARLY (N) L signal is advance timing to the G236 Driver module to turn on the Y read current generator, Y read driver, Y read switch, X read current generator, and X read switch. The X read driver is not turned on at this time, but waits for MAT1 READ LATE (N) L.

Because this is a Read/Restore cycle, signals MAT1 CLEAR 0 (N) L and CLEAR 1 (N) L are produced to clear the G116 Data register prior to the generation of the SENSE STROBE pulses. Approximately 75 ns after the CLEAR pulses reset the Data register, the MAT1 INITIATE L signal is negated. The MAT1 READ LATE (N) L signal is then asserted to turn on the read X drivers, which cause the read X current to start flowing. Approximately 100 ns later, the MATI END STROBE (N) L signal goes high. The SENSE STROBE signals DRVA SS0 L and SS1 L are generated by the output of a one-shot gated with MATI END STROBE being high. The leading edge of the SENSE STROBE signals can be varied (marginally) by placing the appropriate STRB MARGIN switch on the Memory Maintenance panel into the MAR position. This moves the leading edge of the SENSE STROBE signals, but does not affect the trailing edge. The SENSE STROBE signals in the memory stacks are wide to allow additional time for the core outputs to be propagated along the long sense lines and to propagate through the associated signal path delays.

At the end of a 175-ns delay, the MAT1 END STROBE signal negates and turns off the SENSE STROBE signal applied to the sense amplifiers. Then MAT1 READ EARLY (N) L negates, which turns off the X and Y current generators and the X and Y read drivers. When the MAT1 READ LATE (N) L signal negates approximately 25 ns later, the X and Y read switches are turned off.

The CYNT1 C(N) CYC START pulse at the top of the flow diagram (Figure 4-7) was asserted after the MA STRB pulses had loaded the correct memory address and desired type of request. Signal CYT1 C(N) CYC START also sets the CYT1 C(N) RUN flip-flop. Approximately 225 ns later, the CYT1 C(N) CONTINUE pulse is asserted. This is ANDed with the Read cycle to set CYT1 C(N) DATA OUT EN and CYT1 C(N) MB SEL flip-flops after another delay (120 ns). The CYT1 C(N) DO STRB 0–4 pulses are generated 80 ns later.

Signal CYT1 C(N) CBL DO EN H is sent to the G116 to gate out the strobed data residing in the G116 data latches. The gated-out data is sent to the data bus transceivers.

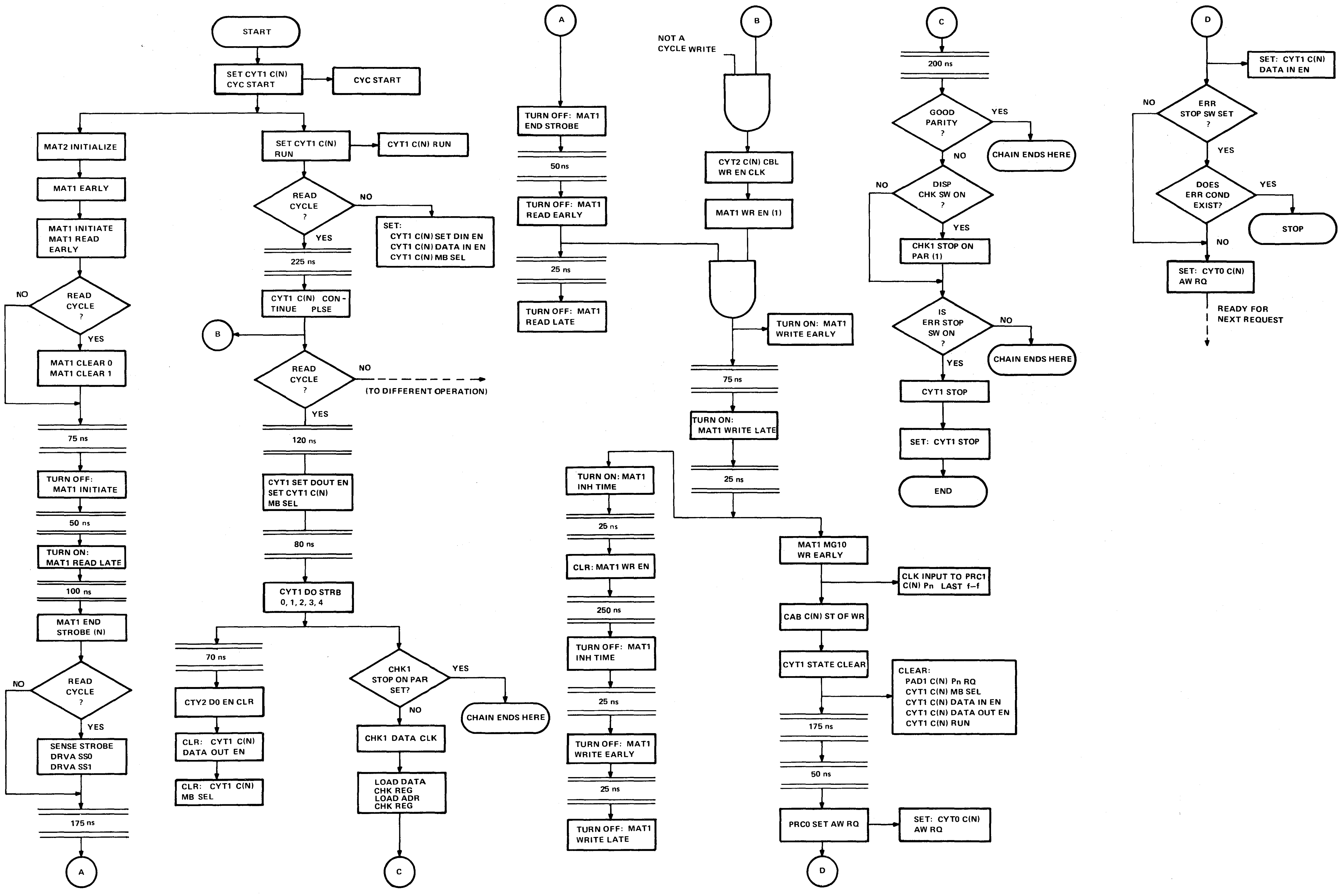


Figure 4-7 Read Restore Timing Flow Diagram

Signal CYT1 C(N) MB SEL is gated with the active port signal PRC1 C(N) P(N) ACT H to generate the port-selected signal PAD0 C(N) P(N) SEL H. This, in turn, is ANDed with CYT1 C(N) DO STRB to strobe the gated-out data from the data bus transceivers out onto the bus of the selected port.

The CYT1 C(N) DO STRB pulse is also used to clock gated-out data from the G116 into the CHK Data register, where parity is checked 200 ns later. Parity is checked by comparing the parity of the 36 data bits with the parity bit. Odd parity is used in the MH10, meaning that if the number of ones in the data bits is even, the parity bit should be a one.

The data read in the read portion of the Read/Restore cycle is sensed from the cores and strobed into the data latches. It is then gated by signal CYT0 C(N) DO STRB 0–4 H to the memory bus transmitters. This data, retained in the data latches, is then rewritten into the same memory locations it was read from.

The restore portion of the Read/Restore cycle is similar to the write portion of the Clear/Write cycle. Refer to Paragraph 4.4.3.1 (Clear/Write Timing) for a detailed description of the write portion of the Clear/Write cycle.

4.4.3.3 Read/Modify/Write Timing – During a Read/Modify/Write cycle, the read operation is performed first. The data read is then sent to the processor for modification and the Memory Buffer is cleared. The memory then pauses (20 μs maximum) to await the return of the modified data.

During the read operation, CYT1 C(N) DOUT EN sets the CYT1 C(N) MB SEL flip-flop, which remains set until CYT1 STATE CLR asserts. In addition, the AND of CYT0 C(N) WR RQ and CYT2 C(N) DOUT EN CLR (the DO STRB pulse delayed) sets the CYT1 C(N) DATA IN EN flip-flop, which also remains set until the assertion of CYT1 C(N) STATE CLR. When the modified data is sent from the processor along with Pn WR RS, a write operation is performed as in the Clear/Write cycle.

4.4.4 Detailed Memory Description

This section of the manual provides the user with a detailed theory of operation and the diagrams necessary to understand the MH10 Core Memory and Control (CMC) logic.

4.4.4.1 3-D 3-Wire Memory Fundamentals – Data is stored in ferrite cores by magnetizing the iron compound in those cores. A core that has been magnetized in the direction shown in Figure 4-8a, can be said (for example) to store a logic 1. Magnetization in the opposite direction (Figure 4-8b) would, then, represent a logic 0.

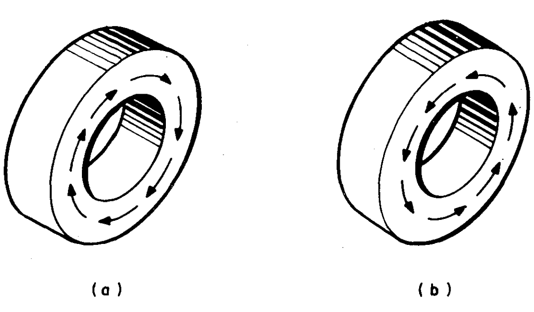


Figure 4-8 Magnetic States of Ferrite Cores

The magnetic state of the core can be switched from a logic 1 to a logic 0, and vice versa by a magnetic field induced by current flowing in a wire threaded through the core (Figure 4-9). Due to the hysteresis effect inherent in all ferromagnetic materials, the current must be large enough to produce sufficient magnetic field intensity to switch the core. Once switched, the core remains in its new state.

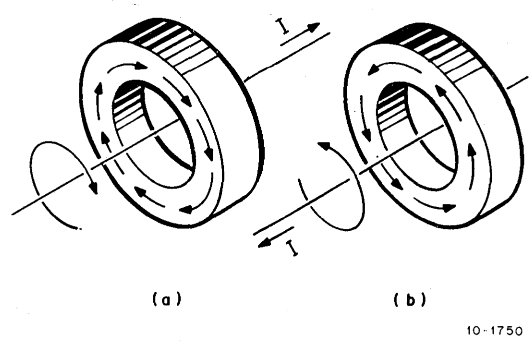


Figure 4-9 Switching Magnetic State of Ferrite Cores

In a 3-D, 3-wire memory configuration, three wires are threaded through each core. The combined magnetic field induced by currents flowing through two of these wires (X- and Y-windings) is used to change the magnetic state of the core. Figure 4-10 shows the 3-D, 3-wire core states. In this configuration, the sense winding also performs the inhibit function. The sense/inhibit lines are wound in parallel with the Y lines. When 0s are to be written in a location, half-select current flows in the inhibit lines in the direction opposite to write current in the Y lines. Those cores where 0s are written are, therefore, subjected to only half-select current in the write direction and do not switch to the 1 state. In a read cycle, the sense inhibit lines perform the normal sense function.

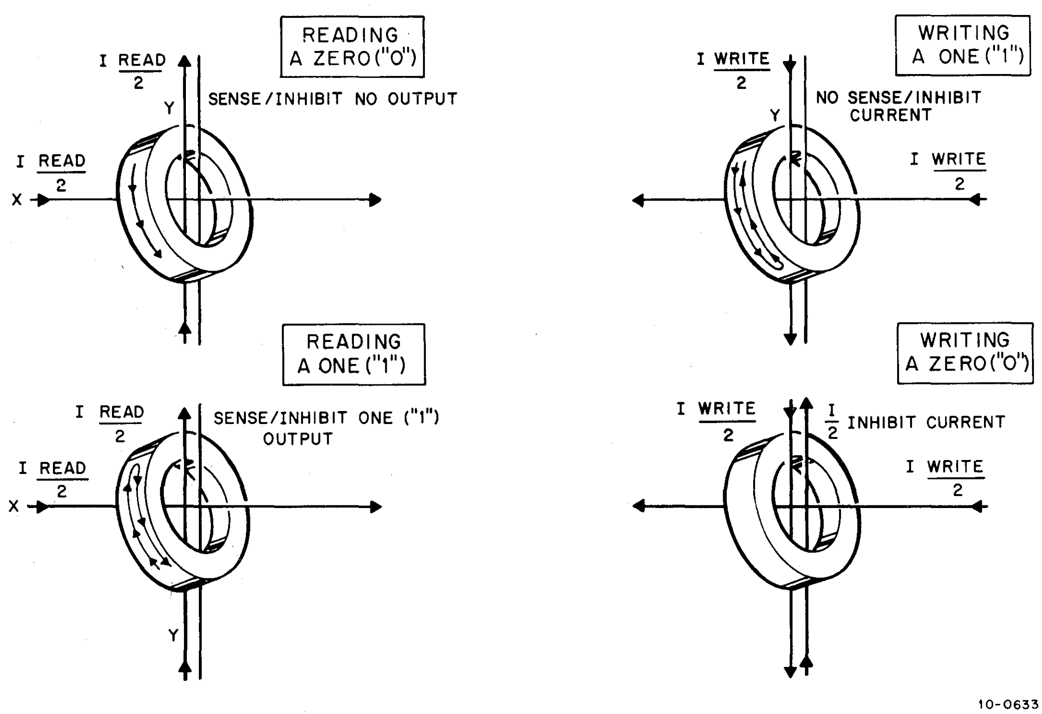


Figure 4-10 3-D, 3-Wire Core States

Note that the directions of current flow must be such that the magnetic fields tend to combine, rather than cancel. This means that X and Y currents required to change a core from state 1 to state 0 must be opposite in direction from the current required to change the core from state 0 to state 1. (If the direction of only one of the currents is reversed, the magnetic fields tend to cancel.)

It is worth reemphasizing that the X- and Y-windings enable the selection of cores, while the sense/inhibit winding implements the reading and writing function.

4.4.4.2 Core Array - The 32K, ferrite core, memory module consists of 19 memory mats arranged in a planar, or stack, configuration. The MH10 operates with stacks organized into 32,768 19-bit half-words; thus each stack contains 32,768 × 19 = 622,592 ferrite cores. The stack is constructed as a planar array of cores organized into 19 mats, with each mat containing 32,768 cores. All the cores in a mat store data corresponding to the same bit position of 32K words.

The 32,768 cores in each mat are arranged in a 256 × 128 array, with 256 X–current windings (X00–X255) and 128 Y-current windings (Y00–Y127) threaded through the cores. These windings form an X-Y coordinate matrix, as illustrated in Figure 4-11. The X- and Y-current windings on all the mats are connected in series, which means, for example, that if current is flowing in winding X35 in mat 0, then the same current is also flowing in winding X35 on the other 18 mats.

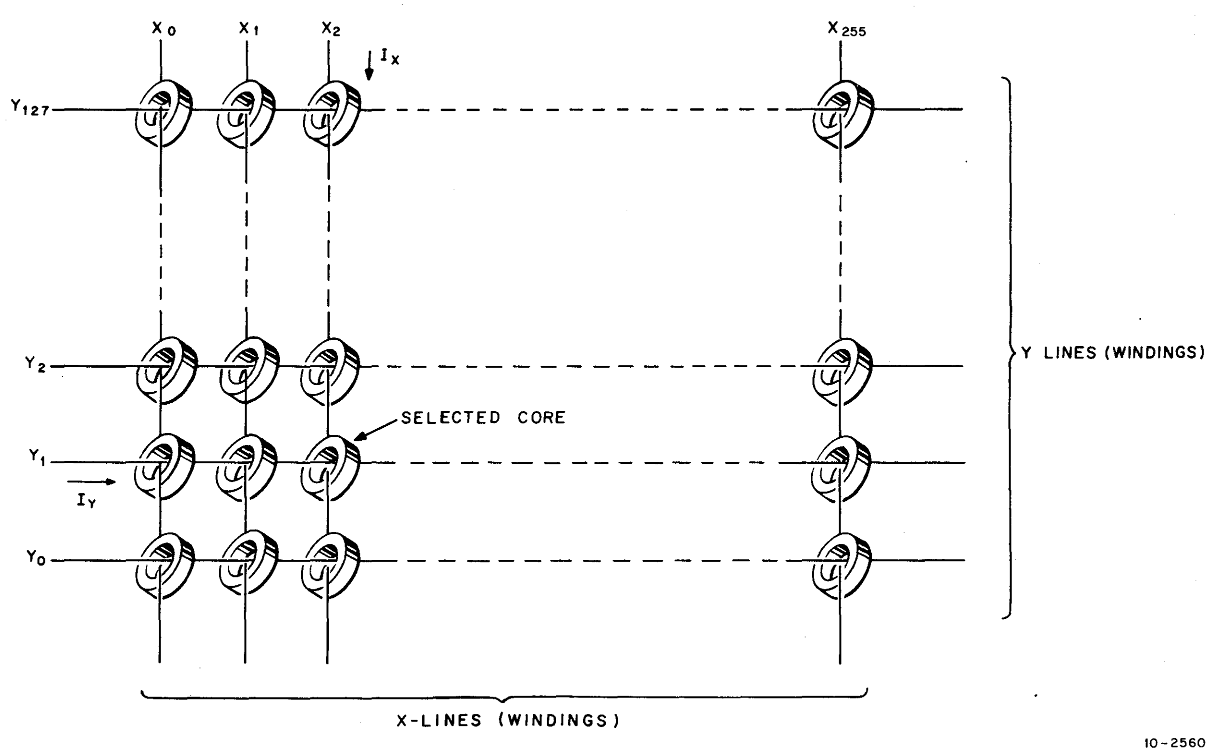


Figure 4-11 Core Configuration in a 256 × 128 Mat

As described earlier, both X- and Y-current is required to read or write data in a core. As a result of address decoding, current is switched through one of the X-windings and one of the Y-windings; this is the selected core within the mat. The set of 19 cores (one in each mat) that is selected by coincidence of X- and Y-current corresponds to the 19-bit word being addressed in the stack.

4.4.4.3 Memory Operation - The H224B Memory Stack is a standard 3-D, 3-wire, coincident current core array. The current passing through any one line (X or Y) is one-half that required to change the magnetic state of the core. The X and Y currents intersect once on each of the 19 mats, thereby producing full current at 19 cores. If the cores are being read, the current direction is such that the 19 cores are forced to the 0 state (destructive read); the other 32,767 cores on each mat are not affected. When an addressed core containing a 1 is switched to the 0 magnetic state, the resultant flux change is detected by the core's sense/inhibit line and a logic 1 is generated at the output of the sense amplifier on the G116 module.

The memory is accessed in a similar fashion during a write operation except that the current through the X and Y lines is in the opposite direction. All 19 cores are switched to the 1 magnetic state except on those cores having current applied to their sense/inhibit line. This current cancels the affect of the half-current in the Y line (inhibit current is in the opposite direction of Y write current) and the addressed core remains in the 0 state. For example, when a write operation is performed to complete a Read/Restore cycle, only those cores containing 1s originally are forced to the 1 state. All cores containing 0s originally have current applied to their sense/inhibit line during the Restore portion of the cycle. Figure 4-12 shows a 16-word by 4-bit planar memory. The 16K H217B Memory Stack is configured in the same manner, except that it has 256 X lines, 128 Y lines, and 19 core mats. The core stringing is identical, and each of the 38 sense lines (2/mat) is laced through 16,384 cores with the interchange between X127 and X128 instead of between X1 and X2.

4.4.4.4 Memory Addressing - The MH10 memory locations are addressed by bits 18-35 of the memory address (Figure 4-13) generated by the processor. These bits are capable of addressing 256K (262,144) locations. One H224B Memory Stack module contains 32K (32,768) half-word locations (19 bits). For each 32K full words, two H224B modules are used to store 36 data bits plus one parity bit.

4.4.4.4.1 Memory Bank Selection - The CMC Logic section is divided into two controllers and subdivided into four banks per controller (Figure 4-3). The four left stacks (looking at the MH10 from the front) store bits 00–17, and the four right stacks store bits 18–35 plus the parity bit. Each pair of stacks forms a bank. Thus, a bank pair (one for each controller) contains 64K 37-bit words. The selection of up to 256K addressable word locations is permitted using up to four bank pairs. Memory address bits 18–20 are decoded in the core interface logic to select the proper 32K data word bank (M0–M3) and controller (C0, C1). Memory bank decoding is shown in Table 4-2.

Table 4-2 Memory Bank Selection Decoding

Decimal Address	Bank Pair	Control No.	Address Contained (octal)	MA Bits		
				18	19	20
0K–32K	M0	0	000000–077777	0	0	0
32K–64K	M0	1	100000–177777	0	0	1
64K–96K	M1	0	200000–277777	0	1	0
96K–128K	M1	1	300000–377777	0	1	1
128K–160K	M2	0	400000–477777	1	0	0
160K–192K	M2	1	500000–577777	1	0	1
192K–224K	M3	0	600000–677777	1	1	0
224K–256K	M3	1	700000–777777	1	1	1

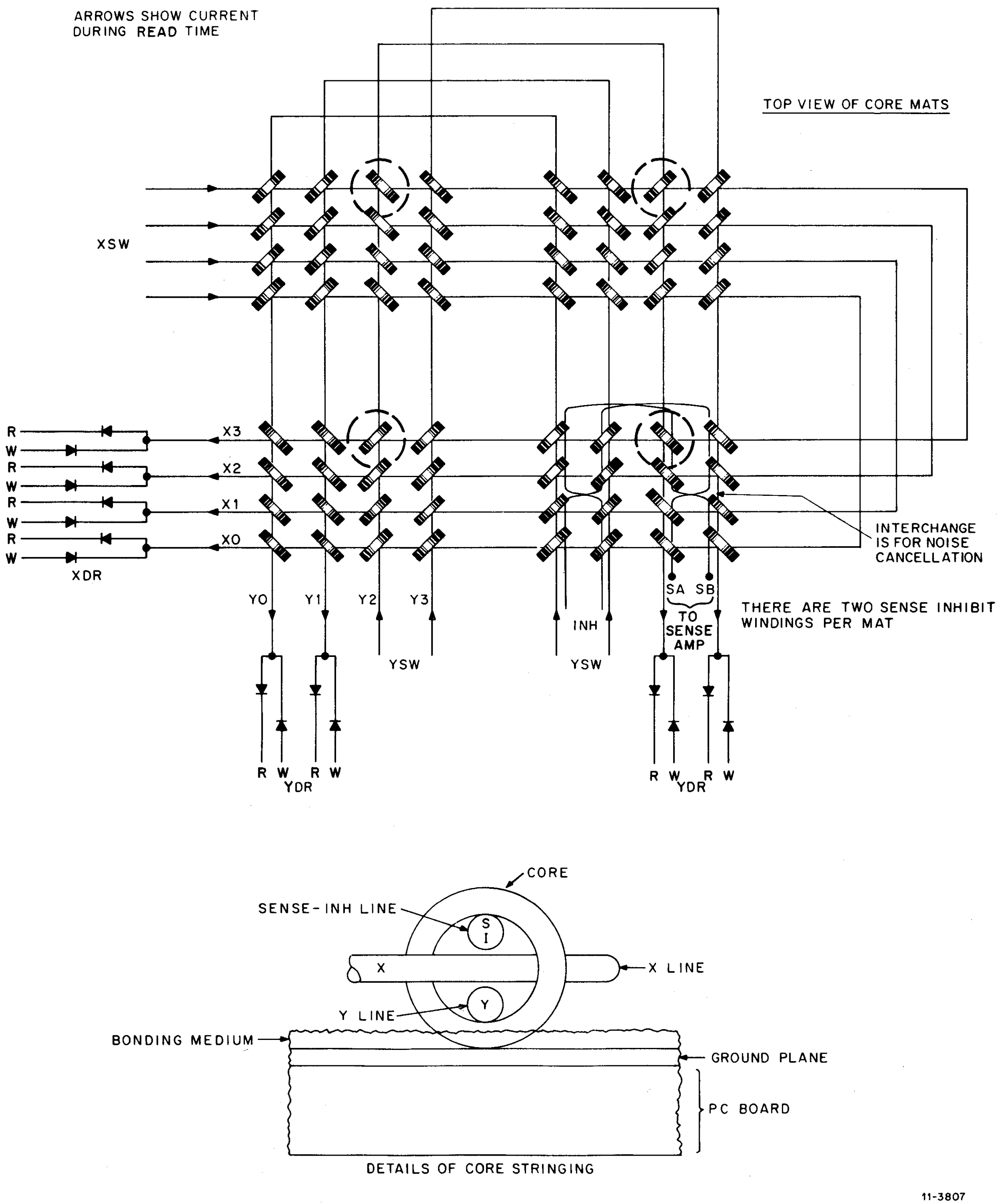


Figure 4-12 3-Wire, 3-D, 16-Word by 4-bit Memory

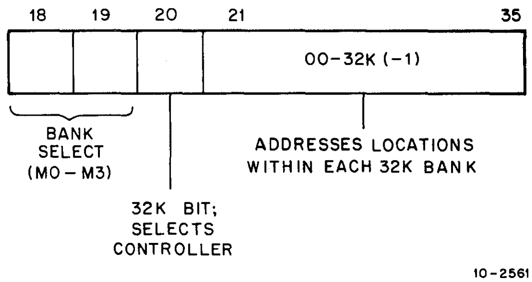


Figure 4-13 Memory Address

4.4.4.4.2 Data Word Selection - Some mechanism is required to perform word selection. As described previously, the 32K stacks used in this memory require that 1 of 256 X-windings and 1 of 128 Y-windings are energized to select a word. In a 3-D memory organization, this is accomplished by decoding and matricing (see Figure 4-14).

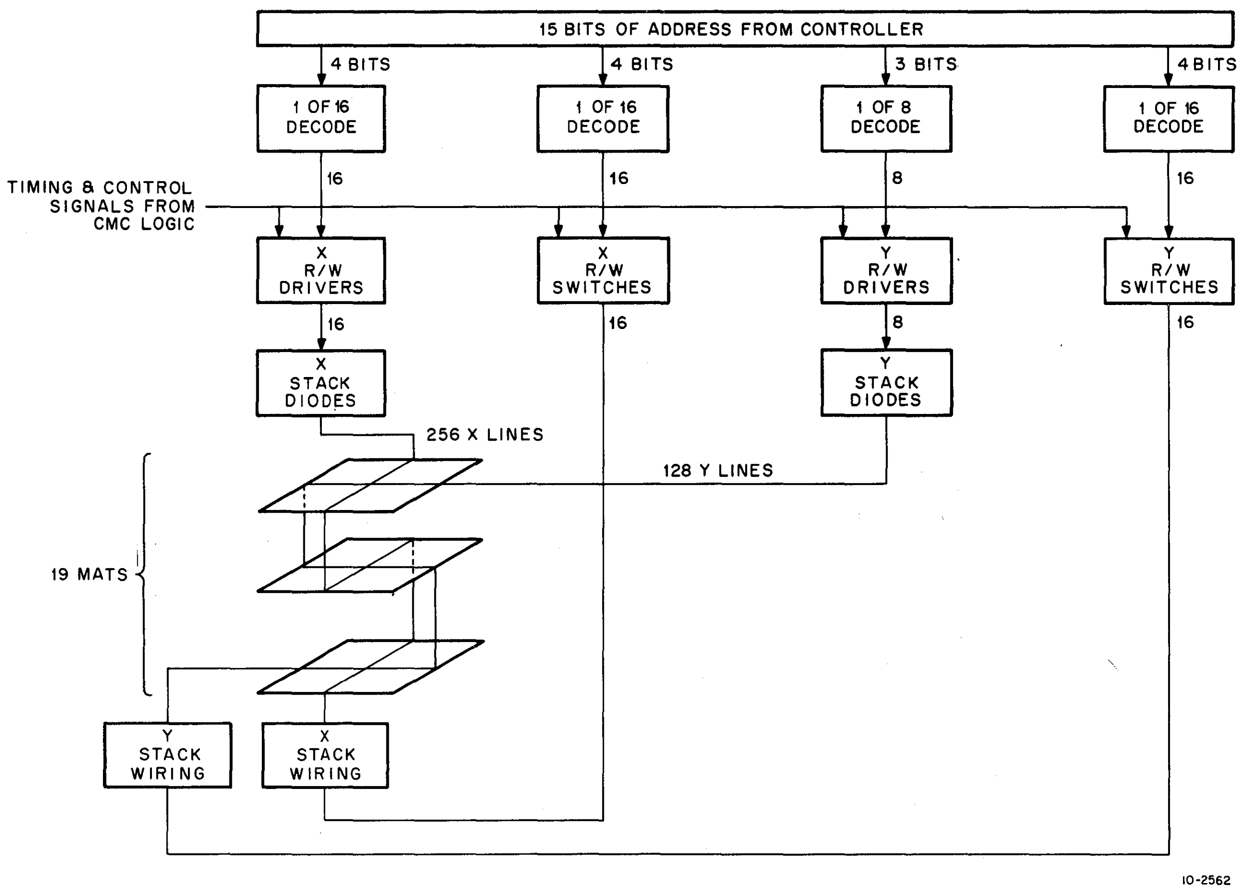


Figure 4-14 Word Selection Using 3-D Organization

Fifteen bits of the incoming address are decoded as follows:

4 bits select one of 16 X drivers
4 bits select one of 16 X switches
3 bits select one of 8 Y drivers
4 bits select one of 16 Y switches.

The outputs of the X drivers and switches are input to an X diode matrix. The outputs of the Y drivers and switches are input to a Y diode matrix. When timing and control signals from the CMC logic energize the selected drivers and switches, the X diode matrix energizes one of the 256 X-current windings; similarly, the Y diode matrix energizes one of the 128 Y-current windings.

In the MH10, memory address bits 21–35 are placed in the memory address latches. The outputs from the latches go directly to a group of type 7442 and 74154 decoder inputs. The outputs from the decoders select the proper X and Y read/write switches and drivers.

4.4.4.4.3 X and Y Line Decoding – The basic decoding units are type 7442 and 74154 4-line to 10-line, and 4-line to 16-line decoders. The inputs are D0, D1, D2, and D3; they are weighted 1, 2, 4, and 8, with D0 as the least significant bit. An output is selected according to the sum of the weighted inputs. The selected output is low and all others are high. Refer to Appendix A for truth tables of 7442 and 74154 decoders. Each 7442 controls 8 read/write driver pairs and each 74154 controls 16 read/write switch pairs. This switch matrix is combined with the stack X-Y diode matrix to allow selection of any location out of the total 32,768 locations (see stack drawing D-CS-H224-0-1 for interconnections).

The X and Y line transistors are differentiated first as switches and drivers. The drivers are those transistors that are connected to the diode end of the stack. Drivers and switches are further differentiated by function: either read or write. Another differentiation is made by polarity: negative or positive, depending on the physical connection. Read switches and write drivers are connected to the current generator outputs and are considered positive; write switches and read drivers are connected to ground and are considered negative.

4.4.4.4.4 Drivers and Switches – Drivers and switches direct the current through the X and Y lines in the proper direction as selected by the read and write operations. Each switch or driver is addressed by one decoder output. A low decoder output selects the associated read and write switch or driver. The 74154 decoders are connected to switches and X-axis drivers, and the 7442 decoders are connected to Y-axis drivers.

Figure 4-15 illustrates a portion of a Y selection matrix and shows the interconnection of the diodes and the lines from the switches and drivers. It illustrates how 4 pairs of switches and drivers are connected to select one of 16 lines. Refer to drawing H224-0-1 for an extension of this method which uses 16 pairs of switches and 8 pairs of drivers to select one of 128 lines.

Polarities are shown for convenience. The diodes are identified to assist in associating them with the drivers and switches. Each line from a twin diode interconnection to a read/write switch pair passes through 256 cores per bit mat and represents one line on each bit mat.

Assume that a read operation is to be performed and the word address decoders have selected read switch RYS00 and read driver YNRD1. The Y current generator sends current through read switch RYS00 (conventional flow) which places a positive voltage on the anodes of diodes 03R, 02R, 01R, and 00R. The anodes of the unselected switch lines are at ground because the stack charge voltage on the unselected switch lines are close to 0 V during the read portion of the core cycle. Read driver YNRD1, which has been selected, turns on and makes the cathode of diode 01R negative with respect to the anode which forward-biases it. The diode conducts and allows current to flow to read driver YNRD1. A half-select current now flows through this line that links 256 cores per bit mat (4864 total for 19 mats).

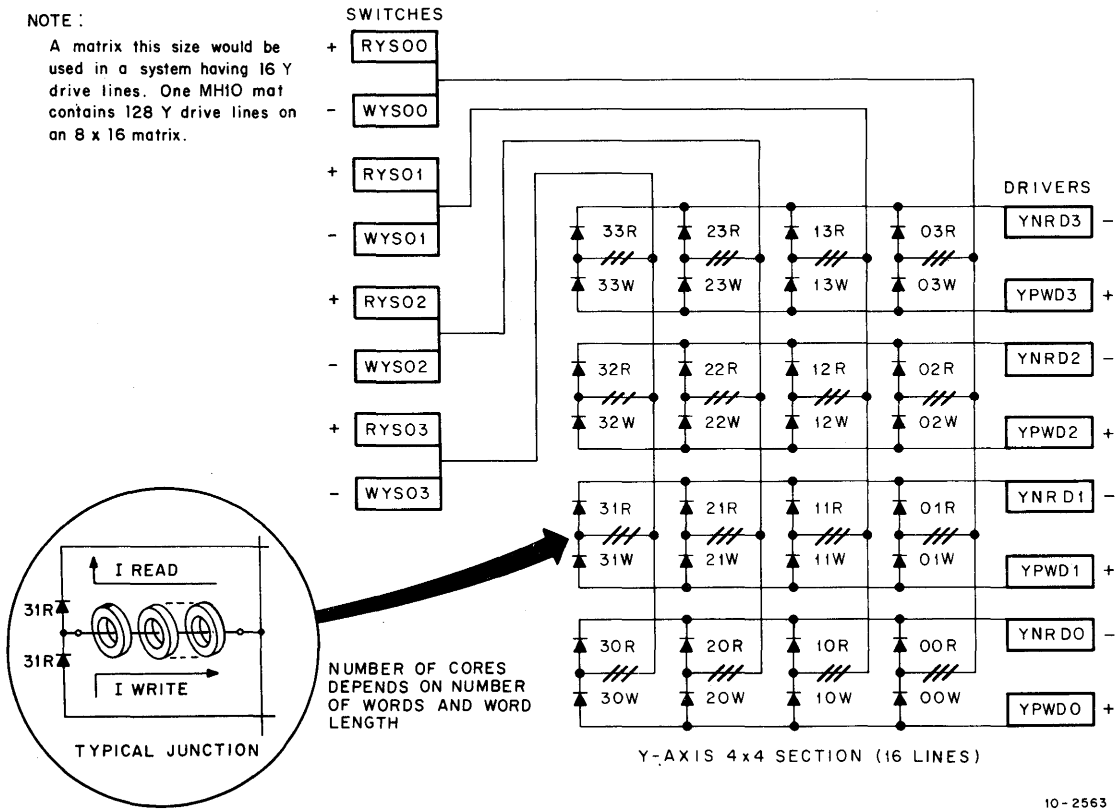


Figure 4-15 Simplified Y Line Selection Stack Diode Matrix

Figure 4-16 is a simplified schematic of two pairs of switches and drivers in the MH10 interconnected with the core stack and current generator. Read/write switches YS07 and read/write drivers YD7 are used as examples. These switches and drivers are chosen for convenience. For a read or write operation, 128 switch/driver combinations on the Y axis and 256 on the X axis are used. For a write operation, decoder E30 selects positive write driver E31 and decoder E16 selects negative write switch E19. Both E31 and E19 are turned on when they are selected and write timing occurs. E31 conducts, which allows current from the Y write current generator to flow through YPWD7, the associated matrix diode, and the cores on the selected line. After passing through the cores, the current flows through E19 to ground. For a read operation, decoder E16 selects positive read switch E20 and decoder E30 selects negative read driver E32. Both E20 and E30 are turned on by read timing. E20 conducts, which allows current from the Y read current generator to flow through E20, D47, and the cores in the opposite direction. After passing through the cores, the current flows through the associated matrix diode to ground. Read current flow is shown as a broken line; a solid line shows write current flow.

4.4.4.5 Read/Write Current Generation and Sensing – Four functional units are involved in generating current to switch the cores and detect their states. The X and Y line current generators supply the drive current (by switches and drivers); the inhibit drivers allow 0s to be stored during a write operation; the sense amplifiers detect 1s during a read operation; and the memory data latches (MDL) temporarily store data being transferred to and from memory.

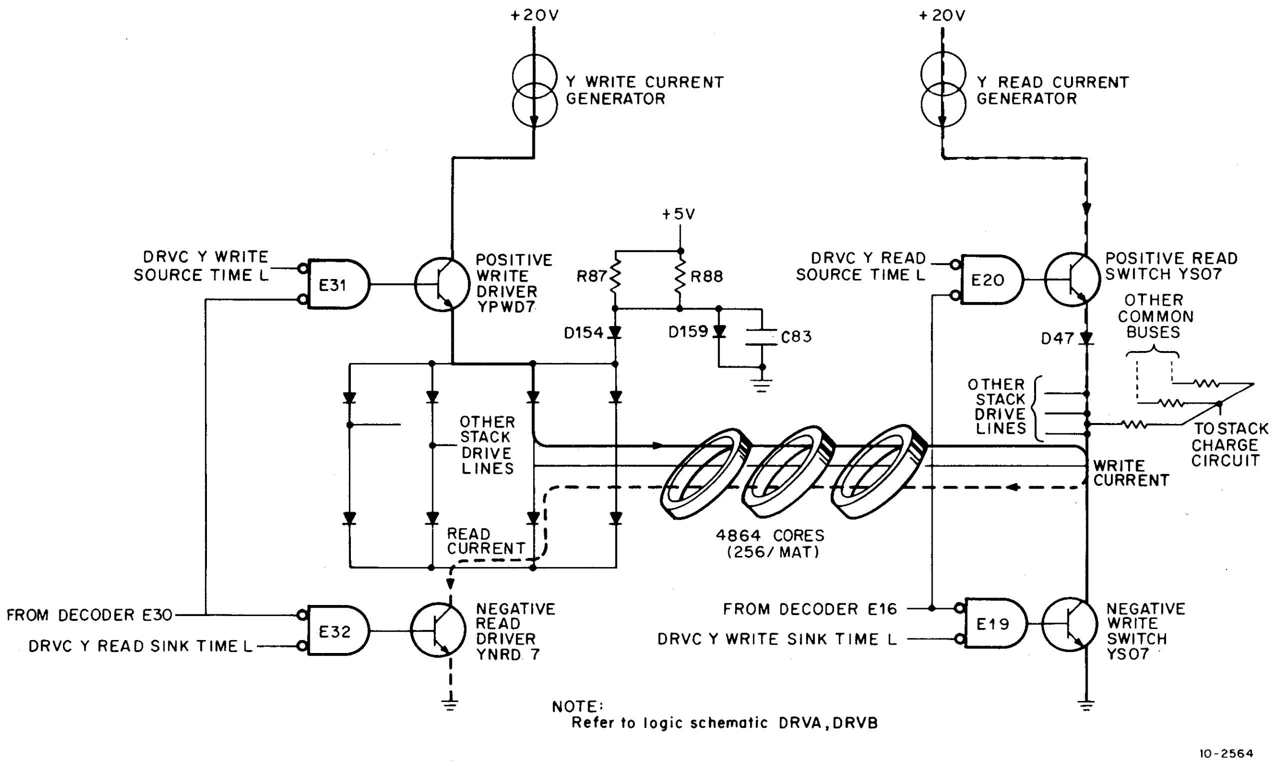


Figure 4-16 Typical Y Line Read Write Switches and Drivers

Components in the read/write data path for a typical data bit (D11) are shown in Figure 4-17. Note that with two sense windings per mat, the data path is split; that is, two sense amplifiers and two inhibit drivers are associated with one data bit. The one sense amplifier and the one inhibit driver selected during a memory reference depend on the memory address and interleave mode. When bus address bit 34 is equal to zero in normal or 2-way interleaved operation or when the address bit swapped with bit 34 (19, 18 or 17 depending on memory size) is equal to zero in 4-way interleaved operation, SINA SENSE STROBE 0 and SINA INH 1 are asserted to select one sense amplifier and inhibit driver combination. When bus address bit 34 (or the swapped bit) is equal to one, SINA SENSE STROBE 1 and SINA INH 2 are asserted to select the other sense amplifier and inhibit driver combination.

During a core read operation, half-select currents flow in the X and Y lines for the selected core in each bit mat. These currents flow opposite to the write currents. Therefore, cores in the 1 state are switched to the 0 state and cores in the 0 state remain unchanged. Assuming bit 11 is a 1 in core, switching the core from the 1 state to the 0 state induces a voltage pulse in one of the sense windings. This pulse is detected by sense amplifier E50 as a differential voltage at the input that exceeds the threshold reference voltage. This pulse is amplified and when SINA SENSE STROBE 0 H or SINA SENSE STROBE 1 H is generated, the output of the sense amplifier goes low. At the beginning of every cycle, the control generates SINA CLEAR MDR 0 L, which clears MDL flip-flop E48. The sense amplifier output is connected to the set input of the flip-flop and a low sets the 1 output (pin 9) high. The high from pin 9 of the flip-flop is sent to the input (pin 14) of bus driver E51. The other input to this gate is the OUTPUT ENABLE signal. When the control logic generates SINA OUTPUT ENABLE L, the output of E51 is low, a logic 1, asserting the data line for data bit 11. Timing diagrams for the sense operation are shown in Figure 4-18.

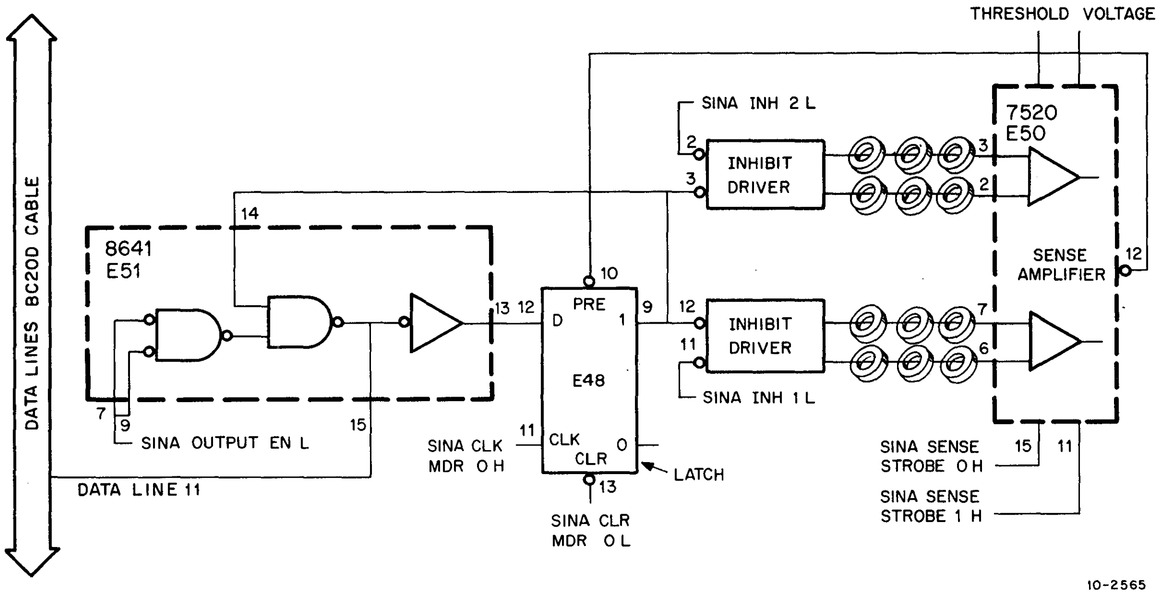


Figure 4-17 Read and Write Data Path

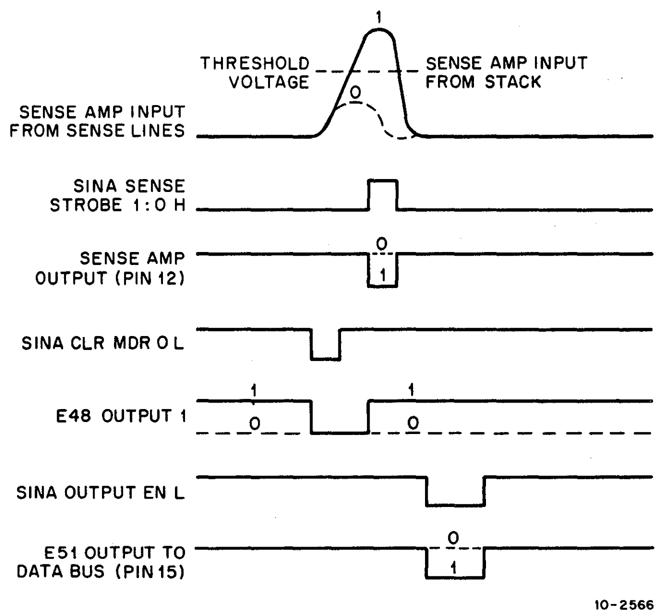


Figure 4-18 Timing Diagram for the Sense Portion of a Read Operation

The read operation is destructive; i.e., all cores at a specified location are switched to 0. The 1 bit that was read during the read operation must be restored by a write operation immediately following the read operation. Flip-flop E48 is still in the set state; therefore, its 1 output is high at the input to the inhibit drivers and inhibit current is not turned on when SINA INH 1 L or SINA INH 2 L is asserted by the control. With no inhibit current in the inhibit line to oppose the half-select Y line current, a 1 is written back into the appropriate core location.

If, however, bit D11 is 0 in core, it does not switch during the read operation and the output of sense amplifier E50 does not go low. Flip-flop E48 remains cleared; its 1 output (pin 9) is low, the data line is not asserted, and the appropriate inhibit driver is turned on by the SINA INH signal that is asserted during the subsequent write cycle. This produces a current that opposes the Y line current and prevents a 1 from being written into the appropriate core.

The memory operation just described is actually a read/restore operation. The requesting device wants to read a word from memory and, as an internal requirement, the memory must restore the word by writing it back in core. During a read/restore operation, the MDL flip-flops are set by the sense amplifier outputs when 1s are read from core. The flip-flop outputs are then used in the subsequent restore operation to control the inhibit drivers.

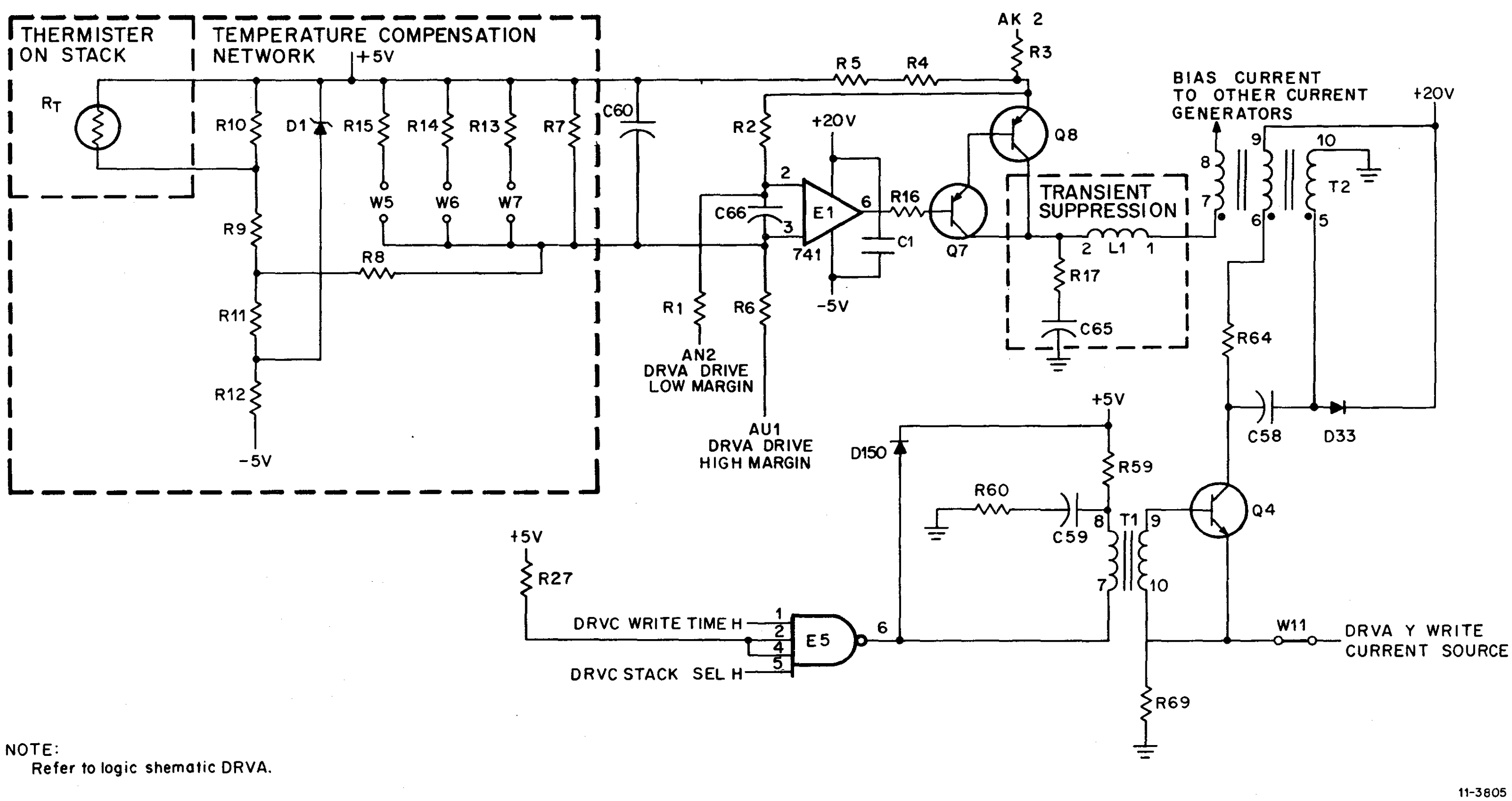
If the requesting device wants to write a word into memory (clear/write operation), it must load the data into the MDL flip-flops through the Data Line receivers. If data bit 11 is loaded (Figure 4-17), the bit is inverted by receiver E51 and sent to the D input (pin 12) of flip-flop E48. During the write operation, the control logic generates SINA CLK MDR 0 H, which clocks the flip-flop. If the D input is high, E48 is set, the inhibit driver is not turned on, and a 1 is written into the selected core. If the D input is low, E48 is not set, the inhibit driver is turned on, and the selected core remains in the 0 state.

4.4.4.5.1 X and Y Current Generators – A read and write current generator is provided for both the X and Y drive lines. The current generators and associated bias current supply are shown in drawing G236-0-1, sheet 4.

Optimum core switching requires current pulses of precise amplitude, duration, and shape. The current amplitude is controlled by the dc bias current supply which is temperature-compensated. Pulse shaping is achieved by resistor, diode, zener diode, and anti-overshoot circuits; duration is controlled by the timing pulses from delay lines.

Figure 4-19 shows the bias current supply and write Y current generator. The heart of the current generators on both the G236 (X-Y current generators) and the G116 (inhibit current generators) modules are special saturating transformers. The saturating transformer for the write Y current generator is T2. It is normally saturated very hard by bias current in the winding designated with pins 7 and 8. In order for the magnetic core of T2 to start to switch its magnetic flux in the opposite direction, the ampere turns applied by the bias current must be exceeded by an equal, *but opposite,* current in another winding. As long as T2 remains saturated, it is a low impedance to changes in current in any of its windings; however, once T2 starts to switch magnetic flux, large voltages may be induced across its windings in response to any additional changes in net current. That is, T2 acts like an ideal current source: low impedance with less than a specified current in winding 6–9, and a high impedance to additional current changes once the specified current amplitude is reached. This specified current is primarily determined by the bias current amplitude and the turns ratio of T2. The third winding of T2 (5–10) conducts current only after the drive current pulse has ended, and restores some current to the +20 V supply during that period. Although some losses occur in T2, most of the energy absorbed by T2 during the current pulse is restored to the power supply at the end of the pulse.

The bias current supply provides the dc bias current required for all the saturating transformers on the G236 and G116 modules (in series). LRC filter networks are provided at intervals to ensure that the bias current does not acquire ac components and that large voltages do not build up along the series path; L1, C65, and R17 comprise such a filter network protecting Q7 and Q8 from transients.



NOTE:
Refer to logic shematic DRVA.

Figure 4-19 Bias Current Supply and Write Y Current Generator

The resistor network, consisting of the stack termistor, R10, R9, R11, R12, R8, R7, R13, R14, R15, and zener diode D1, provides a temperature-compensated reference voltage to pin 3 of E1. R2 feeds back the emitter voltage of Q8 to pin 2 of E1. The 741 operational amplifier uses its gain to adjust its output (pin 6) so that the voltage on pin 2 is nearly equal to the voltage on pin 3. In this way, the amplifier circuit causes a current to flow through R4 and R5 which is precisely controlled by the reference voltage on pin 3 of E1. By measuring the voltage on AK2 with respect to +5 V, an accurate measurement of the bias current can be made because most of the current through R4 and R5 finds its way through the collectors of Q7 and Q8 (Q7 bias current is small) and becomes the bias current.

Module pins AN2 and AU1 provide a means of changing the amplitude of the bias current. Grounding AU1 through a 470K resistor (R6) causes the bias current to be reduced, and grounding AN2 through a 470K resistor (R1) increases the bias current. This capability becomes important for margining the memory.

CAUTION

Jumpers W5, W6, and W7 are factory-cut to adjust the bias current to its optimum value and they should not be changed.

In Figure 4-19, the operation of the write Y current generator is as follows: the output of E5 (pin 6) goes low when the current generator turns on. Current is coupled through T1 to saturate transistor Q4. Current then flows through T2 windings (pins 9 and 6, and 5 and 10), through Q4, and to the write Y switches. R64 and C58 primarily serve as a dc current limit and as a rise time aid, respectively.

When Q4 is turned off by E5 (coupling through T1), current flows through D33 until the core of T2 has been completely resaturated by the bias current. This places energy back in the power supply.

4.4.4.5.2 Inhibit Driver – A detailed schematic of the inhibit driver pair for bit D11 is shown in Figure 4-20. It is typical of all 19 inhibit driver pairs (drawing G116-0-1).

As explained in Paragraph 4.4.4.5, only one of the inhibit drivers in the inhibit driver pair is selected during a memory reference; that is, the control asserts either SINA INH 1 L or SINA INH 2 L at the input (pin 2 or 11) to E46. If a zero is to be written in bit 11 of the selected word, the output of E46 (pin 1 or 13) goes high, driving current through the primary winding of E47 to which the selected gate is connected. The secondary winding of that transformer provides the current to turn on Q27 or Q28. When turned on, current flows from the +20 V power supply, through fuse F14, saturating transformer E45, Q27 or Q28, isolation diodes, the sense/inhibit winding, and the diodes (D92 and D93 or D90 and D91) to ground. The value for the inhibit current is primarily determined by the bias current to transformer E45 (winding 3–12).

Each leg of the sense/inhibit sees half the inhibit current; approximate by 370 mA. Capacitor C125, diodes D88 and D89, and resistor R14 help reduce the power dissipated in Q27 or Q28 during turn-off.

Capacitors C123 and C124 allow the gate to pump reverse current into the transformer primary; they also help to decrease the turn-on time of Q27 or Q28.

4.4.4.5.3 Sense Amplifier – Sense amplifier circuitry for bit D11 is shown in Figure 4-20; it is typical of all 19 sense amplifier circuits (drawing G116-0-1). It consists of the sense amplifier IC, terminating capacitors for the sense/inhibit windings, and threshold voltage network.

As explained in Paragraph 4.4.4.5, there are two sense amplifiers per data bit. Each sense amplifier input connects to 16K cores. During a sense operation, the inhibit driver connection is an open circuit through driver transistor Q27 or Q28. The effect of the inhibit driver circuits and isolation diodes D92 and D93 or D90 and D91 can be ignored during the sense operation because the diodes are reversed-biased.

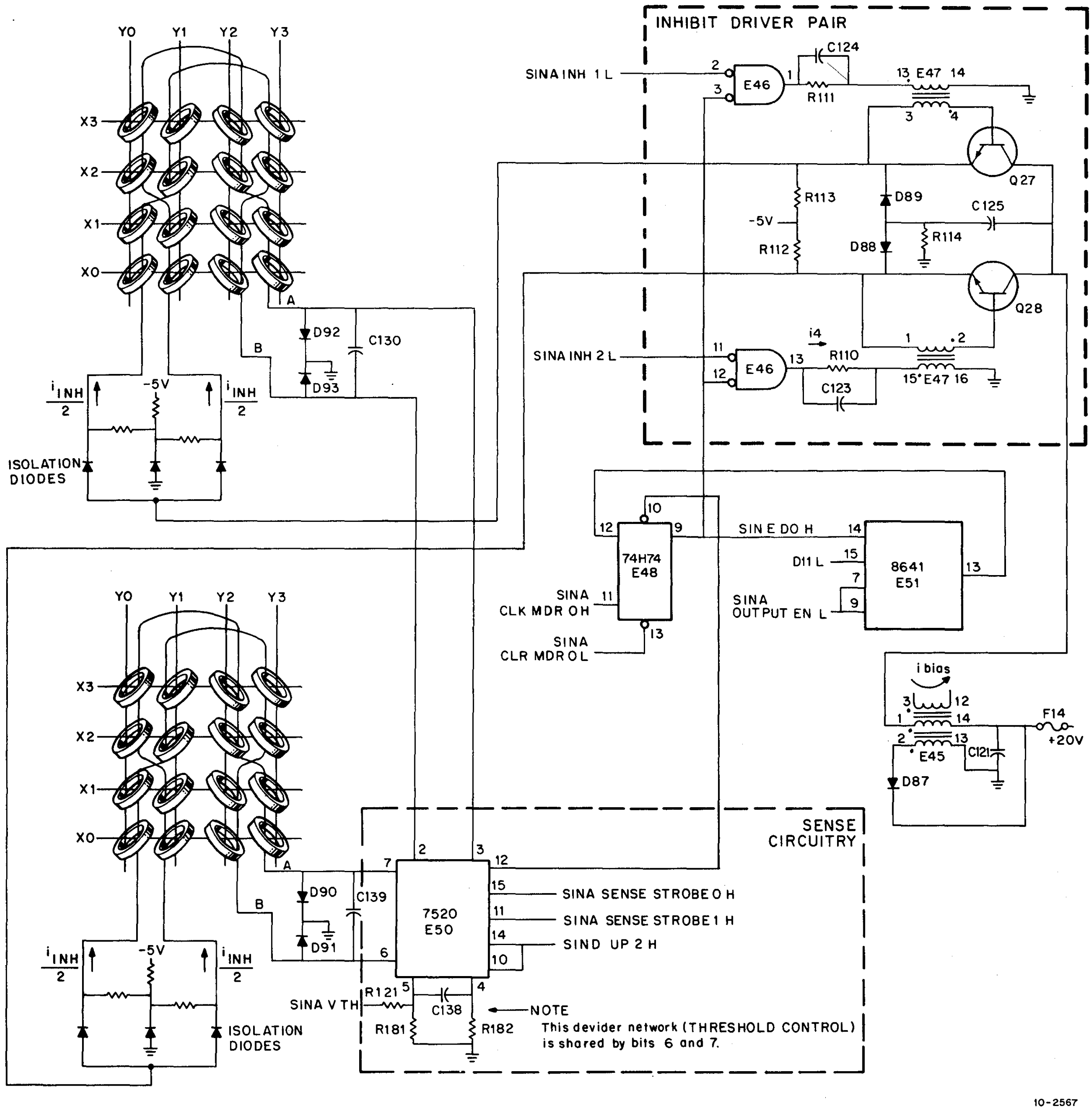


Figure 4-20 Sense Amplifier and Inhibit Driver

Sense amplifier E50 (type 7520), being a dual IC package, connects to both sense/inhibit lines of one mat. A simplified block diagram of the package is shown in Figure 4-21. Each interior circuit consists of a preamplifier and sense amplifier. The inputs to the internal sense amplifiers are available to facilitate accurate strobe timing. Both circuits share a reference voltage (or threshold voltage) amplifier (pins 4 and 5). In this application, pin 4 is grounded through resistor R182 and a positive threshold voltage of approximately 17 mV is supplied to pin 5. This voltage is obtained from the +5 V supply via the resistor voltage divider (Figure 4-20). Operation of the sense amplifier is discussed in Paragraph 4.4.4.5.

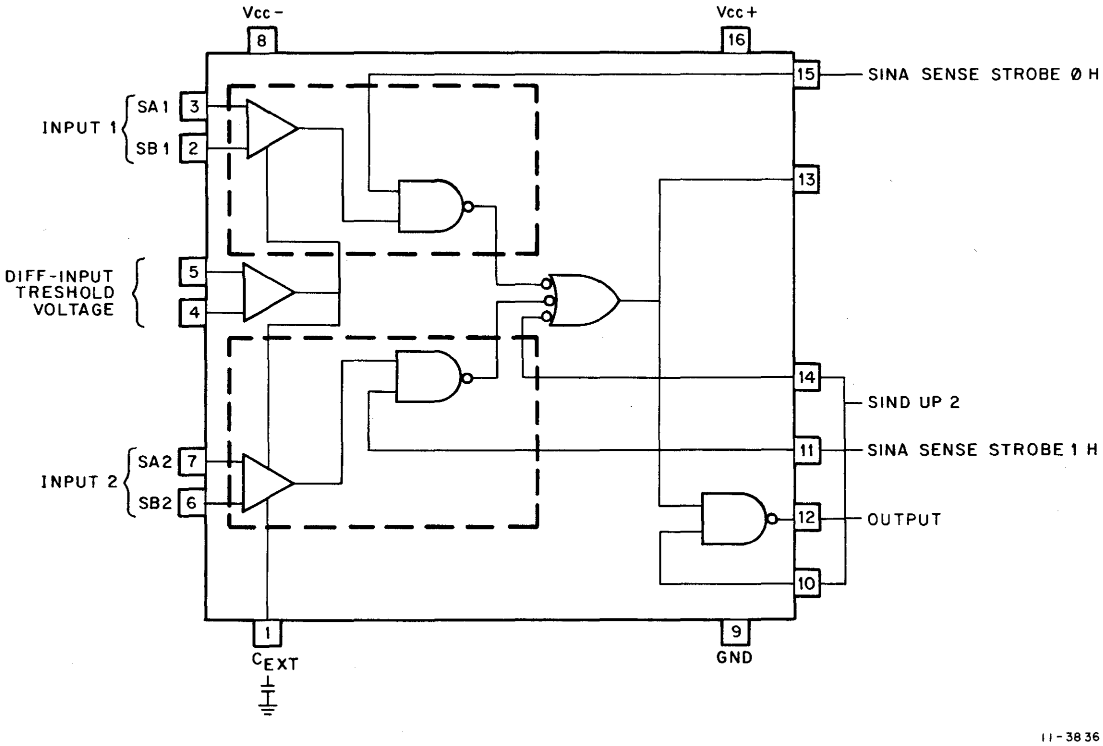


Figure 4-21 Type 7520 Dual Sense Amplifier

4.4.4.5.4 Memory Data Latches – The memory data latches (MDL) in one G116 form a 19-bit register that is used to store a word after it is read out of the memory, or to store a word prior to its being written into memory from the bus. It is composed of ten 74H74 dual high-speed D-type flip-flops. At the start of a memory read operation, the MDL register is cleared directly via the CLEAR input (pin 1 and pin 13) of each flip-flop. The basic register operations are discussed in Paragraph 4.4.4.5.

4.4.4.6 Stack Charge Circuit – The stack charge circuit assists the stack capacitance in recovering and shortens the rise time of the stack current. It also reduces unwanted currents in the unselected lines associated with the selected driver. It is located on the H224B module.

Figure 4-22 shows the stack charge circuit. The outputs are taken from the emitter of transistors and go to the junctions of each X and Y read/write switch pair via a capacitor and jumper. During a read operation, these outputs must be low (approximately 0 V). During a write operation, the outputs are approximately +12 V. The effective stack capacitance associated with each set of lines is shown as C_{STACK}.

During a read operation, the DRVA STK CHARGE TIME H signal is low, making the output of E1 (pins 6 and 8) high, thus saturating Q2 and Q3, and turning off Q1 and Q4. The output voltages of the circuit is also held low by the parallel combination of L1 and D123, and also L2 and D122. A current thus flows from +5 V, through R35 and R36, through L1 and L2, through R37 and R38, and through Q2 and Q3, to ground. Q1 and Q4 are off since their base-emitter junctions are not forward-biased.

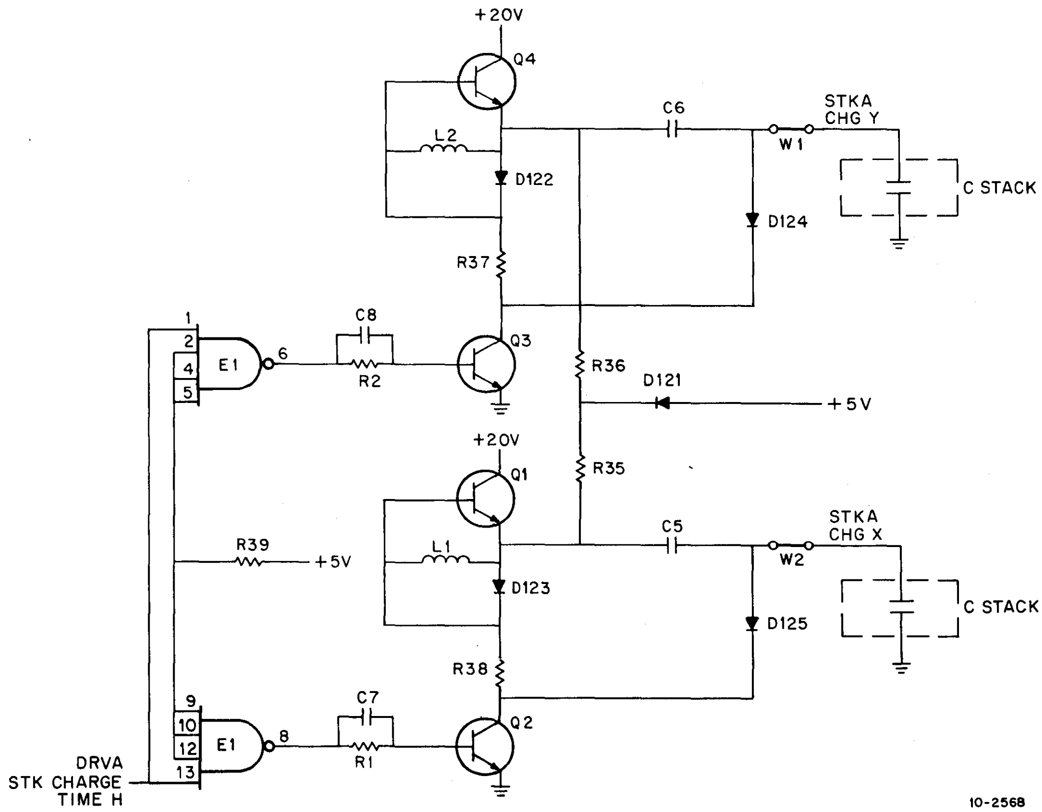


Figure 4-22 Stack Charge Circuit

During a write operation, the DRVA STK CHARGE TIME H signal goes high, making the output of E1 (pin 6 and 8) go low, thus turning off Q2 and Q3. Current that was flowing through L1 and L2 is forced to continue to flow, but now must flow into the base of Q1 and Q4. Hence, with Q1 and Q4 turned on (saturated) and Q2 and Q3 off, the output is equal to 20 V less $V_{CE\ SAT}$ of Q1 or Q4. Current spiking from Q1 and Q4 on the transitions is prevented by D122 and D123. When Q2 and Q3 turn on again, Q1 and Q4 must be fully off before current can flow through D122 and D123. This is due to the fact that if D122 and D123 are forward-biased, the base-emitter junction of Q1 and Q4 are reverse-biased.

4.4.4.7 DC LO Circuit - The 20–30 Vac secondary tap on each of the three H7420 MH10 memory power supplies is continuously monitored to detect any decrease in line voltage. If the line voltage to any of the supplies drops to about 80–86 Vac, signal DC LO L is asserted by the supplies. The DC LO L signals from the top two H7420 power supplies are wired together to pin BJ1 of the M8565 timing board (as signal CROBAR L) and reset the timing. Signal CROBAR L (now as signal C0 DC LO) goes through the BC20D cables to the M8566 Cycle Timing module, where it becomes CAB C0 CROBAR INPUT, clearing the cycle timing. The bottom H7420 DC LO signal is applied to the M8565 and M8566 for the right half (C1) of the stack logic as CAB C1 CROBAR INPUT. This signal, then, when distributed, terminates any operation underway, thereby preserving the integrity of the core memory and inhibiting any further memory accessing.

The MAT2 CROBAR L signal, developed on the M8565 Timing Board, goes to the G236 module (Figure 4-23). The signal is applied to Q11 on the G236, causing it to conduct and Q10 to go into saturation. This drives PWR OK H low and inhibits the X-Y current generators (Q1 through Q4). Also, transistor Q9 is turned off so that DRVA INT DC LO L is no longer asserted. On the G116 Sense Inhibit module, this asserts SINA PF L, which prevents the inhibit drivers (G116-0-1, sheets 4 through 8) from turning on.

NOTE

With DC LO L asserted, the generation occurs as described even though the +5 V and -5 V power supplies are turned off. The memory protection circuits operate even if the +20 V power supply is just above +5 V. If the +20 V supply produces less than +5 V, the circuits may not operate properly; this makes no difference, however, as no substantial driver currents are generated.

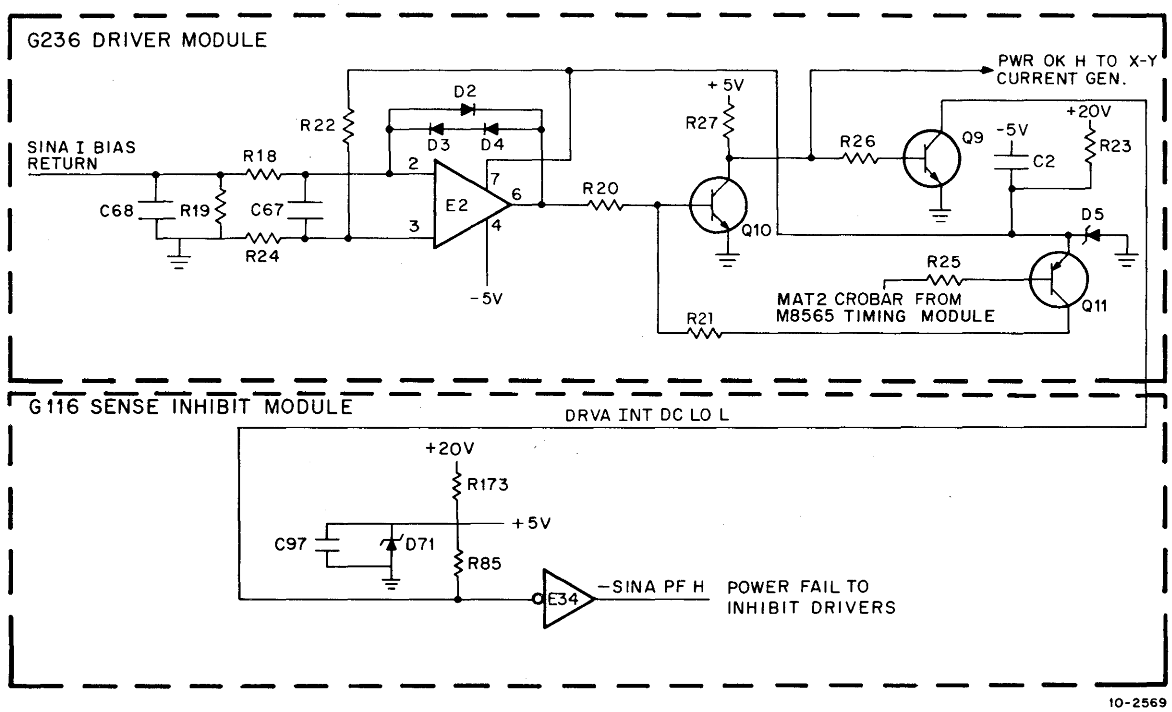


Figure 4-23 DC LO and Bias Current Detection Circuit

4.4.4.8 Loss of Bias Current – If bias current is lost, the current generators (G236-0-1, sheet 6) must be inhibited from turning on. If the current generators are turned on without bias current, it is possible that the saturating transformers may not sufficiently limit the inhibit current. The bias current source is applied to the inhibit drivers on the G116 Sense Inhibit Driver module and is returned to the G236 Driver module as the SINA I BIAS RETURN signal (Figure 4-23). The bias current is returned to ground through R19, generating a slight voltage across R19 which is detected by the differential amplifier. If the voltage across R19 is not sufficient, the amplifier output goes high and turns on transistor Q10. This action causes transistor Q9 to turn off and also causes the X-Y current generators to turn off in a manner similar to that described in Paragraph 4.4.4.7.

NOTE

If the G236 Driver module is removed from the system unit, DRVA INT DC LO L remains unasserted and SINA PF on the G116 Sense Inhibit module prevents the inhibit drivers from being turned on.

4.4.5 Power System

The MH10 power system includes the following major components:

1. One 857 power control

2. Three H7420 power supplies that include:

   a. Nine H744 5 V regulators
   b. Four H754 +20 V, -5 V regulators
   c. One H770 +15 V regulator.

These components are interconnected as shown on drawing D-IC-MH10-0-PW, AC-DC Power Wiring.

4.4.5.1 857 Power Control – The complete circuit schematic of the 857 power control is shown on three separate drawings:

1. D-CS-857-0-ACL shows ac line connection and control circuits.
2. D-CS-857-0-TMP shows temperature sensor and control circuits.
3. D-CS-857-0-RC shows remote control logic.

These drawings are referenced as ACL, RC, and TMP in the following descriptions.

4.4.5.1.1 System Power On – The MH10 power system is remote-controlled by the DEC power control bus which interconnects all cabinets in the system. The 3-wire DEC power control bus cable connects to J5 on the 857 power control. Connectors J6 and J7 are parallel with J5 to allow bus interconnection to adjacent cabinets. The DEC power control bus is defined as follows:

Pin	Signal
J5-1	SYSTEM POWER ON L
J5-2	EMERGENCY SHUTDOWN L
J5-3	GROUND

The DEC power control bus operations are summarized as follows:

1. Any connection between lines 3 and 1 energizes all cabinets on the bus.

2. Any connection of a ground to line 2 causes all cabinet power systems on the bus to shut down.

3. If no connection exists between lines 3 and 1, and no ground is connected to line 2, all components on the bus remain in the power OFF state.

The following paragraphs describe the operating sequence of the 857 power control functions. The timing for these functions is shown on the 857 power control flow diagrams and listed in the following chart:

Drawing	**Operating Sequence or Case**
D-FD-858-0-FL1	Normal power on, Case 1 Normal power off, Case 2 Solid power failure, Case 3
D-FD-858-0-FL2	Solid power return, Case 4 Short power on-off-on cycle, Case 5 Long power dip, Case 6
D-FD-858-0-FL3	Short power dip, Case 7 Short pulse in power, Case 8 Longer pulse in power, Case 9

4.4.5.1.2 Normal Power On – Connector pins J1-1 and -2 are jumpered to provide POWER SW ON, as shown on drawing TMP, POWER SW ON (1) causes the PWR SWD ON indicator lamp to light after 220 ms. Another jumper is connected between connector pins J3-5 and -12 so that when the SYSTEM POWER ON line on the DEC power control bus is switched to GROUND, BUS POWER REQUEST and POWER SW ON assert POWER REQUEST, as shown on drawing RC. Because no LOW VOLTAGE input connection is made to the MH10 857 connector pin J3-4, POWER REQUEST asserts POWER ALLOW as long as EMERGENCY SHUTDOWN is not grounded. Refer to drawing ACL. POWER DOWN LATCH (1) and POWER ALLOW produce POWER ON COMMAND. As -POWER ALLOW goes high, the POWER DOWN LATCH flip-flop latches in the 0 state.

With normal ac input voltage applied to the 857 power control, the +5 V POWER OK signal is available, as shown on drawing ACL, and POWER ON COMMAND asserts POWER ON DRIVE. POWER OK and POWER ON DRIVE are applied to separate sections of the K614 AC Switch module. When these signals are applied, the K614 AC Switch module completes the ac circuit to the coil of contactor relay K1. When K1 energizes, SWITCHED POWER is applied to the MH10 power supplies.

4.4.5.1.3 Normal Power Off – The MH10 power system is normally turned off remotely by removing the ground signal applied to DEC power control bus pin 1. When pin 1 goes high, POWER ALLOW goes low, as shown on drawing RC. Approximately 400 ms after POWER ALLOW goes low, POWER ON DRIVE goes low to deenergize contactor relay K1, as shown on drawing ACL.

The crobar control logic provided by the W519 module in the 857 is not used for MH10 power system control applications. The recycle delay logic prevents the MH10 normal power ON sequence from occurring less than four seconds after power OFF has been initiated.

4.4.5.1.4 Air-Flow Power Control – Four air-flow sense switches are located in the MH10 cabinet. If the flow of cooling air is interrupted at any of the four locations, an air-flow sense line is grounded. The air-flow sense line from all switches is connected to the 857 power control REG STACKS OK H line, as shown on drawing TMP. Any air-flow malfunction causes the OVERTEMP LATCH flip-flop to set, as shown on drawing ACL.

When OVERTEMP LATCH sets, it causes POWER ALLOW to go low and initiate the same power OFF sequence described for normal shutdown.

NOTE

When OVERRIDE switch S2 is ON, the power OFF sequence will not be initiated by OVERTEMP LATCH; however, the OVERTEMP indicator lamp will light.

4.4.5.1.5 Door-Panel Power Control – The door panels enclosing the stack and control logic are equipped with interlocking switches. If either of the door panels is opened while power is applied, the power OFF sequence is initiated to prevent the equipment from operating under abnormal cooling air flow conditions. This protection circuit can be overriden, for maintenance purposes, by setting the 857 OVERRIDE switch S2 to ON.

NOTE

If the OVERRIDE switch is ON, the PWR SWD ON indicator lamp on the 857 flashes as a warning to the technician servicing the equipment.

4.4.5.2 AC Power Distribution – Single-phase 115 or 220 Vac power is connected to TB1 on the 857 power control. A screwdriver-adjustable rotary switch, S11 (located on the 857 Power Control panel), is used to adjust the 857 for five ac input voltages: 100, 115, 200, and 240.

When the 857 power control is sequenced through the normal power ON function, the ac input is switched to the H7420 power supplies.

Cooling fans at the top of the MH10 cabinet receive ac input voltage directly from the 857 power control and are jumper-connected for 115 Vac or 230 Vac operation. Other fans in the cabinet receive ac input voltage from the H7420 power supply, which is prewired at the factory to provide 115 Vac outputs for cooling fans.

The 857 unswitched ac power outputs are not used for MH10 applications, but are available as convenience outlets to provvide test equipment power.

4.4.5.3 H7420 Power Supply – The H7420 power supply is a multipurpose power supply that can be implemented with several voltage regulator configurations, depending upon system requirements. For MH10 applications, it is used with nine H744 +5 V regulators, four H754 +20 V, -5 V regulators, and one H770 +15 V regulator.

Interconnections among the H7420, the voltage regulators, and the cabinet cooling fans are shown on drawing D-IC-MH10-0-PW. Because the H7420 is designed for multipurpose use, it provides several outputs that are used for other applications. Only those circuits that provide outputs used in the MH10 power system are described in the following paragraphs. The H7420 circuit schematic is D-CS-H7420-0-1. Jumper connections for 115 Vac or 230 Vac operation are shown on the schematic. Input voltage across the primary of transformer, T1, is also applied to the power supply cooling fan. The secondary windings provide 20–30 Vac to each of the voltage regulator inputs.

4.4.5.3.1 DC LO Sensing – The MH10 DC LO sensing circuit is located on the power control board of the H7420 power supply. The power control board circuit schematic is C-CS-5409730-0-1. The H7420 secondary provides 20–30 Vac to the DC LO sensing circuit. The 20–30 Vac input is rectified and stored by capacitor C3, which charges and discharges at a known rate whenever the ac power is switched on and off. Thus, the voltage applied to the emitters of differential amplifier Q6/Q7, across R17, is a rising or falling waveform of known value. For example, when ac input power drops, through shutdown or failure, the dc voltage decays at a known rate, as determined by the RC time constant. If the voltage decreases to the point where the base of Q6 becomes negative with respect to the base of Q7, the increased forward bias on Q6 causes it to conduct more current, and the resultant decrease in Q7 causes it to cut off. This removal of voltage across R16 causes Darlingtons Q16/Q17 to conduct. This, in effect, connects the DC LO output at J4-12 to the DC LO RET at J4-7. As a result, DC LO goes low when the ac power input voltage drops below a minimum level required for MH10 operation. DC LO is a natural result of the normal power OFF sequence, as well as an indication of primary power failure. The DC LO signal is used to inhibit memory timing and prevent further memory requests from being accepted. When ac input power is restored, the DC LO goes high, and the RESET signal is generated by the cycle initiate logic.

4.4.5.3.2 +15 V Output – The power control board of the H7420 power supply also contains a +15 V/+8 Vdc supply which receives 15–24 Vac from the secondary of transformer T1. This ac input is full-wave rectified by diode bridge D1. The resultant dc is applied to Darlington power amplifier Q1, through fuse F1. The bias on Q1 is controlled to provide +15 Vdc at output pins 2 and 3 with respect to output pins 4, 5, and 6 (ground). If the Q1 collector voltage starts to increase, the bias at the base of Q2 conducts slightly more current to maintain a constant output voltage. Zener diode D7 provides approximately +8 V at output pin 1; the +9 V output is not used in the MH10. When DC LO is grounded at output pin 9, Q2 conducts hard to cut off Q1 completely, thus removing the +14 V output.

4.4.5.4 +5 V Regulators – Seven H744 +5 V regulators are used in the MH10 power system. Drawing D-IC-MH10-0-PW shows where the H744s are used in the power system; the H744 circuit schematic is D-CS-H744-0-1.

4.4.5.4.1 Regulator Circuit – The 20–30 Vac input is full-wave rectified by bridge D1 to provide a dc voltage (24–40 Vdc, depending on line voltage) across filter capacitor C1 and bleeder resistor R1. Operation centers on voltage regulator E1, which is configured as a positive switching regulator. A simplified schematic of E1 is shown in Figure 4-24. E1 is a monolithic integrated circuit that is used as a voltage regulator. It consists of a temperature-compensated reference amplifier, error amplifier, series pass power transistor, and the output circuit required to drive the external resistors. In addition to E1, the regulator circuit includes pass transistor Q2, predrivers Q3 and Q4, and level shifter Q5. Zener diode D2 is used with Q5 and R2 to provide +15 V for E1. Q5 is used as a level shifter; most of the input voltage is absorbed across the collector-emitter of Q5. This is necessary because the raw input voltage is well above that required for E1 operation. This +15 V input is supplied while still retaining the ability to switch pass transistor Q2 on or off by drawing current down through the emitter of Q5.

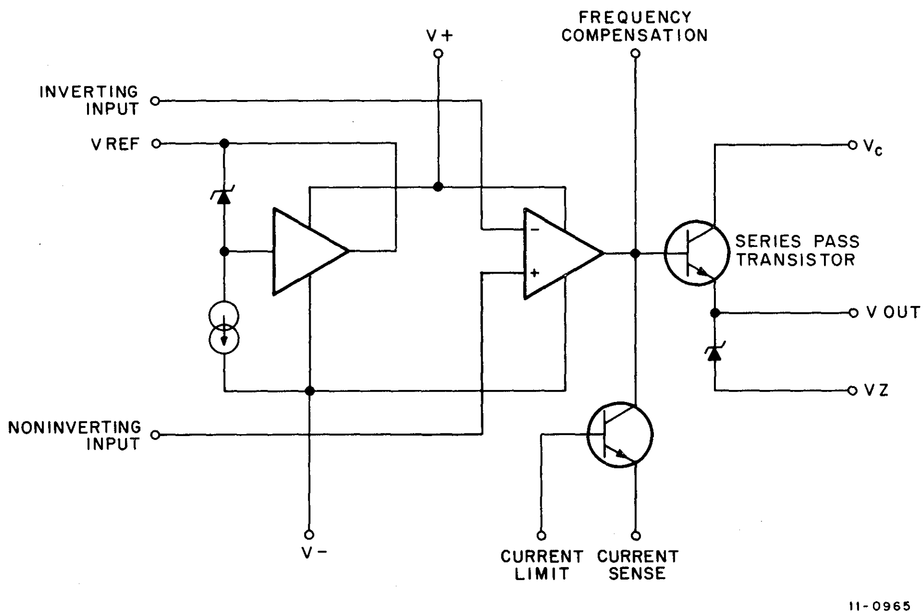


Figure 4-24 Voltage Regulator E1, Simplified Diagram

The output circuit is standard for most switching regulators and consists of diode D5, choke coil L1, and output capacitors C8 and C9. These components make up the regulator output filter. Diode D5 is used to clamp the emitter of Q2 to ground when Q2 shuts off, providing a discharge path for L1.

In operation, Q2 is turned on and off, generating a square wave of voltage that is applied across D5 at the input of the LC filter (L1, C8, and C9). Basically, this filter is only an averaging device, and the square wave of voltage appears as an average voltage at the output terminal. By varying the period of conduction of Q2, the output (average) voltage may be varied or controlled, supplying regulation. The output voltage is sensed and fed back to E1, where it is compared with a fixed reference voltage. E1 turns pass transistor Q2 on or off, according to whether the output level decreases or increases. Defined upper and lower limits for the output are approximately +5.05 V and +4.95 V.

During one full cycle of operation, the regulator operates as follows: Q2 is turned on and a high voltage (approximately +30 V) is applied across L1. If the output is already at a +5 V level, a constant +25 V would be present across L1. This constant dc voltage causes a linear ramp of current to build up through L1. At the same time, output capacitors C8 and C9 absorb this changing current, causing the output level (+5 V at this point) to increase. When the output, which is monitored by E1, reaches approximately +5.05 V, E1 shuts off, turning Q2 off; the emitter of Q2 is then clamped to ground. L1 discharages into capacitors C8, D9, and the load. Predrivers Q3 and Q4 are used to increase the effective gain of Q2, ensuring that Q2 can be turned on and off in a relatively short period of time.

Conversely, once Q2 is turned off and the output voltage begins to decrease, a predetermined value of approximately +4.95 V is reached, causing E1 to turn on. E1, in turn, causes Q2 to conduct, beginning another cycle of operation. Thus, a ripple voltage is superimposed on the output and is detected as predetermined maximum (+5.05 V) and minimum (+4.95 V) values by E1. When +5.05 V is reached, E1 turns Q2 off; when +4.95 V is reached, E1 turns Q2 on. This type of circuit action is called a "ripple regulator."

4.4.5.4.2 +5 V Overcurrent Sensing Circuit – The overcurrent sensing circuit consists of: Q1, R3 through R6, R25, R26, Q7, and C4. Transistor Q1 is normally not conducting; however, if the output exceeds 30 A, the forward voltage across R4 is sufficient to turn Q1 on, causing C4 to begin charging. When C4 reaches a value equal to the voltage on the anode gate of Q7, Q7 turns on and E1 is biased off, turning the pass transistor off. Thus, the output voltage is decreased as required to ensure that the output current is maintained below 35 A (approximately) and that the regulator is short-circuit protected. The regulator continues to oscillate in this new mode until the overload conditions is removed. Capacitor C4 then discharges until E1 is allowed, again, to turn on and the cycle repeats.

4.4.5.4.3 +5 V Overvoltage Crobar Circuit – The following components comprise the overvoltage crobar circuit: zener diode D3, and silicon-controlled rectifier (SCR) D7, D8, R22, R23, C7, and Q6. Under normal output voltage conditions, the trigger input to SCR D7 is at ground because the voltage across zener diode D3 is less than +5.1 V. If the output voltage becomes dangerously high (above +6.0 V), diode D8 conducts and the voltage drop across R23 draws gate current and triggers the SCR. It fires and short-circuits the +5 V output to ground. The SCR remains on until the capacitors discharge.

4.4.5.5 H754 +20, -5 V Regulators – Four H754 +20 V, -5 V regulators are included in the MH10 power system. The H754 circuit schematic is D-CS-H754-0-1; it is referenced in the following paragraphs.

4.4.5.5.1 Regulator Circuit – The regulator circuit has a voltage doubler input, and an output that consists of two shunt regulator circuits: one for the +20 V, the other for the -5 V. The +20 V shunt regulator consists of transistors Q4, Q10, and Q11; the -5 V shunt regulator consists of Q6 and Q9. Both Q10 and Q9 are pass transistors.

The output of the basic regulator is 25 V (-5 V to +20 V). The shunt regulators are connected across this output with a tap to ground between pass transistors Q9 and Q10. The voltage at the bases of Q6 and Q4 varies with respect to ground, depending on the relative amount of current drawn from the +20 V and -5 V outputs of the regulator. If the +20 V current increases while the -5 V current remains constant, the output voltage at the +20 V output tends to go more negative with respect to ground. This causes the -5 V output to go more negative also, because the output of the basic regulator is a fixed 25 V. This change is sensed at the bases of Q6 and Q4; Q6 conducts, causing Q9 to conduct, thus increasing the current between -5 V to ground, until the balance between the +20 V and the -5 V is restored. At this time, neither Q6 nor Q4 is conducting. If the -5 V current increases, Q4 and Q10 conduct to balance the outputs.

4.4.5.5.2 Overvoltage Crobar Circuits – Two crobar circuits are used in the H754: Q7 and its associated circuitry for the +20 V, and Q12 and its associated circuitry for the -5 V. Either circuit can trigger SCR D9.

4.4.5.5.3 Overcurrent Sensing Circuit – The overcurrent circuit is composed mainly of Q1, Q8, Q13, and Q14. The total peak current is sampled by R4. When the peak current reaches approximately 14 A, Q1 turns on sufficiently to establish a voltage across R7 and R38, thus firing Q8. This pulls the voltage on pin 4 of E1 up above the reference voltage on pin 5, thereby shutting off Q2. D6 now conducts, and the current through R37 turns on Q14, which turns on Q13. This keeps Q8 on for a time determined by the output voltage and L1. This action, in turn, allows the off-time of Q2 to be greater than the on-time; the off-time increases as the overload current increases, thereby changing the duty cycle in proportion to the load. The output current is thus limited to approximately 10 A.

4.4.5.5.4 Voltage Adjustment - The +20 V adjustment (R17) is located on the side of the H754; the -5 V potentiometer (R21) is on the top, next to the connector. To set the output voltages, power down, disconnect the load, power up, and adjust for a 25 V reading between the +20 V and -5 V outputs with the 20 V potentiometer. Then set the -5 V between its output and ground. Power down, reconnect the load, and power up; then check and adjust the outputs again. This procedure is necessary because the +20 V potentiometer (R17) actually sets the overall output of the regulator (25 V from +20 V to -5 V), while the -5 V adjustment (R21) controls the -5 V to ground output.

4.4.5.6 H770+15 V Regulator - One H770+15 V reglator is included in the MH10 power system. The H770 circuit schematic is D-CS-H770-0-1; it is referenced in the following paragraph.

4.4.5.6.1 Regulator Circuit - The basic H770 circuit design is the same as the H744 (+15 V regulator) with the following differences:

1. The addition of transistors Q2 and Q8
2. The addition of zener diodes D9 and D11.

Switching transistor Q2 is used to control the application of +15 Vdc to E1. The +15 Vdc is applied to E1 only after the MH10 has been energized (via the 857 power control) for approximately five seconds so that the cooling fans are up to speed.

Transistor Q8 provides remote turn on/off for the crobar circuit. A ground on J1-1 turns Q8 off, which, in turn, turns off Q2 and Q6. With Q6 off, Q3 is off, and no +15 Vdc output appears at J1-3 and J1-5. When the crobar is removed (i.e., when J1-1 is open), Q8 is turned on causing Q3 to be turned on and +15 Vdc to be applied to output pins J1-3 and J1-5.

Zener diodes D9 and D11 establish the voltage at the junction of R23 and R25 to a value of approximately +3.6 Vdc. R23 is a start-up resistor for D9 and D11.

CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION
This chapter discusses the preventive and corrective maintenance procedures that apply to the MH10 Core Memory. A major point in the maintenance philosophy of this manual is that the user understand the normal operation of the memory as described in the previous chapters. This knowledge, plus the maintenance information included in this chapter, will aid the user in isolating and correcting malfunctions.

5.2 JUMPER CONFIGURATION
Depending on the processor (KA10, KI10, etc.) and the memory mix (MH10, MG10, etc.) connecting to an MH10 bus port, various jumpers are installed at the corresponding Quick Latch connector and on the module backplane. Refer to drawings D-BS-MH10-IS0 and 1 for jumper configuration.

A second set of jumpers designated W1 through W7 is located on the G236 Driver module (sheet DRVA). Jumpers 1 through W4 control the strobe margin. Jumpers W5–W7 control the bias current. The cutting of jumpers on the G236 Driver module is a factory adjustment and should not be changed in the field.

5.3 PREVENTIVE MAINTENANCE
Preventive maintenance consists of specific tasks performed at intervals to detect conditions that could lead to subsequent performance deterioration or malfunction. The following tasks are considered preventive maintenance items and are recommended to be performed as noted.

1. Visual inspection (monthly)
2. MAINDEC testing (monthly)
3. Strobe and drive current margins (quarterly)
4. Voltage measurements (quarterly)
5. Sense strobe delay check (quarterly)
6. Drive current check (quarterly)
7. Delay check (quarterly)

The two pieces of test equipment recommended for checking and troubleshooting the memory are the Tektronix 453 Dual Trace Oscilloscope or equivalent, and the Weston Schlumberger Model 4443 Digital Voltmeter or equivalent, with 0.5 percent accuracy.

CAUTION

Make sure all power is off before installing or removing modules. Use special care in positioning sense inhibit cables (flat, 40-conductor) to prevent pinching them when the logic cabinet doors are closed. Avoid scraping cables with side two of the adjacent board as insulation damage may result.

5.3.1 Visual Inspection

Visually inspect the modules and backplane for broken wires, connectors, or other obvious defects. Determine that all fans are running freely and that the air filters are not clogged.

NOTE

All tests and adjustments must be performed in an ambient temperature range of 20° to 30° C (68° to 86° F.)

5.3.2 MAINDEC Testing

Load and run the diagnostic programs in Paragraph 5.5. No errors are permitted.

5.3.3 Strobe and Drive Current Margins

Run MAINDEC-10-DDMMG using the Maintenance panel MARGIN switches (Figure 3-4). The diagnostic should run error-free at both HIGH and LOW margins for each MARGIN switch setting (STRB, THRESH, and CUR).

NOTE

Although more than one MH10 cabinet in a system may be margined simultaneously to minimize preventive maintenance downtime, only one switch setting at a time (either STRB, THRESH, or CUR) should be utilized in one MH10 cabinet. Both CONTROL 0 and CONTROL 1 may be margined at the same time, however.

5.3.4 Voltage Measurements

Turn on the primary power and measure the +20 V, +5 V, and -5 V at the module backplane. All voltages must be within ±5 percent tolerance.

5.3.5 Sense Strobe Delay Check

To check sense strobe delay, connect channel A of the scope to pin FS1 and channel B to pin CN2 of the G236 Driver module associated with the 32K stack set being tested. Run MAINDEC-10-DDMMG with the Maintenance panel MARGIN switches off. The correct delay is 160 ns ±20 percent after the X read driver (FS1) turns on. Measure the delay from the 5 V point on the falling edge of the waveform at FS1 to the 1.5 V point on the falling edge of the waveform at CN2 as shown in Figure 5-1.

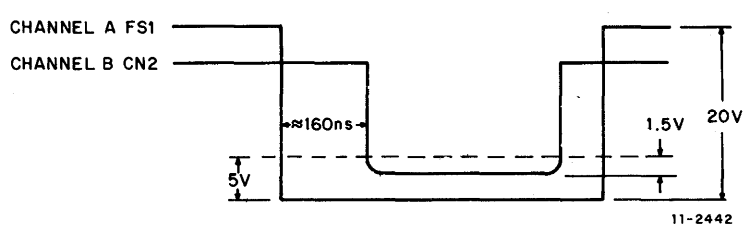


Figure 5-1 Sense Strobe Delay Waveform

5.3.6 Drive Current Checks

Connect a digital voltmeter (Weston Schlumberger Model 4443 or equivalent) between pin AK2 and +5 V on the G236 Driver module associated with the 32K stack set being tested. The drive current is factory-set to provide appropriate drive margins and results in a voltage measurement of 335 mV ±15 percent below the +5 V at 25° C (78° F).

5.3.7 Delay Check

Verify ADR ACK (T) and DATA WARNING timing. Delay times and adjustment procedures are specified on drawing D-BS-MH10-0-IS0 and 1.

5.4 CORRECTIVE MAINTENANCE

This paragraph describes various adjustment procedures for specific corrective maintenance. It also includes aids for performing corrective maintenance, including a troubleshooting chart, waveforms for the sense inhibit circuits, and waveforms for the drive circuits.

NOTE

The G236, G116, and H224 modules comprising a 32K stack set are factory-adjusted as a unit. Thus, if one module fails, all three modules should be replaced with a spare matched set. Return the faulty set to the factory for repair.

5.4.1 Voltage Adjustment Procedure

1. Refer to the power wiring diagram (D-IC-MH10-0-PW) for the location of the MH10 voltage regulators and the corresponding power tabs on the module backplane.
2. Power up and measure the voltage at the +5 V power tabs on the backplane. Set to +5 V by adjusting the +5 V potentiometer located on the top of the appropriate H744 regulators.
3. Measure the voltage at the +20 V power tabs. Set to +20 V by adjusting the +20 V potentiometer (R17) located on the side of the appropriate H754 regulator.
4. Measure the voltage at the -5 V power tabs. Set to -5 V by adjusting the -5 V potentiometer (R21) located on the top of the appropriate H754 regulator.
5. Repeat steps 3 and 4 until no further adjustment is necessary.

5.4.2 Parity Error

When a read/write parity error occurs, the Maintenance panel OVERRIDE CHECK switch (if left in the CHECK position) allows the MH10 to latch the data, address, active port, and the read/write request associated with the failing memory reference. The information is displayed in the MH10 indicator lights when the CONTROL 0/CONTROL 1 switch is in the proper position; that is, when the switch setting corresponds to the parity error light that is lit.

MH10 write data parity errors are usually caused by failures in the processor (CPU or channel) or memory bus cables connecting to an MH10 port. (The active light for the port producing an error is latched by the CHECK switch.) However, failures in the MH10 PCCI logic (e.g., a bad transceiver or Data register) will also cause parity errors during a write operation. The PCCI (port control and core interface) logic and the other major portion of the MH10, the CMC (core memory and associated control) logic, are detailed in Figure 4-2.

MH10 read parity errors are caused by failures in the CMC logic. A failure in the PCCI logic during a read operation causes parity errors to be detected in the processor connecting to the MH10.

Each of the two controllers in the MH10 has its own parity checker. Also, the controller active during a read or write is dependent on interleave mode. Thus, during troubleshooting, switching interleave modes and noting the parity error indications may aid in isolating the failing data path.

5.4.3 Sense Strobe Delay and Drive Current Adjustments

Correction of any failure in either the sense strobe delay or drive current circuits on the G236 module that would require reconfiguration of the jumpers within these circuits should *not* be attempted in the field. Replace the G236 (and associated G116 and H224) modules and return to the factory for repair.

5.4.4 Corrective Maintenance Aids

Figure 5-2 is a troubleshooting chart arranged as a 2-axis grid that identifies fault versus location. Figure 5-3 shows the sense/inhibit circuitry for a stack set and Figure 5-4 shows the various waveforms associated with the sense/inhibit circuitry. The encircled letters in Figure 5-3 are keyed to the waveforms in Figure 5-4. The drive circuitry for a stack set is shown in Figure 5-5 and the associated waveforms are shown in Figure 5-6. The encircled letters in Figure 5-5 are keyed to the waveforms indicated in Figure 5-6.

The waveforms are taken using worst case memory patterns. Signal MAT1 A EARLY L at pin AL2 of the M8565 module can be used as a sync signal for the scope. Minor variations in the waveforms may be observed between different memory systems.

5.5 MAINDEC TESTING

Certain DEC programs can be used to test various memory operations as an aid to troubleshooting. The purpose of each of these memory-related test programs, as well as the program abstract, is given in the following paragraphs. Each program contains instructions for use.

5.5.1 MAINDEC-10-DDQCB

DDQCB is a memory port interaction test that checks for multiport interference problems. The program runs in EXEC mode only. No errors are acceptable.

5.5.2 MAINDEC-10-DDMMD

DDMMD exercises the worst case word patterns throughout all of system memory (up to 256K). No errors are acceptable.

5.5.3 MAINDEC-10-DDMME

DDMME exercises and tests the block transfer instruction, the Address registers, and system memory (up to 256K). No errors are acceptable.

5.5.4 MAINDEC-10-DDMMF

DDMMF exercises memory using floating ones and zeros. In EXEC mode, the program detects both data and parity errors. In USER mode, it detects data errors only. No errors are acceptable.

5.5.5 MAINDEC-10-DDMMG

DDMMG exercises the worst case word patterns through all of system memory (up to 4096K). No errors are acceptable.

NOTE

Programs DCMMA-A-D (basic address test), DCMMB-A-D (basic read/write test), and DCMMD-A-D (memory exerciser) are available on paper tape to provide a back-up diagnostic capability when the programs listed above (Paragraphs 5.5.1–5.5.5) cannot be loaded from disc or magnetic tape.

Loc	SP	PAD	PRC	PRC	ADR	CYT	CYT	CYT	DATA	CYT	CYT	DATA	ADR	AR	DATA	DR	SIN	SIN	SIN	SIN	SIN	SIN	SIN	SIN	STK	STK	DRV	DRV	DRV	DRV	MAT	PS	PS	PS	PS
Possible Circuit Failure / Failure Symptom	ADDRESS PORT BANK/SEL Switch	REQ CYC/Pn RQ	MASTRBW	Pn ACT	ADR ACK/DATA WARNING	M0 3 SEL	CYC ST	DATA IN EN MB SEL	WR RS	WR RS DLY/WREN	DATA OUT EN/STRB	RD RS	ADDRESS RECEIVER	ADDRESS REGISTER	DATA TRANSCEIVER	DATA REGISTER	SENSE STROBE	CLEAR MDR	CLK MDR	INHIBIT TIME	Sense Amplifier/Term	Data Latch	Inhibit Driver	17 mV Threshold	Stack S/I Line	Stack X-Y Line/ Diode	X-Y Volt Reference	Stack Discharge	X Select	Y Select	R/W Timing	-5 V	+5 V	+20 V	DC LO/CROBAR
Memory Does Not Respond	X	X	X			X																											X		X
Incomplete Request				X			X		X	X																									
Non-existent Memory	X	X	X	X	X	X																													
Write Fails								X	X	X									X																
Read Fails											X	X	X	X			X	X																	
All Bits Fail											X	X								X															
Many Bits Fail																	X			X							X	X	X	X	X	X	X	X	
Picks Bits																	LO			X	X	X	X	+5 FA2			HI	X				LO			
Drops Bits																	HI				X						LO	X				HI		LO	
8 Bits Fail																	X	X	X																
4 Bits Fail															X	X																			
2 Bits Fail																						X	X												
1 Bit Fails																					X	X	X		X										
Addressed Port Common	X	X							X			X	X		X																				
*Address Bits 14 17 Common	X																																		
*Address Bits 18 - 19 Common																											X	X			X	X	X	X	
*Address Bit 20 Common		X					X	X		X	X			X		X																			
*Address Bits 21, 23 29 Common																										X			X						
*Address Bits 22, 30 - 35 Common																										X				X					
Read Waveforms Wrong																												X	X	X	X				
Write Waveforms Wrong																				X								X	X	X	X				
No Inhibit															X	X		X		X	X	X	X		X									X	

*Note – Non-Interleaved Operation

Locations:

ADR	– M8591	PAD	– M8592
AR	– M8593YA	PRC	– M8590
CYT	– M8566	PS	– Power Supply
DATA	– M8594	SP	– Switch Panel
DR	– M8593	SIN	– G116
DRV	G236	STK	– H224
MAT	– M8565		

10-2570

Figure 5-2 Troubleshooting Chart

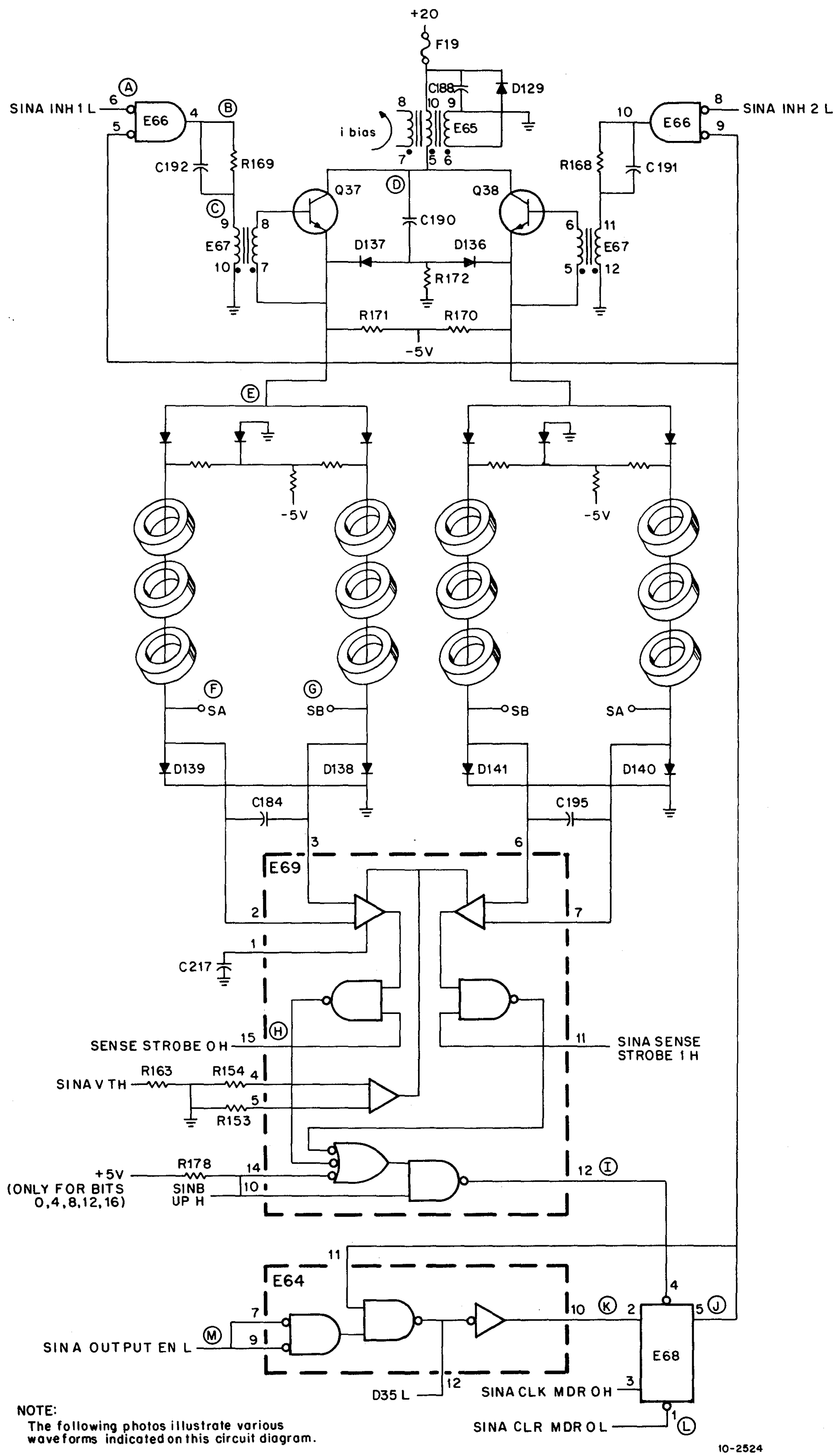
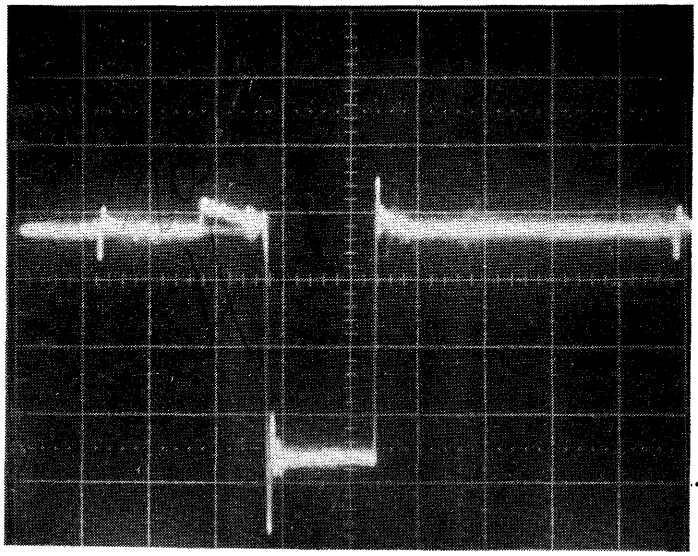


Figure 5-3 Typical Sense/Inhibit Circuit



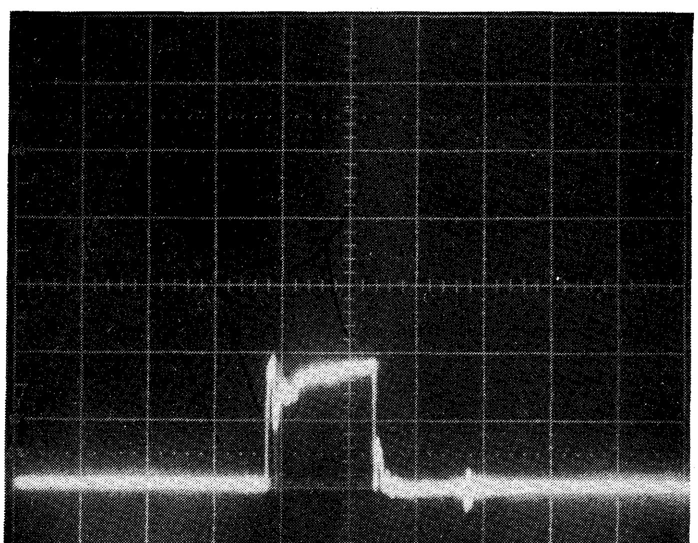
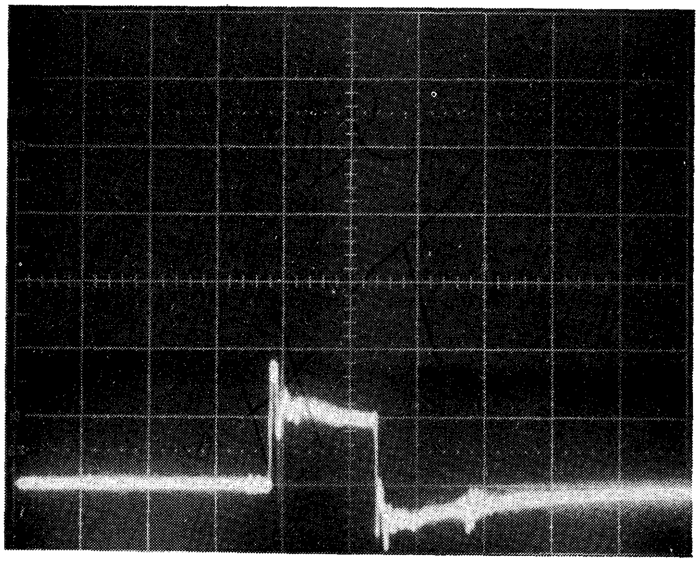


Figure 5-4 Sense Inhibit Module Waveforms (Sheet 1 of 6)

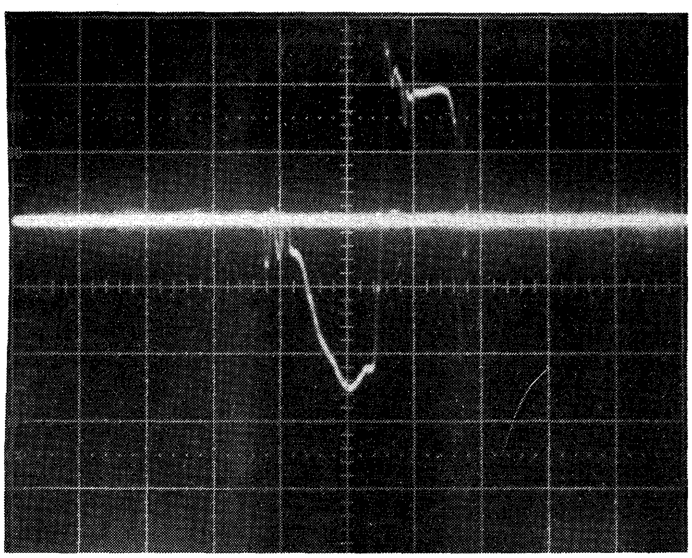


C

1 V/cm
200 ns/cm

GND

M-0563



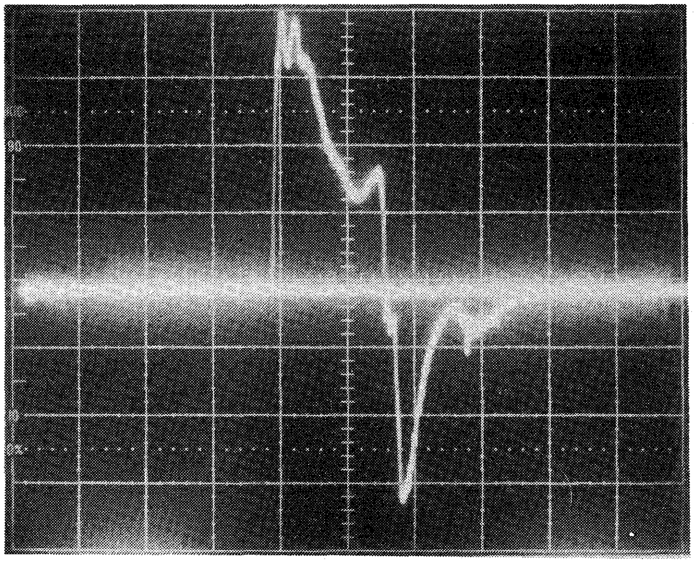
D

5 V/cm
200 ns/cm

GND

M-0564

Figure 5-4 Sense Inhibit Module Waveforms (Sheet 2 of 6)

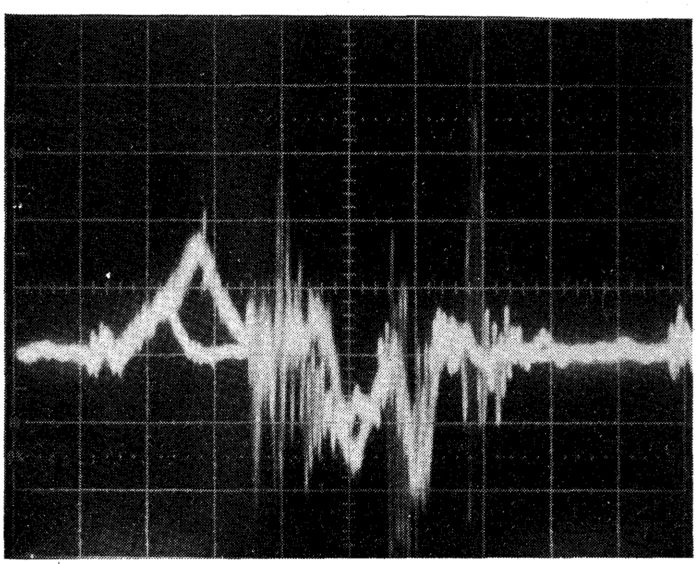


E

10 V/cm
200 ns/cm

GND

M-0565



F,G

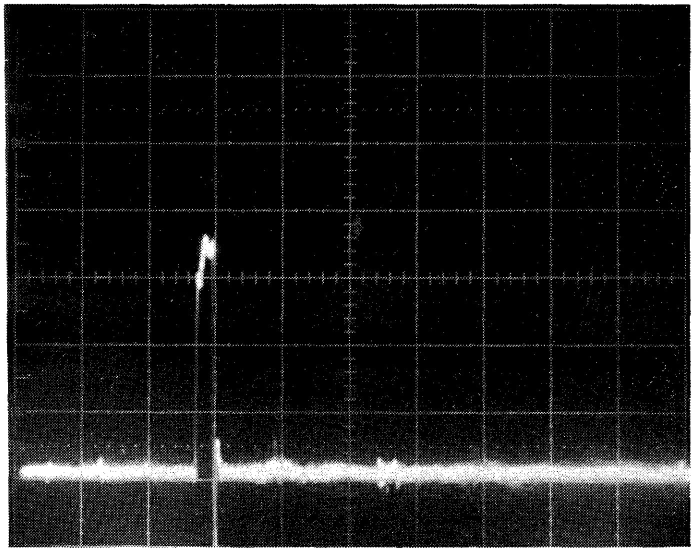
(Potential Difference)

20 mV/cm
200 ns/cm

GND

M-0566

Figure 5-4 Sense Inhibit Module Waveforms (Sheet 3 of 6)



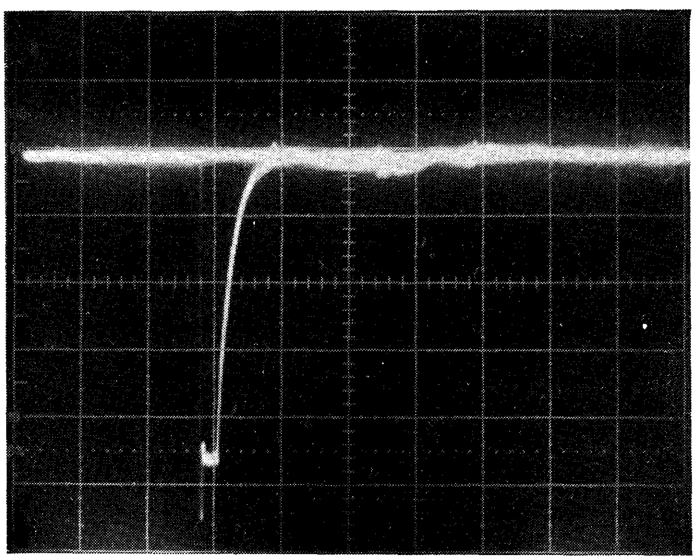
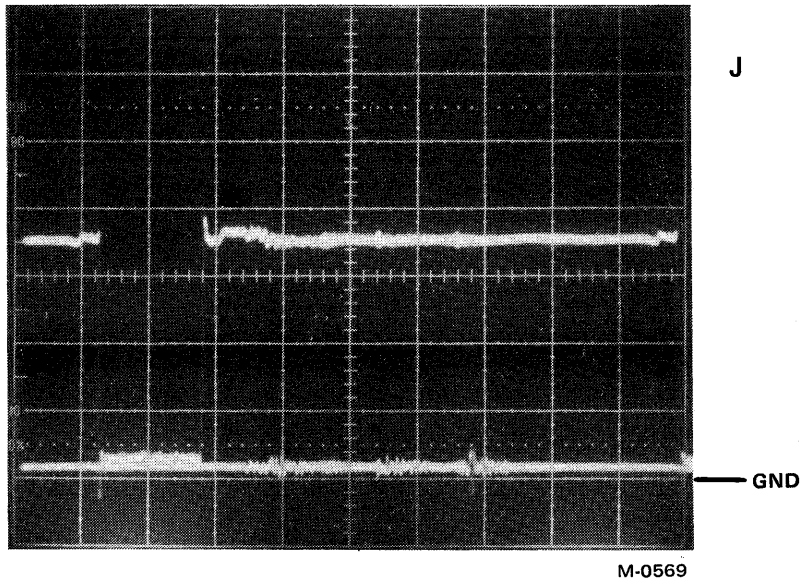


Figure 5-4 Sense Inhibit Module Waveforms (Sheet 4 of 6)



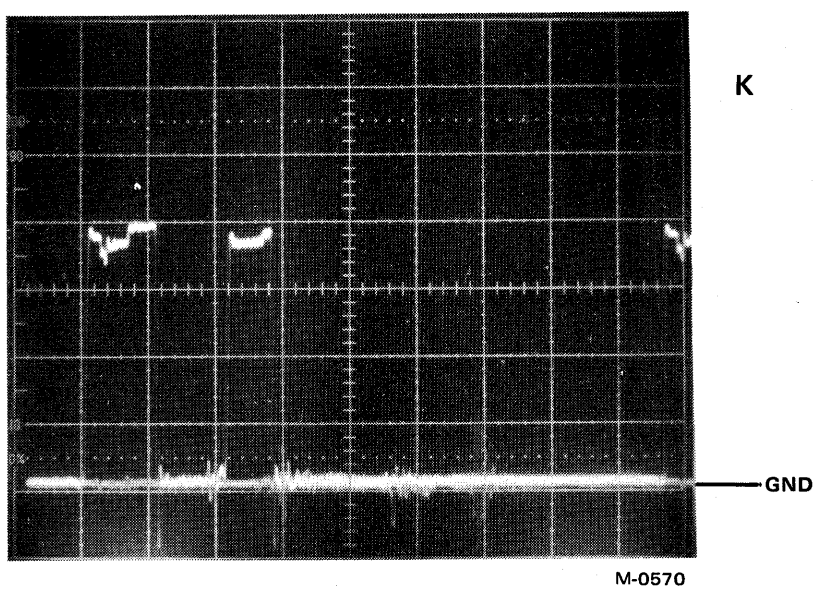
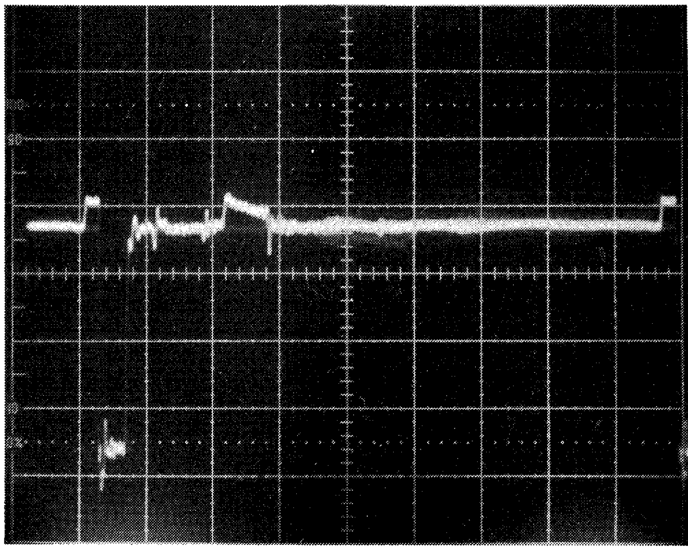
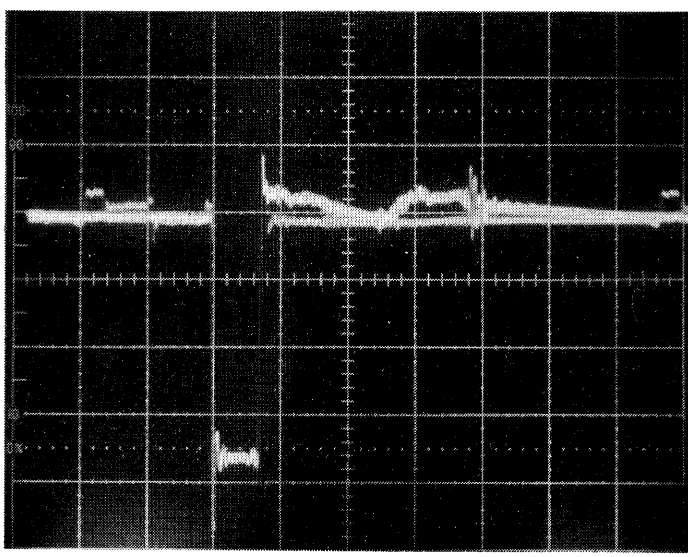


Figure 5-4 Sense Inhibit Module Waveforms (Sheet 5 of 6)



M-0571



M-0572

Figure 5-4 Sense Inhibit Module Waveforms (Sheet 6 of 6)

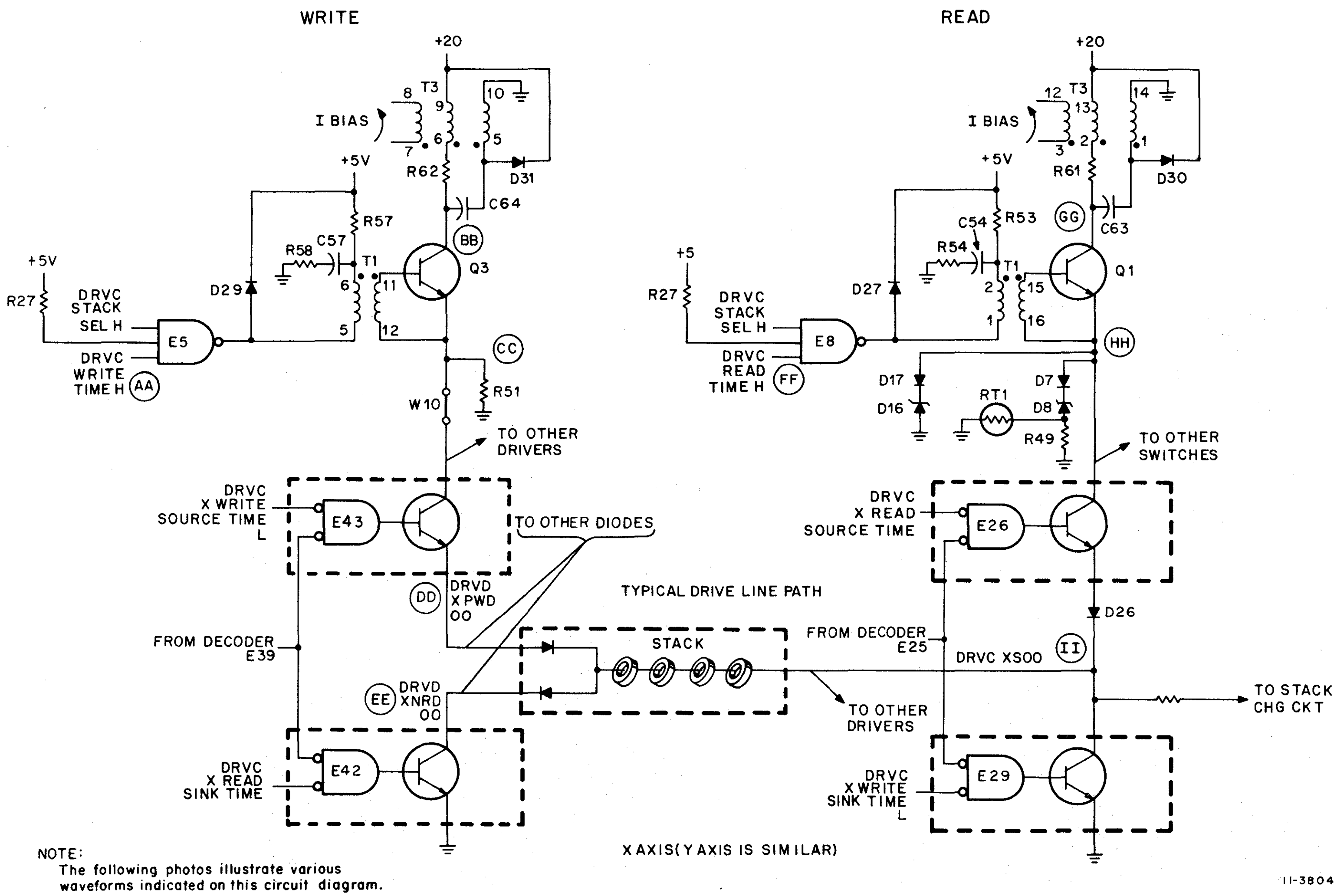
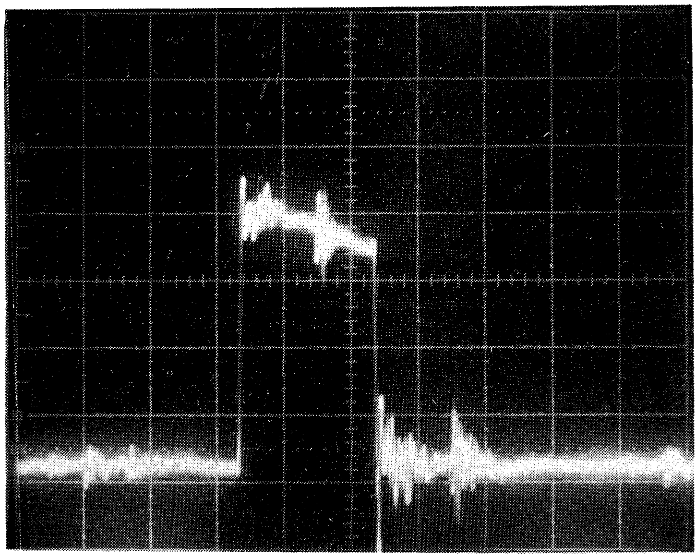


Figure 5-5 Typical Read/Write Drive Circuit



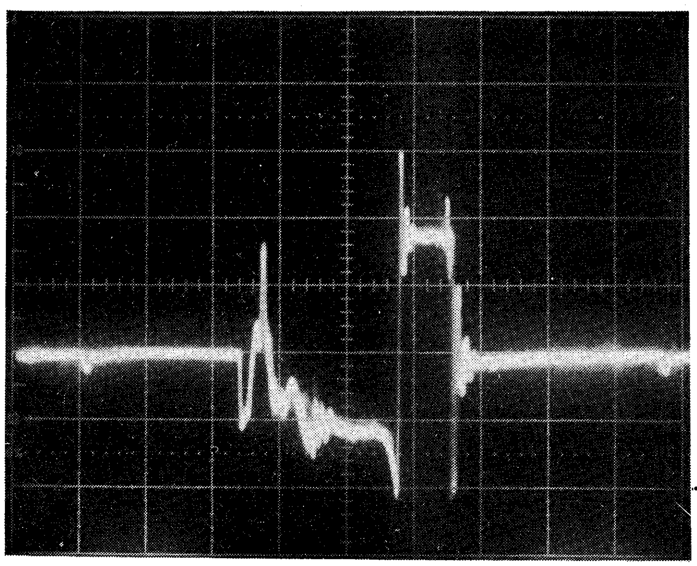
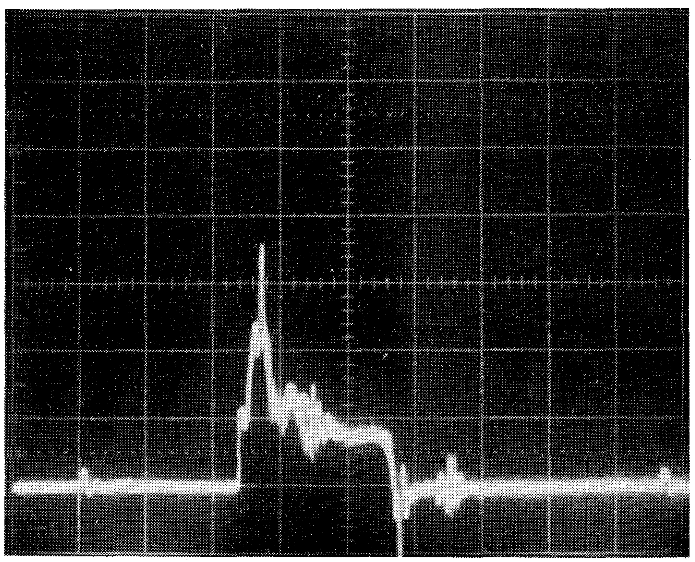


Figure 5-6 Drive Module Waveforms (Sheet 1 of 5)



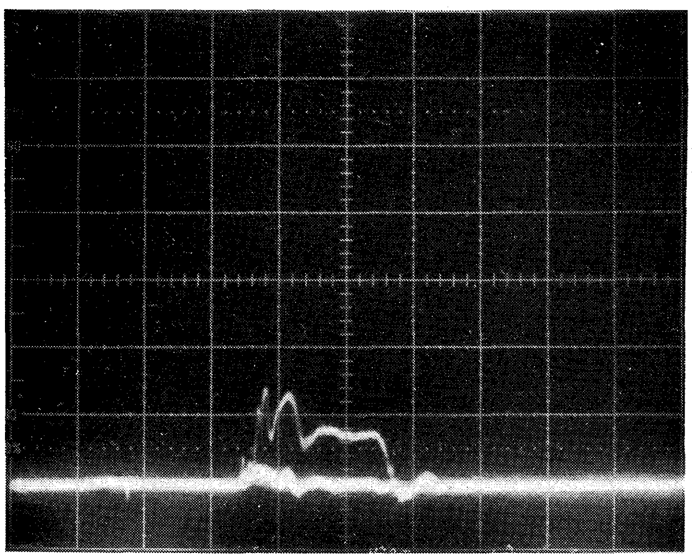
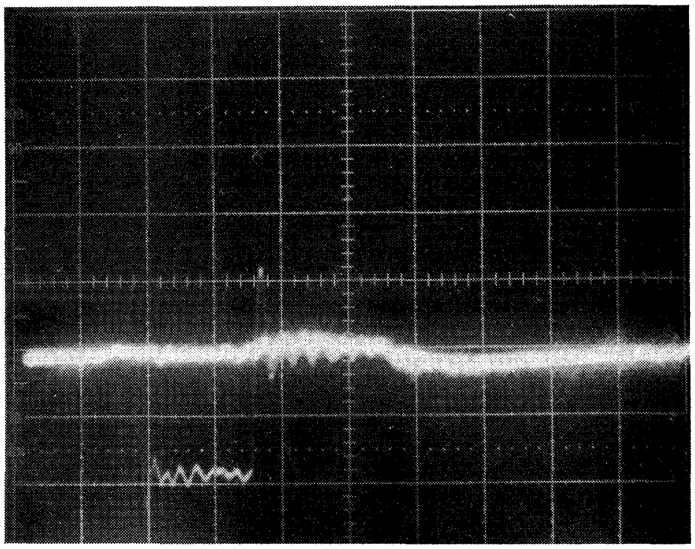


Figure 5-6 Drive Module Waveforms (Sheet 2 of 5)

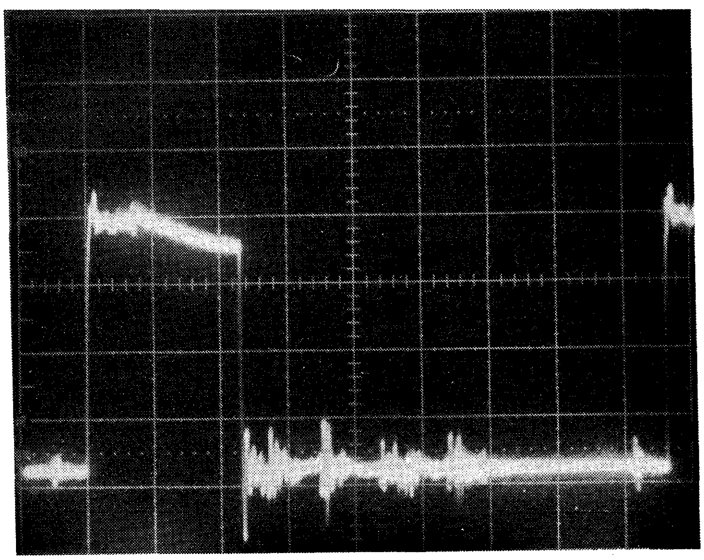


EE

10 V/cm
200 ns/cm

GND

M-0577



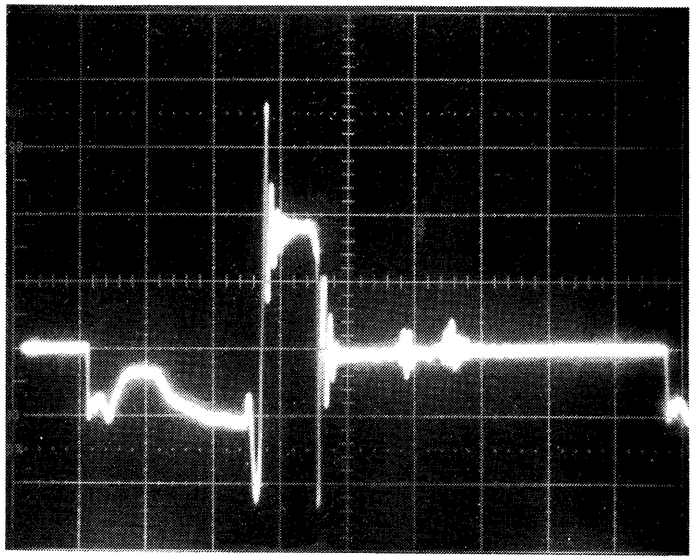
FF

1 V/cm
200 ns/cm

GND

M-0578

Figure 5-6 Drive Module Waveforms (Sheet 3 of 5)



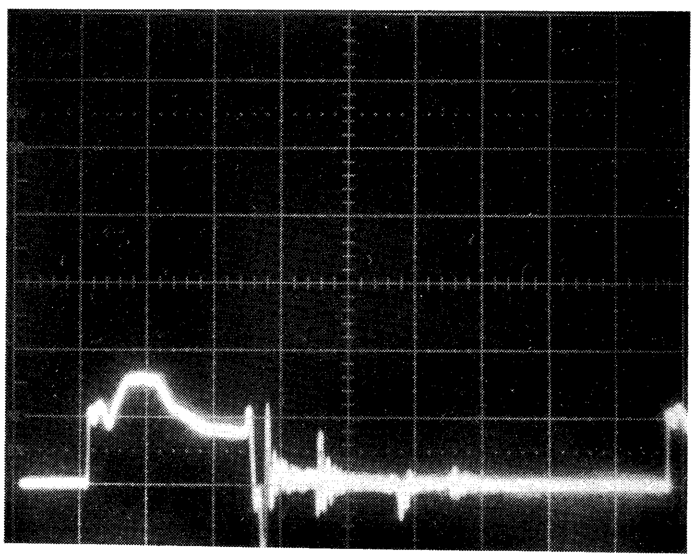


Figure 5-6 Drive Module Waveforms (Sheet 4 of 5)

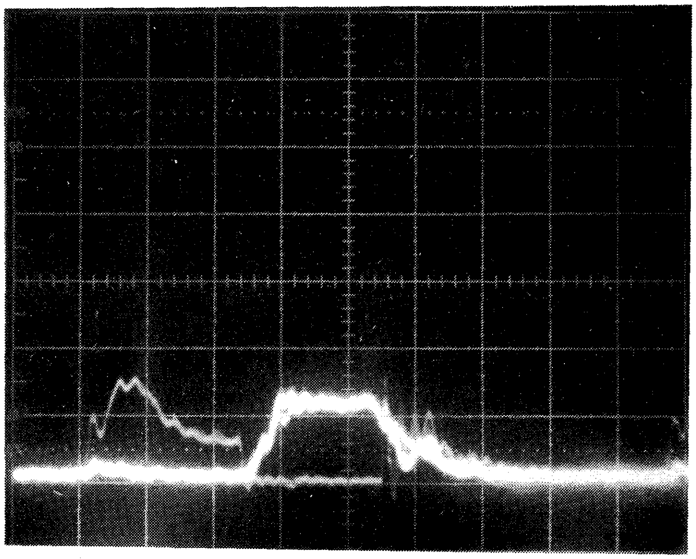


Figure 5-6 Drive Module Waveforms (Sheet 5 of 5)

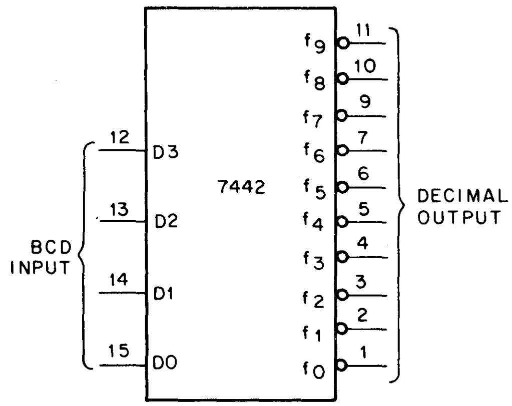
APPENDIX A
IC DESCRIPTIONS

The following ICs are described in this appendix:

7442	4-Line to 1-Line Decoder
7520	Sense Amplifier
74121	Monostable Multivibrator
74154	4-Line to 16-Line Decoder

7442 4 LINE TO 1 LINE DECODER

These BCD-to-decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates.



V_{CC} = PIN 16
GND = PIN 08

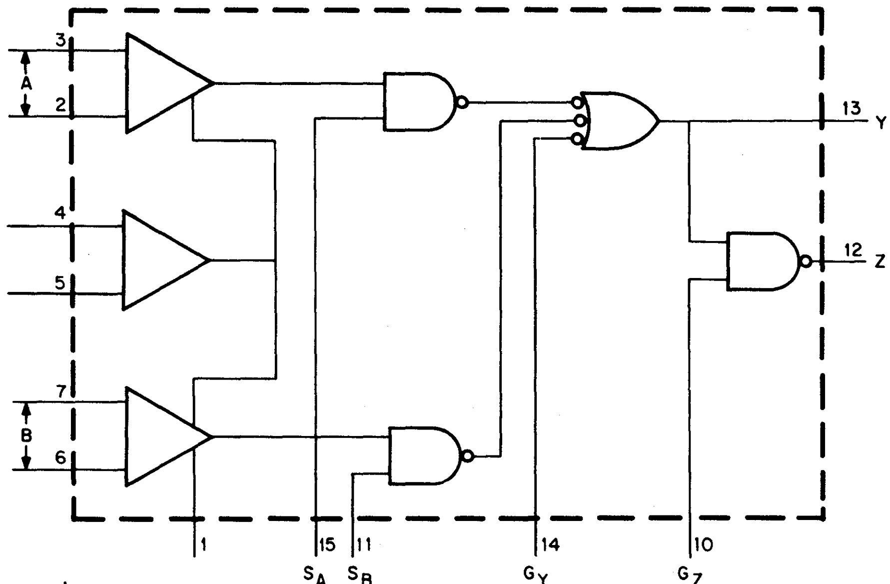
IC-7442

7442
TRUTH TABLE

BCD Input				Decimal Output									
D3	D2	D1	D0	f0	f1	f2	f3	f4	f5	f6	f7	f8	f9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

7520 SENSE AMPLIFIER

The 7520 integrated circuit contains two dc-coupled, single preamplifier sense amplifiers and an OR gate to combine two separate data inputs. The two amplifiers are strobed separately, so only one of the two affects the output in any given cycle.



VCC + = PIN 16
VCC − = PIN 8
GND = PIN 9

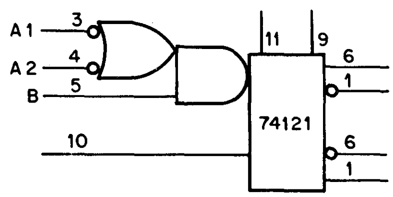
TRUTH TABLE

INPUTS						OUTPUTS	
A	B	G_Y	G_Z	S_A	S_B	Y	Z
X	X	L	X	X	X	H	$\bar{G}_Z$
H	X	X	X	H	X	H	$\bar{G}_Z$
X	H	X	X	X	H	H	$\bar{G}_Z$
L	L	H	X	X	X	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

IC-7520

74121 MONOSTABLE MULTIVIBRATOR

The 74121 Monostable Multivibrator features dc triggering from positive or gated negative-going inputs. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Once fired, the outputs are independent of the input pulses and are dependent only on the timing components on the chip. Input pulses may be of any duration relative to the output pulse.



TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	INHIBIT
0	X	1	0	X	0	INHIBIT
X	1	0	X	0	0	INHIBIT
0	X	0	0	X	1	ONE SHOT
X	0	0	X	0	1	ONE SHOT
1	1	1	X	0	1	ONE SHOT
1	1	1	0	X	1	ONE SHOT
X	0	0	X	1	0	INHIBIT
0	X	0	1	X	0	INHIBIT
X	0	1	1	1	1	INHIBIT
0	X	1	1	1	1	INHIBIT
1	1	0	X	0	0	INHIBIT
1	1	0	0	X	0	INHIBIT

$1 = V_{in(1)} \geq 2$ V

$0 = V_{in(0)} \leq 0.8$ V

Note:

1. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.

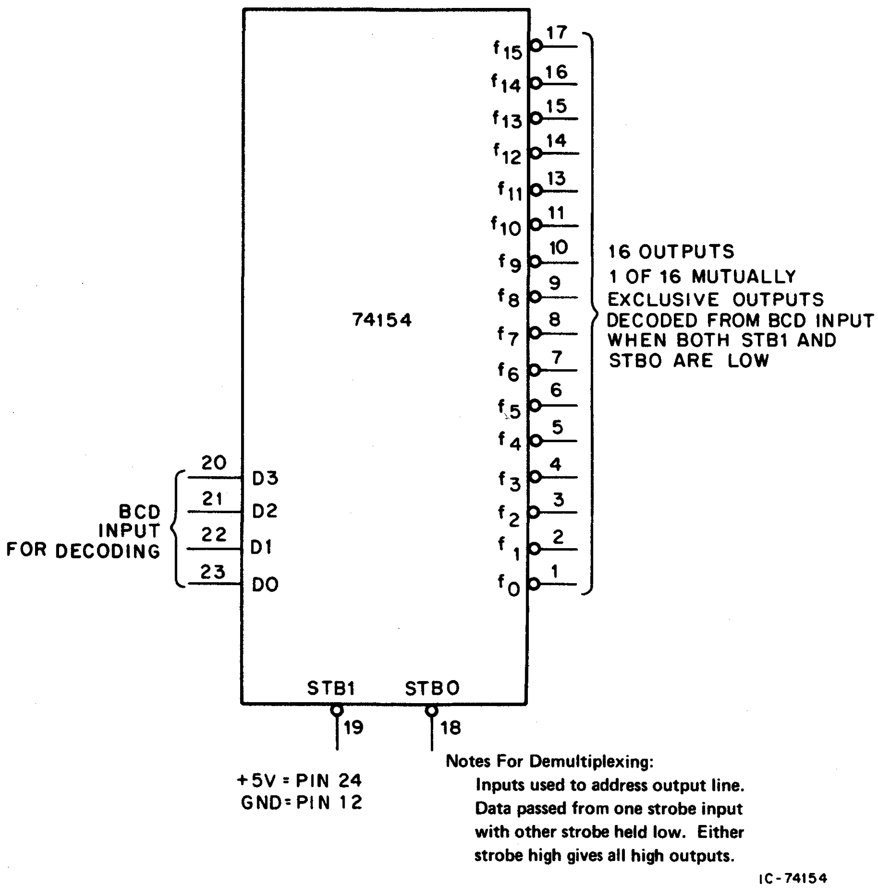
2. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table.)

3. Pins 9, 10, and 11 are inputs to control pulse width of output.

IC-74121

74154 4-LINE TO 16-LINE DECODER

The 74154 4-Line to 16-Line Decoder decodes four binary-coded inputs into one of 16 mutually-exclusive outputs when both strobe inputs (G1 and G2) are low. The decoding function is performed by using the four input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.



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What features are most useful? ____________________

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Does this manual satisfy the need you think it was intended to satisfy? ____________________

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Do Not Tear - Fold Here and Staple

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