Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-10
Maintenance Manual

DS10 SINGLE SYNCHRONOUS LINE UNIT

DEC-10-HDSA-D

pdp10

DS10 SINGLE SYNCHRONOUS LINE UNIT MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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Foreword

The *DS10 Single Synchronous Line Unit Maintenance Manual* comprises the following:

Chapter 1 – presents the purpose and general description of the DS10; its data format and specifications

Chapter 2 – presents the installation and interface requirements

Chapter 3 – describes the DS10 indicator panel and applicable PDP-10 I/O instructions

Chapter 4 – describes the control, receive, and transmit logic in a typical sequence of operation

Chapter 5 – presents preventive maintenance and troubleshooting procedures for the DS10

Chapter 6 – contains a complete set of DS10 engineering drawings for reference purposes by maintenance personnel

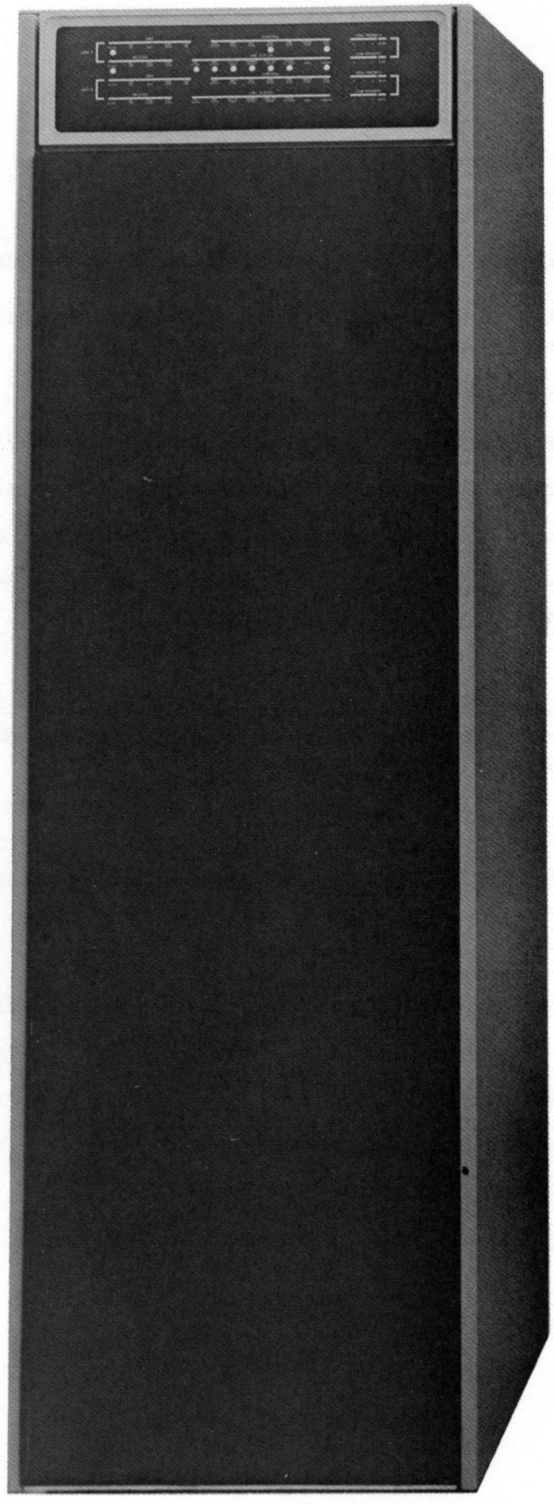
NOTE

A prior knowledge of both the PDP-10 Central Processor and communication modems is essential to the understanding of this manual.

REFERENCE DOCUMENTS

For further information relevant to the DS10, consult the following related publications:

Title	Number
PDP-10 System Reference Manual	DEC-10-HGAC-D
PDP-10 Interface Manual	DEC-10-HIFB-D
PDP-10 Site Preparation Guide	DEC-10-HAAB-D
KA-10 Central Processor Maintenance Manual	DEC-10-HMAB-D
Electronic Industries Association (EIA) Standard RS-232-C	
Bell System Technical Reference Manual for Type 210A and 210B Data Sets	



Chapter 1
Introduction

1.1 SCOPE

This manual contains general information; installation, operating, programming, technical reference, and maintenance data for the DS10 Single Synchronous Line Unit.

1.2 GENERAL DESCRIPTION

The DS10 (see Figure 1-1) is an interface between a PDP-10 I/O Bus and one full-duplex or half-duplex serial-synchronous modem communication link having characteristics compatible with Electronics Industries Association (EIA) Standard RS-232-B (or C). The concept of this interface is to take parallel information from the PDP-10 CP and transmit it in bit-synchronous serial form to the modem, or to take a serial bit stream from the modem and deliver it in parallel to the PDP-10. These two operations can occur either separately or simultaneously, depending upon whether the mode of operation is half-duplex or full-duplex.

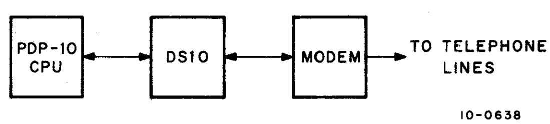


Figure 1-1 DS10 Configuration

The DS10 is capable of controlling most of the common leads associated with an RS-232-B(C)-type modem. In addition, the DS10 can answer and terminate incoming calls. Up to two DS10 units can be used with each PDP-10 CP. The second DS10 is housed in the same cabinet with the first DS10. The DS10 can be operated at either 50 Hz or 60 Hz; four configurations are available:

DS10-A	A single DS10 unit for 60 Hz operation
DS10-B	A single DS10 unit for 50 Hz operation
DS10-C	A second DS10 unit for 60 Hz operation
DS10-D	A second DS10 unit for 50 Hz operation

1.3 FUNCTIONAL DESCRIPTION

The DS10 (see Figure 1-2) consists of a transmit channel and a receive channel controlled by programmed instructions from the PDP-10 CP, and synchronized by timing pulses from the associated modem.

In the transmit mode a full word, containing either four or six characters, is transferred in parallel from the PDP-10 to a buffer register. One character at a time is then transferred to the shift register, which shifts data serially to the data set terminal. When a word is shifted out, the PDP-10 transfers another word to the buffer register and transmission continues in the same manner as above. Facilities for detecting a sync character, determining the character length, maintaining a character count, etc., are provided by the control section.

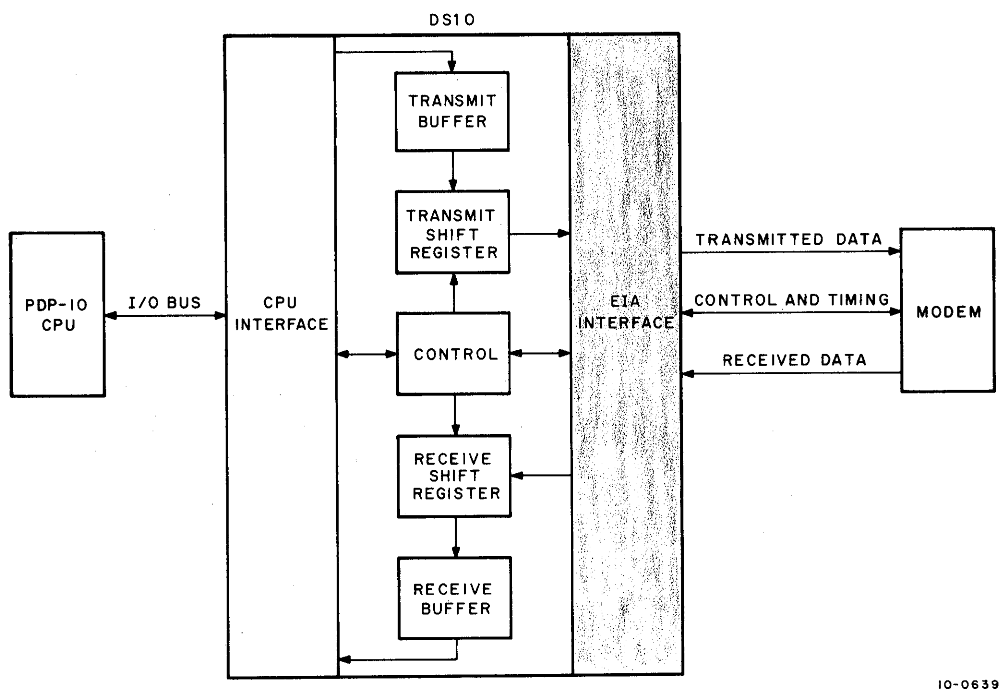


Figure 1-2 Simplified Block Diagram

An additional feature of the transmit mode is the ability to idle after a message has been transmitted instead of turning off the connections to the modem. The idle mode effectively keeps the line open between messages, thus eliminating the need to re-establish contact with the modem.

In the receive mode, input characters from the data set are shifted serially into a register, then transferred to a buffer register. When the buffer is full (with either four or six characters), a priority interrupt is generated and the contents of the buffer are sent to the PDP-10 via the I/O Bus lines. The control section provides for sync character detection, character counting, end-of-transmission detection, and other associated circuitry.

1.4 DATA FORMAT

Serial data is transmitted and received continuously once synchronization is achieved. The transmission format consists of sync characters (one is sufficient) followed by the characters that make up the text of the message. Character lengths may be either 6 or 8 bits; this is a programmable function of the hardware. Because a PDP-10 word contains 36 bits, there are either six 6-bit characters or four 8-bit characters per word (see Figure 1-3).

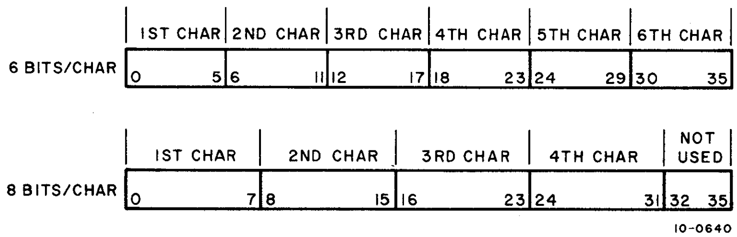


Figure 1-3 Characters Per Word

Sync characters provide a time reference at the start of every message. Once a sync character is detected, the receiving terminal assembles every 6 or 8 bits in a buffer. Sync characters are selected by the user through use of a jumper board. A brief message using 6-bit characters with a sync code of 26_8 is illustrated in Figure 1-4. (The least significant bit is sent first.)

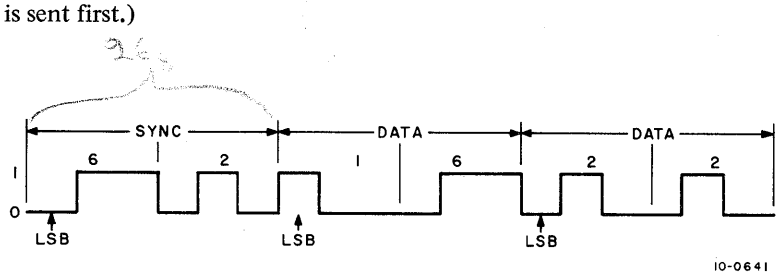


Figure 1-4 DS10 Serial Message Format for 6-Bit Characters

1.5 SPECIFICATIONS

Type of Channel	Serial-synchronous, half- or full-duplex
Speed	20,000 bps maximum
Interface	Conforms to EIA Standard RS-232-C
Data Format	6- or 8-bit characters; unique sync character code for each character length
Compatible Data Sets	**Type** / **Speed (Baud)** Bell 201A — 2000 Bell 201B — 2400 Bell 205 — 600, 1200, 2400 Any other modem that meets EIA Standard RS-232-B(C) Specifications
Operating Environment	Limited only by PDP-10 operating conditions
60 Hz ac Power	115V +10%, 60 Hz +2%
50 Hz ac Power	230V +10%, 50 Hz +2%
Power/Heat Dissipation	450W

1.5 SPECIFICATIONS (Cont)

Height	69 in.
Width	22 in.
Depth	29 in.
Weight	300 lb

Chapter 2
Installation and Interface

This chapter contains general information on installation and interface requirements for the DS10. Included also is a description of the applicable Electronic Industries Association (EIA) circuits utilized by the DS10.

2.1 MOUNTING

The DS10 is contained in three DEC1943 Flip-Chip mounting panels which are housed in a standard DEC 19-in. cabinet. Also included in the cabinet are an 844 power control unit and two 728 power supplies. This equipment is shown in Figures 2-1 and 2-2. If a second DS10 unit is employed, it is housed in the same cabinet with the first DS10 and shares the same power supplies and indicator panel.

The modem and its associated power supplies mount in an external cabinet or rack.

2.2 CABLING

2.2.1 PDP-10 to DS10

The PDP-10 I/O Bus is the only connection between the PDP-10 CP and the DS10. The physical configuration of the I/O Bus is comprised of two coaxial cable sets which terminate in two W851 Flip-Chip Connector Assemblies. The length of the cables is dependent on the proximity of the cabinetry and the configuration of the system (maximum I/O cable length is 50 ft). See DEC drawing DS10-0-IO for I/O cable pin assignments.

2.2.2 DS10 to Modem

A 25-ft cable is provided for connection between the DS10 and the modem. The socket on the modem is a 25-pin receptacle (Cannon DB-19604-433 or equivalent). The plug on the modem end of the cable is a Cannon DB-19604-432 or equivalent. The other end of the cable, which connects to the DS10, is equipped with an M957 Cable Connector. The entire cable assembly is designated BC01R-25. Other cables may be used, but must comply with the specifications in EIA Standard RS-232-B(C).

2.2.3 DS10 Logic to Indicator Panel

Ribbon cables are provided for connection between the DS10 logic and the indicator panel (Figure 2-2, Rear View). If a second DS10 unit is used, additional ribbon cables are provided that connect to the bottom two rows of connectors on the indicator panel.

2.3 INTERFACE CIRCUITS

This section contains material from the Electronic Industries Association Standard RS-232-C concerning communications interface circuits. The standard defines a means of exchanging control signals and binary serialized data

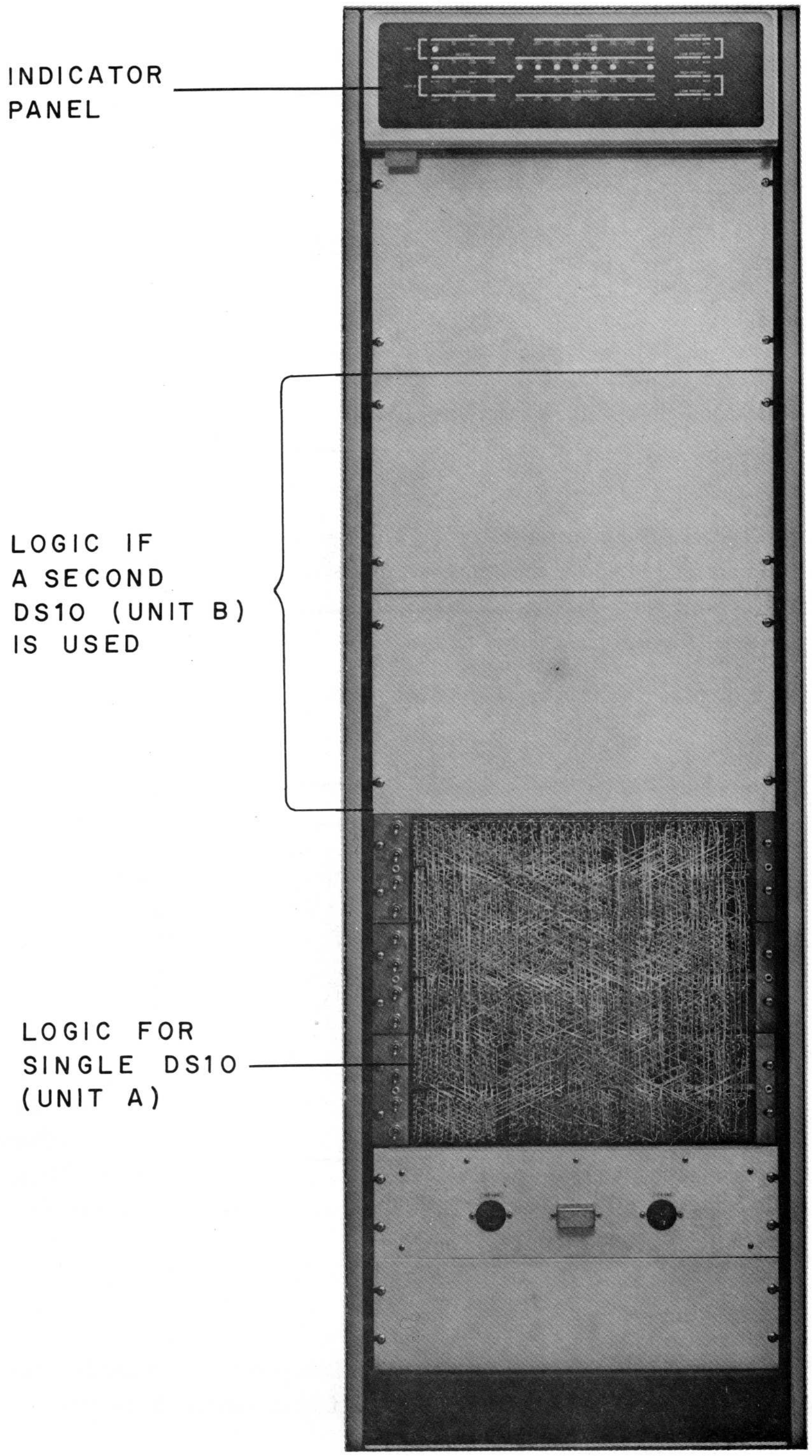


Figure 2-1 DS10 Cabinet, Front View

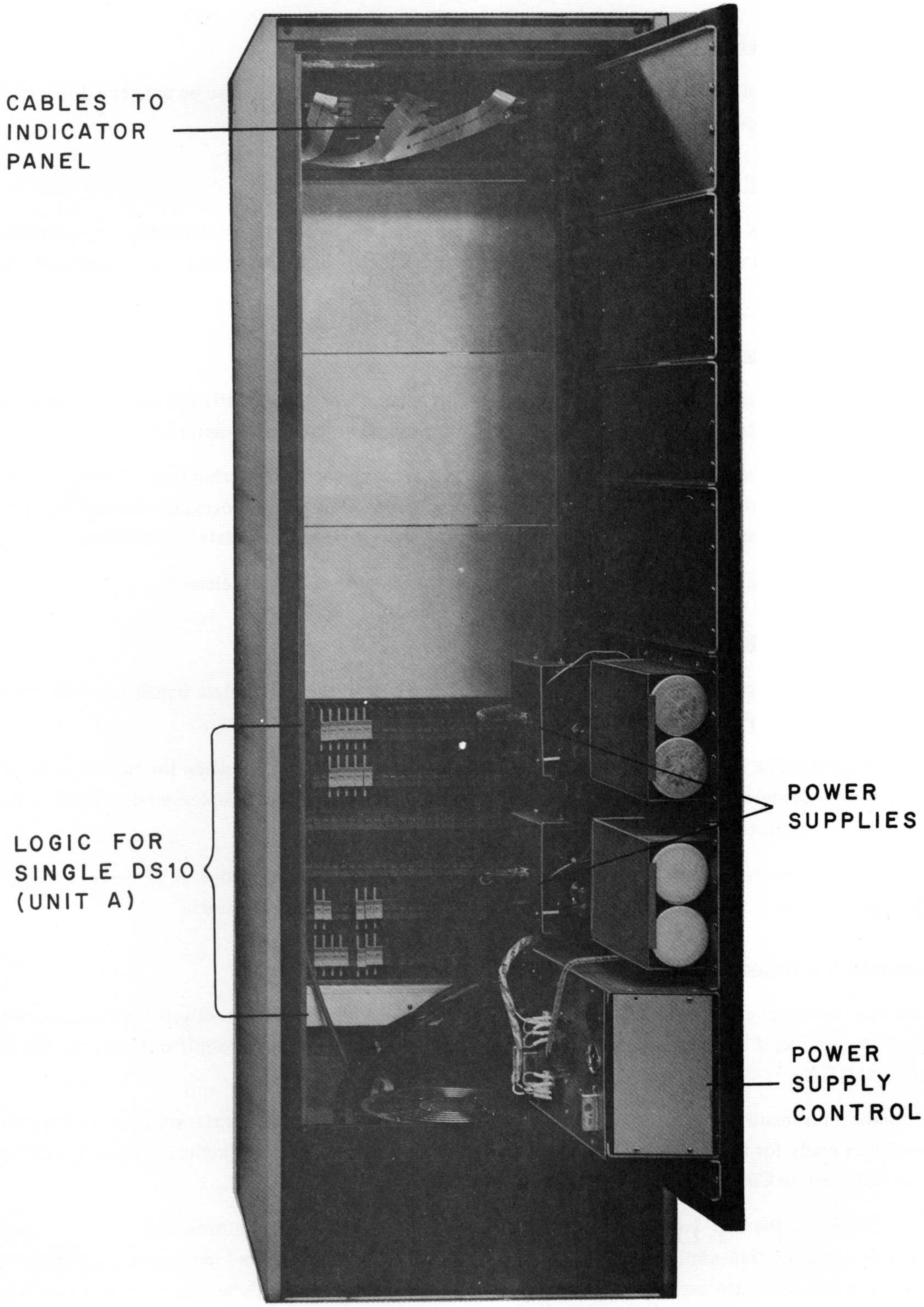


Figure 2-2 DS10 Cabinet, Rear View

signals between data processing terminal equipment and data communication equipment. Drawing DS10-0-RS in Chapter 6 shows the cable and pin assignments for the RS-232-C interface.

2.3.1 Circuit AA – Protective Ground

This conductor is electrically bonded to the machine or equipment frame. It may also be connected to external grounds as required by applicable regulations.

2.3.2 Circuit AB – Signal Ground

This conductor establishes the common ground reference potential for all interchange circuits except circuit AA. In the data set, circuit AB is brought to one point; this point can be connected to circuit AA by means of a wire strap.

2.3.3 Circuit BA – Transmitted Data

Signals on this circuit are generated by the data processing terminal equipment (DS10) and are transferred to the transmitting signal converter for transmission to remote data processing terminal equipment.

The data processing terminal equipment holds Circuit BA in a marking condition during time intervals between characters or words, and at all times when no signals are being transmitted. Data processing terminal equipment designed for receive-only service holds this circuit in marking condition (i.e., the 1 state) at all times.

The marking or spacing signal condition is held for the total duration of each signal element.

2.3.4 Circuit BB – Received Data

Signals on this circuit are generated by the receiving signal converter in response to data signals received from remote data processing terminal equipment.

In half-duplex service, the receiving data set holds marking condition on Circuit BB when the remote data processing terminal equipment has its Circuit CA in the OFF condition. While in half-duplex service, the Received Data circuit may be used to monitor transmitted signals.

A data set equipped for transmit-only service holds Circuit BB in the marking condition at all times, and the marking or spacing signal condition is held for the total duration of each signal element.

2.3.5 Circuit CA – Request-to-Send

Signals on this circuit are generated by the data processing terminal equipment to condition the local data set to transmit. For example, if the data set contains a modulator, the carrier signal is transmitted during the ON condition of Circuit CA.

The ON condition is maintained whenever the data processing terminal equipment is transmitting information or has information ready for transmission. The signal converter transmits all data on Circuit BA while the ON condition is maintained on Circuit CA, Circuit CB, and Circuit CC.

In half-duplex service, the OFF condition holds the data set in the receive-data condition, and the ON condition holds the data set in the transmit-data condition. The above condition is established independent of signals on Circuits BA and BB. Data processing terminal equipment designed for receive-only service holds Circuit CA in the OFF condition at all times.

Data processing terminal equipment designed for either transmit-only or full-duplex service may hold Circuit CA in the ON condition at all times. Similarly, data communication equipment used for transmit-only or full-duplex service may be placed in the transmit condition at all times, regardless of the signal condition on Circuit CA.

2.3.6 Circuit CB – Clear-to-Send

Signals on the circuit are generated by the data communication equipment to indicate that the data set is prepared to transmit data. The ON condition is a response to the ON condition on Circuit CA and indicates to the data terminal equipment that signals presented on Circuit BA (Transmitted Data) will be transmitted to the communication channel. When Circuit CA is turned OFF, Circuit CB is also turned OFF.

In receive-only service, the data set holds Circuit CB OFF at all times.

In transmit-only or full-duplex service, when the data communication equipment is in transmit condition at all times, Circuit CB is held in the ON condition at all times.

2.3.7 Circuit CC – Data Set Ready

Signals on this circuit are generated by the local data set to indicate that it is ready to operate.

The OFF condition is used to indicate:

a. An abnormal or test condition which disables or impairs a normal function associated with the service calls

b. That the communication channel is switched to an alternate means of communication (e.g., alternate voice telephone)

c. That the local data set is not connected to a communication channel.

The ON condition appears at all other times.

Circuit CC is used only to indicate the status of the local data set. The ON condition indicates neither that a communication channel has been established to a remote station, nor the status of any remote station or equipment.

2.3.8 Circuit CD – Data Terminal Ready

Signals on this circuit are used to control switching of the signal converter to the communication channel. The ON condition causes the signal converter to be connected to the communication channel. However, if the station is equipped only for call origination by means external to this interface (e.g., manually or an automatic call origination unit), the ON condition serves only to maintain the connection established by these external means. When the station is equipped for automatic answering of received calls, connection to the line may be arranged to occur only in response to a ringing signal. The OFF condition removes the signal converter from the communication channel, for such reasons as:

a. Freeing the line for alternate use (e.g., voice or use by other terminal stations)

b. Permitting use of the data processing terminal equipment for an alternate function (e.g., off-line operation)

c. Terminating a call

The OFF condition does not disable the operation of Circuit CE.

2.3.9 Circuit CE – Ring Indicator

Signals on this circuit indicate that a ringing signal is being received from a remote station; this circuit may be required for automatic answering of received calls.

The ON condition indicates that a ringing signal is being received; the OFF condition is maintained at all other times. Operation of this circuit is not disabled by the OFF condition on Circuit CD.

2.3.10 Circuit CF – Data Carrier Detector

Signals on this circuit provide an indication that the data carrier is being received. When the data carrier is lost because the transmitting signal converter is turned OFF due to a fault condition, the OFF condition follows after an appropriate guard time delay.

In half-duplex service, where the signal converter is arranged for local copy, Circuit CF may respond to carrier signals from either the local or remote transmitting signal converter.

The ON condition indicates reception of the data carrier. The OFF condition provides an indication of the end of present transmission activity or a fault condition.

2.3.11 Circuit DA – Transmitter Signal Element Timing

Signals on this circuit provide the transmitting signal converter with signal element timing information.

The waveform is normally ON and OFF for equal periods of time, and a transition from ON to OFF normally indicates the center of each signal element on Circuit BA. (This is LOCAL TIMING.)

2.3.12 Circuit DB – Transmitter Signal Element Timing

Signals on this circuit provide the data processing terminal with signal element timing information.

The waveform is normally ON and OFF for equal periods of time. The data processing terminal equipment provides a data signal on Circuit BA. The transitions of this data signal nominally occur at the time of the transitions from OFF to ON condition of the signal on Circuit DB. (This is SERIAL CLOCK TRANSMIT.)

2.3.13 Circuit DD – Receiver Signal Element Timing

Signals on this circuit provide the data processing terminal equipment with signal element timing information.

The waveform is normally ON and OFF for equal periods of time, and the transition from ON to OFF condition nominally indicates the center of each signal element on Circuit BB. (This is SERIAL CLOCK RECEIVE.)

The electrical characteristics of these interchange signals are as follows:

a. The maximum open-circuit voltage to Circuit AA or Circuit AB on any interchange circuit does not exceed 25V, and the maximum short-circuit current flow between any two conductors (including grounds) does not exceed 0.5A.

b. Any circuitry used to generate a signal voltage on an interchange circuit is protected from damage by either an open circuit condition or a short circuit in either Circuit AA or AB. Any circuitry used to receive signals from an interchange circuit is designed for continuous operation with any input signal within the maximum voltage limits specified.

c. For Circuits BA and BB, the signal is considered in the marking condition when the voltage on the circuit is more negative than -3V with respect to signal ground, and the signal is considered in the spacing condition when the voltage is more positive than 3V with respect to signal ground. During transmission of data, the marking condition is used to denote the binary state ONE, and the spacing condition is used to denote the binary state ZERO. Note that marking is the normal condition on a data circuit when no signals are present.

2.3.14 Summary of Data Circuits

Binary State	ONE	ZERO
Signal Condition	Marking	Spacing
Voltage	Negative	Positive
Paper Tape	Hole	No Hole

For all control circuits included in this discussion, the control function is considered ON when the voltage on the circuit is more positive than +3V with respect to signal ground, and is considered OFF when the voltage on the circuit is more negative than 3V with respect to signal ground.

2.3.15 Summary of Control Circuits

Control Function	OFF	ON
Voltage	Negative	Positive

NOTE

The condition in which the voltage of a data circuit or a control circuit is between ±3V is not mentioned in this discussion. This area is undefined by RS-232-C; therefore, this region or its effect on DEC logic is not defined.

26 is sync character
4_8 is End of message
DS10 TO MODEM is EIA MODE

Chapter 3
Operation and Programming

This chapter provides information on the DS10 indicator panel and a description of the PDP-10 I/O instructions as they apply to the DS10.

3.1 OPERATION

The DS10 has no operating controls; operation is under automatic control of the PDP-10 program and timing signals from the data set. The indicator panel at the top of the DS10 cabinet allows the operator to monitor the status of various conditions in the system. Figure 3-1 shows the indicator panel, and Table 3-1 defines the functions of each indicator.

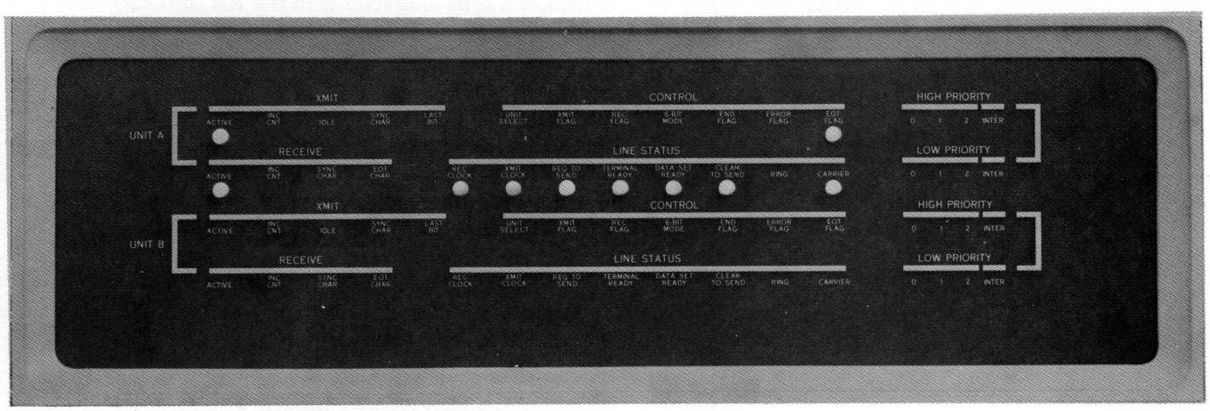


Figure 3-1 DS10 Indicator Panel

The indicator panel consists of two identical sets of indicator lamps. When a single DS10 is mounted in the cabinet, only the top two rows, designated UNIT A, are used. When a second DS10 is installed in the system, the top two rows indicate the status of one unit (UNIT A) and the bottom two rows indicate the status of the second unit (UNIT B).

Table 3-1
Indicator Panel Description

Group	Indicator	Function
XMIT	ACTIVE	Indicates the DS10 is currently in the transmit mode.
	INC CNT	Indicates the transmit character counter is being incremented.
	IDLE - KEEPS MODEM ON LINE	Indicates that IDLE flip-flop is set. Idle mode allows the DS10 to maintain contact with a modem after the last character of a message is transmitted.
	SYNC CHAR	Indicates the first character in the transmit word is a sync character.
	LAST BIT	Indicates that one more bit of a character is to be transmitted to the modem.
RECEIVE	ACTIVE	Indicates the DS10 is currently in the receive mode.
	INC CNT	Indicates the receive character counter is being incremented.
	SYNC CHAR	Indicates a sync character is in the RB shift register.
	EOT CHAR	Indicates an end-of-transmission character is in the RB shift register, which eventually causes the receive logic to be disabled.
CONTROL	UNIT SELECT	Indicates the DS10 has been selected by the PDP-10 CP through a 460_8 or 464_8 I/O instruction.
	XMIT FLAG	Indicates that the Transmit Flag flip-flop is set. The XMIT FLAG is set when there is only one character in each word left to be transmitted. This causes a high priority interrupt to be generated.
	REC FLAG	Indicates that the Receive Flag flip-flop is set. The REC FLAG is set when a full word has been received by the DS10. This causes a high priority interrupt to be generated.
	6-BIT MODE	Indicates the message format consists of six bits per character. When the indicator is not lit, the format is eight bits per character.
	END FLAG	Indicates END FLAG flip-flop is set. The END FLAG is set either when the clock pulses from the data set have stopped before an EOT character is received, or on the transition from on to off of the signal carrier.

Table 3-1 (Cont)
Indicator Panel Description

Group	Indicator	Function
CONTROL (Cont)	ERROR FLAG	Indicates the PDP-10 CP failed to respond to the interrupt generated by Receive Flag (1).
	EOT FLAG	Indicates that the EOT FLAG is set, which means an EOT character has been received.
LINE STATUS (EIA Interface)	REC CLOCK	Indicates that the Receive Clock pulses, supplied by the data set, are active.
	XMIT CLOCK	Indicates that the Transmit Clock pulses, supplied by the data set, are active.
	REQ TO SEND	Indicates the Request-to-Send lead on the EIA Interface is active.
	TERMINAL READY	Indicates the DS10 is ready to begin operation.
	DATA SET READY	Indicates the modem is ready for operation.
	CLEAR TO SEND	Indicates the DS10 can start sending messages.
	RING	Indicates a ringing signal is being received from a data set.
	CARRIER	Indicates information is being received at the local modem.
HIGH PRIORITY	0, 1, 2	Indicates the octal program-interrupt channel number.
	INTER	Indicates that the Interrupt flip-flop is set.
LOW PRIORITY	0, 1, 2 END FLG ERROR FLG RING	Indicates the octal program-interrupt channel number.
	INTER	Indicates that the Interrupt flip-flop is set.

3.2 PROGRAMMING

The DS10 is designed to respond to the standard PDP-10 input/output instructions in the same manner as any other peripheral unit: the DS10 shares the I/O Bus along with other peripherals, and must be selected by a unique device code. The I/O Bus consists of 36 two-way lines that serve to carry data and control information between the DS10 and a PDP-10 CP.

Two device codes (460 and 464) are used to select and condition a DS10 to accept the following four instructions from the PDP-10 CP. (A second set of device codes, 470 and 474, are used when a second DS10 unit is utilized.)

a. CONO (Conditions Out) – accept control information from the CP

b. CONI (Conditions In) – send status information to the CP

c. DATAO (Data Out) – accept data from the CP

d. DATAI (Data In) – send data to the CP

Table 3-2 lists the CONO and CONI instructions for both device select codes and the function of each bit in the instruction. Following the table are detailed descriptions of each bit assignment.

Table 3-2
Bit Assignments

Bit	CONI 460 (470)	CONO 460 (470)	CONI 464 (474)	CONO 464 (474)
18	Character Length	Character Length		
19	Diagnostic	Diagnostic		
20	Idle Enabled	Idle Enabled		
21	Idle			
22	Transmit-Active			
23	Receive-Active	Receive-Active		
24	Receive-Inhibit	Receive-Inhibit		
25	Clear-to-Send			
26	Data Terminal Ready	Data Terminal Ready		
27	Ring Enabled	Ring Enabled		
28	Data Set Ready			
29				
30	Ring Flag*	Ring Flag	Low Priority 2	Low Priority 2
31	End Flag*	End Flag	Low Priority 1	Low Priority 1
32	Error Flag*	Error Flag	Low Priority 0	Low Priority 0
33	Transmit Flag**		High Priority 2	High Priority 2
34	EOT Flag	EOT Flag	High Priority 1	High Priority 1
35	Receive Flag**		High Priority 0	High Priority 0

* causes low priority interrupt
** causes high priority interrupt

IN 8 BIT MODE, CONTROL CHARACTERS ARE EVEN PARITY AND DATA CHARACTER IS ODD PARITY

3.2.1 Status Register (device code = 460 or 470)

The CONO instruction sets or clears the Status Register in the DS10 if the I/O bit associated with the function is set or reset at the time the instruction is issued. All the status bits are reset by IOB RESET (initialization) except Clear-to-Send and Data Set Ready, which are controlled solely by the modem.

Bit 18 (Character Length) – This bit is set and reset by the CONO instruction (bit 18=1,0 respectively). When Character Length is set, both the transmit and receive sides of the DS10 will be operating in the 8-bit mode. The DS10 will be in 6-bit mode when Character Length is reset.

Bit 19 (Diagnostic) – This bit is set or reset by a CONO instruction (bit 19=1,0 respectively) to place the DS10 in and out of diagnostic mode. In the diagnostic mode, an internal clock is used to clock the data and the modem control functions are looped back to simulate various modem operations.

Bit 20 (Idle Enabled) – This bit is set or reset by the CONO instruction to enable or disable the DS10's idle mode operation. After the current word is transmitted, the DS10 enters the idle mode and transmits the first character of the next word repeatedly as long as Idle Enabled is set.

Bit 21 (Idle) – This bit is set when the DS10 has transmitted the last character of a transmit word, provided bit 20 (Idle Enabled) is set. When Idle is set, the DS10 will transmit the first character of the next word repeatedly without interrupting the processor until Idle Enabled is reset by a CONO instruction.

Bit 22 (Transmit-Active) – This bit is set if the first character in the transmit word is decoded to be a synchronous character by the DS10 and bit 25 (Clear-to-Send) is set. This bit is reset after the DS10 has transmitted the last character of a message. Transmit-Active signifies that the transmit logic is in operation and is actively transmitting data to the modem.

Bit 23 (Receive-Active) – This bit is set if a synchronous character is received from the modem. Receive-Active can be reset either by a CONO instruction (with bit 23=1), or when a loss of receive clock is detected. This bit, when set, signifies that the receive logic is actively receiving data from the modem.

Bit 24 (Receive Inhibit) – This bit is set by the programmer to inhibit the echoing back of information that usually occurs during half-duplex operation. The bit is set and reset by a CONO instruction (bit 24 = 1,0 respectively).

Bit 25 (Clear-to-Send) – Data cannot be transmitted over the communication link if Clear-to-Send is reset. This bit will be set when the communication link is established.

Bit 26 (Data Terminal Ready) – This bit is set and reset by a CONO instruction (bit 26=1,0 respectively). When this bit is set, either an attempt is being made to establish a data link, or the link is already in operation.

Bit 27 (Ring Enabled) – This bit is reset and set by a CONO instruction (bit 27=0,1 respectively). When this bit is set, the Ring signal from the modem will be allowed to cause a low priority interrupt.

Bit 28 (Data Set Ready) – Data Set Ready will be set when the modem is ready for normal operation. Data Set Ready will be reset if the modem is not operable or is in test mode.

Bit 29 – not used

Bit 30 (Ring Flag) – This bit is set by the Ring signal from the modem, provided Ring Enabled (bit 27) is set. When this bit is set, a low priority interrupt will be generated. This bit is reset by a CONO instruction (bit 30=1).

Bit 31 (End Flag) – This bit is set if the Receive Clock from the modem had stopped before the EOT flag (bit 34) is set. This bit can be used to distinguish legitimate ends from those that are caused by failures in the communication link. A low priority interrupt will be generated when this bit is set. This bit is reset by a CONO instruction (bit 31=1).

Bit 32 (Error Flag) – This bit is set if the Receive Flag (bit 35) is not answered by the CP by the time another full character is received. When this happens, the character just received will be lost. The characters already assembled in the Data Buffer are not affected. A low priority interrupt is generated if this bit is set. Error Flag is reset by a CONO instruction (bit 32=1).

Bit 33 (Transmit Flag) – This bit is set if there is only one character left to be transmitted to the modem. A high priority interrupt will be generated if this bit is set. Transmit Flag is reset by a DATAO instruction.

Bit 34 (EOT Flag) – This bit is set if an End-of-Transmission character is received from the modem and is reset by a CONO instruction (bit 34=1).

Bit 35 (Receive Flag) – This bit is set when a full word has been received and assembled in the DS10. This bit is reset by a DATAI instruction. A high priority interrupt is generated when Receive Flag is set. The processor has one full character time to respond to this interrupt without losing data.

3.2.2 Status Register (device code = 464 or 474)

Table 3-2 shows the status bit arrangements. Six flip-flops are used to store the high and low interrupt channel numbers. These flip-flops will be reset by the IOB Reset pulse.

Bits 18 through 29 – not used

Bits 30 through 32 (Low Priority Interrupt) – These bits are used to store the low interrupt channel number when a CONO instruction is issued. The following conditions will cause a low priority interrupt to be generated:

a. Ring Flag (bit 30)
b. End Flag (bit 31)
c. Error Flag (bit 32)

Bits 33 through 35 (High Priority Interrupt) – These three bits are used to store the high interrupt channel number when a CONO instruction is issued. The following conditions will cause high priority interrupt to be generated:

a. Receive Flag (bit 35)
b. Transmit Flag (bit 33)

3.2.3 Data Register (device code = 460 or 470)

The DATAO will move a full 36-bit word from PDP-10 memory to the Transmit Data Buffer of the DS10. The DATAI will deliver a full 36-bit word from the Receive Data Buffer of the DS10 to the PDP-10 via the I/O Bus. The DS10 will assemble/disassemble 8- or 6-bit data characters to/from two 36-bit data buffers, each containing 4 or 6 characters. The individual characters of a word are left-justified. Figure 1-3 shows the breakdown of the 36-bit word using 6- and 8-bit characters.

Chapter 4
Principles of Operation

This chapter contains a description of the control, receive, and transmit logic, followed by a description of a typical receive-and-transmit sequence of operation.

The DEC engineering drawings referenced in this chapter are contained in Chapter 6. Each drawing reference consists of the drawing number and, when necessary, the alphanumeric coordinate location of specific logic on the drawing. For example, the origination of the signal CL INI is referenced as drawing DS10-0-CL, sheet 1, B2. It should also be pointed out that each signal is prefixed with the alpha portion of the drawing number from which it originates. For example, TB LOAD 01 is developed on drawing DS10-0-TB, RL SHIFT RB is developed on drawing DS10-0-RL, etc.

4.1 CONTROL LOGIC

The control logic consists of selection logic, I/O instruction decoding, status conditions, and priority interrupts. The logic for these functions is shown on drawing DS10-0-CL, sheets 1 and 2.

4.1.1 DS10 Selection Logic

Each peripheral unit that shares the PDP-10 I/O Bus requires a unique device selection code in order to respond to commands from the CP. The DS10 device code number, received from the PDP-10 instruction register, appears at the W851 Connector located at EF07 (see dwg. DS10-0-IO, sheet 1) on seven pairs of complementary lines (IOS3 through IOS9). When only one DS10 is used in the system, the device code is 460_8 and 464_8. Two device numbers are required because of the large amount of status information that must be carried between the DS10 and the PDP-10. If a second DS10 unit is used in the system, the device code is 470_8, 474_8.

The IOS lines are connected to a W991 Jumper Board (see dwg. DS10-0-JB) that is prewired to recognize the 460_8 or 464_8 codes. When a code is detected, the levels JB IOS 03 through JB IOS 09 become active. (If other device codes are to be used, the W991 Jumper Board can easily be changed to detect the codes.)

4.1.2 I/O Instruction Decoding

The JB IOS 03 through JB IOS 09 levels are combined to produce the signals CL SELECT A and CL SELECT B (see dwg. DS10-0-CL). The CL SELECT signals are gated with various processor outputs to produce the command signals such as CL DATAO SET A and CL CONI B. The functions of each command are discussed in the sequence of operation (refer to Paragraphs 4.3 and 4.5).

4.1.3 Status Condition

The flip-flops located in the lower left-hand corner of drawing DS10-0-CL, sheet 2 allow the program to determine the status of various conditions in the system. These status flip-flops are set, cleared, and read by the I/O commands with certain bits enabled.

4.1.4 Priority Interrupts

Whenever the DS10 requires service from the PDP-10, a priority interrupt must be generated and issued to the CP before the DS10 can be acknowledged. The priority interrupts used in the DS10 unit are shown generated on drawing DS10-0-CL, sheet 2. A specific priority interrupt line is activated by signals CL HI PI or CL LO PI, combined with the states of CL HI PI 0 through CL HI PI 3, or CL LO PI 0 through CL LO PI 3, flip-flops. CL HI PI is generated when either TL XMIT FLG or RL REC FLG is set. The CL LO PI signal is generated when either CL RING FLG, CL END FLG, or CL ERR FLG is set. Flip-flops CL HI (LO) PI 0 through 3 are set by a CONO instruction to activate one of the seven interrupt channels assigned to the DS10 by the programmer.

4.2 RECEIVE LOGIC

This section contains an operating description of the main segments of the receive logic: the buffer register, shift register, character counter, sync character detector, and EOT detector.

4.2.1 Receive Buffer Register (Dwg. DS10-0-RCW)

The receive buffer register (RCW0 through RCW35) stores successive characters formed by the RB shift register until a full word (four 8-bit characters or six 6-bit characters) is assembled. The complete word is then sent in parallel via the IOB Bus Lines to the PDP-10 computer. Each character is jam-transferred into the RCW buffer register by the RL LO RCB 00 or RL LO RCB 18 pulse.

4.2.2 Receive Shift Register (Dwg. DS10-0-RB)

The RB receive shift register continually assembles a stream of incoming data bits into characters for eventual transfer to the RCW buffer register. (Characters actually go through an intermediate buffer stage designated RB RCB 0 through 35.) When a sync character is detected and transferred to the RCW register, the 1 IN pulse presets the most significant bit (either RB8 or RB6) to a 1. This 1 bit is designated the sentinel bit. Pulse RL SHIFT RB then shifts the data in, least significant bit first, and shifting continues until the sentinel bit is present in stage RB1. After one more shift, a fully assembled character is transferred to the RCW register and the preceding operation starts again for the next character. The character length flip-flop determines whether the RB1 through RB6 stages or the RB1 through RB8 stages are to be used.

Once a character is formed in the shift register, it is jam-transferred into the correct location in the buffer register. For example, in 6-bit mode with the character counter at zero, RB6 through RB1 is jam-transferred into RCW0 through RCW5; however, with the character counter at two (third character), RB6 through RB1 is gated into RCW12 through RCW17 (see Figure 4-1).

4.2.3 Receive Character Counter (Dwg. DS10-0-RL)

The receive character counter (RL RCL 00 through 02) is a typical binary up-counter that enables successive characters assembled in the shift register to be loaded into the correct locations in the RCW buffer register. When a 6- or 8-bit character is assembled in the shift register, the character counter outputs (signals RL RCNT 00 through 05) determine where in the RCW register the character is to be loaded (see dwg. DS10-0-RL, sheet 1).

Signal RL RCNT 00 is asserted when the counter is at zero. If the mode of operation is 6-bits-per-character, the level CL LNT 06 is true, and is combined with RL RCNT 00 to produce RL LOAD 10 (see dwg. DS10-0-RB). Signal RB LOAD 10 is gated with shift register bits RB 06 through RB 01 to generate RB RCB 00 through 05, which in turn is loaded into the RCW buffer register locations RCW00 through RCW05 (see Figure 4-1). The counter is then incremented, producing RL RCNT 01, which enables the next character in the shift register to be loaded into RCW06 through RCW11. In this 6-bit example, the counter is incremented until it reaches

RL RCNT 05. At this time the RCW buffer register is full; the counter is therefore cleared in preparation for the next word. If the mode of operation is 8-bits-per-character, the counter is cleared after it has reached RL RCNT 03. The preceding example of 6-bits-per-character operation with counter at zero is illustrated in Figure 4-2.

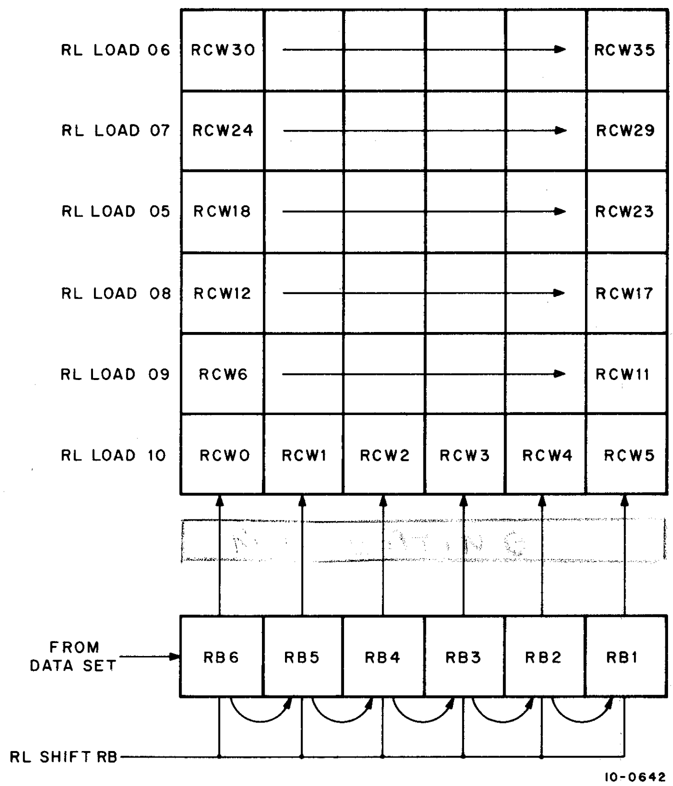


Figure 4-1 Shift Register Operation for Six-Bit Character

4.2.4 Receive Sync Character Detector

The receive sync character detector (see dwg. DS10-0-RL, sheet 1, C3) monitors the contents of the RB shift register in search of a 26_8 code for 6-bit characters or a 026_8 code for 8-bit characters. Sync character detection operates as follows for a 6-bits-per-character mode. Shift register bits RB02 through RB06 are connected at module location AB24 to a W991 Jumper Board that is shown prewired to detect a 26_8 code (see dwg. DS10-0-JB). When bits RB06 through RB02 reflect a $10\ 110_2$, the signals JB REC SYNC 01 through 05 are activated and produce the RL RB EQ SYNC signal (see dwg. DS10-0-RL). If 8-bits-per-character mode is used, signals JB REC SYNC 01 through 07, ANDed with the set state of the length flip-flop, would produce RL RB EQ SYNC.

At this point, however, it is not known if the incoming character is actually a sync code until one more data bit is checked. Therefore, the DS10 logic "looks ahead" at the next incoming bit, which is represented by RL RED 00 or RL RED 01. If this bit is a zero, then the character is indeed a sync character, and signal JB REC SYNC 08A (6-bit) or JB REC SYNC 08B (8-bit) is activated. Signal JB REC SYNC 08A(B) is combined with RL RB EQ SYNC to set the RL REC ACT flip-flop (see dwg. DS10-0-RL, sheet 2, D6). With the receive logic active, the character in the shift register is shifted one more time to bring in the last bit of the sync character. The assembled character is then transferred to the receive buffer register.

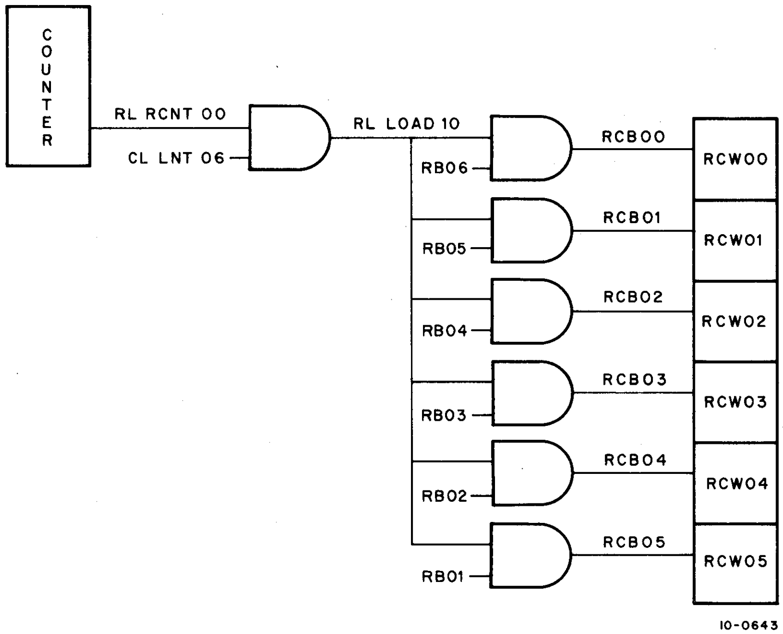


Figure 4-2 Receive Character Counter, 6-Bits Operation

The above description uses a 26_8 code for sync character detection. Other codes can be used by the customer simply by changing the wires on the W991 Jumper Board at location AB24.

4.2.5 Receive End-of-Transmission Detector

While the receive mode is in operation, the contents of the RB shift register are monitored by a W991 Jumper Board at module location AB26 (see dwg. DS10-0-JB). The jumper board is prewired to detect a code of 04_8 for 6-bit mode and 004_8 for 8-bit mode. When either of these codes is recognized, levels JB EOT BIT 01 through 06 (6-bit mode) or levels JB EOT BIT 01 through 08 (8-bit mode) are activated and applied to a NAND gate to produce RL RB EQ EOT (see dwg. DS10-0-RL, sheet 1, C1).

Signal RL RB EQ EOT sets the CL EOT FLG when the EOT character is loaded into the buffer register (see dwg. DS10-0-CL, sheet 2). The EOT code may be changed by the user simply by configuring the wires on the W991 Jumper Board at location AB26.

4.3 RECEIVE SEQUENCE OF OPERATION

This section describes in detail the sequence of operation for the receive mode (previously discussed in Section 4.2).

4.3.1 Overview

Serial data on the RECEIVE DATA line is continually assembled in a shift register under control of the trailing edge of the SERIAL CLOCK RECEIVE pulse stream from the data set. A sync character is required at the start of each message to activate the receive logic; any data sent to the DS10 before a sync character is detected is lost. Once a sync character is recognized, a sentinel bit is set in the most significant bit of the receive shift register. (Prior to this, the character length (6 or 8 bits) is set by means of a CONO instruction.) The next incoming character is assembled when the sentinel bit is shifted out of the least significant stage.

Assembled characters are transferred to the receive data buffer until the buffer contains a word (either four 8-bit characters or six 6-bit characters). At this point a program interrupt is generated and answered by the CP, with a DATAI instruction that loads the assembled word into the processor via the I/O Bus lines.

4.3.2 Initialization

Whenever IOB RESET or a power failure occurs, a signal designated CL INI is generated (see dwg. DS10-0-CL, sheet 1, B2); this signal clears all status flip-flops to prepare them for a receive operation. The IOB RESET signal is sent to the DS10 via the I/O Bus under the following conditions:

a. When CP power is first turned on
b. When READ-IN button on processor console is pushed
c. When RESET button on processor console is pushed

If a power failure occurs, a signal designated CROBAR is developed by the 844 Power Control Unit; this signal clamps the outputs of the CL LO PI and CL HI PI flip-flops, thereby preventing any interrupt requests (see dwg. DS10-0-CL, sheet 2, C7). The CL INI pulse that clears the DS10 status flip-flops is also generated by CROBAR during a power failure: the R303 Integrating-One-Shot (see dwg. DS10-0-CL, sheet 2, B4) is direct-set by CROBAR and, after a preset time, returns to zero. This ground output pulse is applied to an amplifier that produces CL INI. (The delay in the R303 allows the current cycle to be completed before CL INI is generated.)

Once the DS10 is initialized, events are under control of the data set clock pulses.

4.3.3 Establishing a Link Between DS10 and Modem

In the type of link that utilizes the dial-up facilities of the Bell System, the calling station dials (either manually or automatically) the phone number assigned to the data access equipment. The RING INDICATOR lead (EIA Interface) goes active and sets the CL RING FLG flip-flop (see dwg. DS10-0-CL, sheet 2), provided CL RING ENBL is previously set by a 460_8 CONO instruction with IOB 27 = 1. With CL RING FLG (1), a low priority (CL LO PI) interrupt is generated. The program issues a 460_8 CONI instruction to find the cause of interrupt and, with IOB 30 (1), determines the CL RING FLG is set, indicating a data set has information to be sent to the processor.

At this time the program issues a 460_8 CONO instruction to reset CL RING ENBL (IOB 27 = 0), reset CL RING FLG (IOB 30 = 1), and set CL TERM RDY (IOB 26 = 1). By resetting CL RING ENBL, all future interrupts caused by a ringing signal will be inhibited. Flip-flop CL TERM RDY (1) produces RS DTR Data Term Ready (DS10-0-RS), which causes the data set to start sending information and Serial Clock pulses. The receive logic, however, remains inactive until a sync character is detected. Any data sent prior to a sync character is lost.

4.3.4 Receive Active (Figure 4-3)

Timing pulses from the data set enter the DS10 EIA Interface (see dwg. DS10-0-RS) as SERIAL CLK RECEIVE (SCR). These RS SCR pulses are negative levels that are converted to standard DEC levels (0V and -3V) by a

W511 module to produce RS REC TME. Pulse RS REC TME, in turn, generates RL SHIFT RB for either 6- or 8-bit characters (see dwg. DS10-0-RL, sheet 1, D3, D4).

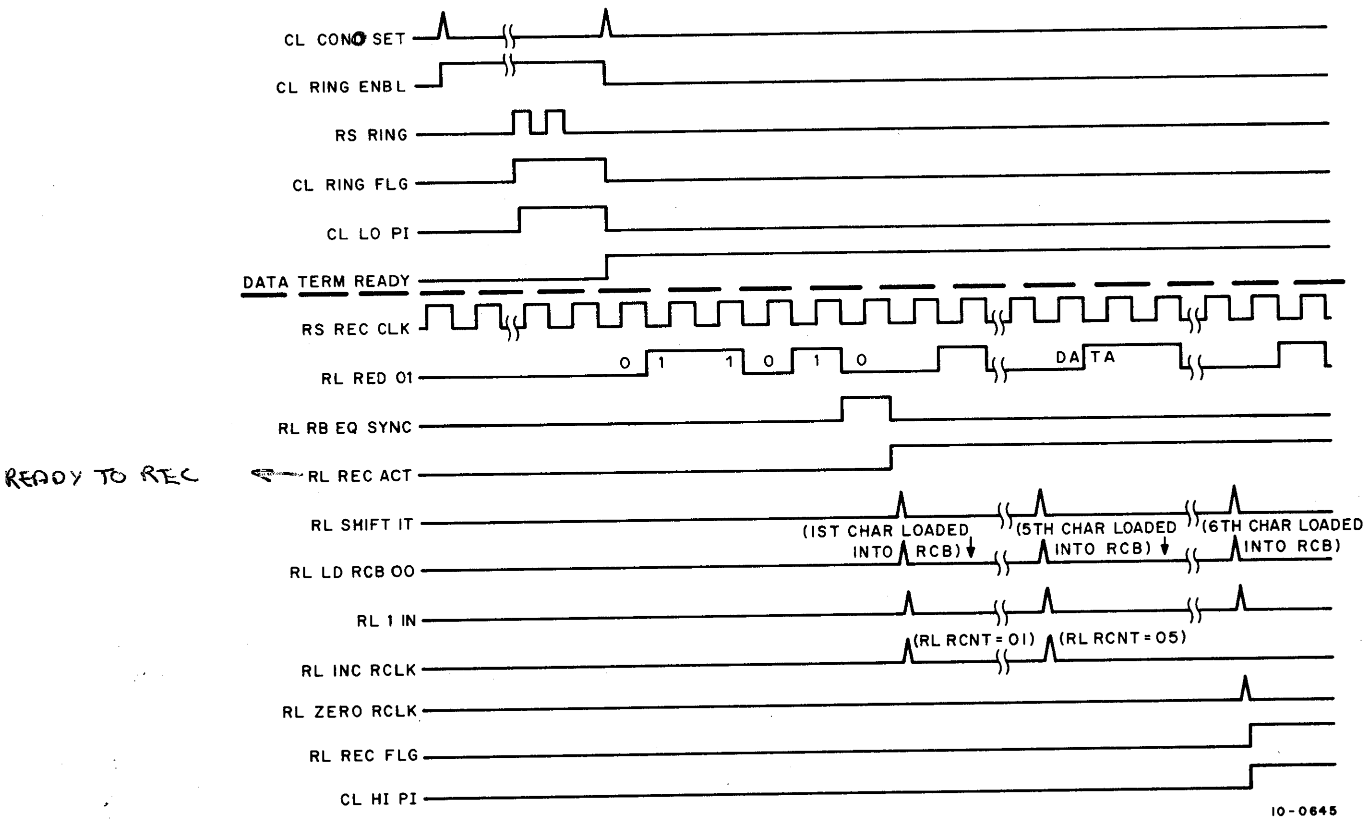


Figure 4-3 Receive Timing Diagram

Data enters the DS10 EIA Interface as RS REC DATA and is converted to DEC levels by a W511 module, the output of which is designated RS DATA (see dwg. DS10-0-RS, D5). Each RS DATA pulse represents one bit of information and is first applied to the W991 Jumper Board at AB26 (see dwg. DS10-0-JB), which is shown jumpered for conventional polarity modems. The W991 output, designated JB DATA IN, generates pulse RS DATA BUF (see dwg. DS10-0-RS, A5). If RS DATA BUF represents a 0, it is ANDed with RL SHIFT RB to produce RL RED 00 (see dwg. DS10-0-RL, sheet 2). If the data bit is a 1, RS DATA BUF is ANDed with RL SHIFT RB to produce RL RED 01.

Each RL RED 01 or RL RED 00 pulse is applied to either stage RB08 or RB06 (depending on the predetermined character length) and shifted through the RB shift register by RL SHIFT RB pulses. As the data moves through the shift register, the sync character detector is constantly looking for a code of 26_8 for 6-bit characters or 026_8 for 8-bit characters.

When a sync character is detected, the signal RL RB EQ SYNC is issued. At the next RS REC TME, a RL SHIFT RB pulse is generated as usual but, with RL RB EQ SYNC true, flip-flop RL REC ACT is set (see dwg. DS10-0-RL, sheet 2, D6).

4.3.5 First Character

With RL REC ACT (1), the first character (sync character) is completely assembled in the RB shift register with the least significant bit in RB01. The 0 side of REC ACT initiates a RL SHIFT IT pulse (see dwg. DS10-0-RL, sheet 2, C5) that triggers a 1.5 μs delay. After the delay times out, pulses RL LD RCB 00 and RL LD RCB 01 are generated; these pulses enable the character in the RB shift register to be loaded into the RCW receive buffer register. Because the RL RCL character counter was set to zero (RL RCNT 00) by the CL INI pulse, the contents of the shift register are loaded into the first character position (RCW0 through 5) of the receive buffer register (see Figure 4-2). An RL CLR RB pulse is also generated at the end of the 1.5 μs delay to clear the RB shift register in preparation for the next character.

4.3.6 Successive Characters

In addition to the RL LD RCB and RL CLR RB pulses generated at the end of the 1.5 μs delay, a 1 μs delay is triggered. When the 1 μs delay times out, it produces a pulse designated RL 1 IN. The RL 1 IN pulse is applied to the set side of either stage RB08 or RB06, depending on the character length. This preset 1 condition acts as a sentinel bit; a complete character will be present in the RB shift register when this bit is shifted out of RB01. The RL 1 IN pulse also initiates the RL INC RCLK pulse that increments the RL RCL character counter.

On the next RL SHIFT RB pulse, the sentinel bit is shifted right one place and the least significant bit of the second character is loaded into either stage RB08 or RB06. This shifting continues until the sentinel bit is present in stage RB01. On the next RL SHIFT RB pulse, the least significant bit of the second character is shifted into stage RB01 (flip-flop RL REC ACT is still set). After the 1.5 μs delay times out, the RL LD RCB pulse is issued and the second character is loaded into locations RCW6 through 11. The RB shift register is cleared by the RL CLR RB pulse. One μs later, the RL 1 IN pulse clocks the RL RCL 00 flip-flop, thus causing the RL RCL 01 flip-flop to be incremented and allowing the gates for the third character to be enabled.

The RL 1 IN pulse again sets the most significant bit of the RB shift register and the third character starts coming in. Operation proceeds as before for the remaining characters of the word.

4.3.7 Last Character of the Word

In 8-bits-per-character mode, the fourth character (last) is shifted in and loaded into RCW24 through 31. Pulse RL 1 IN is generated as usual but levels RL CNT 03 and CL LNT 08 are asserted, thereby preventing the character counter from being incremented. Instead, pulse RL ZERO RCLK (see dwg. DS-0-RL, sheet 2, B4), which serves to clear the character counter to zero, is asserted. At the same time, with RL REC ACT (1), pulse RL ZERO RCLK sets the RL REC FLG, causing a high priority interrupt to be generated (see dwg. DS10-0-CL, sheet 2, C7).

The high priority interrupt indicates to the PDP-10 that there is a complete word in the RCW buffer register. The processor answers this interrupt with a DATAI instruction. If the processor fails to answer the interrupt prior to the time the least significant bit of the next character is shifted into RB01, status flip-flop CL ERR FLG is set. With the error flag set, all future characters are inhibited from being loaded into the RCW buffer register. However, the characters stored in the RCW prior to the interrupt are retained and can be read in by a DATAI instruction.

If the mode is 6-bits-per-character, the character counter is incremented until level RL RCNT 05 is active. At this time the signal RL ZERO RCLK is asserted and causes an interrupt in the same manner as above.

As long as flip-flop RL REC ACT is set, subsequent data characters are shifted in, stored in the RCW buffer register until it is full, and finally sent on to the PDP-10. This procedure continues until an end-of-message code is detected.

4.3.8 End-of-Transmission (EOT) Character

While data is being shifted in, the W991 character detector monitors the contents of the RB shift register. When an EOT character is detected, signal RL RB EQ EOT is asserted, causing status flip-flop CL EOT FLG to be set. The EOT flag in the set state does not cause an interrupt, but will be read as bit IOB 34 (1) by a 310 CONI instruction.

It is up to the program to determine whether the EOT character is a legitimate end-of-message code, or just a character that has the same binary configuration (the latter can occur if the message is being received in transparent mode). If the character is a legal EOT character, a CONO instruction is issued to reset flip-flop RL REC ACT (bit IOB 23 set). At this point, with RL REC ACT (0), another sync character is required to enable the receive logic.

For certain types of modems, the modem serial receive clock (SCR) pulses will stop occurring when there is no data on the Receive Data lead. When this happens, pulse RS CARRIER is developed and triggers an R303 Integrating-One-Shot (see dwg. DS10-0-RS, B2). After 1.5 bit lengths (approx. 600 μs), signal RS REND is produced and generates RL PAEND (see dwg. DS10-0-RL, D6). RL PAEND resets RL REC ACT and sets CL END FLG (see dwg. DS10-0-CL, sheet 2) if EOT FLG is not already set. A low priority interrupt is generated when CL END FLG (1); the End Flag is reset by a CONO with IOB 31 (1).

4.4 TRANSMIT LOGIC

This section contains a description of the major elements in the transmit logic.

4.4.1 Transmit Data Buffer and Gating

The transmit data buffer register (DB0 through 35) stores, in parallel, a 36-bit word sent from the PDP-10 CP. One character at a time is then jam-transferred from this data buffer register into the transmit shift register. When either four or six characters (8- or 6-bits per character respectively) have been transmitted, the buffer register is cleared to accept another word from the PDP-10.

The input gating preceding the transmit buffer register employs six W107 Bus Receiver Modules (see dwg. DS10-0-IO). Each module contains six identical non-inverting receiver circuits for buffering signals from the I/O Bus.

4.4.2 Transmit Shift Register

The transmit shift register (see dwg. DS10-0-TB, sheet 1, D1–D7) is a variable length (6- or 8-bits) register that shifts characters serially to the data set. Figure 4-4 illustrates the general flow of operation for a 6-bit character. Each character is jam-transferred in from the transmit data buffer register with the least significant bit gated into TB1. At the same time, a ONE is set into the END stage. As each TL SHIFT TB pulse occurs, the character is shifted one place towards TB1 and out to the data set until the END bit is detected, indicating the character in the TB has been sent.

As the character is shifted toward TB1, zeros are loaded into the vacated bit positions. The TL CNT0 through 5 signals determine which character is to be loaded into the TB.

4.4.3 Transmit Sync Character Detector

A sync character is required to activate the transmit logic portion of the DS10. Because the sync character detector monitors only bits DB00 through 05 (or DB00 through 07), the sync character must be in the first character location of the word sent from the PDP-10 (see dwg. DS10-0-JB). When a sync code is detected, signals JB XMIT SYNC 00 through 05 (or JB XMIT SYNC 00 through 07) are asserted and, combined with the state of the length flip-flop, generate TL CW EQ SYNC (see dwg. DS10-0-TL, sheet 1, D5–D8).

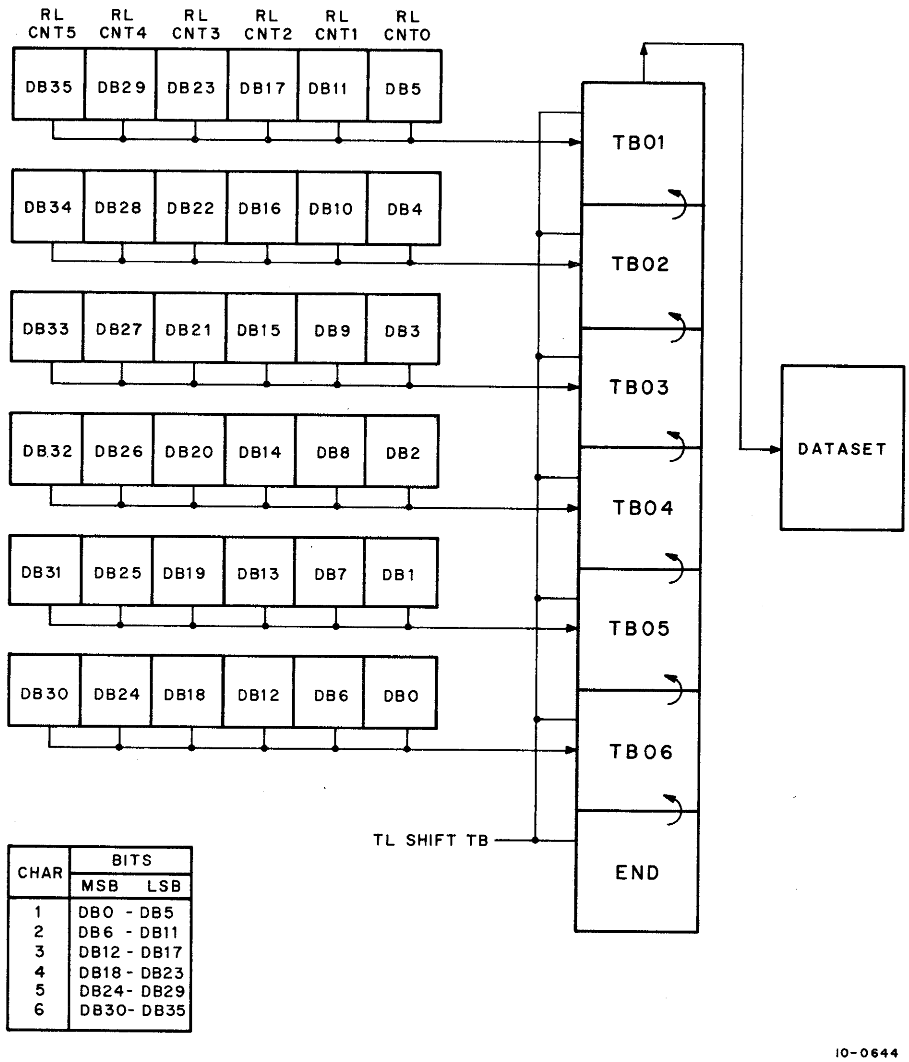


Figure 4-4 Six-Bit Character Operation Through the Shift Register

4.4.4 Last Bit Detector

The last bit detector monitors the contents of the TB shift register and generates the TL LAST BIT signal when TB03 through 08 and the END bit are all zeros. This condition occurs when the END bit has been shifted to TB02, indicating the most significant bit of the character is in TB01.

4.4.5 Transmit Character Counter

The transmit character counter (TL XCL 00 through 02, dwg. DS10-0-TL, sheet 2) operates as a typical binary up-counter that enables successive characters of a word to be loaded into the TB shift register from the DB buffer register. Figure 4-4 shows the respective counter outputs as they affect the DB register. The signal TL CHAR TO TB initiates the actual loading of the TB, but the character counter determines which six or eight bits should be loaded.

4.5 TRANSMIT SEQUENCE OF OPERATION

This section describes a typical transmit sequence of operation and expands upon the discussions in 4.4 (see Figure 4-5).

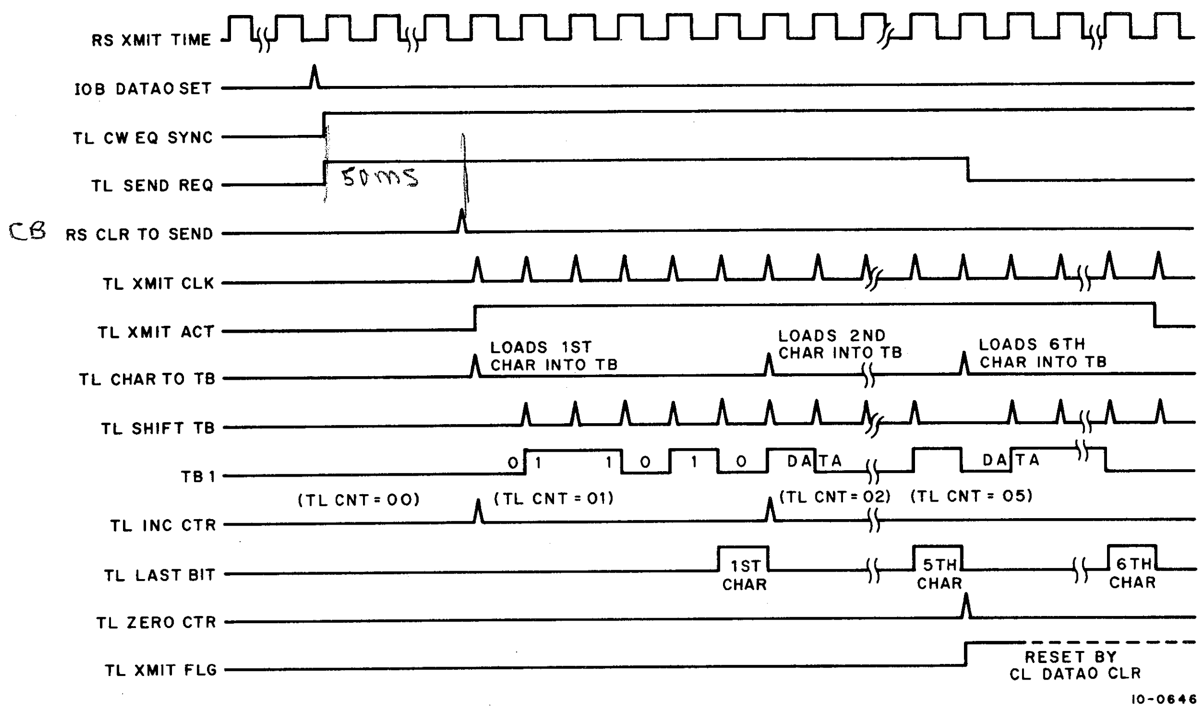


Figure 4-5 Transmit Timing Diagram

4.5.1 Transmit Active

A transmit operation begins when the program issues a DATAO instruction that enables the data on the IOB lines to be loaded into the DB register (see dwg. DS10-0-DB). For the transmit logic to be activated, however, a sync character must be detected. As mentioned in Section 4.4.3, the sync character must be in locations DB00 through 05 (or DB00 through 07 for 8-bit characters). When a sync character is recognized, the signal TL CW EQ SYNC is generated, causing the TL SEND REQ flip-flop to be set. TL SEND REQ (1) allows the RS RTS Request-to-Send lead on the modem to turn on (see dwg. DS10-0-RS). Approximately 50–500 ms later, the modem responds with RS CTS Clear-to-Send (which produces RS CLR TO SND) and sometime later, RS SCT serial clock transmit (produces RS XMIT TIME). Signal RS CLR TO SND forces the TL XMIT ACT flip-flop to remain reset until the RS XMIT TIME pulses arrive. The RS XMIT TIME pulse is then ANDed with RS CLR TO SND to produce TL XMIT CLK (see dwg. DS10-0-TL, sheet 2, C3).

At this point, TL CW EQ SYNC and TL XMIT CLK are ANDed to set the TL XMIT ACT flip-flop (see dwg. DS10-0-TL, sheet 1, B2). With TL XMIT ACT (1), synchronization is established.

4.5.2 First Character

Up until now the sync character has been detected and the TL XMIT ACT flip-flop has been set. To transfer the first character (sync character) from the DB buffer register to the TB shift register, a signal designated TL CHAR TO TB is developed (see dwg. DS10-0-TL, sheet 2, C3). To initially generate TL CHAR TO TB, the signals TL XMIT ACT (0) and TL CW EQ SYNC must be coincident with signal TL XMIT CLK (see dwg. DS10-0-TL, sheet 2). Because the character counter was reset by the CL INI pulse at the start of the operation, counter level TL CNT 00 is true. If the DS10 is operating in 6-bit mode, TL CNT 00 is ANDed with CL LNT 06 to produce TB LOAD 07 (see dwg. DS10-0-TB, sheet 1, B5). Note that TB LOAD 07 enables bits DB 00 through 05 to generate TB BIT 06 SET through TB BIT 01 SET, respectively (see dwg. DS10-0-TB, sheet 2). Thus the first character is loaded in parallel into the TB shift register with the least significant bit in TB01. The TL CHAR TO TB also sets the END flip-flop. (If the DS10 is operating in 8-bit mode, with TL CNT 00 true, signal TB LOAD 03 would be generated, enabling bits DB00 through 07.) At the same time the TL CHAR TO TB is generated, a TL INC CTR pulse is generated that increments the character counter in preparation for the next character.

On the next TL XMIT CLK pulse, a signal (TL SHIFT TB) is generated that shifts the TB one place towards RB01 (see dwg. DS10-0-TB, sheet 1) and out to the data set. Each TL SHIFT TB pulse causes each TB stage to assume the state of the preceding stage. Eventually the END bit arrives at TB02. When this occurs, and the other TB flip-flops of higher order are all zeros, TL LAST BIT is generated, indicating the most significant bit of the first character is in TB01. On the next TL XMIT CLK pulse, TL SHIFT TB is not generated. However, TL CHAR TO TB is generated to jam-transfer the second character of the word into the TB register. TL CHAR TO TB also increments the counter again in preparation for the third character.

4.5.3 Successive Characters

When the second character is ready to be transferred to the TB register, counter level TL CNT 01 is asserted. If 6-bit mode is selected, TL CNT 01 is combined with CL LNT 06 to produce TB LOAD 06. If 8-bit mode is selected, TL CNT 01 is combined with CL LNT 08 to produce TB LOAD 02 (see dwg. DS10-0-TB, sheet 1).

The second character is shifted through the TB in the same manner as the first character until the last bit is detected. The TL CHAR TO TB signal is generated, again causing the third character to be jam-transferred into the TB and incrementing the counter to produce TL CNT 03. In a similar manner, the third character is shifted through the TB, a last bit is detected, and the fourth character is loaded into the TB register.

At this point, if 8-bit mode is selected, the fourth character is shifted through as usual but with TL CNT 03 and CL LNT 08 true, a signal designated TB RST 08 is produced (see dwg. DS10-0-TB, sheet 1). On the next TL CHAR TO TB generated, instead of incrementing the counter, TB RST 08 causes TL ZERO CTR to be generated (see dwg. DS10-0-TL, sheet 2, D1). Signal TL ZERO CTR sets the TL XMIT FLG (see dwg. DS10-0-TL, sheet 1), generating a high priority interrupt (see dwg. DS10-0-CL, sheet 2). The PDP-10 program responds to the interrupt with a 460_8 DATAO instruction containing another word for transmission. The DATAO instruction clears the TL XMIT FLG and removes the interrupt from the IOB lines.

If the mode is 6-bits-per-character, two more characters are transferred before the TL XMIT FLG is set. With CL LNT 06 true, the counter is incremented until it reaches TL CNT 05, at which time signal TB RST 06 is generated (see dwg. DS10-0-TB, sheet 1). TB RST 06 and TL CHAR TO TB combine to generate the TL ZERO CTR pulse, which sets the TL XMIT FLG flip-flop. Again the program responds to the interrupt with a DATAO instruction that loads another word into the DB register. In either the 6- or 8-bit mode, the least significant bit of the first character of the succeeding word follows the last bit of the word shifted out. This procedure continues until the last character in the message is transmitted.

4.5.4 Last Character of Message

When the last character of the message is placed in the TB, the TL XMIT FLG is set, generating a high priority interrupt. However, the program does not respond with another DATAO that normally clears the TL XMIT FLG. As the last character is shifted out, signal TL LAST BIT is activated and, with TL XMIT FLG (1), generates TL XMIT OK (see dwg. DS10-0-TL, sheet 1, B2). On the next clock pulse TL XMIT OK resets TL XMIT ACT, which causes TL XMIT FLG to be cleared. Signal TL XMIT OK also clears the TL SEND REQ flip-flop, causing the Request-to-Send lead to the modem to turn off.

4.5.5 Idle Mode Operation

An additional feature contained within the transmit logic is the ability to idle the Send Data lead to the modem without actually removing the Request-to-Send lead. This mode is useful when there is a small pause between messages, because the time to establish a link is bypassed. The idle mode is entered when the TL IDLE flip-flop is set by CL IDLE ENBL (1).

With the logic in the idle mode, the first character of the next word in the DB buffer register is repeatedly sent to the modem. This occurs because the character counter is never incremented; TL IDLE (1) keeps generating TL ZERO CTR (see dwg. DS10-0-TL). The idle mode is exited by issuing a CONO instruction with IOB 20 (0) to reset Idle Enable. When this process is completed, the remaining characters in the DB buffer register can be transmitted. These remaining characters can constitute the beginning of the next message.

4.6 DIAGNOSTIC MODE

The diagnostic mode simulates the modem receive and transmit clock to aid in DS10 maintenance. All of the logic for the diagnostic mode is shown on drawing DS10-0-RS. Transmit data is fed back to the Receive Data lead and the other modem control functions are also looped back to simulate the modem operations. The diagnostic mode is entered when a CONO instruction is issued with IOB 19 (1) to set the RS DIAG flip-flop. The RS DIAG flip-flop is reset either by a CONO instruction with IOB 19 (0), or during DS10 power-up (by the CROBAR circuit). The modem cable does not have to be removed for diagnostic operation.

Chapter 5
Maintenance

5.1 SCOPE

Maintenance of the DS10 consists of preventive maintenance procedures that are performed periodically, and troubleshooting procedures that are performed in the event of equipment malfunction. For maintenance information on the PDP-10 CP and the data sets, refer to the Foreword of this manual for a list of applicable maintenance documents.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the DS10, and tasks performed periodically during its operating life to ensure satisfactory operating condition. Faithful performance of these tasks forestalls possible future failure by correcting minor damage and discovering progressive deterioration at an early stage. A log book used to record data found during the performance of each preventive maintenance task will indicate the rate of circuit deterioration and provide information enabling maintenance personnel to determine when components should be replaced to prevent failure of the equipment. These tasks consist of the following checks: mechanical checks which include cleaning and visual inspections; power supplies checks; and delay module timing checks and adjustments.

All preventive maintenance tasks should be performed as a function of conditions at the installation site and the down-time limitations of equipment use. Perform the mechanical checks at least once each month, or as often as required to maintain efficient functioning of the equipment. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. For a typical application, a schedule of every four months or 1000 equipment operating hours, whichever occurs first, is suggested.

5.2.1 Mechanical Checks

The following steps should be performed during a mechanical check; the indicated corrective action should be performed if a substandard condition is located.

Step	Procedure
1	Clean the exterior and the interior of the equipment cabinet housing the DS10 by using a vacuum cleaner or clean cloths moistened in nonflammable, nonconductive solvent. Be sure the solvent is not harmful to paint.
2	Clean dirt from the blower assemblies; be careful not to damage cable assemblies or modules.
3	Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas.

Step	Procedure
4	Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain; check mechanical security. Tape, solder, or replace any defective wiring.
5	Inspect each row of modules to assure that each module is securely seated in its connector.
6	Verify that the proper I/O Bus cables and all other interconnecting cables are firmly seated in their respective connectors.
7	Inspect power supply capacitors for leaks, bulges, or discolorations. Replace any capacitors indicating signs of malfunction.

5.2.2 Power Supply Check

The 728 (728A) Power Supplies provide -10 Vdc and -15 Vdc to the DEC logic. These voltages are not adjustable; therefore, if the output voltages or ripple content is not within specified tolerances, the power supply is defective and troubleshooting procedures should be performed. All measurements should be made at the logic racks.

Measure the +10 Vdc power supply and ensure that the voltage output is between +9.5 Vdc and +11.0 Vdc with less than 800 mV rms ripple. Measure the -15 Vdc supply and ensure that its output is between -14.5 Vdc and -16.0 Vdc, with less than 100 mV rms ripple.

5.2.3 Delay Adjustments

This section presents an off-line procedure for setting up the delay-one-shots and integrating-one-shots in the DS10.

5.2.3.1 Test Equipment – The following equipment is necessary for the procedure described in this section:

Oscilloscope, Tektronix Type 453 or equivalent.
Oscilloscope probes provided with ground leads.
Jumper leads, two 4-in. red jumpers.

5.2.3.2 Preliminary Connections – Before initiating the Delay Adjustment procedure, perform the following preliminary connections:

Step	Procedure
1	Connect pin D25H (RL REC ACT (1) H) to GROUND.
2	Connect pin F16V (RS DIAG CLOCK) to pin F16E (CL DATAI A).
3	Remove the R613 module from location D24.
4	Remove the R302 modules from locations F16 and F25. Adjust the lower potentiometer on each module clockwise to its maximum setting, then re-install the two modules in their respective locations.
5	Power up the DS10, then ground pin E17H (RS DIAG (1) H) to set the RS DIAG flip-flop. Initiate the RS DIAG CLOCK pulses.
6	Set oscilloscope to trigger internally from channel 1, select a vertical sensitivity of 1V per div, and sync negative.

5.2.3.3 **Delay Adjustment Procedure** – To set up the delay-one-shots and integrating-one-shots in the DS10, perform the following:

Step	Procedure
1	Connect channel 1 to pin E31D (RS REND). Adjust potentiometer of R303 module in location E31 for 650 μs negative level on channel 1.
2	Connect channel 1 to pin F16V (RS DIAG CLOCK). Adjust lower potentiometer of R302 module in location F16 for 300 μs negative level on channel 1.
3	Connect channel 1 to pin F25V (RS DIAG ENB). Adjust lower potentiometer of R302 module in location F25 for 100 μs negative level on channel 1.
4	Connect channel 1 to pin D23M (RL CLR RB). Adjust upper potentiometer of R302 module in location D23 for 1.5 μs negative pulse on channel 1.
5	Connect channel 1 to pin D23V (RL 1 IN). Adjust lower potentiometer of R302 module in location D23 for 1 μs negative pulse on channel 1.
6	Connect channel 1 to pin F16M (CL DATAI CLR). Adjust upper potentiometer of R302 module in location F16 for 2.5 μs pulse on channel 1.
7	Remove the following jumpers: D25H to GROUND E17H to GROUND F16V to F16E Re-install the R613 module in location D24.
8	To adjust the R303 module in location F20, turn its potentiometer fully CCW, then 10 turns CW.
9	The R302 one-shot (RS REC INH) in location F25 (upper potentiometer) must be adjusted to 100 ms while the DS10 is operating on-line with diagnostic test MAINDEC-10-D2KB running.

Table 5-1
Summary of DS10 Delay Settings

Signal	Print	Module	Location	Setting
RL CLR RB	RL	R302	D23M	1.5 μs
RL 1 IN	RL	R302	D23V	1 μs
CL DATAI CLR	CL	R302	F16M	2.5 μs
RS DIAG CLOCK	RS	R302	F16V	300 μs
F25M*	RS	R302	F25M	100 μs
RS DIAG ENB	RS	R302	F25V	100 μs
RS REND	RS	R303	E31D	650 μs
F20D	CL	R303	F20E	300 ms

* Set up on-line as described in Step 9.

5.3 TROUBLESHOOTING

Begin troubleshooting by repeating the operation during which the malfunction was initially observed, using the same conditions. Thoroughly check the operating conditions for proper control settings, and note the operation of all indicators before and at the time of malfunction. Careful checks should be performed to assure that the system is actually at fault before continuing the corrective maintenance procedures. Loose or faulty cable connections can often give indications very similar to those caused by internal malfunctions; faulty ground connections between pieces of equipment are a common source of trouble. If the malfunction is determined to lie within the DS10, but cannot be localized to a specific logic function, perform the diagnostic program procedure.

5.4 DIAGNOSTIC MODE

The two diagnostic programs listed below provide the most efficient way of checking out the DS10 operation:

MAINDEC-10-D2KB	Paper tape or DECtape, write-up, and listing
MAINDEC-10-D2LA	Paper tape or DECtape, write-up, and listing

Program D2KB is designed to check out one DS10 at a time for full-duplex operation. This program is always run, regardless of whether there is one or two DS10 units in the system. Prior to running D2KB, however, the adjustments in Section 5.2.3 should be performed. If two DS10 units are employed, program D2LA is used to check out the half-duplex operation after program D2KB has been run. In both cases, refer to the diagnostic write-up for operating instructions.

The diagnostic printout is generally self-explanatory, as indicated by the D2KB samples below:

```
DS-10 DATAPHONE INTERFACE TEST
THIS PROGRAM IS CODED FOR DEVICE CODES MIC=420 AND MPL=424.
DO YOU WISH TO CHANGE THESE?
 Y OR N - Y
DEVICE CODE FOR MIC= 310
DEVICE CODE FOR MPL= 314

DO YOU WISH TO CHANGE THE SIX AND EIGHT BIT SYNCH CHARACTERS FROM
26 AND 226?
 Y OR N - N

DO YOU WISH TO CHANGE THE SIX AND EIGHT BIT EOT CHARACTERS FROM 04
AND 004?
 Y OR N - N

TEST PASS COUNT = 2
PC=  012701
ERROR IN ALTERNATING BIT PATTERN - COMPARISON ERROR
CORRECT:   525252 525240
ACTUAL:    001777 777760
DISCREP:   524525 252520

ADDRESS OF INCORRECT WORD = 013535

TEST PASS COUNT = 7
PC= 006474
ERROR IN TRANSMIT FLAG TEST -
TEST 50 -FLAG DID NOT SET
CHECK FLOP OR ZERO CTR OR IDLE<0> OR BUSS XMITTER FOR BIT 33

DS-10 DATAPHONE INTERFACE TEST

TEST PASS COUNT = 1
PC=  004163
ERROR IN BASIC SELECTION TEST -
TEST01-DS-10 FAILED TO RESPOND TO CONO MIC COMMAND
MAYBE DS-10 IS NOT POWERED UP OR IS DEAD OR DOES NOT EXIST
```

Chapter 6

Engineering Drawings

6.1 GENERAL

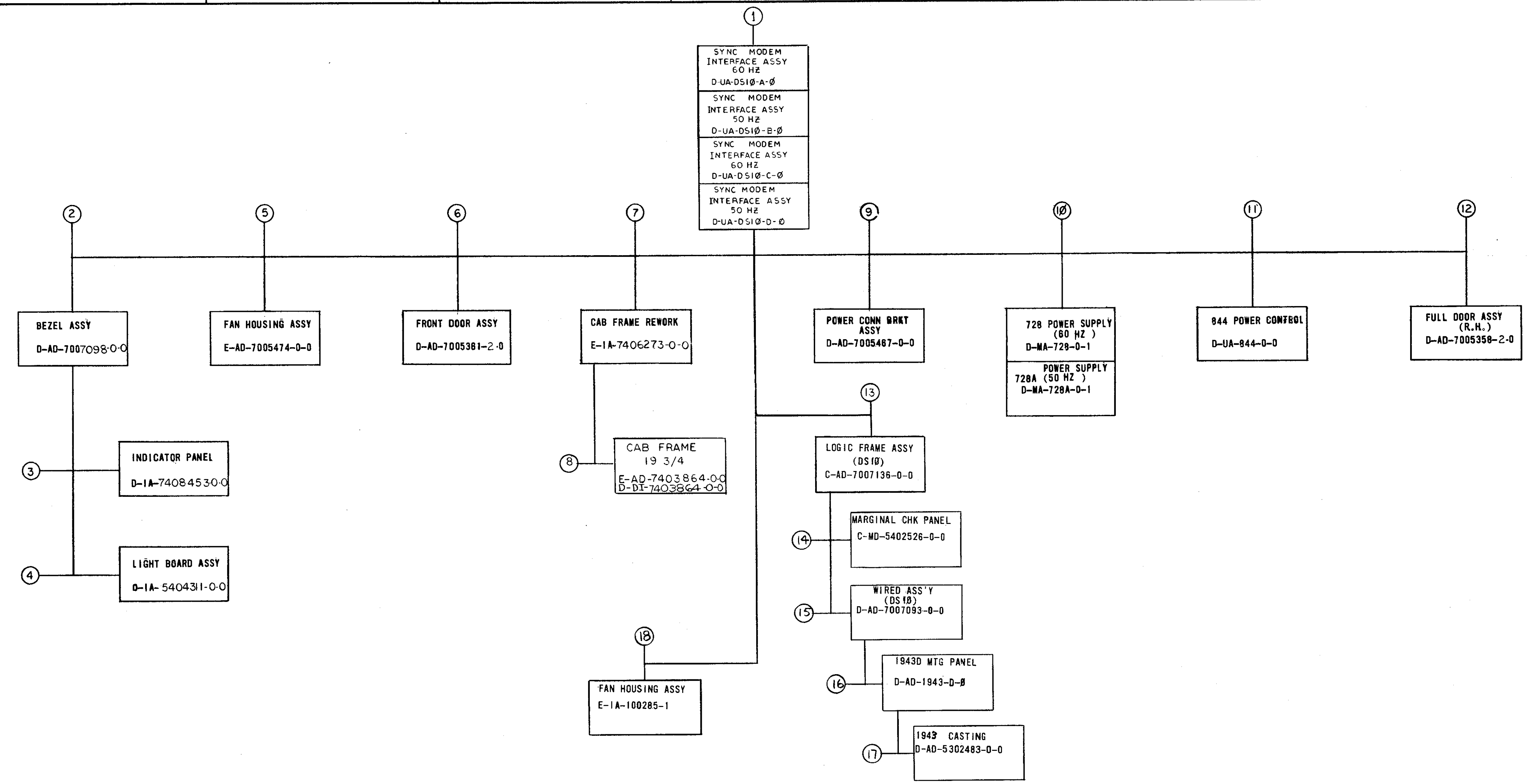
This chapter contains a complete set of DS10 engineering drawings for reference purposes. During actual maintenance, refer to the current prints supplied with the equipment.

6.2 ENGINEERING DRAWING LIST

Table 6-1
DS10 Engineering Drawings

Dwg. No.	Title	Page
D-DI-DS10-0-1	Drawing Index List (2 sheets)	6-3
D-UA-DS10-0-0	DS10 Unit Assembly (1 sheet)	6-7
A-PL-DS10-0-0	DS10 Unit Assembly Parts List (2 sheets)	6-9
A-ML-DS10-A	Master Drawing List – DS10A, 60 Hz (2 sheets)	6-11
A-ML-DS10-B	Master Drawing List – DS10B, 50 Hz (2 sheets)	6-13
A-ML-DS10-C	Master Drawing List – DS10C, 60 Hz (2 sheets)	6-15
A-ML-DS10-D	Master Drawing List – DS10D, 50 Hz (2 sheets)	6-17
D-BS-DS10-0-CL1	Control Logic (1 sheet)	6-19
D-BS-DS10-0-CL2	Control Logic (1 sheet)	6-21
D-BS-DS10-0-DB	Data Buffer (1 sheet)	6-23
D-BS-DS10-0-IO1	I/O Bus Interface (1 sheet)	6-25
D-BS-DS10-0-IO2	I/O Bus Interface (1 sheet)	6-27
D-BS-DS10-0-INDC	Indicators (1 sheet)	6-29
D-BS-DS10-0-JB	Jumper Boards (1 sheet)	6-31
D-BS-DS10-0-RB	Receive Buffer (1 sheet)	6-33
D-BS-DS10-0-RCW	Rec Bit Pack (1 sheet)	6-35
D-BS-DS10-0-RL1	Rec Logic (1 sheet)	6-37
D-BS-DS10-0-RL2	Rec Logic (1 sheet)	6-39
D-BS-DS10-0-RS	RS-232-C Interface (1 sheet)	6-41
D-BS-DS10-0-TB1	Transmit Buffer (1 sheet)	6-43
D-BS-DS10-0-TB2	Transmit Buffer (1 sheet)	6-45
D-BS-DS10-0-TL1	Transmit Logic (1 sheet)	6-47
D-BS-DS10-0-TL2	Transmit Logic (1 sheet)	6-49
D-MU-DS10-0-MU	Module Utilization Drawing (2 sheets)	6-51
A-PL-DS10-0-MU	Module Utilization Parts List (2 sheets)	6-55
D-IC-DS10-0-IOB	I/O Bus Interface (1 sheet)	6-57
D-IC-DS10-0-2	AC/DC Power Wiring, DS10A (B) (1 sheet)	6-59
D-IC-DS10-0-3	AC/DC Power Wiring, DS10C (D) (1 sheet)	6-61

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.



FIRST USED ON OPT/MOD: DS10

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —
FINISH —

QTY. | DESCRIPTION | PART NO. | ITEM NO.
PARTS LIST

DRN 9/28/70
CHK'D 10/20/70
ENG
PROJ ENG.
PROD 11/5/70
FIRST USED ON A-ML-DS10-A

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DRAWING INDEX LIST (DS10)

SIZE D CODE DI NUMBER DS10-0-1 REV.
SCALE —
SHEET 1 OF 2
DIST. G

REVISIONS | CHANGE NO. | REV. | CHK

DEC FORM NO. DRD 100

8	7	6	5	4	3	2	1

MECHANICAL

FIND NO.	DESCRIPTION	PART NO.	PROD	CUST	F/C
1	SYNC MODEM INTERFACE ASSY	D-UA-DS1Ø-Ø-Ø			
	SYNC MODEM INTERFACE ASSY (PL)	A-PL-DS1Ø-Ø-Ø			
	BRACKET (DOOR PIVOT)	B-MD-7405861-0-0			
	SPACER	A-MD-7405860-0-0			
	BLANK PANEL (7402027)	B-MD-5100			
	RMTE CONT MARGIN CHK CABLE	C-UA-BC1ØB-25-Ø			
	TRIM STRIP (BOTTOM)	D-MD-7405862-0-0			
	CHASSIS 7402033	B-MD-5111			
	CHASSIS 7402037	B-MD-5111			
	CABLE POWER TWIST LOCK	C-AD-7005128-0-0			
	END PANEL	E-IA-7405092-0-0			
	CABLE, BC10A (LGTH SPEC BY ENG)	D-UA-BC1ØA-Ø-Ø			
	BLANK PANEL 7402016	B-MD-5100			
	CABLE SET (DS1Ø-A&B)	D-AD-7007148-1-0			
	CABLE SET (DS1Ø-C&D)	D-AD-7007148-2-0			
	CABLE BC01R	D-UA-BCØ1R-25-Ø			
	CABLE BC10A	D-UA-BC10A-5-Ø			
2.	BEZEL ASSY	D-AD-7007098-0-0			
	BEZEL ASSY (PL)	A-PL-7007098-0-0			
	BEZEL INDICATOR (REWORK)	D-MD-7405729-1-0			
	BRACKET PANEL MTG	D-IA-7405929-0-0			
	PLATE STRIKER CASTING MTG	A-MB-7405899-0-0			
	RETAINER FR. PANEL	B-MD-7405931-0-0			
	SUPPORT GLASS	D-IA-7406192-0-0			
3.	INDICATOR PANEL	D-IA-7408453-0-0			
	SILK SCREEN, FRONT (GRY)	C-SS-7408453-0-1			
	SILK SCREEN, REAR (BLK)	C-SS-7408453-0-2			
4	LIGHT BOARD ASSY	C-IA-5404311-0-0			
	RECEPTACLE	B-MD-5503954-0-0			
	ETCH BD	C-IA-5004310-0-0			
5	FAN HOUSING ASSY	E-AD-7005474-0-0			
	FAN HOUSING ASSY (PL)	A-PL-7005474-0-0			
	HOUSING FAN	D-MD-7406032-0-0			
	PANEL FRONT FAN	D-MD-7406030-0-0			
	COVER PROTECTION 4 TERM	B-MD-7404721-0-0			
	SCREEN FAN	C-MD-7405287-0-0			
	DECALS-FAN HOUSING	A-DC-7405287-0-0			
6.	FRONT DOOR ASSY (RH)	D-AD-7005361-2-0			
	FRONT DOOR ASSY (PL)	A-PL-7005361-2-0			
	FRONT DOOR	D-IA-7405877-0-0			
	HINGE PIN (TOP)	B-MD-7405865-0-0			
	DOOR SPACER (BOTTOM)	A-MD-7405312-0-0			
	HINGE PIN (BOTTOM)	B-MD-20400-8			
7.	CAB FRAME REWORK	E-IA-7406273-0-0			
8.	CAB FRAME ASSY 19-3/4	E-AD-7403864-0-0			
	CAB FRAME ASSY (PL)	A-PL-7403864-0-0			
	DRAWING INDEX CAB FRAME ASSY	D-DI-7403864-0-1			
9.	POWER CONN BRKT ASSY	D-AD-7005467-0-0			
	POWER CONN BRKT ASSY (PL)	A-PL-7005467-0-0			
	BRACKET, POWER CONN	D-MD-7406024-0-0			
	SCOTCHCAL BRAND FILM DECALS	A-SS-7406051-0-0			
10.	728 POWER SUPPLY (60 HZ)	D-MA-728-0-1			
	728 POWER SUPPLY (PL)	A-PL-728-0-1			
	728A POWER SUPPLY (50 HZ)	D-MA-728A-Ø-1			
	728A POWER SUPPLY (PL)	A-PL-728A-Ø-1			
11.	844 POWER CONTROL	D-UA-844-0-0			
	844 POWER CONTROL (PL)	A-PL-844-0-0			

MECHANICAL

FIND NO.	DESCRIPTION	PART NO.	PROD	CUST	F/C
12.	FULL DOOR ASSY (RH)	D-AD-7005358-2-0			
	FULL DOOR ASSY (RH) (PL)	A-PL-7005358-2-0			
	FULL DOOR	D-IA-7405741-0-0			
	HINGE PIN (TOP)	B-MD-20400-7			
	DOOR SPACER (BOTTOM)	A-MD-7405312-0-0			
	HINGE PIN (BOTTOM)	B-MD-20400-8			
13.	LOGIC FRAME ASSY	C-AD-7007136-0-0			
	LOGIC FRAME ASSY (PL)	A-PL-7007136-0-0			
	RIGHT END PANEL	C-MD-5302486-0-0			
	DECAL (CROBAR)	A-DC-7406255-0-0			
	RETAINER BLOCK	B-MD-7406047-0-0			
14.	MARGINAL CHK PANEL ASSY	C-MD-5402526-0-0			
	PANEL, MARGINAL CHK	C-MD-5302484-0-0			
	SCOTCHCALS	C-SS-10801			
15.	WIRED ASSY	D-AD-7007093-0-0			
	WIRED ASSY (PL)	A-PL-7007093-0-0			
	LOGIC FRAME DECALS	B-DC-5308753-2, 4,6,8,10&12			
16.	1943D MTG PANEL	D-AD-1943-D-Ø			
	1943D MTG PANEL (PL)	A-PL-1943-D-Ø			
17.	1943 CASTING	D-AD-5302483-0-0			
	1943 CASTING (PL)	A-PL-5302483-0-0			
18.	FAN HSG ASSY #7404880-0	E-MA-100285-1			
	FAN HSB ASSY #704880-0 (PL)	A-PL-100285-1			
	LOWER ENCLOSURE	C-MD-100285-1-0-1			
	END PLATE	D-MD-100285-1-0-5			
	TOP ENCLOSURE	E-MD-100285-1-0-3			
	FILTER SUPPORT	B-MD-100185-1-0-4			
	FAN SCREENING	C-MD-7404881-0-0			

ELECTRICAL

FIND NO.	DESCRIPTION	PART NO.	PROD	CUST	F/C
1.	SYNC MODEM INTERFACE (DS1Ø-A)	A-ML-DS1Ø-A			
	SYNC MODEM INTERFACE (DS1Ø-B)	A-ML-DS1Ø-B			
	SYNC MODEM INTERFACE (DS1Ø-C)	A-ML-DS1Ø-C			
	SYNC MODEM INTERFACE (DS1Ø-D)	A-ML-DS1Ø-D			
	WIRED ASSY (DS1Ø)	D-AD-7007093-0-0			
	WIRED ASSY PART LIST	A-PL-7007093-0-0			
	MODULE UTILIZATION	D-MU-DS1Ø-Ø-MU1			
	MODULE UTILIZATION	D-MU-DS1Ø-Ø-MU2			
	MODULE UTILIZATION	A-PL-DS1Ø-Ø-MU1			
	MODULE UTILIZATION	A-PL-DS1Ø-Ø-MU2			
	CONTROL LOGIC	D-BS-DS1Ø-Ø-CL1			
	CONTROL LOGIC	D-BS-DS1Ø-Ø-CL2			
	DATA BUFFER	D-BS-DS1Ø-Ø-DB			
	I/O BUS INTERFACE	D-BS-DS1Ø-Ø-IO1			
	I/O BUS INTERFACE	D-BS-DS1Ø-Ø-IO2			
	INDICATORS	D-BS-DS1Ø-Ø-INDC			
	JUMPER BOARDS	D-BS-DS1Ø-Ø-JB			
	RECEIVE BUFFER	D-BS-DS1Ø-Ø-RB			
	REC BIT PACK	D-BS-DS1Ø-Ø-RCW			
	REC LOGIC	D-BS-DS1Ø-Ø-RL1			
	REC LOGIC	D-BS-DS1Ø-Ø-RL2			
	RS. 232C INTERFACE	D-BS-DS1Ø-Ø-RS			
	TRANSMIT BUFFER	D-BS-DS1Ø-Ø-TB1			
	TRANSMIT BUFFER	D-BS-DS1Ø-Ø-TB2			
	TRANSMIT LOGIC	D-BS-DS1Ø-Ø-TL1			
	TRANSMIT LOGIC	D-BS-DS1Ø-Ø-TL2			
	I/O BUS INTERFACE	D-IC-DS1Ø-Ø-IOB			
	WIRE LIST (DS1Ø)	K-WL-DS1Ø-Ø-WI			
	POWER WIRING AC,DC (DS1Ø-A&B)	D-IC-DS1Ø-Ø-2			
	POWER WIRING AC,DC (DS1Ø-C&D)	D-IC-DS1Ø-Ø-3			
	DELAY SET UP PROC SPEC	A-SP-DS1Ø-Ø-DSP			
	MFG TEST PROC SPEC	A-SP-DS1Ø-Ø-MTP			
	PDP-10 SINGLE SYNCLINE UNIT SPEC	A-SP-DS1Ø-Ø-ES			
6.	LIGHT BOARD ASSY	C-IA-5404311-Ø-Ø			
	CIRCUIT SCHEMATIC	B-CS-5404311-Ø-1			
7.	FAN HOUSING ASSY	E-AD-7005474-0-0			
9.	PWR CONN BKT. ASSY	D-AD-7005467-0-0			
10.	CIRCUIT SCHEMATIC 728	B-728-0-1			
	CIRCUIT SCHEMATIC 728A	B-728A-Ø-1			
11.	CIRCUIT SCHEMATIC 844	B-CS-844-0-1			
14.	MTG PANEL 1943	B-CS-1943-0-1			
18.	FAN HSG ASSY	E-MA-100285-1			

FIND NO.	DESCRIPTION	PART NO.	PROD	CUST	F/C

REVISIONS: REV. | CHANGE NO. | CHK

FIRST USED ON OPTION/MODEL	DS1Ø
DRN. J. Cahill	DATE 9/28/70
CHK'D. D. Healy	DATE 10-16-70
ENG. U. Ku	DATE 11/04/70
PROJ. ENG. U. Ku	DATE 11/04/70
PROD. W.C. Hunt	DATE 11/5/70
NEXT HIGHER ASSY	A-ML-DS1Ø-A
SCALE	—
SHEET	2 OF 2

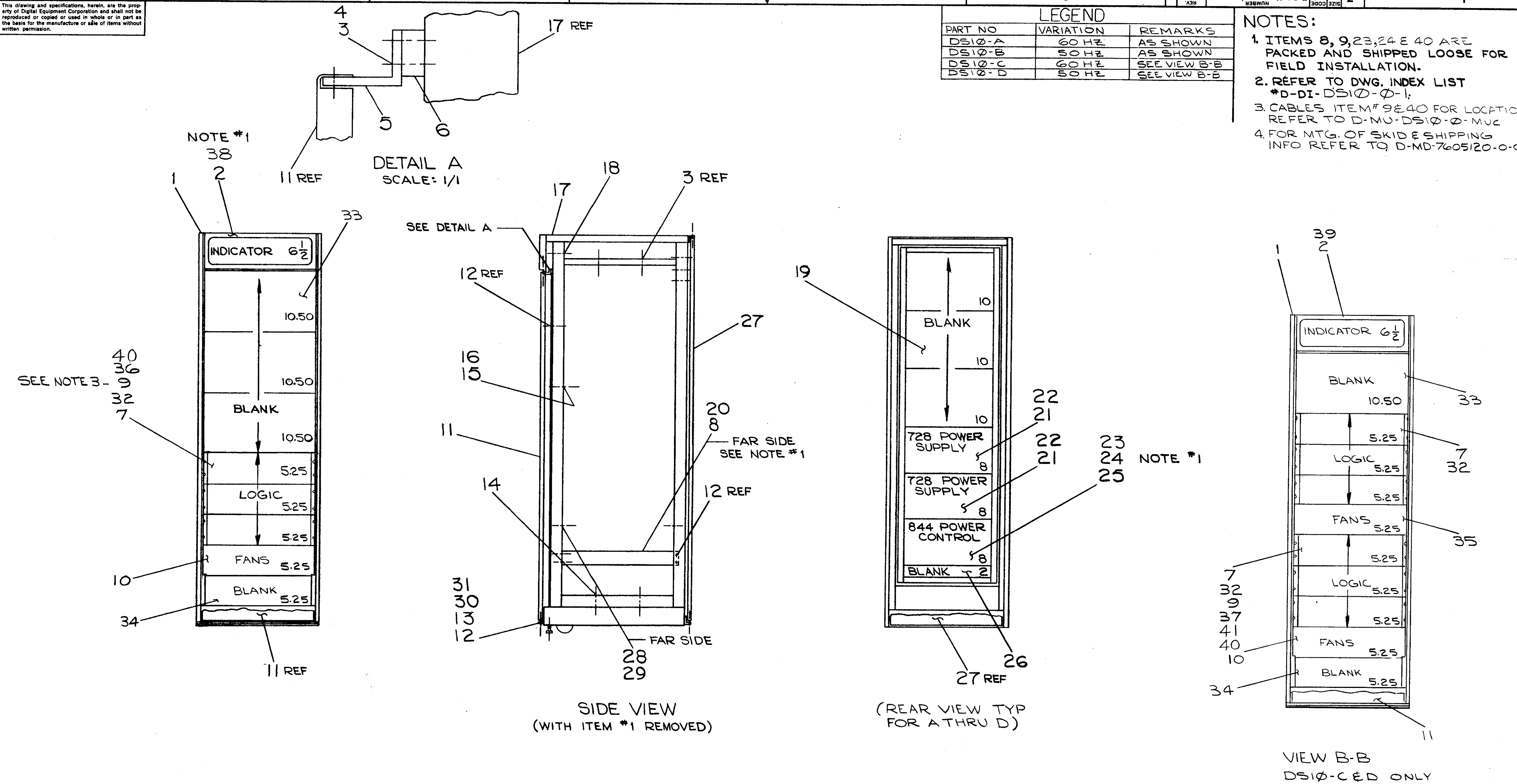
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DRAWING INDEX LIST (DS1Ø)

SIZE	CODE	NUMBER	REV
D	DI	DS1Ø-Ø-1	PO4

DIST.

DEC FORM NO. DRD 100



LEGEND

PART NO	VARIATION	REMARKS
DSIØ-A	60 HZ	AS SHOWN
DSIØ-B	50 HZ	AS SHOWN
DSIØ-C	60 HZ	SEE VIEW B-B
DSIØ-D	50 HZ	SEE VIEW B-B

NOTES:

1. ITEMS 8, 9, 23, 24 & 40 ARE PACKED AND SHIPPED LOOSE FOR FIELD INSTALLATION.
2. REFER TO DWG. INDEX LIST #D-DI-DSIØ-Ø-1.
3. CABLES ITEM # 9 & 40 FOR LOCATION REFER TO D-MU-DSIØ-Ø-MUC
4. FOR MTG. OF SKID & SHIPPING INFO REFER TO D-MD-7605120-0-0

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.008 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL
FINISH

DRN. DATE 9/30/70
CHKD. DATE 10/16/70
ENG. DATE
PROJ. ENG. DATE
PROD. DATE 11/3/70
FIRST USED ON D-DI-DSIØ-0-1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DSIØ ASSY, SYNC MODEM INTERFACE

SIZE D | CODE UA | NUMBER DSIØ-Ø-Ø | REV. A
SCALE 1/8 | SHEET 1 OF 1

REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 100

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY J. CAHILL — DATE 9/30/70
ENG U. Ku — DATE 11/04/70
CHECKED D. HEALY — DATE 10/9/70
PROD DC Healy — DATE 11/5/70
SECTION 1 — ISSUED SECT. 1

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	DS1Ø-A	DS1Ø-B	DS1Ø-C	DS1Ø-D
1	E-IA-7405092-0-0	PANEL, END	2	2	2	2
2	D-AD-7007098-0-0	ASSY BEZEL	1	1	1	1
3	9006350	SCR SOC HD CAP #10-32 x 1 LG	6	6	6	6
4	9007651	WASH LOCK EXT TOOTH #10	96	96	96	96
5	B-MD-7405861-0-0	BRACKET (DOOR PIVOT)	1	1	1	1
6	A-MD-7405860-0-0	SPACER	1	1	1	1
7	C-AD-7007136-0-0	LOGIC FRAME,ASSY (DS1Ø)	1	1	2	2
8	C-UA-BC10B-25-0	RMTE CONT MARGIN CHK CABLE	1	1	1	1
9	D-UA-BC10A-0-0	CABLE BC10A (LGTH SPEC BY ENG)	2	2	2	2
10	E-AD-7005474-0-0	FAN HOUSING ASSY	1	1	1	1
11	D-AD-7005361-2-0	FRONT DOOR R.H. (ASSY)	1	1	1	1
12	9006074-3	SCR PHL HD TRUSS #10-32 x .62 SST	94	94	94	94
13	D-MD-7405862-0-0	TRIM STRIP (BOTTOM)	1	1	1	1
14	9006346	SCR SOC HD CAP #10-32 x .50 SST	4	4	4	4
15	9007772-9	CABLE CLAMP #2C1-100 DAKOTA	4	4	4	4
16	9006075-2	SCR PHL HD FLAT #10-32 x .75 SST	4	4	4	4
17	E-IA-7406273-0-0	CABINET FRAME (REWORK)	1	1	1	1
18	9006083-1	SCR PHL HD PAN #10-32 x 2.50 SST	2	2	2	2
19	B-5111	CHASSIS (7402037)	3	3	2	2
20	D-AD-7005467-0-0	BRACKET POWER CONN. ASSY	1	1	1	1
21	D-MA-728-0-1	728 POWER SUPPLY	2	0	2	0
22	D-MA-728A-0-1	728A POWER SUPPLY	0	2	0	2

TITLE: DS1Ø ASSY, SYNC MODEM INTERFACE
ASSY NO. D-UA-DS1Ø-Ø-Ø — SHEET 1 OF 2
SIZE A — CODE PL — NUMBER DS1Ø-Ø-Ø — REV. POO — ECO NO.
DIST.

DEC FORM NO.16-1031
DRA 110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY J. CAHILL — DATE 9/30/70
ENG U. Ku — DATE 11/04/70
CHECKED D. HEALY — DATE 10/12/70
PROD DC Healy — DATE 11/5/70
SECTION 1 — ISSUED SECT. 1

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	DS1Ø-A	DS1Ø-B	DS1Ø-C	DS1Ø-D
23	1202980	CORD, EXT 25 FEET	1	1	1	1
24	C-AD-7005128-0-0	25' POWER CORD	1	1	1	1
25	D-UA-844-0-0	844 POWER CONTROL	1	1	1	1
26	B-MD-5111	CHASSIS (7402033)	1	1	1	1
27	D-AD-7005358-2-0	FULL DOOR R.H. ASSY 19 .750 CAB	1	1	1	1
28	9007082	CLAMP #NPC -5 HOLOB IND	5	5	5	5
29	9006073-1	SCR PHL HD # 10-32 x .500 LG SST	5	5	5	5
30	9006020-1	SCR PHL HD PAN #6-32 x .250 LG SST	4	4	4	4
31	9007649	WASHER EXT. TOOTH #6	4	4	4	4
32	D-MU-DS01-0-MU1 D-MU-DS01-0-MU2	MODULE UTILIZATION (DS1Ø)	REF	REF	REF	REF
33	B-MD-5100	BLANK PANEL (7402027)	3	3	1	1
34	B-MD-5100	BLANK PANEL (7402016)	1	1	1	1
35	E-MA-100285-1	FAN HSG ASSY (7404880-0)	0	0	1	1
36	D-IC-DS10-0-2	WIRING AC DC (DS10 A&B)	REF	REF	-	-
37	D-IC- DS10-0-3	WIRING AC DC (DS10 C&D	-	-	REF	REF
38	D-AD-7007148-1-0	CABLE SET(DS1Ø -A&B)	1	1	0	0
39	D-AD-7007148-2-0	CABLE SET (DS10-C&D)	0	0	1	1
40	D-UA-BCØ1R-25-Ø	CABLE CARD ASSY (BCØ1R)	1	1	2	2
41	D-UA-BC1ØA-5-Ø	CABLE BC1ØA 5 FT LONG	Ø	Ø	2	2

TITLE: DS1Ø ASSY, SYNC MODEM INTERFACE
ASSY NO. D-UA-DS1Ø-Ø-Ø — SHEET 2 OF 2
SIZE A — CODE PL — NUMBER DS1Ø-Ø-Ø — REV. POO — ECO NO.
DIST.

DEC FORM NO.16-1031
DRA 110

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-DS1Ø-A-Ø		1	SYNC MODEM INTERFACE (DS10-A)
A-PL-DS1Ø-A-Ø		1	SYNC MODEM INTERFACE (DS10-A) P.L.
D-DI-DS1Ø-0-1		1	DRAWING INDEX LIST (DS1Ø)
D-AD-7ØØ7Ø93-Ø-Ø		1	WIRED ASSY (DS1Ø)
A-PL-7ØØ7Ø93-Ø-Ø		1	WIRED ASSY PART LIST (DS1Ø)
D-MU-DS1Ø-Ø-MU1		1	MODULE UTILIZATION
D-MU-DS1Ø-Ø-MU2		1	MODULE UTILIZATION
A-PL-DS1Ø-Ø-MU1		1	MODULE UTILIZATION
A-PL-DS1Ø-Ø-MU2		1	MODULE UTILIZATION
D-BS-DS1Ø-Ø-CL1		1	CONTROL LOGIC
D-BS-DS1Ø-Ø-CL2		1	CONTROL LOGIC
D-BS-DS1Ø-Ø-DB		1	DATA BUFFER
D-BS-DS1Ø-Ø-IO1		1	I/O BUS INTERFACE
D-BS-DS1Ø-Ø-IO2		1	I/O BUS INTERFACE
D-BS-DS1Ø-ØINDC		1	INDICATORS
D-BS-DS1Ø-Ø-JB		1	JUMPER BOARDS
D-BS-DS1Ø-Ø-RB		1	RECEIVER BUFFER
D-BS-DS1Ø-Ø-RCW		1	REC BIT PACK
D-BS-DS1Ø-Ø-RL1		1	REC LOGIC
D-BS-DS1Ø-Ø-RL2		1	REC LOGIC
D-BS-DS1Ø-Ø-RS		1	RS 232 C INTERFACE
D-BS-DS1Ø-Ø-TB1		1	TRANSMIT BUFFER
D-BS-DS1Ø-Ø-TB2		1	TRANSMIT BUFFER
D-BS-DS1Ø-Ø-TL1		1	TRANSMIT LOGIC
D-BS-DS1Ø-Ø-TL2		1	TRANSMIT LOGIC
D-IC-DS1Ø-Ø-IOB		1	I/O BUS INTERFACE
K-WL-DS1Ø-Ø-WL		1	WIRE LIST (DS1Ø)
D-IC-DS1Ø-Ø-2		1	AC/ DC PWR WIRING (DS1Ø-AB)

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. AKIBOT DATE 10/1/70
CHK'D. W.A.S. DATE 10/17/70
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
FIRST USED ON DS1Ø
SCALE
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE SYNC MODEM INTERFACE DS1Ø-A 60 HZ

SIZE A CODE ML NUMBER DS1Ø-A REV.

DIST.

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DEC FORM NO.16-1033 DRA 103

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
A-SP-DS1Ø-Ø-DSP		4	DS1Ø DELAY SET UP PROCEDURE SPEC
A-SP-DS1Ø-Ø-MTP		4	DS1Ø MFG TEST PROCEDURE AND SPEC
A-SP-DS1Ø-Ø-ES		4	PDP-1Ø SINGLE SYNC LINE UNIT (DS1Ø) SPEC

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. A. KIBORT DATE 10/1/70
CHK'D. W.A.S. DATE 10/17/70
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
FIRST USED ON DS1Ø
SCALE
SHEET 2 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE SYNC MODEM INTERFACE DS1Ø-A 60 HZ

SIZE A CODE ML NUMBER DS1Ø-A REV.

DIST.

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DEC FORM NO.16-1033 DRA 103

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-DS1Ø-B-Ø		1	SYNC MODEM INTERFACE (DS10-B)
A-PL-DS1Ø-B-Ø		1	SYNC MODEM INTERFACE P.L. (DS10-B)
D-DI-DS1Ø-Ø-1		1	DRAWING INDEX LIST (DS1Ø)
D-AD-7007093-Ø-Ø		1	WIRED ASSY (DS1Ø)
A-PL-7ØØ7Ø93-Ø-Ø		1	WIRED ASSY PART LIST (DS1Ø)
D-MU-DS1Ø-Ø-MU1		1	MODULE UTILIZATION
D-MU-DS1Ø-Ø-MU2		1	MODULE UTILIZATION
A-PL-DS1Ø-Ø-MU1		1	MODULE UTILIZATION
A-PL-DS1Ø-Ø-MU2		1	MODULE UTILIZATION
D-BS-DS1Ø-Ø-CL1		1	CONTROL LOGIC
D-BS-DS1Ø-Ø-CL2		1	CONTROL LOGIC
D-BS-DS1Ø-Ø-DB		1	DATA BUFFER
D-BS-DS1Ø-Ø-IO1		1	I/O BUS INTERFACE
D-BS-DS1Ø-Ø-IO2		1	I/O BUS INTERFACE
D-BS-DS1Ø-Ø-INDC		1	INDICATORS
D-BS-DS1Ø-Ø-JB		1	JUMPER BOARDS
D-BS-DS1Ø-Ø-RB		1	RECEIVER BUFFER
D-BS-DS1Ø-Ø-RCW		1	REC BIT PACK
D-BS-DS1Ø-Ø-RL1		1	REC LOGIC
D-BS-DS1Ø-Ø-RL2		1	REC LOGIC
D-BS-DS1Ø-Ø-RS		1	RS 232 C INTERFACE
D-BS-DS1Ø-Ø-TB1		1	TRANSMIT BUFFER
D-BS-DS1Ø-Ø-TB2		1	TRANSMIT BUFFER
D-BS-DS1Ø-Ø-TL1		1	TRANSMIT LOGIC
D-BS-DS1Ø-Ø-TL2		1	TRANSMIT LOGIC
D-IC-DS1Ø-Ø-IOB		1	I/O BUS INTERFACE
K-WL-DS1Ø-Ø-WL		1	WIRE LIST (DS1Ø)
D-IC-DS1Ø-Ø-2		1	AC, DC PWR WIRING (DS1Ø-AB)

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. A. KIBOT DATE 10/1/70
CHK'D. W.A.S. DATE 10/12/70
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
FIRST USED ON DS1Ø
SCALE
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE SYNC MODEM INTERFACE DS1Ø-B 50 HZ

SIZE A CODE ML NUMBER DS1Ø-B REV.

DIST.

DEC FORM NO.16-1033 DRA 103

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
A-SP-DS1Ø-Ø-DSP		4	DS1Ø DELAY SET UP PROCEDURE SPEC
A-SP-DS1Ø-Ø-MTP		4	DS1Ø MEG TEST PROCEDURE AND SPEC
A-SP-DS1Ø-Ø-ES		24	PDP-1Ø SINGLE SYNC LINE UNIT (DS1Ø) SPEC

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. A. KIBORT DATE 10/1 70
CHK'D. W.A.S. DATE 10/12/70
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
FIRST USED ON DS1Ø
SCALE
SHEET 2 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE SYNC MODEM INTERFACE DS1Ø-B 50 HZ

SIZE A CODE ML NUMBER DS1Ø-B REV.

DIST.

DEC FORM NO.16-1033 DRA 103

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-DS1Ø-C-Ø		1	SYNC MODEM INTERFACE (DS1Ø-C)
A-PL-DS1Ø-C-Ø		1	SYNC MODEM INTERFACE (DS1Ø-C) (P.L.)
D-DI-DS1Ø-Ø-1		1	DRAWING INDEX LIST (DS1Ø)
D-AD-7ØØ7Ø93-Ø-Ø		1	WIRED ASSY (DS1Ø)
A-PL-7ØØ7Ø93-Ø-Ø		1	WIRES ASSY PART LIST (DS1Ø)
D-MU-DS1Ø-Ø-MU1		1	MODULE UTILIZATION
D-MU DS1Ø-Ø-MU2		1	MODULE UTILIZATION
A-PL-DS1Ø-Ø-MU1		1	MODULE UTILIZATION
A-PL-DS1Ø-Ø-MU2		1	MODULE UTILIZATION
D-BS-DS1Ø-Ø-CL1		1	CONTROL LOGIC
D-BS-DS1Ø-Ø-CL2		1	CONTROL LOGIC
D-BS-DS1Ø-Ø-DB		1	DATA BUFFER
D-BS-DS1Ø-Ø-IO1		1	I/O BUS INTERFACE
D-BS-DS1Ø-Ø-IO2		1	I/O BUS INTERFACE
D-BS-DS1Ø-Ø-INDC		1	INDICATORS
D-BS-DS1Ø-Ø-JB		1	JUMPERS BOARDS
D-BS-DS1Ø-Ø-RB		1	RECEIVE BUFFER
D-BS-DS1Ø-Ø-RCW		1	REC BIT PACK
D-BS-DS1Ø-Ø-RL1		1	REC LOGIC
D-BS-DS1Ø-Ø-RL2		1	REC LOGIC
D-BS-DS1Ø-Ø-RS		1	RS 232 C INTERFACE
D-BS-DS1Ø-Ø-TB1		1	TRANSMIT BUFFER
D-BS-DS1Ø-Ø-TB2		1	TRANSMIT BUFFER
D-BS-DS1Ø-Ø-TL1		1	TRANSMIT LOGIC
D-BS-DS1Ø-Ø-TL2		1	TRANSMIT LOGIC
D-IC-DS1Ø-Ø-IOB		1	I/O BUS INTERFACE
K-WL-DS1Ø-Ø-WL		1	WIRE LIST (DS1Ø)
D-IC-DS1Ø-Ø-3		1	A C/DC PWR WIRING (DS1Ø-CD)

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. A. KIBOT — DATE 10/1/70
CHK'D. W.A.S. — DATE 10/12/70
ENG. — DATE
PROJ. ENG. — DATE
PROD. — DATE
FIRST USED ON DS1Ø
SCALE
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE SYNC MODEM INTERFACE DS1Ø-C 60 HZ

SIZE A — CODE ML — NUMBER DS1Ø-C — REV.

DIST.

DEC FORM NO.16–1033
DRA 103

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
A-SP-DS1Ø-Ø-DSP		4	DS1Ø DELAY SET UP PROCEDURE SPEC
A-SP-DS1Ø-Ø-MTP		4	DS1Ø MFG TEST PROCEDURE AND SPEC
A-SP-DS1Ø-Ø-ES		24	PDP-1Ø SINGLE SYNC LINE UNIT (DS1Ø) SPEC

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. A. KIBORT — DATE 10/1/70
CHK'D. W.A.S. — DATE 10/17/70
ENG. — DATE
PROJ. ENG. — DATE
PROD. — DATE
FIRST USED ON DS1Ø
SCALE
SHEET 2 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE SYNC MODEM INTERFACE DS1Ø-C 60 HZ

SIZE A — CODE ML — NUMBER DS1Ø-C — REV.

DIST.

DEC FORM NO.16–1033
DRA 103

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-DS1Ø-D-Ø		1	SYNC MODEM INTERFACE DS1Ø-D
A-PL-DS1Ø-D-Ø		1	SYNC MODEM INTERFACE DS1Ø-D P.L.
D-DI-DS1Ø-Ø-1		1	DRAWING INDEX LIST (DS1Ø)
D-AD-7ØØ7Ø93-Ø-Ø		1	WIRED ASSY (DS10)
A-PL-7ØØ7Ø93-Ø-Ø		1	WIRED ASSY PART LIST (DS1Ø)
D-MU-DS1Ø-Ø-MU1		1	MODULE UTILIZATION
D-MU-DS1Ø-Ø-MU2		1	MODULE UTILIZATION
A-PL-DS1Ø-Ø-MU1		1	MODULE UTILIZATION
A-PL-DS1Ø-Ø-MU2		1	MODULE UTILIZATION
D-BS-DS1Ø-Ø-CL1		1	CONTROL LOGIC
D-BS-DS1Ø-Ø-CL2		1	CONTROL LOGIC
D-BS-DS1Ø-Ø-DB		1	DATA BUFFER
D-BS-DS1Ø-Ø-IO1		1	I/O BUS INTERFACE
D-BS-DS1Ø-Ø-IO2		1	I/O BUS INTERFACE
D-BS-DS1Ø-Ø-INDC		1	INDICATORS
D-BS-DS1Ø-Ø-JB		1	JUMPER BOARDS
D-BS-DS1Ø-Ø-RB		1	RECEIVE BUFFER
D-BS-DS1Ø-Ø-RCW		1	REC BIT PACK
D-BS-DS1Ø-Ø-RL1		1	REC LOGIC
D-BS-DS1Ø-Ø-RL2		1	REC LOGIC
D-BS-DS1Ø-Ø-RS		1	RS 232 C INTERFACE
D-BS-DS1Ø-Ø-TB1		1	TRANSMIT BUFFER
D-BS-DS1Ø-Ø-TB2		1	TRANSMIT BUFFER
D-BS-DS1Ø-Ø-TL1		1	TRANSMIT LOGIC
D-BS-DS1Ø-Ø-TL2		1	TRANSMIT LOGIC
D-IC-DS1Ø-Ø- IOB		1	I/O BUS INTERFACE
K-WL-DS1Ø-Ø-WL		1	WIRE LIST (DS1Ø)
D-IC-DS1Ø-Ø-3		1	AC/DC PWR WIRING (DS1Ø-CD)

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. A. KIBOT — DATE 10/1 7[illegible]
CHK'D W.A.S. — DATE 10/12/70
ENG. — DATE
PROJ. ENG. — DATE
PROD. — DATE
FIRST USED ON DS1Ø
SCALE
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE SYNC MODEM INTERFACE DS1Ø-D 50 HZ

SIZE	CODE	NUMBER	REV.
A	ML	DS1Ø-D	

DIST.

DEC FORM NO.16-1033
DRA 103

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MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
A-SP-DS1Ø-Ø-DSP		4	DS1Ø DELAY SET UP PROCEDURE SPEC
A-SP-DS1Ø-Ø-MTP		4	DS1Ø MFG TEST PROCEDURE AND SPEC
A-SP-DS1Ø-Ø-ES		24	PDP-1Ø SINGLE SYNC LINE UNIT (DS1Ø) SPEC

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. A. KIBORT — DATE 10/1/7[illegible]
CHK'D. W.A.S. — DATE 10/17/70
ENG. — DATE
PROJ. ENG. — DATE
PROD. — DATE
FIRST USED ON DS1Ø
SCALE
SHEET 2 OF 2

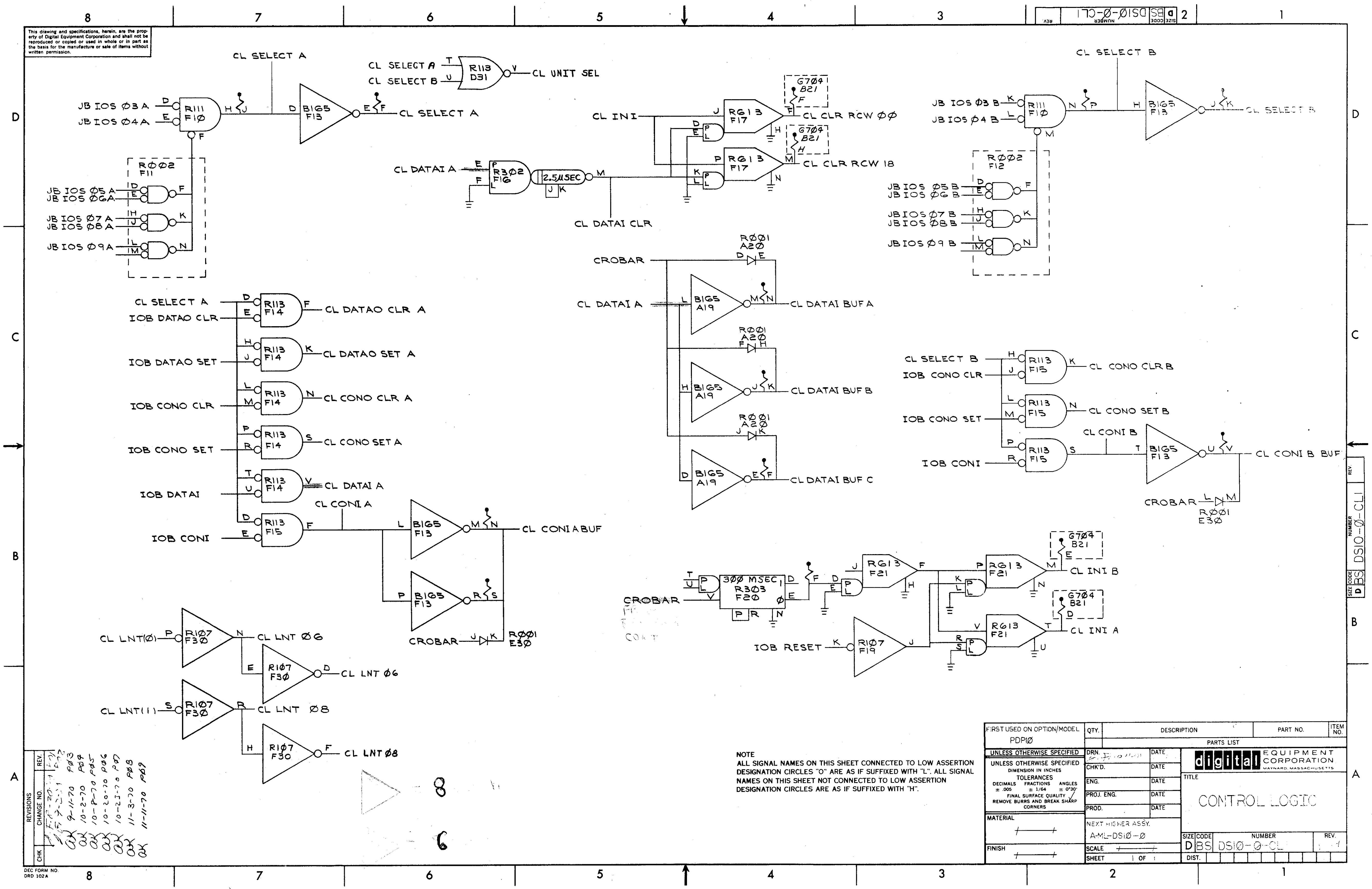
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE SYNC MODEM INTERFACE DS1Ø-D 5Ø HZ

SIZE	CODE	NUMBER	REV.
A	ML	DS1Ø-D	

DIST.

DEC FORM NO.16-1033
DRA 103



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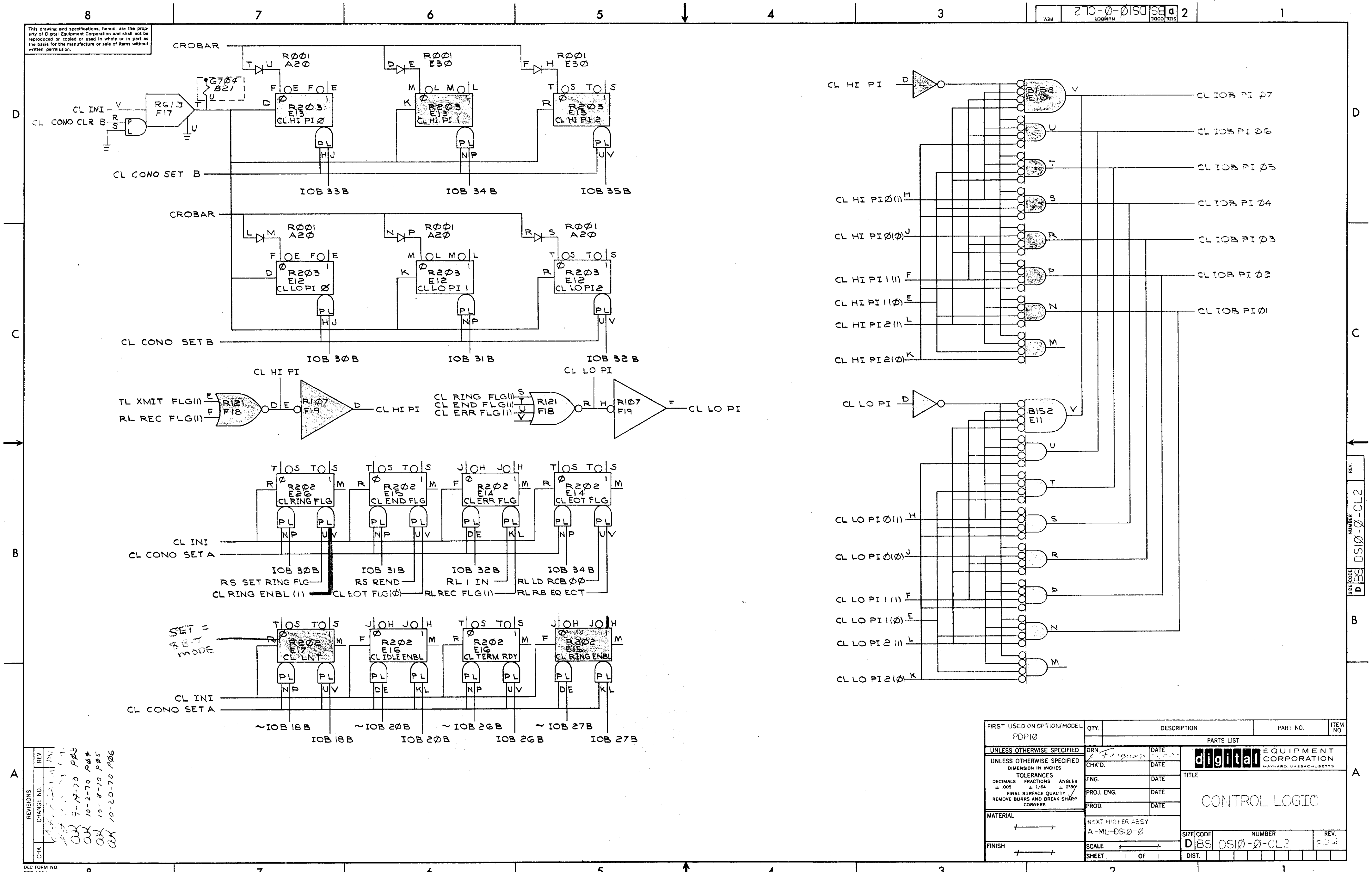
CL SELECT A
JB IOS Ø3 A
JB IOS Ø4 A
R111 F1Ø
B165 F13
CL SELECT A
R002 F11
JB IOS Ø5 A
JB IOS Ø6 A
JB IOS Ø7 A
JB IOS Ø8 A
JB IOS Ø9 A
CL SELECT A
CL SELECT B
R113 D31
CL UNIT SEL
CL DATAI A
R302 F16
2.5μSEC
CL DATAI CLR
CL INI
RG13 F17
G7Ø4 B21
CL CLR RCW ØØ
CL CLR RCW 18
CL SELECT B
JB IOS Ø3 B
JB IOS Ø4 B
R111 F1Ø
B165 F13
CL SELECT B
RØØ2 F12
JB IOS Ø5 B
JB IOS Ø6 B
JB IOS Ø7 B
JB IOS Ø8 B
JB IOS Ø9 B
CL SELECT A
IOB DATAO CLR
R113 F14
CL DATAO CLR A
IOB DATAO SET
CL DATAO SET A
IOB CONO CLR
CL CONO CLR A
IOB CONO SET
CL CONO SET A
IOB DATAI
CL DATAI A
IOB CONI
R113 F15
CL CONI A
B165 F13
CL CONI A BUF
CROBAR
RØØ1 E3Ø
CROBAR
RØØ1 A2Ø
CL DATAI A
B165 A19
CL DATAI BUF A
CL DATAI BUF B
CL DATAI BUF C
CL SELECT B
IOB CONO CLR
R113 F15
CL CONO CLR B
IOB CONO SET
CL CONO SET B
CL CONI B
IOB CONI
B165 F13
CL CONI B BUF
CROBAR
RØØ1 E3Ø
CL LNT(Ø)
R107 F3Ø
CL LNT Ø6
CL LNT Ø6
CL LNT(1)
CL LNT Ø8
CL LNT Ø8
CROBAR
300 MSEC R303 F20
RG13 F21
G7Ø4 B21
CL INI B
CL INI A
IOB RESET
R107 F19
NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".
FIRST USED ON OPTION/MODEL
PDP1Ø
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
QTY. DESCRIPTION PART NO. ITEM NO.
PARTS LIST
DRN. CHK'D. ENG. PROJ. ENG. PROD. DATE
NEXT HIGHER ASSY. A-ML-DSIØ-Ø
SCALE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE
CONTROL LOGIC
SIZE D CODE BS NUMBER DSIØ-Ø-CL REV.
DIST.
REVISIONS
DEC FORM NO. DRD 102A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CROBAR
CL INI
CL CONO CLR B
RG13 F17
G704 B21
R001 A20
R001 E30
R203 E13 CL HI PI Ø
R203 E13 CL HI PI 1
R203 E13 CL HI PI 2
CL CONO SET B
IOB 33B
IOB 34 B
IOB 35B
R203 E12 CL LO PI Ø
R203 E12 CL LO PI 1
R203 E12 CL LO PI2
IOB 30 B
IOB 31 B
IOB 32 B
CL HI PI
TL XMIT FLG(1)
RL REC FLG(1)
R121 F18
R107 F19
CL LO PI
CL RING FLG(1)
CL END FLG(1)
CL ERR FLG(1)
R202 E26 CL RING FLG
R202 E15 CL END FLG
R202 E14 CL ERR FLG
R202 E14 CL EOT FLG
CL CONO SET A
IOB 3ØB
IOB 31B
IOB 32B
IOB 34 B
RS SET RING FLG
RS REND
RL I IN
RL LD RCB ØØ
CL RING ENBL (1)
CL EOT FLG(Ø)
RL REC FLG(1)
RL RB EQ ECT
SET = 8 BIT MODE
R202 E17 CL LNT
R202 E16 CL IDLE ENBL
R202 E16 CL TERM RDY
R202 E15 CL RING ENBL
~IOB 18 B
~IOB 2Ø B
~IOB 26 B
~IOB 27 B
IOB 18B
IOB 2ØB
IOB 26 B
IOB 27 B
B152 E10
B152 E11
CL HI PIØ(1)
CL HI PIØ(Ø)
CL HI PI 1 (1)
CL HI PI 1 (Ø)
CL HI PI 2 (1)
CL HI PI 2 (Ø)
CL LO PI Ø (1)
CL LO PI Ø (Ø)
CL LO PI 1 (1)
CL LO PI 1 (Ø)
CL LO PI 2 (1)
CL LO PI 2 (Ø)
CL IOB PI Ø7
CL IOB PI Ø6
CL IOB PI Ø5
CL IOB PI Ø4
CL IOB PI Ø3
CL IOB PI Ø2
CL IOB PI Ø1
FIRST USED ON OPTION/MODEL
PDP1Ø
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
DRN.
CHK'D.
ENG.
PROJ. ENG.
PROD.
DATE
NEXT HIGHER ASSY
A-ML-DSIØ-Ø
SCALE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE
CONTROL LOGIC
SIZE CODE NUMBER REV.
D BS DSIØ-Ø-CL2
DIST.
REVISIONS
CHANGE NO
REV
CHK
DEC FORM NO DRD 102A

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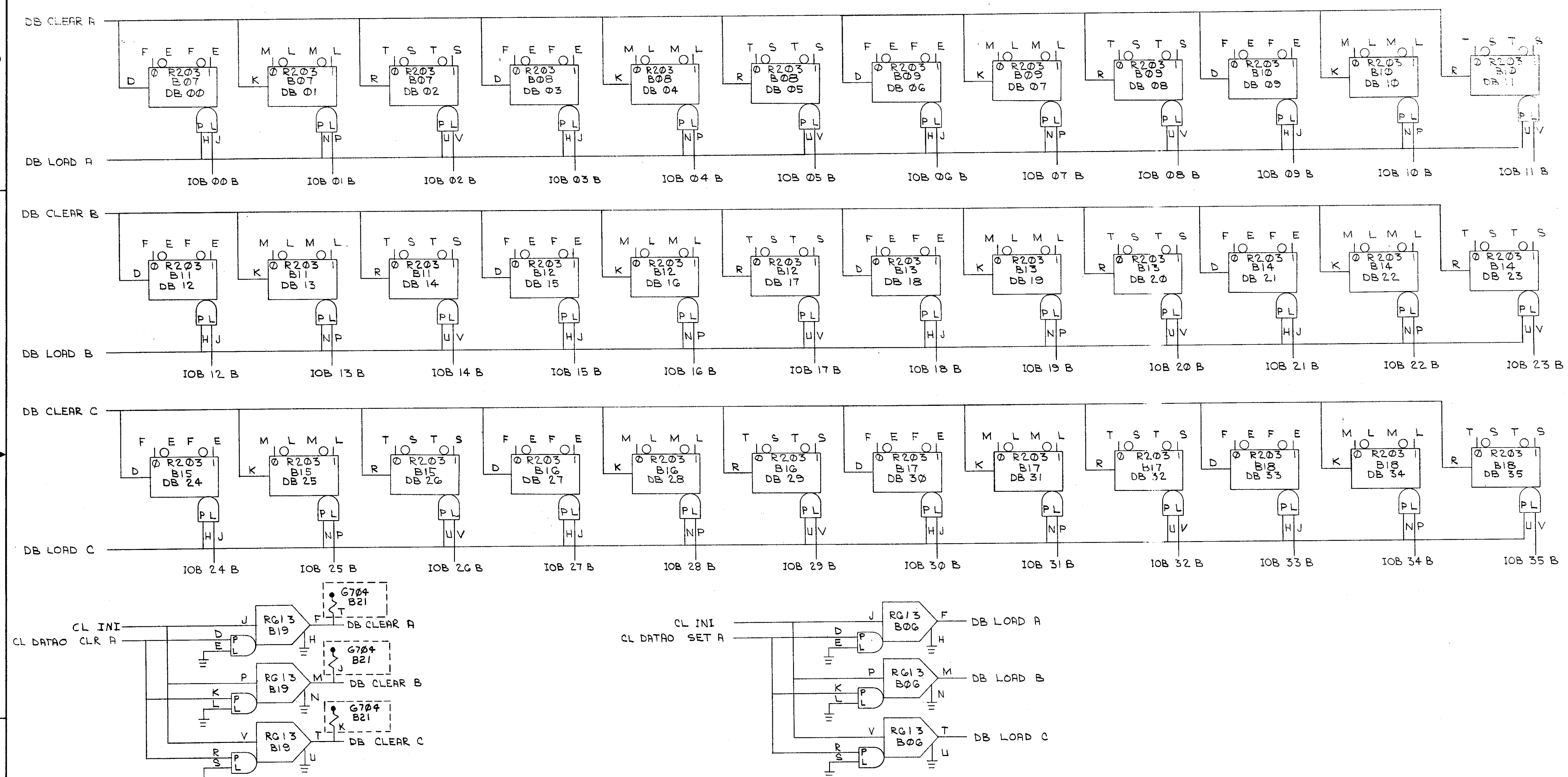


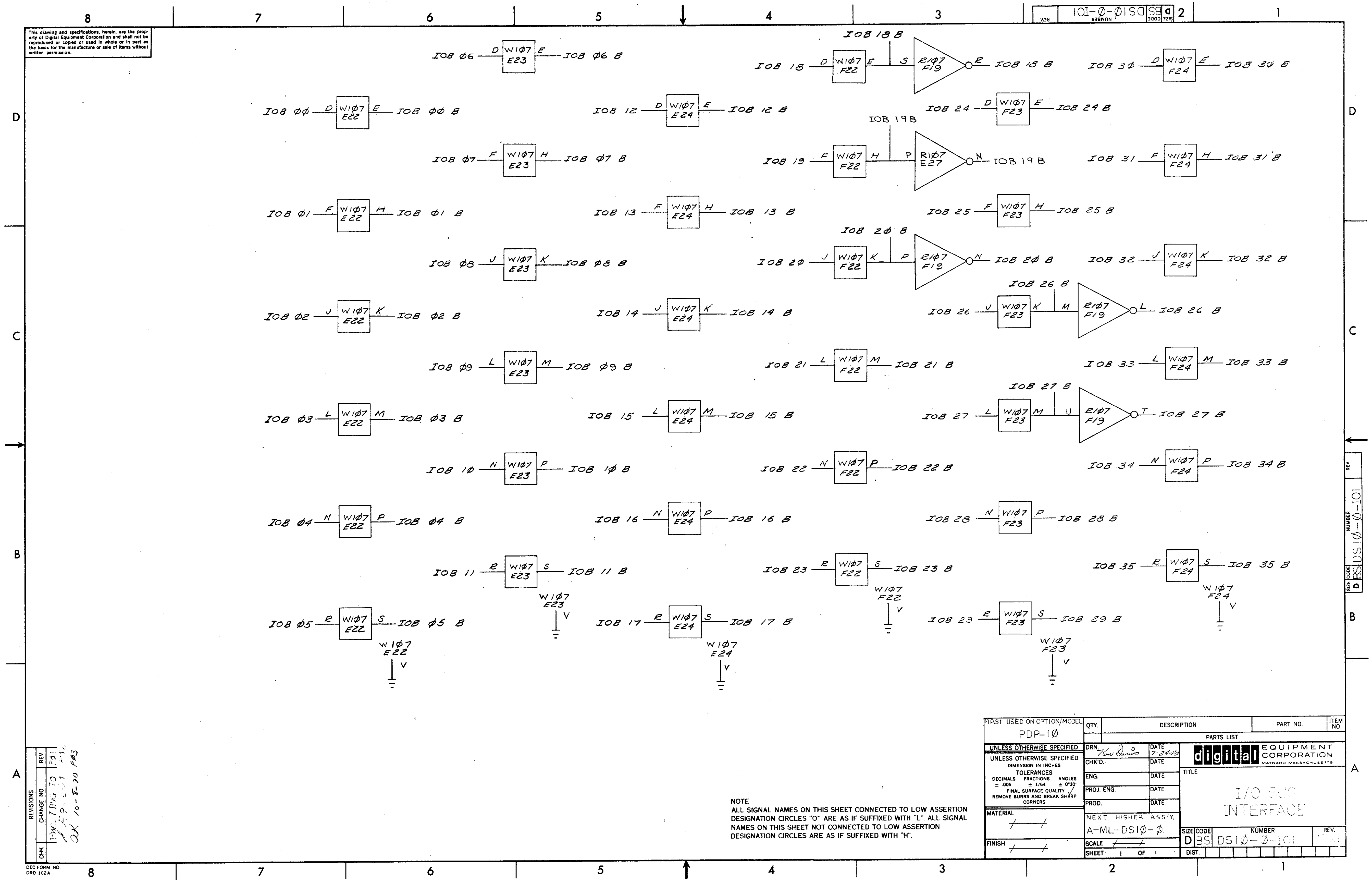
NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".

REVISIONS		
CHK	CHANGE NO.	REV.
	7 AUG 70	F01
	10-5-70	F02
	10-20-70	F03

FIRST USED ON OPTION/MODEL	PDP-10
UNLESS OTHERWISE SPECIFIED	DIMENSION IN INCHES; TOLERANCES: DECIMALS ± .005, FRACTIONS ± 1/64, ANGLES ± 0°30'; FINAL SURFACE QUALITY; REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL	—/—
FINISH	—/—
DRN.	DATE 16 JULY 70
CHK'D.	DATE
ENG.	DATE
PROJ. ENG.	DATE
PROD.	DATE
NEXT HIGHER ASSEMBLY	A-ML-DS10-0
SCALE	NONE
SHEET	1 OF 1
TITLE	DATA BUFFER
SIZE	D
CODE	BS
NUMBER	DS10-0-DB

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DEC FORM NO. DRD 102A



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NOTE
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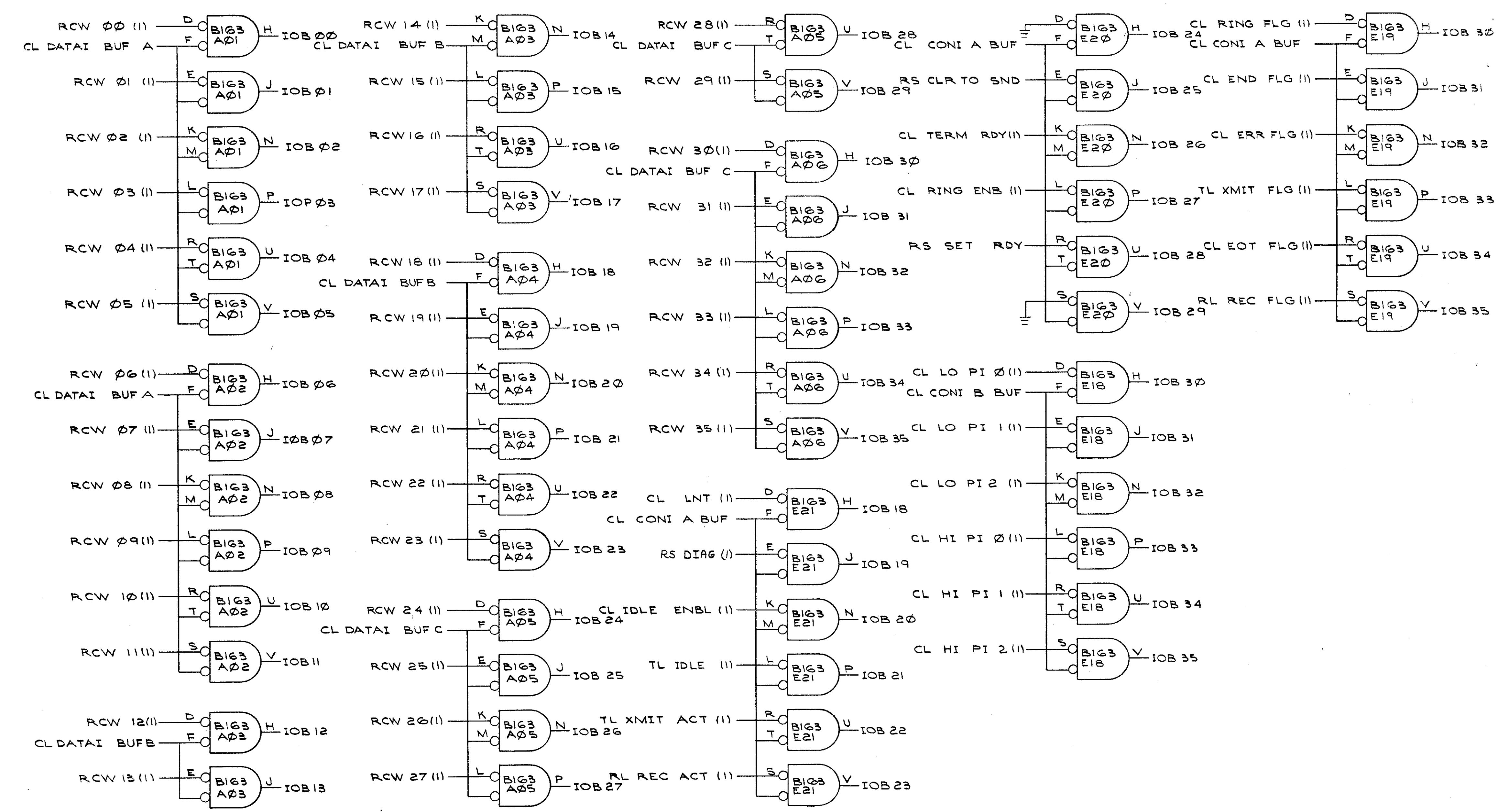
FIRST USED ON OPTION/MODEL PDP-10
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
TITLE I/O BUS INTERFACE
NEXT HIGHER ASS'Y. A-ML-DS10-0
SIZE D CODE BS NUMBER DS10-0-101
SHEET 1 OF 1
DEC FORM NO. DRD 102A



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FIRST USED ON OPTION/MODEL PDP1Ø

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

NEXT HIGHER ASS'Y A-ML-DS1Ø-Ø

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE I/O BUS

SIZE D CODE BS NUMBER DS1Ø-Ø-IO2

SHEET 1 OF 1

DEC FORM NO. DRD 102A

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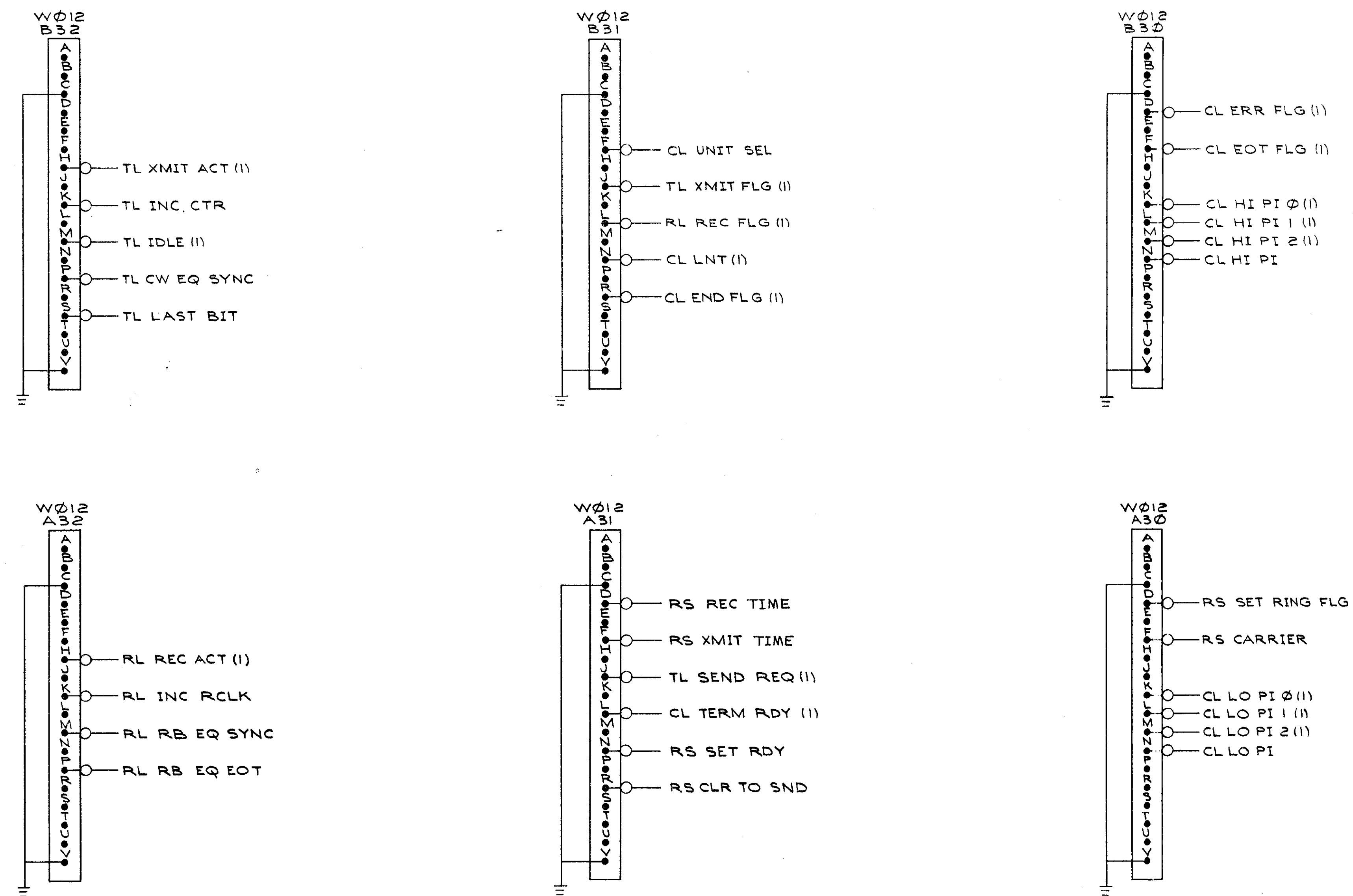


FIRST USED ON OPTION/MODEL: PDP1∅

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

DRN. / CHK'D. / ENG. / PROJ. ENG. / PROD. / DATE

NEXT HIGHER ASSY. A-ML-DSI∅-∅

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

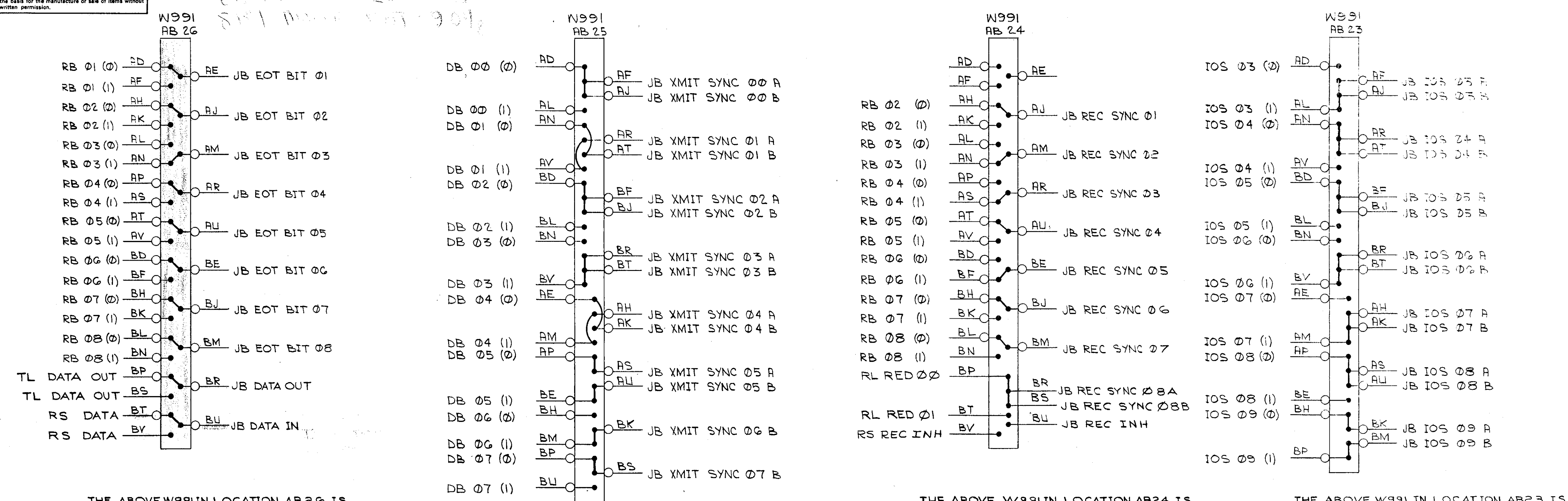
TITLE: INDICATORS

SIZE D CODE BS NUMBER DSI∅-∅-INDC REV.

SCALE — SHEET 1 OF 1

REVISIONS: REV. / CHANGE NO. / CHK

DEC FORM NO. DRD 102A



THE ABOVE W991 IN LOCATION AB26 IS JUMPERED FOR THE FOLLOWING EOT CHARACTER

6 BIT MODE = Ø4
8 BIT MODE = ØØ4

JB EOT BIT Ø8 IS THE MSB

JB DATA OUT - IS JUMPERED FOR CONVENTIONAL POLARITY MODEMS

JB DATA IN - IS JUMPERED FOR CONVENTIONAL POLARITY MODEMS

THE ABOVE W991 IN LOCATION AB25 IS JUMPERED FOR THE FOLLOWING XMIT SYNC CODES

6 BIT MODE = 26_8 (XMIT SYNC A)
8 BIT MODE = ~~Ø26~~ $_8$ (XMIT SYNC B)

JB XMIT SYNC ØØ IS THE MSB

THE ABOVE W991 IN LOCATION AB24 IS JUMPERED FOR THE FOLLOWING REC SYNC CODES

6 BIT MODE = 26_8
8 BIT MODE = $Ø26_8$

JB REC SYNC Ø8A IS MSB FOR 6 BIT MODE
JB REC SYNC Ø8B IS MSB FOR 8 BIT MODE
JB REC SYNC Ø7 APPLIES TO 8 BIT MODE ONLY
JB REC SYNC Ø6 APPLIES TO 8 BIT MODE ONLY
JB REC INH - IS ONLY JUMPERED FOR HALF DUPLEX OPERATION.

THE ABOVE W991 IN LOCATION AB23 IS JUMPERED FOR DEVICE CODES 46Ø AND 464

JB IOS Ø3 IS MSB

NOTE
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FIRST USED ON OPTION/MODEL: PDP-1Ø

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES: DECIMALS ± .005, FRACTIONS ± 1/64, ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL: -/-
FINISH: -/-

DRN: [signature] DATE: 12 AUG 70

digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: JUMPER BOARDS

NEXT HIGHER ASSEMBLY: A-ML-DSIØ-Ø

SIZE D, CODE BS, NUMBER DSIØ-Ø-JB, REV. FØ1

SCALE NONE, SHEET 1 OF 1

DEC FORM NO. DRD 102A

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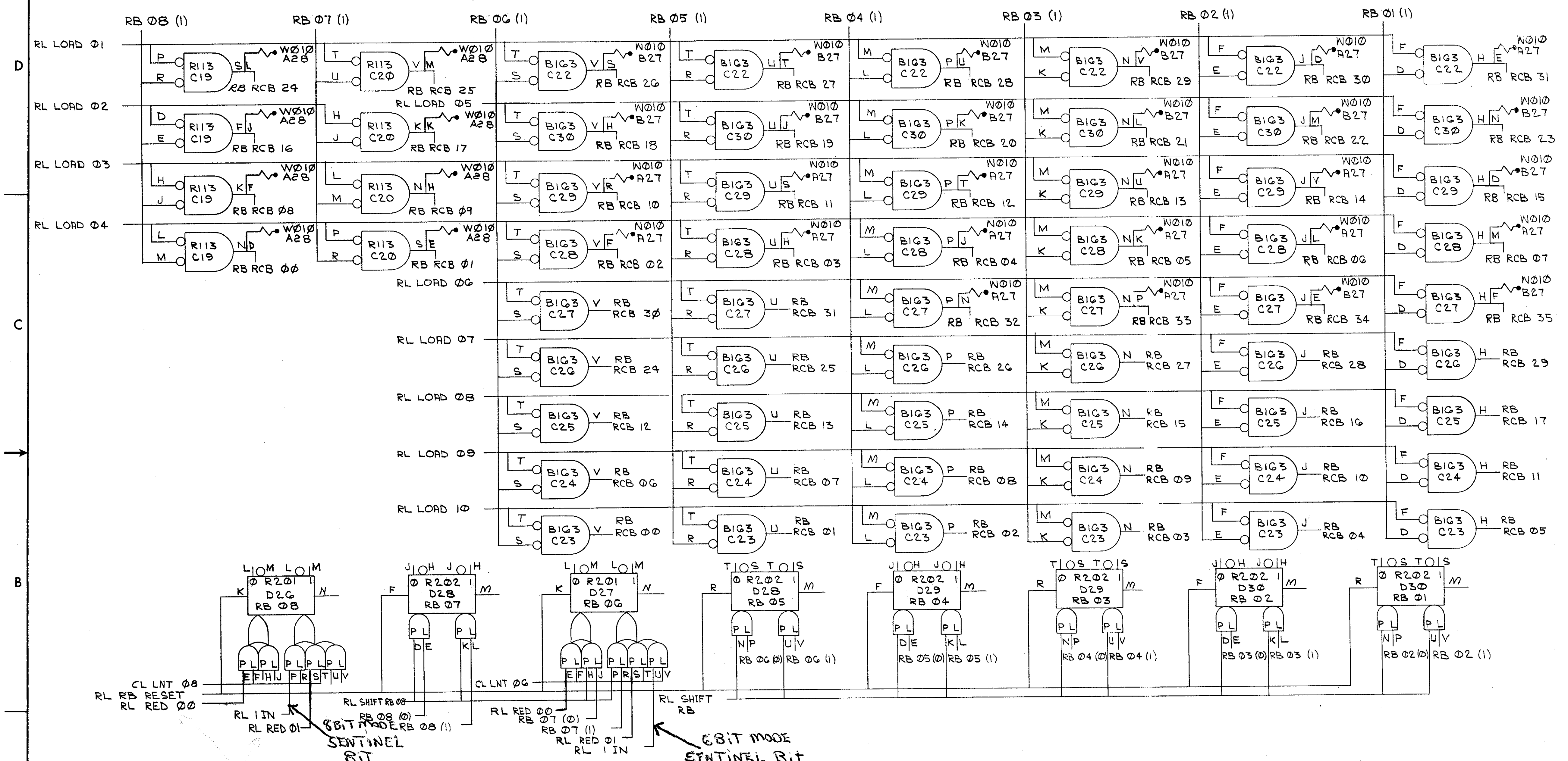
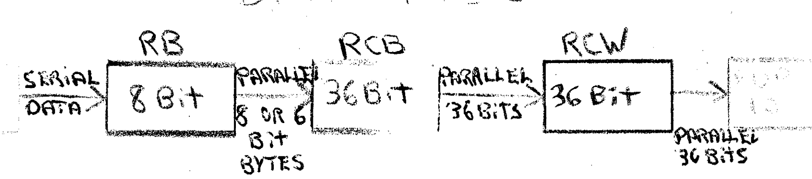


DATA REGISTERS



NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".

REV.	CHANGE NO.	CHK
PØ1	PMR 13 AUG 70	
PØ2	9-2-70	
PØ3	10-2-70	
PØ4	10-9-70	
PØ5	10-20-70	

FIRST USED ON OPTION/MODEL	PDP-1Ø
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	
MATERIAL	
FINISH	
DRN.	DATE 7 AUG 70
CHK'D.	DATE
ENG.	DATE
PROJ. ENG.	DATE
PROD.	DATE
NEXT HIGHER ASSEMBLY	A-ML-DSIØ-Ø
SCALE	NONE
SHEET	1 OF 1

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: RECEIVE BUFFER

SIZE D | CODE BS | NUMBER DSIØ-Ø-RB | REV. PØ5

DEC FORM NO. DRD 102A

NOTE: SENTINEL Bit indicates 1 CHAR HAS BEEN ASSEMBLED
First SENTINEL Bit is generated after SYNC CHAR. HAS BEEN DECODED

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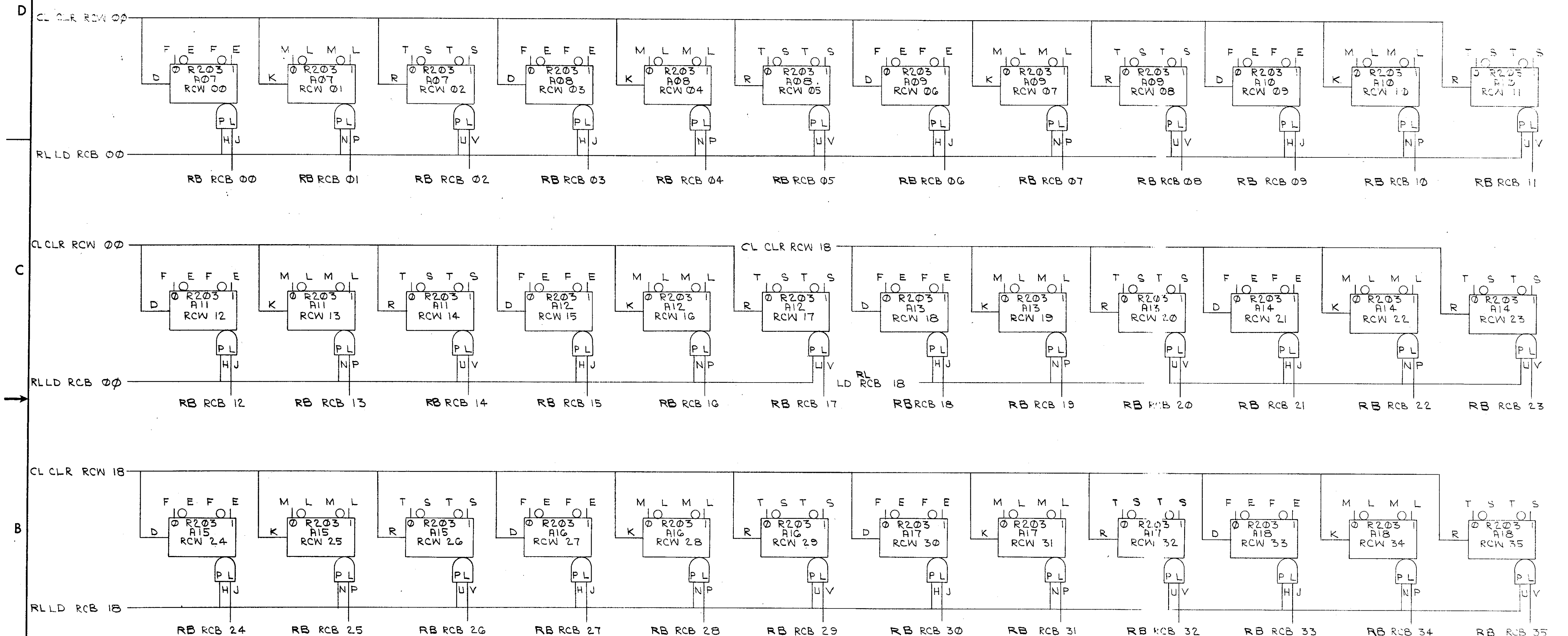


NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".

FIRST USED ON OPTION/MODEL: PDP-10

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —/—
FINISH —/—

QTY.	DESCRIPTION	PART NO.	ITEM NO.

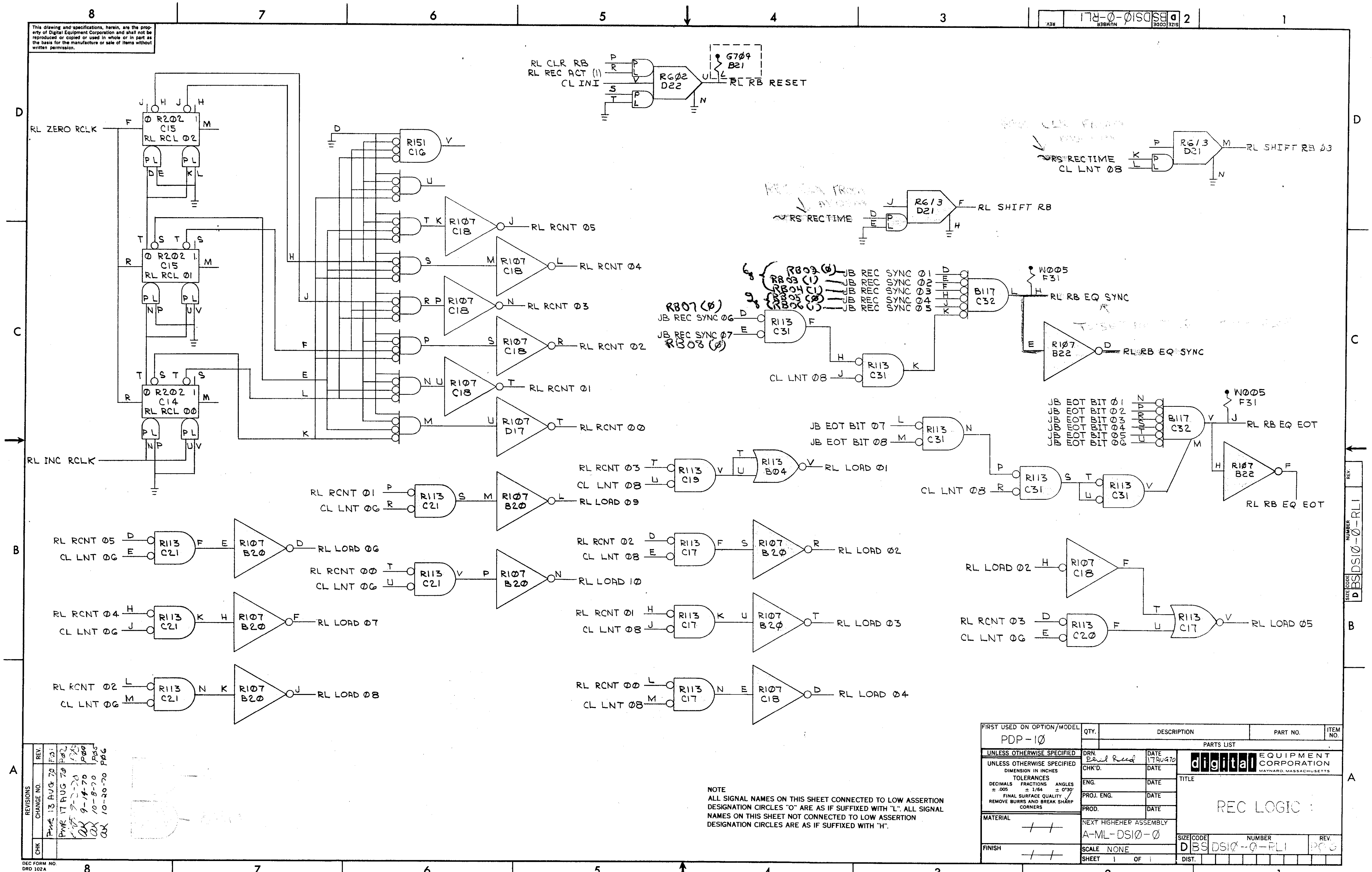
PARTS LIST

DRN. Bill Reed
NEXT HIGHER ASSEMBLY: A-ML-DS10-0
SCALE: NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: REC BIT RACK

SIZE D CODE BS NUMBER DS10-0-RCW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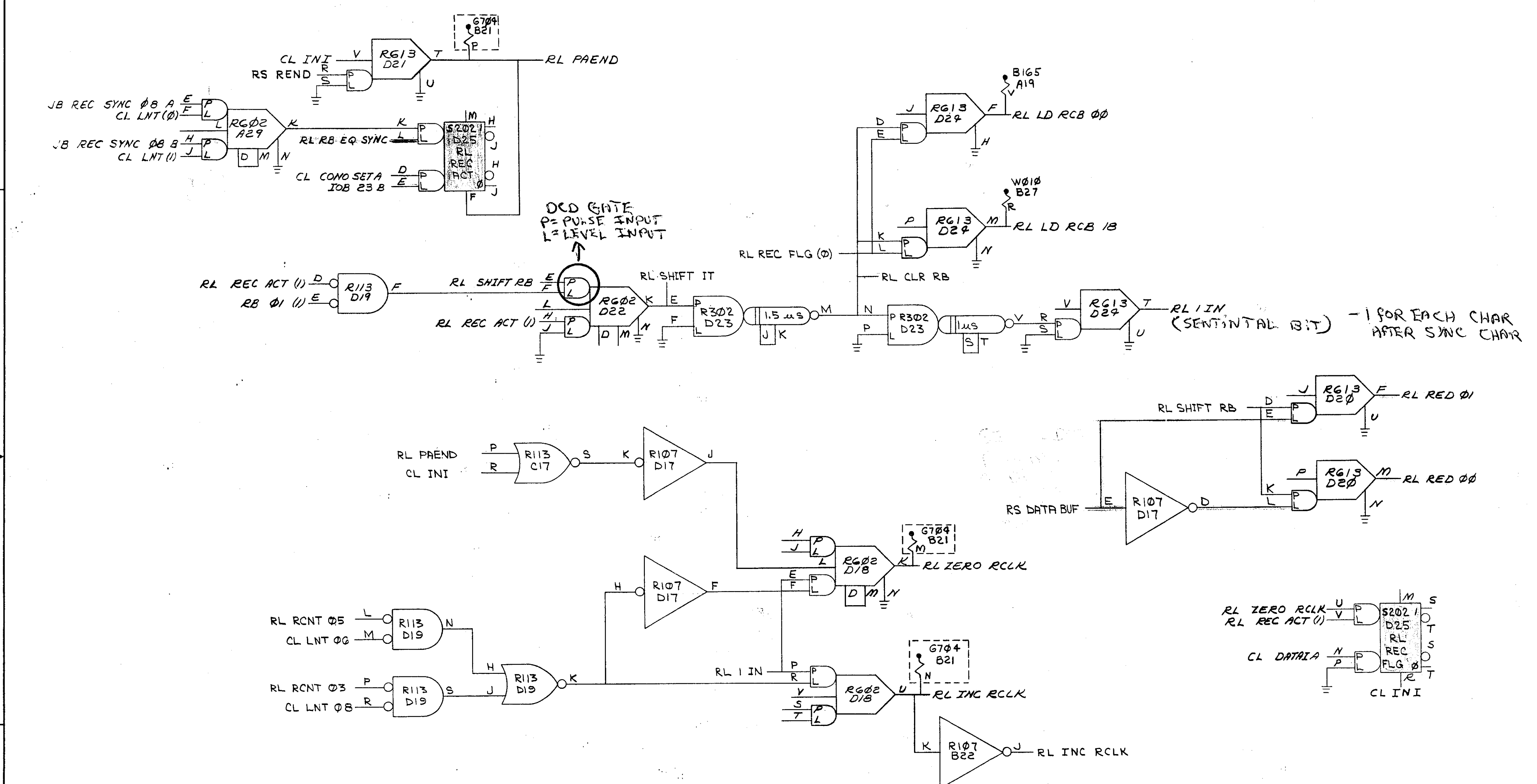
RL ZERO RCLK
RL INC RCLK
RL RCL Ø2
RL RCL Ø1
RL RCL ØØ
RL RCNT Ø5
RL RCNT Ø4
RL RCNT Ø3
RL RCNT Ø2
RL RCNT Ø1
RL RCNT ØØ
RL CLR RB
RL REC ACT (1)
CL INI
RL RB RESET
RL SHIFT RB
RL SHIFT RB Ø3
RS RECTIME
CL LNT Ø8
JB REC SYNC Ø1
JB REC SYNC Ø2
JB REC SYNC Ø3
JB REC SYNC Ø4
JB REC SYNC Ø5
JB REC SYNC Ø6
JB REC SYNC Ø7
RL RB EQ SYNC
JB EOT BIT Ø1
JB EOT BIT Ø2
JB EOT BIT Ø3
JB EOT BIT Ø4
JB EOT BIT Ø5
JB EOT BIT Ø6
JB EOT BIT Ø7
JB EOT BIT Ø8
RL RB EQ EOT
CL LNT Ø6
RL LOAD Ø1
RL LOAD Ø2
RL LOAD Ø3
RL LOAD Ø4
RL LOAD Ø5
RL LOAD Ø6
RL LOAD Ø7
RL LOAD Ø8
RL LOAD Ø9
RL LOAD 1Ø
NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".
FIRST USED ON OPTION/MODEL PDP-1Ø
NEXT HIGHER ASSEMBLY A-ML-DSIØ-Ø
DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE REC LOGIC
SIZE D CODE BS NUMBER DSIØ-Ø-RL1
SCALE NONE
SHEET 1 OF 1

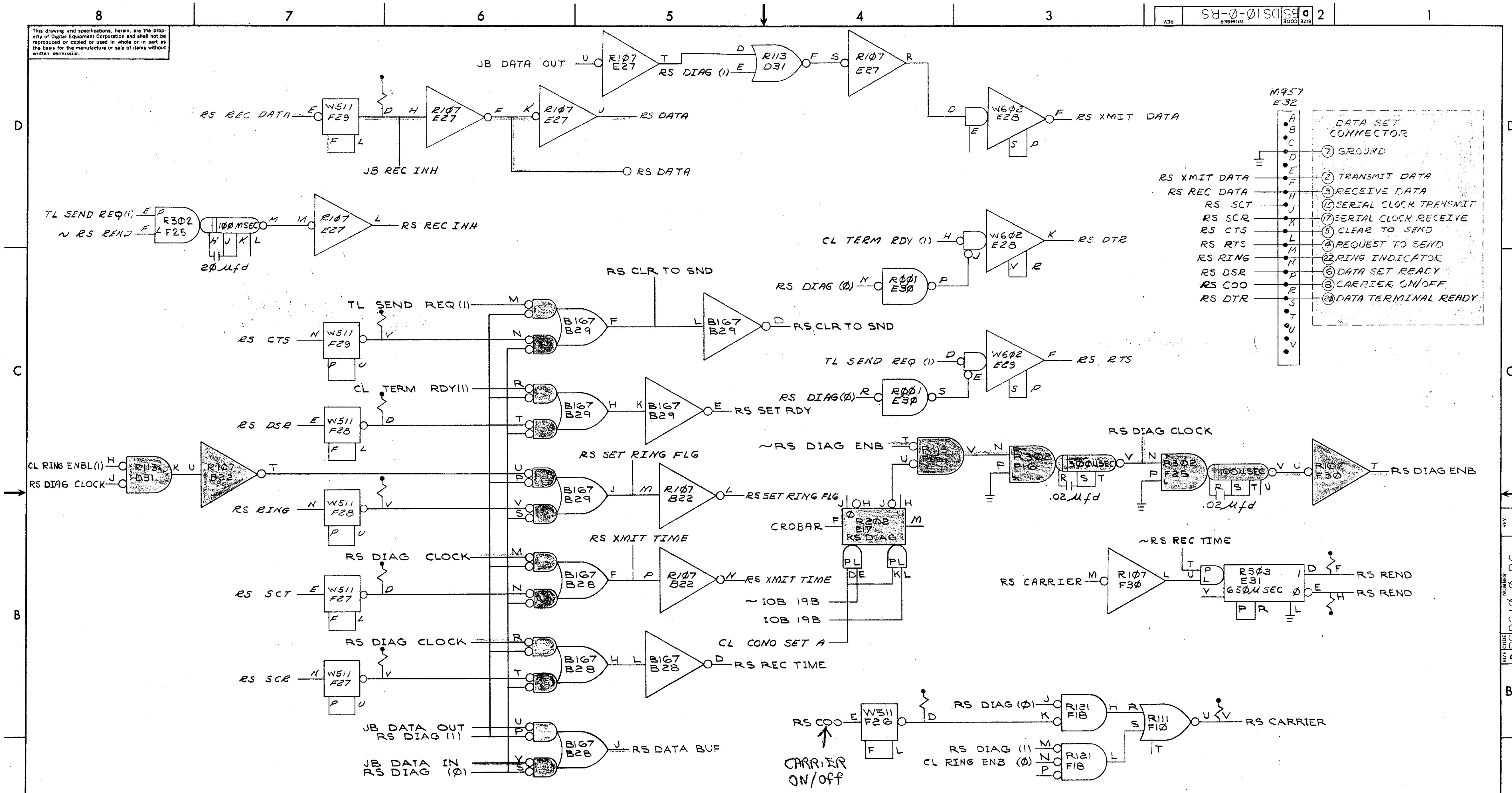


NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".

CHK	CHANGE NO.	REV.
PWR	13 AUG 70	PØ1
PWR	17 AUG 70	PØ2
	9-10-70	PØ4
	10-2-70	PØ5
	10-8-70	PØ6
	10-20-70	PØ7
	11-1-70	PØ8

FIRST USED ON OPTION/MODEL: PDP-1Ø	QTY.	DESCRIPTION	PART NO. / ITEM NO.
		PARTS LIST	
UNLESS OTHERWISE SPECIFIED: DIMENSION IN INCHES; TOLERANCES: DECIMALS ± .005, FRACTIONS ± 1/64, ANGLES ± 0°30'; FINAL SURFACE QUALITY; REMOVE BURRS AND BREAK SHARP CORNERS	DRN. Phil Reed	DATE 11 AUG 70	digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS
	CHK'D.	DATE	TITLE: REC LOGIC
	ENG.	DATE	
	PROJ. ENG.	DATE	
	PROD.	DATE	
MATERIAL	NEXT HIGHER ASSEMBLY: A-ML-DSIØ-Ø		SIZE D, CODE BS, NUMBER DSIØ-Ø-RL2, REV. PØ8
FINISH	SCALE NONE; SHEET 1 OF 1		DIST.

DEC FORM NO. DRD 102A



NORMAL OPERATION

DIAGNOSTIC MODE. MODEM IS DISCONNECTED SO THAT DATA CAN BE LOOPED FROM XMIT TO REC WITHIN THE DS10. CONTROL SIGNALS NEEDED FROM THE MODEM ARE GENERATED BY DIAG MODE LOGIC.

NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".

FIRST USED ON OPTION/MODEL: PDP-1Ø

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES: DECIMALS ± .005, FRACTIONS ± 1/64, ANGLES ± 0°30'. FINAL SURFACE QUALITY. REMOVE BURRS AND BREAK SHARP CORNERS.

digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: RS 232 C INTERFACE TO DATA SET

DRN. DATE 7-22-70

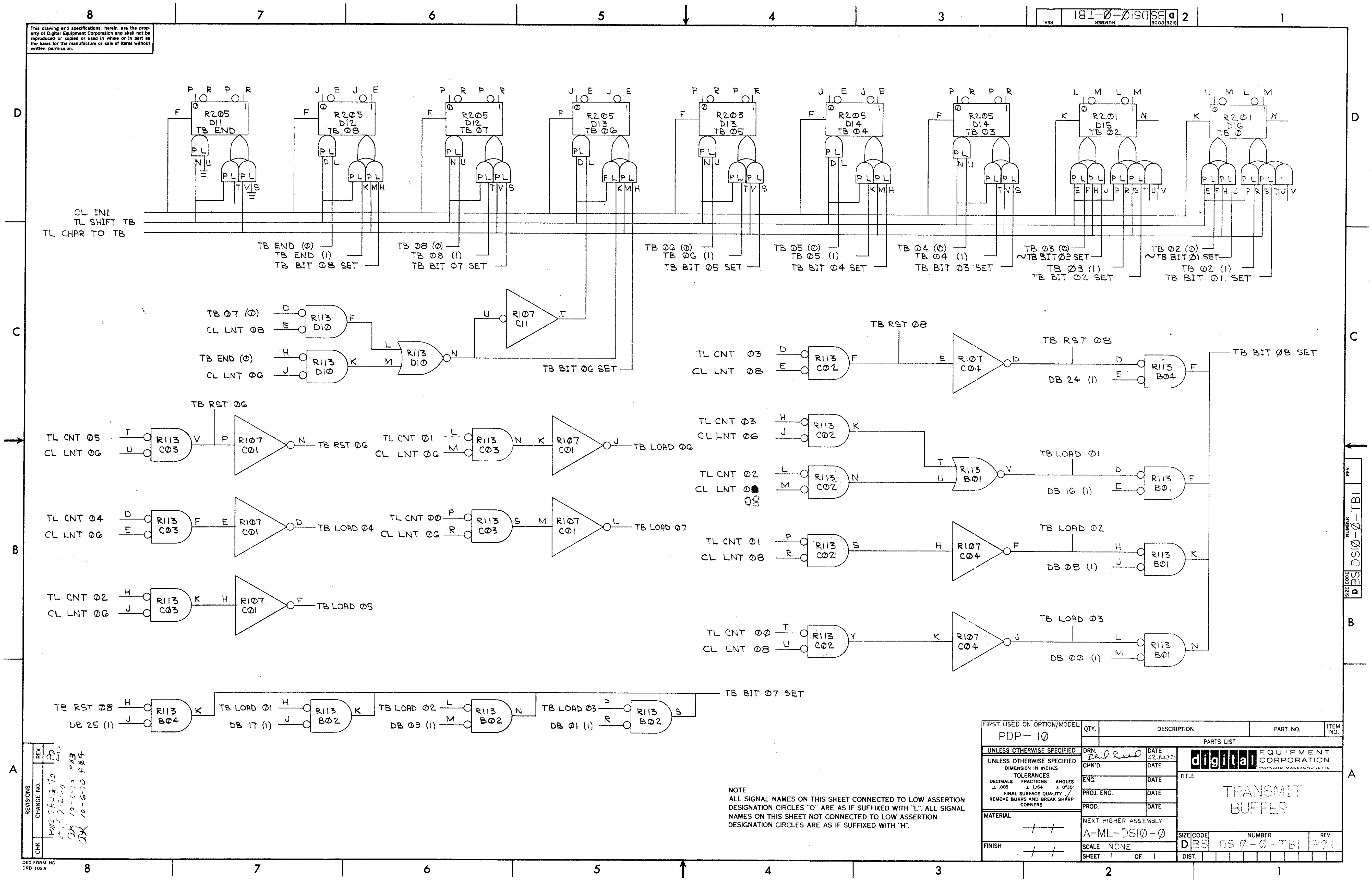
NEXT HIGHER ASS'Y. A-ML-DS1Ø-Ø

SIZE D CODE BS NUMBER DS1Ø-Ø-RS REV. PØ9

SCALE — SHEET 1 OF 1

REVISIONS	REV.	CHANGE NO.	DATE
	PØ5	PM 7AUG70	9-14-70
	PØ6		10-2-70
	PØ7		10-20-70
	PØ8		10-23-70
	PØ9		11-3-70

DEC FORM NO DRD 102A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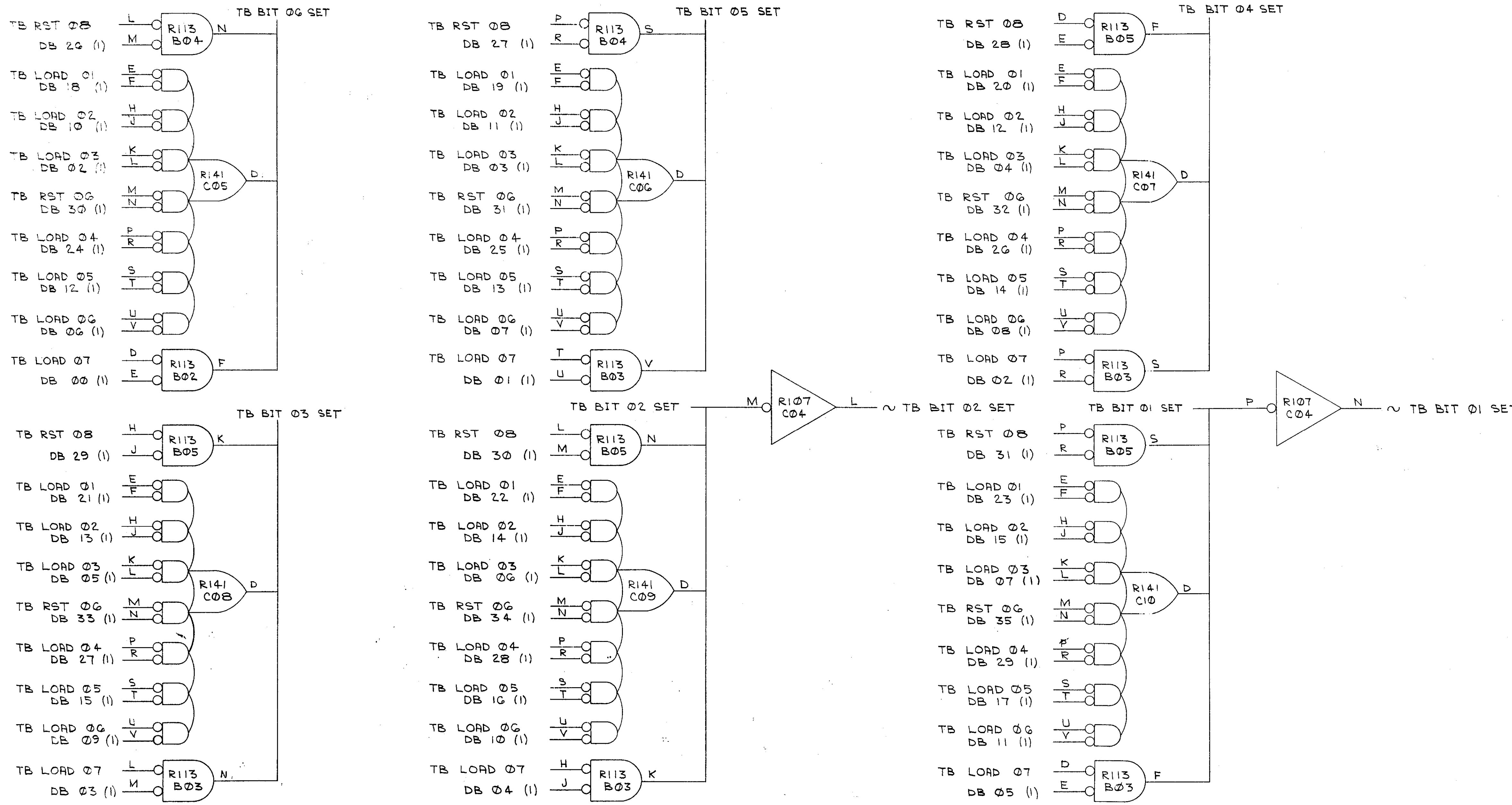
D BS DSIØ-Ø-TBI
CL INI
TL SHIFT TB
TL CHAR TO TB
TB END (Ø)
TB END (1)
TB BIT Ø8 SET
TB Ø8 (Ø)
TB Ø8 (1)
TB BIT Ø7 SET
TB Ø6 (Ø)
TB Ø6 (1)
TB BIT Ø5 SET
TB Ø5 (Ø)
TB Ø5 (1)
TB BIT Ø4 SET
TB Ø4 (Ø)
TB Ø4 (1)
TB BIT Ø3 SET
TB Ø3 (Ø)
~TB BIT Ø2 SET
TB Ø3 (1)
TB BIT Ø2 SET
TB Ø2 (Ø)
~TB BIT Ø1 SET
TB Ø2 (1)
TB BIT Ø1 SET
TB Ø7 (Ø)
CL LNT Ø8
TB END (Ø)
CL LNT Ø6
TB BIT Ø6 SET
TB RST Ø6
TL CNT Ø5
CL LNT Ø6
TL CNT Ø1
TB LOAD Ø6
TL CNT Ø4
TB LOAD Ø4
TL CNT ØØ
TB LOAD Ø7
TL CNT Ø2
TB LOAD Ø5
TB RST Ø8
TL CNT Ø3
DB 24 (1)
TB BIT Ø8 SET
TB LOAD Ø1
DB 16 (1)
TB LOAD Ø2
DB Ø8 (1)
TB LOAD Ø3
DB ØØ (1)
DB 25 (1)
DB 17 (1)
DB Ø9 (1)
DB Ø1 (1)
TB BIT Ø7 SET
NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".
FIRST USED ON OPTION/MODEL PDP-10
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
DRN. DATE 22 JULY 70
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE TRANSMIT BUFFER
NEXT HIGHER ASSEMBLY A-ML-DSIØ-Ø
SIZE D CODE BS NUMBER DSIØ-Ø-TBI
SCALE NONE
SHEET 1 OF 1
DEC FORM NO DRD 102A



NOTE
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FIRST USED ON OPTION/MODEL: PDP-1Ø

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL
FINISH

DRN. DATE 23JULY70
CHK'D. DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE

NEXT HIGHER ASSEMBLY: A-ML-DSIØ-Ø

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: TRANSMIT BUFFER

SIZE: D CODE: BS NUMBER: DSIØ-Ø-TB2

SCALE NONE
SHEET 1 OF 1

DEC FORM NO DRD 102A

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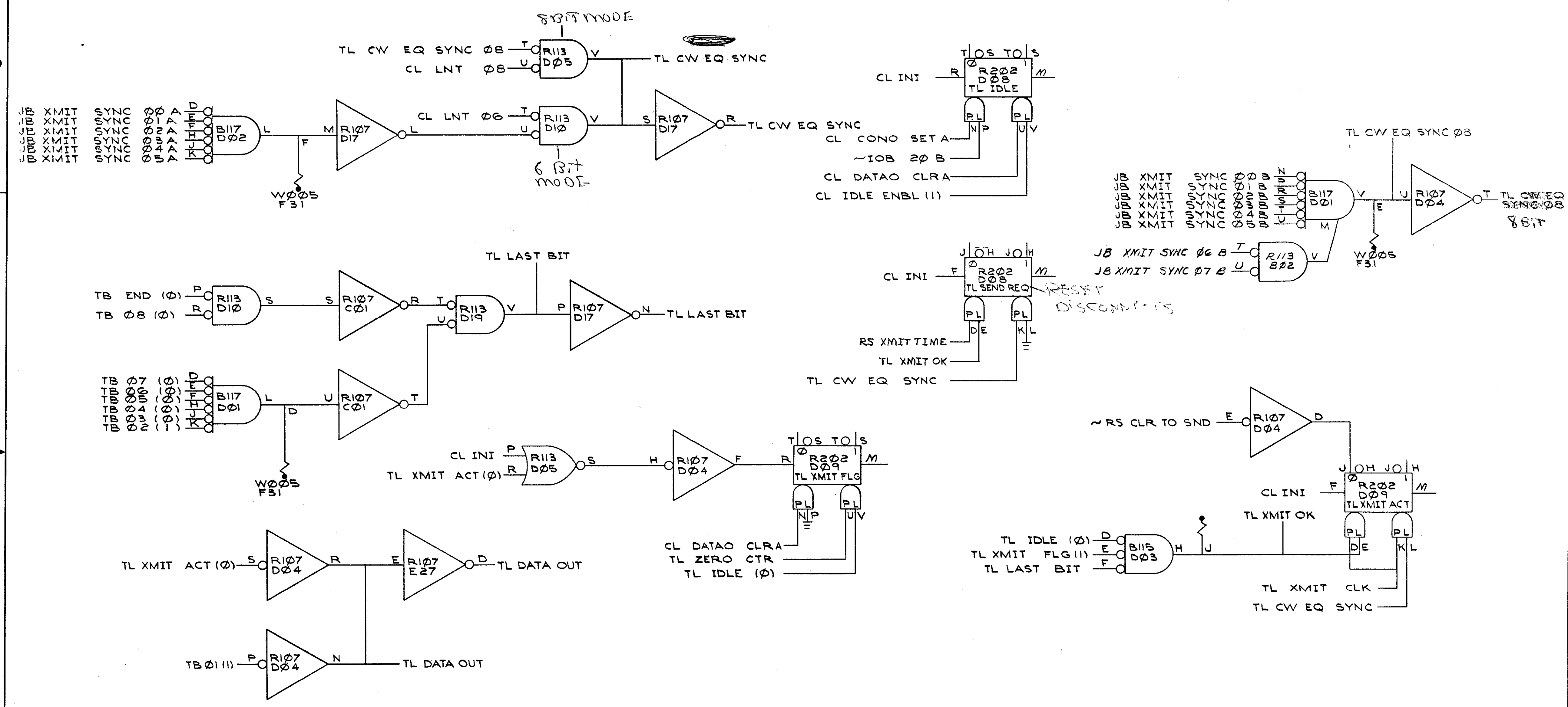

NOTE
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FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP1Ø		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES: DECIMALS ±.005, FRACTIONS ±1/64, ANGLES ±0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL —
FINISH —

DRN. J. Ferguson DATE 7-21-70
CHK'D. DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
NEXT HIGHER ASSY. A-ML-DS1Ø-Ø

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE TRANSMIT LOGIC

SIZE D CODE BS NUMBER DS1Ø-Ø-TL1 REV.
SCALE — SHEET 1 OF
DIST.

REVISIONS

REV.	CHANGE NO.	CHK
1	9-2-70	
Ø2	10-2-70	
Ø3	10-8-70	

DEC FORM NO. DRD 102A

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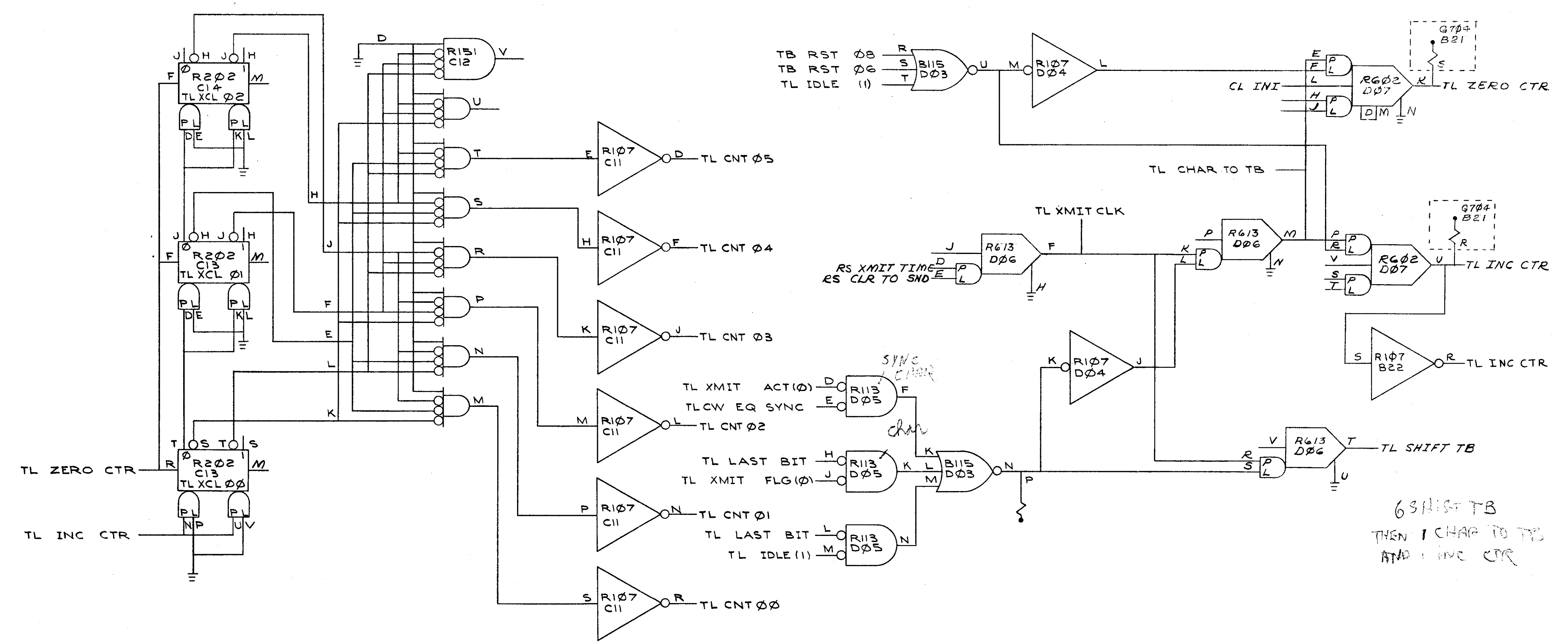

NOTE
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FIRST USED ON OPTION/MODEL: PDP1Ø

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

NEXT HIGHER ASSY. A-ML-DS1Ø-Ø

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: TRANSMIT LOGIC

SIZE D CODE BS NUMBER DS1Ø-Ø-TL2

SHEET 1 OF 1

D MU DSI0-MU

MODULE UTILIZATION

Slots 33–44 are empty in all rows.

Row A

1	B163	IOB 00; THRU; IOB 05
2	B163	IOB 06; THRU; IOB 11
3	B163	IOB 12; THRU; IOB 17
4	B163	IOB 18; THRU; IOB 23
5	B163	IOB 24; THRU; IOB 29
6	B163	IOB 30; THRU; IOB 35
7	R203	RCW 00; THRU; RCW 02
8	R203	RCW 03; THRU; RCW 05
9	R203	RCW 06; THRU; RCW 08
10	R203	RCW 09; THRU; RCW 11
11	R203	RCW 12; THRU; RCW 14
12	R203	RCW 15; THRU; RCW 17
13	R203	RCW 18; THRU; RCW 20
14	R203	RCW 21; THRU; RCW 23
15	R203	RCW 24; THRU; RCW 26
16	R203	RCW 27; THRU; RCW 29
17	R203	RCW 30; THRU; RCW 32
18	R203	RCW 33; THRU; RCW 35
19	B165	CL DATAI BUF C; CL DATAI BUF B; CL DATAI BUF A; RL LD RCB00
20	R001	CL DATAI BUF A; CL DATAI BUF B; CL DATAI BUF C; CL LO PI 0; CL LO PI 1; CL LO PI 2; CL HI PI 0
21		
22		
23	W991	JB IOS 03 A THRU JB IOS 09 A; JB IOS 03 B THRU JB IOS 09 B
24	W991	JB REC SYNC 01 THRU JB REC SYNC 07; JB REC SYNC 08 A; JB REC SYNC 08 B; JB REC INH
25	W991	JB XMIT SYNC 00 A THRU JB XMIT SYNC 05 A; JB XMIT SYNC 00 B THRU JB XMIT SYNC 07 B
26	W991	JB EOT BIT 01 THRU JB EOT BIT 08; JB DATA OUT; JB DATA IN
27	W010	D THRU V
28	W010	D THRU M
29	R602	RL REC ACT
30	W012	RS SET RING FLG; RS CARRIER; CL LO PI 0; CL LO PI 1; CL LO PI 2; CL LO PI
31	W012	RS REQ TIME; RS XMIT TIME; TL SEND REQ; CL TERM RDY; RS SET RDY; RS CLR TO SND
32	W012	RL REC ACT; RL INC RCLK; RC RB EQ SYNC; RL RB EQ EOT

Row B

1	R113	TB BIT 08 SET; TB LOAD 01
2	R113	TB BIT 06 SET; TB BIT 07 SET; TL CW EQ SYNC 08
3	R113	TB BIT 01 SET; THRU; TB BIT 05 SET
4	R113	TB BIT 08 SET; TB BIT 07 SET; TB BIT 06 SET; TB BIT 05 SET; RL LOAD 01
5	R113	TB BIT 04 SET; TB BIT 03 SET; TB BIT 02 SET; TB BIT 01 SET
6	R613	DB LOAD A; THRU; DB LOAD C
7	R203	DB 00; THRU; DB 02
8	R203	DB 03; THRU; DB 05
9	R203	DB 06; THRU; DB 08
10	R203	DB 09; THRU; DB 11
11	R203	DB 12; THRU; DB 14
12	R203	DB 15; THRU; DB 17
13	R203	DB 18; THRU; DB 20
14	R203	DB 21; THRU; DB 23
15	R203	DB 24; THRU; DB 26
16	R203	DB 27; THRU; DB 29
17	R203	DB 30; THRU; DB 32
18	R203	DB 33; THRU; DB 35
19	R613	DB CLEAR A; THRU; DB CLEAR C
20	R107	RL LOAD 06; THRU; RL LOAD 10; RL LOAD 02; RL LOAD 03
21	G704	D THRU U
22	R107	RL RB EQ SYNC; RL RB EQ EOT; RL INC RCLK; RS SET RING; RX XMIT TIME; TL INC CTR; RS SET RING FLG
23		
24		
25		
26		
27	W010	D THRU V
28	B167	RS REC TIME; RS XMIT TIME; RS REC TIME; RS DATA BUF
29	B167	RS CLR TO SND; RS SET RDY; RS CLR TO SND; RS SET READY; RS SET RING FLG
30	W012	CL ERR FLG; CL EOT FLG; CL HI PI 0; CL HI PI 1; CL HI PI 2; CL HI PI
31	W012	CL UNIT SEL; TL XMIT FLG; RL REC FLG; CL CNT EQ; CL END FLG
32	W012	TL XMIT ACT; TL INC CTR; TL IDLE; TL CW EQ SYNC; TL LAST BIT

Row C

1	R107	TB LOAD 04; TB LOAD 05; TB LOAD 06; TB LOAD 07; TB RST 06; TL LAST BIT
2	R113	TB RST 08; TB LOAD 01; TB LOAD 01; TB LOAD 02; TB LOAD 03
3	R113	TB LOAD 04; TB LOAD 05; TB LOAD 06; TB LOAD 07; TB RST 06
4	R107	TB RST 08; TB LOAD 02; TB LOAD 03; TB BIT 02 SET; TB BIT 01 SET
5	R141	TB BIT 06 SET
6	R141	TB BIT 05 SET
7	R141	TB BIT 04 SET
8	R141	TB BIT 03 SET
9	R141	TB BIT 02 SET
10	R141	TB BIT 01 SET
11	R107	TL CNT 05; THRU; TL CNT 00; TB 06
12	R151	TL CNT 05; THRU; TL CNT ØØ
13	R202	TL XCL 01; TL XCL 00
14	R202	TL XCL 02; RL RCL 00
15	R202	RL RCL 02; RL RCL 01
16	R151	RL RCNT 05; THRU; RL RCNT 00
17	R113	RL LOAD 02; THRU; RL LOAD 04; RL ZERO RCLK; RL LOAD 05
18	R107	RL LOAD 04; RL LOAD 05; RL RCNT 05; THRU; RL RCNT 01
19	R113	RB RCB 16; RB RCB 08; RB RCB 00; RB RCB 24; RL LOAD 01
20	R113	RL LOAD 05; RB RCB 17; RB RCB 09; RB RCB 01; RB RCB 25
21	R113	RL LOAD 06; THRU; RL LOAD 10
22	B163	RB RCB 31; THRU; RB RCB 26
23	B163	RB RCB 05; THRU; RB RCB 00
24	B163	RB RCB 11; THRU; RB RCB 06
25	B163	RB RCB 17; THRU; RB RCB 12
26	B163	RB RCB 23; THRU; RB RCB 24
27	B163	RB RCB 35; THRU; RB RCB 30
28	B163	RB RCB 07; THRU; RB RCB 02
29	B163	RB RCB 15; THRU; RB RCB 10
30	B163	RB RCB 23; THRU; RB RCB 18
31	B113	RL RB EQ SYNC; RL RB EQ EOT
32	B117	RL RD EQ SYNC; RL RD EQ EOT

Row D

1	B117	TL LAST BIT; TL CW EQ SYNC 08
2	B117	TL CW EQ SYNC
3	B115	TL XMIT OK; TL XMIT OK; TL SHIFT TB; TL ZERO CTR
4	R107	TL XMIT ACT; TL XMIT FLG; TL INC CTR; TL ZERO CTR; TL DATA OUT; TL CW EQ SYNC08
5	R113	TL SHIFT; TB; TL XMIT FLG; TL CW EQ SYNC
6	R613	TL XMIT CLK; TL INC CTR; TL SHIFT TB
7	P602	TL ZERO CTR; TL INC CTR
8	R202	TL SEND REQ; TL IDLE
9	R202	TL XMIT ACT; TL XMIT FLG
10	R113	TB 06; TL LAST BIT; TL CW EQ SYNC
11	R205	TB END
12	R205	TB 08; TB 07
13	R205	TB 06; TB 05
14	R205	TB 04; TB 03
15	R201	TB 02
16	R201	TB 01
17	R107	RL RED 00; RL ZERO RCLK; RL ZERO RCLK; TL CW EQ SYNC; TL LAST BIT; TL CW EQ SYNC; RL RCNT. 00
18	R602	RL ZERO RCLK; RL INC RCLK
19	R113	RL SHIFT IT; RL INC RCLK; RL INC RCLK; RL INC RCLK; TL LAST BIT
20	R613	RL RED 01; RL RED 00
21	R613	RL SHIFT RB; RL SHIFT RB 08; RL PAEND
22	R602	RL SHIFT IT; RL RB RESET
23	R302	RL 1 IN; RL 1 IN
24	R613	RL LD RCB 00; RL LD RCB 18; RL 1 IN
25	S202	RL REC ACT; RL REC FLG
26	R201	RB 08
27	R201	RB 06
28	R202	RB 07; RB 05
29	R202	RB 04; RB 03
30	R202	RB 02; RB 01
31	R113	RS XMIT DATA; RS SET RING FLG; CL UNIT SEL
32		

REVISIONS — CHK: [illegible]; CHANGE NO: 10-20-70, 10-23-?0; REV: P01, P02

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES: DECIMALS ±.005, FRACTIONS ±1/64, ANGLES ±0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —/—/—
FINISH —/—/—
FIRST USED ON OPTION/MODEL

DRN. [signature] DATE 9-15-70
CHK'D. / ENG. / PROJ. ENG. / PROD.

NEXT HIGHER ASSY. A-ML-DSI0-0

digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: MODULE UTILIZATION

SIZE D — CODE MU — NUMBER DSI0-MU — REV. F02
SCALE NONE — SHEET 1 OF 2

DEC FORM NO. DRD 105

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Slot	Row E module	Row E signals	Row F module	Row F signals
1	W851	10B 00 THRU 10B 17		
2	W851	10B 18 THRU 10B 35		
3	W851	10B RESET (REVED) (10B OR SPLIT) 10S 03 THRU 10S 09		
4	W851	10B DATAO CLR; 10B DATAO SET; 10B CONO CLR; 10B CONO SET; 10B DATAI; 10B CONI (10B RDI PULSE) (10B RDI DATA); CL 10B PI 01 THRU CL 10B PI 07		
5	W851	10B 00 THRU 10B 17		
6	W851	10B 18 THRU 10B 35		
7	W851	10B RESET (REVED) (10B OR SPLIT) 10S 03 THRU 10S 09		
8	W851	10B DATAO CLR; 10B DATAO SET; 10B CONO CLR; 10B CONO SET; 10B DATAI; 10B CONI (10B RDI PULSE) (10B RDI DATA); CL 10B PI 01 THRU CL 10B PI 07		
9				
10	B152	CL 10B PI 01 THRU CL 10B PI 07	R111	CL SELECT A; CL SELECT B; RS CARRIER
11	B152	CL 10B PI 01 THRU CL 10B PI 07	R002	CL SELECT A
12	R203	CL LO PI 0; CL LO PI 1; CL LO PI 2	R002	CL SELECT B
13	R203	CL HI PI 0; CL HI PI 1; CL HI PI 2	B165	CL SELECT A; CL SELECT B; CL CONI A BUF; CL CONI A BUF; CL CONI B BUF
14	R202	CL ERR FLG; CL EOT FLG	R113	CL DATAO CLR A; CL DATAO SET A; CL CONO CLR A; CL CONO SET A; CL DATAI A
15	R202	CL RING ENBL; CL END FLG	R113	CL CONI A; CL CONO CLR B; CL CONO SET B; CL CONI B; RS DIAG CLOCK
16	R202	CL IDLE ENBL; CL TERM RDY	R302	CL DATAI CLR; RS DIAG CLOCK
17	R202	CL DIAG CLOCK; CL LNT	R613	CL CLR RCW 00; CL CLR RCW 18; CL HI PI 0
18	B103	10B 20 THRU 10B 35	R121	CL HI PI; RS CARRIER; RS CARRIER; CL LO PI
19	B163	10B 30 THRU 10B 35	R107	CL HI PI; CL LO PI; CL INI B; 10B 26 B; 10B 20 B; 10B 18 B; 10B 27 B
20	B163	10B 24 THRU 10B 29	R303	CL INI B
21	B163	10B 18 THRU 10B 23	R613	CL INI; CL INI B; CL INI A
22	W107	10B 00 B THRU 10B 05 B	W107	10B 18 B THRU 10B 23B
23	W107	10B 06 B THRU 10B 11 B	W107	10B 24 B THRU 10B 29B
24	W107	10B 12 B THRU 10B 17 B	W107	10B 30 B THRU 10B 35B
25			R302	RS DATA; RS DIAG ENB
26	R202	CL RING FLAG	W511	RS CARRIER
27	R107	TL DATA OUT; RS DATA; RS REC INH; 10B 19 B; RS XMIT DATA	W511	RS XMIT TIME; RS REC TIME
28	W602	RS XMIT DATA; RS DTR	W511	RS SET RDY; RS SET RING FLG
29	W602	RS RTS	W511	RS DATA; RS CLR TO SND
30	R001	CL HI PI 1; CL HI PI 2; CL CONI A BUF; CL CONI B BUF; RS RTR; RS DTS	R107	CL LNT 06; CL LNT 08; RS REND; CL LNT 06; CL LNT 08; RS DIAG ENB
31	R303	RS REND	W005	D THRU J
32	W957	DATA SET CONN		
33–44				

REVISIONS: CHANGE NO. / REV. — 10-20-70 P01; 10-23-70 P02

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL: —
FINISH: —
FIRST USED ON OPTION/MODEL:

DRN. A. Kilbert DATE 9-15-70
CHK'D. DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
NEXT HIGHER ASSY. A-ML-DS10-0
SCALE NONE
SHEET 2 OF 2

digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: MODULE UTILIZATION

SIZE D CODE MU NUMBER DS10-0-MU REV. P02

DEC FORM NO. DRD 105

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

MADE BY A. KIBORT | DATE 9/15/70 | CHECKED | DATE | SECTION
ENG | DATE | PROD | DATE | ISSUED SECT.

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
	R613	PULSE AMPLIFIER	8
	WØØ5	CLAMP LOADS	1
	WØ1Ø	CLAMP LOADS	3
	WØ12	INDICATOR CABLE CONNECTOR	6
	W1Ø7	I/O BUS RECEIVER CKT.	6
	W511	NEGATIVE INPUT CONVERTER	4
	W6Ø2	BIPOLAR OUTPUT CONVERTER	2
	W851	PDP-1Ø BUS CONNECTOR BOARD	8
	W991	BLANK MODULE/36 PINS	4
	S202	FLIP-FLOP	1
	G704	LEVEL TERMINATORS	1

TITLE: MODULE UTILIZATION PARTS LIST
ASSY NO. D-MU-DS1Ø-Ø-MU
SHEET 2 OF 2
SIZE A | CODE PL | NUMBER DS1Ø-Ø-MU | REV. PØ1 | ECO NO.
DIST.

DEC FORM NO.16-1031
DRA 110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

MADE BY A. KIBORT | DATE 9/15/70 | CHECKED | DATE | SECTION
ENG | DATE | PROD | DATE | ISSUED SECT.

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
	B115	NAND/NOR GATE	1
	B117	NAND/NOR GATE	3
	B152	BINARY TO OCTAL DECODER	2
	B163	DIODE GATE	19
	B165	DIODE INVERTER	2
	B167	ADDER GATE	2
	M957		1
	RØØ1	DIODE NETWORK	2
	RØØ2	DIODE NETWORK	2
	R1Ø7	INVERTER	11
	R111	EXPANDABLE NAND/NOR GATE	1
	R113	NAND/NOR GATE	18
	R121	NAND/NOR GATE	1
	R141	AND/NOR GATE	6
	R151	BINARY-TO-OCTAL DECODER	2
	R2Ø1	FLIP-FLOP	4
	R2Ø2	DUAL FLIP-FLOP	13
	R2Ø3	TRIPLE FLIP-FLOP	26
	R2Ø5	DUAL FLIP-FLOP	4
	R3Ø2	DUAL DELAY MULTIVIBRATOR	3
	R3Ø3	INTEGRATING ONE SHOT	2
	R6Ø2	PULSE AMPLIFIER	4

TITLE: MODULE UTILIZATION PARTS LIST
ASSY NO. D-MU-DS1Ø-Ø-MU
SHEET 1 OF 2
SIZE A | CODE PL | NUMBER DS1Ø-Ø-MU | REV. PØ1 | ECO NO.
DIST.

DEC FORM NO.16-1031
DRA 110

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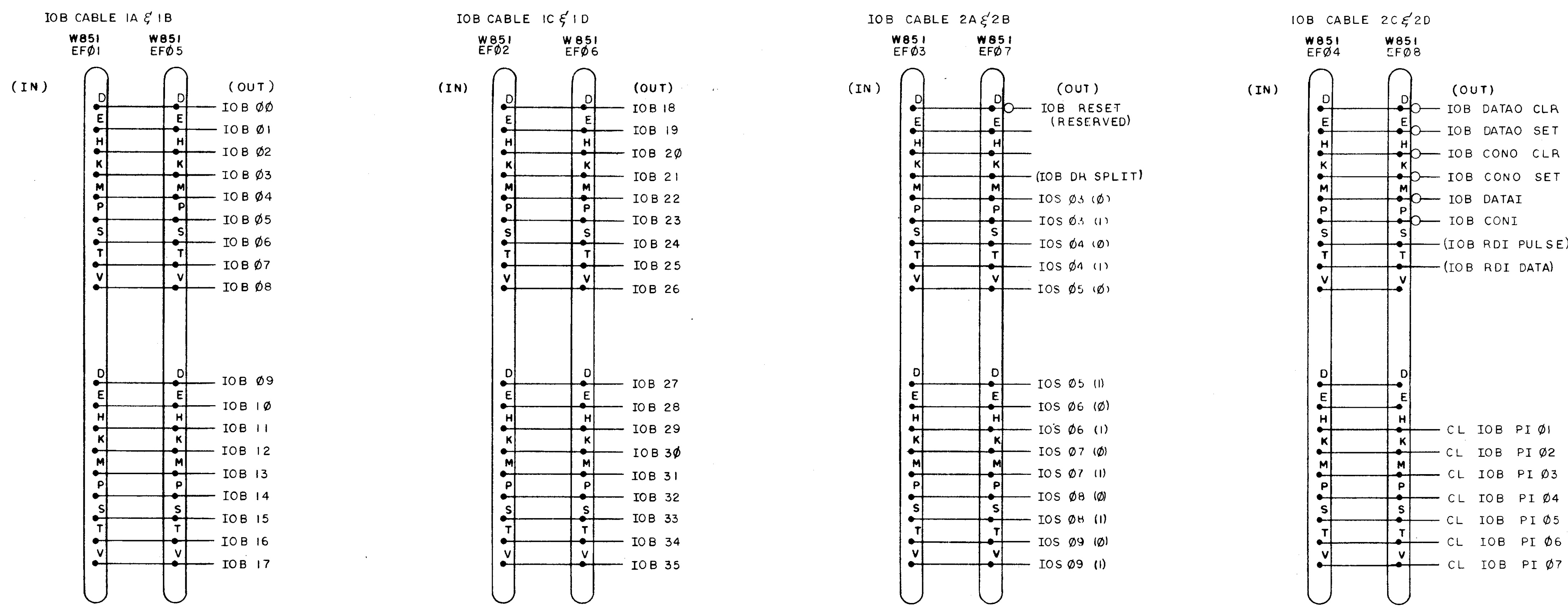


NOTES:

1. PINS C,F,J,L,N,R,U ARE GROUNDED

NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".

REV.	CHANGE NO.	CHK
P01	PJW 7 AUG 70	
P02	JF 9-2-70	
P03	AK 10-06-70	

FIRST USED ON OPT/MOD: PDP-10

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES: DECIMALS ± .005, FRACTIONS ± 1/64, ANGLES ± 0°30'. FINAL SURFACE QUALITY. REMOVE BURRS AND BREAK SHARP CORNERS.

DRN. [signature] DATE 7-23-70

NEXT HIGHER ASSY. A-ML-DS10-0

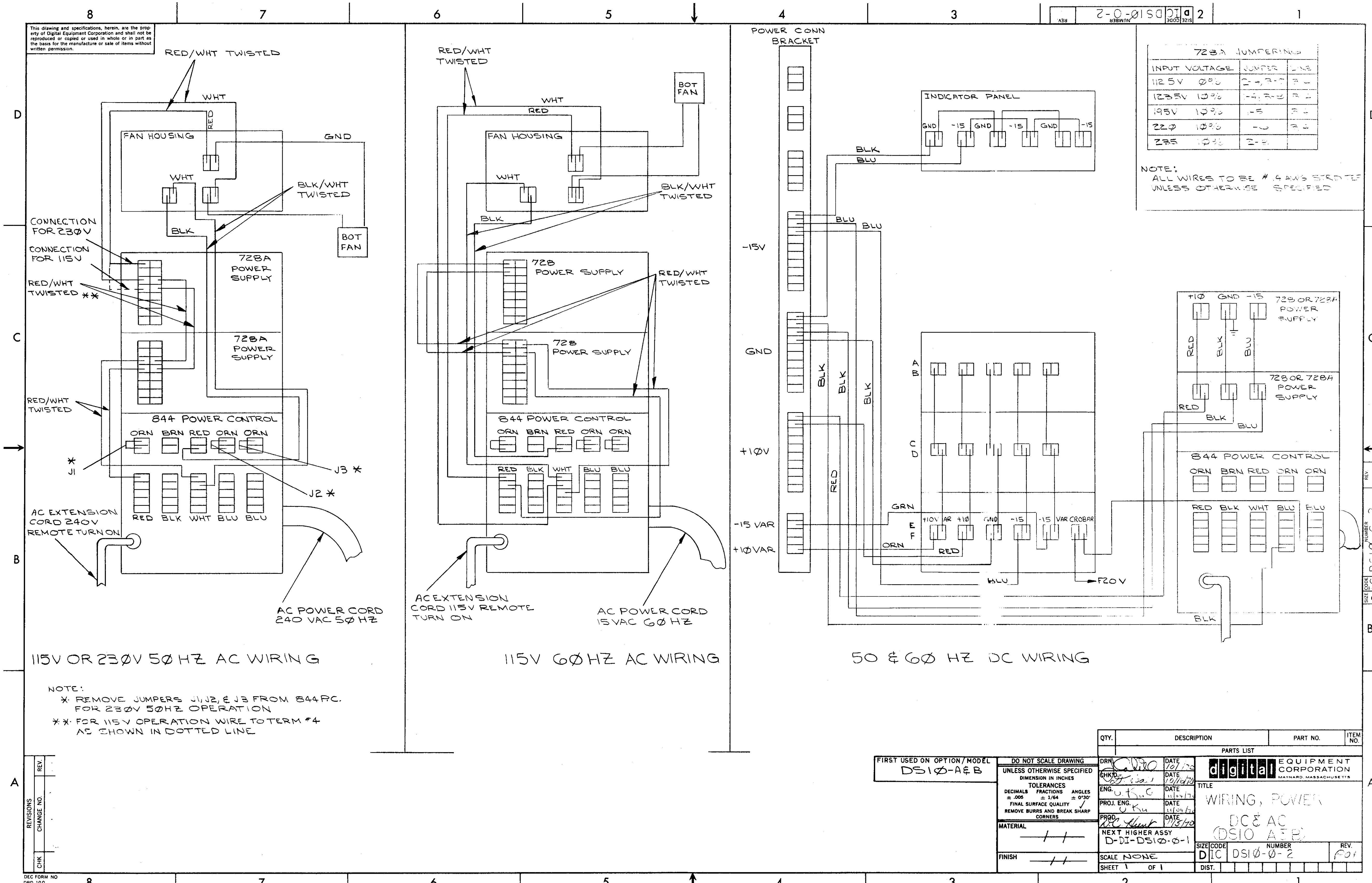
SCALE NONE — SHEET 1 OF 1

digital EQUIPMENT CORPORATION, MAYNARD MASSACHUSETTS

TITLE: I/O BUS INTERFACE

SIZE D — CODE IC — NUMBER DS10-0-IOB — REV. P03

DEC FORM NO DRD 102A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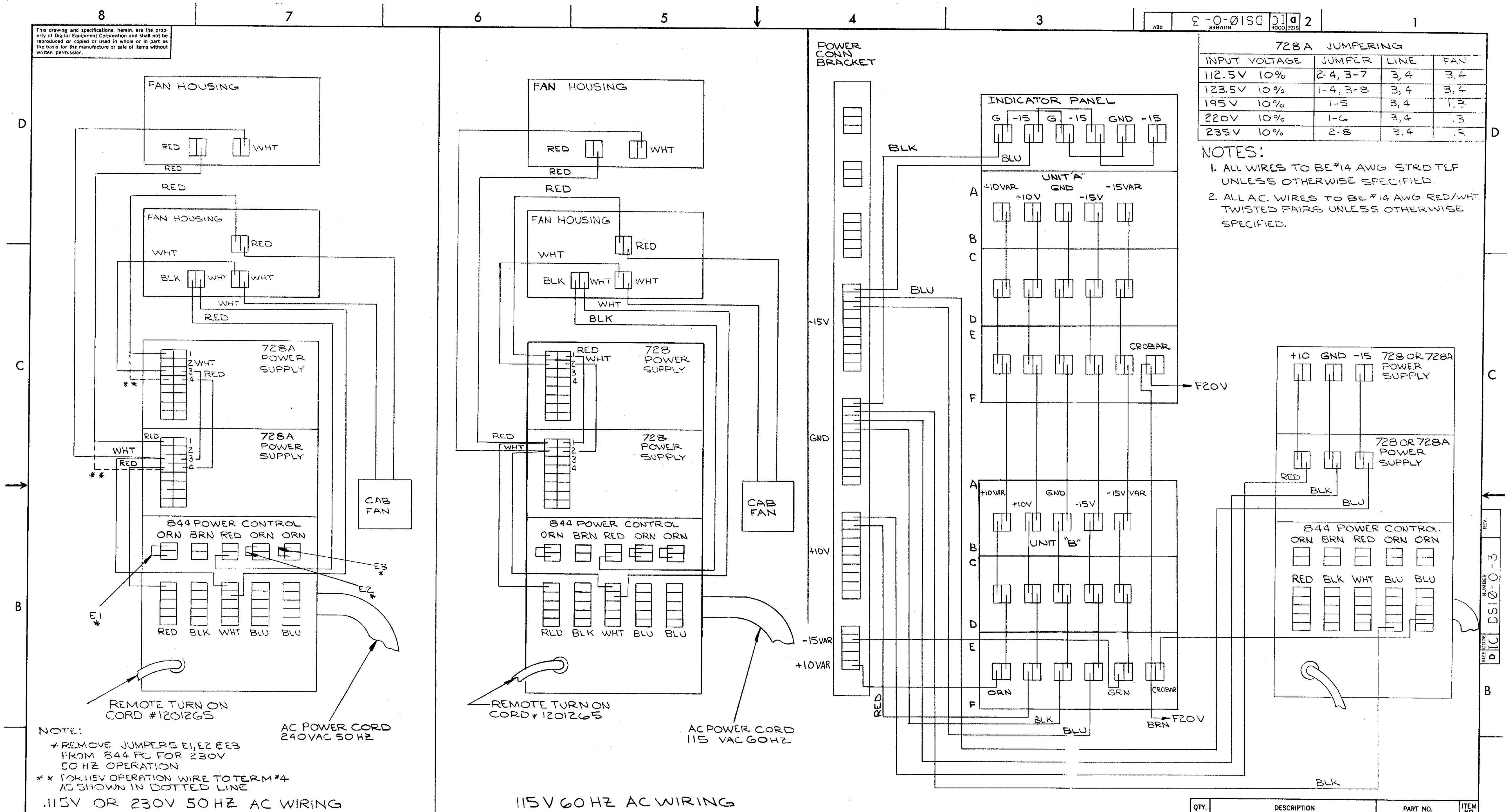
RED/WHT TWISTED
WHT
RED
FAN HOUSING
GND
WHT
BLK/WHT TWISTED
BOT FAN
BLK
CONNECTION FOR 230V
CONNECTION FOR 115V
RED/WHT TWISTED **
728A POWER SUPPLY
728A POWER SUPPLY
RED/WHT TWISTED
844 POWER CONTROL
ORN BRN RED ORN ORN
* J1
J3 *
J2 *
AC EXTENSION CORD 240V REMOTE TURN ON
RED BLK WHT BLU BLU
AC POWER CORD 240 VAC 50 HZ
115V OR 230V 50 HZ AC WIRING
NOTE:
*. REMOVE JUMPERS J1, J2, & J3 FROM 844 P.C. FOR 230V 50HZ OPERATION
**. FOR 115V OPERATION WIRE TO TERM #4 AS SHOWN IN DOTTED LINE
RED/WHT TWISTED
BOT FAN
728 POWER SUPPLY
RED/WHT TWISTED
728 POWER SUPPLY
844 POWER CONTROL
ORN BRN RED ORN ORN
RED BLK WHT BLU BLU
AC EXTENSION CORD 115V REMOTE TURN ON
AC POWER CORD 115 VAC 60 HZ
115V 60HZ AC WIRING
POWER CONN BRACKET
-15V
GND
+10V
-15 VAR
+10 VAR
INDICATOR PANEL
GND -15 GND -15 GND -15
BLK
BLU
A B
C D
E F
GRN
ORN
+10V AR +10 GND -15 -15 VAR CROBAR
F20V
728 OR 728A POWER SUPPLY
+10 GND -15
728 OR 728A POWER SUPPLY
RED BLK BLU
844 POWER CONTROL
ORN BRN RED ORN ORN
RED BLK WHT BLU BLU
50 & 60 HZ DC WIRING
728A JUMPERING
INPUT VOLTAGE
115V
123.5V
195V
220
235
NOTE:
ALL WIRES TO BE #.. AWG STRANDED UNLESS OTHERWISE SPECIFIED
QTY. DESCRIPTION PART NO. ITEM NO.
PARTS LIST
FIRST USED ON OPTION/MODEL DS10-A&B
DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
TITLE WIRING, POWER DC & AC (DS10 A & B)
NEXT HIGHER ASSY D-DI-DS10-0-1
SIZE D CODE IC NUMBER DS10-0-2
SCALE NONE
SHEET 1 OF 1
REVISIONS
DEC FORM NO DRD 100



728A JUMPERING			
INPUT VOLTAGE	JUMPER	LINE	FAN
112.5V 10%	2-4, 3-7	3, 4	3, 4
123.5V 10%	1-4, 3-8	3, 4	3, 4
195V 10%	1-5	3, 4	1, 3
220V 10%	1-6	3, 4	.3
235V 10%	2-8	3, 4	.3

NOTES:

1. ALL WIRES TO BE #14 AWG STRD TEF UNLESS OTHERWISE SPECIFIED.
2. ALL A.C. WIRES TO BE #14 AWG RED/WHT TWISTED PAIRS UNLESS OTHERWISE SPECIFIED.

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: DSI0- C&D

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —
FINISH —

DRN. [signature] DATE 10-6-70
CHK'D. D. Healy DATE 10-16-70
ENG. [signature] DATE 11/04/70
PROJ. ENG. V. Ku DATE 11/04/70
PROD. D.C. Hunt DATE 11/5/70

NEXT HIGHER ASSY: D-DI-DS10-0-1
SCALE: NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: WIRING POWER DC & AC (DS10 C&D)

SIZE D CODE IC NUMBER DS10-0-3 REV.

Digital Equipment Corporation
Maynard, Massachusetts

digital

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