

PDP-11/40 system manual

Gunnar Barbro

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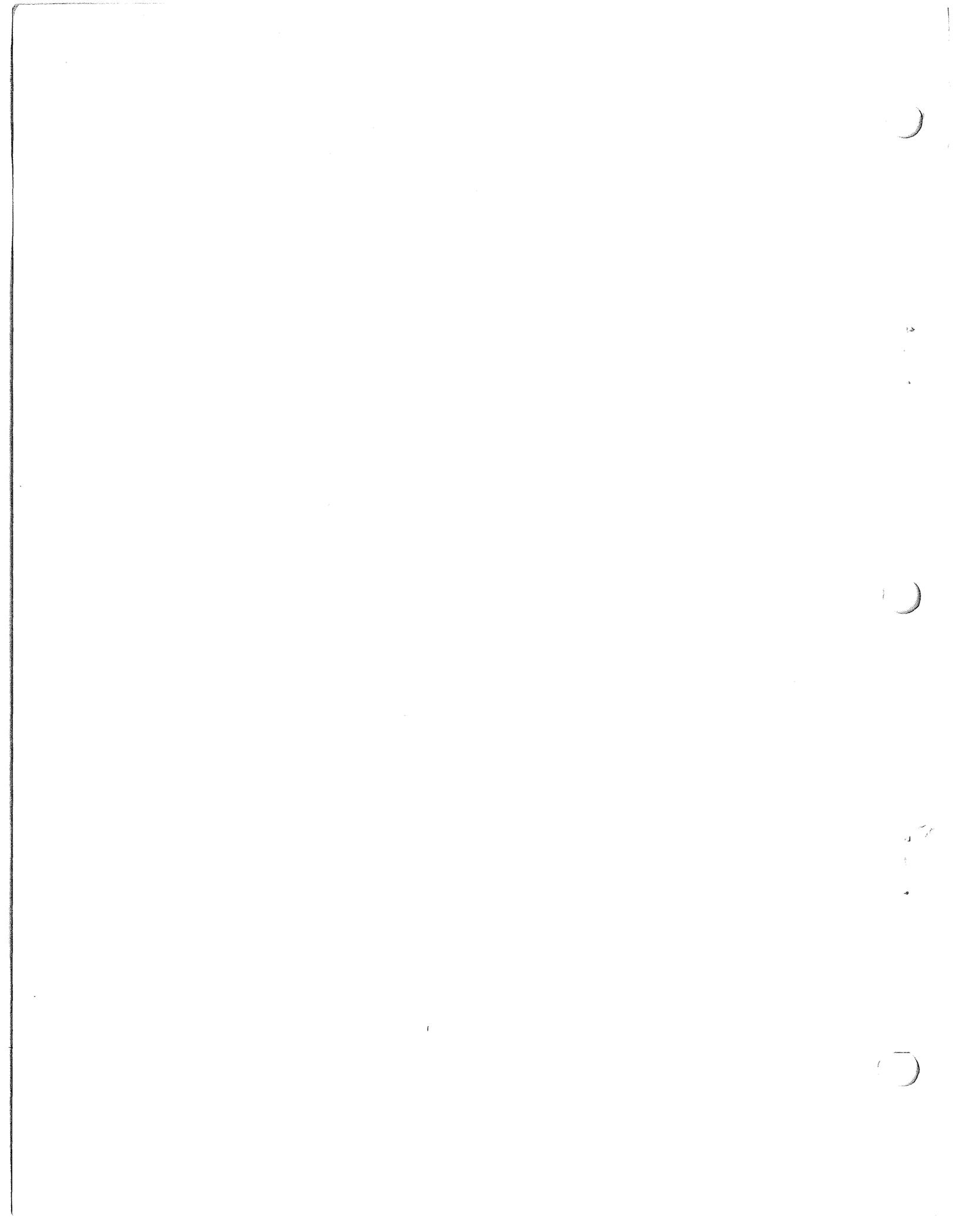


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CHAPTER 1 INTRODUCTION

1.1 SCOPE

This manual, the PDP11/40 System Manual, provides a general introduction to the PDP11/40 system and includes sections on installation, operation, the instruction set, options, mounting and power, and maintenance. This overview is supplemented with references to other manuals in the PDP11/40 series for detailed explanations.

The PDP11/40 manuals provide the user with the theory of operation necessary to understand, operate, and maintain the PDP11/40 System. These manuals reference associated engineering drawings, both are listed in Table 1-2. Please note that the associated drawings are separate volumes and documented by their Drawing Directory number (not the manual number). Both volumes are necessary.

The level of discussion in each manual assumes that the reader is familiar with basic digital computer theory. The maintenance philosophy presents information about normal system operation and enables the user to recognize trouble symptoms and to perform necessary corrective action. Each individual manual contains theory of operation, diagrams, maintenance techniques. Logic drawings for the specific component covered are contained in separate volumes.

This chapter describes the basic system components (paragraph 1.2) and provides a functional description of the overall PDP-11/40 system and each of its major components (paragraph 1.3). The remainder of the chapter covers applicable documents (paragraph 1.4), engineering drawings (paragraph 1.5), and terminology (paragraph 1.6).

1.2 SYSTEM COMPONENTS

The PDP-11/40 System consists of six basic components: processor, programmer's console, core memory, DECwriter with associated control, power supply, and mounting box. Possible variations to this basic system are listed in Table 1-1.

Options and peripherals added to the basic PDP-11/40 System are covered in separate manuals delivered with the system. Manuals are included only for those options specifically ordered with an individual system.

Table 1-1

Possible PDP-11/40 Variations

| Major Component | Possible Variations |
|------------------------------|--|
| *KD11-A Processor | No variations in basic processor. However, any of the following internal processor options can be included: KE11-E Extended Instruction Set (EIS) KE11-F Floating Instruction Set (FIS) KJ11-A Stack Limit Register KM11-A Maintenance Module (console) KT11-D Memory Management KW11-L Line Frequency Interrupt Clock |
| *KY11-D Programmer's Console | None |

Table 1-1 (Cont)

Possible PDP-11/40 Variations

| Major Component | Possible Variations | |
|-----------------|---------------------|--|
| Core Memory | MM11-L | - 8K core memory, 900 ns cycle time, 350 ns internal access time |
| | *MF11-L | - MM11-L memory plus backplane, space exists for two additional MM11-Ls |
| | ME11-L | - MM11-L memory plus backplane, mounting box, and power supply (complete memory system) |
| | MM11-S | - MM11-L memory, interleaved, plus backplane (may be used for expansion of memory above 24K) |

Table 1-1 (Cont)

Possible PDP-11/40 Variations

Major Component

Possible Variations

Core Memory (Cont)

NOTES

Memory systems compatible with the PDP-11/20 may also be used in the PDP-11/40. These memories are:

- MM11-E - 4K by 16 bit
- MM11-F - 4K by 16 bit
- MM11-FP - 4K by 16 bit,
with parity
- MM11-H - 1K by 16 bit
- MM11-J - 2K by 16 bit

These memories cannot be mounted within or powered within the basic PDP11/40 mounting box.

Table 1-1 (Cont)

Possible PDP-11/40 Variations

| Major Component | | Possible Variations |
|------------------------|---|---|
| DECwriter | **LA30 | Standard 97-character keyboard. Optional 128-character keyboard available. (LA30-S is a serial DECwriter and is controlled by a DL11 control; LA30-P is a parallel DECwriter and is controlled by an LC11 control.) |
| Teletype Unit | <p>**33 ASR</p> <p>33 KSR</p> <p>35 ASR</p> <p>35 KSR</p> | Each unit is available in 120V or 240V models. |
| Input Terminal Control | <p>DL11-A</p> <p>DL11-B</p> <p>DL11-C</p> <p>DL11-D</p> <p>DL11-E</p> | <p>Teletype, display, or LA30-S control</p> <p>EIA terminal control</p> <p>Teletype, display, or LA30-S control</p> <p>EIA terminal control</p> <p>Dataset control</p> |

Table 1-1 (Cont)

Possible PDP-11/40 Variations

Major Component

Possible Variations

KL11-B Similar to KL11-A. Differ
KL11-C primarily in baud rates as
KL11-E described in KL11 manual.
KL11-F

LC11 LA30-P DECwriter control

Power System

*H742 Power Supply (may be jumpered for either
120V or 240V, 50/60 Hz)

*H744 +5V regulator, 25A (two normally
supplied with basic system; additional
unit may be included to handle system
options)

*H745 -15V regulator, 10A (two)

Table 1-1 (Cont)

Possible PDP-11/40 Variations

Major Component

Possible Variations

*860 Power Control - mounted in top of cabinet. Two versions available:

860A - requires 120V input

860B - requires 240V input

Mounting Box

*BA11-FC Mounting Box

* An asterisk indicates that this is the normal configuration shipped with the basic machine, unless otherwise specified by the customer.

** Either the LA30 DECwriter or the Teletype Unit may be used as the basic PDP-11/40 System input/output device.

1.3 FUNCTIONAL DESCRIPTION

The PDP-11/40 is a 16-bit, general-purpose, parallel-logic, microprogrammed computer using 1- and 2-address instructions and 2s complement arithmetic. The system contains a variable instruction length processor, which directly addresses all of core memory. All communication among system components (including processor, core memory, and peripherals) is performed on a single high-speed bus, the Unibus. Because of the bus concept, all peripherals are compatible, and device-to-device transfers can be accomplished at the rate of 2,500,000 words-per-second. All peripherals are in the basic system address space; therefore, all instructions are I/O instructions. All system components and peripherals are linked by the Unibus and power connectors.

Subsequent paragraphs present a brief functional description of basic PDP-11/40 System components. A functional description of all processor options is presented in Chapter 4 of this manual.

1.3.1 Unibus

The Unibus is a single high-speed bus that provides communication between system components. The Unibus, with bidirectional data, address, and control lines, allows data transfers between all units on the bus with control of the bus an important factor in these transfers. The fixed repertoire of bus operations is flexible enough for speed and design economy, yet provides a fixed specification for interfaces. The asynchronous nature of these operations also eases design and operation. The repertoire of bus operations is:

DATI, DATIP, DATO, DATOB - data operations

INTR, PTR (BR, NPR) - control operations

Full 16-bit words or 8-bit bytes of information can be transferred on the bus between the master and slave. The DATI, DATIP operations transfer data into the master; the DATO, DATOB operations transfer data out of the master. When a device is capable of becoming bus master and requests use of the bus, it is generally for one of two purposes: to make a direct memory access (DMA) transfer of data directly to, or from, another device without processor intervention; or to interrupt (INTR) program execution and force the processor to branch to a specific address where an interrupt service routine is located.

Bus control is obtained under a non-processor request (NPR) for the direct memory access (DMA) or under a bus request (BR)

for an interrupt (INTR). A device can perform a DMA after acquiring bus control by a BR: bus control acquisition is at a lower priority.

Requests for the bus can be made at any time on the bus request (BR) and non-processor request (NPR) lines. Transfer of bus control from one device to another is made by the processor priority arbitration logic which grants control of the bus to the device having the highest priority. The NPR's are serviced before and directly after Unibus data cycles, in addition to specific times during WAIT or TRAP sequences. The BR's are serviced at the end of the instruction if the requesting priority exceeds that of the processor.

The processor has a special role in bus control operations as it performs the priority arbitration to select the next bus master. The processor assumes bus control when no other device has control.

The Unibus originates in the processor with the Internal Unibus and Terminator module (M981) that carries the Unibus from the processor to the next system unit. All 56 Unibus signals and 17 grounds are carried in this one module. In addition, a 120-conductor Flexprint cable may be used to connect system units in different mounting boxes or to connect a peripheral device removed from the mounting box.

A complete description of the Unibus, including specifications,
is presented in the PDP-11 Peripherals and Interfacing
Handbook.

1.3.2 KD11-A Processor

The KD11-A Processor decodes instructions, modifies data, makes decisions, and controls allocation of the Unibus among external devices. The processor contains eight hardware programming registers which are used as arithmetic accumulators, index register, autoincrement and autodecrement registers, and stack pointer registers. Two registers are specifically used for the processor: s program counter (PC) and stack pointer (SP).

Because of the flexibility of hardware registers, address modes, instruction set, and direct memory access, PDP-11/40 programs are written in directly relocatable codes. The processor also includes a full complement of instructions that manipulate byte operands, including provisions for byte swapping. Either words or bytes may be displayed on the programmer's console.

Any of the eight internal registers can be used to build last-in, first-out stacks. One register serves as a processor (or machine) stack pointer for automatic stacking. This stack handling capability permits save and restore of the program counter and status word in conjunction with subroutine calls and interrupts. This feature allows true reentrant codes and automatic nesting of subroutines. Addition of the KJ11 Stack Limit Register Option permits alteration of the stack overflow limit and provides both warning (yellow) and fatal (red) stack error indications.

The Unibus is used by the processor and all peripheral devices; therefore, there must be a priority structure to determine which device becomes bus master. A device generally requests use of the bus to make a nonprocessor transfer of data directly to or from memory, or to interrupt program execution and force the processor to branch to an interrupt service routine. A nonprocessor request (NPR) is granted by the processor at the end of bus cycles and allows device-to-device data transfers without processor intervention. A bus request (BR) is granted by the processor at the end of an instruction and allows the device to interrupt the current processor task. The entire instruction set is then available for manipulating device registers.

The processor recognizes four levels of hardware bus requests; each major level contains sublevels. Many devices can be attached on each major level with the device that is electrically closest to the processor given priority over other devices on the same priority level. The priority level of the processor itself is programmable within the hardware levels; therefore, a running program can select the priority level of permissible interrupts.

Additional speed and power are added to the interrupt structure through the use of the PDP-11/40 fully vectored interrupt scheme. With vectored interrupts, the device identifies itself, and a unique interrupt service routine is automatically selected by the processor. This eliminates device polling, and permits nesting of device service routines. The device interrupt

priority and service routine priority are independent to allow dynamic adjustment of system behavior in response to real-time conditions.

The address mapping of the system is dependent on the three most significant bits of the 16 bits in the KD11-A processor address for the basic processor. If these bits are all 1s, the two most significant bits of the Unibus address are forced to 1s; otherwise, the two most significant bits of the 18-bit Unibus address are forced to 0s. The KT11-D Memory Management Option converts these 16-bit addresses into full 18-bit physical Unibus addresses.

A detailed description of the processor is presented in the KD11 Processor Manual, DEC-11-HKDAA-A-D.

1.3.3 KY11-D Programmer's Console

The KY11-D Programmer's Console provides the programmer with a direct system interface. The console allows the user to start, stop, load, modify, step, or continue a program. Console displays indicate data and address as well as which device is controlling the bus; thus, operations can be monitored.

The programmer's console interacts with the processor, with microprogram control for the processor operation located in the processor. The console contains only indicators (light emitting diodes), switches, and the contact bounce filtering circuits for the control switches. Console operation does require certain Unibus operations through the processor: DATO for DEP and DATI for EXAM. For single-step operation, the processor responds to a console bus request (CBR). The CBR priority supersedes all other BR priorities. Note that use of the KM11 Maintenance Console option provides further display of machine states and allows single microstate stepping.

The programmer's console is mounted as the front panel of the BA11-FC mounting box and is connected to the processor by means of two cables.

Console operation, including descriptions of all controls and indicators, is presented in Chapter 3 of this manual. Detailed descriptions of console logic circuits are covered in the KD11 Processor Manual, DEC-11-HKDAA-A-D.

1.3.4 MF11-L Core Memory

The MF11-L Core Memory used in the PDP-11/40 System is a random access, coincident current, magnetic core, read/write memory with a cycle time of 900 ns and an internal access time of 350 ns. The memory consists of ferrite cores wired in a planar 3-D, 3-wire configuration that uses a shared sense/inhibit line. The basic memory unit consists of the backplane and three modules capable of storing 8192 (8K) 16-bit words. Provision for additional memory is made by this 9-slot, 2-system unit equivalent backplane. Two MM11-Ls, each consisting of three modules providing 8192 (8K) words, can be added.

The core memory uses the Unibus for data transfers to and from the processor and other devices; however, core memory is never bus master. Because the memory is always a slave device, a DATO or DATOB indicates information transferred out of the master into the memory. Because of the Unibus structure, the memory can be directly addressed by the processor or any other master device; every location in core can function as a true arithmetic accumulator.

The memory does not enter the priority structure because it is never bus master. The master device, however, can request use of the memory through either a bus request (BP) or a non-processor request (NPP). Because the memory is completely independent of the processor, any master device can perform direct data transfers with memory without processor intervention.

A detailed description of the memory is presented in the ME11-L Core Memory manual, DEC-11-HMELA-A-D. Note that the ME11-L is basically an MF11-L with the addition of a mounting box and power supply.

Note that the instruction timing specified for the PDP-11/40 System applies only for the MF11-L and MM11-S memories. These memories employ a special MSYN signal between the processor and the memory housed in the same mounting box.

1.3.5 Optional Memory Systems

There are two types of optional memory systems that may be used with the PDP-11/40 System: core memories similar to the MM11-L, and core memories used with other members of the PDP-11 family.

There are four memory systems similar to the MM11-L. The prime difference is packaging. These four memories are:

- MM11-L - 8K by 16 bit, 900 ns cycle time, modules and stack only.

- MF11-L - MM11-L memory plus backplane accomodating three MM11-L memories in a double system unit.

- ME11-L - Complete memory system consisting of MM11-L memory, backplane, mounting box, and power supply.

- MM11-S - MM11-L memory singularly in a single system unit.

There are five core memories designed for use with the PDP-11/20 System that may be used, if desired, with the PDP-11/40 System provided they are powered by H720 type power supplies. These memories are:

- MM11-E - 4K by 16 bit, 1.2 us access time
- MM11-F - 4K by 16 bit, 950 ns access time
- MM11-FP - an MM11-F with parity option included
- MM11-H - 1K by 16 bit, 950 ns access time
- MM11-J - 2K by 16 bit, 950 ns access time

Both the MM11-E and MM11-F memories may be expanded up to 28K in 4K increments. Each 8K segment may be interleaved.

1.3.6 DECwriter System

The LC11 DECwriter System is a high-speed teletypewriter system designed to interface with the PDP-11 family of processors to provide both input (keyboard) and output (printer) functions for the system. It can be used as the console input/output device. The system can receive characters from the keyboard or can print at speeds up to 30 characters per second in standard ASCII formats. The LC11 System consists of two distinct components: an LA30 DECwriter and a DEC PDP-11 interface unit, which is referred to as the LC11 Controller.

The LA30 DECwriter is a dot matrix impact printer and keyboard for use as a full-scale hard copy I/O terminal teletypewriter. The keyboard is either 97 or 128 characters. The print set is 64 ASCII characters, 80 characters per line, 10 characters per inch.

The LC11 Controller is the interface between the DECwriter and the PDP-11 Unibus. It controls data transfers between the DECwriter and other devices in the system. It also monitors print status, indicates when the keyboard buffer is full, and enables the interrupt logic.

The LC11 controller consists of a single quad module that can be mounted in the processor small peripheral controller slot. The LA30 DECwriter is covered in detail in the LA30 DECwriter manual,

DEC-00-LA30-DA and the LC11 is covered in the LC11 DECwriter System manual, DEC-11-HLCB-D.

Note that the LC11 Controller is only used with the LA30-P parallel word DECwriter. If an LA30-S serial word DECwriter is used, it is controlled by the DL11 interface.

1.3.7 DL11 Asynchronous Line Interface

The DL11 Asynchronous Line Interface provides an interface between a communications device, such as a Teletype, and the PDP-11/40 Unibus. Serial information read or written by the device is assembled or disassembled by the control for parallel transfer to, or from, the Unibus. The control also formats the data from the Unibus so that it is in the format required by the device. The interface provides the flags that initiate these data transfers and cause a priority interrupt to indicate the availability of the device. The DL11 is used when a Teletype is used as a system input/output device. It is also used with other types of communications devices such as datasets.

The interface transfers data via processor DATI and DATOB bus cycles. Although a DATO can be used, normal operation consists of a DATOB transfer because the device and the interface handle byte, rather than word, data. The interface can acquire bus control by a bus request (BR) and is normally set at the BR4 priority level. Because the interface operates by a means of an interrupt, no non-processor request (NPR) can be made.

There are five available DL11 interface options (DL11-A through DL11-E) in order to provide the flexibility needed to handle a variety of terminals. For example, the user can select an option for interfacing a Teletype or display keyboard, for handling EIA data, or for handling dataset devices. In addition, depending

on the option used, the user has a choice of line speeds, character size, stop-code length, and parity.

The DL11 interface consists of a single quad module. This module contains address selection logic for decoding the incoming bus address, an interrupt control for generating the interrupt, and receiver/transmitter logic that performs the conversion and formatting functions. The interface can be mounted in a standard processor small peripheral controller slot.

A detailed description of the DL11 interface is presented in the DL11 Asynchronous Line manual, DEC-11-HDLAA-A-D.

1.3.8 Power System

The PDP-11/40 Power System provides power for the basic system and for expansion units (e.g., extra memory or device interfaces) mounted within the basic BA11-FC mounting box. Expansion within the box is limited by space and available power.

The basic power system consists of a base H742 power supply, two H745 -15V regulators, and two H744 +5V regulators. There is additional space in the H742 base power system for an additional power regulator unit (either H744 or H745) depending on the requirements of the particular system.

All regulated outputs are protected with current limiting circuits. In addition, a crowbar overvoltage circuit protects the +5V output and the -15V output. An unregulated, partially filtered +5V output is supplied for the indicators on the programmer's console.

In addition to voltage, other outputs are provided by the power system: a line frequency signal, a DC LO logic signal, and an AC LO logic signal. The line frequency signal, which is a sine wave clipped at both ground and +5V, is used by the line frequency interrupt clock option (KW11-L) within the processor. The DC LO signal indicates that the dc voltage outputs are not at the proper value; the AC LO signal indicates insufficient ac voltage.

The basic power system is controlled by a cabinet-mounted 860 power control unit. This power control unit provides thermal and overload protection for the base power supply. Overloads in the switched ac line are handled by a circuit breaker and a thermal switch removes input power in the event of excessive heat or fire. The power control, which is controlled by the OFF/PWR/PANEL LOCK switch on the console, applies power to the base H742 power supply and to the cabinet ac power connectors.

1.4 APPLICABLE DOCUMENTATION

PDP-11 documents related to the PDP-11/40 System are listed in Table 1-2 in two main categories: general handbooks and PDP-11/40 System manuals. System manuals cover the hardware manuals specifically related to the PDP-11/40 and have associated engineering drawings. General documentation covers overall PDP-11 system descriptions, instruction set, addressing modes, basic logic modules, Unibus description, interfacing information. Also covered is general software documentation covering basic programs necessary for developing, loading, running, and diagnostic applications. A current list of other available programs may be obtained from the DEC program library.

Both the PDP-11/40 series of manuals and the general handbooks must be used together for a complete understanding of PDP-11/40 systems. The prime subject of this series is the processor and related internal options unique to the PDP-11/40 system. Other handbooks discuss the Unibus used to connect the processor to peripherals, the peripherals themselves, and programming information. A detailed hardware description of each peripheral is provided in its associated hardware maintenance manual supplied with the peripheral.

Table 1-2

Applicable Documents

| Title | Associated Drawing Set | Description |
|--|---------------------------|---|
| PDP-11/40 Processor Handbook DEC, 1972 | N/A | A general PDP-11/40 System handbook covering system architecture, addressing modes, the instruction set, pro- gramming techniques, memory management, internal processor options, console operation, and system specifications. |
| PDP-11 Peripherals and Interfacing Handbook DEC, 1972 | N/A | A general peripheral interface handbook. The first part is devoted to a discussion of the various peripherals used with PDP-11 Systems. The second part provides detailed theory, flow, and logic (continued next page) |

Table 1-2 (Cont)

Applicable Documents

| Title | Associated Drawing Set | Description |
|------------------------------|---------------------------|---|
| Logic Handb ook DEC, 1972 | N/A | descriptions of the Unibus and external device logic; methods of interface construction; and examples of typical interfaces. Presents functions and specifications of the M-series logic modules and accessories used in PDP-11 inter- facing (includes other types of logic produced by DEC but not used with the PDP-11. |

Table 1-2 (Cont)

Applicable Documents

| Title | Associated Drawing Set | Description |
|---|---------------------------|--|
| Paper-Tape Software Programming Handbook DEC-11-GGPB-D | N/A | Detailed discussion of the PDP-11 soft- ware system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output pro- gramming; and the floating point and math package. |
| PDP-11/40 System Manual DEC-11-H405A | PDP-11/40 Systems | A general intro- duction to the basic PDP-11/40 system including sections on in- stallation, operation, and the instruction set. Also provides detailed information, including maintenance, of the system power supply. |

Table 1-2 (Cont)
Applicable Documents

| Title | Associated Drawing Set | Description |
|--|---------------------------|---|
| KD11 Processor Manual DEC-11-HKDAA-A-D | PDP-11/40 Systems | Block diagram discussion, flow diagram discussion, theory of operation, and maintenance for the KD11-A processor, KY11-D programmer's console, KJ11 stack limit register option, KW11-L line frequency clock option, and KM11 maintenance console option. |
| ME11-L Core Memory Manual DEC-11-IMELA-A-D | PDP-11/40 System | General description, detailed description, and maintenance of the MM11-L core memory. (Note that ME11-L is the memory system; MM11-L the basic (continued next page) |

Table 1-2 (Cont)

Applicable Documents

| Title | Associated Drawing Set | Description |
|---|---------------------------|--|
| DL11 Asynchronous Line Interface Manual DEC-11-HDLAA-A-D | PDP-11/40 System | <p>core memory. The MF11-L uses the backplane and core memory of the ME11-L without the box and power supply.</p> <p>Installation, configuration, programming, and theory of operation of the DL11 interface. Covers DL11-A through DL11-E. The DL11-A or C is normally used as a control for the Teletype of LA30-S DECwriter but the DL11 can be used for a variety of communications devices.</p> |

Table 1-2 (Cont)
Applicable Documents

| Title | Associated Drawing Set | Description |
|--|--|--|
| KE11 Instruction Set Options Manual DEC-11-HKEFA-A-D | KE11-E Extended Instruction Set (EIS) Option and KE11-F Floating Instruction Set (FIS) Option | Algorithms, data programming, theory of operation, and maintenance for the KE11-E Extended Instruction Set (EIS) option and the KE11-F Floating Instruction Set (FIS) option. |
| KT11-D Memory Management Option Manual DEC-11-HKTDA-A-D | KT11-D Memory Management | Operation, programming, and detailed theory of operation for the KT11-D Memory Management option. |

Table 1-2 (Cont)

Applicable Documents

| Title | Associated Drawing Set | Description |
|---------------------------------|---------------------------|--|
| LA30 DECwriter Manual | DEC-00-LA30-DA | Presents a detailed discussion of the DECwriter including installation, operation, principles of operation, maintenance, troubleshooting, and engineering drawings. |
| LC11 DECwriter System Manual | DEC-11-HLCB-D | Provides general and detailed descriptions, programming, and operation for the LC11 DECwriter interface. The LC11 is used when an LA30-P (parallel) DECwriter is used as a system input/output device. |

Table 1-2 (Cont)
Applicable Documents

| Title | Associated Drawing Set | Description |
|--|--|--|
| KL11 Teletype Control Manual | DEC-11-HR4C-D | Provides general and detailed descriptions, programming, ad- justments, and main- tenance for the KL11 Teletype Control that may be used instead of the DL11 Control. |
| Automatic Send- Receive Sets, Manual | Bulletin 273B, two volumes, Teletype Corp. | Describes operation and maintenance of the Model 33 ASP Teletype unit that can be used as an input/output device with the PDP-11/40 System. Comparable manuals available for other Teletype models. |

Table 1-2 (Cont)

Applicable Documents

| Title | Associated Drawing Set | Description |
|--|-----------------------------------|--|
| Model 33 Page Printer Set, Parts | Bulletin 1184B, Teletype Corp. | Contains an illustrated parts breakdown to serve as a guide for dis- assembly, reassembly, and parts ordering for the Model 33 ASR Teletype Unit. Comparable manuals available for other Teletype models. |

1.5 ENGINEERING DRAWINGS

A complete set of engineering drawings and module circuit schematics is provided with each PDP-11/40 System. These prints sets were noted in Table 1-2 of paragraph 1-4 either under a Drawing Directory reference or as a second volume to the Maintenance Manual. The engineering drawings are necessary and interrelate with the manual discussion. The DDI (Drawing Directory Index) provides a list of prints included in the set and includes drawing number, title, and revision numbers. An X in the column labeled CUSTOMER PRINT SET indicates each drawing that is provided for the customer. The 1972 DEC Logic Handbook contains general logic symbols used on DEC drawings. A more detailed discussion of drawing set conventions is contained in the KD11 Processor Manual, DEC-11-HKDAA-A-D with this convention directly applicable to the processor and processor options of the PDP-11/40.

An overall corporate convention is useful in identifying prints and is noted below:

D-CS-M7233-0-1

Original drawing size

Series

Drawing type

Manufacturing variation
Module type, equipment
type, or a 7-digit
DEC part number.

CS: Circuit schematic
BS: Block schematic
BD: Block diagram
FD: Flow diagram
DD: Drawing directory
MU: Module utilization
AD: Assembly drawing
UA: Unit Assembly
WL: Wire list
PL: Parts list
AL: Accessory list

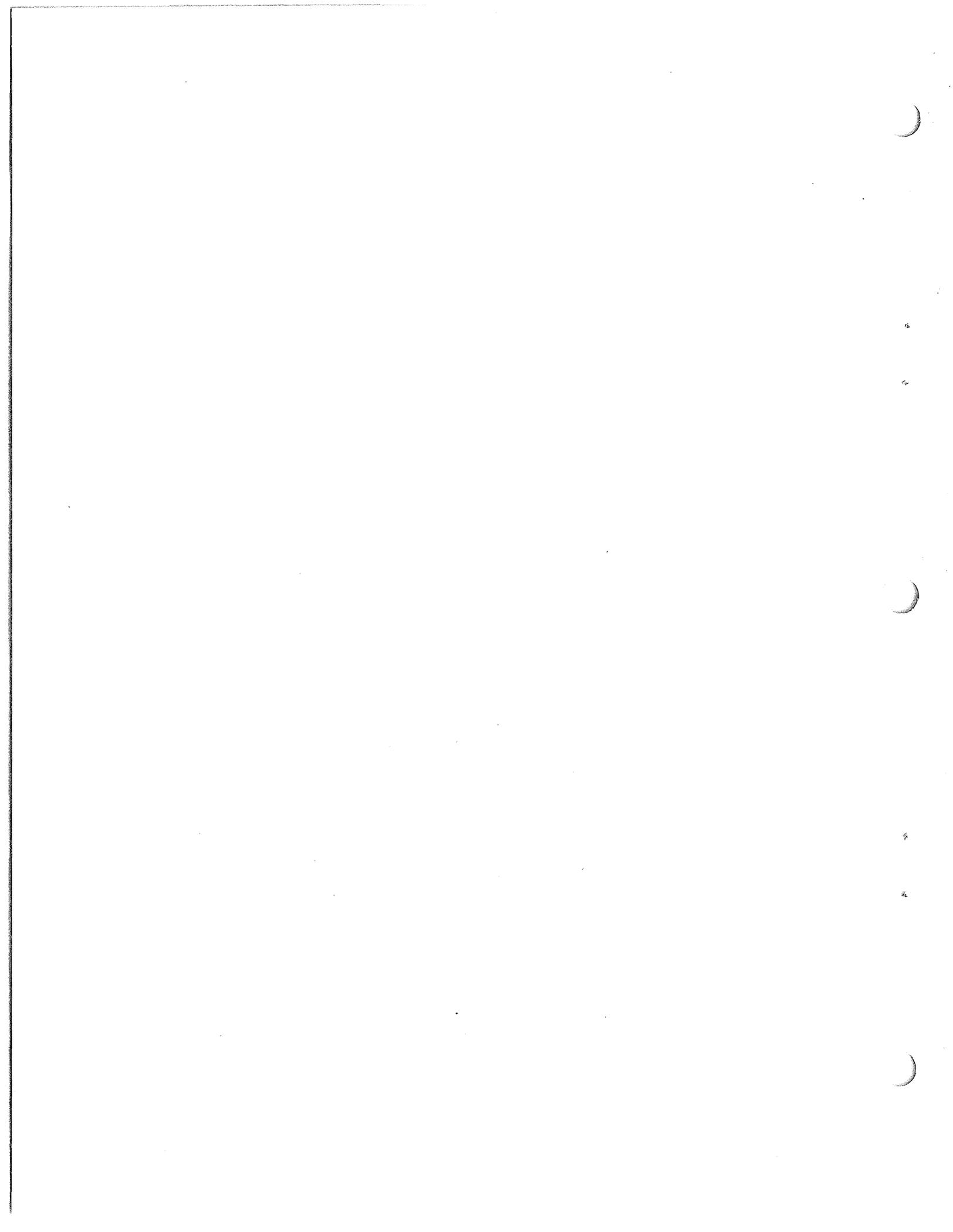
In addition to the basic drawing number, a second type of number is used with logic drawings. It consists of a 3-digit number located in the title block. For example:

KT-3

KT11-D Option drawing set

Sheet 3 of this specific drawing set

The processor drawing set uses a number designation for each module. Thus, K2-4 indicates sheet 4 of the K2 drawing set. K2 indicates the U WORD drawing set. Processor drawing set designations are listed in the KD11-A Processor Manual along with a description of the flow chart and logic diagram conventions.



CHAPTER 2 INSTALLATION

2.1 SCOPE

This chapter provides installation information and recommendations to ensure proper installation, and subsequent operation of the PDP-11/40 System.

Only installation of the basic PDP-11/40 System and processor options is included in this chapter. A section on installation of peripherals is not provided because of the modular and Unibus concepts of the system. To install a peripheral, for example, it is usually only necessary to insert the interface module(s) into the basic system mounting box and connect appropriate cabling between the interface and the peripheral. Installation and maintenance of the peripheral itself is normally covered in associated manuals.

It is recommended that sufficient time be given to site planning and preparation with particular attention given to the user's specific system configuration especially if a large number of peripherals are part of the system.

There are two DEC documents that aid in proper site planning: the PDP-11 Configuration Worksheet and the PDP-11 Site Preparation Worksheet.

The configuration worksheet permits the user to lay out the system prior to ordering so that he is aware of drawer layout, cabinet layout, and Unibus interconnection. This ensures that the proper number of drawers and cabinets are used and that Unibus length is sufficient for the system.

The Site PREPARATION Worksheet permits the user to determine the power requirements, environmental preparations, and physical arrangement of his system. The worksheet provides data on operating environment, power requirements, service and access requirements, and physical specifications for the basic system and available peripherals.

A final layout plan should be approved jointly by the user and DEC prior to delivery of equipment. It is recommended that any modifications to the installation site be effected prior to shipment and installation of the system.

DEC Sales Engineers and Field Service Engineers are available for consultation and planning and it is recommended that a qualified DEC representative either install the system, or be present during the installation process.

2.2 SITE PREPARATION

Adequate site planning and preparation can greatly simplify the installation process, resulting in more efficient and reliable PDP-11/40 installation. DEC Sales Engineers and Field Service Engineers are available for consultation and planning with customer representatives regarding objectives, course of action, and progress of the installation. The information in this paragraph is provided primarily to permit review of the site planning.

2.2.1 Physical Dimensions

The overall dimensions and total weight of the particular PDP-11/40 System as well as dimensions, weights, and cable lengths of any optional cabinets and free-standing peripherals should be known prior to shipment of the equipment.

The route the equipment is to travel from the customer receiving area to the installation site should be studied and measurements of doors, passageways, etc. should be taken to facilitate delivery of equipment. All measurements and floor plans should be submitted to the DEC Sales Engineer and DEC Field Service to ensure that the equipment is packed to suit the installation site facilities. Any restrictions (such as bends or obstructions in hallways, etc.) should be reported to DEC.

If an elevator is to be used for transferring the PDP-11/40 and its related equipment to the installation site, DEC should be notified of the size and gross weight limitations so that the equipment can be shipped accordingly.

Installation site space requirements are determined by the specific system configuration to be installed and, when applicable, provision for future expansion. To determine the exact area required for a specific configuration, a machine-room floor plan layout can be helpful. When applicable, space should be provided in the machine room for storage of

tape reels, printer forms, card files, etc. The integration of the work area with storage area can be considered in relation to the work flow requirements between areas.

In large installations where test equipment is maintained, DEC recommends that the test equipment storage area be within or adjacent to the machine room.

Operational requirements determine the specific location of the various options and free-standing peripherals of the system. Dimensions, weights and cable lengths of free-standing peripheral equipment must be known prior to installation; preferably during site preparation and planning. The system peripherals must not be located at distances from the basic system where connecting cables exceed maximum limits. The following points should be considered when planning the PDP-11/40 layout:

- a. Ease of visual observation of input/output devices by operating personnel.
- b. Adequate work area for installing tapes, access to console, etc.
- c. Space availability for contemplated future expansion.

- d. Proximity of the cabinets to peripherals.

- e. Proximity of cabinets and peripherals to any humidity controlling or air conditioning equipment.

The final layout should be reviewed by the DEC Sales Engineer, DEC Field Service, and in-house engineering personnel to ensure that cable limitations have not been exceeded and that proper clearances have been maintained.

2.2.2 Fire and Safety Precautions

The following fire and safety precautions are presented as an aid in providing an installation that affords adequate operational safeguards for personnel and system components.

- a. If an overhead sprinkler system is used, a "dry pipe" system is recommended. This type of system, upon detection of a fire, removes source power to the room and then opens a master valve to fill the room's overhead sprinklers.
- b. If the fire detection system is the type that shuts off the power to the installation, a battery-operated emergency light source should be provided.
- c. If an automatic carbon-dioxide fire protection system is used, an alarm should sound prior to release of the CO₂ to warn personnel within the installation.
- d. If power connections are made beneath the floor of a raised-floor installation, waterproof electrical receptacles and connections should be used.

e. An adequate earth ground connection should be provided for the protection of operating personnel.

2.2.3 Environmental Requirements

An ideal computer room type environment has an air distribution system which provides cool, well-filtered, humidified air. The room air pressure should be kept higher than that of adjacent areas to prevent dust infiltration.

2.2.3.1 Humidity and Temperature - The PDP-11/40 electronics are designed to operate in a temperature range of from 50 F (10°C) to 122°F (50°C) at a relative humidity of 20 to 95% without condensation. However, typical system configurations that use I/O devices such as magnetic tape units, card readers, etc., require an operational temperature range of from 60°F (15°C) to 80°F (27°C) with 40 to 60% relative humidity. Nominal operating conditions for a typical system configuration are a temperature of 70°F (20°C) and a relative humidity of 45%.

2.2.3.2 Air Conditioning - When used, computer room air-conditioning equipment should conform to the requirements of the "Standard for the Installation of Air Conditioning and Ventilating Systems (non-residential)", N.F.P.A. Number 90A; as well as the requirements of the "Standard for Electronic Computer Systems", N.F.P.A. Number 75.

2.2.3.3 Acoustical Damping - Some peripheral devices (such as line printers and magnetic tape transports) are quite noisy. In installations that use a group of high noise level devices, an acoustically damped ceiling reduces the noise. Operator comfort and efficiency is a major concern here.

2.2.3.4 Lighting - If cathode-ray tube (CRT) peripheral devices are part of the system, the illumination surrounding these peripherals should be reduced to enable the operator to conveniently observe the display.

2.2.3.5 Special Mounting Conditions - If the PDP-11/40 is to be subjected to rolling, pitching, or vibration of the mounting surface (e.g., aboard a ship), the cabinets should be securely anchored to the installation floor by mounting bolts. Since such installations require modifications to the system cabinets, DEC must be notified upon placement of the order so that necessary modifications can be made.

2.2.3.6 Static Electricity - Static electricity can be an annoyance to personnel and can, in extreme cases, affect the operational characteristics of the PDP-11/40 System and related peripherals. If carpeting is installed on the installation room floor, it should be of a type designed to minimize the effects of static electricity. Flooring consisting of metal panels, or flooring with metal edges, should be adequately grounded.

2.2.4 Electrical Requirements

The PDP-11/40 can be operated from a nominal 115V, 50/60 Hz or 230V, 50/60 Hz ac power source. The primary ac operational voltages should be maintained within the defined tolerances.

Line voltage tolerance should be maintained within 10% of the nominal value and the 50/60 Hz line frequency should not vary more than 3 Hz.

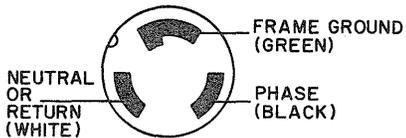
Primary power to the system should be provided on a line separate from lighting, air-conditioning, etc., so that computer operation is not affected by voltage surges or fluctuations.

The PDP-11/40 cabinet grounding point should be connected to the building power transformer ground or to the building ground point. Direct any questions regarding power requirements and installation wiring to the DEC Sales Engineer or Field Service Engineer.

Primary power outlets at the installation site must be compatible with the PDP-11/40 primary power input connectors. The PDP-11/40 basic system requires only one receptacle. Figure 2-1 shows the ac plug.

115V, OR 230V, 60Hz, SINGLE-PHASE, 30A
(PIN VIEW OF MALE PLUG)

NOTE:
Hubbell 2610
Nema L5-30P (plug)
L5-30R (receptacle)



11-1134

Figure 2-1 PDP-11/40 Connector



6

8



4

2



2.3 INSTALLATION PROCEDURES

The procedures presented in the following paragraphs are provided to assist in unpacking, inspection, and installation of the PDP-11/40 System and associated processor options.

CAUTION

Do not attempt to install the system until DEC has been notified and a DEC Field Service Representative is present.

2.3.1 Unpacking

Before unpacking the equipment, check the shipment against the packing list provided. Check that the correct number of packages has been delivered and that each package contains all the items listed on the accompanying packing slip. Also, check that all items on the accessories list in the Customer Acceptance Procedures have been included in the shipment. Unpack the cabinets as described in the following procedure.

Step

Procedure

- 1 Remove outer shipping container.

NOTE

The container may be either heavy corrugated cardboard or plywood. In either case remove all metal straps first and then remove any fasteners and cleats securing the container to the skid. If applicable, remove wood framing and supports from around the cabinet perimeter.

- 2 Remove the polyethylene cover from the cabinets.
- 3 Remove the tape or plastic shipping pins, as applicable, from the cabinet(s) rear access door(s).
- 4 Unbolt cabinet(s) from the shipping skid. Access to the bolts, located on the lower supporting siderails, is facilitated by opening the access door(s). Remove the bolts.
- 5 Raise the leveling feet so that they are above the level of the roll-around casters.

- 6 Use wood blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.
- 7 Roll the system to the proper location for installation.
- 8 If applicable, repeat Steps 1 through 7 for the expansion cabinets.
- 9 When the cabinets are oriented properly follow the procedure of Paragraphs 2.3.2 and 2.3.3 to install the cabinet(s).

2.3.2 INSPECTION

After removing the equipment packing material, inspect the equipment, and report any damage to the local DEC slaes office.

Inspect as follows:

| Step | Procedure |
|------|---|
| 1 | Inspect external surfaces of the cabinets and related equipments for surface, bezel, switch, and light damage, etc. |
| 2 | Remove the shipping bolts from the rear door, then open the rear door of the cabinet, and internally inspect the cabinet for console, processor, and interconnecting cable damage; loose mounting rails, loose or broken modules, blower or fan damage, any loose nuts, bolts, screws, etc. |
| 3 | Inspect the wiring side of the logic panels for bent pins, broken wires, loose external components and foreign material. |
| 4 | Inspect the power supply for proper seating of fuses and power connections. |

Step

Procedure

- 5 Inspect all peripheral equipment for internal and external damage. This includes inspection of magnetic tape and DECTape transport heads, motors, paper-tape sprockets, etc.

CAUTION

Do not operate any peripheral device which employs motors, tape heads, sprockets, etc., if they appear to be damaged in shipment.

2.3.3 Cabinet Installation

The PDP-11/40 cabinets are provided with roll-around casters and adjustable leveling feet. It is not necessary to bolt the cabinet to the mounting floor unless conditions indicate otherwise (e.g., shipboard installation). Cabinet installation procedures are as follows:

NOTE

In multiple cabinet installation, receiving restrictions may necessitate shipping cabinets individually or in pairs. In such cases the cabinets are connected at the installation site.

| Step | Procedure |
|------|---|
| 1 | With the cabinets positioned in the room, install H952-GA filler strips between cabinet groups (filler strips are shipped attached to the end of a cabinet group). Remove 4 bolts each from the front and rear filler strips. Butt the cabinet groups together while holding the filler strips in place and rebolt through both cabinets and the filler strips (see Drawing C-UA-H952-G-0). Do not tighten the bolts securely at this time. |

- 2 Lower the leveling feet so that the cabinet(s) are not resting on the roll-around casters but are supported on the leveling feet.
- 3 Use a spirit level to level all cabinets and ensure that all leveling feet are firm against the floor.
- 4 Tighten the bolts that secure the cabinet groups together and then recheck the cabinet leveling. Again ensure that all leveling feet are planted firmly on the floor
- 5 Remove the shipping bracket that secures the extendable BA11-FC Mounting Box in the cabinet.

2.3.4 Ac Power Connections

A 3-wire cable is used to connect the site source power to the power control in the top of the H960-C cabinet (see Figure 2-1 for connector type). The cable is connected at the factory for either 230V, 50 Hz or 115V, 60 Hz operation. Most cabinets in a PDP-11/40 system include a power control and a single ac power cable; power is distributed within the cabinet from the power control.

Power cables are intended to be connected to a site power system that provides ac power on a single-phase, 2-wire plus ground system. One of the two wires should maintain a constant (neutral) voltage, while the supply voltage is developed on the other (phase) wire.

The cabinets should be grounded to an earth ground, with ground straps connecting all the cabinets to each other. In addition, the frame ground wire in each power cable connects the cabinet ground system to the site power system ground.

The power controls in all the cabinets are connected together to provide a central control of power turn-on and turn-off. These connections require that the phase of the voltage supplied to each power control be the same as the phase of the voltage supplied to all other power controls in the same system.

Before connecting any power cables to the site source power, check all customer wiring. Ensure that power receptacles of the appropriate types have been provided for each cabinet, and that the receptacles are positioned close enough to the cabinet positions to allow connecting the cables without stretching or crossing the cables. In particular, check that the phase and neutral wires have been connected to the same pins in each receptacle, so that all cabinet power controls receive the same voltage phase.

2.3.5 Intercabinet Connections

When a multi-cabinet system is assembled, three types of electrical connections must be made between cabinets (see Paragraph 2.3.3 for mechanical connections). These connections are:

- a. Unibus connections - a BC11-A cable must connect the last system unit in a cabinet to the first system unit in the next cabinet.
- b. Remote power connections - all cabinet power controls are connected to a 3-wire control bus that provides for system turn-on and turn-off, and
- c. Ground strapping - the frame ground of the system is distributed through the cabinets by direct electrical connections between the cabinet frames.

2.3.5.1 Unibus Connections - To connect the Unibus between the H960-C cabinet and an H960-D Expansion Cabinet, insert the BC11-A cable in the rear system unit slot of the BA11-FC mounting box of the H960-C Cabinet. The cable then runs through a cable clamp in the upper left corner at the rear of the BA11-FC mounting box, and is passed under the power supply mounting rails into the next cabinet. In the H960-D cabinet, the cable passes through a similar cable clamp, and is inserted in the appropriate slot of the first system unit of the mounting box. The BA11-FC is noted above as an example, other mounting boxes might be the last box.

2.3.5.2 Remote Power Connections - Each cabinet in the system has one 860 power control. All the power controls are connected by a 3-wire bus that carries a remote turn-on signal, an emergency turn-off signal, and a control ground; there are three Mate-N-Lok connectors on each power control for the 3-wire bus. A cable is supplied with each cabinet to connect the power control of that cabinet to the next cabinet. Because each 860 power control must be capable of connecting to the 860 power controls in the preceding and following cabinets, two Mate-N-Lok connectors are reserved for the intercabinet cables. A third connector is provided for connection to the on/off switch, the thermal switch, or other emergency shut-off devices within the cabinet.

2.3.5.3 Ground Strapping - Electrical safety is provided by connecting all the cabinet frames to the ground level of the site power system. This is done by connecting a wire in each power cable between the frame and the power system ground; this is not a load carrying wire, and is intended only as an emergency ground path. The green wire in each power cable is the frame ground, while the white wire is the neutral, or return wire, that carries the load current.

To improve the level of safety provided by the frame ground connections, all cabinet frames are connected by braided copper straps of 4 AWG solid wire with crimp-on lugs, which are fastened to copper studs that are welded to the frames (this also prevents the generation of ground loops between cabinets that are connected by signal-carrying cables). The studs are welded to the bottom side rails of the cabinet frame, facing inward; the stud on the left side of the cabinet is slightly forward of center while the stud on the right side is slightly to the rear.

The ground strap supplied with each cabinet is fastened to one stud, passed over the side rail of that cabinet and the side rail of the adjacent cabinet, and fastened to the stud in that cabinet. The copper studs are threaded, and nuts are supplied on the studs.

2.3.6 Remote Peripheral Interconnection

Installation instructions for remote peripherals, such as line printers, card readers, and magnetic tape units, are covered in the appropriate peripheral maintenance manual. Normally, the peripheral itself is a free-standing unit and the peripheral controller is mounted in one of the system drawers. The controller and peripheral must be interconnected and the peripheral must also be connected to an ac power source.

In a basic PDP-11/40 System, there is a small peripheral controller mounting slot that houses the controller for the system input/output device (LA30 DECwriter or Teletype Unit). This device is characteristic of remote peripherals installation.

When installing the system, it is necessary to interconnect the system and the input/output device (Teletype or DECwriter) as described in the following steps:

| Step | Procedure |
|------|--|
| 1 | Place the freestanding DECwriter or Teletype in the desired position next to the system cabinet. |

Step

Procedure

- 2 Run the control cable from the DECwriter or Teletype unit through the back of the system cabinet and through the cable clamp at the rear of the mounting box. Note that, because of the size of the control cable connector, the cable clamp must first be removed before the connector is brought into the box. Once this is done, the clamp can be replaced.
- 3 Connect the control cable connector to the receptacle on the controller (DL11, KL11, or LC11) mounted in the small peripheral controller slot of the processor.
- 4 Verify that the controller module is plugged securely into the small controller slot.
- 5 Connect the power cable from the DECwriter or Teletype unit into one of the cabinet power receptacles.

2.3.7 Installation Verification

Prior to turning power on, proper installation of all processor internal options and memory should be verified. Although memory and processor options are installed in the system at the factory, installation should be verified at the site.

Installation verification procedures for the available processor options are given in Table 2-1. Verification procedures for core memory, as well as procedures for installing additional memory, are given in Table 2-2. A diagram of the memory system unit is shown in Figure 2-2.

Table 2-1

Option Installation Verification

| Option | Procedure |
|--|---|
| KE11-E Extended Instruction Set (EIS) Option | <ol style="list-style-type: none"><li data-bbox="678 499 1425 722">1. Verify that KE11-E module M7238 is installed in slot 2 (sections A-F) of processor backplane assembly.<li data-bbox="678 821 1425 1043">2. Ensure that jumper W1 on print K3-8 of KD11-A processor module M7233 (located in slot 5, sections A-F) has been removed.<li data-bbox="678 1142 1425 1680">3. Ensure that the three over-the-back cables have been connected to the 40-pin Berg connectors on the M7238 KE11-E module and the M7232 processor module (slot 3, section A-D). These cables provide the required logic interconnection between the processor and the KE11-E option. |

Table 2-1
Option Installation Verification

| Option | Procedure |
|--|---|
| KE11-F Floating Instruction Set (FIS) Option | <ol style="list-style-type: none"> <li data-bbox="800 512 1563 674">1. Verify that the KE11-E option has been installed. The KE11-E is a prerequisite for the KE11-F. <li data-bbox="800 772 1563 934">2. Verify that KE11-F module M7239 is installed in slot 1 (section A-D) of processor backplane assembly. <li data-bbox="800 1033 1563 1312">3. Ensure that the three jumpers on the KE11-E M7238 module have been removed. These must be removed to allow the KE11-F option to execute floating-point instructions. |

| Jumper | Print | Module |
|--------|-------|--------|
| W1 | KE-2 | M7238 |
| W2 | KE-5 | M7238 |
| W3 | KE-9 | M7238 |

Table 2-1 (Cont)

Option Installation Verification

| Option | Procedure |
|--|--|
| KT11-D Memory Management Option (requires the KJ11-A installation procedure also) | <ol style="list-style-type: none"><li data-bbox="699 478 1455 642">1. Verify that KT11-D module M7236 is installed in slot 8 (section A-F) of processor system unit.<li data-bbox="699 732 1455 1083">2. Verify that processor jumper changes have been made as indicated below (these changes are detailed in the installation section of the KT11-D option manual): |

Verify that the following jumpers have been removed:

| Jumper | Print | Module |
|--------|-------|--------|
| W10 | K1-6 | M7231 |
| W9 | | |
| W6 | K1-8 | M7231 |
| W5 | | |

Table 2-1 (Cont)
Option Installation Verification

| Option | Procedure | | |
|--------|-----------|-------|--------|
| | Jumper | Print | Module |
| | W1 | | |
| | W2 | K1-7 | M7231 |
| | W3 | | |
| | W4 | | |
| | W7 | K1-9 | M7231 |
| | W8 | | |

Verify that the following jumper has been moved:

| | | |
|----|------|-------|
| W2 | K4-4 | M7234 |
|----|------|-------|

Verify that the following have been added:

| | | |
|------|------|-------|
| C106 | K4-4 | M7234 |
| C107 | | |

Table 2-1 (Cont)

Option Installation Verification

Option

Procedure

KJ11-A Stack Limit Register

1. Verify that KJ11-A module M7237 is installed in slot E03 of the processor backplane.
2. Verify that the following processor jumpers have been changed:

| Jumper | Print | Module |
|--------|-------|--------|
| W2* | K1-8 | M7231 |
| W1 | K4-4 | M7234 |
| W1 | K5-4 | M7235 |

Jumpers are moved according to instructions on prints.

*Note that if the KT11-D option is present Jumper W2 of M7231 is removed completely.

Table 2-1 (Cont)

Option Installation Verification

| Option | Procedure |
|-----------------------------|---|
| KW11-L Line Frequency Clock | Verify that KW11-L module M787 is installed in slot F03 of the processor backplane. Verify that the backpanel wire between pin F03R2 and F03V2 for BG6 H has been removed. |
| KM11-A Maintenance Console | This option consists of a double-length module (W130/W131) that is plugged into slot F01 when used to monitor KD11-A operation, and slot E01 when used to monitor KT11-D, KE11-E, or KE11-F operation. Note that this option is not installed in the system during normal use. |

Table 2-2
Memory Verification or Installation

Memory

Procedure

MF11-L Core Memory (basic to PDP11/40) 1. Verify proper address selection on jumpers on CONTROL & DATA LOOPS(G110) module.

2. Verify that modules are installed properly:

| Module | Slot |
|----------------------------|----------------------|
| MEMORY STACK(H214) | 1, Sections C thru F |
| MEMORY DRIVERS(G231) | 2, Sections A thru F |
| CONTROL & DATA LOOPS(G110) | 3, Sections A thru F |

3. Verify Unibus interconnection to the KD11-A processor (M980) and interconnection or termination to rest of system (M920 or M930).

4. Verify that system unit power cable (D-IA-7009103-0-0) is connected from the system unit to MATE-N-LOK receptacles of the power distribution panel located on the BA11-FC mounting box. Connector P1 goes to 3; connector P2 goes to 4.

Table 2-2 (Cont)

Memory Verification or Installation

Memory

Procedure

5. Verify the interconnection of K4-4 MSYNA L signal from the KD11-A processor system unit (pin A0781) to MF11-L memory system unit (pin C01U1). Use twisted pair wire with grounding at nearest ground pin.

MM11-L Core

Memories

(additional

memories added

to MF11-L

memories)

1. Select proper address selection on jumpers on CONTROL & DATA LOOPS (G110) module.
2. Insert modules in either set of locations:

| Module | Slot |
|-----------------------------|----------------------|
| MEMORY DRIVERS (G231) | 4, Sections A thru F |
| CONTROL & DATA LOOPS (G110) | 5, Sections A thru F |
| MEMORY STACK (H214) | 6, Sections C thru F |

| Module | Slot |
|-----------------------------|----------------------|
| MEMORY DRIVERS (G231) | 7, Sections A thru F |
| CONTROL & DATA LOOPS (G110) | 8, Sections A thru F |
| MEMORY STACK (H214) | 9, Sections C thru F |

Table 2-2 (Cont)

Memory Verification or Installation

Memory

Procedure

3. Verify the interconnection by wire wrap of pins C03U1 to C04U1 and C06U1 to C07U1.

MF11-L Core
Memory
(expansion units
added to basic
PDP11/40)

1. Insert the MF11-L system unit into the BA11-FC mounting box using thumb screws provided.
2. Rearrange Unibus connections and termination using the M920 and M930, respectively. If memory is last unit in the mounting box use BC11-A cable for interconnection to a next box.
3. Verify proper address selections on jumpers on CONTROL & DATA LOOPS(G110) modules.
4. Insert modules according to locations noted for MF11-L Core Memory (basic) and MM11-L Core Memories (additional).

Table 2-2 (Cont)

Memory Verification of Installation

Memory

Procedure

5. A system unit power cable (D-IA-7009174-0-0) is used to connect the backpanel of the additional MF11-L to the power distribution panel's MATE-N-LOK receptacles. See paragraph 6.5.4 for power loading restrictions.

6. Connect the K4-4 MSYNA L signal from the previous MF11-L system unit (pin C09U1) to this additional MF11-L system unit (C01U1). Twisted pair wire with grounding at nearest pins should be used.

2.3.8 Initial Power Turn-On

Before turning power on, check the PDP-11/40 system as described in the following steps:

- | Step | Procedure |
|------|---|
| 1 | Ensure that all installation verification procedures (paragraph 2.3.7) have been performed. |
| 2 | Before plugging in the system ac power cables, disconnect the following Mate-N-Lok plugs in the basic H742 power supply wiring harness (see Figure 2-3): P1 through P7. Note that plugs P8 through P15 remain connected. |
| 3 | Turn off the circuit breaker on the 860 power regulator. (If more than one cabinet exists, turn off all 860 regulators.) |
| 4 | Plug in the ac power cable, turn on the circuit breaker, and check the dc voltages generated by the regulators. These voltages can be checked at pins of plugs P1 through P6. See drawing D-IC-11/40-0-2 for specific pin numbers. Check fan ac power on plug P7. |

Step

Procedure

- 5 Turn off the circuit breaker and re-connect all connectors (P1 through P7).

- 6 Turn on the circuit breaker and verify correct operation of the console OFF/POWER/PANEL switch.

- 7 Check the operation of all fans in the top of the mounting box.



2

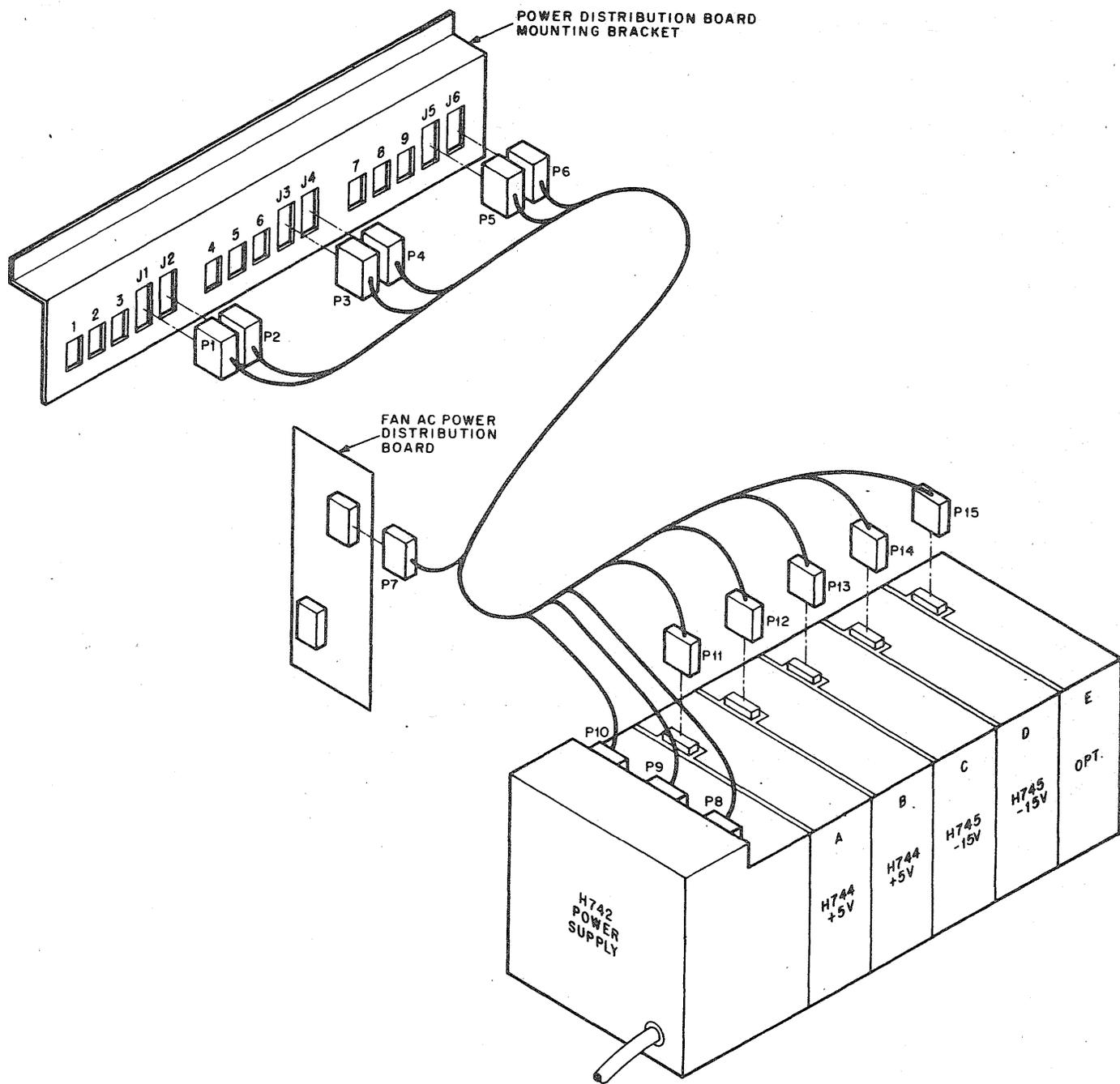
3



4

5





11-1385

Figure 2-3 D.C. CABLE HARNESS

2-45A

2.4 INITIAL OPERATION AND PROGRAMMING

Once the system has been installed and power applied, preliminary operating and programming procedures should be followed prior to using the system. Console operation, as well as the basic operating procedures noted in Chapter 3, should be performed first. If the user is already familiar with console operation, then the basic operating procedures given in paragraph 3.6 may be performed immediately. These procedures are necessary to, but independent from, the customer acceptance procedure noted in paragraph 2.5.

After initial operation, both procedures use a common set of system, peripheral, and individual instruction diagnostics. These programs, listed in Table 2-3, define initial acceptance and operation. They also provide for a continuing check on proper operation as well as permit analysis of system failures.

Table 2-3
PDP-11/40 Diagnostic Programs

| Number | Tests |
|-----------------------------------|---|
| PROCESSOR (INSTRUCTION SET) TESTS | |
| MAINDEC-11-DOAA | Unconditional branch |
| MAINDEC-11-DOBA | Conditional branch |
| MAINDEC-11-DOCA | Single operand instructions |
| MAINDEC-11-DODA | Single & double operand instructions |
| MAINDEC-11-DOEA | Rotate/Shift instructions |
| MAINDEC-11-DOFA | Compare with equal results |
| MAINDEC-11-DOGA | Compare with not equal results |
| MAINDEC-11-DOHA | Move instructions |
| MAINDEC-11-DOIA | Bit manipulation instructions (BIT,BIC,BIS) |
| MAINDEC-11-DOJA | Add instruction |
| MAINDEC-11-DOKA | Subtract instruction |
| MAINDEC-11-DOLA | Jump instruction |
| MAINDEC-11-DOMA | RTS, RTI, JSR instructions |
| MAINDEC-11-DCKBA-A | Sign extend instruction |
| MAINDEC-11-DCKBB | Subtract one and branch instruction |
| MAINDEC-11-DCKBC | Exclusive OR instruction |
| MAINDEC-11-DCKBD | Mark instruction |
| MAINDEC-11-DCKBE | Trap and interrupt return |
| MAINDEC-11-DBKDM | Trap instructions & error traps |
| MAINDEC-11-DOQB | T15 combined instruction test |

Table 2-3 (Cont)
PDP-11/40 Diagnostic Programs

| Number | Tests |
|---------------------|---------------------------------------|
| MEMORY TESTS | |
| MAINDEC-11-DZMMA | Address test up |
| MAINDEC-11-DZMMB | Address test down |
| MAINDEC-11-DZMMK | Up/Down address test for ACT-11 |
| MAINDEC-11-DZMMD | Basic memory patterns test |
| MAINDEC-11-DZMME | Moving 1s and 0s |
| MAINDEC-11-DZMMF | 1s susceptibility test |
| MAINDEC-11-DZMMG | Worst-case noise test |
| MAINDEC-11-DZMMI | Random data test |
| MAINDEC-11-DZQMB | Memory exerciser |
| MAINDEC-11-DZQMA | Extended memory exerciser |
| KE11-E (EIS) OPTION | |
| MAINDEC-11-DCKBL | Divide instruction |
| MAINDEC-11-DCKBK | Multiply instruction |
| MAINDEC-11-DCKBJ | Arithmetic shift combined instruction |
| MAINDEC-11-DCKBI | Arithmetic shift instruction |
| MAINDEC-11-DCQKA | MUL/DIV Exerciser |

Table 2-3 (Cont)
PDP-11/40 Diagnostic Programs

| Number | Tests |
|-----------------------------|-----------------------------|
| KE11-F (FIS) OPTION | |
| MAINDEC-11-DBKEA | Basic instruction tests |
| MAINDEC-11-DBKEB | Exerciser |
| MAINDEC-11-DBKEO | GTP overlay |
| KT11-D MEMORY MANAGEMENT | |
| MAINDEC-11-DBKTA | Basic logic test |
| MAINDEC-11-DBKTB | Access keys test |
| MAINDEC-11-DBKTC | MFPI/MTPI tests |
| MAINDEC-11-DBKTD | States test |
| MAINDEC-11-DBKTG | Memory management exerciser |
| MAINDEC-11-DBKTF | Abort test |
| KJ11-A STACK LIMIT REGISTER | |
| MAINDEC-11-DCKBF | Stack limit test |
| KW11-L LINE FREQUENCY CLOCK | |
| MAINDEC-11-DZKWA | Line frequency clock test |

2.5 CUSTOMER ACCEPTANCE

Verify correct system operation by performing the Customer Acceptance Procedures. The Customer Acceptance Procedures document is shipped with the PDP-11/40 System and lists all the tools, programs, and tests required to certify system operation.

3 SYSTEM OPERATION

3.1 SCOPE

This chapter provides the information necessary to operate and program the PDP-11/40 System and associated input/output terminal (Model 33 ASR Teletype or LA30 DECwriter). The description is divided into five major parts: programmer's console, DECwriter, Teletype, basic system operation, and basic system programming.

The description of controls and indicators for the consoles is in tabular form and provides the user with the type and function of each operating switch and indicator. Operating controls for peripheral devices that are not part of the basic machine are contained in the appropriate peripheral manual.

Basic step-by-step procedures for both manual and program operation are given in paragraph 3.5. Basic system programming is covered in paragraph 3.6.

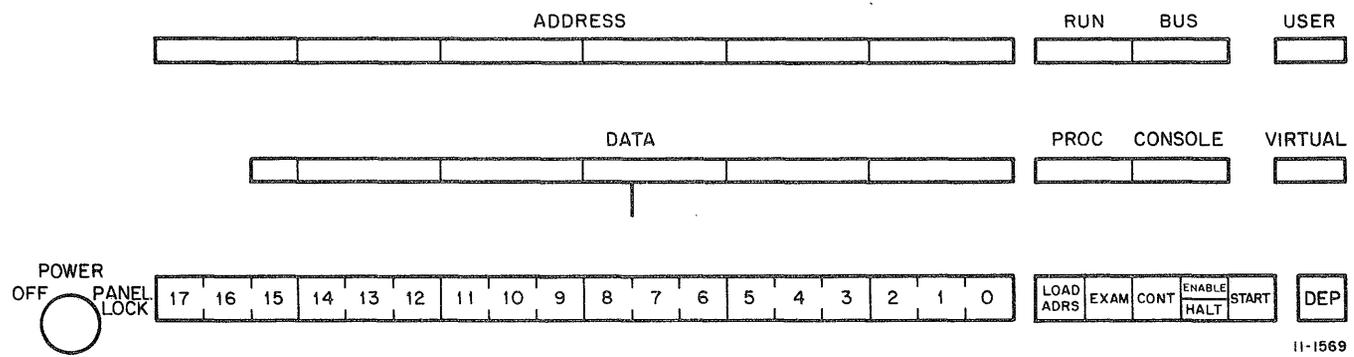
3.2 KY11-D PROGRAMMER'S CONSOLE

The KY11-D Programmer's Console (Figure 3-1) provides the PDP-11/40 System with a necessary and useful programmer's interface. Manual operation of the system is controlled by switches mounted on this console which is the front panel of the basic mounting box. Visual displays indicate processor operation and the contents of the address and data registers.

All register displays and switches, whether marked on the console panel or not, are numbered from right to left. The numbers correspond to the powers of two, i.e., 2^{15} 2^2 , 2^1 , 2^0 . Therefore, the most significant bit (MSB) is at the left of each specific register or display, the least significant bit (LSB) is at the right. Whenever an indicator is on, it denotes the presence of a binary 1 in the particular bit position. The alternate color coding on the console identifies the different functions or segments of the binary number in octal format.

In addition to the alternate color coding, the DATA register contains an index mark that divides the low-order byte (bits 0-7) from the high-order byte (bits 8-15). The high-order byte is divided into octal format by two more index marks. No marks are required for the low-order byte because octal coding for this byte is identical to the alternate color coding.

Figure 3-1 shows the location of all PDP-11/40 console controls and indicators. Each indicator and associated function is listed in Table 3-1. Each control and related function is listed in Table 3-2.



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Figure 3-1 PDP-11/40 Programmer's Console

Table 3-1

PDP-11/40 Console Indicators

| <u>Indicator</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|------------------|--|--|---|
| DATA | 16-bit display MSB at left Color-coded in 3-bit segments for octal format Byte division noted with additional indexing for octal format in upper byte | <p>Displays the output of a processor data multiplexer which gates information from a variety of sources within the processor. Normal programming use results in the following displays:</p> <p>HALT instruction has R(OO) RESET instruction has R(OO) WAIT instruction has R(IR) SINGLE STEP and HALT switch has processor status (PS)</p> <p>The display of the data multiplexer is especially important when used in the single clock mode. During this mode, the KMI1 maintenance console is used to step through a program a single micro-instruction at a time. In this instance, the information in the DATA display is the result of a single microword and shown on the processor flow diagrams (refer to KD11-A Processor Manual).</p> | <p>When console switches are used, information shown on the DATA display is as follows:</p> <p>LOAD ADRS - the transferred switch register information</p> <p>DEP - the switch register data just deposited. Note that data and address are correlated. The address is where this data was stored.</p> <p>EXAM - the information from the address examined. Note address and data correlation.</p> <p>HALT - displays the current processor status (PS) word.</p> <p>When a programmed HALT instruction is issued, bus control is transferred to the console and processor register, RC, is displayed on the DATA display. This allows program identification of halts.</p> <p>During direct memory access (DMA) operations, the processor is not involved in data transfer functions. Therefore, the data displayed in the DATA display is not that of the last bus operation.</p> |

Table 3-1
(continued)

| <u>Indicator</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|------------------|---|---|--|
| ADDRESS | 18-bit display MSB at left Color-coded in 3-bit segments for octal format | <p>Displays the address in the bus address register (BAR) of the processor. This varies with an instruction execution but for a HALT, WAIT, or single step operation, the program counter is displayed between operations. The updated (or incremented) value of the program counter is always displayed.</p> <p>If the KT11-D option is not included in the system, the two most significant bits (A17,A16) are ordered according to the lower 16 bits; they are set only when bits A15,A14, and A13 are all set. Addresses between 160000 and 177777, therefore, are translated to addresses between 760000 and 777777, respectively.</p> <p>If the KT11-D memory option is installed, the ADDRESS display usually displays a virtual address with the KT11-D providing an offset physical bus address (not displayed). During console operations, however, the console provides and displays a full 18-bit physical address.</p> | <p>When console switches are used, information shown on the ADDRESS display is as follows:</p> <p>LOAD ADRS - the transferred switch register information.</p> <p>DEP or EXAM - indicates the bus address just deposited into or examined.</p> <p>During a programmed HALT or WAIT instruction, the ADDRESS displays the incremented address of the instruction. The BAR is the instruction location plus 2.</p> <p>In single instruction mode, the next PC is placed into the BAR and displayed in ADDRESS between instructions.</p> <p>During direct memory access (DMA) operations, the processor is not involved in the data transfer functions, and the address displayed in the ADDRESS display is <u>not</u> that of the last bus operation.</p> <p>Within instructions, the display indicates various processor bus addresses. These values are apparent only in a maintenance mode, using the KM11 and single clocking.</p> |

Table 3-1
(continued)

| <u>Indicator</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|------------------|--------------|---|--|
| RUN | Single light | <p>When the RUN indicator is on, the processor clock is running and is operating on an instruction or looping in console operation.</p> <p>When the RUN indicator is off, the microprogramming is not processing an instruction. The processor may be in control of the bus and awaiting a response for a data transfer; or the processor may have relinquished bus control for an NPR or BR request.</p> | <p>During normal machine operation, the RUN light flickers on and off (indicated by a faint glow).</p> <p>A programmed RESET command turns off the RUN light. This also occurs between single clocks when the KM11 maintenance console is used.</p> <p>For programmed HALT and WAIT instructions, the clock continues to run with the processor looping in the microprogram. This is also true for console operation of the HALT switch.</p> |

Table 3-1
(continued)

| <u>Indicator</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|------------------|--------------|--|--|
| PROC | Single light | When lit, indicates that the processor is controlling the Unibus as the master device. | When the PROC light is on and the RUN light is off, the processor is waiting for data from the bus. These conditions indicate that the processor is in control of the bus (PROC on) but that the processor clock is off (RUN off). |
| BUS | Single light | When lit, indicates that some device has control of the Unibus. If the PROC indicator is lit, that device is the processor. | This display is useful for determining where bus control is and that it is present. |
| CONSOLE | Single light | When lit, indicates that the processor is in the console portion of the microflow. Control switch activation is sensed and acted upon. | |

Table 3-1
(continued)

| <u>Indicator</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|------------------|--------------|--|--|
| USER | Single light | When lit, indicates that the processor is in the user mode and certain KT11-D restrictions on instruction operation and processor status (PS) word loading exist. Refer to the KT11-D option discussion in chapter 4 and the KT11-D manual. | Does not function unless the KT11-D memory management option has been installed in the system. |
| VIRTUAL | Single light | <p>When lit, indicates that a virtual address is displayed in the ADDRESS display. This virtual address is usually modified by the KT11-D option to provide a different physical address for the Unibus. If the KT11-D option is installed, this display is usually active during program operation. During console operation, the console ADDRESS display and switch register both provide a full 18-bit physical address. The VIRTUAL light is off in this instance.</p> <p>When VIRTUAL light is off, it indicates that the bus address indicated by the ADDRESS display is the physical address.</p> | Does not function unless the KT11-D memory management option has been installed in the system. |

Table 3-2

PDP-11/40 Console Controls

| <u>Switch</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|--------------------------|------------------------------------|---|---|
| OFF/POWER/ PANEL LOCK | 3-position, key operated switch | Provides power control to console and lock-out of console controls as follows: <u>OFF position</u> - removes all power from the processor. <u>POWER position</u> - applies primary power to the processor. All console controls are fully operational when switch is in this position. <u>PANEL LOCK position</u> - disables all console (panel) controls except the switch register key switches. This prevents inadvertant switch operation from disturbing a running program. The data entered in the switch register is still available to the processor whenever the program explicitly addresses the switch register (address 777570). | System not being used Normal operation. Processor operating; console control disabled. |

Table 3-2
(continued)

| <u>Switch</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|-----------------|---|---|----------------|
| Switch Register | 18 key-type switches | Provides a means of specifying an address or data word into the processor. | |
| | Bit position of each switch is labeled; MSB is at left. | If the word contains data, it is loaded into the address specified by the ADDRESS REGISTER by lifting the DEP key. | |
| | Color-coded in 3-bit segments for octal format. | If the word in the switch register represents an address, it can be loaded into the ADDRESS REGISTER by depressing the LOAD ADRS key. | |
| | Up position - logical one (or on). Down position - logical zero (or off). | If the KT11-D memory management option is used, bits 17 and 16 are directly used as the physical bus address during console operation. | |
| | | If the KT11-D is <u>not</u> installed, the processor bus address bits 17 and 16 are set if switch register bits 15, 14, and 13 are all set. Bits 17 and 16 of the switch register have no effect. | |
| | | The contents of the switch register may be used by the processor any time the program explicitly addresses the register at address 777570. This address can only be used by the processor. | |

Table 3-2
(continued)

| <u>Switch</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|---------------|--|---|---|
| LOAD ADRS | Momentary key-type switch Depress to activate | The LOAD ADRS switch transfers the contents of the switch register to the bus address register (BAR) through a temporary location R(TEMPC) within the processor. This bus address, displayed in ADDRESS, provides an address for the console functions of EXAM, DEP, and START. | The address is loaded into a temporary location which is <u>not</u> modified during program execution. To restart a program, it is only necessary to depress the START switch. <u>NOTE</u> Double examine or deposit functions increments the value of the loaded address both in the BAR and in R(TEMPC). Attempts to examine or deposit an odd bus address (bit 00 enabled) cause bit 00 to be disregarded. For example, an attempt to examine address 1001 results in address 1000 being displayed. Byte data for location 1001 is located in DATA bit 15 through bit 08. |

Table 3-2
(continued)

| <u>Switch</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|---------------|--|--|--|
| EXAM | Momentary key-type switch Depress to activate | <p>The EXAM switch uses the contents of R(TEMPC) as a bus address; the contents of this bus address is displayed in DATA, the bus address is displayed in ADDRESS.</p> <p>A LOAD ADRS operation usually pre-establishes the initial R(TEMPC) address; sequential examines automatically update R(TEMPC).</p> <p>If the EXAM switch is depressed twice in succession, the contents of the next sequential bus address is displayed in DATA. This action is repeated each time EXAM is depressed provided no other switch is used between these steps.</p> <p>Whenever the LOAD ADRS or DEP switch is depressed, it destroys the incrementing sequence. The next time EXAM is used, it displays the current address rather than the next sequential address.</p> | <p>If an odd address is examined, bit 00 is ignored. For example, if address 1001 is examined, the address 1000 is displayed in ADDRESS.</p> <p>An EXAM operation that references a non-existent address causes a time out (with no TRAP) and the switch register address (777570) is displayed in DATA.</p> |

Table 3-2
(continued)

| <u>Switch</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|---------------|--|--|--|
| CONT | Momentary key-type switch Depress to activate | <p>Causes the processor to continue operation from the point at which it had stopped.</p> <p>If the ENABLE/HALT switch is in the ENABLE mode, CONT returns bus control from the console to the processor and continues program operation.</p> <p>If the ENABLE/HALT switch is set to HALT, depressing the CONT key causes the processor to perform a single instruction. Control is returned to the console after each instruction, permitting a program to be stepped through an instruction at a time.</p> | <p>If program stops, depressing CONT provides a restart without power clear.</p> |

Table 3-2
(continued)

| <u>Switch</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|---------------|-----------------------------|---|---|
| ENABLE/HALT | 2-position, key-type switch | <p>Allows either the program or the console to control processor operation.</p> <p>ENABLE position - permits the system to run in a normal manner. No console control requests are made. All switches except ENABLE/HALT and the switch register are disabled.</p> <p>HALT position - halts the processor after the next instruction or outstanding TRAP sequences, and before Unibus BR requests, and passes control to the console.</p> <p>The HALT mode is used with the CONT switch to step the machine through programs one instruction at a time.</p> <p>When the START switch is activated in the HALT mode, a system clear is effected without program start. This mode of operation is useful for clearing conditions in the system that might prevent proper operation. When the START switch is activated in the ENABLE mode, it provides a system clear with a program start.</p> | <p>Continuous program control requires the ENABLE mode.</p> <p>The HALT mode is used to interrupt program control, perform single instruction operation, or clear the system.</p> |

Table 3-2
(continued)

| <u>Switch</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|---------------|--|---|----------------|
| START | Momentary key-type switch Depress to activate initialize, release to have START function occur. | Depressing the START switch provides a system clear (initialize). When the ENABLE/HALT switch is set to HALT, the processor does not start. When ENABLE/HALT is set to ENABLE, releasing START begins processor operation. The starting address is that of the last console operation determined by R(TEMPC). Usually, this temporary location is loaded from the switch register by a LOAD ADRS operation. If the program stops at any time, it can be restarted at its original location by the START switch; the value of R(TEMPC) remains unchanged. Use of the START switch in the HALT mode provides for a system clear. This mode of operation is useful for clearing conditions that might prevent proper operation. | |

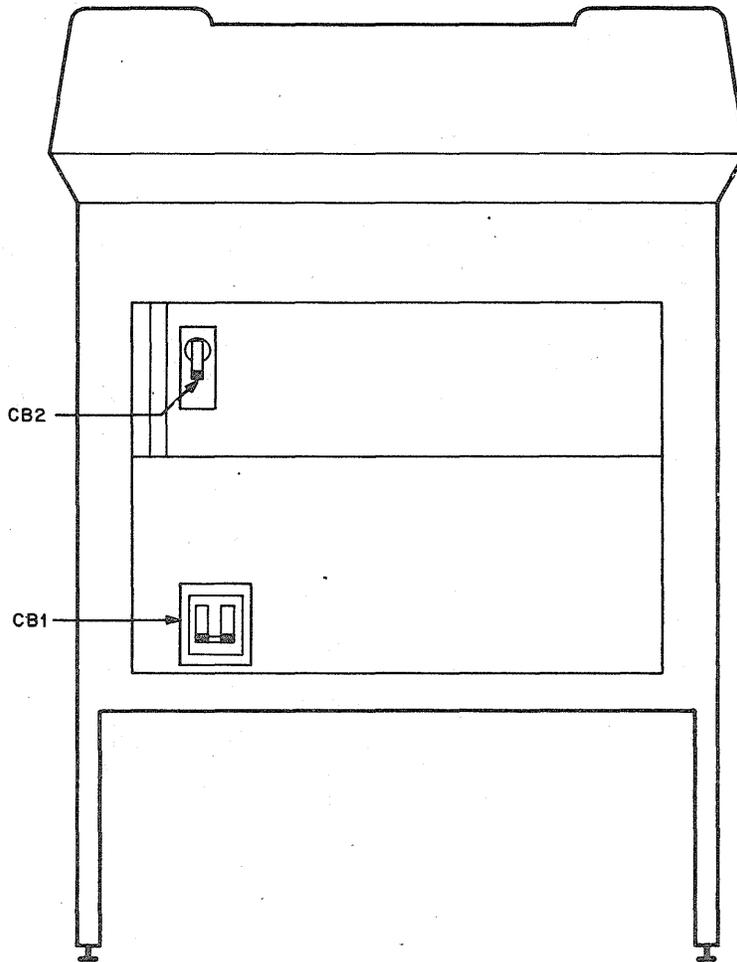
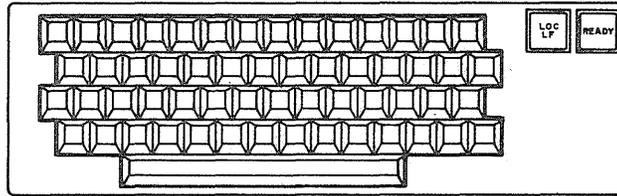
Table 3-2
(continued)

| <u>Switch</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|---------------|---|---|--|
| DEP | Momentary key-type switch Lift to activate | <p>The DEP switch uses the contents of R(TEMPC) as a bus address. The contents of the switch register are transferred to this location. After use, the data appears on the DATA display and the address is on the ADDRESS display.</p> <p>A LOAD ADRS operation usually pre-establishes the initial address; sequential DEP operations automatically update R(TEMPC).</p> <p>If the DEP switch is raised twice in succession, the contents of the switch register is deposited in the next sequential bus address location. This action is repeated each time DEP is raised provided no other switch is used between these steps. Whenever the LOAD ADRS or EXAM switch is depressed, it destroys the incrementing process. The next time DEP is used, it deposits the current address rather than the next sequential address.</p> | <p>If an attempt is made to deposit an odd address, bit 00 is ignored and a word deposit occurs.</p> <p>A deposit operation that references a non-existent address causes a time out (with no TRAP). No error message is visible from the console for a deposit to a non-existent address. An immediate verification by an examine operation, however, would result in the display of the switch register address in the DATA display.</p> |

3.3 DECWRITER

The LA30 DECwriter unit is one of the input/output devices that can be used with the PDP-11/40 System. Data can be entered into the processor via the keyboard or data from the processor can be printed out by the DECwriter.

Controls and indicators for the LA30 DECwriter are shown in Figure 3-2 and listed in Table 3-3. Further detailed operating information is contained in the LA30 DECwriter manual (DEC-00-LA30-DA) and in the LC11 DECwriter System manual (DEC-11-HLCB-D).



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Figure 3-2 DECwriter Controls

Table 3-3

LA30 Controls and Indicators

| <u>Control or Indicator</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|-----------------------------|--|--|----------------|
| READY indicator | single light (white) | When lit, indicates that power has been applied to the system and the DECwriter is ready for use in either an input (keyboard) or output (printer) mode. | |
| LOC LF switch | pushbutton switch with indicator | When depressed, advances paper as long as switch is held down. Keyboard and printer operation disabled during line feed. This is an off-line operation. | |
| CB2 | circuit breaker 2-position toggle switch | When set to on (up) position, applies power to printer stepping motor electronics. | |
| CB1 | circuit breaker double-pole, single throw | When set to on (up) position, applies primary power to the DECwriter. | |
| Keyboard | Typewriter-like layout 97 or 128 characters | Uses a typewriter-like keyboard to print characters on paper or to input information into the computer. The keyboard does not type directly into the printer; it simply sends the appropriate ASCII code to the controller for transmission to the Unibus. Therefore, an echo keyboard program must be used for typing directly on the paper. | |

3.4 TELETYPE

The model 33 ASR Teletype unit is one of the input/output devices that can be used with the PDP-11/40 System. Data can be entered into the processor via the keyboard or through a paper-tape reader. The Teletype can also be operated off-line to punch paper tapes. Controls for the Model 33 ASR Teletype are shown in Figure 3-3 and listed in Table 3-4. Further detailed operating information is contained in the Teletype Corporation manuals listed in Table 1-2 of this manual.

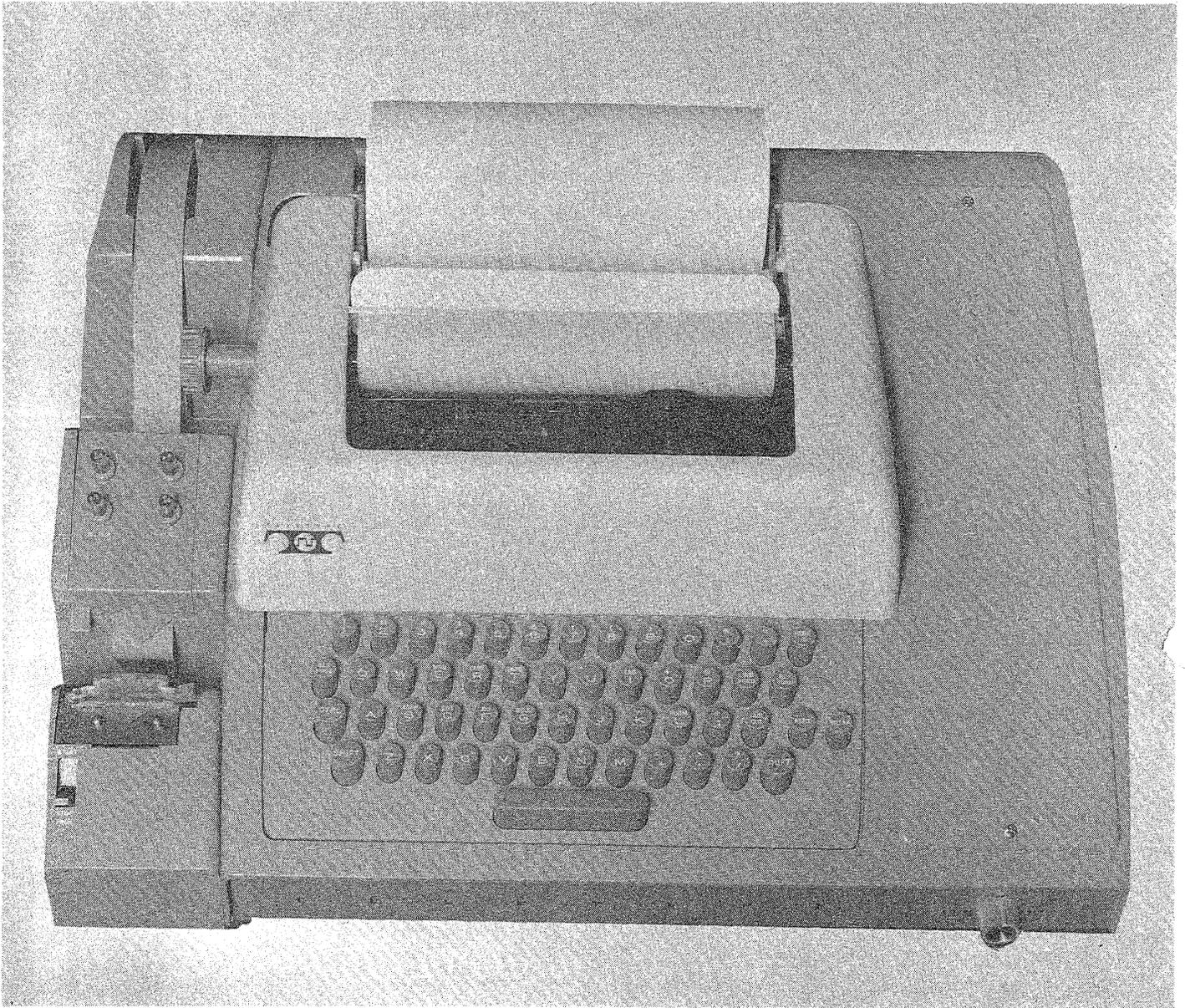


Figure 3-3 Teletype Controls

Table 3-4
Teletype Controls

| <u>Control</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|------------------|--|---|----------------|
| | | <u>PUNCH</u> | |
| REL. pushbutton | Momentary switch, depress to activate | Disengages the paper tape from the punch to allow loading or removal of tape. | |
| B.SP. pushbutton | Momentary switch, depress to activate | Backspaces the paper tape by one space each time the pushbutton is depressed to allow manual correction or rubout of character just punched. | |
| ON pushbutton | 2-position switch, connected to OFF pushbutton | When depressed, turns on the paper tape punch and releases OFF switch. | |
| OFF pushbutton | 2-position switch, connected to ON pushbutton | When depressed, turns off the paper tape punch and releases ON switch. | |

Table 3-4
(continued)

| <u>Control</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|----------------------------|-------------------|--|----------------|
| | | <u>READER</u> | |
| START/STOP/ FREE switch | 3-position switch | Controls operation of the tape reader. <u>START position</u> - engages tape reader which begins operation under program control. <u>STOP position</u> - engages reader mechanism but does not energize it. In effect, tape is locked in the reader but reading operation does not begin until the switch is moved to START. <u>FREE position</u> - disengages reader to permit loading and unloading of tape. | Used on-line |

Table 3-4
(continued)

| <u>Control</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|---------------------------|-----------------------------|--|----------------|
| LINE/OFF/ LOCAL switch | 3-position rotary switch | <p>Serves two functions: applies primary power to Teletype and connects computer to Teletype.</p> <p><u>LINE position</u> - energizes Teletype and connects it to the computer as an input/output device. Signals from either the Teletype reader or keyboard can be used as an input while the computer output can be used to control the keyboard or punch.</p> <p><u>OFF position</u> - deenergizes the Teletype by removing primary power.</p> <p><u>LOCAL position</u> - disconnects the Teletype from the computer. The Teletype can be used for punching or reading tapes but all control is localized at the keyboard.</p> | |

Table 3-4
(continued)

| <u>Control</u> | <u>Type</u> | <u>Function</u> | <u>Remarks</u> |
|----------------|---|--|----------------|
| Keyboard | 45 printing characters 6 non-printing characters Typewriter-like layout | <p>Uses a typewriter-like keyboard to print characters on paper, punch tape, or input information into the computer.</p> <p><u>Off-Line Operation (LOCAL)</u> - When tape reader and punch are off, prints characters on paper.</p> <p>When punch is on, simultaneously prints characters on paper and punches equivalent code into paper tape.</p> <p>When reader is on, reads code from punched paper tape and prints equivalent characters on paper.</p> <p><u>On-Line Operation (LINE)</u> - When tape reader and punch are off, prints characters on paper and sends equivalent signals to the computer.</p> <p>When tape reader is on, reads code from punched paper tape and sends equivalent signals to computer. No characters are printed.</p> <p>When receiving signals from computer, prints equivalent characters on paper and punches tape if punch is on.</p> | |
| Cover Guard | Latch, push to release | Used to hold paper tape in position when using tape reader. | |

3.5 BASIC OPERATION

Many methods exist for storing, modifying, and retrieving information from the PDP-11/40 System. These methods depend on the form of the information, time limitations, and the peripheral equipment connected to the processor. The following procedures are basic to the use of the PDP-11/40 System. Although they may be used less frequently as the programming and use of the system become more sophisticated, they are valuable in preparing the initial programs and in learning the function of system input and output transfers. For an understanding of the various operational controls and indicators, refer to paragraphs 3.2 through 3.4. Basic programming techniques are given in paragraph 3.6.

Operating procedures are separated into the following categories:

- a. Power on paragraph 3.5.1
- b. Basic console paragraph 3.5.2
 control
- c. Manual program paragraph 3.5.3
 loading
- d. Automatic program paragraph 3.5.4
 loading
- e. Running programs paragraph 3.5.5

3.5.1 Power On

When the console OFF/POWER/PANEL switch is turned from OFF to POWER, the system is initialized (or zeroed). A time delay allows sufficient time for voltages to logic units (especially memory elements) to stabilize.

The power-up initialization logic directly sets the microprogram control to a sequence of controlled events determined by the setting of the ENABLE/HALT switch.

If the console ENABLE/HALT switch is set to ENABLE when power is turned on, the processor executes a power-up microprogram sequence with the power-up vector address determined by jumpers on the Status module (M7285) of the KD11-A processor. A new processor status (PS) word and program counter (PC) are unstacked from the vector address, and vector address plus two, respectively.

Program operation begins with an entrance to the FETCH portion of the microflow with the new PC used to obtain the first instruction. Note that the processor Status module jumpers are initially set at octal location 24. This location can be changed to accommodate system requirements.

If the console ENABLE/HALT switch is set to HALT when power is turned on, the processor microflow is directly set to the console microloop. The machine awaits the activation of a console control switch.

The third position of the OFF/POWER/PANEL switch is PANEL which provides for program operation with the console control switches disabled. However, the console switch register may still be accessed.

3.5.2 Basic Console Control

Two major areas of control exist: control influenced by the ENABLE/HALT switch, which selects either program or console control; and control by the switches and sequences used for loading data manually into the processor.

3.5.2.1 ENABLE/HALT Switch

When the processor has control (ENABLE/HALT in ENABLE), either the START or CONT switch causes the program to run. The START switch initializes the system with a clear signal and begins operation at a specific address determined by the last console operation (usually LOAD ADRS). The CONT switch merely releases console control, and the program continues.

When the ENABLE/HALT switch is set to HALT, the console obtains control. The LOAD ADRS, EXAM, and DEP switches can be used. The CONT switch can now cause the processor to step through the program a single instruction at a time.

3.5.2.2 Loading Data Manually

Whenever data is manually loaded into a computer, it is desirable to have the address increment automatically upon each deposit. Thus, the user can set a starting address and continue to store data in sequential memory locations providing only new data for each location. The programmer's console logic also permits the user to immediately examine the data just deposited without re-addressing, to re-deposit if necessary, and to continue with automatic incrementation. These sequences are associated with the functioning of the DEP and EXAM switches.

The address in the ADDRESS register, and R(TEMPC), does not increment the first time EXAM or DEP is used after a HALT or LOAD ADRS. It does not increment if DEP is used immediately after EXAM or if EXAM is used immediately after DEP. It does increment if a DEP is used immediately after a DEP, or if an EXAM is used immediately after an EXAM. This increment is a word increment as the console is word oriented. Thus, the user can look at a location, change it, deposit the changed data, and then re-examine them without having to load an address each time.

Incrementation is on even boundaries for all addresses except the address specifically designated for the processor internal registers, which are incremented by one.

For example, to alter several successive locations, the following steps are performed:

| <u>Step</u> | <u>Procedure</u> |
|-------------|--|
| 1 | LOAD ADRS (starting location) |
| 2 | EXAM (no increment - looks at starting location) |
| 3 | DEP (no increment - loads starting location) |
| 4 | EXAM (no increment - checks previous deposit) |
| 5 | EXAM (increment - looks at next location) |
| 6 | DEP (no increment - loads second location) |
| 7 | EXAM (no increment - checks previous deposit) |
| 8 | EXAM (increment - looks at third location) |
| | etc. |

If the user desires to take advantage of automatic address incrementation for examining or loading data, the following steps can be used to load data into sequential locations:

| <u>Step</u> | <u>Procedure</u> |
|-------------|--|
| 1 | LOAD ADRS (starting location) |
| 2 | DEP (no increment - loads starting location) |
| 3 | DEP (increment - loads second location) |
| 4 | DEP (increment - loads third location) |
| 5 | DEP (increment - loads fourth location) |
| | etc. |

The same procedure can be used for examining data in sequential memory locations.

3.5.3 Manual Loading

A primary manual use of the programmer's console is to store the bootstrap loader in the core memory. (Programs and data can be stored or modified by manual use of the programmer's console.) The bootstrap loader (DEC-11-L1PA-LA) is a minimal instruction program that can automatically load programs into core memory from a paper tape punched in a special bootstrap format. One of these programs, after being stored, can in turn load any binary format tape into the computer. (An explanation of the number designations used for DEC programs is given in Table 3-5.)

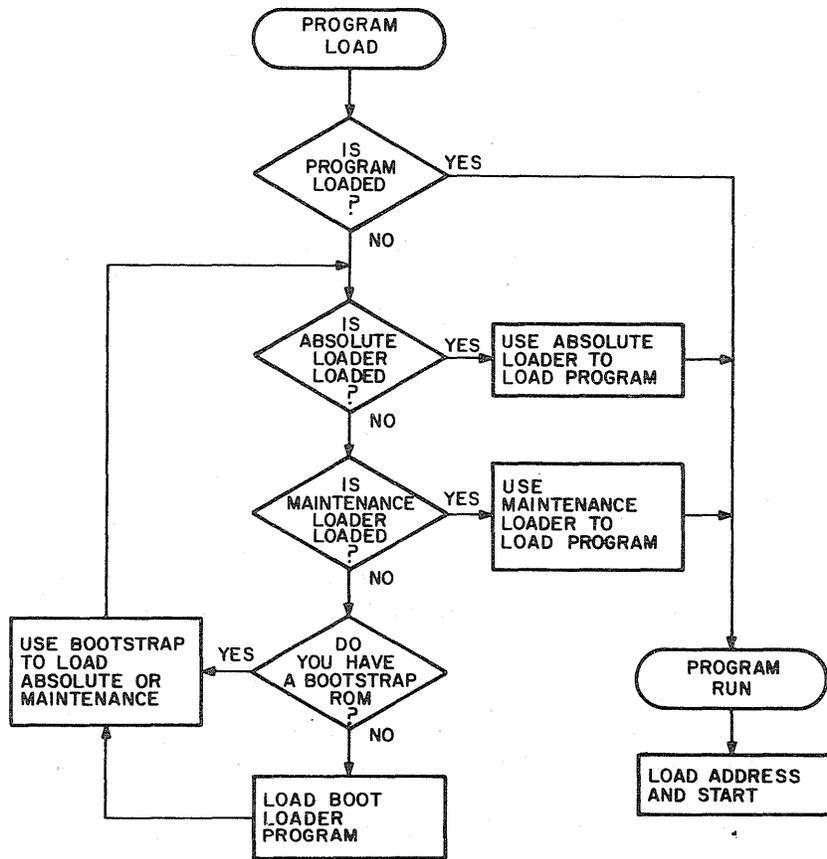
Table 3-5

Program Identification Codes

| | | COMPUTER IDENTIFICATION |
|--------------------|---|--|
| | | PRODUCT DISTRIBUTION |
| Format: | | DEC-11-LIPA-LA |
| Notes: | | ↑ ↑ ↑↑↑↑ ↑↑ 1 2 3456 78 |
| 1 | Product Code | MAINDEC = maintenance library products DEC = programming library products |
| 2 | Computer Series | 11 = PDP-11 Computer Systems |
| 3 | Major Category | L = Loader |
| 4 | Minor Category (sequential numbers) | 1 = first in a series of programs 2 = second in series, etc. |
| 5 | Option Category (hardware required to use software) | P = paper tape system H = high-speed reader and/or punch K = Teletype keyboard only M = magtape |
| 6 | Revision Category (sequential letters) | A = basic program B = first revision C = second revision, etc. |
| 7 | Distribution Method | L = listing P = paper tape |
| 8 | Distribution Mode | A = ASCII B = binary (absolute) O = other (bootstrap binary) |
| Example: | DEC-11-L2PB-PO | indicates a PDP-11 programming library product, second in a series of loaders, requiring a paper tape system to use, the first revision to the program, supplied as a paper tape in bootstrap binary format. |
| References: | <i>DEC Classifying and Documenting Standard, DEC-00-BZZB-D.</i> A list of all identification codes is in the <i>PDP-11 Convention Manual</i> . | |

The sequence of loading the computer is shown in Figure 3-4 with programs noted as follows:

- a. Bootstrap loader (DEC-11-L1PA-LA) - manually loaded by console switches; provides for automatic loading of programs punched in a special format.
- b. Absolute loader - punched in special format; loaded by bootstrap loader; provides for automatic loading of programs punched in binary format.
- c. Selected program - punched in binary format; loaded automatically by absolute loader.



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Figure 3-4 Flowchart of Procedure for Loading and Running Programs

In order to eliminate the necessity of more than one bootstrap loader, the bootstrap loader instructions contain two variables (x and y) to provide compatibility with various memory configurations and reading devices. These variables are listed in Table 3-6. A complete explanation of the bootstrap loader program is given in Chapter 5 of the Paper Tape Software Programming Handbook (DEC-11-GGPB-D); further information may be found in the program listing, DEC-11-L1PA-LA.

The following procedure is used for manually loading the BOOT loader program (DEC-11-L1PA-LA):

| <u>Step</u> | <u>Procedure</u> |
|-------------|---|
| 1 | Set ENABLE/HALT switch to HALT to give bus control to the console when powering up. |
| 2 | Turn OFF/POWER/PANEL switch to POWER position. This energizes the programmer's console. |
| 3 | Enter starting address of bootstrap loader (Table 3-6) into switch register. Make certain that the correct xx value is used (<u>037744</u> for 8K memory, <u>077744</u> for 16K memory, <u>137744</u> for 24K memory, etc.). |
| 4 | Depress LOAD ADRS switch. The address set in the switch register is shown on the ADDRESS display. |
| 5 | Enter starting address <u>contents</u> (016701) into switch register. |
| 6 | Lift DEP switch. The contents just entered in the switch register is displayed in the DATA display. |
| 7 | Enter <u>contents</u> of next address into switch register. |

NOTE

It is not necessary to load addresses after the starting address has been loaded because the address is automatically incremented by two each time DEP is used sequentially.

StepProcedure

- 8 Lift DEP switch.
- 9 Repeat steps 7, and 8 above for each location of the bootstrap loader. When loading the contents of address xx7766, make certain that the correct x value is used. When loading the contents of the last address, make certain that the correct y value is used.
- 10 The bootstrap loader program is now loaded in memory locations xx7744 through xx7766 and can be used to automatically load other programs into memory.
- 11 Correct program entry can be verified by examining the addresses between xx7744 and xx7766. This is accomplished by setting the starting address into the switch register and depressing the EXAM switch. The contents of the starting addresses are shown in the DATA display. Each time the EXAM is again depressed, the address is automatically incremented by two and the corresponding contents displayed.
- 12 This last step (verification) may be sufficient if the bootstrap loader program has already been loaded into the system. The program is stored in the last portion of available memory so that it tends to survive program operation and is available for reloading programs. If the program is not intact, load according to the above procedure, beginning with step 1.

Table 3-6

Bootstrap Loader
(DEC-11-L1PA-LA)

Bootstrap loader should be toggled into highest core memory bank.

| Address | Instruction |
|---------|-------------|
| xx7744 | 016701 |
| xx7746 | 000026 |
| xx7750 | 012702 |
| xx7752 | 000352 |
| xx7754 | 005211 |
| xx7756 | 105711 |
| xx7760 | 100376 |
| xx7762 | 116162 |
| xx7764 | 000002 |
| xx7766 | xx7400 |
| xx7770 | 005267 |
| xx7772 | 177756 |
| xx7774 | 000765 |
| xx7776 | yyyyyy |

xx represents highest available memory bank. First location of the loader is one of the following, depending on memory size; xx in all subsequent locations is the same as the first.

| Address | Memory Bank | Memory Size |
|---------|-------------|-------------|
| 037744 | 1 | 8K |
| 077744 | 2 | 16K |
| 137744 | 3 | 24K |
| 157744 | 4 | 28K |

Contents of address xx7776 (yyyyyy) should contain device status register address of paper-tape reader to be used when loading the bootstrap formatted tape. Addresses are:

| | |
|------------------------------|--------|
| Teletype Paper-Tape Reader | 177560 |
| High-Speed Paper-Tape Reader | 177550 |

3.5.4 Automatic Loading

Information can be stored or modified in the computer automatically only if a program capable of performing these functions has previously been stored in the core memory. For example, having the bootstrap loader stored in the computer enables the user to operate any program that has been punched in the special tape format required by the bootstrap loader. Typical programs of this type include the absolute loader, the absolute dump, and the teleprinter dump.

The bootstrap loader is limited because of the special tape format; another loader is used to load any binary format tape into the computer. This is the absolute loader (DEC-11-L2PB-PO), which is loaded into the computer by the bootstrap loader. Once the absolute loader is in memory, any binary tape program (such as PAL III assembler, symbolic editor, input/output service routines, diagnostics, mathematical routines, etc.) may be automatically loaded.

The following paragraphs give procedures for loading the absolute loader, and for using the absolute loader to store other programs. A complete description of the absolute loader program is give in Chapter 5 of the Paper Tape Software Programming Handbook (DEC-11-GGPB-D); refer also the the program listing, DEC-11-L2PB-LA.

3.5.4.1 Loading Absolute Loader

The following procedure is used for automatically loading the ABSolute Loader Program (DEC-11-L2PB-PO):

| <u>Step</u> | <u>Procedure</u> |
|---|--|
| 1 | Set ENABLE/HALT switch to HALT. |
| 2 | Make certain that the bootstrap loader has been stored in core memory (refer to Paragraph 3.6.3, step 11). |
| 3 | Enter starting address of bootstrap loader into switch register. The starting address is xx7744 (037744 for 8K memory, 077744 for 16K memory, 137744 for 24K memory, etc.). |
| 4 | Depress LOAD ADRS switch. The address set in the switch register is displayed in ADDRESS REGISTER indicators. |
| 5 | Set Teletype LINE/OFF/LOCAL switch to LINE. This connects the Teletype to the computer. |
| NOTE | |
| If some other reading device (such as the high speed paper tape reader) is used, make sure that the y value in bootstrap loader address xx7776 corresponds to the device as described in Table 3-6. | |
| 6 | Place the absolute loader tape in the Teletype reader. Make certain that the special leader (a sequence of 351 punches) is under the reader station. Blank leader does not work. |
| 7 | Set ENABLE/HALT to ENABLE. |
| 8 | Depress START switch. The tape is now read into the computer which halts when the entire program is loaded. |
| 9 | Upon completion of loading this tape, the DATA display lights may be in any configuration. The main |

reason for this is that no checksum capability exists in the bootstrap loader.

Any PDP-11 program punched in binary format may be loaded automatically by using the absolute loader. The absolute loader can be set up to select either an absolute or relocatable code. If a relocatable code is selected, the user may specify that the relocatable code start at a specific address or that the code start loading at the point the previous load stopped. The absolute loader also provides a checksum test to ensure accurate loading. Although the computer normally stops when the binary tape is loaded, instructions on the tape itself may cause the computer to begin execution of the program immediately after loading is finished. This action is beyond the control of the user because it is a part of the program on certain binary tapes.

The following procedure is used for automatic loading of binary tapes into the computer by using the absolute loader:

- | <u>Step</u> | <u>Procedure</u> |
|-------------|---|
| 1. | Make certain that the absolute loader program is stored in core memory (refer to paragraph 3.5.4.1). |
| 2. | Set ENABLE/HALT switch to HALT. |
| 3 | Enter starting address of absolute loader into switch register. The starting address is $\text{xx}7500$ (037500 for 8K memory, 077500 for 16K memory, 137500 for 24K memory, etc.). |

StepProcedure

- 4 Depress LOAD ADRS switch. The starting address of the absolute loader is now displayed in ADDRESS REGISTER indicators.
- 5 Select the type of load desired by setting switch register as specified in Table 3-7.

Table 3-7

Binary Tape Load Selection
(using ABSolute Loader)

| Type of Load | Switch Register Settings | |
|---|--------------------------|--------|
| | Bits 15-01 | Bit 00 |
| Normal (absolute) | Not applicable | 0 |
| Relocatable (continue where left off) | 0 | 1 |
| Relocatable (load at specified address) | Offset from tape origin | 1 |

- 6 Make certain that input/output device (Teletype unit of LA30 DECwriter) is on-line.

NOTE

The reading device may be changed at any time by the user without reloading the absolute loader. If a reader is to be changed, simply replace the contents of address xx7776 with the appropriate device status address (y value in Table 3-6).

- 7 Load desired binary tape into reader by placing leader under the reader station.

Step

Procedure

- 8 Set ENABLE/HALT switch to ENABLE.
- 9 Depress START switch. This begins the binary tape load.
- 10 If the binary tape contains a transfer address instruction, the computer begins execution of the program as soon as loading is complete.
- 11 The computer stops when either loading is complete or there is a checksum error.
 - a. Loading complete - the low-order (right hand) byte displayed in the DATA indicators is zero. Additional binary tapes may be loaded by repeating steps 5 through 7 above and depressing the CONT switch.
 - b. Checksum error- the low-order byte displayed in the DATA indicators is not zero, thereby indicating a checksum error has occurred in the previous block of data. In this case, reposition the tape in front of the error-producing block and depress the CONT switch.

3.5.4.3 Loading Maintenance Loader

The maintenance Loader program, MainDEC-11-D9EA, provides an alternate method of loading diagnostic programs that can be used if the Absolute Loader fails to function because of a hardware failure. This loader should only be used to load diagnostic programs if the Absolute Loader malfunctions.

Use the following procedure to automatically load the maintenance loader:

| <u>Step</u> | <u>Procedure</u> |
|-------------|---|
| 1 | Set ENABLE/HALT switch to HALT and depress START to clear the system. |
| 2 | Make certain that the bootstrap loader has been stored in memory, starting at address 037744. |

NOTE

The maintenance loader operates in the lowest 8K of memory. If some other memory area must be used, several program locations must be changed as listed in Table 3-8 after the maintenance program is loaded.

| | |
|---|---|
| 3 | Set switch register to 037744 and depress LOAD ADRS. |
| 4 | Set Teletype LINE/OFF/LOCAL switch to LINE. |
| 5 | Place the maintenance loader tape in paper-tape reader. |
| 6 | Set ENABLE/HALT switch to ENABLE and depress START. The tape is read into memory and the processor halts when the entire program has been loaded. |

NOTE

If the maintenance loader was not loaded into the lowest 8K of memory, make location changes at this time (see Table 3-8).

Table 3-8

Maintenance Loader Location Changes For Different Memories

Change Contents of:

To:

xx7502
xx7510
xx7542
xx7566
xx7624
xx7674

xx7470
xx7474
xx7475
xx7475
xx7776
xx7474

Where xx equals: 03 for 8K memory
 07 for 16K memory
 13 for 24K memory

3.5.5 Running Programs

When running any program, the program must first be loaded into the core memory either manually or by using one of the automatic loading programs (bootstrap loader or absolute loader). Once the program is in storage, it can be run at any time by loading the starting address of the program (refer to appropriate program documentation) into the switch register, depressing the LOAD ADRS switch, and then depressing the START switch. The user also must make certain that the ENABLE/HALT switch is in ENABLE and that the appropriate external devices are on-line (connected to the computer).

The program can be manually stopped at any time by setting the ENABLE/HALT switch to HALT. It can be restarted from that point by returning the ENABLE/HALT switch to ENABLE and depressing the CONT switch. It can be started anew by reloading the starting address and depressing the START switch.

A program can be altered during operation, or new data introduced, through the switch register. This console register has a bus address that the processor can reference in its instruction sequence. The information transferred may be treated as data or used to alter program flow.

Because of the speed of the computer, console indicators are

of limited value while the computer is running. Major use of the indicator panel is made during manual operation, single instruction operation, or during the maintenance mode. During manual operation, the console indicators reflect the console operations of LOAD ADRS, EXAM, and DEP. During maintenance operations, the console indicators display various data functions of the processor as the maintenance module is used to step through the program a microword at a time. Use of the maintenance module is described in the KD11 Processor Manual, DEC-11-HKDAA-A-D.

3.6 BASIC PROGRAMMING

In order to produce programs that fully utilize the power and flexibility of the PDP-11/40, it is necessary for the user to first become familiar with various programming techniques that are part of the basic design philosophy of the PDP-11/40 System. These techniques (such as use of stacks, subroutine linkage, interrupt nesting, reentrant and recursive programming, etc.) are covered in the PDP-11/40 Processor Handbook which also provides a detailed discussion of the instruction set.

In addition to the general programming information given in the PDP-11/40 Processor Handbook, the user should familiarize himself with console operation (described in paragraph 3.2) and with the basic and extended PDP-11/40 instruction sets (Chapter 4).

In the event the user is already familiar with programming the PDP-11/20 System, the PDP-11/40 can quickly be learned by comparing the prime programming differences between the two systems. These differences are listed in Table 3-9. Basically, the PDP-11/40 has added capabilities and speed. These capabilities are increased even more if the K11-D Memory Management Option and the K11 Extended (EIS) and Floating (FIS) Instruction Set Options are included in the system.

Note that the basic PDP-11/40 System (without options) has four more instructions than the PDP-11/20. These instructions are: eXclusive OR (XOR), Subtract One and Branch (SOB), ReTurn from inTerrupt (RTT), and Sign eXTend (SXT).

Table 3-9

PDP-11 Programming Comparison

PDP-11/20

JMP/JSR (R)+ uses (REG)+2 as address

All REG 6 (SP) autodecrement references can cause overflow. Address modes 4 and 5, JSR and traps are tested.

No red zone on stack overflow.

SWAB instruction does not ~~NOT TRUE~~ affect V.

Program HALT displays PC of HALT instruction in ADDRESS display.

Byte operations to the odd byte of the PS cause odd address traps.

No RTT instruction.

If RTI sets T bit, T bit trap acknowledged after instruction following RTI.

Explicit reference to PS can load T bit. Console can load T bit, initialize can clear it.

PDP-11/40

JMP/JSR (R)+ uses (REG) before auto-increment as address. All auto-increments are now post auto-increments.

Address modes 1,2,4, and 6, JSR and traps are tested except that nonaltering (DATIs) references to stack data are always allowed.

Red zone trap occurs if stack is 16 words below boundary. This trap saves PC+2 and PS on new stack at locations 2 and 0.

SWAB instruction clears V

Program HALT displays PC+2 of HALT instruction in ADDRESS display.

Byte operations to the odd byte of the PS do not trap. Not all bits may exist.

If RTT sets the T bit, the T bit trap occurs after the instruction following RTT.

If RTI sets T bit, T bit trap acknowledged immediately following RTI.

Only implicit references (RTI, RTT, traps, and interrupts) can load T bit. Console cannot load T bit but initialize can clear it.

Table 3-9
(continued)

PDP-11/20

Odd address or non-existent references using the SP cause a HALT. This is a case of double bus error with a second error occurring in the trap service of the first error.

Stack limit boundary fixed at octal 400 with violations serviced by an OVFL trap.

First instruction in an interrupt service routine is guaranteed to be executed.

Power up vector at 24 when power returns.

A trap instruction to vector location 14 exists for the IR code 3. No name is given this instruction.

PDP-11/40

Odd address or non-existent references using the SP cause a fatal trap. On bus error in trap service, a new stack is created at locations 0 and 2.

Optional variable stack limit boundary (KJ11-A Option). Use of red and yellow zones on either basic (octal 400) or optionally variable boundary.

The first instruction in an interrupt routine is not executed if another interrupt occurs at a higher priority level than was assumed by the first interrupt.

Power up vector is initially at 24; can alter jumpers to other addresses.

The formerly unnamed instruction for IR code 3 is now called BPT.

Table 3-9
(continued)

PDP-11/20

PDP-11/40

NOTE

The following is the sequence of service for internal processor traps, external interrupts, and HALT and WAIT.

| | |
|--|--|
| BUS ERROR TRAP - odd address, data time out. | BUS ERROR TRAP - odd address, fatal stack overflow (red); if KT11-D option is used, memory management violations to 250. |
| HALT instruction for console operation. | Same. (Refer to KT11-D, if installed, for other changes.) |
| TRAP instructions - illegal or reserved instructions, TRT, IOT, EMT, TRAP. | TRAP instructions - Illegal or reserved instructions, BPT, IOT, EMT, TRAP. |
| TRACE TRAP - T bit of processor status | Same |
| OVFL trap - stack overflow | OVFL - warning (yellow) stack overflow |
| PWR FAIL trap - power down | Same |
| CONSOLE BUS REQUEST - console operation after HALT switch | Same |
| UNIBUS BUS REQUEST - peripheral request, compared with processor priority, usually an interrupt occurs. | Same |
| WAIT LOOP - loop on a WAIT instruction in the IR until an interrupt allows exit. A CONSOLE BUS REQUEST returns to this loop after being honored. | Same |

4 PROCESSOR INSTRUCTIONS AND OPTIONS

4.1 SCOPE

The purpose of this chapter is to present a brief introduction of the PDP-11 instruction set and the processor options available for the PDP-11/40 System.

Paragraph 4.2 discusses the basic PDP-11 instruction set and also covers the expanded instructions that are available if certain processor options (Kell-E, Kell-F, and KT11-D) are installed in the basic system.

Paragraph 4.3 describes each of the options that can be mounted in the basic KD11-A processor and references appropriate documents containing detailed information on the specific option. These options are: Kell-E, Kell-F, KJ11-A, KT11-D, KW11-L, and KM11-A with an additional Small Peripheral Controller. Specifications are contained in Tables 4-12 through 4-16.

Information on memory units is presented in paragraph 4.4. These units include the MM11-L, MF11-L, ME11-L, and MM11-S memories.

4.2 INSTRUCTION SET

This section summarizes the PDP-11/40 address modes and instruction set. Its purpose is to define the KD11-A and provide tabular, quick-reference information. A complete description of PDP-11/40 address modes and instructions, with additional details and examples, is provided in the PDP-11/40 Processor Handbook.

The Instruction Set Processor (ISP) notation is used to define the processor operations for each address mode and instruction. Table 4-1 defines the modified ISP symbology used in this chapter. A more detailed description of ISP notation is provided in Appendix A of the PDP-11/40 Processor Handbook. Similar notation is used in the block diagram and flow diagram description of instruction implementation.

The following paragraphs cover address modes (paragraph 4.2.1), the basic instruction set (paragraph 4.2.2), and the extended instruction set (paragraph 4.2.3). The conventions used in the KD11-A Processor are:

- () is used for < > or []
- or () around an expression indicates logical AND
- + indicates logical OR
- indicates logical negation
- plus indicates addition
- minus indicates subtraction

Table 4-1

ISP Symbology

| Symbol | Definition |
|-------------|---|
| < > | Defines the limits of an expression, such as word length <15:0>. |
| [] | Defines the limits of a memory declaration; Mw [SP] specifies the address of the stack pointer in memory. |
| ← | The expression to the left of this symbol is replaced by the expression to the right of this symbol, Z ← 1 indicates the Z bit is set, PC ← PC + 2 indicates the program counter register (PC) is incremented by 2. |
| cat | Indicates concatenation; registers to the left and right of this expression are considered to be one register |
| equiv | Designates that expressions to the left and right are equivalent. |
| & | Logical AND |
| OR | Logical inclusive-OR |
| ~ | Negate |
| XOR | Logical exclusive-OR |
| ' | Indicates that a reference to the expression with which this symbol is used may cause side effects, e.g., registers may be changed as a result of the operation. |
| ; | Used as a delimiter |
| next | A sequential delimiter, the operation to the left must occur before the operation to the right. |
| m | Designates an address mode; address mode 1 is indicated by m = 1. |
| rg | General register 7 (program counter) |
| ai | Auto-increment; by 2 for word instructions, and by 1 for byte instructions. |
| r | Indicates a result; used many times with limit symbols as an intermediate register (r <15:0>). |
| + | Addition; expression to the left is added to expression to the right. |
| - | Subtraction; expression to the right is subtracted from expression to the left. |
| X | Multiply; expression to the left is multiplied by expression to the right. |
| / | Divide; expression to the left is divided by the expression to the right. |
| sign-extend | The sign bit of a byte, bit 7, is extended through bits 8 to 15. |
| Mw | Memory word declaration; the address in brackets points to the memory location. |
| nw' | Indicates next word, as pointed to by the PC with side effects ('). The word is at the next sequential PC address, or the word pointed to by the next word (deferred addressing). |
| R [dr] | Indicates that a register (R) address as a memory declaration is that of a device register. |
| D | Destination |
| Db | Byte destination |
| S | Source |
| Sb | Byte source |

4.2.1 Address Modes

The instruction set of the PDP-11/40 System flexibly interacts with the general-purpose registers through the address modes. Table 4-2 lists all of the address modes, including the program counter (PC) register address modes. These address modes, along with the general-purpose register designation, determine the instructions' operands (source and/or destination) and form part of the 16-bit instruction format (Figure 4-1).

Table 4-2

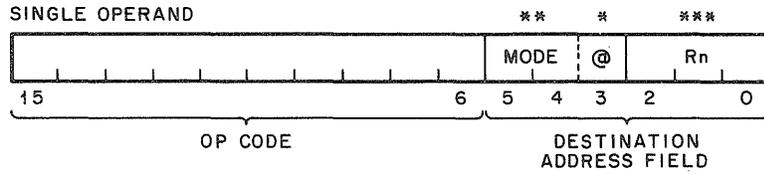
Address Modes

| Mode | Designation | Symbolic | ISP | Description |
|--|-------------------------|-------------------|---|--|
| General Purpose Register Addressing | | | | |
| 0 | register | R | if (m=0) then Rr (w1:0); | The register (R, Rr) is the operand. |
| 1 | register deferred | @R or (R) | if (m=1) then M[Rr]; | Defer to operand through register (R, Rr) as address. |
| 2 | auto-increment | (R)+ - | if (m=2) and (rg≠7) then M[Rr]; next Rr ← Rr + ai; | Defer to operand through register (R, Rr) as address, then increment. |
| 3 | auto-increment deferred | @(R)+ | if (m=3) and (rg≠7) then M[Mw[Rr]]; next Rr ← Rr + 2; | Defer to operand through (R), Mw [Rr] as address, then increment register (R, Rr). |
| 4 | auto-decrement | -(R) | if (m=4) then (Rr ← Rr - ai); next M[Rr]; | Decrement register (R, Rr), then defer to operand through register (R, Rr) as address. |
| 5 | auto-decrement deferred | @-(R) | if (m=5) then (Rr ← Rr - ai); next M[Mw[Rr]]; | Defer to operand through (R), Mw Rr after decrement of register (R, Rr). |
| 6 | indexed | ±X(R) | if (m=6) and (rg≠7) then M[nw' + Rr]; | Index via register = (R, Rr) by the amount specified in next PC word (X). |
| 7 | indexed deferred | @±X(R) or @(R) | if (m=7) and (rg≠7) then M[Mw[nw' + Rr]]; | Defer to operand through index of register (R, Rr) specified in next PC word (X) as address. |
| PC Register Addressing | | | | |
| 2 | immediate | #n | if (m=2) and (rg=7) then nw' (w1:0) | Defer to operand through PC value (next word); next word is immediate operand. |
| 3 | absolute | @#A | if (m=3) and (rg=7) then M[nw'] | Defer via next word (PC address) as address to operand; absolute addressing. |
| 6 | relative | A | if (m=6) and (rg=7) then M[nw' + PC]; | Relative to PC; uses next word as deferred address of operand. |
| 7 | relative deferred | @A | if (m=7) and (rg=7) then M[Mw[nw' + PC]]; | Defer relative to PC; uses next word as address of deferred address of the operand. |

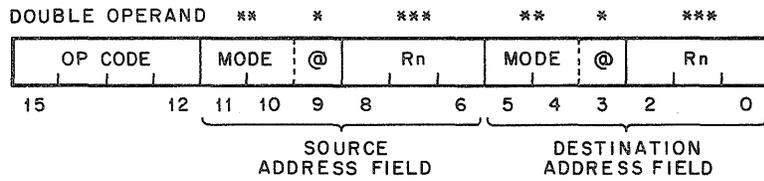
NOTE: The following symbols are used in this table:

R = Register

X, n, A = next program counter (PC) word (constant)



* = SPECIFIES DIRECT OR INDIRECT ADDRESS.
 ** = SPECIFIES HOW REGISTER WILL BE USED.
 *** = SPECIFIES ONE OF EIGHT GENERAL PURPOSE REGISTERS.



* = DIRECT/DEFERRED BIT FOR SOURCE AND DESTINATION ADDRESS.
 ** = SPECIFIES HOW SELECTED REGISTERS ARE TO BE USED.
 *** = SPECIFIES A GENERAL REGISTER.

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Figure 4-1 Double and Single Operand Addressing

4.2.2 Basic Instruction Set

The KD11-A basic instruction set is divided into six groups of instructions. The format of each group is shown in Figure 4-2. The six groups of instructions are:

- a. Double Operand - Operations which imply two operands (such as add, subtract, move, and compare) are handled by instructions that specify two addresses. The first operand is called the source operand; the second is called the destination operand. Bit assignments in the source and destination address fields may specify different address modes and different registers.

Double-operand instructions are listed in Table 4-3.

- b. Single Operand - Operations which require only one operand (such as clear, increment, test) are handled by instructions that specify only a destination address (operand). The operation code, address mode, and destination address are specified by the instruction.

Single-operand instructions are listed in Table 4-4.

- c. Register Source or Destination - Instructions in this group make use of the general processor registers as simple accumulators and the result is stored in the selected register. Information can be used as either a source or destination operand. For example, the exclusive OR of the selected register and the destination operand can be stored in the destination address.

Register source or destination instructions are listed in Table 4-5.

- d. Program Control (Branch) - These instructions permit control of the program by branching to new locations in the program dependent on conditions tested by the program. The instructions cause the program to branch to a location specified by the sum of an offset value (multiplied by 2) and the current contents of the PC provided the branch is either unconditional, or is conditional and the conditions are met after testing the PS word.

Program control instructions are listed in Table 4-6.

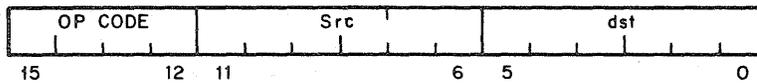
- e. Miscellaneous - These instructions include HALT, WAIT, and RESET as well as interrupt and trap handling instructions such as RTI, RTT, EMT, and TRAP.

Miscellaneous instructions are listed in Table 4-7.

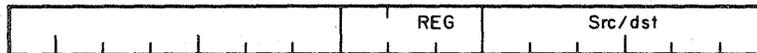
- f. Condition Code Operators - These instructions are used to set or clear individual condition codes in the processor status (PS) word. Selected combinations of these bits may be set or cleared together.

Condition code operators are listed in Table 4-8.

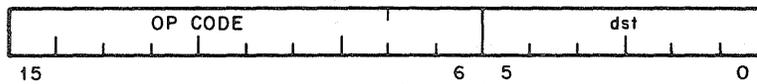
DOUBLE OPERAND



REGISTER SOURCE OR DESTINATION



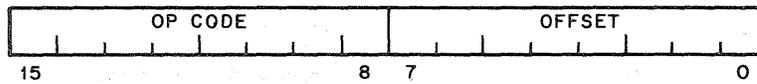
SINGLE OPERAND



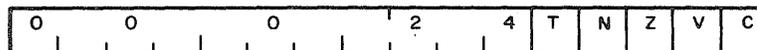
MISCELLANEOUS



BRANCH (PROGRAM CONTROL)



CONDITION CODE OPERATORS



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Figure 4-2 Instruction Formats

Table 4-3
Double Operand Instructions

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|---|--|--|
| MOV Move (Src to Dst) 01SSDD | $r \leftarrow S'$; next $N \leftarrow r \langle 15 \rangle$ if ($r \langle 15:0 \rangle = 0$) then ($Z \leftarrow 1$ else $Z \leftarrow 0$); $V \leftarrow 0$; $D' \leftarrow r$ | Move source to intermediate register, r. Set N if negative. Set Z if 0. Clear V. Transmit result to destination. |
| MOVB Move Byte (Src to Dst) 11SSDD | $r \leftarrow Sb'$; next $N \leftarrow r \langle 7 \rangle$; if ($r \langle 7:0 \rangle = 0$) then ($Z \leftarrow 1$ else $Z \leftarrow 0$); $V \leftarrow 0$; $Db' \leftarrow r$ | Move source to intermediate register, r. Set N if negative. Set Z if 0. Clear V. Transmit result to destination. |
| CMP Compare (Src to Dst) 02SSDD | $r \langle 16:0 \rangle \leftarrow S' - D'$; next $N \leftarrow r \langle 15 \rangle$; if ($r \langle 15:0 \rangle = 0$) then ($Z \leftarrow 1$ else $Z \leftarrow 0$); if ($S \langle 15 \rangle = \sim D \langle 15 \rangle$) & ($S \langle 15 \rangle \text{ XOR } r \langle 15 \rangle$) then ($V \leftarrow 1$ else $V \leftarrow 0$); $C \leftarrow r \langle 16 \rangle$ | Source and destination operands are compared, but unaffected. Only condition codes are affected, as follows: Set N if r is negative. Set Z if r is 0. Set V if operands have opposite signs and the sign of the source is the same as the result, r. Set C if 17th bit is carry. |
| CMPB Compare Byte 12SSDD | $r \langle 8:0 \rangle \leftarrow Sb' - Db'$; next $N \leftarrow r \langle 7 \rangle$; if ($r \langle 7:0 \rangle = 0$) then ($Z \leftarrow 1$ else $Z \leftarrow 0$); if ($Sb \langle 7 \rangle = \sim Db \langle 7 \rangle$) & ($Sb \langle 7 \rangle \text{ XOR } r \langle 7 \rangle$) then ($V \leftarrow 1$ else $V \leftarrow 0$); $C \leftarrow r \langle 8 \rangle$ | Same as CMP, except operands are bytes. |
| BIT Bit Test 03SSDD | $r \leftarrow D' \& S'$; next $N \leftarrow r \langle 15 \rangle$; if ($r \langle 15:0 \rangle = 0$) then ($Z \leftarrow 1$ else $Z \leftarrow 0$); $V \leftarrow 0$ | Logical AND of source and destination operands. Set N if negative. Set Z if 0. No overflow. |
| BITB Bit Test, Byte 13SSDD | $r \leftarrow Db' \& Sb'$; next $N \leftarrow r \langle 7 \rangle$; if ($r \langle 7:0 \rangle = 0$) then ($Z \leftarrow 1$ else $Z \leftarrow 0$); $V \leftarrow 0$ | Same as BIT, except byte |
| BIC Bit Clear 04SSDD | $r \leftarrow D' \& \sim S'$; next $N \leftarrow r \langle 15 \rangle$; if ($r \langle 15:0 \rangle = 0$) then ($Z \leftarrow 1$ else $Z \leftarrow 0$); $V \leftarrow 0$; $D \leftarrow r$ | AND destination operand with complemented source operand. Set N if negative. Set Z if 0. Clear V and put result in destination address. |
| BICB Bit Clear, Byte 14SSDD | $r \leftarrow Db' \& \sim Sb'$; next $N \leftarrow r \langle 7 \rangle$; if ($r \langle 7:0 \rangle = 0$) then ($Z \leftarrow 1$ else $Z \leftarrow 0$); $V \leftarrow 0$; $Db \leftarrow r$ | Same as BIC, except byte. |

(continued on next page)

Table 4-9
(continued)

Double Operand Instructions

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|--|---|---|
| BIS Bit Set 05SSDD | $r \leftarrow D' \text{ OR } S'$; next $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0)$; $V \leftarrow 0$; $D \leftarrow r$ | Inclusive OR of source operand and destination operand. Set N if negative. Set Z if 0. Clear V. Put result in destination. |
| BISB Bit Set, Byte 15SSDD | $r \leftarrow Db' \text{ OR } Sb'$; next $N \leftarrow r(7)$; if $(r(7:0) = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0)$; $V \leftarrow 0$; $Db \leftarrow r$ | Same as BIS, except byte. |
| ADD Add 06SSDD | $r(16:0) \leftarrow S' + D'$; next $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0)$; if $(S(15) \text{ equiv } D(15) \ \& \ (S(15) \text{ XOR } r(15)))$ then $(V \leftarrow 1 \text{ else } V \leftarrow 0)$; $C \leftarrow r(16)$; $D \leftarrow r(15:0)$ | Add source and destination to provide 17-bit sum. Set N if negative result. Set Z if 0. Set V if both operands were same sign and the result is of opposite sign. Set C if carry. Put result in destination. |
| SUB Subtract 16SSDD | $r(16:0) \leftarrow D' - S'$; next $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0)$; if $(D(15) \text{ XOR } S(15) \ \& \ (D(15) \text{ XOR } r(15)))$ then $(V \leftarrow 1 \text{ else } V \leftarrow 0)$; $C \leftarrow r(16)$; $D \leftarrow r(15:0)$ | Subtract source operand from destination operand. Set N if negative results. Set Z if 0. Set V if operands had different signs and result is opposite sign from destination. Set C if a carry. Put result in destination. |

Table 4-4

Single Operand Instructions

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|--|---|--|
| CLR Clear dst 0050DD | $D' \leftarrow 0;$ $N \leftarrow 0;$ $Z \leftarrow 1;$ $V \leftarrow 0;$ $C \leftarrow 0$ | Clear destination, N, V, and C; set Z. |
| CLRB Clear Byte dst 1050DD | $Db' \leftarrow 0;$ $N \leftarrow 0;$ $Z \leftarrow 1;$ $V \leftarrow 0;$ $C \leftarrow 0$ | Clear destination byte. |
| COM Complement dst 0051DD | $r \leftarrow \sim D';$ next $N \leftarrow r(15);$ if $(r(15:0) = 0)$ then $Z \leftarrow 1$ else $Z \leftarrow 0;$ $V \leftarrow 0;$ $C \leftarrow 1;$ $D \leftarrow r$ | Complement destination. Set N if negative. Set Z if 0. Clear V. Set C. Put result in destination. |
| COMB Complement Byte dst 1051DD | $r \leftarrow \sim Db';$ next $N \leftarrow r(7);$ if $(r(7:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0);$ $V \leftarrow 0;$ $C \leftarrow 1;$ $Db \leftarrow r$ | Same as COM, except byte. |
| INC Increment dst 0052DD | $r \leftarrow D' + 1;$ next $N \leftarrow r(15);$ if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0);$ if $(r(15:0) = 100000_8)$ then $(V \leftarrow 1$ else $V \leftarrow 0);$ $D \leftarrow r$ | Result is sum of D plus 1. Set N if negative. Set Z if 0. Set V if result equals 100000_8 (dst was 077777_8). Put result in destination. |
| INCB Increment Byte dst 1052DD | $r \leftarrow Db' + 1;$ next $N \leftarrow r(7);$ if $(r(7:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0);$ if $(r(7:0) = 200_8)$ then $(V \leftarrow 1$ else $V \leftarrow 0);$ $Db \leftarrow r$ | Same as INC, except byte. Set V if result equals 200_8 (dst byte was 177_8). |
| DEC Decrement dst 0053DD | $r \leftarrow D' - 1;$ next $N \leftarrow r(15);$ if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0);$ if $(r(15:0) = 77777_8)$ then $(V \leftarrow 1$ else $V \leftarrow 0);$ $D \leftarrow r$ | Result is destination operand minus 1. Set N if negative. Set Z if 0. Set V if result equals 77777_8 (dst was 100000_8). Put result in destination. |
| DECB Decrement Byte dst 1053DD | $r \leftarrow Db' - 1;$ next $N \leftarrow r(7);$ if $(r(7:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0);$ if $(r(7:0) = 177_8)$ then $(V \leftarrow 1$ else $V \leftarrow 0);$ $Db \leftarrow r$ | Same as DEC, except byte. Set V if result is 177_8 (dst byte was 000_8). |

(continued on next page)

Table 4-4
(continued)

Single Operand Instructions

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|--|--|--|
| NEG Negate dst 0054DD | $r \leftarrow -D'$; next $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; if $(r(15:0) = 100000_8)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$; if $(r(15:0) = 0)$ then $(C \leftarrow 0$ else $C \leftarrow 1)$; $D \leftarrow r$ | Negate D by 2's complement. Set N if negative result. Set Z if 0. Set V if destination operand was 100000_8 . Clear C if result is 0, otherwise set C. Put result in destination. |
| NEGB Negate Byte 1054DD | $r \leftarrow -Db'$; next $N \leftarrow r(7)$; if $(r(7:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; if $(r(7:0) = 200_8)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$; if $(r(7:0) = 0)$ then $(C \leftarrow 0$ else $C \leftarrow 1)$; $Db \leftarrow r$ | Same as NEG, except byte. |
| ADC Add Carry 0055DD | $r \leftarrow D' + C$; next $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; if $(r(15:0) = 100000_8) \& (C = 1)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$; next if $(r(15:0) = 0) \& (C = 1)$ then $(C \leftarrow 1$ else $C \leftarrow 0)$; $D \leftarrow r$ | Add the C bit to the destination. Set N if negative. Set Z if 0. Set V if destination was 077777_8 and C was 1. Set C if destination was 177777_8 and C was 1. |
| ADCB Add Carry Byte 1055DD | $r \leftarrow Db' + C$; next $N \leftarrow r(7)$; if $(r(7:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; if $(r(7:0) = 200_8) \& (C = 1)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$; next if $(r(7:0) = 0) \& (C = 1)$ then $(C \leftarrow 1$ else $C \leftarrow 0)$; $Db \leftarrow r$ | Same as ADC, except byte. |
| SBC Subtract Carry 0056DD | $r \leftarrow D' - C$; next $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; if $(r(15:0) = 100000_8)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$; if $(r(15:0) = 0) \& (C = 1)$ then $(C \leftarrow 0$ else $C \leftarrow 1)$; $D \leftarrow r$ | Subtract C bit from contents of destination Set N if negative. Set Z if 0. Set V if result is 100000_8 . Clear C if result is 0 and C = 1. Put result in destination. |
| SBCB Subtract Carry Byte 1056DD | $r \leftarrow Db' - C$; next $N \leftarrow r(7)$; if $(r(7:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; if $(r(7:0) = 200_8)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$; if $(r(7:0) = 0) \& (C = 1)$ then $(C \leftarrow 0$ else $C \leftarrow 1)$; $Db \leftarrow r$ | Same as SBC, except byte. |

(continued on next page)

Table 4-4
(continued)

Single Operand Instructions

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|---|--|---|
| TST Test 0057DD | $r \leftarrow D' - 0$; next $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; $V \leftarrow 0$; $C \leftarrow 0$ | Sets N and Z condition codes according to contents of destination address. |
| TSTB Test Byte 1057DD | $r \leftarrow Db' - 0$; next $N \leftarrow r(7)$; if $(r(7:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; $V \leftarrow 0$; $C \leftarrow 0$ | Same as TST, except byte. |
| ROR Rotate Right 0060DD | $r(16:0) \leftarrow D'(0)$ cat C cat $D'(15:1)$; next $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; C cat $D(15:0) \leftarrow r(16:0)$; next if $(N \text{ XOR } C)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$ | 17-bit intermediate result is C and contents of destination rotated right one place. Set N if high order bit is set. Set Z if result is 0. Put 17-bit result into C bit and destination. Load V with exclusive-OR of N and C (after rotation is complete). |
| RORB Rotate Right Byte 1060DD | $r(8:0) \leftarrow Db'(0)$ cat C cat $Db'(7:1)$; next $N \leftarrow r(7)$; if $(r(7:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; C cat $Db \leftarrow r(8:0)$; next if $(N \text{ XOR } C)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$ | Same as ROR, except byte. |
| ROL Rotate Left 0061DD | $r(16:0) \leftarrow D'(15:0)$ cat C; next $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; C cat $D \leftarrow r(16:0)$; next if $(N \text{ XOR } C)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$ | 17-bit result is C and contents of destination rotated left one bit. Set N if result is negative. Set Z if result is 0. Put result into C and D. Bit 15 into C bit and previous C bit into bit 0. Load V with exclusive-OR of N and C after rotation is complete. |
| ROLB Rotate Left Byte 1061DD | $r(8:0) \leftarrow Db'(7:0)$ cat C; next $N \leftarrow r(7)$; if $(r(7:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; C cat $Db \leftarrow r(8:0)$; next if $(N \text{ XOR } C)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$ | Same as ROL, except byte. |
| ASR Arithmetic Shift Right 0062DD | $r \leftarrow D'/2$; next $C \leftarrow D(0)$; $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; next if $(N \text{ XOR } C)$ then $(V \leftarrow 1$ else $V \leftarrow 0)$; $D \leftarrow r$ | Contents of destination shifted right one place ($\div 2$). Least-significant bit loaded into C. Set N if result negative. Set Z if result 0. Load V with exclusive-OR of N and C after shift is complete. Put result into destination. |

(continued on next page)

Table 4-4
(continued)

Single Operand Instructions

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|--|--|--|
| ASRB Arithmetic Shift Right Byte 1062DD | $r \leftarrow Db' / 2; \text{ next}$ $C \leftarrow Db \langle 0 \rangle;$ $N \leftarrow r \langle 7 \rangle;$ if $(r \langle 7:0 \rangle = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0); \text{ next}$ if $(N \text{ XOR } C)$ then $(V \leftarrow 1 \text{ else } V \leftarrow 0);$ $Db \leftarrow r$ | Same as ASR except byte. |
| ASL Arithmetic Shift Left 0063DD | $r \leftarrow D' \langle 15 \rangle \text{ cat } D' \langle 13:0 \rangle \text{ cat } 0; \text{ next}$ $C \leftarrow D \langle 14 \rangle; \text{ next}$ $N \leftarrow r \langle 15 \rangle;$ if $(r \langle 15:0 \rangle = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0); \text{ next}$ if $(N \text{ XOR } C)$ then $(V \leftarrow 1 \text{ else } V \leftarrow 0);$ $D \leftarrow r$ | Shifts contents of destination left one place, but sign bit remains in most significant place. Bit 14 loaded into C. Set N if result negative. Set Z if result 0. Load V with exclusive-OR of N and C after shift completed. Put result in destination. |
| ASLB Arithmetic Shift Left Byte 1063DD | $r \leftarrow Db' \langle 7 \rangle \text{ cat } Db' \langle 5:0 \rangle \text{ cat } 0; \text{ next}$ $C \leftarrow Db \langle 6 \rangle; \text{ next}$ $N \leftarrow r \langle 7 \rangle;$ if $(r \langle 7:0 \rangle = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0); \text{ next}$ if $(N \text{ XOR } C)$ then $(V \leftarrow 1 \text{ else } V \leftarrow 0);$ $Db \leftarrow r$ | Same as ASL, except byte. |
| MARK Mark 0064nn | $SP \leftarrow SP + (2 \times df \langle 5:0 \rangle); \text{ next}$ $PC \leftarrow R[5]; \text{ next}$ $R[5] \leftarrow Mw [SP];$ $SP \leftarrow SP + 2$ | Adjusts stack pointer by the number of words indicated in the low 6 bits of the instruction ($2 \times nn$ locations). Puts old PC (R5) into PC. Contents of old R5 popped into R5. |
| SXT Sign Extend destination 0067DD | if $(N = 1)$ then $(r \langle 15:0 \rangle \leftarrow -1 \text{ else } r \langle 15:0 \rangle \leftarrow 0);$ next if $(r \langle 15:0 \rangle = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0);$ $D' \leftarrow r$ | If the N bit is set, then -1 is placed in the destination operand. Otherwise, 0 is placed in the destination operand. Set Z if result is 0. |

Table 4-5

Register Source or Destination Instructions

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|---|---|---|
| XOR Exclusive-OR 074RDD | $r \leftarrow R[\text{sr}] \text{ XOR } D'; \text{ next}$ if ($r = 0$) then ($Z \leftarrow 1$ else $Z \leftarrow 0$); $N \leftarrow r(15)$; $V \leftarrow 0$; $R[\text{sr}] \leftarrow r$ | The exclusive-OR of the register and the destination operand is stored in the destination address. Set Z if result is 0. Set N if result is negative. Clear V; no overflow possible. |
| SOB Subtract One and Branch 077R offset | $r \leftarrow R[\text{sr}] - 1; \text{ next}$ $R[\text{sr}] \leftarrow r$; if ($r \neq 0$) then ($PC \leftarrow PC - 2 \times \text{df}(5:0)$) | Decrement register by 1. If result is not equal to 0, branch. Subtract 2×6 -bit offset from PC to get new PC. |

Table 4-6
Program Control Instructions

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|---|---|--|
| BR Branch Unconditional 0004 loc | $PC \leftarrow PC + \text{sign-extend}(\text{instr} \langle 7:0 \rangle \times 2)$ | Always branch. PC changed as follows: Eight least-significant bits of instruction are multiplied times 2 and added to PC with sign extended. |
| BNE Branch Not Equal 0010 loc | if $(Z = 0)$ then $(PC \leftarrow PC + \text{sign-extend}(\text{instr} \langle 7:0 \rangle \times 2))$ | Branch if Z is 0. |
| BEQ Branch on Equal 0014 loc | if $(Z = 1)$ then $(PC \leftarrow PC + \text{sign-extend}(\text{instr} \langle 7:0 \rangle \times 2))$ | Branch if Z is 1. |
| BGE Branch if Greater than or Equal (zero) 0020 loc | if $(N \text{ equiv } V)$ then $(PC \leftarrow PC + \text{sign-extend}(\text{instr} \langle 7:0 \rangle \times 2))$ | Branch if N is equivalent to V. |
| BLT Branch on Less Than 0024 loc | if $(N \text{ XOR } V)$ then $(PC \leftarrow PC + \text{sign-extend}(\text{instr} \langle 7:0 \rangle \times 2))$ | Branch if exclusive-OR of N and V equal 1. |
| BGT Branch on Greater Than 0030 loc | if $(\sim Z \& (N \text{ equiv } V))$ then $(PC \leftarrow PC + \text{sign-extend}(\text{instr} \langle 7:0 \rangle \times 2))$ | Branch if Z not 0 and N equals V. |
| BLE Branch on Less Than or Equal (zero) 0034 loc | if $(Z \text{ OR } (N \text{ XOR } V))$ then $(PC \leftarrow PC + \text{sign-extend}(\text{instr} \langle 7:0 \rangle \times 2))$ | Branch if Z equals 1 or if exclusive-OR of N and V equals 1. |
| BPL Branch on Plus 1000 loc | if $(N = 0)$ then $(PC \leftarrow PC + \text{sign-extend}(\text{instr} \langle 7:0 \rangle \times 2))$ | Branch if N is 0. |
| BMI Branch on Minus 1004 loc | if $(N = 1)$ then $(PC \leftarrow PC + \text{sign-extend}(\text{instr} \langle 7:0 \rangle \times 2))$ | Branch if N is 1. |
| BHI Branch on Higher 1010 loc | if $\sim(C \text{ OR } Z)$ then $(PC \leftarrow PC + \text{sign-extend}(\text{instr} \langle 7:0 \rangle \times 2))$ | Branch if C and Z are 0. |

(continued on next page)

Table 4-6
(continued)

Program Control Instructions

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|--|---|--|
| BLOS Branch on Lower or Same 1014 loc | if (C OR Z) then (PC ← PC + sign-extend (instr (7:0) × 2)) | Branch if C or Z is 1. |
| BVC Branch on Overflow Clear | if (V = 0) then (PC ← PC + sign-extend (instr (7:0) × 2)) | Branch if V is 0. |
| BVS Branch on Overflow Set 1024 loc | if (V = 1) then (PC ← PC + sign-extend (instr (7:0) × 2)) | Branch if V is 1. |
| BHIS Branch on Higher or Same 1030 loc | if (C = 0) then (PC ← PC + sign-extend (instr (7:0) × 2)) | Branch if C is 0. |
| BLO Branch on Lower 1034 loc | if (C = 1) then (PC ← PC + sign-extend (instr (7:0) × 2)) | Branch if C is 1. |
| JSR Jump to Subroutine 004RDD | SP ← SP - 2; next Mw [SP] ← R[sr]; R[sr] ← PC PC ← D address | Push contents of R onto stack. Store current PC in R. Load subroutine address into PC. |
| RTS Return from Subroutine 00020R | PC ← R[dr]; R[dr] ← Mw [SP]; SP ← SP + 2 | Load contents of R into PC. Pop stack pointer into R. |

Table 4-7

Miscellaneous Instructions

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|--|---|--|
| HALT Halt 000000 | Off ← true | Processor halts with console in control. No activities or instructions can be executed until a console actions restarts the processor. |
| WAIT Wait 000001 | Wait ← true | Processor relinquishes bus and waits for an external interrupt. |
| IOT I/O Trap 000004 | SP ← SP - 2; next Mw [SP] ← PS; SP ← SP - 2; next Mw [SP] ← PC; PC ← Mw [20]; PS ← Mw [22] | Push PS onto Stack. Push PC onto stack. Get new PC from location 20. Get new PS from location 22. |
| RESET Reset External Bus 000005 | Init ← 1; Delay (20 milliseconds); next Init ← 0 | Send INIT on Unibus for 20 ms. |
| SPL Set Priority Level 00023N | PS (7:5) ← df (2:0) | Load three least significant bits, N, into PS. |
| RTI Return from Interrupt 000002 | PC ← Mw [SP]; SP ← SP + 2; next PS ← Mw [SP]; SP ← SP + 2 | Pop PC off stack. Pop PS off stack. (RTI permits trace trap.) |
| RTT Return from Interrupt 000006 | PC ← Mw [SP]; SP ← SP + 2; next PS ← Mw [SP]; SP ← SP + 2 | Pop PC off stack. Pop PS off stack. (RTT inhibits trace trap.) |
| EMT Emulator Trap 104 Code (104000 - 104377) | SP ← SP - 2; next Mw [SP] ← PS; SP ← SP - 2; next Mw [SP] ← PC; PC ← Mw [30]; PS ← Mw [32] | Push PS onto stack. Push PC onto stack. Get new PC and PS from locations 30 and 32. |
| TRAP Trap 104 Code (104400 - 104777) | SP ← SP - 2; next Mw [SP] ← PS SP ← SP - 2; next Mw [SP] ← PC; PC ← Mw [34]; PS ← Mw [36] | Push PS onto stack. Push PC onto stack. Get new PC and PS from locations 34 and 36. |

Table 4-8
Condition Code Operators

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|--|---|--|
| CLC Clear C 000241 | if (instr (4) = 0 & instr (0) = 1) then C ← 0 | When bit 4 of the instruction is 0 bits 3, 2, 1, and 0 clear corresponding bits in PS. |
| CLV Clear V 000242 | if (instr (4) = 0 & instr (1) = 1) then V ← 0 | |
| CLZ Clear Z 000244 | if (instr (4) = 0 & instr (2) = 1) then Z ← 0 | |
| CLN Clear N 000250 | if (instr (4) = 0 & instr (3) = 1) then N ← 0 | |
| CCC Clear all Condition Codes 000257 | if (instr (4) = 0 & instr (3:0) = 17) then (C ← 0; V ← 0; Z ← 0; N ← 0) | When bit 4 of the instruction is 1, bits 3, 2, 1, and 0 set corresponding bits in PS. |
| SEC Set C 000261 | if (instr (4) = 1 & instr (0) = 1) then C ← 1 | |
| SEV Set V 000262 | if (instr (4) = 1 & instr (1) = 1) then V ← 1 | |
| SEZ Set Z 000264 | if (instr (4) = 1 & instr (2) = 1) then Z ← 1 | |
| SEN Set N 000270 | if (instr (4) = 1 & instr (3) = 1) then N ← 1 | |
| SCC Set all Condition Codes 000277 | if (instr (4:0) = 37) then (C ← 1; V ← 1; Z ← 1; N ← 1) | |

4.2.3 Extended Instruction Set

Additional instructions are available if certain processor options are added to the basic system. These instructions are:

- a. KE11-E Extended Instruction Set (EIS) - These instructions have the same format as double-operand instructions and provide an increased arithmetic capability to the basic instruction set. These instructions are: multiply (MUL), divide (DIV), arithmetic shift (ASH), and arithmetic shift combined (ASHC).

The EIS instructions are listed in Table 4-9.

- b. KE11-F Floating Instruction Set (FIS) - These instructions permit arithmetic operations in floating-point notation. The instructions are: FADD, FSUB, FMUL, and FDIV (floating point addition, subtraction, multiplication, and division). Descriptions of each of these instructions are given in the PDP-11/40 Processor Handbook.

- c. KT11-D Memory Management - The MFPI instruction is provided to allow inter-address space communication when the PDP-11/40 is using the memory management option. The MFPI instruction determines the address of the destination operand in the current address space.

Note that in the table, the move from previous instruction (MFPI) and the move to previous instruction (MTPI) are listed as MFPI/D and MTPI/D. This is because in the PDP-11/40, MFPI and MFPI are executed in an identical manner as are MTPI and MTPD.

The KT11-D instructions are listed in Table 4-10.

Table 4-9
Extended Instruction Set (EIS)

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|---|--|--|
| MUL Multiply 070RSS | $r(31:0) \leftarrow D' \times R[sr]; \text{next}$ if $(r(31:0) = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0)$; $N \leftarrow r(31)$; if $(r(31:0) < -2^{15}) \text{ OR } (r(31:0) \geq 2^{15})$ then $(C \leftarrow 1 \text{ else } C \leftarrow 0)$; $V \leftarrow 0$; $R[sr](15:0) \leftarrow r(31:16); \text{next}$ $R[sr \text{ OR } 1](15:0) \leftarrow r(15:0)$; | Multiply contents of source register and destination to form 32-bit product. Set Z if product is 0. Set N if product is negative. Set C if product is more than 16-bit result. No overflow possible; clear V. Store the high-order result in R. Store the low-order result in succeeding register if R is even number. Otherwise, store in R. |
| DIV Divide 071RSS | $r1(31:0) \leftarrow R[sr] \text{ cat } R[sr \text{ OR } 1]/D'; \text{next}$ $r2(15:0) \leftarrow R[sr] \text{ cat } R[sr \text{ OR } 1] - (r1 \times D)$; next $N \leftarrow r1(15)$; if $(r1(31:0) = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0)$; if $(D = 0)$ then $(C \leftarrow 1 \text{ else } C \leftarrow 0)$; if $(r1(15) = 0) \& (r1(31:16) \neq 0)$ OR if $(r1(15) = 1) \& (r1(31:16) \neq -1)$ OR if $(D = 0)$ then $(V \leftarrow 1 \text{ else } V \leftarrow 0)$; $R[sr] \leftarrow r1(15:0)$ $R[sr \text{ OR } 1] \leftarrow r2$ | The 32-bit dividend, R, R OR 1, is divided by source operand D. R must be even number. Determine the remainder. Set N if quotient is negative. Set Z if quotient is 0. Set C if divide by 0 attempted. Set V if divisor is 0, or if the result is too large to be stored as a 16-bit number. Store quotient in R. Store remainder in R OR 1. |
| ASH Arithmetic Shift 072RDD | $r(79:0) \leftarrow \text{sign-extend}(R[sr](15:0) \times 2^{\uparrow}(D'(5:0) + 32) \bmod 64); \text{next}$ $R[sr](15:0) \leftarrow r(47:32); \text{next}$ if $(R[sr] = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0)$; if $((R[sr](15) = 0) \& (r(79:48) \neq 0) \text{ OR } (R[sr](15) = 1) \& (r(79:48) \neq -1))$ then $(V \leftarrow 1 \text{ else } V \leftarrow 0)$; $N \leftarrow R[sr](15)$; if $(D(5) = 1)$ then $C \leftarrow r(31)$; if $(D(5) = 0) \& (D(5:0) \neq 0)$ then $C \leftarrow r(48)$; if $(D(5:0) = 0)$ then $C \leftarrow 0$ | Contents of R are shifted NN places right or left, where NN equals the six low-order bits of DD. $NN = -32 \text{ to } +31$. Store result in R. Set Z if result is 0. Set V if sign of register changed during shift. Set N if result is negative. Load C from last bit shifted out of register. |
| ASHC Arithmetic Shift Combined 073RDD | $r(95:0) \leftarrow \text{sign-extend}(R[sr] \text{ cat } R[sr \text{ OR } 1] \times 2^{\uparrow}(D'(5:0) + 32) \bmod 64); \text{next}$ $R[sr] \leftarrow r(63:48); \text{next}$ $R[sr \text{ OR } 1] \leftarrow r(47:32); \text{next}$ if $(R[sr] \text{ cat } R[sr \text{ OR } 1] = 0)$ then $(Z \leftarrow 1 \text{ else } Z \leftarrow 0)$; $N \leftarrow R[sr](15)$; if $(r(63) = 0) \& (r(95:64) \neq 0) \text{ OR } (r(63) \neq 0) \& (r(95:64) \neq -1)$ then $(V \leftarrow 1 \text{ else } V \leftarrow 0)$; if $(D(5) = 1)$ then $C \leftarrow r(31)$; if $(D(5) = 0) \& (D(5:0) \neq 0)$ then $C \leftarrow r(64)$; if $(D(5:0) = 0)$ then $C \leftarrow 0$ | Contents of R, and R ORed with 1, form a 32-bit word ($R = 31:16, ROR 1 = 15:0$) that is shifted right or left NN places, specified by six low-order bits of destination operand, DD. Store results in R and R OR 1. Set Z if result is 0. Set N if result is negative. Set V if sign bit changes during the shift. Load C with high order if left shift. Load C with low order if right shift. Otherwise, clear C. |

Table 4-10

Memory Management Instruction Set

| Mnemonic Instruction and Op Code | ISP Notation | Description |
|--|---|---|
| MFPI/D Move From Previous Instruction Space 0065DD | $r \leftarrow D'$; next $SP \leftarrow SP - 2$; $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; $V \leftarrow 0$; $Mw[SP] \leftarrow r$ | Get destination operand from previous I space. Push stack. Set N if negative. Set Z if 0. Clear V. Put operand into current address space. |
| MTPI/D Move To Previous Instruction Space 0066DD | $r \leftarrow Mw[SP]$; $SP \leftarrow SP + 2$; next $N \leftarrow r(15)$; if $(r(15:0) = 0)$ then $(Z \leftarrow 1$ else $Z \leftarrow 0)$; $V \leftarrow 0$; $D' \leftarrow r$ | Get data from current stack. Pop stack. Set N if negative. Set Z if 0. Clear V. Move to previous I space destination. |

4.3 PROCESSOR OPTIONS

The basic KD11-A processor of the PDP-11/40 System contains space for installing six processor options. In addition, there is a small peripheral controller slot that is usually used for a programmer's console device (such as the DECwriter or Teletype interface) but that also can be used for a variety of options dependent on the user's individual requirements. The specific slot, or slots, allocated for each option is listed in Table 4-11 and shown in Figure 6- .

The processor options that are available are:

- a. KE11-E Extended Instruction Set (EIS)
- b. KE11-F Floating Instruction Set (FIS)
- c. KJ11-A Stack Limit Register
- d. KT11-D Memory Management
- e. KW11-L Line Frequency Interrupt Clock
- f. KM11-A Maintenance Console
- g. Small peripheral controller slot (variable option)

The above options can be used in any combination as they function independently with two exceptions. The KE11-F(FIS) option physically requires the KE11-E(EIS) option, and software for the KT11-D option requires the KJ11-A option. Each option is discussed separately in subsequent paragraphs which include a general description, specifications, and a reference to more detailed documents.

Table 4-11
Location of Processor Options

| <u>Option</u> | <u>Section(s)</u> | <u>Slot</u> |
|---|-------------------|-------------|
| KE11-E Extended Instruction Set (EIS) | A-F | 02 |
| KE11-F Floating Instruction Set (FIS) | A-D | 01 |
| KJ11-A Stack Limit Register | E | 03 |
| KT11-D Memory Management | A-F | 08 |
| KW11-L Line Frequency Clock | F | 03 |
| KM11-A Maintenance Console | | |
| For maintenance of the basic processor | F | 01 |
| For maintenance of the KT11-D and /or EIS and FIS options | E | 01 |
| Small Peripheral Controller Slot | C-F | 09 |

4.3.1 Kell-E Extended Instruction Set (EIS) Option

The Kell-E Extended Instruction Set Option is a processor option that expands the basic PDP-11/40 instruction set to include: multiply (MUL), divide (DIV), arithmetic shift (ASH), and arithmetic shift combined (ASHC). The option permits multiplication and division of signed 16-bit numbers and arithmetic shifting of signed 16-bit or 32-bit numbers. Condition codes are set on the result of each instruction.

The Kell-E (EIS) option is a single hex (six section) module (M7238) that plugs directly into slot A02-F02 of the processor system unit. The option functions as an extension of the basic KD11-A data paths, microbranch control, and control ROM. The basic processor timing is not degraded when this option is used. The NPR latency is not affected when the instructions are being executed. Interrupts are serviced at the end of each instruction in the standard manner.

There are no addressable registers in the Kell-E option. All operands are fetched from either core memory or from the general processor registers and the result of each operation is stored in the general registers.

The MUL instruction uses the contents of the effective address specified by the destination register and the source register as 2's complement integers which are multiplied. The result is stored in the source register and, if even, the low-order result in the succeeding register. If the source register address is odd, only the low-order product is stored. The MUL instruction multiplies full 16-bit numbers for a 32-bit product.

The DIV instruction permits a 32-bit dividend to be divided by a 16-bit divisor to provide a 16-bit quotient and a 16-bit remainder. The sign of the remainder is always the same as the sign of the dividend unless the remainder is zero. Overflow is indicated if more than 16 bits are required to express the quotient. In this case, the instruction is aborted, the overflow condition code is set, the expansion processor status (EPS) word is loaded into the processor PS register, and the program branches to a service routine. If the source register is zero, indicating divide by 0, an overflow is indicated.

When the ASH instruction is used, the contents of the selected register is shifted right or left the number of places specified by a count. This shift count is a 6-bit, 2's complement number which is the least significant 6 bits of the destination operand. If the count is positive, the number is shifted left; if it is negative, the number is shifted right. This allows for shifts from 31 positions left to 32 positions right (+31 to -32). A count of zero causes no change in the number.

When the ASHC instruction is used, the contents of a register (address R) and the contents of another register (address of the first register ORed with one, R+1) are treated as a single 32-bit word. Register R+1 represents bits 0-15, register R represents bits 16-31. This 32-bit word is shifted right or left the number of places specified by a count. This shift count is the same as that described for the ASH instruction and permits shifts from +31 to -32. If the selected register (R) is an odd number, then R and R+1 are the same. In this case, a shift becomes a rotate and the 16-bit word is rotated the number of counts specified by the shift count (up to 16 shifts).

Specifications for the KELL-E option are listed in Table 4-12 at the end of this paragraph. A detailed description of this option is given in the KELL Instruction Set Options Manual, DEC-11-HKEFA-A-D.

Table 4-12

KE11-E (EIS) Specifications

| | |
|----------------------|--|
| Instructions | Multiply (MUL) Divide (DIV) Arithmetic Shift (ASH) Arithmetic Shift Combined (ASHC) |
| Operations | Multiplication and division of signed 16-bit numbers. Arithmetic shifting of signed 16-bit or 32-bit numbers |
| Registers | None in option. Operands fetched from core or general processor registers. |
| Timing (approximate) | MUL = 9.5 us DIV = 10.5 us ASH = 3.4 us plus address calculation time plus 300 ns times absolute value of shift count ASHC = 3.8 us plus address calculation time plus 300 ns times absolute value of shift count |
| Size | Single hex module (M7238) |

4.3.2 KE11-F Floating Instruction Set (FIS) Option

The KE11-F Floating Instruction Set Option is a processor option that enables the KD11-A processor to perform arithmetic operations using floating-point arithmetic. The prime advantage of this option is increased speed without the necessity of writing complex floating-point software routines. The KE11-F performs single-precision operations. The KE11-F option cannot be used unless the KE11-E (EIS) option has been installed in the system.

The KE11-F (FIS) option is a single quad module (M7239) that plugs directly into slot A01-D01 of the processor system unit. If a BR request is issued before the instruction is within approximately 8 us of completion, the floating-point instruction is aborted. In this event, the program counter (PC) points to the aborted floating-point instruction, making the instruction the next instruction to be performed by the program. The NPR latency is not affected when floating-point instructions are being executed. Interrupts are serviced at the end of each instruction in the standard manner.

The FIS option provides four special instructions: floating-point addition (FADD), floating-point subtraction (FSUB), floating-point multiplication (FMUL), and floating-point division (FDIV).

Floating-point representation of a binary number consists of three parts: an exponent, a mantissa, and the sign of the mantissa. The mantissa is a fraction in magnitude format with the binary point positioned between the sign bit and the most significant bit. If the mantissa is normalized, all leading 0s are eliminated from the binary representation; the most significant bit is thus a 1. Leading 0s are removed by shifting the mantissa left; however, each left shift of the mantissa must be followed by a decrement of the exponent value to maintain the true value of the number. The exponent value represents the power of 2 by which the mantissa is multiplied to obtain the value to be used.

For FADD or FSUB operations, the exponents must be aligned (or equal). If they are not, the mantissa with the smaller exponent is shifted right until they are. Each right shift is accompanied by incrementation of the exponent value. Once the exponents are aligned (equal), the mantissa is added or subtracted. The exponent value indicates the number of places the binary point is to be moved in order to obtain the actual representation of the number.

For FMUL instructions, the mantissas are multiplied and the exponents are added. For FDIV instructions, the mantissas are divided and the exponents are subtracted.

The KE11-F Floating-Point option stores the exponent in excess 200_8 notation. Therefore, values from -128 to +127 are represented by the binary equivalent of 0 to 255 (octal 0-377). Mantissas are represented in sign magnitude form.

The binary radix point is to the left. The result of the floating-point operations is always rounded away from zero, increasing the absolute value of the number.

If the exponent is equal to 0, the number is assumed to be 0 regardless of the sign bit or fraction value. The hardware generates a clean 0 in this instance.

Specifications for the KE11-F option are listed in Table 4-13 at the end of this paragraph. A detailed description of this option is given in the KE11 Instruction Set Options Manual, DEC-11-HKEFA-A-D.

Table 4-13

KE11-F (FIS) Specifications

| | |
|--------------|---|
| Prerequisite | KE11-E Extended Instruction Set Option |
| Instructions | Multiply (MUL) Divide (DIV) Arithmetic Shift (ASH) Arithmetic Shift Combined (ASHC) Floating-point Addition (FADD) Floating-point Subtraction (FSUB) Floating-point Multiply (FMUL) Floating-point Divide (FDIV) |
| Operations | Multiplication and division of signed 16-bit numbers. Arithmetic shifting of signed 16-bit or 32-bit numbers. Single-precision floating-point addition, subtraction, multiplication, and division of 16-bit numbers. |
| Registers | None in option. Operands fetched from core or general processor registers (stack ordered) |
| Size | Single quad module (M7239) |

4.3.3 KJ11-A Stack Limit Register Option

The KD11-A processor is capable of performing hardware stack operations. Because the number of locations occupied by a stack is unpredictable, some form of protection must be provided to prevent the stack from expanding into locations containing other information. In the basic machine, this protection is provided by a fixed boundary. The KJ11-A Stack Limit Register Option provides a programmable boundary.

The KJ11-A consists of a single addressable register, accessible to both the console and the processor, that is used to change the stack limit and to provide warning (yellow zone violation) and error (red zone violation) indications to the processor. The stack limit register is an 8-bit register (high byte) that can be addressed either as a high-order byte (777775) or as a full word (777774).

During operation, the register is loaded with an address signifying the lower limit of the stack (stack violations occur at or below this limit). During subsequent stack pointer related bus operations (DATO, DATOB, and DATIP), if the address of the bus operation is less than the contents of the stack limit register, an error condition exists.

If the difference is less than or equal to 16 words, a yellow zone violation occurs. The operations that caused the yellow zone violation are completed and then a bus error trap occurs. This error trap, which itself uses the stack, executes without causing an additional violation.

If the space between the bus address and the stack limit register is greater than 16 words, then a red zone violation occurs and the operation causing the error is aborted. The stack is repositioned and a bus error trap occurs; that is, the old PS and PC are pushed into locations 2 and 0 and the new PC and PS are taken from locations 4 and 6. A red zone violation is a fatal stack error. Other fatal stack errors are odd stack or non-existent stack. Note that these two stack error conditions exist in the basic KD11-A processor; however, in this case the stack limit is fixed at memory location 400_8 . The option utilizes this 400_8 boundary also.

The KJ11-A Stack Limit Register Option is a single-height module that plugs into slot E03 of the processor.

Specifications for the KJ11-A option are listed in Table 4-14 at the end of this paragraph. A detailed description of this option is presented in the KD11-A Processor Manual, DEC-11-HKDAA-A-D.

Table 4-14

KJ11-A Specifications

| | |
|-----------------------|---|
| Register | 8-bit stack limit register (bits 15-08) addressable by console or processor, but not by any bus device |
| Register Address | 777774 (word addressing) 777775 (byte addressing) |
| Stack Limit | programmable; if register is all 0s, then: 000 - 337 = red zone 340 - 377 = yellow zone |
| Yellow Zone Violation | occurs if the stack operation's address is less than the stack limit address by 16 words or less. The operation is completed and then a TRAP is executed. |
| Red Zone Violation | occurs if the stack operation's address is less than the stack limit address by more than 16 words. The operation is aborted (fatal stack error), a stack vector exists at address 4, and a bus error TRAP occurs. The old PS and PC are pushed into locations 2 and 0; the new PC and PS are taken from locations 4 and 6. |
| PDP-11/40 Stack Limit | The PDP-11/40 System has a fixed stack limit at 377. Therefore, it is equivalent to the initialized state of the KJ11-A. |
| Size | one single-height module |

4.3.4 KT11-D Memory Management Option

The KT11-D Memory Management Option is a PDP-11/40 processor option that provides the capability to expand the 32K-word addressing of the KD11-A processor to 128K words and to enhance the use of multi-user, multi-program systems. A time-sharing environment is created by providing two operating modes: kernel and user. These modes can operate with or without relocation and protection. Mode selection is made by using an expanded KD11-A processor status word.

The KT11-D option basically performs four functions:

- a. Expands the basic 32-K word address capability to 128K words.
- b. Provides address space with memory relocation and protection for multi-user timesharing systems.
- c. Implements the separate address spaces for the kernel and user modes of operation.
- d. Provides memory management information for use of memory in multi-user, multi-program systems.

The standard 16-bit word length of the KD11-A processor limits the memory address capability to 32K words. In addition, the upper 4K of address space is always reserved for internal register and external device addresses. The KT11-D converts the 16-bit virtual address generated by the processor to an 18-bit physical bus address, thereby increasing the usable memory address capability from 28K to 124K words.

Because the KT11-D option relocates all addresses automatically, the KD11-A processor may be considered to be operating in a virtual address space. This means that no matter where a program is loaded into physical memory, it does not have to be re-linked; it always appears to be at the same virtual location in memory.

In a multi-programmed, timeshared system, user programs must be prevented from modifying or destroying the operating system. The KT11-D option implements the kernel/user modes of operation upon which the timeshared system is based. The option uses two sets of eight 32-bit Active Page Registers (APR). An APR is actually a pair of 16-bit registers: a Page Address Register (PAR), and a Page Descriptor Register (PDR). These registers are always used as a pair and contain all the information needed to describe and locate the currently active memory pages. One PAR/PDR set is provided for each mode of operation (kernel and user). Logic within the KT11-D analyzes every memory

reference to enable the correct PAR/PDR set. Thus, a user mode program, for example, cannot operate in the space assigned to kernel programs.

In a multi-program, multi-user environment, memory space must be used in the most efficient method possible in order to accomodate as many users as possible with minimum delay. The KT11-D option maintains bits that indicate whether the associated page has ever been written into. The software memory management system can interrogate each PDR to determine how that page had been used. This information enables the software system to evaluate the overall use of available memory space. For example, if an active memory page has never been altered, the memory management system might, if necessary, overlay that page with a new program requested by a user. If a current active page has been written into, the memory management operating system needs to be informed so that the modified program can be rewritten into secondary storage before the page is overlaid.

Specifications for the KT11-D Memory Management Option are listed in Table 4-15 at the end of this paragraph. A detailed description of this option is given in the KT11-D Memory Management Option Manual, DEC-11-HKTDA-A-D.

Table 4-15

KT11-D Specifications

| | |
|------------------|---|
| Memory Expansion | Expands PDP-11/40 memory address capability up to 124K words. |
| Interface | Address line outputs compatible with PDP-11 Unibus |
| Timing | Timing derived from KD11-A processor |
| Delay | Adds 150 ns to every memory reference when installed. |
| Operating Modes | Kernel and user |
| Available Pages | Provides 8 4K-word pages for each mode |
| Page Length | A page can vary in length from one 32-word block up to 128 32-word blocks. Maximum page length is 4096 words. |
| Program Capacity | Eight 4096-word pages accomodate 32K-word programs. |
| Size | Single hex-size module (M7236) |

4.3.5 KW11-L Line Frequency Clock

The KW11-L Line Frequency Clock is a PDP-11/40 processor option that provides a method of referencing real intervals. This option generates a repetitive interrupt request to the processor. The rate of interrupt is derived from the ac line frequency, either 50 Hz or 60 Hz. The accuracy of the clock period, therefore, is dependent on the accuracy of this frequency source.

The KW11-L Line Frequency Clock can be operated in either an interrupt or non-interrupt mode. When in the interrupt mode, the clock option interrupts the processor each time it receives a pulse from the line frequency source. In the non-interrupt mode, the clock option functions as a program switch that the processor can examine or ignore. Mode selection is made by the program.

Specifications for the KW11-L Line Frequency Clock Option are listed in Table 4-16 at the end of this paragraph. A detailed description of this option is given in the KW11-L Line Time Clock Manual, DEC-11-HKWB-D.

Table 4-16

KW11-L Specifications

| | |
|------------------|--|
| Register | 2-bit status register bit 06 - interrupt enable bit 07 - interrupt monitor |
| Register Address | 777546 |
| Vector Address | 100 |
| Mode Control | bit 06 set - interrupt mode bit 06 clear - non-interrupt mode |
| Monitor Function | bit 07 can be used to serve as a partial check on the origin of the interrupt vector |
| Interrupt Rate | same as line frequency; 50 or 60 Hz |
| Priority Level | BR6 |
| Size | Single-height module (M787) that mounts in KD11-A processor slot F3 |

4.3.6 KM11-A Maintenance Console Option

The KM11-A Maintenance Console (Also referred to as the maintenance module) is a 2-module set containing 28 indicator lights and four switches used to monitor and control functions during maintenance tests.

The functions monitored by the option depend on which processor slot the module is installed in. Different overlays are provided to indicate the function being tested. The module is installed in processor slot F01 when testing the KD11-A processor and is installed in slot E01 when testing the KT11-D or KE11-E,F options.

Use of the maintenance module, including a description of the overlays, is given in the KD11-A Processor Manual, DEC-11-HKDAA-A-D and in the appropriate option manuals. Also, a detailed description of the option is presented in the KD11-A Processor Manual.

4.3.7 Small Peripheral Controller Slot

Processor slot 09, sections C-F, permit installation of any small peripheral controller option. This slot is normally used to install the controller for the PDP-11/40 System input/output console device, but may be used for any small peripheral controller, if desired.

The standard controllers for system I/O devices are:

- a. DL11 Asynchronous Line Interface - the standard controller used for either the LA30-S DECwriter or for the ASR 33 Teletype unit.
- b. LC11 DECwriter Control - a controller used when the LA30-P DECwriter is used as the system I/O device.
- c. KL11 Teletype Control - an earlier version of the Teletype Control which is used only with the ASR 33 Teletype unit.

A brief description of the LC11 and DL11 are given in paragraphs 1.3.6 and 1.3.7, respectively, of this manual.

Detailed descriptions of all three controllers are included in the related maintenance manual listed in Table 1-2.

4.4 MEMORY OPTIONS

Memories with different ranges of speeds and various physical and electrical characteristics can be freely mixed and interchanged in a single PDP-11/40 System. The basic system mounting box can house up to 56K of memory in addition to the processor and processor options. Additional memory units may be added by using separate boxes and power supplies. Each box may be expanded up to 24K in 8K increments.

The following paragraphs describe four of the core memory types that can be used with the PDP-11/40 System. It should be noted that core memories compatible with the PDP-11/20 may also be used with the PDP-11/40 provided they are mounted in a different box and powered by an H720 power supply.

4.4.1 MM11-L Core Memory

The MM11-L core memory is a read/write, random access, coincident current, magnetic core type memory with a cycle time of 900 ns and an access time of 400 ns. The memory is organized in a 3D, 3-wire planar configuration. It provides 8192 (8K) 16-bit words that are both word and byte addressable.

The memory is organized into 16-bit words, each word containing two 8-bit bytes. The bytes are identified as the low-order byte (bits 00-07) and the high-order byte (bits 8-15). Each byte is addressable and has its own address location. Low bytes are always even numbered and high bytes are odd numbered. Full words are addressed at even-numbered locations only. When a full word is addressed, the high byte is automatically included. For example, the 8K memory has 8,192 words or 16,384 bytes; therefore, 16,384 locations are assigned. Address 000000 is the first low byte, address 000001 is the first high byte, 000002 is the second low byte, 000003 is the second high byte, etc.

The MM11-L consists of three modules: a G110 hex-type module containing the memory control logic; a G231 hex-type module containing the memory driver logic; and an H214 quad-type module containing the memory core stack.

The memory control logic acknowledges the request of the master device, determines which of the four basic operations (DATI, DATIP, DATO, or DATOB) is to be performed, and sets up appropriate timing and control circuits to perform the desired read or write operation. It also contains the inhibit drivers and sense amplifiers as well as device selector logic to determine if the memory bank has been addressed from the Unibus. The control logic includes a 16-bit flip-flop register that stores the contents of a word after it is read out from destructive memory. This same word can then be written back into memory (restored) when in the DATI mode. The register is also used during DATO and DATOB cycles to accommodate loading of incoming data from the Unibus lines into the core memory.

The memory driver logic includes: address selection logic that decodes the incoming address to determine the core specifically addressed; the switches and drivers that direct current flow through the magnetic cores to ensure the proper polarity for the desired function; and the X and Y current generators that provide the necessary current to change the state of the magnetic cores.

The ferrite core memory stack consists of 16 memory mats arranged in a planar configuration. Each mat contains 8192 ferrite cores arranged in a 128 by 64 matrix. Each mat represents a single bit position of a word. Each ferrite core can assume a stable magnetic state corresponding to either a binary 1 or binary 0. Even if power is removed from the core, the core retains its state until changed by appropriate control signals.

Information for installation of the MM11-L in the BA11-FC box of the PDP-11/40 is noted in Table 2-2.

4.4.2 MF11-L Core Memory

The MF11-L core memory is basically a standard MM11-L, 8K core memory with the addition of a backplane. The backplane provides the interconnections between the core memory modules. The MF11-L is the normal memory supplied with the PDP-11/40 System.

Information for installation of the MF11-L in the BA11-FC box of the PDP-11/40 is noted in Table 2-2.

4.4.3 ME11-L Core Memory

The ME11-L is a complete memory system consisting of an MM11-L core memory and associated backplane (MF11-L) housed in its own mounting box which contains an integral power supply. This power supply and mounting box can accommodate up to three MM11-L core memories. In effect, the ME11-L can be expanded up to 24K in 8K increments.

The system mounting box is $5\frac{1}{2}$ inches high, 19 inches wide, and 20 inches deep and is designed for mounting in a standard 19-inch cabinet. Rack-mountable slides are included but the box can be used as a stand-alone unit, if desired. In addition to holding the core memory, backplane, and power supply, the box contains all cables necessary for providing power and for interfacing the units of the ME11-L. It also provides for connection to the Unibus. The rear of the box contains cable clamps, a line cord for input power, a cooling fan for the memory modules and power supply, and a power control circuit breaker.

The system power supply converts single-phase 115V or 230V ac line voltage to the two regulated dc voltages required by the memory system: +5V for the logic and -15V for the core memory. Both outputs are overvoltage and overcurrent protected. The power supply also provides line power to the mounting box cooling fan and the BUS AC LO and BUS DC LO signals which are sent to the Unibus in the event of a power failure.

The power supply consists of a power control, a power chassis assembly, and a dc regulator along with associated ac and dc cables. The power control contains a thermal circuit breaker which protects against input overload and is reset by depressing a button on the rear of the mounting box. A thermostat in the regulator opens one side of the primary circuit and deenergizes the power supply if the temperature rises above 100° C. It is automatically reset when the temperature reaches 63° C.

4.4.4 MM11-S Core Memory

The MM11-S core memory is an MM11-L memory with backplane and is capable of being interleaved in 16K segments. This permits the memory to be expanded above the 24K limit of the MF11-L. The prime physical difference between the MM11-S and the MF11-L is that the MM11-S is a single system unit while the MF11-L is a double system unit.

If the MM11-S is interleaved, it permits faster memory operation. When interleaved, two adjacent contiguously addressed 8K memory banks are used and successive memory cycles are performed within alternate 8K memory blocks.

5 UNIBUS AND SYSTEM OPTIONS

5.1 SCOPE

The purpose of this chapter is to provide a general description of the Unibus that is used to interconnect all major components of the PDP-11/40 System. In addition, it provides brief descriptions of some of the Unibus options (peripherals) that can be used with the PDP-11/40. Because of the Unibus concept, these peripherals can be used, without modification, with any member of the PDP-11 family of computers.

Detailed information on the Unibus and peripheral interfacing is provided in the PDP-11 Peripherals and Interfacing Handbook.

5.2 UNIBUS

The Unibus is a single, common path that connects the processor, memory, and all peripherals. Address, data, and control information is transmitted along the 56 lines of the bus. The form of communication is the same for every device on the Unibus. The same signal format is used by the processor to communicate with memory and peripheral devices. Peripheral devices also use this format when communicating with the processor, memory, or other peripheral devices.

All instructions applied to data in memory can be applied equally well to data in peripheral device registers and peripheral device registers may be manipulated as flexibly as memory by the processor. This is an especially powerful feature, considering the special capability of PDP-11/40 instructions to process data in any memory location as though it were an accumulator.

Most Unibus lines are bidirectional; therefore, the input lines can also be driven as output lines. This means that a peripheral device register can be either read or changed by the processor or other peripheral devices, and the same data lines can be used for transfer operations. Thus, the same register can be used for both input and output functions.

Communication between two devices on the bus is in a master-slave relationship. During any bus operation, one device has control of the bus. This device, the bus master, controls the bus when communicating with another device on the bus, called the slave. A typical example of this relationship is the processor, as master, fetching an instruction from memory (which is always a slave). Another example is the disk, as master, transferring data to memory, as slave. Master-slave relationships are dynamic. The processor, for example, passes bus control to a disk. The disk, as master, then communicates with a slave memory bank.

The Unibus is used by the processor and all I/O devices; thus, a priority structure determines which device obtains control of the bus. Consequently, every device on the Unibus capable of becoming bus master has an assigned priority. When two devices, which are capable of becoming bus master, have identical priority values and simultaneously request use of the bus, the device that is electrically closest to the processor receives control.

Communication on the Unibus is interlocked between devices. Each control signal issued by the master device must be acknowledged by a response from the slave to complete the transfer. Therefore, communication is independent of the

physical bus length and the response time of the master and slave devices. The maximum transfer rate on the Unibus with optimum device design, is one 16-bit word every 400 ns, or 2.5 million 16-bit words per second.

Registers in peripheral devices are assigned addresses similar to memory; thus all PDP-11/40 instructions that address memory locations can become I/O instructions. Data registers in devices can take advantage of all the arithmetic and logic power of the processor. The PDP-11/40 controls devices differently than most computer systems. Control functions are assigned a register address, and then the individual bits within that register can cause control operations to occur. For example, the command to make the paper-tape reader read a frame of tape is provided by setting a bit (the reader enable bit) in the control register of the device. Instructions such as MOV and BIS may be used for this purpose. Status conditions are also handled by the assignment of bits within this register, and the status is checked with TST, BIT, and CMP instructions. In addition, there is no limit to the number of registers that a device may have, providing an unlimited flexibility in the design and control of peripheral equipment. The same bit locations in peripheral registers are assigned to the same or similar operation. For example, regardless of the device, bit 15 usually represents an ERROR flag.

A device (other than the processor) that is capable of becoming bus master generally requests use of the bus for one of two purposes:

- a. To make a non-processor transfer of data directly to or from memory by means of a non-processor request (NPR).
- b. To interrupt program execution and force the processor to branch to a specific address where an interrupt service routine is located by means of a bus request (BR).

The request and granting of bus mastership is performed in parallel with data transfers on a completely independent set of bus lines. Thus, while one device is using the bus, the next request is being checked for priority and the next user is being assigned. Because of this time parallelism, successive data transfers by different master devices can occur at the full Unibus speed.

When a device capable of becoming bus master requests use of the bus, the handling of that request depends on the location of that device in the priority structure. The following factors must be considered to determine the priority of the request:

- a. The processor's priority is set under program control to one of eight levels using bits 7,6, and 5 in the processor's status register. These three bits set a priority level that inhibits granting of bus requests (BRs) on the same or lower levels.
- b. Requests from external devices can be made on any one of five request lines. Non-processor request (NPR) has the highest priority, and its request is granted by the processor between bus cycles of an instruction execution. Bus request 7 (BR7) is the next highest priority and bus request 4 (BR4) is the lowest.

The four lower level priority requests (BR7 to BR4) are granted by the processor between instructions. When the processor priority is set to a specific level, all bus requests on that level and below are ignored. For example, if the processor priority is 6, requests on BR6 or any other lower level are not granted.

- c. When more than one device is connected to the same bus request line, the device electrically nearer the processor has a higher priority than the device further away. Any number of devices can be connected to a specific BR or NPR line.

When a device other than the processor gains control of the bus, it uses the bus to perform either a data or interrupt transfer.

Direct memory or device access data transfers can be accomplished between any two peripherals without processor supervision. These are called NPR level data transfers. Normally, NPR transfers are made between the memory and a mass storage device, such as a disk. During NPR transfers, it is not necessary for the processor to transfer the information between the memory and the mass storage device. The bus structure allows device-to-device transfers, thereby allowing customer-designed peripheral controllers to directly access other devices (such as disks) on the bus. This direct access capability permits operations such as a disk directly refreshing a CRT display. An NPR device is allowed extremely fast access to the bus and can transfer data at high rates once it gains control. The processor state is not affected

by this type of transfer; therefore, the processor can relinquish bus control while an instruction is in progress. This release of the bus normally occurs at the beginning or end of bus cycles; however, the bus is never released between cycles of a read-modify-write sequence.

Devices that gain bus control with one of the bus request lines (BR7, BR6, BR5, BR4) can take full advantage of the power and flexibility of the processor by requesting an interrupt. The entire instruction set is then available for manipulating data and status registers. When a device servicing program is to be run, the task being performed by the processor is interrupted, and the device service routine is initiated. After the device request has been satisfied, the processor returns to its former task. Note that interrupt requests can be made only if bus control has been gained through a BR priority level. An NPR level request can never be used for an interrupt request.

5.3 UNIBUS OPTIONS

A large number of Unibus options are available for use with the PDP-11/40 System. A brief description of some of these options is included in the following paragraphs. For more detailed information, refer to the associated hardware maintenance manual.

5.3.1 PC11 High-Speed Paper-Tape Reader/Punch

The High-Speed Reader and Punch is capable of reading 8-hole uncoiled perforated paper tape at 300 characters per second, and punching tape at 50 characters per second. The system consists of a High-Speed Paper-Tape Reader/Punch and the PC11 Control. A unit containing a reader only (PR11) is also available.

In reading tape, a set of phototransistors translate the presence or absence of holes in the tape to logic levels representing 1s and 0s to the presence or absence of holes in the tape. Any information read or punched is parallel-transferred through the control. When an address is placed on the Unibus, the control decodes the address and determines if the reader or punch has been selected. If one of the four device register addresses have been selected, the control determines whether an input or an output operation should be performed. An input operation from the reader is initiated when the processor transmits a command to the paper-tape reader status register. An output operation is initiated when the processor transfers a byte to the paper-tape punch buffer register.

The control enables the PDP-11 System to control the reading or punching of paper tape in a flexible manner. The reader can be under direct program control or can operate without direct supervision through the use of interrupts to maintain continuous operation.

5.3.2 LP11 High-Speed Line Printer

The LP11 High-Speed Line Printer is available in several models, ranging from an 80-column, 64-character model (LP11-FA) to an 132-column, 96-character model (LP11-HB). Either column-width printer can be ordered with 64- or 96-character print sets. The printer is an impact type using a revolving character drum and one hammer per column. Forms up to six parts may be used for multiple copies. Fanfold paper from 4 inches to 14 7/8 inches wide may be used with adjustment for pin-feed tractors. The print rate is dependent upon the data and the number of columns to be printed. Characters are printed 20 at a time (24 on the 132-column model) and if 20 (or 24) or less are used, the rate can be as high as 1100 lines per minute.

An 8-bit value, representing a character to be printed, is transferred in parallel from the Unibus to the line printer. The line printer then loads the character serially into the printer memory via the line printer buffer (LPB). When the memory becomes full (20 characters) the characters are automatically printed. This continues until the full 80 columns have been printed or a special character is recognized. The 132-column model prints 24 characters at a time.

5.3.3 CR11 Card Reader

Model CR11 Card Reader reads EIA standard 80-column punched data cards at 300 cards per minute; model CM11 reads 40-column mark-sense cards, which can have punched holes, at 200 cards per minute.

The punched card reader uses a vacuum picker which works in conjunction with riffle air so that card wear is insignificant, card jam virtually impossible and the reader extremely tolerant of damaged cards. The riffling action separates the cards in the input hopper to prevent sticking. The picker uses a strong vacuum to grasp the bottom card and deliver it to the read station on demand. The picker and associated throat block prevent the unit from multiple picking to the extent that taped or stapled cards are not allowed to enter the card track. In such cases the reader stops with pick check alarm. The operator can separate the cards and enter them into the input hopper for normal reading. The card track is very short, so that only one card is in motion at a time. The combination of damaged card tolerance, gentle card handling, and short card track provide virtually jam-proof operation.

Cards are read by column, beginning with Column 1. A select

instruction starts the card moving past the read station. Once a card is in motion, all 80 columns are read. Column information is read in one of two program-selected modes: card image or compressed code. In the card image mode 12 information bits in one column are loaded into the data buffer and are available to the program at CRB1 address. In the compressed code mode, the card image is encoded into 8-bit bytes and is available to the program at CRB2 address. A punched hole is interpreted as binary 1, and the absence of a hole as binary 0.

5.3.4 TC11/TU56 DECTape System

The TC11/TU56 is a dual-unit, bidirectional magnetic - tape transport system for auxiliary data storage. Low cost, low maintenance and high reliability are assured by:

- a. simply designed transport mechanisms which have no capstans and no pinch rollers.
- b. hydrodynamically lubricated tape guiding (the tape floats on air over the tape guides while in motion)
- c. redundant recording
- d. Manchester recording techniques (virtually eliminate drop-outs)

Each transport has a read/write head for information recording and playback on five channels of tape. The system stores information at fixed positions on magnetic tape as in magnetic disk or drum storage devices, rather than at unknown or variable positions as in conventional magnetic tape systems. This feature allows replacement of blocks of data on tape in a random fashion without disturbing other previously recorded information. In particular, during the writing of information on tape, the system reads format (mark) and timing information from the tape and uses this information to determine the exact position at which to record the information to be written. Similarly, in reading, the same mark and timing information is used to locate data to be played back from the tape.

The DECTape system consists of the TU56 dual transport, the TC11 Control (which will buffer and control information for up to four dual transports) and DECTape(3/4 inch magnetic tape on 3.9inch reels).

The system utilizes a 10-track read/write head. On a tape the first five tracks include a timing track, a mark track, and three data tracks. The other five tracks are identical counterparts and are used for redundant recording to increase system reliability. The redundant recording of each character bit on non-adjacent tracks materially reduces bit dropout and minimizes the effect of skew. The use of Manchester phase recording, rather than amplitude sensing techniques, virtually eliminates dropouts.

5.3.5 TM11/TU10 DECmagtape System

The TM11/TU10 is a high-performance, low-cost magnetic tape system ideally suited for writing, reading, and storing large volumes of data and programs in a serial manner.

Because the system reads and writes in industry-compatible format, information can be transferred between a PDP-11 and other computers. For example, a PDP-11 might be used to collect data and record it for later processing on a large

computer. The 10 1/2 inch tape reels contain up to 2400 feet of tape upon which over 96 million bits of data can be stored on high density 9-track tape or over 72 million bits can be stored on high density 7-track tape.

The TM11/TU11 employs read after write error checking to check that proper data is written on the tape. Should a tape dropout be detected, appropriate action can be taken to assume no loss of data.

Tape motion is controlled by vacuum columns and a servo-controlled single capstan. Long tape life is possible because the only contact with the oxide surface is at the magnetic head and at a rolling contact on one low-friction, low-inertia bearing.

5.3.6 RC11/RS64 DECdisk Memory

The RC11/RS64 is a fast, low-cost, random access, bulk storage system. One RC11/RS64 combination provides 65,536, 16-bit words of storage. Up to four RS64 disks can be controlled by one RC11 Controller for a total of 262,144 words of storage. Disk functions include: look ahead, read, write, and write check, as well as a "look ahead" register which indicates current disk position.

The RS64 disk stores data in a 32 x 16-bit word block format. Cyclic Redundancy Check (CRC) error detection is performed automatically by the controller on a block basis, the blocks being randomly addressable. A self-synchronizing, phase lock clock recovery system is used to ensure exceptional data reliability. This technique facilitates data recovery in of restart after a power failure or during periods of high shock or vibration.

Fast track switching time permits spiral read and write. Data may be read or written as 32-word blocks from one to 65,536 words. When the last address on a track or surface has been used, the RC11 Controller will automatically advance to the next track or to the first track of a new disk surface.

Each RS64 disk unit has a set of switches for Write protecting the disk. The Write Lock ENABLE/DISABLE switch determines whether protection is desired or not. If this switch is in ENABLE position, writing data on tracks selected by five switches is not allowed. The setting of five switches below the ENABLE/DISABLE switch forms a binary number that corresponds to the number of a track; when write protection is in effect, all tracks numbered from zero to the selected number (both inclusive) are write protected. Any attempt to write in a write protected area will result in an error indication by the controller.

5.3.7 RF11/RS11 Disk System

The RF11 Controller and RS11 Disk combine as a fast, low-cost random-access bulk-storage package for the PDP-11. One RS11 and the RF11 provide 262,144 17-bit words (16 data bits and 1 parity bit) of storage. Up to eight RS11 disks can be controlled by one RF11 for a total of 2,047,152 words of storage.

The RF11/RS11 is unique in fixed head disks because each word is addressable. Data transfers may be as small as one word or as large as 65,536 words. Individual words or groups of words may be read or rewritten without any limits of fixed blocks or sectors, providing optimum use of both disk storage and main memory in the PDP-11 system.

The RS11 contains a nickel-cobalt-plated disk driven by a hysteresis synchronous motor. Data is recorded on a single disk surface by 128 fixed read/write heads.

Fast track switching time permits spiral read or write. Data may be written in blocks from 1 to 65,536 words. The RF11 control automatically continues on the next track, or on the next disk surface, when the last address on a track or surface has been used.

The disk stores data words in a 22-bit format which includes guard bits and a sync bit to operate the self-clocking logic of the RS11 Disk logic. The sync bit adjusts the timing of the data strobing to ensure proper recovery of each word of data. The RS11 has a redundant set of timing tracks, recorded exactly in phase with the primary timing tracks.

5.3.8 RK11-C DECpack Disk Cartridge System

The DECpack cartridge disk drive and control is a complete mass storage system, offering an economical solution for large volume, random-access data storage. The system includes a modular mass storage device utilizing removable disk cartridges and a complete easy-to-program control.

The DECpack is available in two models: The RK02 drive with over 600,000 words per drive; and the RK03 drive with over 1.2 million words of storage per drive.

The DECpack is ideal where a large volume of programs and data are developed and maintained for one or more users. When used with PDP-11 software such as the Disk Operating System or RSTS-11 System, DECpack offers the flexibility of permitting each member of a group of users to maintain his own private program and data files. It is expandable up to 4.8 million words (RK02) or 9.6 million words (RK03 or RK05) per controller.

The removable disk cartridge offers the flexibility of virtually unlimited off-line capacity with rapid transfers of files between on-line and off-line without copying operations. It utilizes a cartridge similar to the IBM 2315, but with 12 sectors.

Average total access time on each drive is 90 milliseconds. On expanded systems, operations are overlapped for efficiency; one drive may read or write while one or more additional drives are seeking new head positions for the next transfer. All data transfers utilize the non-Processor Request facility during transfers.

Each disk is permanently mounted inside a protective case that automatically opens when inserted in the disk drive. While on-line, dust contamination is prevented by a highly-efficient continuous "absolute" air filtration system.

The DECpack provides accurate data storage and transfers by means of a write check function, correct cylinder verification by hardware, hardware checksum, and hardware maintenance features. There are no mechanical detents, thus a major source of wear and critical adjustment is eliminated.

5.3.9 VT01 Storage Display

The VT01A is a Tektronix Model 611 direct-view storage tube with a resolution of 400 stored line pairs vertically and 300 stored line pairs horizontally. Dot writing time is 20 μ s , with a full screen erase time of 500 ms. The VT01 can display 30,000 discrete resolvable points.

The VT01A is interfaced to the Unibus and controlled via the AAll-A and AAll-D conversion subsystem.

5.3.10 VR01 Oscilloscope Display

The VR01A, a modified Tektronix type Rm504 oscilloscope, provides accurate measurements in DC-to-450 KHz applications. It is a low-frequency, high-sensitivity display and can be used for accurate curve plotting in the X-Y mode of operation.

The VR01 is interfaced to the Unibus and controlled by means of the AAll-B and AAll-D Digital-to-Analog Conversion Subsystem.

5.3.11 VR14 Point Plot Display

The VR14 is a completely self-contained CRT display with a 6.75 by 9-inch viewing area in a compact 19-inch package. The VR14 requires only analog X and Y position information with an intensity pulse to generate sharp, bright point plot displays. Except for the CRT itself, the unit uses all solid-state circuits with high-speed magnetic deflection to enhance brightness and resolution. The intensity pulse may be time multiplexed or gated by a separate input to allow the screen to be timeshared between two inputs. The display unit is available in rack-mountable or stand-alone models.

The VR14 is interfaced to the Unibus and controlled through the AAll-C and AAll-D Digital-to-Analog Conversion subsystem.

A two-color display (VR20) is also available. It is used with the AAll-E and AAll-D Digital-to-Analog Conversion subsystems.

5.3.12 VT05 Alphanumeric Display

The VT05 is a flexible, high performance alphanumeric display terminal with a cathode ray tube display and communications equipment capable of transmitting data over standard phone lines and data sets at half or full duplex at rates up to 300 Baud.

It is controlled by the DL11, the same controller used with Teletype terminals, or it may be used over a Bell 103A or equivalent modem.

5.3.13 RT01 DEClink Terminal

DEC-link is a low-cost, self contained data entry device which is remotely locatable. It features Teletype and EIA serial line compatibility. DEC-link offers 16 unique keyboard characters which a monitoring computer may use for either numeric data or control functions. It can display up to 12 digits of decimal data (plus decimal point) as well as status indicators.

Data is entered via an integral 16-character keyboard; numeric data is displayed locally. The status indicators are used to indicate non-numeric information such as "repeat transmission", "computer ready", etc. Four programmable status indicators are standard on DEC-link.

The DL11 Control may be used with the RT01 for direct connection or it may be used over a Bell 103A or equivalent modem.

5.3.14 Communications Options

DIGITAL has extended the PDP-11's adaptability to various communications applications with a variety of interfaces. These devices enable the PDP-11 to be connected both locally and remotely to serial asynchronous and serial synchronous lines. The interfaces allow both full and half duplex operations with connections to communications terminals via the standard EIA RS232-C and CCITT interface. The devices are summarized below:

| <u>DEVICE</u> | <u>INTERFACES PDP-11 WITH:</u> | <u>TYPICAL USES</u> |
|---------------|------------------------------------|---|
| DC11 | Serial Asynchronous Line | Connects PDP-11 to various asynchronous terminals, or to another computer via a common carrier communications facility. Has program controlled Baud rates, character lengths, and stop codes. |
| DP11 | Serial Synchronous Line | Connects PDP-11 to local or remote computers and terminals via high speed serial line. |
| DN11 | Autocalling Unit | To dial remote computer or terminal. |
| DM11 | Up to 16-serial Asynchronous Lines | Terminal-oriented systems for timesharing, message switching, store and forward, data collection, remote concentrators. |
| DL11 | Serial 8-bit Asynchronous Line | Connects PDP-11 to local teletype connections and local 8-bit current mode devices. |

DL11

Serial 8-bit
Asynchronous Line

Connects PDP-11 to local or remote 8-bit EIA-compatible asynchronous terminals such as CRTs, plotters, card readers, and line printers.

5.3.15 AFC11 Low-Level Analog Input Subsystem

The AFC11 is a flexible, high performance, differential analog input subsystem for IDACS-11 industrial data acquisition control systems.

The AFC11 system multiplexes up to 1024 differential input analog signals, selects gain, and performs a 13-bit analog-to-digital conversion at a 200 channel per second rate under program control. Three signal conditioning modules and eight program-selectable gains allow the system to intermix and accept a wide range of signals: low level (10mv f.s.), high level (100.0v f.s.), and current inputs (1 to 50ma f.s.).

Designed for accurate and reliable operation in demanding industrial environments, the AFC11 achieves high isolation and common mode noise rejection through relay switched capacitor multiplexing. The subsystem also simplifies input wiring, requiring only simple twisted pairs which connect to screw terminals.

Modularly constructed in eight-channel standard hardware units, the AFC11 is easy to configure to user applications, and simple to expand.

The analog input subsystem is particularly suited for data

acquisition in the high noise environments encountered in process monitoring and control, production testing and laboratory applications. In such environments common and normal mode noise, cabling and grounding problems can greatly affect the operation of such transducers as thermocouples, strain gages, analytical bridges, and industrial milliamp, current transmitters. These problems can also affect the accuracy and performance of the measuring system.

In typical applications, use of ungrounded sensors could cause common mode voltages of up to 150 volts peak-to-peak (at power line frequency) to appear on the input signal leads to the measuring system. For example, if thermocouples become ungrounded during operation, large common mode voltages can appear in coincidence with the signal. The design features of the AFC11 allow either floating or grounded signal sources thus insuring reliable, trouble - free operation. Due to the flying capacitor design, the system tolerates common mode voltages in excess of 200 volts. FET solid-state multiplexers, in contrast, can be seriously damaged with common mode voltages over 25 volts.

5.3.16 AD01-D Analog-to-Digital Conversion Subsystem

The AD01-D is a flexible, low-cost multichannel analog data acquisition option which interfaces directly to PDP-11 computers. When it is under computer or external clock control, the AD01-D provides 10-bit digitization of unipolar high-level analog signals having a nominal full-scale range of 0 to ± 1.25 , ± 2.5 , ± 5.0 or ± 10.0 volts. An optional sign-bit addition allows 11-bit bipolar operation. Programmable input range selection extends the AD01-D's dynamic range at moderate sampling rates the the equivalent of 13 bits for unipolar signals or 14 bits for bipolar signals.

An optional sample-and-hold amplifier reduces the conversion aperture to 100 nanoseconds.

Available as a factory or field-installed PDP-11 option, the standard AD01-D consists of an expandable solid-state input multiplexer, programmable input range selector, A/D converter, control, and bus interface in a single 5 1/4 inch rackmountable assembly plus a separate logic power supply. The multiplexer can be expanded by adding 4-channel modules up to 32 channels. An expansion multiplexer may be added to provide a maximum configuration of 64 channels.

The subsystem is well suited to a variety of tasks-testing, monitoring, logging, and analytical instrument data reduction - in both laboratoy and manufacturing environments. It is also a first choice with OEM's and system contractors as an economic and efficient system component for sophisticated data acquisition systems.

5.3.17 AAll-D Digital-to-Analog Conversion Subsystem

The AAll-D is a low cost, high performance multichannel digital to analog conversion subsystem for PDP-11 computers.

Interfacing directly to the PDP-11 Unibus, the AAll-D controls up to four single buffered, 12 bit bipolar digital to analog converters. Each BA614 converter, which includes output amplifier and reference voltage source, is contained on a plug-in module and provides 10 ma current output at ± 10 volts. Full scale output voltage is trimpot adjustable from $\pm 1v$ to $\pm 10v$ in two ranges.

Storage scope, display scope, and light pen control options are available for the AAll-D. These options provide Z axis blanking for intensity control and require two D/A converters to control X and Y trace coordinates.

Available as a factory or field installed option, the AAll-D fully implemented with four digital to analog converters and a scope control option, is contained in a single System Unit. A rack mountable power supply is separate.



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6 EQUIPMENT MOUNTING AND POWER

6.1 SCOPE

The purpose of this chapter is to provide detailed information on the PDP-11/40 mounting and power system.

The BA11-FC mounting box is basic to the PDP-11/40 mounting system and is discussed in paragraph 6.2. System unit allocations as well as processor and basic memory slot allocations are noted for the basic box. This mounting information is presented in context with the system mounting space within the same cabinet and in adjacent cabinets (paragraph 6.3).

System power is provided by a cabinet ac power control unit (paragraph 6.4) and a basic power supply. This power supply (paragraph 6.5) consists of an H742 bulk power supply and its individual H744 (+5V) and H745 (-15V) regulators. These three items are covered separately in paragraphs 6.5.1 through 6.5.3.

Basic dc power distribution is covered in paragraph 6.5.4 and troubleshooting of the power system is described in paragraph 6.5.5.

6.2 SYSTEM MOUNTING BOX

The major components of the PDP-11/40 System, with the exception of the power system and console I/O device, are mounted in a single BA11-FC mounting box. Space for additional memory and/or peripheral interfaces is also provided within this mounting box.

The BA11-FC mounting box is mounted in a standard DEC H960-C cabinet as shown in Figure 6-1. The box is mounted on Chassis slides so that it can be pulled out for maintenance and/or installation of logic modules; the power supply, however, remains within the cabinet. Cooling fans are mounted on top of the box to provide proper cooling of the logic elements within the box. The KY11-D Programmer's Console is located on the front of this box.

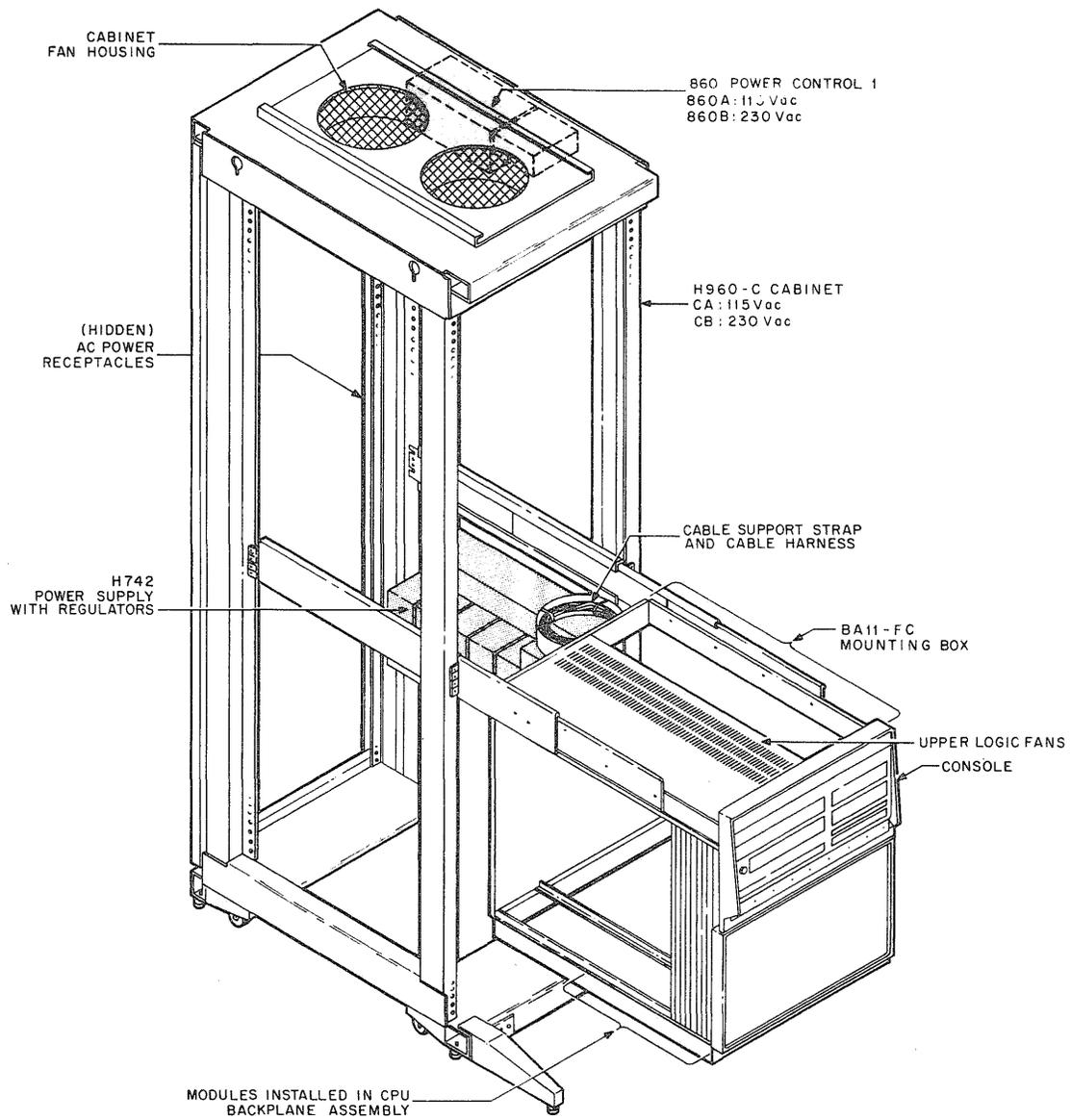
The mounting box is capable of holding nine system units or equivalents. Each system unit casting contains four slots for mounting logic modules. An alternate double system unit contains nine slots as it has no center casting. This double system unit is used for the KD11-A processor and MF11-L memory.

Allocation of logic within the box is shown in Figure 6-2. A double system unit (with nine slots) is used for the processor and processor options. Another double system unit is used for the MF11-L core memory which includes three modules to provide a basic 8K memory. This leaves space for five additional system units (or equivalents) for additional memory and/or peripheral interfaces. Note that core memory should always

be placed as close to the processor as possible. The basic mounting box provides mounting space, power, and cooling for these additional (expansion) units.

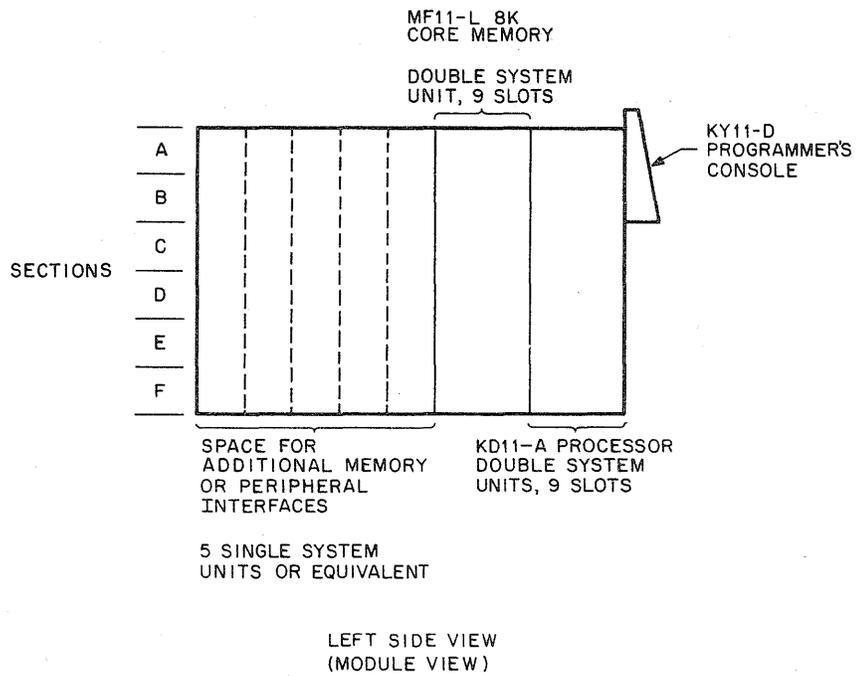
Module allocations for the processor, memory, and programmer's console are covered in paragraphs 6.2.1 through 6.2.3, respectively.

Whenever an expansion item is added to the basic box, certain factors must be considered such as the number of system units required by the device, power cable connections, Unibus connections, and jumpers. Power cable connections are covered in paragraph 6.5, Unibus interconnections are discussed in paragraph 6.3.2. When certain devices (such as the KT11-D, KJ11-A, etc.) are installed in the box, it is often necessary to cut jumpers both on the new device and on an existing device (such as the processor). Pertinent jumper information is included in the manual covering the device. However, information on the KT11-D, KE11-E, KE11-F, and KJ11-A processor options is also included in Chapter 2 of this manual.



11-1386

Figure 6-1 PDP-11/40 System Cabinet



11-1570

Figure 6-2 PDP-11/40 Mounting Box (BA11-FC)

6.2.1 Processor Module Allocations

Figure 6-3 shows the module allocation for the KD11-A double system unit for the basic KD11-A processor and processor options. The modules noted with an asterisk are the standard basic modules and must always be present. Other modules are optional with the specific option designation noted on the figure. The KT11-D Memory Management option requires the M7237 module in addition to the M7236 module. The KM11-A Maintenance Console option may be plugged into either slot F1 or E1 depending on whether the user is monitoring the basic KD11-A processor or one of three processor options (KT11-D, Memory Management, KE11-E, Extended Instruction Set, or KE11-F, Floating Instruction Set).

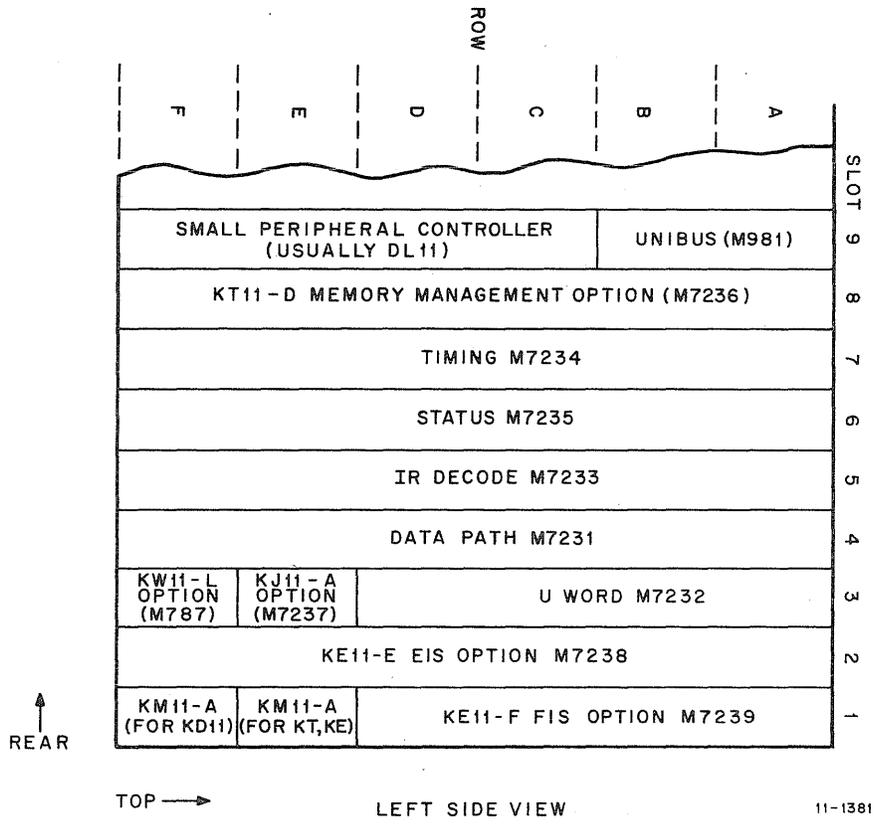


Figure 6-3 Module Allocation - KD11-A Processor, Basic (*) and Options



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6.2.2 Memory Module Allocations

Figure 6-4 shows the module allocation for the MF11-L double system unit. This memory unit is provided with a single 8K memory segment for the basic PDP-11/40; two additional 8K segments (MM11-Ls) can also be mounted within the same system unit. Additional MF11-L and MM11-L memories can be installed in the free system unit space within the BA11-FC mounting box (Figure 6-2).

6.2.3 Programmer's Console Mounting

The KY11-D Programmer's Console is mounted on the front of the BA11-FC mounting box as shown in Figure 6-1. Mounting is integral with the bezel and panel mounting. The console is cabled directly to the processor modules and provides both switch and display signals. Power to the console is applied through these same cables.

| SECTION | | | | | | SLOT |
|------------------------------|---|---|---|--------|---|------|
| F | E | D | C | B | A | |
| H214 MEMORY STACK | | | | UNIBUS | | 09 |
| G231 MEMORY DRIVER | | | | | | 08 |
| G110 CONTROL AND DATA LOOPS | | | | | | 07 |
| G110 CONTROL AND DATA LOOPS | | | | | | 06 |
| G231 MEMORY DRIVER | | | | | | 05 |
| H214 MEMORY STACK | | | | | | 04 |
| *G110 CONTROL AND DATA LOOPS | | | | | | 03 |
| *G231 MEMORY DRIVER | | | | | | 02 |
| *H214 MEMORY STACK | | | | UNIBUS | | 01 |

REAR ↑
 TOP →

11-1571

Figure 6-4 Module Allocation - MF11-L Memory, Basic (*) and Optional MM11-Ls



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6.3 CABINET AND SYSTEM MOUNTING

Because of the modularity of the PDP-11/40 System, a variety of peripherals may be added to the basic system. Depending on the type and number of peripherals selected, the remaining space in the basic system cabinet may be sufficient, or additional cabinets may have to be added to the system. The basic system cabinet is discussed in paragraph 6.3.1 and multiple-cabinet systems are discussed in paragraph 6.3.2.

6.3.1 System Cabinet

The cabinet housing the basic PDP-11/40 is divided into six levels. The bottom level (level six) is reserved for power supplies and cable entry. Levels four and five contain the BA11-FC mounting box which houses the basic system. Levels one through three provide space for mounting up to three peripherals, each having a front panel height of 10½ inches. If a high-speed paper-tape reader is added to the basic system, it always is installed directly above the BA11-FC mounting box. There are certain restrictions to mounting peripherals in cabinets. These are discussed in paragraph 6.3.2. As far as the basic system cabinet is concerned, it should be noted that any free-standing peripheral (system I/O device, card reader, etc.) can be no further from the cabinet than the maximum length of the interconnecting cable between the interface in the cabinet and the device itself.

6.3.2 System Configuration

In many cases, the number and types of peripherals added to a basic system necessitate additional mounting cabinets. The standard cabinet layout for PDP-11 systems starts at the right and evolves to the left. Another standard practice is to define the equipment in the processor cabinet first, then move to the next cabinet not defined for a specific device. It is always necessary to keep in mind the overall Unibus chain to keep Unibus length to a minimum. Cooling, cabling and logic interaction are all system considerations which must be accommodated.

Configuring multiple cabinet systems therefore requires, as a general rule, no full-depth device, or combination of devices, should be placed at the top position (level 1) or bottom position (level 6) of a cabinet. This restriction is necessary to ensure unrestricted cable entry at the bottom. Devices can be placed in the unused cabinet space of another device provided the installation does not interfere with the operation of that device. Disk cabinets are normally used only for mounting that specific disk system and its options.

In any cabinet, the top position (level 1) should be used only for rigidly fixed equipment. Levels 2 through 5 may be used for either rigidly fixed equipment or slide-mounted equipment. The level in any cabinet may be used for a peripheral device or for mounting an extension mounting box which is then used to house various device interfaces at the discretion of the user. Figure 6-5 illustrates typical mounting information for a multiple cabinet system.

The major logic interaction consideration in multiple cabinet systems is latency. Latency is defined as the longest time a device can be left unserviced before it loses data. Latency is usually a problem only in extremely large systems but should still be considered for optimum system performance. A recommended priority has been established to determine which peripherals should be mounted closer to the processor to compensate for timing characteristics of NPR devices and latency requirements for BR devices. These priorities are listed in Tables 6-1 and 6-2, respectively. The typical mounting information of Figure 6-5 accommodates these priorities. Additional information on system configuration is contained in PDP-11 Configuration Worksheet and the PDP-11/40 Site Preparation Worksheet.

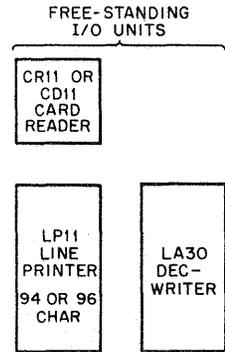
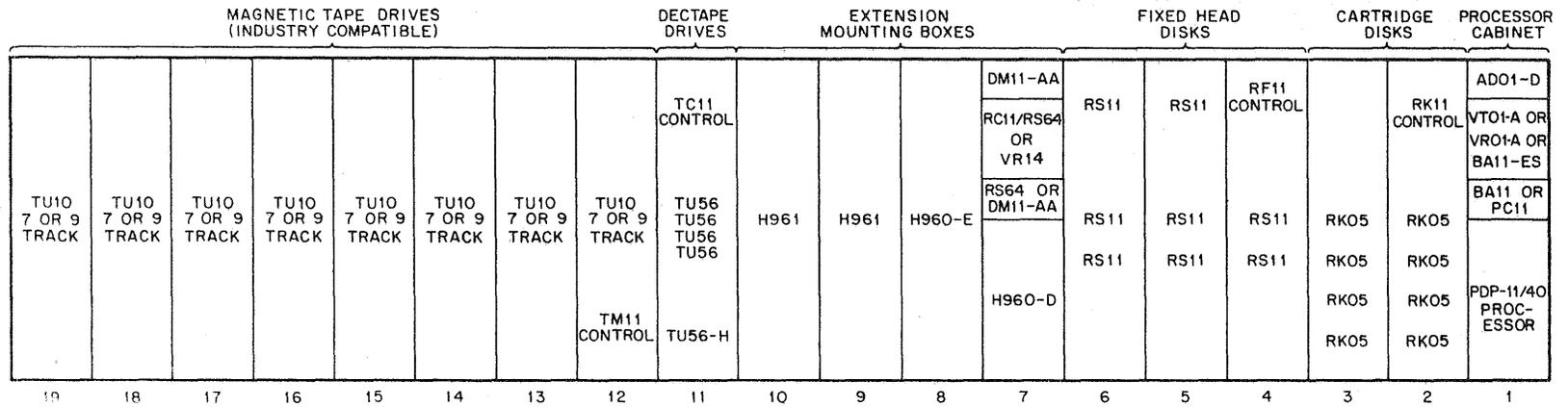


Figure 6-5 Typical Multiple Cabinet System Configuration

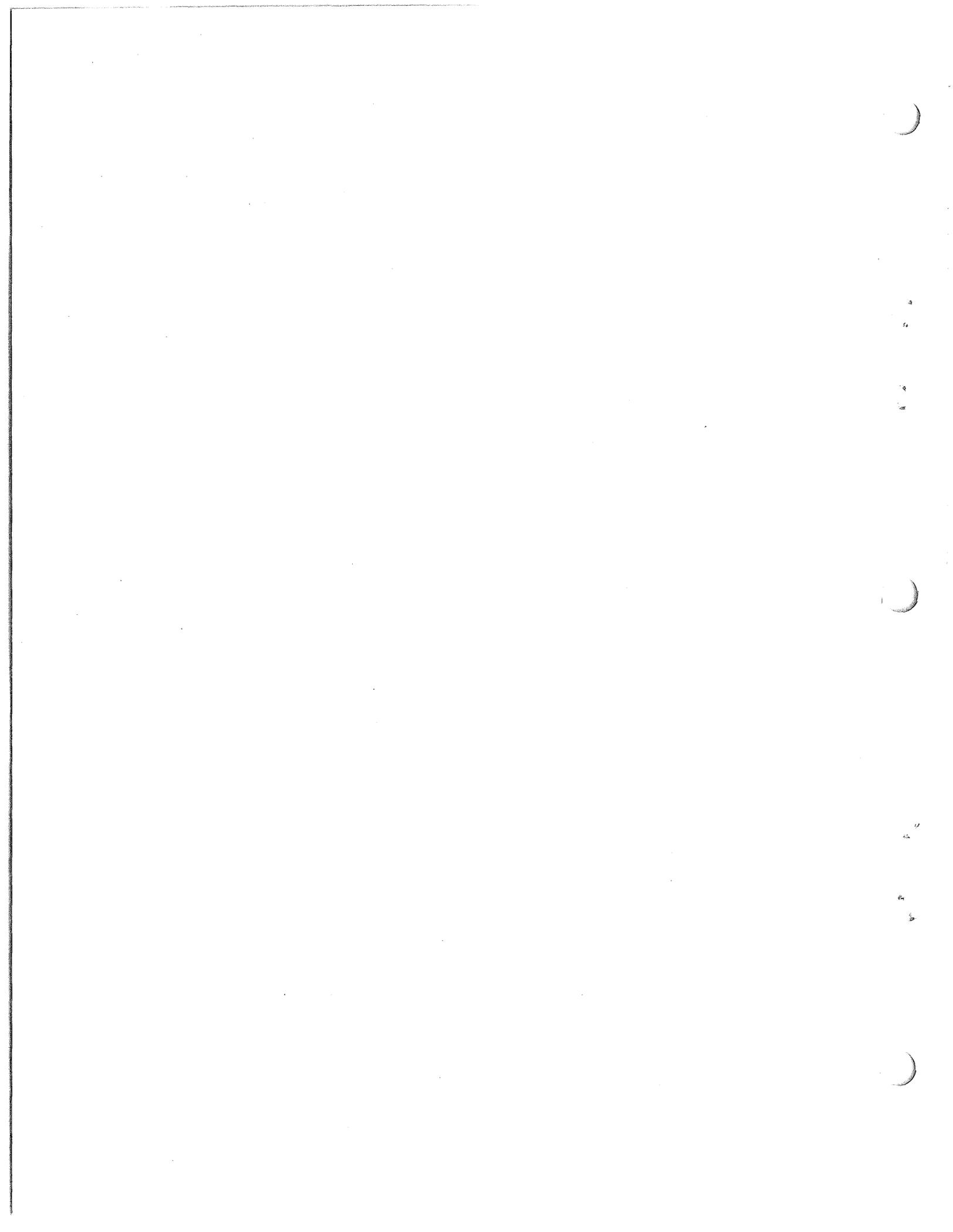


Table 6-1

Timing Characteristics of PDP-11 NPR Devices

| NPR Priority | Device | Worst Case Latency (usec) | Time Between Data Available (usec) |
|-----------------|-----------|------------------------------|---------------------------------------|
| 1 | RK11/RK03 | 8.5 | 11.1 |
| 2 | RP11 | 11 | *14.8 |
| 3 | RC11 | 12 | 16 |
| 4 | RF11 | 13 | 16 |
| 5 | RK11/RK02 | 19 | 22.2 |
| 6 | TM11 | 29 | 32 (at 800 bpi) |
| 7 | TC11 | 67 | 200 |
| 8 | DM11 | 100 | 119 (at 1200 baud) |
| 9 | CD11 | 800 | |
| 10 | DR11-B | Dependent on customer use | |

*The RP11 transfers two words each 14.8 microseconds

Table 6-2

Priority of Devices Affected by BR Latency

| Priority | BR7 | BR6 | BR5 | BR4 |
|----------|--------|--------|----------------------------|----------|
| 1 | *AD01 | KW11-L | DP11 @ 9600 baud or higher | KL11 |
| 2 | DT11-B | TC11 | DC11 @ 1800 baud | +UDC11 |
| 3 | | CR11 | DP11 @ 4800 baud | ** AFC11 |
| 4 | | CM11 | DC11 @ 1200 baud | |
| 5 | | KW11-P | DP11 @ 2400 baud | |
| 6 | | +UDC11 | DC11 @ 600 baud | |
| 7 | | | DP11 @ 2000 baud | |
| 8 | | | DC11 @ 300 baud | |
| 9 | | | DM11 | |
| 10 | | | **DR11-A | |
| 11 | | | DR11-B | |

*For AD01 sampling at high rates. Can be assigned to a lower level for slow input applications.

**Priority positions depend on customer application.

+ UDC immediate = BR6; UDC deferred = BR4.

6.4 POWER CONTROL SYSTEM

Both the basic and expanded versions of the PDP-11/40 include a power control system that controls ac power to system components, permits operation of the entire system from a single master switch, and shuts down the entire system in the event of fire in any cabinet. This power control system is functionally the same for all PDP-11 computers and consists of the following:

- a. cabinet-mounted power control unit
- b. a master power switch (OFF/POWER/PANEL switch on programmer's console of the PDP-11/40)
- c. cabinet-mounted thermal switch

A specific PDP-11/40 system may use either an 860 or 861 power control system. The 860 power control unit is described in paragraph 6.4.1 and the 861 power control unit is referenced in paragraph 6.4.2.

6.4.1 860 Power Control Unit

The 860 power control unit is operated from the console panel switch and is capable of switching up to 30A of 115 Vac (860A) or up to 15A of 230 Vac (860B). The power control unit distributes ac voltage to two output strips located within the cabinet. One strip provides switched (or controlled) ac power; that is, any component plugged into this strip is under control of the master switch. The second strip provides unswitched ac for operating devices that require continual application of power, such as magnetic disk drives. These strips permit all system devices to be connected within the cabinet, thereby necessitating only one power cord from the cabinet. In the basic PDP11/40 cabinet the right strip (as you face the cabinet from the front) is the switched or controlled ac power strip.

In multiple cabinet configurations, operation of the entire system can be controlled by the console OFF/POWER/PANEL switch provided there is at least one power control unit. However, any systems containing more than one processor require a master switch that is separate from the processor console switch.

The cabinet-mounted thermostat removes power from the switched ac power strip in the event of fire in any cabinet.

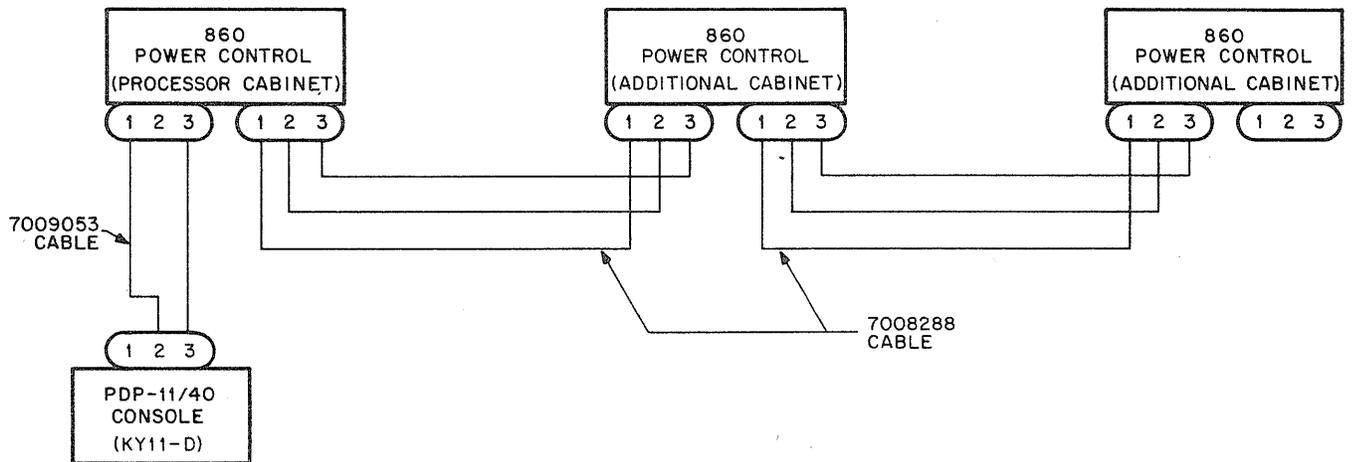
A power control bus cable is used to interconnect all devices in the system. Devices may be added to the system by connecting them to the bus in parallel at any convenient point. No terminators are required on

the bus and "T" connections may be used without any restrictions. The power control bus cable is a 3-wire cable joining two 3-wire male Mate-N-Lok connectors. Detailed instructions for interconnecting devices are given in paragraph 6.4.1.1.

6.4.1.1 860 Physical Description

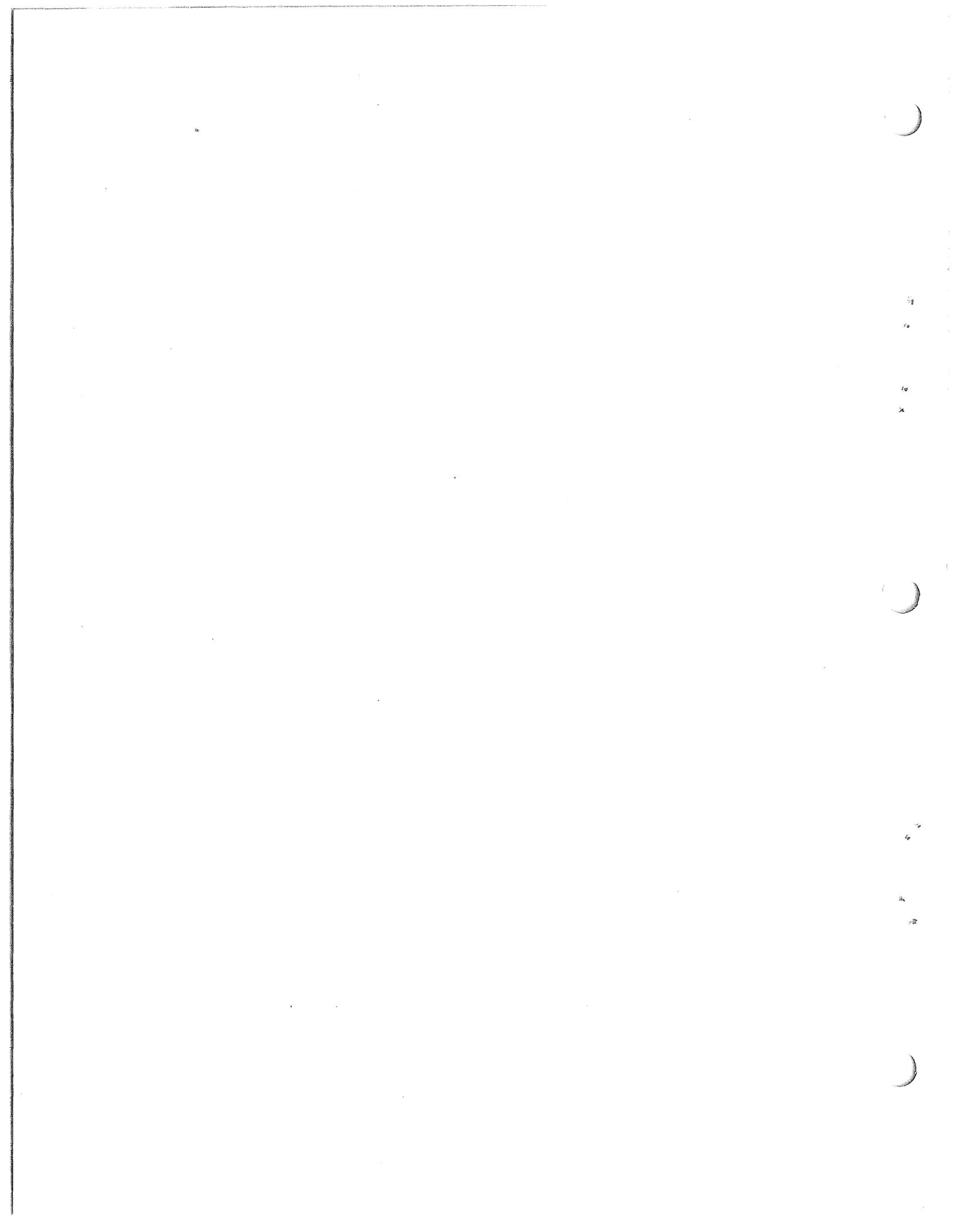
The 860 power control unit consists of an input circuit breaker, line filter, pilot light, relay, output filter, control board, and thermal detector. These components are housed in an enclosure which is mounted in the top of the system cabinet next to the cabinet air intake fan. The bottom of the enclosure contains three 3-pin Mate-N-Lok connectors, a REMOTE/OFF/LOCAL switch, and the detection element of the thermal switch.

The three connectors are wired in parallel to accept connection from the standard 3-wire control system. These connectors permit interconnection of power control units from one system cabinet to another. The REMOTE/OFF/LOCAL switch permits all system power to be controlled by one power control unit. When set to LOCAL, it allows the specific power control unit to be removed from the overall power system so that it can be run independently. In a system containing more than one power control, interconnecting cables would be installed between the connectors of adjacent power control units in a daisy chain manner to provide system power control (Figure 6-6). In this instance, the switch would be set to REMOTE to allow routing of power control from one cabinet to another.



11-1573

Figure 6-6 Power Control Interconnection



6.4.1.2 860 Functional Description

The 860 power control unit has two main functions: to route ac power from its line cord to an unswitched ac power strip and to switch the incoming ac on another power strip when the console switch is closed to turn on the system. The PDP-11/40 system may use either an 860A or 860B power control unit. The differences between these two models are listed in Table 6-3.

The power control operates on a 3-wire parallel control. The three lines are:

- a. Line 1 - power on
- b. Line 2 - emergency off
- c. Line 3 - ground

If neither Line 1 or Line 2 is connected to Line 3, the system is in a power off state.

When lines 1 and 3 are connected through the console switch, operation of the switch causes activation of the power relay within the 860 power control and provides input power to the switched or controlled ac power strip. Connecting Lines 2 and 3 causes an override of any other state of the power control and removes the switched ac power by opening the 860 power control internal relay.

Line 2 is utilized by the thermal detector to provide protection in case of fire or excessive heat.

Table 6-3

Model Differences

| Item | Model 860A | Model 860B |
|------------------------|--|--|
| Input line voltage | 115 Vac | 230 Vac |
| Circuit breaker CB1 | 30A | 15A |
| Transformer T1 primary | 115 Vac | 230 Vac |
| Input power line cord | 115 Vac 30A 25 feet P/N 1203485 | 230 Vac 15A 25 feet P/N 1204687 |

6.4.1.3 860 Circuit Description

The basic 860 power control circuit is shown in Figure 6-7. A pilot light on the line side of the circuit breaker lights when the ac line cord is plugged into the wall and power is applied to the unit. The voltage from the secondary of transformer T1 is half-wave rectified to provide +24V which is used to provide B+ to control transistors Q1 and Q2, and to energize relay K1. The transformer secondary is fused. In the event the system is connected properly and ac power is applied to the power control but no output is present on the switched ac strip, this fuse should be checked. Note that power is available on the unswitched ac power strip in this case because it is tapped off the line and does not pass through relay K1.

When the power control is used as a switched power control, the REMOTE/OFF/LOCAL switch S1 is set to REMOTE. When the console OFF/POWER/PANEL switch is set to POWER, it completes a ground circuit that causes Q1 to cut off. When Q1 cuts off, Q2 conducts and causes relay K1 to energize, which closes the switched ac output circuit. Other connectors are provided to allow remote power control switches to perform the same function as the console switch (close the circuit between pins 1 and 3). A remote power switch would be used, for example, in systems containing more than one processor.

Thermal switch S2 provides protection against fire or excessive heat. It is normally open but closes if the cabinet ambient temperature exceeds 130°F (54°C). When it closes, Q2 cuts off, relay K1 deenergizes,

and the switch connects Line 2 (emergency off) to ground, thereby switching off the ac output. Pin 2 on connectors J1, J2, and J3 permits additional thermal switches (in the cabinet and extension mounting box) to be connected in parallel with thermal switch S2 to perform the same function. The switch opens to restore power once the temperature falls below 85° F.

When the power control is used as an unswitched power control, REMOTE/OFF/LOCAL switch S1 is always set to LOCAL. Thus, Q1 is always cut off, Q2 always conducts, and K1 remains energized. Relay K1 is deenergized, thereby removing power from the switched ac power strip, only if there is an input power failure or if an overtemperature condition occurs.

6.4.2 861 Power Control Unit

A specific PDP-11/40 system may use an 861 power control unit rather than an 860. The 861 power control is a later version and is available in three different models:

- a. 861A - 115 Vac, 50/60 Hz, 2-phase
- b. 861B - 230 Vac, 50/60 Hz, single phase
- c. 861C - 115 Vac, 50/60 Hz, single phase

A detailed description of the 861 power control unit is given in the Type 861-A, 861-B, 861-C Power Controller Maintenance Manual.

6.5 PDP11/40 Basic Power Supply

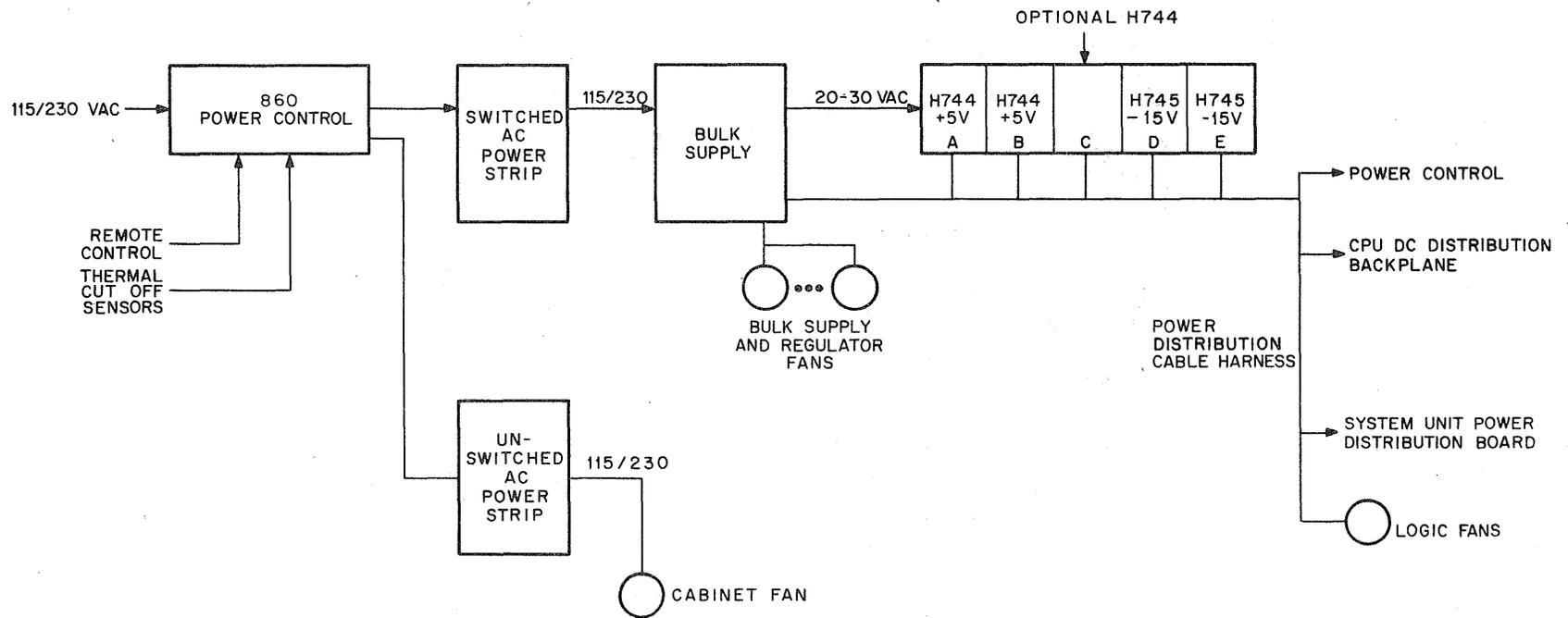
The basic PDP11/40 power system consists of the power control unit, the ac power distribution strips, power distribution for the cabinet and basic box fans, and a modular power supply for regulated dc voltages.

A block diagram of the basic power system is shown in Figure 6.8. The power control unit (860 or 861) and the ac power strips have already been discussed. The distribution for cabinet fan power is the unswitch ac power strip with the basic box fans receiving power through the H742 bulk power supply. The PDP11/40 Modular Power Supply (Figure 6.9) consists of this H742 bulk power supply, two H744 +5V regulators and two H745 -15V regulators. These elements of the modular power supply are discussed in detail in paragraphs 6.5.1 through 6.5.3, respectively.

Please note that these details are for theory of operation and off-line repair. Maintenance should consist of replacement per paragraph 6.5.5.

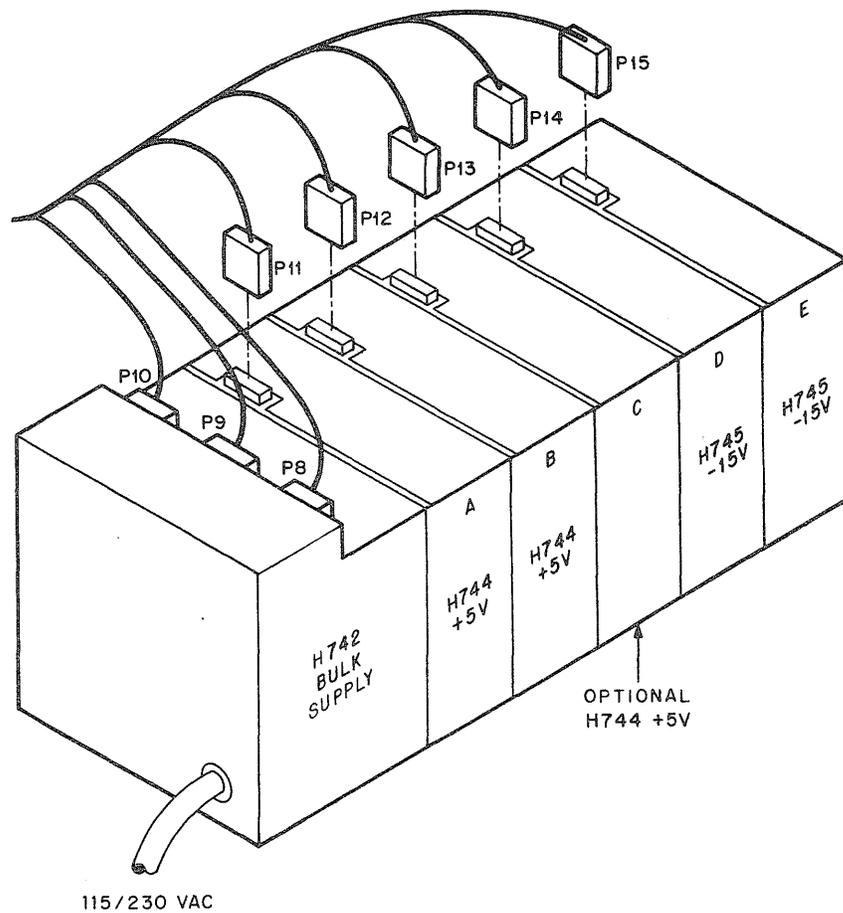
DC power distribution and cabling are covered in paragraph 6.5.4 with information on expansion provided. Power supply maintenance is covered in paragraph 6.5.5.

6-22A



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Figure 6-8 PDP-11/40 Power System Block Diagram



11-1384

Figure 6-9 PDP-11/40 Power Supply

6.5.1 H742 Bulk Power Supply

The H742 power supply is functionally divided into two major parts:

- a. Bulk Power Supply (drawing D-CS-H742-0-1) - used to provide the various ac input voltages required by the fans, regulators, and power control board.
- b. Power Control Board (drawing C-CS-5409730-0-1) - used to provide +15 and +8 voltages, line clock, and AC LO and DC LO signals for system use.

The PDP-11/40 power system operates with 115 Vac or 230 Vac primary source power inputs. Although different 860 (or 861) power control units are provided for each input voltage, the same H742 power supply can be used with both versions. Jumpers are connected to terminal strip TB1, which is the primary of power supply transformer T1, so that it can operate with the selected input voltage.

If 115 Vac operation is required, jumpers are placed between pins 1 and 2, and between pins 3 and 4 of TB1. If 230 Vac operation is required, a jumper is connected between pins 2 and 3.

Line power is applied through TB1 to the primary of transformer T1. The transformer secondaries provide 20-30 Vac input power for the regulators and power control board as well as 15-24 Vac power for the power control board. Power to cooling fans is tapped directly from TB1 and does not come from the transformer.

The power control board portion of the power supply (drawing C-CS-5409730-0-1) provides +15 and +8 Vdc outputs, a clock output used to drive the KW11-L Line Frequency Clock option, and the AC LO and DC LO control signals used for power fail sequences. These outputs are discussed in paragraphs 6.5.1.1 through 6.5.1.3.

6.5.1.1 +15V and +8V of the H742 Supply

The power control board of the H742 supply contains a +15V/+8V dc supply and is described on print C-CS-5409730-0-1. This dc supply receives 15-24 Vac from the secondary of transformer T1. This ac input is full-wave rectified by diode bridge D1. The resultant dc is applied to Darlington power amplifier Q1, through fuse F1. The bias on Q1 is controlled to provide +15 Vdc at output pins 2 and 3 with respect to output pins 4, 5, and 6 (ground). If the Q1 collector voltage starts to increase, the bias at the base of Q2 increases, and Q2 conducts slightly more current to maintain a constant output voltage. Zener diode D7 provides approximately +8 Vdc at output pin 1. When DC LO is grounded at output pin 9, Q2 conducts hard to cut off Q1 completely; thus removing both the +15V and +8V outputs.

6.5.1.2 Clock Output of the H742 Supply

The CLOCK output is derived off one leg of full-wave rectifier bridge D1 by voltage divider R10 and R11, and Zener diode D2. The CLOCK output is a 0 to 5V square wave at the line frequency of the input power source (47 to 63 Hz). The CLOCK output is used to drive the KW11-L Line Frequency Clock option, which mounts in slot F3 of the processor backplane or the KW11-P option, which can be mounted in the Small Peripheral Controller slot. Operation of the KW11-L option is described in the KD11-A Processor Manual; operation of the KW11-P is described in its manual.

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6.5.1.3 AC LO and DC LO Circuits

The AC LO and DC LO control signals are used to warn the processor that a power failure is imminent so that the processor has time to perform a power-fail sequence. If there is an ac power failure (line power or bulk supply failure), AC LO is asserted on the bus followed by DC LO. Sufficient time exists between these signals to allow storage of volatile data and the conditioning of peripherals.

The 20-30 Vac input from the secondary of transformer T1 is applied to the AC LO and DC LO sensing circuits on the power control board. The ac input is rectified and filtered by diodes D8 through D11, and capacitor C3. A common reference voltage is derived by resistor R18 and zener diode D12. Both sensing circuits operate in a similar manner. Each contains a differential amplifier, a transistor switch, and associated circuits. The major difference is that the base of Q6 in the AC LO circuit differential amplifier is at a slightly lower value than that of Q9 in the DC LO differential amplifier. The operation of both sensing circuits depends upon the voltage across capacitor C3.

When AC LO is being sensed, the 20-30 Vac input is rectified and stored in capacitor C3 which charges and discharges at a known rate whenever the ac power is switched on or off. Thus, the voltage that is applied to the emitters of differential amplifier Q6/Q7 through R17 is a rising or falling waveform of known value. For example, when power fails, or is shut down, the dc voltage decays

at a known rate as determined by the RC time constant. If the voltage decreases to approximately 20V, the base of Q6 becomes negative with respect to the base of Q7. The increased forward bias on Q6 causes it to conduct more and the resultant decrease in Q7 causes it to cut off. This removal of voltage across R16 causes Q5 and Q4 to conduct, grounding the AC LO line at pin 8. The AC LO signal is applied through the cable harness and processor backplane to the processor power fail initialize logic so that the power fail sequence can be started.

The DC LO sensing circuit operates in a similar manner to the AC LO sensing circuit. The prime difference between these two circuits is the voltage level at which they "trip." For example, if the ac input starts to decrease, as a result of a power failure or shutdown, the AC LO lines are grounded before the DC LO lines. As power is restored, the ground is removed from the DC LO lines before it is removed from the AC LO lines. The DC LO signal is also applied to the power fail initialize logic.

A description of how the AC LO and DC LO control signals are used in the KD11-A processor is provided in the KD11-A Processor Manual.

6.5.2 H744 +5V Regulator

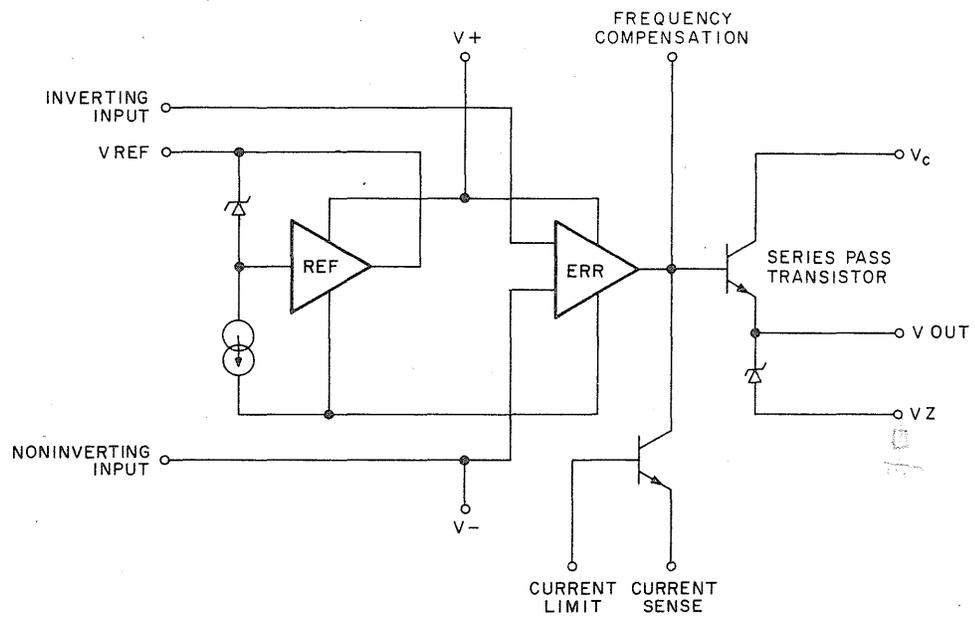
Two H744 +5V regulators are used in the basic PDP-11/40 Power System. The H744 circuit schematic is shown in drawing D-CS-H744-0-1. The following paragraphs describe the regulator circuit, overcurrent sensing circuit, and overvoltage crowbar circuit.

6.5.2.1 H744 Regulator Circuit

The 20-30 Vac input is a full wave which is rectified by bridge D1 to provide a dc voltage (24 to 40V, depending on line voltage) across filter capacitor C1 and bleeder resistor R1. Operation centers on precision voltage regulator E1 which is configured as a positive switching regulator. A simplified schematic of E1 is shown in Figure 6-10. Regulator E1 is a monolithic integrated circuit that is used as a precision voltage regulator. It consists of a temperature-compensated reference amplifier, error amplifier, series-pass power transistor, and the output circuit required to drive the external transistors. In addition to E1, the regulator circuit includes pass transistor Q2, pre-drivers Q3 and Q4, and level shifter Q5. Zener diode D2 is used with Q5 and R2 to provide +15V for E1. Q5 is used as a "level shifter"; most of the input voltage is absorbed across the collector-emitter of Q5. This is necessary since the raw input voltage is well above that required for E1 operation. This +15V input is supplied while still retaining the ability to switch pass transistor Q2 on or off by drawing current down through the emitter of Q5.

The output circuit is standard for most switching regulators and consists of "free-wheeling" diode D5, choke coil L1, and output capacitors C8 and C9. These components make up the regulator output filter. Free wheeling diode D5 is used to clamp the emitter of Q2 to ground when Q2 shuts off, thus providing a discharge path for L1.

In operation, Q2 is turned on and off generating a square wave of



11-1391

Figure 6-10 Simplified Diagram of Precision Voltage Regulator E1



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voltage which is applied across D5 at the input of the LC filter (L1, C8 and C9). This type circuit is basically only an averaging device, and the square wave of voltage appears as an average voltage at the output terminal. By varying the period of conduction of Q2, the output (average) voltage may be varied or controlled, thus supplying regulation. The output voltage is sensed and fed back to E1 where it is compared with a fixed reference voltage. E1 turns pass transistor Q2 on and off according to whether the output voltage level decreases or increases. Defined upper and lower limits for the output are approximately +5.05V and +4.95V.

During one full cycle of operation the regulator operates as follows: Q2 is turned on and a high voltage (approximately +30V) is applied across L1. If the output is already at a +5V level, then a constant +25V would be present across L1. This constant dc voltage causes a linear ramp of current to build up through L1. At the same time, output capacitors C8 and C9 absorb this changing current and voltage, causing the output level (+5V at this point) to increase. When the output, which is monitored by E1 reaches approximately +5.05V, E1 shuts off turning Q2 off, and the emitter of Q2 is clamped to ground. L1 discharges into capacitors C8, C9, and the load. Pre-drivers Q3 and Q4 are used to increase the effective gain of Q2 to ensure that Q2 can be turned on and off in a relatively short period of time.

Conversely, once Q2 is turned off and the output voltage begins to decrease, a predetermined value of approximately +4.95V will be reached causing E1 to turn on which in turn causes Q2 to conduct,

beginning another cycle of operation.

Thus, a ripple voltage is superimposed on the output and is detected as predetermined maximum (+5.05V) and minimum (+4.95V) values by E1. When +5.05V is reached, E1 turns Q2 off and when +4.95V is reached, E1 turns Q2 on. This type of circuit action is also referred to as a "ripple regulator."

6.5.2.2 +5V Overcurrent Sensing Circuit of the H744

The overcurrent sensing circuit consists of: Q1, R3 through R6, R25, R26, Q7, and C4. Transistor Q1 is normally not conducting; however, if the output exceeds 30A, the forward voltage across R4 is sufficient to turn Q1 on, causing C4 to begin charging. When C4 reaches a value equal to the voltage on the anode gate of Q7, Q7 turns on and E1 is biased off, turning the pass transistor off. Thus, the output voltage is decreased as required to ensure that the output current is maintained below 35A (approximately) and the regulator is "short circuit" protected. The regulator continues to oscillate in this new mode until the overload condition is removed.

6.5.2.3 +5V Overvoltage Crowbar Circuit of the H744

The overvoltage crowbar circuit consists of the following components: Zener diode D1, silicon-controlled rectifier (SCR) D7, D8, R22, R23, C7, and Q6.

Under normal conditions, the trigger input to the SCR (D7) is at ground because the voltage across Zener diode D3 is too small to cause it to conduct. As the +5V line approaches 6V, Zener diode D3 conducts and the voltage drop across resistor R23 draws gate current and triggers the SCR. The SCR shorts the +5V line to ground through resistor R21, which is a current-limiting resistor. The SCR remains on until the capacitors discharge.

6.5.3 H745 -15V Regulator

Two H745 -15V regulators are included in the PDP-11/40 Power System. Operation of the H745 is basically the same as that of the +5V regulator. The H745 schematic is shown in drawing C-CS-H745-0-1. Input power (20 to 30 Vac) is taken from the secondary of transformer T1 and applied to the full-wave bridge rectifier (D1). The output of D1 is a variable 24 to 40 Vdc and is applied across capacitor C1 and resistor R1. The following paragraphs discuss the regulator circuit, overcurrent sensing circuit, and the overvoltage crowbar circuit.

6.5.3.1 -15V Regulator Circuit of the H745

Regulator operation is almost identical to that of the +5V regulator; however, the +15V input that is required for operation of E1 is derived externally and is applied across capacitor C2 to E1 and the inverting and non-inverting inputs to E1 are reversed. In addition, the polarities of the various components are reversed. For example, Q5, which is used as a level shifter, is an NPN transistor on the +5V regulator but a PNP is required on the -15V regulator to allow the regulator to operate below ground (at -15V).

Under normal operating conditions, regulator operation centers around linear regulator E1 and pass transistor Q2, which is controlled by E1. Predetermined output voltage limits are -14.85V (minimum) and -15.15V (maximum). When the output reaches -15.15V, E1 shuts off, turning Q2 off, and L1 discharges into C8 and C9. When the output reaches -14.85V, E1 conducts, causing Q2 to turn on, increasing the output voltage.

6.5.3.2 -15V Overcurrent Sensing Circuit of the H745

The -15V regulator overcurrent sensing circuit is basically made up of the same components as the +5V regulator except Q1 is an NPN transistor in the -15V regulator. Transistor Q1 is normally not conducting; however, once the output exceeds 15A, Q1 turns on and C3 charges. When C3 reaches the same value as the anode gate of Q7, E1 is biased off, which turns Q2 off, thereby stopping current flow and turning the -15V regulator off. Thus, the regulator is short-circuit protected.

6.5.3.3 -15V Overvoltage Crowbar Circuit of the H745

When SCR D5 is fired, the -15V output is pulled up to ground and latched at ground until input power, or the +15V input is removed. A negative slope on the +15V line can be used to trip the crowbar for power-down sequencing, if desired.

6.5.4 DC Power Distribution

Distribution of dc power from the basic PDP11/40 power supply is shown on the cabling diagram (Sheet 3) of the BASIC ASS'Y (11/40) print (D-VA-11/40-0-0). Distribution is effected by cabling from the various H744 and H745 regulator to a power distribution panel with further cabling to the individual system units. The cable (E-IA-70008754-00) from the regulators to the power distribution panel is defined in the prints: POWER HARNESS (11/40), D-IC-IV40-0-2 and HARNESS, POWER (WIRE LIST), K-WL-7008784-0-1. The cables from the power distribution panel to the system units are diverse, and relate to the power interconnection technique on the system units. Detailed information is provided for the connections to the KD11-A backpanel and for the MF11-L backpanel, both basic to the PDP11/40. The cable types are noted on Sheet 3 of the BASIC ASS'Y (11/40), print D-VA-11/40-0-0 with details on connection on Sheet 4 and in the respective cable drawings. Connection to DD11 type system units requiring the G772 module connection is provided by the D-IA-7009177-0-0 cable.

The distribution of dc power from the regulators to the power distribution panel results in certain regulators driving certain connectors. Limitations, therefore, exist on the amount of power on a connector and the number of connectors available. Figure 6-11 is a representation of the distribution panel with usage (KD11-A, MF11-L) and source (H744's and H745's per slot assignment in the H742 bulk power supply).

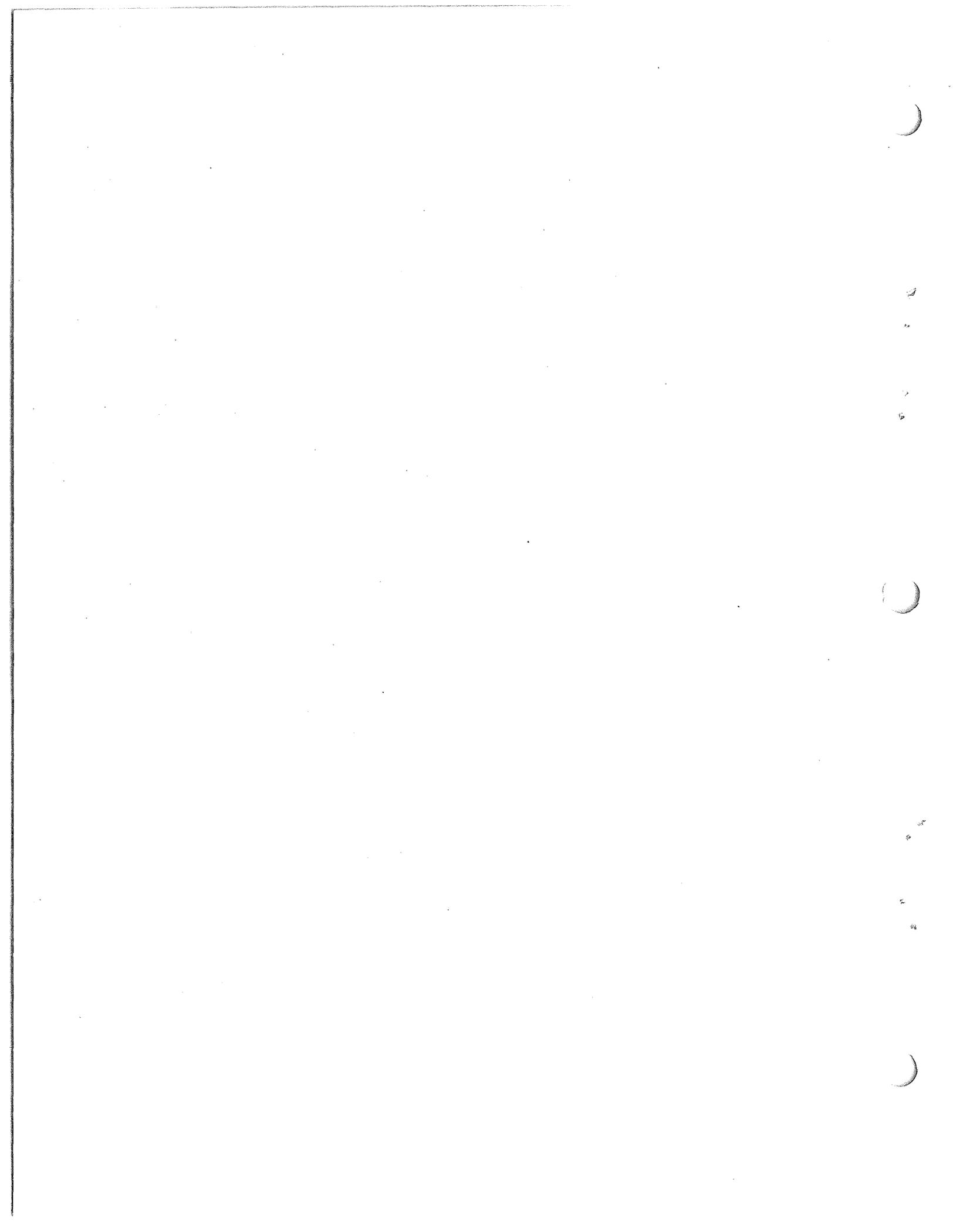
Power is supplied to three groups of connectors on J1, J2 and J3, J4 and J5, J6, respectively. Each of these input connectors have output connectors: J1, J2 have 1, 2 and 3; J3, J4 have 4, 5 and 6; and J5, J6 have 7, 8 and 9.

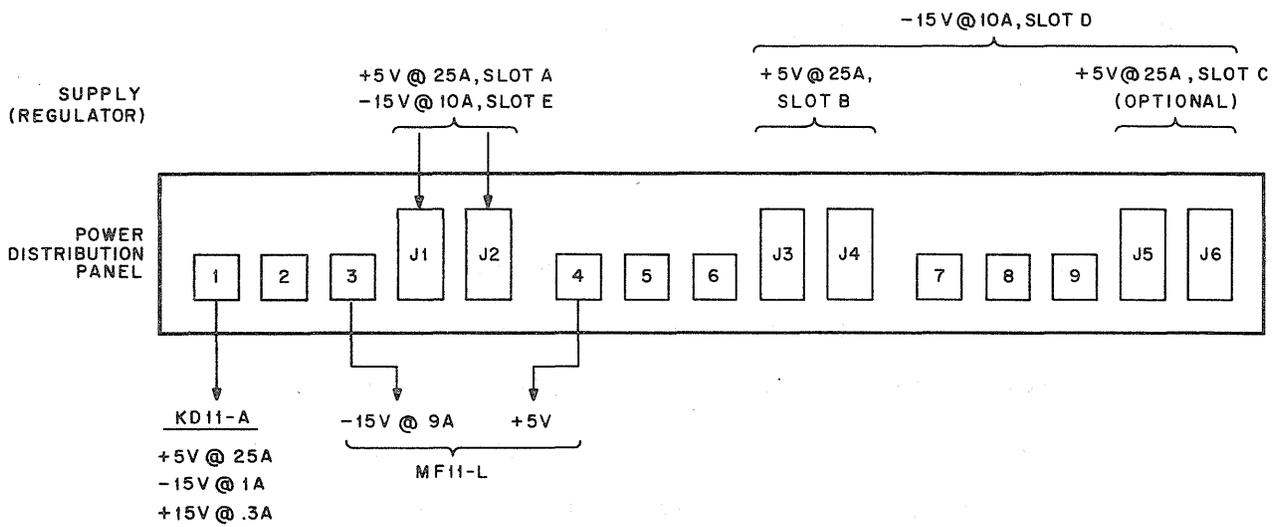
Connectors J1, J2 receive power from the +5V regulator of SLOT A and the -15V regulator of SLOT E. All of this power is committed to the KD11-A processor and the MF11-6 memory. Note that this happens with only two of the three distribution connectors being used, 1 and 3. The cable from 3 is a joint cable, this portion from 3 supplying the MF11-6 with -15V power.

Connectors J3, J4 receive power from the +5V regulator of SLOT B and the -15V regulator of SLOT D. Note that only two distribution connectors, 5 and 6, are available for expansion use; connector 4 is already used to provide +5V power (A) to the basic MF11-6. The +5V power left for connectors 5 and 6 is reduced by that amount; the -15V power must be shared with any further expansion logic from connector 7, 8 or 9.

Connectors J5, J6 receive power from the optional +5V regulator of SLOT C and the already mentioned -15V regulator of SLOT D. Three distribution connectors 7, 8 and 9 are available but care must be used to avoid overloading the -15V regulator also used for the J3, J4 connectors. Note that expansion beyond two additional single system units require the optional +5V regulator of SLOT C due to distribution connection limitation. The first two system units use up connectors

5 and 6, additional units require connector (and therefore power) from the J5, J6 connector group. The optional +5 regulator of SLOT C is provided with logics originally ordered with the PDP11/40; it must be separately ordered for add on situations.





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Figure 6-11

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6.5.5 Maintenance of Power System

For the most part, maintenance of the power system at the field level consists of replacing defective modules, such as the regulators. The details on regulator operation presented in paragraphs 6.5.1 through 6.5.3 are for theory of operation and off-line repair of failed units (see paragraph 7.5). With Maintenance consisting of module replacement, the major maintenance effort consists of failure isolation. Table 6-4 lists a procedure that can be followed as a guideline to assist in locating defective components.

CAUTION

Because there are two +5V and two -15V regulators in the PDP-11/40 System, a common troubleshooting technique would be to swap an operating regulator with a faulty regulator. If this is done, first check regulator input voltages to prevent damage to the second regulator in the event the fault lies in the power supply.

Table 6-4

Power System Troubleshooting Guide

| Step | Test | Procedure | Results |
|------|--|--|--|
| 1 | Verify that proper ac voltage input to power supply is present. | 115V system - measure between pin 1 or 2 and pin 3 or 4 of TB1 on H742 power supply. | Correct - proceed to Step 2. Incorrect - indicates failure may be in 860 power control or input line. Proceed to Step 5. |
| | | 230V system - measure between pin 2 and 3 of TB1. | |
| 2 | Verify that H742 bulk power supply is providing the proper ac outputs. | 20-30 volts should be present on the following pins: J1 - pins 1,2 J2 - pins 1,2 pins 8,9 pins 11,12 | Correct - proceed to step 3. Incorrect - indicate failure of H742 transformer. If all voltages are correct except one, problem could be either transformer secondary or a wiring malfunction. |

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Table 6-4 (Cont)

Power System Troubleshooting Guide

| Step | Test | Procedure | Results |
|------|---|--|---|
| | | J3 - pins 1,2 pins 3,4 pins 5,6 pins 7,8 | |
| | | 15-24 volts should be present between pins 3 and 4 of J1. | |
| 3 | Verify that the proper input voltage is present at the regulator. | +5V Regulator - check for 20-30 Vac at pins 6 and 7 of J1. -15V Regulator - check for 20-30 Vac at pins 6 and 8 of J1. Check for +15V at pins 4,5 of J1. | Correct - proceed to step 4. Incorrect - indicates failure is probably in the wiring between the H742 and the regulator. If the +15V for the -15V regulator is not present, the trouble may be in the H742 power control board. |

Table 6-4 (Cont)
Power System Troubleshooting Guide

| Step | Test | Procedure | Results |
|------|---|--|---|
| 4 | Verify that the proper output voltage is being produced by the regulator. | <p>+5V Regulator - measure between pin 2,5 (+5) and 3,4 (GND) of J1. Output must be between +5.05V and +4.95V.</p> <p>-15V Regulator - measure between pin 1 (-15V) and pin 2,3 (GND) of J1. Output must be between -15.15V and -14.85V.</p> | <p>Correct - check remaining regulators. If all regulators are within tolerance, the power system is not malfunctioning and the problem exists elsewhere.</p> <p>Incorrect - If the +5V regulator is not functioning replace. If the -15V regulator is not functioning check fuse F1 in the regulator. If this does not correct the problem, replace the regulator.</p> |

Table 6-4 (Cont)
Power System Troubleshooting Guide

| Step | Test | Procedure | Results |
|------|---|--|---|
| 5 | If previous tests indicate that proper input voltage is not being supplied to bulk supply, perform the tests listed in this step. | <ul style="list-style-type: none"> <li data-bbox="842 433 1352 654">a. Verify that proper ac voltage is supplied to input terminals of 860 (or 861) power control. <li data-bbox="842 743 1283 841">b. Verify that circuit breaker CB1 is ON. <li data-bbox="842 938 1335 1159">c. Verify that REMOTE/OFF/LOCAL switch S1 is set to either LOCAL or REMOTE. <li data-bbox="842 1256 1289 1346">d. Verify that thermal switch S2 is closed. | <p data-bbox="1373 436 1793 594">If not, check input line cord and line power receptacle.</p> <p data-bbox="1373 748 1793 911">If none of these tests correct the problem, proceed to step 6.</p> |

Table 6-4 (Cont)
Power System Troubleshooting Guide

| Step | Test | Procedure | Results |
|------|--|---|--|
| 6 | Verify that the power control board is functioning properly. | Verify that the power control board is producing the proper outputs. Refer to drawings C-CS-860-0-1 and C-CS-5409770-0-1. | If the board is producing the proper outputs, the problem could be a malfunction of power control relay K1. If the board is not producing correct outputs, replace the board. |



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7 GENERAL MAINTENANCE

7.1 SCOPE

This chapter provides general maintenance information for the PDP-11/40 System and includes: preventive maintenance of mechanical assemblies, system power checks, and power supply maintenance.

Maintenance information related to the processor and memory components of the basic PDP-11/40 System is presented in the associated maintenance manuals. Maintenance of Unibus peripherals requires not only the associated maintenance manual, but also an understanding of Unibus operation.

In addition to the maintenance information contained in the processor, memory, and peripherals manuals of the PDP-11/40, significant maintenance information is available in the diagnostic programs documentation. The diagnostic programs are a major tool for detecting and isolating machine faults and Preventive maintenance should include their regular use.

7.2 OVERALL MAINTENANCE TECHNIQUES

Maintenance of the PDP-11/40 System requires:

knowledge of proper hardware operation,
ability to detect and isolate an error condition, and
means to repair the error condition.

This is true for all but the preventive maintenance procedures for mechanical assemblies and for the relatively simple power check-out procedures. This section outlines techniques for performing maintenance on the PDP-11/40. Note, however, that the essential starting point is to have knowledgeable and able service personnel.

7.2.1 Knowledge of Proper Hardware Operation

Training courses and machine documentation provide information on hardware operation and is available at the programming, systems, and individual device levels.

The training courses available for the PDP-11/40 System include:

PDP-11/40 Hardware Familiarization (10 days)

PDP-11/40 Options Maintenance (5 days)

Interfacing the PDP-11 (5 days)

Other courses are available on Paper Tape Software, Disk Operating System Software, and Resource Timesharing System Software. Information on these and other PDP-11 courses is available from either the Digital Account Representative or from the Digital Education Centers.

Documentation pertinent to the PDP-11/40 System includes documents produced specifically for the PDP-11/40, and common PDP-11 documents on programming and Unibus interfacing. All of the relevant documents are listed in Table 1-2 of this manual.

A special effort has been expended in production of documents relating to the PDP-11/40 processor (KD11-A) and processor options (KE11-E, KE11-F, and KT11-D). Innovations include: print set formats, tables and notes on the prints, and wire list print notations. These are provided to facilitate initial learning but,

more importantly, to provide instant reminders of specific details during maintenance. Information describing the print sets appears in the processor and options maintenance manuals.

7.2.2 Detection and Isolation of Error Condition

Malfunctioning hardware is normally indicated by either software failure or by peripheral malfunctions. This can occur with customer's system software or with the periodic operation of various MainDEC diagnostic programs. If the failure occurs with system software, verification by MainDEC programs is suggested.

Isolation of the specific failure is the most difficult aspect of maintenance repair and the reason for trained service personnel. Operation of MainDEC diagnostic programs can isolate the failure to a specific device or operation but knowledge of program operation and documentation is necessary. The modular nature of the Unibus, with its separate peripherals, may also help isolate failures, but knowledge of Unibus specifications and peripheral operation is essential. Often, however, error detection is reduced to knowledge of proper machine operation with detection of discrepancies. Detailed manuals on device operation with clear, annotated prints, provide information on operation. Detection of discrepancies requires experience and expertise.

The level of fault isolation is important. In the power supply, regulator units such as the H744 or H745 are replaced if their

output voltages are in error; the circuit board of the H742 unit is replaced if the AC LO or DC LO control signals are in error. Repair procedures for the replaced units are given in paragraph 7.5.2. Replacement of KD11-A processor modules is suggested for situations requiring minimum down time. Experienced service personnel, however, may find integrated circuit (IC) replacement a practical alternative to the cost or transportation of modules.

7.2.3 Means of Repairing the Error Condition

The method of repairing an error condition is directly related to the level of fault isolation mentioned in the previous paragraph. If, for example, fault isolation and repair is to be at the IC level, then the parts identified in the machine documentation must be available. Suitable repair and rework techniques must be followed to avoid equipment damage. If module or sub assembly level of fault isolation and repair is to be used, these units must be available. Spare part kits are available for the PDP-11/40 (SP11-KP for processor and SP11-PD for the power supply) and the various Unibus devices. Repair is normally at this level when down time is critical or when a large number of machines is involved.

Verification of repair at any level is made by running the appropriate MainDEC diagnostic programs.

7.2.4 Digital Field Service

The present state-of-the-art in complex computer systems requires qualified service personnel. Installation and 90-day warranty service are provided by such personnel from Digital Field Service. These people are trained both in basic PDP-11/40 components (processor, console, and memory) and in the peripherals that may be placed on the Unibus. Material support exists both at the IC level (directly equivalent parts) and at the module and subassembly level.

Digital Field Service support may be continued beyond the warranty period with a Digital Service Agreement. Total equipment maintenance programs are available. Details of this service may be obtained from the Digital Account Representative at the local Field Service Office.

7.3 MAINTENANCE EQUIPMENT REQUIRED

Maintenance procedures for the PDP-11/40 require the standard equipment (or equivalent) listed in Table 7-1. Especially important in analyzing operation of the processor, or processor options, is the KM11 option consisting of W130 and W131 modules and associated overlays. Use of the KM11 maintenance displays and switches is covered in the processor and processor options maintenance manuals. The module extender board (W900) is also an important diagnostic tool and is discussed in paragraph 7.4.

Table 7-1

Maintenance Equipment Required

| Equipment or Tool | Manufacturer | Model, Type, or Part No. | DEC Part No. |
|---------------------------------|--------------------------------|-----------------------------|--------------|
| Oscilloscope | Tektronix | *453 | |
| Volt/Ohmmeter (VOM) | Triplet | | 29-13510 |
| Unwrapping Tool | Gardner-Denver (Cat. H812A) | 505 244-475 | 29-18387 |
| Hand Wrap Tool | Gardner-Denver (Cat. H811A) | A-20557-29 | 29-18301 |
| Diagonal Cutters | Utica | 47-4 | 29-13460 |
| Diagonal Cutters | Utica | 466-4 (modified) | 29-19551 |
| Miniature Needle Nose Pliers | Utica | 23-4-1/2 | 29-13462 |
| Wire Strippers | Millers | 101S | 29-13467 |
| Solder Extractor | Solder Pullit | Standard | 29-13467 |

Table 7-1 (Cont)
Maintenance Equipment Required

| Equipment or Tool | Manufacturer | Model, Type, or Part No. | DEC Part No. |
|---|--------------|-----------------------------|--------------------------------|
| Soldering Iron (30 watts) | Paragon | 615 | 29-13452 (IC type head) |
| Soldering Iron Tip | Paragon | 605 | 29-19333 |
| 16-pin IC Clip | AP Inc. | AP923700 | 29-10246 |
| 24-pin IC Clip | AP Inc. | AP923714 | 29-19556 |
| KM11 Option | DEC | KM11-A | **W130,W131 |
| Maintenance Modules | | | |
| Maintenance Card Overlay (KD11-A) | DEC | | 559081-0-12 |
| Maintenance Card Overlay (KE11-E,F, KT11-D) | DEC | | 5509081-0-13 |
| Module Extender Board | DEC | | W900 |

Table 7-1 (Cont)

Maintenance Equipment Required

| Equipment or Tool | Manufacturer | Model, Type, or Part No. | DEC Part No. |
|----------------------|--------------|-----------------------------|--------------|
|----------------------|--------------|-----------------------------|--------------|

| | | | |
|--------------------|-----|--------------|--|
| Regulator Extender | DEC | 70-08850-0-1 | |
|--------------------|-----|--------------|--|

Cable

* Tektronix Type 453 Oscilloscope is adequate for most test procedures; Type 454 (or equivalent) may be required for some measurements.

** W133 is a dual version of W130. It provides the drivers for two W131 maintenance cards. The 130 may still be used; however, two units would be required for simultaneous monitoring of the basic processor and options. Two W131s are required for simultaneous monitoring in any case.

7.4 PREVENTIVE MAINTENANCE

Preventive maintenance consists of specific tasks to be performed periodically; its major purpose is to prevent future failures caused by minor damage or progressive deterioration due to aging. A preventive maintenance log book should be established and necessary entries made according to a regular schedule. This data, compiled over an extended period of time, can be very useful in anticipating possible component failures resulting in module replacement on a projected module or component reliability basis.

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to conditions at the particular installation site that are dependent on environmental conditions, usage, etc. Mechanical checks should be performed as often as required to allow the fans and air filters to function efficiently. All other preventive maintenance tasks should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 1000 operation hours or every three months, whichever comes first.

7.4.1 Physical Checks

The following procedure contains the necessary steps required for mechanical checks and physical care of the PDP-11/40:

| Step | Procedure |
|------|--|
| 1 | Clean the exterior and interior of the cabinet with a vacuum cleaner or clean cloth moistened with non-flammable, non-corrosive solvent. |
| 2 | Check all fans to ensure that they are not obstructed in any way. Vacuum clean the air vents of the upper and lower logic fan housings, and upper and lower regulator fan housings. Remove and wash the filters in the cabinet fan, located in the top of the cabinet. |
| 3 | Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Repair or replace any defective wiring or cable covering. |
| 4 | Inspect the following for mechanical security: LED or lamp assemblies, jacks, connectors, switches, power supply regulators, fans, capacitors, etc. Tighten or replace as required. |

- 5 Inspect all module mounting panels to ensure that each module is securely seated in its connector and the locking-releasing mechanism is functioning properly.

- 6 Inspect power supply capacitors for leaks, bulges, or discoloration and replace as required.

- 7 Inspect module guides for wear, damage, and secure fastening.

7.4.2 Electrical Checks and Adjustments

The following checks should be made when the system is first installed and whenever a new component is installed in the system (such as an additional regulator, processor option module, interface module, etc.).

7.4.2.1 Voltage Regulator Checks - Perform the power system checks listed in Table 7-2. Use a VOM to check the output voltages under normal load conditions. Use an oscilloscope to measure the peak-to-peak ripple content on all dc outputs. Each voltage regulator has an adjustment potentiometer located just below the output indicator lamp. If the regulator output is not within the specified tolerance, adjust as required to obtain an acceptable output (use a non-conducting adjustment tool). If a voltage regulator cannot be adjusted to meet specifications, remove and replace the regulator.

Table 7-2

DC Output Voltage Checks

| Regulator | Voltage | Ripple Peak-to-Peak |
|--|-------------|------------------------|
| H744 +5V Regulator (slot A) | +5.0 volts | 0.15 volts |
| H744 +5V Regulator (slot B) | +5.0 volts | 0.15 volts |
| H744 +5V Regulator, options1 (slot C) | +5.0 volts | 0.15 volts |
| H745 -15V Regulator (slot D) | -15.0 volts | 0.45 volts |

Table 7-2 (Cont)
DC Output Voltage Checks

| Regulator | Voltage | Ripple Peak-to-Peak |
|----------------------------------|----------------------|------------------------|
| H745 - 15V Regulator (slot E) | -15.0 volts | 0.45 volts |
| H742 Power Supply | +8.0 (6.8 to 9.2) | 0.24 volts |

7.4.2.2 860 Power Control - Operate the REMOTE/OFF/LOCAL switch S1 on the 860 Power Control to make sure power is turned on in the LOCAL position and disconnected in the OFF position. Return S1 to the LOCAL position after performing this test if only a basic (single box) PDP11/40 is present. See section 6.4 of this manual for other connections.

7.3.2.3 Ac Power Connector REceptacles - Test the output voltage at each plug to be sure 115- or 230-volt ac power is available.

7.4.3 ASR33 Teletype

7.4.3.1 Preventive Maintenance Checks - Check the following ASR33 items during system preventive maintenance:

- a. Check distributor plates for deposits.
- b. Check platen and typewheel for deposits.
- c. Check wires around distributor area for secure mechanical and electrical connections.
- d. Check the print hammer and replace if worn.
- e. Rotate the mainshaft manually and check that movement is free. If movement is restricted, check clutch assemblies.
- f. Check typewheel pinion racks, and gears for dirt.

7.4.3.2 Lubrication - Use a 50-50 mixture of 20 weight, non-detergent oil and STP oil additive for viscosity improvement to perform the following lubrication, except where otherwise noted:

- a. Oil all clutch assemblies.
- b. Oil all felts until saturated.
- c. Lightly oil all pivot points.
- d. Oil drive motor at both lubrication points provided.
- e. Oil print carriage bearings.
- f. Oil main shaft bearings.
- g. Oil bearing on function shaft.
- h. Oil the eye ends of all springs.
- i. Oil the typewheel pinion and gear.
- j. Oil repeat mechanism in keyboard assembly.
- k. Clean the dashpot assembly and lubricate it with graphite dust.

NOTE

Do not put oil in the dashpot.

1. Grease the teeth on spacing ratchet.

7.4.4 LA30 DECwriter

7.4.4.1 Preventive Maintenance Schedule - When the LA30 DECwriter is included in the system, it is supplied with a maintenance manual that contains detailed preventive maintenance procedures. The items to be cleaned, inspected, and replaced on a regular schedule are listed in the following chart:

| Printing Interval (Hours) | Clean | Inspect | Replace |
|------------------------------|---|------------------------------------|--|
| 300-500 | 1. Ribbon Idlers (Para. 5.2) | 1. Ribbon Tension | 1. Print Head Assy (Para. 5.4.2) |
| 2000 | 1. Ribbon Motors (Para. 5.2) 2. Carriage Assy Round Shaft (Para. 5.2) 3. Ventilating Fan Blades, if nec- essary (Para. 5.2) | 1. Ribbon Tension (Para. 5.4.6) | |

Printing Interval Clean

Inspect

Replace

(Hours)

4. Linkage Pins,
Ratchet and
Pawl Mechanism
(Para. 5.2)

NOTE

Paragraphs referenced in this chart refer to applicable paragraphs in Chapter 5 of the LA30 DECwriter Maintenance Manual.

7.4.4.2 Cleaning Procedures - Always use a clean, lint-free cloth to wipe off outside surfaces and a lightly-oiled cloth to remove any dust or ink from inside the unit. (The ink is oil-base). Use commercial furniture or automotive wax to protect the outside of the cover. Dust the cover and wipe the keyboard clean whenever paper is replenished.

Do not attempt to clean the print head assembly; rather, replace it after 300-500 hours of operation. The replacement procedure is described in Paragraph 5.4.2 of the LA30 DECwriter maintenance Manual. At the time it is replaced, wipe the ribbon idlers clean with an oiled cloth.

After 2000 hours of operation, remove each ribbon motor, as described in Paragraph 5.4.5 of the LA30 manual. Apply a light oil to the lower bearing felt. At this time, lubricate the carriage assembly round shaft, DEC part number 74-8656-1/2. Spray a light coating of Molykote 557 along the entire shaft and wipe lightly with a dry cloth to leave a thin coating of lubricant on the shaft.

NOTE

Do not attempt to clean ^{or} ~~of~~ vacuum-clean the control box assembly. It will function better if left alone.

If necessary, after 2000 hours of operation remove the fan and wipe the blades clean with an oiled cloth. The fan motor does

not require scheduled lubrication.

At the 2000-hour interval of preventive maintenance, check the paper advance mechanism linkage pin and pivot pins for grease and freedom of movement. Normally, no maintenance is required. However, if the terminal is in an extreme ambient temperature environment, these pins will require lubrication. If so, disassemble the linkages and apply Molykote B2KR grease to all bearing surfaces.

NOTE

The two dark green nylon rollers must remain free of oil or grease to allow the mechanism to function properly.

7.4.5 PC05 High-Speed Paper-Tape Reader/Punch (option)

The PC05 High-Speed Paper-Tape Reader/Punch includes a ROYTRON 500 Series Reader/Punch mechanism. Complete lubrication and preventive maintenance instructions for this mechanism are contained in the Preventive Maintenance Section of the Roytron Maintenance Manual, which is supplied with the PC05. In addition to the preventive maintenance procedures listed in that manual, perform the following mechanical and electrical checks as part of the system preventive maintenance procedure.

7.4.5.1 Mechanical Checks - Inspect the PC05 as follows:

| Step | Procedure |
|------|--|
| 1 | Visually inspect the general condition of the tape reader. |
| 2 | Clean the PC05, inside and out, using a vacuum cleaner or a clean cloth that has been moistened with a non-flammable solvent. |
| 3 | Lubricate the chassis slide mechanism with a light machine oil. Wipe off excess oil. |
| 4 | Inspect all wiring and replace any defective wiring or defective cables. |
| 5 | Check that the READER FEED switch, READER ON/OFF LINE switch light condensor, phototransistor assembly, depressor arm, hold-down bracket, all connectors and circuit modules, tape feed motor, front cover, and resistor assembly are mechanically secure. |

7.4.5.2 Electrical Checks - Perform power supply output tests listed in the following chart:

| Output | Pin Number | Tolerance | Ripple (peak-to-peak V) |
|-----------|------------|------------------|----------------------------|
| +5 volts | A1A2 | ± 0.25 volts | 0.1 volts |
| -15 volts | A1B2 | ± 1.0 volts | 0.1 volts |
| -18 volts | B8V2 | ± 2.0 volts | 1.0 volts |
| -36 volts | A8V2 | ± 4.0 volts | 1.0 volts |

Use a VOM to measure output voltage and an oscilloscope to check ripple voltage. The +5- and -15-volt outputs are adjustable; the -18- and -36-volt outputs are not adjustable.

7.5 USE OF MODULE EXTENDERS

The W900 module extender is a double-height, multi-layer etch board that provides one-to-one connections between module connectors and corresponding processor backplane connector slots. Thus, three W900 module extenders can be used to extend a PDP-11/40 hex-size module from the processor backplane to provide access to ICs and discrete components for test purposes under active operating conditions.

CAUTION

Do not attempt to extend more than one module at a time while performing tests. Note that the processor clock may have to be adjusted to allow operation with the modules extended.

7.6 PDP-11/40 POWER SYSTEM MAINTENANCE

System maintenance of the PDP11/40 power system consists of replacement of the modular elements. Offline repair is then necessary for the replaced element, and is presented in this section. Detailed circuit operation is presented in paragraph 6.5 and is necessary for background to the troubleshooting procedures of this section.

7.6.1 Circuit Tracing

The user should first read the description of the power system contained in Chapter 6 of this manual. By next referring to the schematic and interconnecting diagrams in the print set, the user should be able to trace through the ac power control and dc power distribution circuits from the primary ac input connectors to the dc inputs of each logic module.

7.6.2 Voltage Regulator Tests (Off-Line Repair)

Figure 7-1 shows a recommended bench test source that can be fabricated from standard parts. It also shows the bench test loads used to test the voltage regulator outputs under various load conditions. No additional test equipment or tools are required other than those listed in Table 7-1.

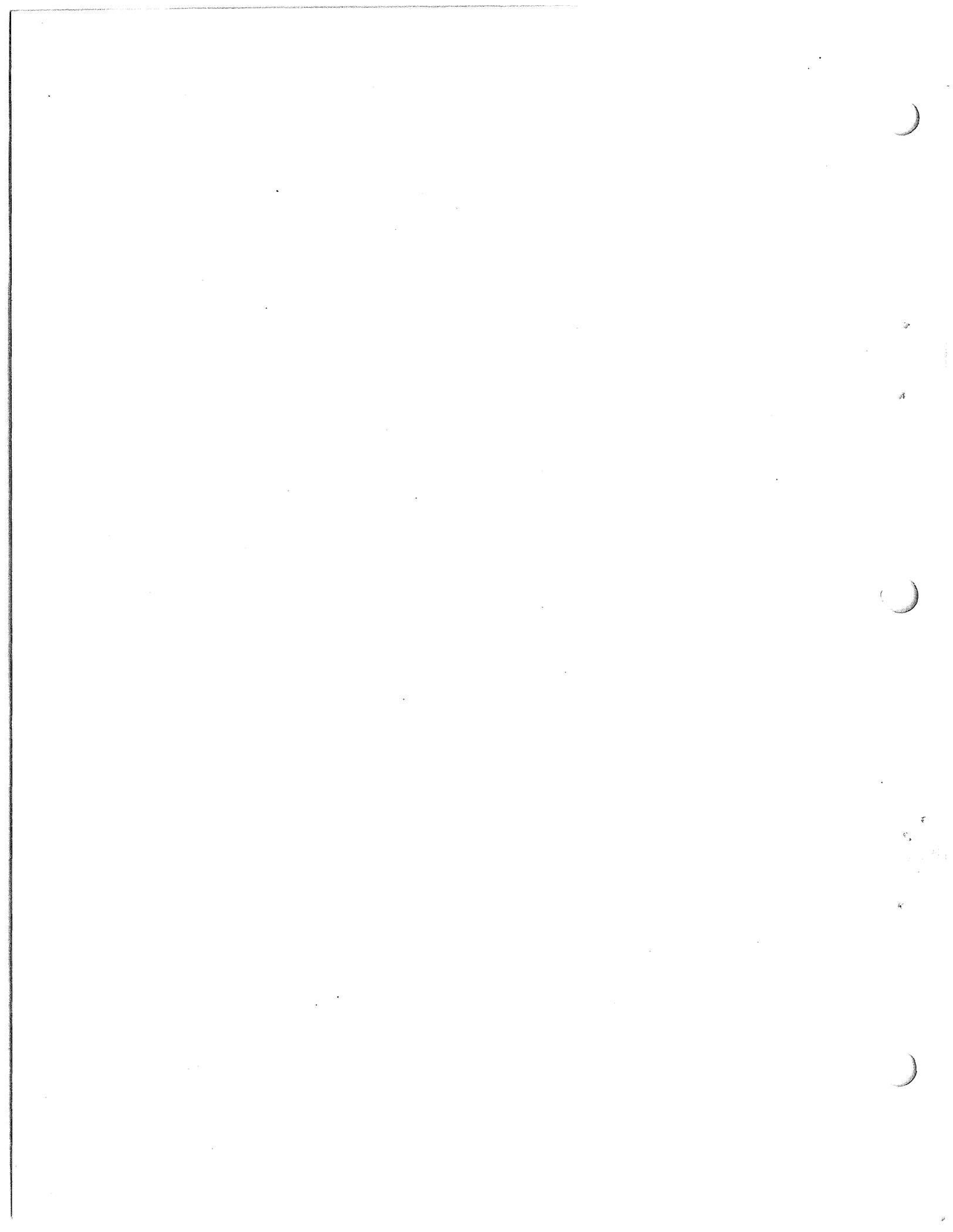
The voltage regulator extender cable allows a voltage regulator to be removed from its assigned slot on the H742 power supply to provide access for test purposes. This cable only supplies ac input power to the voltage regulator. An additional voltage regulator bench test source and load fixture can be fabricated from standard DEC parts to perform troubleshooting and performance tests under the various load conditions required. The circuit schematic and part numbers required to build this optional test fixture are shown in Figure 7-1.

Whenever a power system fault has been isolated to a voltage regulator, examine the internal fuse F1. A blown fuse usually means that the main pass transistor Q2, and/or one of its drivers (Q3, Q4) is short circuited. This can be checked by using the following procedure:

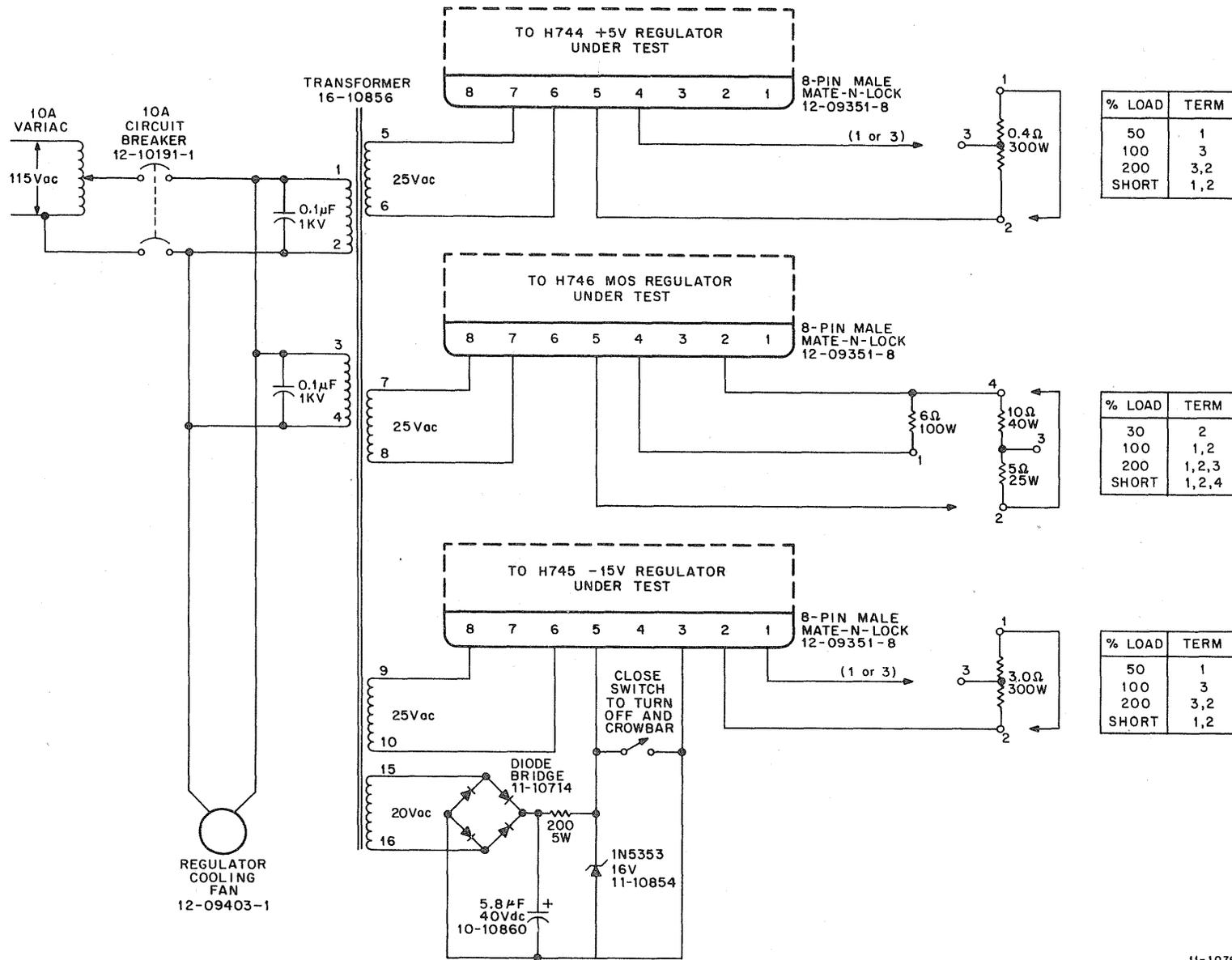
Step

Procedure

- 1 Check for damage to base-emitter bleeder resistors and scorching of the etched board in the area or Q3 and Q4.
- 2 If the pass transistor and drivers are not faulty, the fault may be caused by continuous base drive to the first driver (Q4). Check level shifter Q5 for a short circuit.
- 3 Check the resistance to ground at the input to the precision voltage regulator integrated circuit E1 (pins 4 and 5) to determine if an external short circuit is holding the IC in conduction. The approximate resistance to ground is listed for each voltage regulator in Table 7-3.
- 4 Use a VOM to check for short circuit between fuse terminals and ground. Possible short circuits involving mounting TO-3 components to the heat sink may be located by connecting the VOM leads between TO-~~3~~³ cases and a regulator mounting screw on the end of the heat sink.



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Figure 7-1 Voltage Regulator Test Bench Source and Loads

Table 7-3

Regulator Resistance to Ground

| Regulator Type | Inverting (-) Input at Pin 4 | Non-Inverting (+) Input at Pin 5 |
|-------------------|---------------------------------|-------------------------------------|
| H744 | 20K | 1.5K |
| H745 | 1.5K | 5K |

A voltage regulator that provides no output, or a low output, without causing fuse F1 to blow, probably has a short circuit in the output. This can be checked by the following procedure:

NOTE

An activated crowbar, or a short-circuited output, in an otherwise properly operating voltage regulator does not cause F1 to blow.

| Step | Procedure |
|------|--|
| 1 | If fuse F1 is not blown, and the area of etched circuit around the ac input to the bridge circuit is not damaged, it is safe to apply an ac input to the voltage regulator to determine if the regulator is overloaded by a short circuit across the output. |

Step

Procedure

- 2 Connect the voltage regulator to the bench test source and advance the variac to about 90 volts. An audible tone indicates overload conditions.

If the output is near 0 volts, turn the voltage adjustment fully CCW and repeat the test.

- 3 If the regulator appears overloaded, check for short circuits across the output and for a component failure in the crowbar circuit.

NOTE

H744 revision G modules contain an additional SCR in the crowbar circuit to pull down the +15V control voltage and hold the IC drivers off until ac power is removed. Therefore, the "overload whistle" may not be heard under failure conditions of some of these modules.

If a faulty voltage regulator does not exhibit any of the previous symptoms, then perform the following steps:

Step

Procedure

- 1 Apply 115 Vac to the bench test source (25 Vac at the voltage regulator input) with no load on the regulator output.

Step

Procedure

- 2 Check for 30 Vdc across filter capacitor C1.
- 3 Check for +15 Vdc at pin 12 of precision voltage regulator E1. No voltage at this point could mean that Zener diode D2 (in the H744) has failed.
- 4 Check for 6.8 to 7.5 Vdc at pin 7 of E1 with respect to ground (pin 6).
- 5 If all output measurements in the above steps are correct, and if there is no output voltage, then pin 5 of E1 should be positive with respect to pin 4.

Pin 2 of E1 should be +0.6V with respect to pin 3.

If it is not, connect emitter and base of Q5 together. If a 0.6V indication is then obtained, precision voltage regulator E1 is not faulty and the fault is probably caused by Q5 or Q4.

7.6.3 Voltage Regulator Test (After Repair)

After a voltage regulator has been repaired, it should be tested with the bench test source before installing it into the system. Use the recommended bench test loads when performing the following steps:

| Step | Procedure |
|------|--|
| 1 | Connect the repaired voltage regulator to the appropriate source connector. |
| 2 | Set voltage adjustment full CCW and set load to zero. |
| 3 | Close input circuit breaker and advance variac until output voltage is indicated (at approximately 60-80 Vac input). No audible noise should be heard under no-load conditions. |
| 4 | Advance variac to 130 Vac and return to 115 Vac. |
| 5 | Make certain Q2 is connected and soldered before loading the regulator. |
| 6 | Apply a 30% to 50% load. The output voltage should remain nearly constant. A clean whistle may be heard. A buzz or a harsh hissing sound indicates possible instability. Check waveforms as shown in Figure 7-2. |

Step

Procedure

7 Apply 100% load and set voltage adjustment for nominal output as follows:

H744 +5.10 Vdc

H745 -15.10 Vdc

8 Apply 200% load and check for a decrease in the frequency and the output voltage.

CAUTION

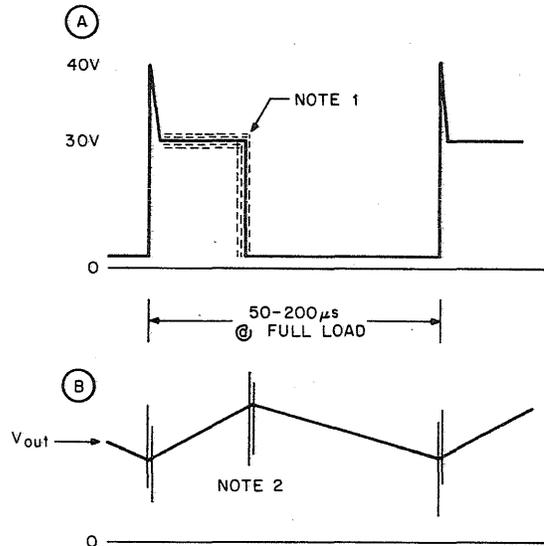
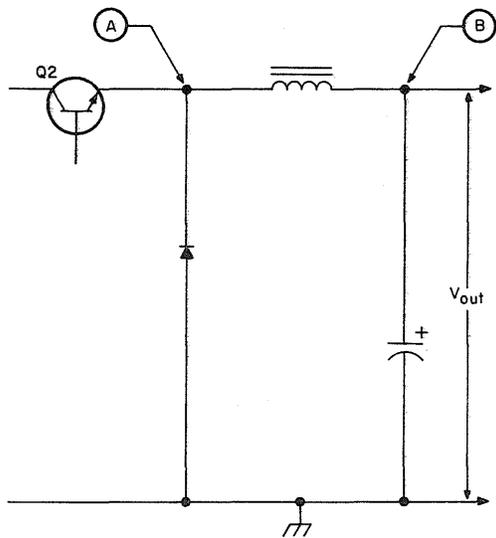
If the output voltage does not decrease noticeably (1 volt on H744; 1 to 5 volts on H745), do not attempt the following short-circuit test.

9 Short circuit the output. The regulator should continue to operate at a low frequency, with a clean, smooth whistle and stable waveforms.

10 Increase the voltage adjustment and observe the output voltage when the crowbar circuit fires. A sudden decrease in frequency and output voltage should be observed. The output voltage should be within the following ranges:

H744 6.00 - 6.65V

H745 16.8 - 20.5V



NOTE 1: 30 volt level shifts with AC input voltage. This value doubles in H746 (i.e. 60V). Small 120Hz jitter is normal

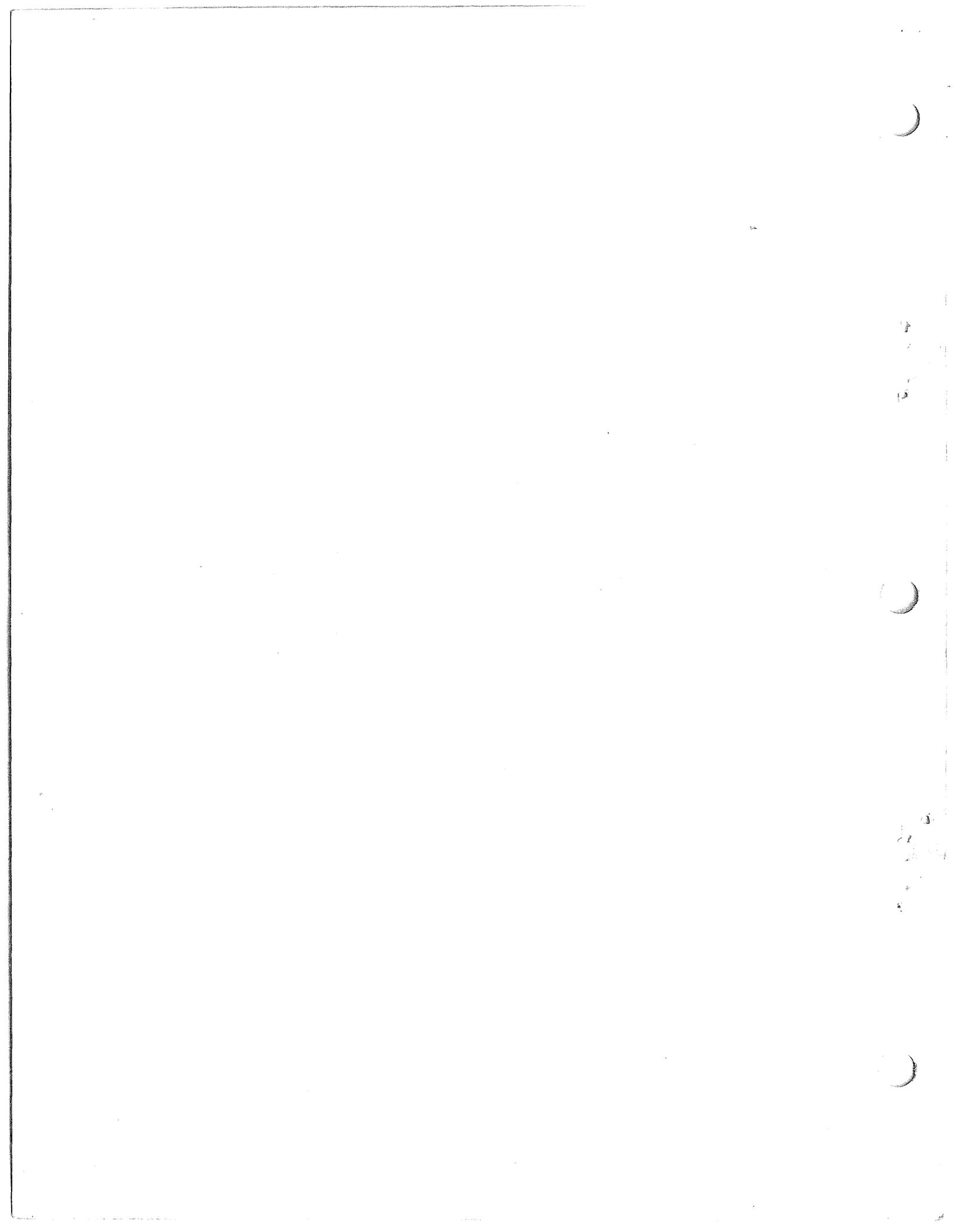
NOTE 2: Output ripple and noise as follows:

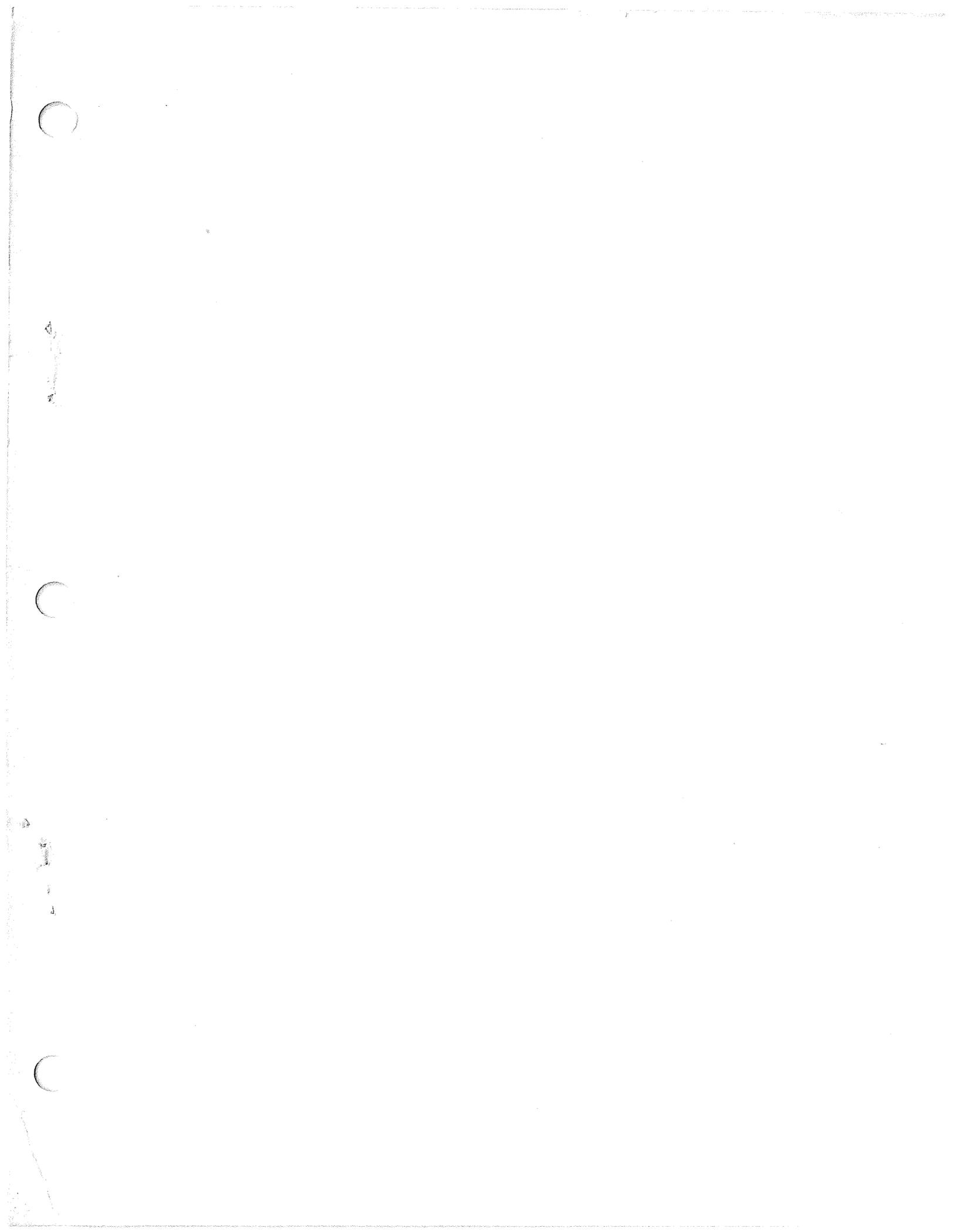
| | H744 | H745 | H746 |
|-----------------|--------------------|--------------------|--------------------|
| RIPPLE (P to P) | 3% max. 2% typ. | 3% max. 2% typ. | 3% max. 2% typ. |
| NOISE (PEAK) | 1% | 1% | 1% |

Measure noise with a short 100Ω terminated piece of foil coax. Normal 10:1 scope probe will not give an accurate noise measurement.

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Figure 7-2 Typical Voltage Regulator Output Waveforms







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