digital INTEROFFICE MEMORANDUM

SUBJECT: Programming Considerations PDP-11

DATE: January 26, 1670

TO: List C

FROM: John Hittell

LOCATION:

I am in the process of collecting a list of interesting "items" about the PDP-11 system. If any of you encounter any item that you feel I might be interested in, would you please contact or send the information to me. I will collect and redistribute the information.

IRREGULARTIES OF PDP 11

1) MOV %R, (R)+

If Register R contained 1000
this instruction would put 1002
into location 1000.

Believe this exists with all binary
instructions where source and destination
are the same register, and the source
is data and the destination is auto Incremented.

2) JMP (R)+
JSR %N, (R)+

In these two cases the Auto Increment
takes place before the jump, there
for you jump to a destination 2 greater
than expected.

3) With a flag up on a device the code:

```
CLR   177776     ; PROCESSOR PRIORITY ZERO
BIS   #1ØØ, CSR; SET INTERRUPT ENABLE
BIC   #1ØØ, CSR ; CLR INTERRUPT ENABLE
```

No interrupt window occurs between the
setting and clearing of interrupt enable
in the control and status register of a device.

4) The Reset instruction clears the run
light. In any program that performs
iteration of groups of instructions that include
Reset the precessor appears not to be running,
due to the duty cycle of the Reset instruction.

5) Reset is supposed to return the outside
world to the power up state. What if
a TTY is given a Read command just before
a command to Reset is issued. 80 mill seconds
after the Reset settles the flag comes up.