PDP-11/40 Technical Memorandum # 13

Title: A Microprogrammed 11/40 CPU

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PDP-11/60 think before 11/40 design.

CONTENTS

1.0 INTRODUCTION

An eight bit microprogram CPU was looked into and was partially designed and analyzed with different existing components. The purpose of the above project was to aid us in arriving at a valid estimate, as far as speed, cost, packaging, and power dissipation for a microprogram 11/40 CPU with using different types of semiconductor components. The flow diagram used for such an implementation is shown in Figure 1. A breakdown of each of the sections drawn in the diagram as far as cost, technology, speed, power dissipation, and packaging is analyzed in this report. Finally, a similar estimate on a microprogram 11/40 CPU is made using today's components with some conclusions drawn.

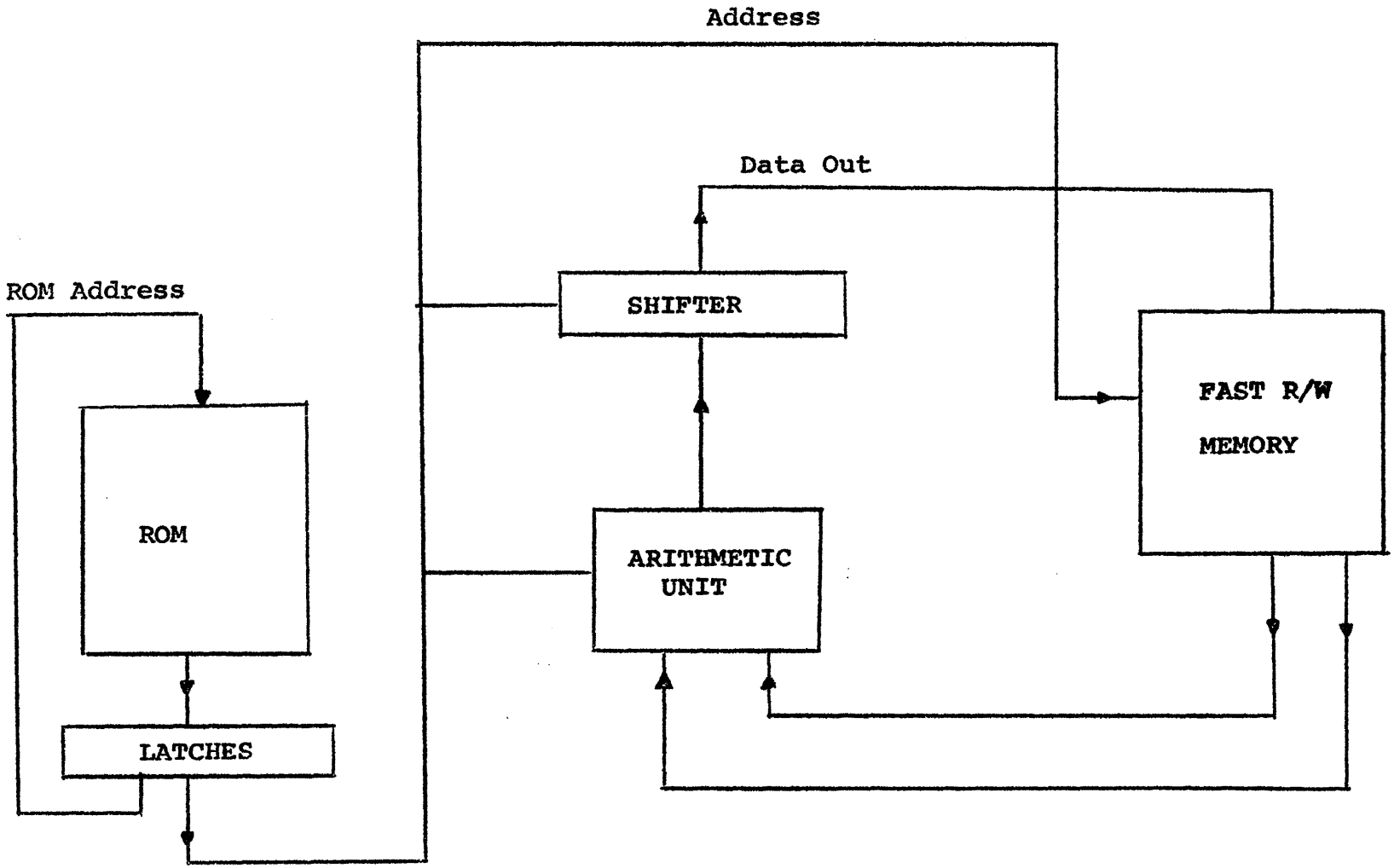
Address
Data Out
ROM Address
SHIFTER
FAST R/W
MEMORY
ROM
ARITHMETIC
UNIT
LATCHES

Figure 1.

2.0 BRIEF DESCRIPTION OF A MICROPROGRAMMED INSTRUCTION LOOP

The microprogram loop consists basically of Read Only Memory (ROM), an arithmetic unit plus shifters, and a scratch pad (R/W) memory (RAM) which can be a mixture of registers and fast semiconductor memories. This R/W Memory is usually accessed by the ROM or by the outside.

The ROM's main function is to be the storage area for the microprogram instructions. Each ROM word can contain the source and destination addresses from and to the RAM, the next ROM address, the type of operation required, the shifting controls. and some test bits. The wider the word length of the ROM, the less control or address decodings are needed, and thus, the faster the cycle time. This loop consists most of the hardware required for a microprogrammed CPU, except for control logic. A detailed analysis of the ROM, RAM, and the arithmetic unit is discussed in the next sections of this report.

3.0 READ ONLY MEMORY

The bipolar ROMs seems to be the most attractive memories to use for our application today as far as speed, cost, and availability. Different types of organizations are available from different vendors without any problems with second sourcing. The most popular organizations are the 32 words x 8 bits and the 256 words x 4 bits, both of which have fully decoded addresses and open collector outputs for word expansion capability.

Maximum read access time for the above devices is 60 ns and cost per bit is 5 cents using the large organization, and 10 cents for the small one. Delivery time for a new mask is about three months.

Both of the above units come in a 16 pins dual in line packages with 1 mw and 2 mw maximum power dissipation per bit for the large and small organization respectively.

To avoid extra costs and time delays, a prototype machine using Read Only Memory can use RAM instead of ROM. The most popular bipolar RAM available in the market today, which is suited for such an application, is the 16 words x 4 bits organization. Properties of this type memory are discussed in the next section of this report.

4.0 FAST R/W MEMORY

A read/write scratch pad memory can be implemented in many different ways with today's components. Bipolar semiconductor components are the only ones considered here because of its availability and cost. the table that follows gives a list of various bipolar components with their respective speed, cost, power dissipation, packaging, and expandability. The component underlined in the table is the one, I think, is best suited for our application.

Table 1.

Component No.	Description	IC Packs Req. for 16 bits	Max Pwr Dis./Bit	Speed Read	Speed Write	Today's Cost/Bit	Expandability
74H74	2 D type flip-flop per package	12	120 mw	30 ns	35 ns	$0.50	16 wxn bits
MC4015	4 D type flip-flop per package	8	20 mw	30 ns	40 ns	0.44	16 wxn bits
DM8551	4 D type flip-flops open collect. outputs	4	18 mw	40 ns	55 ns	1.00	40 wxn bits
74170	4 w x 4 bits per IC.	1	10 mw	55 ns	45 ns	0.25	1024 wxn bits
Intel 3101	16 w x 4 bits per IC.	1/4	20 mw	60 ns	40 ns	0.37	1024 wxn bits

*Read time includes the address decoding time and read access time for the cell, while write time includes data set up time and write time. All of the components used, except for the last one, can afford some overlap between the read and write time.

5.0 ARITHMETIC UNIT

The most attractive arithmetic unit available in the market today as far as performance, and cost, is the 74181 unit made by Texas Instrument. A total of 32 different arithmetic and logic operations can be achieved by this unit on two 4 bits words. These operations include add, subtract, complement, clear, set, increment, decrement, inclusive or, exclusive or, etc.. It also provides a check if the two input words are equal. These units can be cascaded and used to perform operations on word lengths of up to 128 bits. However, word length effects the speed of the arithmetic operations, and a carry look ahead units (74182) can be used to speed up the operations.

The table that follows gives the cost, maximum propagations time, and number of IC packages required for different word lengths. Maximum power dissipation per bit using the above arithmetic units is 40 mw.

Table 2

Word Length	Speed		Number of IC Packages		Total Cost*
	Logic Operation	Arithmetic Operation	74181	74182	
8 bits	50 ns	60 ns	2	0	14.00
16 bits	50 ns	60 ns	4	1	29.67
32 bits	50 ns	90 ns	8	3	61.01
64 bits	50 ns	90 ns	16	5	120.35

* The 74181 comes in a 24 pins dual in line package at a current cost of $7.00.
The 74182 is a 16 pins dual in line package and costs $1.67.

6.0 SHIFTERS

For the multiple levels of shifting and rotating implementations, discrete IC components are the recommendable components to use today as far as speed and cost. IC components such as 74H53, 74H60, and 74H62 represents one level of gating plus flexibility in expansion.

An average of two IC packages are required per bit for 16 different shifting and rotating operations with buffering at the output. Maximum propagation delay for a shifting operation plus buffering is 30 ns.

Average cost for shifting per bit is about one dollar, and the average power dissipation is 150 mw.

7.0 MICROPORGRAMMED INSTRUCTION CYCLE TIME

The speed of a microprogram instruction is heavily dependent on the technology used for implementation. With using the bipolar components mentioned earlier, the maximum cycle time achieved is 180 ns which is broken down into the following:

1.	ROM latching time	20 ns max
2.	Read access time for the R/W memory plus address decoding time	55 ns max
3.	Arithmetic operation time (16 bits words)	60 ns max
4.	Shift time	30 ns max
5.	Write set up time	15 ns max
6.	Skew time	10 ns max

The read access time for the ROM is not accounted for in computing the cycle time since the next ROM' address is usually contained in ROM instruction bits. Naturally, this access time should be added to the cycle time at the start of the microprogram loop and upon branching. In that case, the cycle time is delayed by 80 ns. Also, note that by using the 74170 components for the R/W memory, a good deal of read and write overlap is achieved.

Improvements on the cycle time can be made in the future by utilizing schottky gates in some parts of the loop such as the shifters, the ROM latch network, and the R/W address decoders. By doing so, we can easily reduce the cycle time by 30 ns. Also, that the only effective way to reduce speed is to implement all the loop, except the ROM, by ECL logic where a 100 ns cycle time can be achieved. However, this will tend to increase the number of components and the cost by at least 30 percent. In addition to cost, there will be other problems we might have to face with such as; system noise, packaging, and single source items. Therefore, I recommend staying out for the time being from using fast ECL logic, especially with our present system packaging schemes.

8.0 COST ESTIMATE OF A MICROPROGRAMMED 11/40 CPU

A breakdown of parts used in an 11/40 microprogrammed CPU is listed in the table that follows. Costs do not include wire wraps, mounting panels, system checkout, or cables.

Table 3.

Logic	Size	No. of IC Packages required	Package Type	Max Pwr Dissipation	Cost 1970	Cost 1972
ROM	512w x 48 bits	24	16 pins	12W	960	450
RAM	32w x 32 bits	64	16 pins	10W	200	120
Arithmetic Unit	56 bits	18	14IC of 24 pins 4IC of 16 pins	2.5W	105	50
General Purpose addr.	16 bits	4	16 pins	.5W	12	6
General Registers	10 x 16 bits	80	14 pins	15W	60	35
Shifters	56 bits	100	14 pins	5W	50	30
Control Logic	--	300	mixed	40W	300	175
Line Drives and Receivers	120 lines	50	mixed	5W	50	30
Terminating Resistors	120 lines	--	--	6W	5	4
Etched Boards	15 Quad. size	--	--	--	450	350
Power Supply	--	--	--	--	150	120
TOTAL		640	mixed	96W	2342	1370

9.0 CONCLUSIONS

The following factors should be considered in deciding whether we should build a microprogrammed or a conventional type 11/40 CPU.

Economy

To my knowledge, a microprogrammed 11/40 CPU can use at least 10 percent less control logic than that of a conventionally built 11/40 CPU. However, in adding the microprogram storage, the overall microprogrammed machine can now cost about 25 percent more than the conventional one. This cost figure will change substantially within the next two years, as it is estimated that the cost of the microprogram storage will drop by half by 1972 to give the convential CPU a cost advantage of only 10 percent over the microprogrammed one.

Speed

Using the same type technology in both machines, a conventional 11/40 CPU can go as fast as 120 ns/per machine cycle time compared to 180 ns for a microprogrammed instruction without including branching time. Thus, if a fast machine is required, an exclusive microprogrammed machine is not the way to go.

Ease of Design and Flexibility

A microprogrammed machine is known to be more flexible and easier to design. Also, as the computer instruction set grows the microprogrammed machine's logic external to the microprogram storage area needs not to increase while the control logic of the conventional machine increases.

Packaging

Again, a microprogrammed machine wins here since a large portion of it is amenable to use MSI chips. I estimate that a convential machine uses at least 10 percent more IC packages than that of a microprogrammed machine. However, this figure might drop if custom designed LSI chips are used two years from now.