

SET 7777 = 5301 for BINLOADER
(that should be the only corrupted
location after running CDTST1)

IDENTIFICATION

CPTST2

PRODUCT CODE: MAINDEC-12-D0AB-B

PRODUCT NAME: PDP-12 CP TEST 2
(SKIP AND DATA HANDLING)

DATE CREATED: SEPTEMBER 19, 1969

MAINTAINER: DIAGNOSTIC GROUP

AUTHOR: JAMES KELLY

SNS = 77

8MODE

start 20

halt @ 0022, 8MODE, ACK = 0000

CONT

halt @ 0026, 4MODE, ACK = 7777

CONT

resetting any SNS switch should

BEL RINGS EVERY 27 SECONDS

- a. Set the teletype reader switch to FREE.
- b. Open the teletype reader and insert the program tape so that the arrows on the tape are visible to, and pointing toward the operator.
- c. Close the reader and set the reader switch to START.
- d. Set the teletype front panel switch to ON LINE.
- e. Set the LEFT switch to 7777.
- f. Set the RIGHT switch to 4000.
- g. Set the MODE switch to 8 mode.
- h. Depress I/O preset.
- i. Depress START LS.
- j. When the program tape has been read in the computer will halt.
- k. The ACCUMULATOR must be = 0000, if it is not, a read in error has occurred and one might try reloading the binary loader.
- l. Remove the program tape from the reader.

NOTE: This program can be started in either LINC or 8 mode. This feature was incorporated to reduce the possibility of error. However, the preferred method and the one listed below is to start the program in the 8-mode.

4. STARTING PROCEDURE

- a. Remove the paper tape from the teletype.
- b. Set the 6 SENSE SWITCHES to all ones.
- c. Set the MODE switch to 8 mode.
- d. Depress I/O preset.
- e. Set IF instruction field switches to all 0.
- f. Depress START 20.
- g. The computer will halt at address 0022, i.e. MEMORY ADDRESS register = 0022, in 8 MODE, with the ACCUMULATOR = 0000.
If any of these circumstances do not exist it is a hardware error and must be rectified before proceeding.
- h. Depress CONTINUE.
- i. The computer will halt at address 0026, in L MODE, with The ACCUMULATOR: 7777.
If any of these circumstances do not exist it is a hardware error and must be rectified before proceeding.
- j. Depress CONTINUE.
- k. The program is now running and any further computer halts are errors and must be evaluated by referring to the listing.
- l. The test will ring the teletype bell once every 4096 passes. This should occur every 25 seconds. If the bell does not ring it is a hardware error and must be rectified before proceeding.

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- b. Open the teletype reader and insert the program tape so that the arrows on the tape are visible to, and pointing toward the operator.
- c. Close the reader and set the reader switch to START.
- d. Set the teletype front panel switch to ON LINE.
- e. Set the LEFT switch to 7777.
- f. Set the RIGHT switch to 4000.
- g. Set the MODE switch to 8 mode.
- h. Depress I/O preset.
- i. Depress START LS.
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If any of these circumstances do not exist it is a hardware error and must be rectified before proceeding.
- h. Depress CONTINUE.
- i. The computer will halt at address 0026, in L MODE, with The ACCUMULATOR: 7777.
If any of these circumstances do not exist it is a hardware error and must be rectified before proceeding.
- j. Depress CONTINUE.
- k. The program is now running and any further computer halts are errors and must be evaluated by referring to the listing.
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4.1 Switch Settings

The left and right LSW and RSW have no effect on the program what so ever and their settings are of no concern.

The sense switches which under normal condition are set to 77 should be set to zero, one at a time, so be certain that they will cause error halts, i.e. the switch logic isn't tied to "TRUE".

5. ERROR ANALYSIS

In general the program listing is made up of 5 to 10 instruction modules which tests a skip, a bit or a gate and by stoping the coding just prior to the halt and the comments it's possible to determine what failed.

Any subroutine can be caused to scope loop by toggling in a jump to the beginning of the subroutine, and restarting the entire program. Great care must be exercised to remember where the jump was placed and to remove it after the hardware bug is found so that the program can test the entire computer.

/PDP-12 CP TEST PART 2 SKIP AND DATA HANDLING MAINDEC D0AB
 /COPYRIGHT 1969, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.
 /LINC-8 INSTRUCTION DEFINITIONS
 /MISCELLANEOUS

```

EXPUNGE
0000 HLT=0000 /HALT
0002 PDP=0002 /CHANGE TO PDP-8 MODE
0005 QAC=0005 /Z TO A1=J(11 BITS) I EQUALS 1 TO 11
0011 CLR=0011 /CLEAR ACCUMULATOR LINK, AND Z REGISTER
0014 ATR=0014 /{A6-A11}>R REGISTER
0015 RTA=0015 /R REGISTER>(A6-A11)
0016 NOP=0016 /NO OPERATION
0017 COM=0017 /C(AC)>C(A)
0040 SET=0040 /C(P=1)>BETA REGISTER (OR INDIRECT)
0200 XSK=0200 /SKIP ON 1777

/SHIFT
0240 ROL=0240 /ROTATE LEFT
0300 ROR=0300 /ROTATE RIGHT ALSO SHIFT RIGHT INTO MQ REGISTER
0340 SCR=0340 /SCALE RIGHT ALSO SHIFT RIGHT INTO MQ REGISTER

/SKIP
0400 SXL=0400 /SKIP IF EXTERNAL LEVEL IS =3
0415 KST=0415 /SKIP IF KEY HAS BEEN STRUCK
0440 SNS=0440 /SKIP IF SENSE SWITCH IS UP
0456 SKP=0456 /SKIP UNCONDITIONALLY
0450 AZE=0450 /SKIP IF ACCUMULATOR ZERO
0451 APD=0451 /SKIP IF ACCUMULATOR POSITIVE
0452 LZE=0452 /SKIP IF LINK ZERO
0453 IBZ=0453 /SKIP IF BETWEEN TAPE BLOCKS
0454 FLO=0454 /SKIP IF ADD OVERFLOW FLAG IS SET
0455 QLZ=0455 /SKIP IF BIT 11 OF MQ REGISTER IS 0

/OPERATE
0513 IOT=0513 /EXECUTE THE FOLLOWING IOT INSTRUCTION IN PDP-8 MODE

/ARITHMETIC
1000 LDA=1000 /LOAD ACCUMULATOR
1040 STA=1040 /STORE CONTENTS OF ACCUMULATOR
1100 ADA=1100 /ADD TO CONTENTS OF ACCUMULATOR
1140 ADM=1140 /ADD TO CONTENTS OF MEMORY REGISTER
  
```

1200 LAM=1200 /ADD CONTENTS OF LINK AND ACCUMU-
/LATOR TO CONTENTS OF MEMORY REGISTER
1240 MUL=1240 /MULTIPLY
6141 LINC=6141 /CHANGE TO LINC MODE
/HALF WORD OPERATIONS

1300 LDH=1300 /TRANSFER HALF WORD FROM MEMORY INTO
/THE RIGHT HALF OF ACCUMULATOR
1340 STH=1340 /TRANSFER THE HALF WORD FROM THE RIGHT
/SIDE OF ACCUMULATOR REGISTER INTO THE
/DESIGNATED HALF OF A MEMORY REGISTER
1400 SHD=1400 /SKIP IF THE HALF WORD IN ACCUMULATOR
/REGISTER AND THE MEMORY REGISTER DIFFER

/MEMORY REFERENCE OPERATIONS
1440 SAE=1440 /SKIP IF THE CONTENTS OF THE ACCUMULATOR
/EQUAL THE CONTENTS OF THE DESIGNATED
/MEMORY REGISTER
1500 SRO=1500 /SKIP IF THE RIGHTMOST BIT IN THE
/DESIGNATED MEMORY REGISTER IS 0
/AFTER TESTING, ROTATE THE CONTENTS
/ONE PLACE TO THE RIGHT,
1540 BCL=1540 /FOR EACH BIT POSITION OF MEMORY REGISTER
/Y THAT CONTAINS A 1, CLEAR THE
/CORRESPONDING BIT POSITION OF THE
/ACCUMULATOR (LOGICAL AND)
1600 BSE=1600 /FOR EACH BIT POSITION OF MEMORY
/REGISTER Y THAT CONTAINS A 1, SET THE
/CORRESPONDING BIT POSITION OF THE ACCUMULATOR (INCLUSIVE OR)
1640 BCO=1640 /FOR EACH BIT POSITION OF MEMORY
/REGISTER Y THAT CONTAINS A 1, COMPLEMENT
/THE CORRESPONDING BIT POSITION OF THE
/ACCUMULATOR (EXCLUSIVE OR)

/FULL ADDRESS
2000 ADQ=2000 /ADD THE CONTENTS OF THE DESIGNATED
/MEMORY REGISTER TO ACCUMULATOR
4000 STQ=4000 /STORE THE CONTENTS OF ACCUMULATOR
/IN THE DESIGNATED MEMORY REGISTER
/THEN CLEAR ACCUMULATOR
/LINC MODE JUMPS ARE NOT USED IN THIS TEST

7100 CLL=7100
7020 CML=7020
7604 LAS=7604
0000 ANQ=0000
1000 TAD=1000
3000 DCA=3000
7006 RTL=7006
7200 CLA=7200
2000 ISZ=2000
6046 TLS=6046

```
0002 *2
0002 0000 HLT /G141 FAILED TO LOAD IF @ 2001
0020 *20
/PRIOR TO STARTUP THE OPERATOR MUST SET ALL SENSE
/SWITCHES TO ONES AND LEFT AND RIGHT SWITCHES TO ZERO
/HLT AND SKIP TEST START IN PDP-8 MODE
/MAJOR START
0020 0002 START, PDP /GO TO 8 MODE
0021 0000 HLT /LINC MODE HALT
0022 7402 7402 /8 MODE HALT
0023 6141 LINC /GO TO LINC MODE
0024 1020 LDA*20
0025 7777 7777
0026 0000 HLT /TEST HALT
0027 0011 CLR

/SKP TEST
0030 0456 SKP
0031 0000 HLT /SKIP FAILED
0032 0456 SKP /SKIP OVER LINC
0033 6141 LINC /MAJOR RESTART FROM END OF PASS

0034 0476 SKP*20
0035 0456 SKP
0036 0000 HLT /SKP*20 FAILED
```

/SENSE SWITCH TEST CHECK SNS INSTRUCTION, I=0, I=1

0037	0440	SNS+0	
0040	0000	HLT	/SNS+0 FAILED TO DETECT SENSE SWITCH 0
0041	0460	SNS+20+0	/UNCONDITIONAL SKIP
0042	0496	SKP	
0043	0000	HLT	/SNS I+0 SKIPPED IN ERROR
0044	0441	SNS+1	
0045	0000	HLT	/SNS+1 FAILED TO DETECT SENSE SWITCH 1
0046	0461	SNS+20+1	
0047	0456	SKP	
0050	0000	HLT	/SNS I+1 SKIPPED IN ERROR
0051	0442	SNS+2	
0052	0000	HLT	/SNS+2 FAILED TO DETECT SENSE SWITCH 2
0053	0462	SNS+20+2	
0054	0456	SKP	
0055	0000	HLT	/SNS I+2 SKIPPED IN ERROR
0056	0443	SNS+3	
0057	0000	HLT	/SNS+3 FAILED TO DETECT SENSE SWITCH 3
0060	0463	SNS+20+3	
0061	0456	SKP	
0062	0000	HLT	/SNS I+3 SKIPPED IN ERROR
0063	0444	SNS+4	
0064	0000	HLT	/SNS+4 FAILED TO DETECT SENSE SWITCH 4
0065	0464	SNS+20+4	
0066	0456	SKP	
0067	0000	HLT	/SNS I+4 SKIPPED IN ERROR
0070	0445	SNS+5	
0071	0000	HLT	/SNS+5 FAILED TO DETECT SENSE SWITCH 5
0072	0465	SNS+20+5	
0073	0456	SKP	/TEST COMPLETE SKIP TO APO TEST
0074	0000	HLT	/SNS I+5 SKIPPED IN ERROR

/
/APO TEST
/

0075	0011	CLR	/SET AC=0000
0076	0451	APO	/TEST IT USING APO
0077	0000	HLT	/APO FAILED TO SKIP AC=0000
0100	0471	APO+20	
0101	0456	SKP	
0102	0000	HLT	/APO I SKIPPED IN ERROR AC=0000
0103	1020	LDA+20	
0104	4000	4000	
0105	0471	APO+20	
0106	0000	HLT	/APO I FAILED TO SKIP AC=4000
0107	0451	APO	
0110	0456	SKP	/TEST COMPLETE SKIP TO AZE TEST PART 1
0111	0000	HLT	/APO SKIPPED IN ERROR AC=4000

/
/AZE TEST PART 1 AC=0000 AND FLOAT A SINGLE 1 BIT
/

0112	0011	CLR	
0113	0450	AZE	
0114	0000	HLT	/AZE FAILED TO SKIP AC=0000
0115	0470	AZE+20	
0116	0456	SKP	
0117	0000	HLT	/AZE I SKIPPED IN ERROR AC=0000
0120	1020	LDA+20	/SET EACH BIT IN THE AC IN TURN, TESTING TO
0121	0001	0001	/SEE IF (AZE) DETECTS THE FACT THAT THE AC IS
0122	0470	AZE+20	/NON ZERO
0123	0000	HLT	/AZE I FAILED TO SKIP AC=0001
0124	0450	AZE	
0125	0456	SKP	
0126	0000	HLT	/AZE SKIPPED IN ERROR AC=0001
0127	1020	LDA+20	
0130	0002	0002	
0131	0470	AZE+20	
0132	0000	HLT	/AZE I FAILED TO SKIP AC=0002
0133	0450	AZE	
0134	0456	SKP	
0135	0000	HLT	/AZE SKIPPED IN ERROR AC=0002
0136	1020	LDA+20	
0137	0004	0004	
0140	0470	AZE+20	
0141	0000	HLT	/AZE I FAILED TO SKIP AC=0004
0142	0450	AZE	

2143	0456	SKP	
2144	0000	HLT	/AZE SKIPPED IN ERROR AC=0004
2145	1020	LDA+20	
2146	0010	0010	
2147	0470	AZE+20	
2150	0000	HLT	/AZE I FAILED TO SKIP AC=0010
2151	0450	AZE	
2152	0456	SKP	
2153	0000	HLT	/AZE SKIPPED IN ERROR AC=0010

0154	1020	LDA+20	
0155	0020	0020	
0156	0470	AZE+20	
0157	0000	HLT	/AZE I FAILED TO SKIP AC=0020
0160	0450	AZE	
0161	0456	SKP	
0162	0000	HLT	/AZE SKIPPED IN ERROR AC=0020
0163	1020	LDA+20	
0164	0040	0040	
0165	0470	AZE+20	
0166	0000	HLT	/AZE I FAILED TO SKIP AC=0040
0167	0450	AZE	
0170	0456	SKP	
0171	0000	HLT	/AZE SKIPPED IN ERROR AC=0040
0172	1020	LDA+20	
0173	0100	0100	
0174	0470	AZE+20	
0175	0000	HLT	/AZE I FAILED TO SKIP AC=0100
0176	0450	AZE	
0177	0456	SKP	
0200	0000	HLT	/AZE SKIPPED IN ERROR AC=0100
0201	1020	LDA+20	
0202	0200	0200	
0203	0470	AZE+20	
0204	0000	HLT	/AZE I FAILED TO SKIP AC=0200
0205	0450	AZE	
0206	0456	SKP	
0207	0000	HLT	/AZE SKIPPED IN ERROR AC=0200
0210	1020	LDA+20	
0211	0400	0400	
0212	0470	AZE+20	
0213	0000	HLT	/AZE I FAILED TO SKIP AC=0400
0214	0450	AZE	
0215	0456	SKP	
0216	0000	HLT	/AZE SKIPPED IN ERROR AC=0400
0217	1020	LDA+20	
0220	1000	1000	
0221	0470	AZE+20	
0222	0000	HLT	/AZE I FAILED TO SKIP AC=1000
0223	0450	AZE	
0224	0456	SKP	
0225	0000	HLT	/AZE SKIPPED IN ERROR AC=1000

0226	1020	LDA+20	
0227	2000	2000	
0230	0470	AZE+20	
0231	0000	HLT	/AZE I FAILED TO SKIP AC=2000
0232	0450	AZE	
0233	0456	SKP	
0234	0000	HLT	/AZE SKIPPED IN ERROR AC=2000
0235	1020	LDA+20	
0236	4000	4000	
0237	0470	AZE+20	
0240	0000	HLT	/AZE I FAILED TO SKIP AC=4000
0241	0450	AZE	
0242	0456	SKP	/TEST COMPLETE SKIP TO PART 2
0243	0000	HLT	/AZE SKIPPED IN ERROR AC=4000
/AZE TEST PART 2 AC=7777 AND FLOAT A SINGLE 0 BIT			
0244	1020	LDA+20	
0245	7777	7777	/SET AC=7777 AND FLOAT A SINGLE 0 BIT THRU IT
0246	0450	AZE	/TO DETERMINE IF AC DETECTS THE FACT THAT THE AC
0247	0000	HLT	/IS NON ZERO
			/AZE FAILED TO SKIP AC=7777
0250	0470	AZE+20	
0251	0456	SKP	
0252	0000	HLT	/AZE I SKIPPED IN ERROR AC=7777
0253	1020	LDA+20	
0254	7776	7776	
0255	0470	AZE+20	
0256	0000	HLT	/AZE I FAILED TO SKIP AC=7776
0257	0450	AZE	
0260	0456	SKP	
0261	0000	HLT	/AZE SKIPPED IN ERROR AC=7776
0262	1020	LDA+20	
0263	7775	7775	
0264	0470	AZE+20	
0265	0000	HLT	/AZE I FAILED TO SKIP C=7775
0266	0450	AZE	
0267	0456	SKP	
0270	0000	HLT	/AZE SKIPPED IN ERROR AC=7775
0271	1020	LDA+20	
0272	7773	7773	
0273	0470	AZE+20	
0274	0000	HLT	/AZE I FAILED TO SKIP AC=7773

0275	0450	AZE	
0276	0456	SKP	
0277	0000	HLT	/AZE SKIPPED IN ERROR AC=7773
0300	1020	LDA+20	
0301	7767	7767	
0302	0470	AZE+20	
0303	0000	HLT	/AZE I FAILED TO SKIP AC=7767
0304	0450	AZE	
0305	0456	SKP	
0306	0000	HLT	/AZE SKIPPED IN ERROR AC=7767
0307	1020	LDA+20	
0310	7757	7757	
0311	0470	AZE+20	
0312	0000	HLT	/AZE I FAILED TO SKIP AC=7757
0313	0450	AZE	
0314	0456	SKP	
0315	0000	HLT	/AZE SKIPPED IN ERROR AC=7757
0316	1020	LDA+20	
0317	7737	7737	
0320	0470	AZE+20	
0321	0000	HLT	/AZE I FAILED TO SKIP AC=7737
0322	0450	AZE	
0323	0456	SKP	
0324	0000	HLT	/AZE SKIPPED IN ERROR AC=7737
0325	1020	LDA+20	
0326	7677	7677	
0327	0470	AZE+20	
0330	0000	HLT	/AZE I FAILED TO SKIP AC=7767
0331	0450	AZE	
0332	0456	SKP	
0333	0000	HLT	/AZE SKIPPED IN ERROR AC=7677
0334	1020	LDA+20	
0335	7577	7577	
0336	0470	AZE+20	
0337	0000	HLT	/AZE I FAILED TO SKIP AC=7577
0340	0450	AZE	
0341	0456	SKP	
0342	0000	HLT	/AZE SKIPPED IN ERROR AC=7577
0343	1020	LDA+20	
0344	7377	7377	
0345	0470	AZE+20	
0346	0000	HLT	/AZE I FAILED TO SKIP AC=7377

0347	0450	AZE	
0350	0456	SKP	
0351	0000	HLT	/AZE SKIPPED IN ERROR AC=7377
0352	1020	LDA+20	
0353	6777	6777	
0354	0470	AZE+20	
0355	0000	HLT	/AZE I FAILED TO SKIP AC=6777
0356	0450	AZE	
0357	0456	SKP	
0360	0000	HLT	/AZE SKIPPED IN ERROR AC=6777
0361	1020	LDA+20	
0362	5777	5777	
0363	0470	AZE+20	
0364	0000	HLT	/AZE I FAILED TO SKIP AC=5777
0365	0450	AZE	
0366	0456	SKP	
0367	0000	HLT	/AZE SKIPPED IN ERROR AC=5777
0370	1020	LDA+20	
0371	3777	3777	
0372	0470	AZE+20	
0373	0000	HLT	/AZE I FAILED TO SKIP AC=3777
0374	0450	AZE	
0375	0456	SKP	
0376	0000	HLT	/AZE SKIPPED IN ERROR AC=3777

/AZE TESTS WITH L=1 SEE IF LINK AFFECTS THE AZE COMMAND

```

0377 0002      PDP      /ROUTINE IN 8 MODE TO SET LINK
0400 7320      CLL CML CLA /AC=0000, L=1
0401 6141      LINC

0402 1020      LDA+20
0403 7777      7777
0404 0450      AZE
0405 0000      HLT      /AZE FAILED TO SKIP AC=7777 L=1

0406 0470      AZE+20
0407 0456      SKP
0410 0000      HLT      /AZE I SKIPPED IN ERROR AC=7777 L=1

0411 1020      LDA+20
0412 0000      0000
0413 0450      AZE
0414 0000      HLT      /AZE FAILED TO SKIP AC=0000 L=1

0415 0470      AZE+20
0416 0456      SKP
0417 0000      HLT      /TEST COMPLETE SKIP TO LZE TEST
                        /AZE I SKIPPED IN ERROR AC=0000 L=1

```

/LZE TEST L=0 I=0, I=1

```

0420 0011      CLR      /CLEAR AC, L, MQ
0421 0452      LZE      /SKIP IF LINK = 0
0422 0000      HLT      /LZE FAILED TO SKIP AC=0000 L=0

0423 0472      LZE+20
0424 0456      SKP
0425 0000      HLT      /LZE I SKIPPED IN ERROR AC=3777 L=0

0426 0002      PDP      /ROUTINE IN 8 MODE TO SET LINK
0427 7120      CLL CML
0430 6141      LINC

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/LZE TEST L=1, I=0, I=1

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0431 0472      LZE+20
0432 0000      HLT      /LZE I FAILED TO SKIP AC=3777 L=1

0433 0452      LZE
0434 0456      SKP
0435 0000      HLT      /TEST COMPLETE SKIP TO SAE TEST
                        /LZE SKIPPED IN ERROR AC=3777 L=1

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/SAE TEST PART 1 AC=0000 L=1 MEM=0001 FLOAT A SINGLE ONE BIT THRU MEM

```

0436 1020      LDA+20      /SET EACH AC BIT IN TURN TO A ONE COMPARE
0437 0000      0000      /II WITH AN ALL ZERO IN THE SAE INSTRUCTION
0440 1460      SAE+20
0441 0000      0000

```

0442	0000	HLT	/SAE FAILED TO SKIP MEM=0000 AC=0000 L=1
0443	1460	SAE+20	/LEAVE AC=0000 AND FLOAT A SINGLE 1 BIT THRU MEM
0444	0001	0001	
0445	0456	SKP	
0446	0000	HLT	/SAE SKIPPED IN ERROR MEM=0001 AC=0000
0447	1460	SAE+20	
0450	0002	0002	
0451	0456	SKP	
0452	0000	HLT	/SAE SKIPPED IN ERROR MEM=0002 AC=0000
0453	1460	SAE+20	
0454	0004	0004	
0455	0456	SKP	
0456	0000	HLT	/SAE SKIPPED IN ERROR MEM=0004 AC=0000
0457	1460	SAE+20	
0460	0010	0010	
0461	0456	SKP	
0462	0000	HLT	/SAE SKIPPED IN ERROR MEM=0010 AC=0000
0463	1460	SAE+20	
0464	0020	0020	
0465	0456	SKP	
0466	0000	HLT	/SAE SKIPPED IN ERROR MEM=0020 AC=0000
0467	1460	SAE+20	
0470	0040	0040	
0471	0456	SKP	
0472	0000	HLT	/SAE SKIPPED IN ERROR MEM=0040 AC=0000

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0473 1460      SAE+20
0474 0100      0100
0475 0406      SKP
0476 0000      HLT                /SAE SKIPPED IN ERROR MEM=0100 AC=0000

0477 1460      SAE+20
0500 0200      0200
0501 0456      SKP
0502 0000      HLT                /SAE SKIPPED IN ERROR MEM=0200 AC=0000

0503 1460      SAE+20
0504 0400      0400
0505 0456      SKP
0506 0000      HLT                /SAE SKIPPED IN ERROR MEM=0400 AC=0000

0507 1460      SAE+20
0510 1000      1000
0511 0456      SKP
0512 0000      HLT                /SAE SKIPPED IN ERROR MEM=1000 AC=0000

0513 1460      SAE+20
0514 2000      2000
0515 0456      SKP
0516 0000      HLT                /SAE SKIPPED IN ERROR MEM=2000 AC=0000

0517 1460      SAE+20
0520 4000      4000
0521 0456      SKP
0522 0000      HLT                /TEST COMPLETE SKIP TO SAE PART 2
                                   /SAE SKIPPED IN ERROR MEM=4000 AC=0000

/SAE TEST PART 2 MEM=0000 AC=0001 FLOAT A SINGLE ONE BIT THRU AC
/

0523 1020      LDA+20
0524 0001      0001
0525 1460      SAE+20
0526 0000      0000
0527 0456      SKP
0530 0000      HLT                /SAE SKIPPED IN ERROR MEM=0000 AC=0001

0531 1020      LDA+20
0532 0002      0002
0533 1460      SAE+20
0534 0000      0000
0535 0456      SKP
0536 0000      HLT                /SAE SKIPPED IN ERROR MEM=0000 AC=0001

0537 1020      LDA+20
0540 0004      0004
0541 1460      SAE+20
0542 0000      0000
0543 0456      SKP
0544 0000      HLT                /SAE SKIPPED IN ERROR MEM=0000 AC=0002

0545 1020      LDA+20

```

0546	0010	0010
0547	1460	SAE+20
0550	0000	0000
0551	0456	SKP
0552	0000	HLT

/SAE SKIPPED IN ERROR MEM=0000 AC=0010

0553	1020	LDA+20	
0554	0020	0020	
0555	1460	SAE+20	
0556	0000	0000	
0557	0456	SKP	
0560	0000	HLT	/SAE SKIPPED IN ERROR MEM=0000 AC=0010
0561	1020	LDA+20	
0562	0040	0040	
0563	1460	SAE+20	
0564	0000	0000	
0565	0456	SKP	
0566	0000	HLT	/SAE SKIPPED IN ERROR MEM=0000 AC=0040
0567	1020	LDA+20	
0570	0100	0100	
0571	1460	SAE+20	
0572	0000	0000	
0573	0456	SKP	
0574	0000	HLT	/SAE SKIPPED IN ERROR MEM=0000 AC=0100
0575	1020	LDA+20	
0576	0200	0200	
0577	1460	SAE+20	
0600	0000	0000	
0601	0456	SKP	
0602	0000	HLT	/SAE SKIPPED IN ERROR MEM=0000 AC=0200
0603	1020	LDA+20	
0604	0400	0400	
0605	1460	SAE+20	
0606	0000	0000	
0607	0456	SKP	
0610	0000	HLT	/SAE SKIPPED IN ERROR MEM=0000 AC=0400
0611	1020	LDA+20	
0612	1000	1000	
0613	1460	SAE+20	
0614	0000	0000	
0615	0456	SKP	
0616	0000	HLT	/SAE SKIPPED IN ERROR MEM=0000 AC=1000
0617	1020	LDA+20	
0620	2000	2000	
0621	1460	SAE+20	
0622	0000	0000	
0623	0456	SKP	
0624	0000	HLT	/SAE SKIPPED IN ERROR MEM=0000 AC=2000
0625	1020	LDA+20	
0626	4000	4000	
0627	1460	SAE+20	
0630	0000	0000	

0631 0496 SKP
0632 0000 HLT

/TEST COMPLETE SKIP TO SAE TEST PART 3
/SAE SKIPPED IN ERROR MEM=0000 AC=4000

/SAE TEST PART 3 MEM=7777 AC=7776 FLOAT A SINGLE 0 BIT THRU AC

0633	1020	LDA+20	/FLOAT A SINGLE 0 THRU THE AC COMPARE THIS
0634	7776	7776	/AGAINST 7777 IN THE SAE OPERAND,
0635	1460	SAE+20	
0636	7777	7777	
0637	0456	SKP	
0640	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=7776
0641	1020	LDA+20	
0642	7775	7775	
0643	1460	SAE+20	
0644	7777	7777	
0645	0456	SKP	
0646	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=7775
0647	1020	LDA+20	
0650	7773	7773	
0651	1460	SAE+20	
0652	7777	7777	
0653	0456	SKP	
0654	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=7773
0655	1020	LDA+20	
0656	7767	7767	
0657	1460	SAE+20	
0660	7777	7777	
0661	0456	SKP	
0662	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=7767
0663	1020	LDA+20	
0664	7757	7757	
0665	1460	SAE+20	
0666	7777	7777	
0667	0456	SKP	
0670	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=7757
0671	1020	LDA+20	
0672	7737	7737	
0673	1460	SAE+20	
0674	7777	7777	
0675	0456	SKP	
0676	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=7737
0677	1020	LDA+20	
0700	7677	7677	
0701	1460	SAE+20	
0702	7777	7777	
0703	0456	SKP	
0704	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=7677

0705	1020	LDA+20	
0706	7577	7577	
0707	1460	SAE+20	
0710	7777	7777	
0711	0456	SKP	
0712	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=7577
0713	1020	LDA+20	
0714	7377	7377	
0715	1460	SAE+20	
0716	7777	7777	
0717	0456	SKP	
0720	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=7377
0721	1020	LDA+20	
0722	6777	6777	
0723	1460	SAE+20	
0724	7777	7777	
0725	0456	SKP	
0726	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=6777
0727	1020	LDA+20	
0730	5777	5777	
0731	1460	SAE+20	
0732	7777	7777	
0733	0456	SKP	
0734	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=5777
0735	1020	LDA+20	
0736	3777	3777	
0737	1460	SAE+20	
0740	7777	7777	
0741	0456	SKP	/TEST COMPLETE SKIP TO SAE TEST PART 4
0742	0000	HLT	/SAE SKIPPED IN ERROR MEM=7777 AC=3777
/SAE TEST PART 4 MEM=7776 AC=7777 L=1 FLOAT A SINGLE 0 THRU MEM			
0743	1020	LDA+20	/SET THE AC TO 7777 AND FLOAT A SINGLE
0744	7777	7777	/ZERO THRU THE SAE OPERAND
0745	1460	SAE+20	
0746	7776	7776	
0747	0456	SKP	
0750	0000	HLT	/SAE SKIPPED IN ERROR MEM=7776 AC=7777
0751	1460	SAE+20	
0752	7775	7775	
0753	0456	SKP	
0754	0000	HLT	/SAE SKIPPED IN ERROR MEM=7775 AC=7777
0755	1460	SAE+20	
0756	7773	7773	
0757	0456	SKP	
0760	0000	HLT	/SAE SKIPPED IN ERROR MEM=7773 AC=7777

0761	1400	SAE+20	
0762	7767	7767	
0763	0456	SKP	
0764	0000	HLT	/SAE SKIPPED IN ERROR MEM=7767 AC7777
0765	1400	SAE+20	
0766	7757	7757	
0767	0456	SKP	
0770	0000	HLT	/SAE SKIPPED IN ERROR MEM=7757 AC=7777
0771	1400	SAE+20	
0772	7737	7737	
0773	0456	SKP	
0774	0000	HLT	/SAE SKIPPED IN ERROR MEM=7737 AC=7777

0775	1460	SAE+20	
0776	7677	7677	
0777	0456	SKP	
1000	0000	HLT	/SAE SKIPPED IN ERROR MEM=7677 AC=7777
1001	1460	SAE+20	
1002	7577	7577	
1003	0456	SKP	
1004	0000	HLT	/SAE SKIPPED IN ERROR MEM=7577 AC=7777
1005	1460	SAE+20	
1006	7377	7377	
1007	0456	SKP	
1010	0000	HLT	/SAE SKIPPED IN ERROR MEM=7377 AC=7777
1011	1460	SAE+20	
1012	6777	6777	
1013	0456	SKP	
1014	0000	HLT	/SAE SKIPPED IN ERROR MEM=6777 AC=7777
1015	1460	SAE+20	
1016	5777	5777	
1017	0456	SKP	
1020	0000	HLT	/SAE SKIPPED IN ERROR MEM=5777 AA=7777
1021	1460	SAE+20	
1022	3777	3777	
1023	0456	SKP	
1024	0000	HLT	/SAE SKIPPED IN ERROR MEM=3777 AC=7777

/SAE SOME COMBINATIONS OF EQUALITY

1025	1020	LDA+20	/TEST SAE USING NOISY OPERANDS
1026	5252	5252	
1027	1460	SAE+20	
1030	5252	5252	
1031	0000	HLT	/SAE FAILED TO SKIP MEM=5252 AC=5252
1032	1020	LDA+20	
1033	2525	2525	
1034	1460	SAE+20	
1035	2525	2525	
1036	0000	HLT	/SAE FAILED TO SKIP MEM=2525 AC=2525
1037	1020	LDA+20	
1040	7777	7777	
1041	1460	SAE+20	/END OF SAE TESTS SKIP TO ROL TEST PART 1
1042	7777	7777	
1043	0000	HLT	/SAE FAILED TO SKIP MEM=7777 AC=7777

```

/
/ROL TEST PART 1 FLOATS A SINGLE ONE THRU THE AC, THE LINK BIT IS SET TO ONE
/LATER ON WE WILL TEST TO BE SURE WE DIDN'T DISTURB THE LINK
1044 0002      PDP
1045 7120      CLL CML      /SET LINK
1046 6141      LINC
1047 1020      LDA+20      /SET A SINGLE BIT IN THE AC, ROL ONE PLACE
1050 0001      0001      /AND TEST THE RESULT
1051 0240      ROL
1052 1460      SAE+20
1053 0001      0001
1054 0000      HLT      /ROL 0 CHANGED AC AC=0001 L=0

1055 1020      LDA+20
1056 0001      0001
1057 0241      ROL+1
1060 1460      SAE+20
1061 0002      0002
1062 0000      HLT      /ROL+1 FAILED AC11 TO AC10 AC=0002

1063 1020      LDA+20
1064 0002      0002
1065 0241      ROL+1
1066 1460      SAE+20
1067 0004      0004
1070 0000      HLT      /ROL+1 FAILED AC10 TO AC9 AC=0004

1071 1020      LDA+20
1072 0004      0004
1073 0241      ROL+1
1074 1460      SAE+20
1075 0010      0010
1076 0000      HLT      /ROL+1 FAILED AC9 TO AC8 AC=0010

1077 1020      LDA+20
1100 0010      0010
1101 0241      ROL+1
1102 1460      SAE+20
1103 0020      0020
1104 0000      HLT      /ROL+1 FAILED AC8 TO AC7 AC=0020

1105 1020      LDA+20
1106 0020      0020
1107 0241      ROL+1
1110 1460      SAE+20
1111 0040      0040
1112 0000      HLT      /ROL+1 FAILED AC7 TO AC6 AC=0040

1113 1020      LDA+20
1114 0040      0040
1115 0241      ROL+1
1116 1460      SAE+20
1117 0100      0100
1120 0000      HLT      /ROL+1 FAILED AC6 TO AC5 AC=0100

```

1121	1020	LDA+20	
1122	0100	0100	
1123	0241	ROL+1	
1124	1460	SAE+20	
1125	0200	0200	
1126	0000	HLT	/ROL+1 FAILED AC5 TO AC4 AC=0200
1127	1020	LDA+20	
1130	0200	0200	
1131	0241	ROL+1	
1132	1460	SAE+20	
1133	0400	0400	
1134	0000	HLT	/ROL+1 FAILED 0C4 TO AC3 AC=0400
1135	1020	LDA+20	
1136	0400	0400	
1137	0241	ROL+1	
1140	1460	SAE+20	
1141	1000	1000	
1142	0000	HLT	/ROL+1 FAILED AC3 TO AC3 AC=1000
1143	1020	LDA+20	
1144	1000	1000	
1145	0241	ROL+1	
1146	1460	SAE+20	
1147	2000	2000	
1150	0000	HLT	/ROL+1 FAILED AC2 TO AC1 AC=2000
1151	1020	LDA+20	
1152	2000	2000	
1153	0241	ROL+1	
1154	1460	SAE+20	
1155	4000	4000	
1156	0000	HLT	/ROL+1 FAILED AC1 TO AC0 AC=4000
1157	1020	LDA+20	
1160	4000	4000	
1161	0241	ROL+1	
1162	1460	SAE+20	
1163	0001	0001	
1164	0000	HLT	/ROL+1 FAILED AC0 TO AC11 AC=0001
1165	0472	LZE+20	/TEST COMPLETE SKIP TO ROL TEST PART 2
1166	0000	HLT	/LINK CLEARED BY ROL+1 IN ERROR AC=0001

/ROL TEST PART 2 COUNTER TEST USING NOISY NUMBER IN THE AC

```
1167 1020 LDA+20 /LOAD A TEST NUMBER INTO THE AC
1170 5252 5252 /PERFORM ROL *2,3,4,..,17 AND TEST THE RESULT
1171 0242 ROL*2
1172 1460 SAE+20
1173 5252 5252
1174 0000 HLT /ROL*2 FAILED AC=5252

1175 1020 LDA+20
1176 2525 2525
1177 0243 ROL*3
1200 1460 SAE+20
1201 5252 5252
1202 0000 HLT /ROL*3 FAILED AC=5252

1203 1020 LDA+20
1204 0077 0077
1205 0244 ROL*4
1206 1460 SAE+20
1207 1760 1760
1210 0000 HLT /ROL*4 FAILED AC=1760

1211 1020 LDA+20
1212 7700 7700
1213 0245 ROL*5
1214 1460 SAE+20
1215 4037 4037
1216 0000 HLT /ROL*5 FAILED AC=4037

1217 1020 LDA+20
1220 5200 5200
1221 0246 ROL*6
1222 1460 SAE+20
1223 0052 0052
1224 0000 HLT /ROL*6 FAILED AC=0052

1225 1020 LDA+20
1226 2500 2500
1227 0247 ROL*7
1230 1460 SAE+20
1231 0052 0052
1232 0000 HLT /ROL*7 FAILED AC=0052

1233 1020 LDA+20
1234 0025 0025
1235 0250 ROL*10
1236 1460 SAE+20
1237 2401 2401
1240 0000 HLT /ROL*10 FAILED AC=2401
```

1241	1020	LDA+20	
1242	0052	0052	
1243	0251	ROL+11	
1244	1460	SAE+20	
1245	2005	2005	
1246	0000	HLT	/ROL+11 FAILED AC=2005
1247	1020	LDA+20	
1250	0770	0770	
1251	0252	ROL+12	
1252	1460	SAE+20	
1253	0176	0176	
1254	0000	HLT	/ROL+12 FAILED AC=0176
1255	1020	LDA+20	
1256	0707	0707	
1257	0253	ROL+13	
1260	1460	SAE+20	
1261	4343	4343	
1262	0000	HLT	/ROL+13 FAILED AC=4343
1263	1020	LDA+20	
1264	7070	7070	
1265	0254	ROL+14	
1266	1460	SAE+20	
1267	7070	7070	
1270	0000	HLT	/ROL+14 FAILED AC=7070
1271	1020	LDA+20	
1272	7007	7007	
1273	0255	ROL+15	
1274	1460	SAE+20	
1275	6017	6017	
1276	0000	HLT	/ROL+15 FAILED AC=6017
1277	1020	LDA+20	
1300	0520	0520	
1301	0256	ROL+16	
1302	1460	SAE+20	
1303	2500	2500	
1304	0000	HLT	/ROL+16 FAILED AC=2500
1305	1020	LDA+20	
1306	0250	0250	
1307	0257	ROL+17	
1310	1460	SAE+20	
1311	2500	2500	
1312	0000	HLT	/ROL+17 FAILED AC=1240
1313	0472	LZE+20	/TEST COMPLETE SKIP TO ROL TEST 3
1314	0000	HLT	/LINK CLEARED BY ROL+2 THRU 17 IN ERROR AC=2500

/ROL I TEST PART 3

1315	0002	PDP	/ROUTINE IN 8 MODE TO SET LINK
1316	7120	CLL CML	
1317	6141	LINC	
1320	1020	LDA+20	/DOES SETTING THE I BIT EFFECT THE LINK
1321	2525	2525	
1322	0260	ROL+20	
1323	1460	SAE+20	
1324	2525	2525	
1325	0000	HLT	/ROL I=0 FAILED AC=2525
1326	0472	LZE+20	
1327	0000	HLT	/ROL I=0 FAILED L=1
1330	1020	LDA+20	
1331	2525	2525	
1332	0261	ROL+20+1	
1333	1460	SAE+20	
1334	5253	5253	
1335	0000	HLT	/ROL I+1 FAILED AC=5253 /IF AC=5252 LINK TO AC11 FAILED
1336	0452	LZE	
1337	0000	HLT	/ROL I+1 FAILED L=0
1340	0011	CLR	/CLEAR LINK AND AC
1341	1020	LDA+20	
1342	5252	5252	
1343	0261	ROL+20+1	
1344	1460	SAE+20	
1345	2524	2524	
1346	0000	HLT	/ROL I+1 FAILED AC=2524
1347	0472	LZE+20	
1350	0000	HLT	/ROL I+1 FAILED AC=00 TO LINK L=1
1351	0011	CLR	
1352	1020	LDA+20	
1353	5252	5252	
1354	0277	ROL+20+17	
1355	1460	SAE+20	
1356	5251	5251	
1357	0000	HLT	/ROL I+17 FAILED AC=5251
1360	0452	LZE	/TEST COMPLETE SKIP TO ROL TEST 4
1361	0000	HLT	/ROL I+17 FAILED L=0

```

/
/ROR TEST 4 FLOATS A SINGLE ONE THRU THE AC THE LINK BIT IS SET TO A ONE
/LATER ON WELL WILL TEST TO BE SURE WE DIDN'T DISTURB THE LINK
1362 0002      PUP          /SET LINK IN 8 MODE
1363 7120      CLL CML
1364 6141      LINC
1365 1020      LDA+20
1366 4000      4000
1367 0300      ROR
1370 1460      SAE+20
1371 4000      4000
1372 0000      HLT          /ROR 0 FAILED AC0 TO AC0 AC=4000
1373 1020      LDA+20
1374 4000      4000
1375 0301      ROR+1
1376 1460      SAE+20
1377 2000      2000
1400 0000      HLT          /ROR +1 FAILED AC0 TO AC1 AC=2000
1401 1020      LDA+20
1402 2000      2000
1403 0301      ROR+1
1404 1460      SAE+20
1405 1000      1000
1406 0000      HLT          /ROR +1 FAILED AC1 TO AC2 AC=1000
1407 1020      LDA+20
1410 1000      1000
1411 0301      ROR+1
1412 1460      SAE+20
1413 0400      0400
1414 0000      HLT          /ROR +1 FAILED AC2 TO AC3 AC=0400
1415 1020      LDA+20
1416 0400      0400
1417 0301      ROR+1
1420 1460      SAE+20
1421 0200      0200
1422 0000      HLT          /ROR+1 FAILED AC3 TO AC4 AC=0200
1423 1020      LDA+20
1424 0200      0200
1425 0301      ROR+1
1426 1460      SAE+20
1427 0100      0100
1430 0000      HLT          /ROR+1 FAILED AC4 TO AC5 AC=0100

```

1431	1020	LDA+20	
1432	0100	0100	
1433	0301	ROR+1	
1434	1460	SAE+20	
1435	0040	0040	
1436	0000	HLT	/ROR+1 FAILED AC5 TO AC6 AC=0040
1437	1020	LDA+20	
1440	0040	0040	
1441	0301	ROR+1	
1442	1460	SAE+20	
1443	0020	0020	
1444	0000	HLT	/ROR+1 FAILED AC6 TO AC7 AC=0020
1445	1020	LDA+20	
1446	0020	0020	
1447	0301	ROR+1	
1450	1460	SAE+20	
1451	0010	0010	
1452	0000	HLT	/ROR+1 FAILED AC7 TO AC8 AC=0010
1453	1020	LDA+20	
1454	0010	0010	
1455	0301	ROR+1	
1456	1460	SAE+20	
1457	0004	0004	
1460	0000	HLT	/ROR+1 FAILED AC8 TO AC9 AC=0004
1461	1020	LDA+20	
1462	0004	0004	
1463	0301	ROR+1	
1464	1460	SAE+20	
1465	0002	0002	
1466	0000	HLT	/ROR+1 FAILED AC9 TO AC10 AC=0002
1467	1020	LDA+20	
1470	0002	0002	
1471	0301	ROR+1	
1472	1460	SAE+20	
1473	0001	0001	
1474	0000	HLT	/ROR+1 FAILED AC10 TO AC11 AC=0001
1475	1020	LDA+20	
1476	0001	0001	
1477	0301	ROR+1	
1500	1460	SAE+20	
1501	4000	4000	
1502	0000	HLT	/ROR+1 FAILED AC11 TO AC0 AC=4000
1503	0472	LZE+20	/TEST COMPLETE SKIP RD ROR TEST 5
1504	0000	HLT	/ROR+1 CLEARED LINK IN ERROR AC=4000

/
/ROR TEST 5 COUNTER TEST WITH NOISY NUMBERS IN THE AC
/

1505	1020	LDA+20	
1506	5252	5252	
1507	0302	ROR+2	
1510	1460	SAE+20	
1511	5252	5252	
1512	0000	HLT	/ROR+2 FAILED AC=5252
1513	1020	LDA+20	
1514	2525	2525	
1515	0303	ROR+3	
1516	1460	SAE+20	
1517	5252	5252	
1520	0000	HLT	/ROR+3 FAILED AC=5252
1521	1020	LDA+20	
1522	0077	0077	
1523	0304	ROR+4	
1524	1460	SAE+20	
1525	7403	7403	
1526	0000	HLT	/ROR+4 FAILED AC=7403
1527	1020	LDA+20	
1530	7700	7700	
1531	0305	ROR+5	
1532	1460	SAE+20	
1533	0176	0176	
1534	0000	HLT	/ROR+5 FAILED AC=0176
1535	1020	LDA+20	
1536	5200	5200	
1537	0306	ROR+6	
1540	1460	SAE+20	
1541	0052	0052	
1542	0000	HLT	/ROR+6 FAILED AC=0052
1543	1020	LDA+20	
1544	2500	2500	
1545	0307	ROR+7	
1546	1460	SAE+20	
1547	4012	4012	
1550	0000	HLT	/ROR+7 FAILED AC=4012

1551	1020	LDA+20	
1552	0025	0025	
1553	0310	ROR+10	
1554	1460	SAE+20	
1555	0520	0520	
1556	0000	HLT	/ROR+10 FAILED AC#0520
1557	1020	LDA+20	
1560	0052	0052	
1561	0311	ROR+11	
1562	1460	SAE+20	
1563	0520	0520	
1564	0000	HLT	/ROR+11 FAILED AC#0520
1565	1020	LDA+20	
1566	0770	0770	
1567	0312	ROR+12	
1570	1460	SAE+20	
1571	3740	3740	
1572	0000	HLT	/ROR+12 FAILED AC#0374
1573	1020	LDA+20	
1574	0707	0707	
1575	0313	ROR+13	
1576	1460	SAE+20	
1577	1616	1616	
1600	0000	HLT	/ROR+13 FAILED AC#1616
1601	1020	LDA+20	
1602	7070	7070	
1603	0314	ROR+14	
1604	1460	SAE+20	
1605	7070	7070	
1606	0000	HLT	/ROR+14 FAILED AC#7070
1607	1020	LDA+20	
1610	7007	7007	
1611	0315	ROR+15	
1612	1460	SAE+20	
1613	7403	7403	
1614	0000	HLT	/ROR+15 FAILED AC#7403
1615	1020	LDA+20	
1616	0520	0520	
1617	0316	ROR+16	
1620	1460	SAE+20	
1621	0124	0124	
1622	0000	HLT	/ROR+16 FAILED AC#0124
1623	1020	LDA+20	
1624	0250	0250	
1625	0317	ROR+17	
1626	1460	SAE+20	
1627	0025	0025	
1632	0000	HLT	/ROR+17 FAILED AC#0025

1631 0472
1632 0000

LZE+20
HLT

/TEST COMPLETE SKIP TO ROR TEST 2
/LINK CLEARED BY ROR2 THRU 17

/ROR I TEST 2

1633	0002	PDP	/ROUTINE IN B MODE TO SET LINK
1634	7120	CLL CML	
1635	6141	LINC	
1636	1020	LDA+20	
1637	5252	5252	
1640	0320	ROR+20	
1641	1460	SAE+20	
1642	5252	5252	
1643	0000	HLT	/ROR I+0 FAILED AC=5252
1644	0472	LZE+20	
1645	0000	HLT	/ROR I+0 FAILED L=1,
1646	1020	LDA+20	
1647	5252	5252	
1650	0321	ROR+20+1	
1651	1460	SAE+20	
1652	6525	6525	
1653	0000	HLT	/ROR I+1 FAILED AC=6525
1654	0452	LZE	
1655	0000	HLT	/ROR I+1 FAILED AC=0 TO LINK L=0
1656	0011	CLR	
1657	1020	LDA+20	
1660	2525	2525	
1661	0321	ROR+20+1	
1662	1460	SAE+20	
1663	1252	1252	
1664	0000	HLT	/ROR I+1 FAILED AC=2524
1665	0472	LZE+20	
1666	0000	HLT	/ROR I+1 FAILED AC=0 TO LINK L=1
1667	0011	CLR	
1670	1020	LDA+20	
1671	2525	2525	
1672	0337	ROR+20+17	
1673	1460	SAE+20	
1674	4525	4525	
1675	0000	HLT	/ROR I+17 FAILED AC=2525
1676	0452	LZE	/TEST COMPLETE, SKIP TO ROR TEST 3
1677	0000	HLT	/ROR I+17 FAILED L=0

/ROR TEST 3 AC DATA TO THE MQ TEST (QAC) TEST

1700	0011	CLR	/CLEAR AC, L, MQ
1701	1020	LDA+20	/=9S
1702	0001	0001	/ROR INTO MQ REGISTER,
1703	0301	ROR+1	/QAC IT INTO AC,
1704	0005	QAC	/AND TEST IT
1705	1460	SAE+20	
1706	2000	2000	
1707	0000	HLT	/MQ DATA FAILED AC=2000 MQ=4000
1710	0011	CLR	
1711	1020	LDA+20	
1712	0001	0001	
1713	0302	ROR+2	
1714	0005	QAC	
1715	1460	SAE+20	
1716	1000	1000	
1717	0000	HLT	/MQ DATA FAILED AC=1000 MQ=2000
1720	0011	CLR	
1721	1020	LDA+20	
1722	0001	0001	
1723	0303	ROR+3	
1724	0005	QAC	
1725	1460	SAE+20	
1726	0400	0400	
1727	0000	HLT	/MQ DATA FAILED AC=0400 MQ=0000
1730	0011	CLR	
1731	1020	LDA+20	
1732	0001	0001	
1733	0304	ROR+4	
1734	0005	QAC	
1735	1460	SAE+20	
1736	0200	0200	
1737	0000	HLT	/MQ DATA FAILED AC=0200 MQ=0400
1740	0011	CLR	
1741	1020	LDA+20	
1742	0001	0001	
1743	0305	ROR+5	
1744	0005	QAC	
1745	1460	SAE+20	
1746	0100	0100	
1747	0000	HLT	/MQ DATA FAILED AC=0100 MQ=0200
1750	0011	CLR	
1751	1020	LDA+20	
1752	0001	0001	
1753	0306	ROR+6	
1754	0005	QAC	

1755	1460	SAE+20	/TEST PARTIALLY COMPLETE, CHANGE IF
1756	0040	0040	
1757	0000	HLT	/MQ DATA FAILED AQ=0040 MQ=0010

/SUBROUTINE TO CHANGE INSTRUCTION FIELDS:
/GO TO P MODE, JUMP INDIRECT INTO NEXT
/2K OF MEMORY, AND SWITCH BACK TO L MODE,
/THE MA IS LOADED INTO THE IB, THEN THE
/IB IS TRANSFERRED TO TO THE IF
/IF THIS FAILS, WE SHOULD LAND @ 0002

1760	0002	PDP	/GO TO 8 MODE
1761	5762	5600 ,+1	/JMP I ,+1
1762	2001	2001	/NEW FIELD
	2001	*2001	
2001	6141	LINC	
2002	0011	CLR	/CONTINUE FOR TEST 3
2003	0456	SKP	
2004	0000	HLT	/ERROR 6141 AT 3767 FAILED
2005	1020	LDA+20	
2006	0001	0001	
2007	0307	ROR+7	
2010	0005	QAC	
2011	1460	SAE+20	
2012	0020	0020	
2013	0000	HLT	/MQ DATA FAILED AC=0020 MQ=0040
2014	0011	CLR	
2015	1020	LDA+20	
2016	0001	0001	
2017	0310	ROR+10	
2020	0005	QAC	
2021	1460	SAE+20	
2022	0010	0010	
2023	0000	HLT	/MQ DATA FAILED AC=0010 MQ=0020
2024	0011	CLR	
2025	1020	LDA+20	
2026	0001	0001	
2027	0311	ROR+11	
2030	0005	QAC	
2031	1460	SAE+20	
2032	0004	0004	
2033	0000	HLT	/MQ DATA FAILED AC=0004 MQ=0010
2034	0011	CLR	
2035	1020	LDA+20	
2036	0001	0001	
2037	0312	ROR+12	
2040	0005	QAC	
2041	1460	SAE+20	
2042	0002	0002	
2043	0000	HLT	/MQ DATA FAILED AC=0002 MQ=0004

```

2044 0011      CLR
2045 1020      LDA+20
2046 0001      0001
2047 0313      ROR+13
2050 0005      QAC
2051 1460      SAE+20      /TEST COMPLETE SKIP TO QLC TEST
2052 0001      0001
2053 0000      HLT          /MQ DATA FAILED AC=0001 MQ=0002

```

```

/
/QLZ TEST
/

```

```

2054 0455      QLZ
2055 0000      HLT          /MQ11 NOT ZERO ON QLC FAILED AC=0001 MQ=0002

2056 0475      QLZ+20
2057 0496      SKP
2060 0000      HLT          /QLC +20 SKIPPED IN ERROR

2061 1020      LDA+20
2062 0001      0001
2063 0314      ROR+14
2064 0475      QLZ+20
2065 0000      HLT          /QLC +20 FAILED MQ=0001

2066 0455      QLZ
2067 0496      SKP
2070 0000      HLT          /QLC FAILED MQ=0001

```

```

/ROR TEST 4
/ROR INTO MQ USING NOISY NUMBERS
/

```

```

2071 1020      LDA+20
2072 5252      5252
2073 0314      ROR+14
2074 0005      QAC
2075 1460      SAE+20
2076 2525      2525
2077 0000      HLT          /ROR+14 FAILED AC=2525 MQ=5252

2100 0455      QLZ
2101 0000      HLT          /MQ11=0

2102 1020      LDA+20
2103 2525      2525
2104 0314      ROR+14
2105 0005      QAC
2106 1460      SAE+20
2107 1252      1252
2110 0000      HLT          /ROR+14 FAILED AC=1252 MQ=2525

2111 0475      QLZ+20
2112 0000      HLT          /MQ11=1

```

2113	1020	LDA+20	
2114	0077	0077	
2115	0314	ROR+14	
2116	0005	QAC	
2117	1460	SAE+20	
2120	0037	0037	
2121	0000	HLT	/ROR+14 FAILED AC=0037 MQ=0077
2122	0475	QLZ+20	
2123	0000	HLT	/MQ11=1
2124	1020	LDA+20	
2125	7700	7700	
2126	0314	ROR+14	
2127	0005	QAC	
2130	1460	SAE+20	
2131	3740	3740	
2132	0000	HLT	/ROR+14 FAILED AC=3740 MQ=7700
2133	0455	QLZ	
2134	0000	HLT	/MQ11=0
2135	1020	LDA+20	
2136	5200	5200	
2137	0314	ROR+14	
2140	0005	QAC	
2141	1460	SAE+20	
2142	2500	2500	
2143	0000	HLT	/ROR+14 FAILED AC=2500 MQ=5200
2144	0455	QLZ	
2145	0000	HLT	/MQ11=0
2146	1020	LDA+20	
2147	2500	2500	
2150	0314	ROR+14	
2151	0005	QAC	
2152	1460	SAE+20	
2153	1240	1240	
2154	0000	HLT	/ROR+14 FAILED AC=1240 MQ=2500
2155	0455	QLZ	
2156	0000	HLT	/MQ11=0
2157	1020	LDA+20	
2160	0025	0025	
2161	0314	ROR+14	
2162	0005	QAC	
2163	1460	SAE+20	
2164	0012	0012	
2165	0000	HLT	/ROR+14 FAILED AC=0012 MQ=0025

2166	0475	QLZ+20	
2167	0000	HLT	/MQ11=1
2170	1020	LDA+20	
2171	0052	0052	
2172	0314	ROR+14	
2173	0005	QAC	
2174	1460	SAE+20	
2175	0025	0025	
2176	0000	HLT	/ROR+14 FAILED AC=0025 MQ=0052
2177	0455	QLZ	
2200	0000	HLT	/MQ11=0
2201	1020	LDA+20	
2202	0770	0770	
2203	0314	ROR+14	
2204	0005	QAC	
2205	1460	SAE+20	
2206	0374	0374	
2207	0000	HLT	/ROR+14 FAILED AC=0374 MQ=0770
2210	0455	QLZ	
2211	0000	HLT	/MQ11=0
2212	1020	LDA+20	
2213	0707	0707	
2214	0314	ROR+14	
2215	0005	QAC	
2216	1460	SAE+20	
2217	0343	0343	
2220	0000	HLT	/ROR+14 FAILED AC=0343 MQ=0707
2221	0475	QLZ+20	
2222	0000	HLT	/MQ1=1
2223	1020	LDA+20	
2224	7070	7070	
2225	0314	ROR+14	
2226	0005	QAC	
2227	1460	SAE+20	
2230	3434	3434	
2231	0000	HLT	/ROR+14 FAILED AC=3434 MQ=7070
2232	0455	QLZ	
2233	0000	HLT	/MQ11=0
2234	1020	LDA+20	
2235	7007	7007	
2236	0314	ROR+14	
2237	0005	QAC	
2240	1460	SAE+20	
2241	3403	3403	
2242	0000	HLT	/ROR+14 FAILED AC=3403 MQ=7007

2243	0475	QLZ+20	
2244	0000	HLT	/MQ11=1
2245	1020	LDA+20	
2246	0520	0520	
2247	0314	ROR+14	
2250	0005	QAC	
2251	1460	SAE+20	
2252	0250	0250	
2253	0000	HLT	/ROR+14 FAILED AC=0250 MQ=0520
2254	0455	QLZ	
2255	0000	HLT	/MQ11=0
2256	1020	LDA+20	
2257	0250	0250	
2260	0314	ROR+14	
2261	0005	QAC	
2262	1460	SAE+20	
2263	0124	0124	
2264	0000	HLT	/ROR+14 FAILED AC=0124 MQ=0250
2265	0455	QLZ	/END OF TEST SKIP RO BLC TEST 1
2266	0000	HLT	/MQ11

/BCL TEST 1, BCL WILL CLEAR ONE BIT OUT OF A FIELD OF ZEROS
/

2267	1020	LDA+20	
2270	0001	0001	
2271	1560	BCL+20	
2272	0001	0001	
2273	0450	AZE	
2274	0000	HLT	/BCL FAILED TO CLEAR AC11, AC=0000
2275	1020	LDA+20	
2276	0002	0002	
2277	1560	BCL+20	
2300	0002	0002	
2301	0450	AZE	
2302	0000	HLT	/BCL FAILED TO CLEAR AC 10, AC=0000
2303	1020	LDA+20	
2304	0004	0004	
2305	1560	BCL+20	
2306	0004	0004	
2307	0450	AZE	
2310	0000	HLT	/BCL FAILED TO CLEAR AC9, AC=0000
2311	1020	LDA+20	
2312	0010	0010	
2313	1560	BCL+20	
2314	0010	0010	
2315	0450	AZE	
2316	0000	HLT	/BCL FAILED TO CLEAR AC8, AC=0000
2317	1020	LDA+20	
2320	0020	0020	
2321	1560	BCL+20	
2322	0020	0020	
2323	0450	AZE	
2324	0000	HLT	/BCL FAILED TO CLEAR AC 7, AC=0000
2325	1020	LDA+20	
2326	0040	0040	
2327	1560	BCL+20	
2330	0040	0040	
2331	0450	AZE	
2332	0000	HLT	/BCL FAILED TO CLEAR AC 6, AC=0000
2333	1020	LDA+20	
2334	0100	0100	
2335	1560	BCL+20	
2336	0100	0100	
2337	0450	AZE	
2340	0000	HLT	/BCL FAILED TO CLEAR AC 5, AC=0000

```
2341 1020 LDA+20
2342 0200 0200
2343 1500 BCL+20
2344 0200 0200
2345 0450 AZE
2346 0000 HLT /BCL FAILED TO CLEAR AC 4, AC=0000

2347 1020 LDA+20
2350 0400 0400
2351 1500 BCL+20
2352 0400 0400
2353 0450 AZE
2354 0000 HLT /BCL FAILED TO CLEAR AC 3, AC=0000

2355 1020 LDA+20
2356 1000 1000
2357 1500 BCL+20
2360 1000 1000
2361 0450 AZE
2362 0000 HLT /BCL FAILED TO CLEAR AC 2, AC=0000

2363 1020 LDA+20
2364 2000 2000
2365 1500 BCL+20
2366 2000 2000
2367 0450 AZE
2370 0000 HLT /BCL FAILED TO CLEAR AC 1, AC=0000

2371 1020 LDA+20
2372 4000 4000
2373 1500 BCL+20
2374 4000 4000
2375 0450 AZE
2376 0000 HLT /END OF BCL TEST 1, SKIP TO BCL TEST 2
/BCL FAILED TO CLEAR AC 0, AC=0000

/
/BCL TEST 2 WILL CLEAR A SINGLE ONE OUT OF A FIELD OF ONES
/

2377 1020 LDA+20
2400 7777 7777 /SET ALL BITS AND TRY TO CLEAR
2401 1500 BCL+20 /ONE AND ONLY 1 BIT
2402 0001 0001
2403 1400 SAE+20
2404 7776 7776
2425 0000 HLT /BCL CLEARED OR SET A BIT IN ERROR, AC=7776

2426 1020 LDA+20
2427 7777 7777
2410 1500 BCL+20
2411 0002 0002
2412 1400 SAE+20
2413 7775 7775
2414 0000 HLT /BCL CLEARED OR SET A BIT IN ERROR, AC=7775

2415 1020 LDA+20
```

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2416 7777
2417 1560
7777
BCL*20

2420	0004	0004	
2421	1460	SAE+20	
2422	7773	7773	
2423	0000	HLT	/BCL_CLEARED OR SET A BIT IN ERROR, AC=7773
2424	1020	LDA+20	
2425	7777	7777	
2426	1560	BCL+20	
2427	0010	0010	
2430	1460	SAE+20	
2431	7767	7767	
2432	0000	HLT	/BCL_CLEARED OR SET A BIT IN ERROR, AC=7767
2433	1020	LDA+20	
2434	7777	7777	
2435	1560	BCL+20	
2436	0020	0020	
2437	1460	SAE+20	
2440	7757	7757	
2441	0000	HLT	/BCL_CLEARED OR SET A BIT IN ERROR, AC=7757
2442	1020	LDA+20	
2443	7777	7777	
2444	1560	BCL+20	
2445	0040	0040	
2446	1460	SAE+20	
2447	7737	7737	
2450	0000	HLT	/BCL_CLEARED OR SET A BIT IN ERROR, AC=7737
2451	1020	LDA+20	
2452	7777	7777	
2453	1560	BCL+20	
2454	0100	0100	
2455	1460	SAE+20	
2456	7677	7677	
2457	0000	HLT	/BCL_CLEARED OR SET A BIT IN ERROR, AC=7677
2460	1020	LDA+20	
2461	7777	7777	
2462	1560	BCL+20	
2463	0200	0200	
2464	1460	SAE+20	
2465	7577	7577	
2466	0000	HLT	/BCL_CLEARED OR SET A BIT IN ERROR, AC=7577
2467	1020	LDA+20	
2470	7777	7777	
2471	1560	BCL+20	
2472	0400	0400	
2473	1460	SAE+20	
2474	7377	7377	
2475	0000	HLT	/BCL_CLEARED OR SET A BIT IN ERROR, AC=7377

2476	1020	LDA+20	
2477	7777	7777	
2500	1500	BCL+20	
2501	1000	1000	
2502	1400	SAE+20	
2503	6777	6777	
2504	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=6777

2505	1020	LDA+20	
2506	7777	7777	
2507	1500	BCL+20	
2510	2000	2000	
2511	1400	SAE+20	
2512	5777	5777	
2513	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=5777

2514	1020	LDA+20	
2515	7777	7777	
2516	1500	BCL+20	
2517	4000	4000	
2520	1400	SAE+20	
2521	3777	3777	
2522	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=3777

/

/BCL WILL CLEAR ALL BITS EXCEPT FOR A SINGLE ONE

/

2523	1020	LDA+20	
2524	7777	7777	
2525	1500	BCL+20	
2526	7776	7776	
2527	1400	SAE+20	
2530	0001	0001	
2531	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=0001

2532	1020	LDA+20	
2533	7777	7777	
2534	1500	BCL+20	
2535	7775	7775	
2536	1400	SAE+20	
2537	0002	0002	
2540	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=0002

2541	1020	LDA+20	
2542	7777	7777	
2543	1500	BCL+20	
2544	7773	7773	
2545	1400	SAE+20	
2546	0004	0004	
2547	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=0004

2550	1020	LDA+20	
2551	7777	7777	
2552	1500	BCL+20	

2553	7767	7767	
2554	1460	SAE+20	
2555	0010	0010	
2556	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=0010
2557	1020	LDA+20	
2560	7777	7777	
2561	1560	BCL+20	
2562	7757	7757	
2563	1460	SAE+20	
2564	0020	0020	
2565	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=0020
2566	1020	LDA+20	
2567	7777	7777	
2570	1560	BCL+20	
2571	7737	7737	
2572	1460	SAE+20	
2573	0040	0040	
2574	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=0004
2575	1020	LDA+20	
2576	7777	7777	
2577	1560	BCL+20	
2600	7677	7677	
2601	1460	SAE+20	
2602	0100	0100	
2603	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=0100
2604	1020	LDA+20	
2605	7777	7777	
2606	1560	BCL+20	
2607	7577	7577	
2610	1460	SAE+20	
2611	0200	0200	
2612	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=0200
2613	1020	LDA+20	
2614	7777	7777	
2615	1560	BCL+20	
2616	7377	7377	
2617	1460	SAE+20	
2620	0400	0400	
2621	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=0400
2622	1020	LDA+20	
2623	7777	7777	
2624	1560	BCL+20	
2625	6777	6777	
2626	1460	SAE+20	
2627	1000	1000	
2630	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=1000

2631	1020	LDA+20	
2632	7777	7777	
2633	1560	BCL+20	
2634	5777	5777	
2635	1460	SAE+20	
2636	2000	2000	
2637	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=2000
2640	1020	LDA+20	
2641	7777	7777	
2642	1560	BCL+20	
2643	3777	3777	
2644	1460	SAE+20	
2645	4000	4000	
2646	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR AC=4000
/BCL WILL CLEAR ALL CLEARED BITS AND NOT CLEAR A SINGLE SET BIT			
/			
2647	1020	LDA+20	
2650	0001	0001	
2651	1560	BCL+20	
2652	7776	7776	
2653	1460	SAE+20	
2654	0001	0001	
2655	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=0001
2656	1020	LDA+20	
2657	0002	0002	
2660	1560	BCL+20	
2661	7775	7775	
2662	1460	SAE+20	
2663	0002	0002	
2664	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=0002
2665	1020	LDA+20	
2666	0004	0004	
2667	1560	BCL+20	
2670	7773	7773	
2671	1460	SAE+20	
2672	0004	0004	
2673	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=0004
2674	1020	LDA+20	
2675	0010	0010	
2676	1560	BCL+20	
2677	7767	7767	
2700	1460	SAE+20	
2701	0010	0010	
2702	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=0010
2703	1020	LDA+20	
2704	0020	0020	
2705	1560	BCL+20	
2706	7757	7757	

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2707 1400 SAE*20

2710	0020	0020	
2711	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=0020
2712	1020	LDA+20	
2713	0040	0040	
2714	1560	BCL+20	
2715	7737	7737	
2716	1460	SAE+20	
2717	0040	0040	
2720	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=0040
2721	1020	LDA+20	
2722	0100	0100	
2723	1560	BCL+20	
2724	7677	7677	
2725	1460	SAE+20	
2726	0100	0100	
2727	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=0100
2730	1020	LDA+20	
2731	0200	0200	
2732	1560	BCL+20	
2733	7577	7577	
2734	1460	SAE+20	
2735	0200	0200	
2736	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=0200
2737	1020	LDA+20	
2740	0400	0400	
2741	1560	BCL+20	
2742	7377	7377	
2743	1460	SAE+20	
2744	0400	0400	
2745	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=0400
2746	1020	LDA+20	
2747	1000	1000	
2750	1560	BCL+20	
2751	6777	6777	
2752	1460	SAE+20	
2753	1000	1000	
2754	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=1000
2755	1020	LDA+20	
2756	2000	2000	
2757	1560	BCL+20	
2760	5777	5777	
2761	1460	SAE+20	
2762	2000	2000	
2763	0000	HLT	/BCL CLEARED OR SET A BIT IN ERROR, AC=2000

```

2764 1020          LDA+20
2765 4000          4000
2766 1560          BCL+20
2767 3777          3777
2770 1460          SAE+20
2771 4000          4000
2772 0000          HLT

```

```

/END OF BCL TEST 5, SKIP TO BSE TEST 1
/BCL CLEARED OR SET A BIT IN ERROR, AC=4000

```

```

/BSE TEST1 BSE WILL SET A SINGLE ONE IN A FIELD OF ZEROS
/

```

```

2773 0011          CLR
2774 1620          BSE+20
2775 0001          0001
2776 1460          SAE+20
2777 0001          0001
3000 0000          HLT

```

```

/BSE WILL ATTEMPT TO SET A SINGLE 1 BIT
/IN A FIELD OF ZEROS

```

```

/BSE FAILED TO SET AC 11 AC=0001

```

```

3001 0011          CLR
3002 1620          BSE+20
3003 0002          0002
3004 1460          SAE+20
3005 0002          0002
3006 0000          HLT

```

```

/BSE FAILED TO SET AC 10 AC=0002

```

```

3007 0011          CLR
3010 1620          BSE+20
3011 0004          0004
3012 1460          SAE+20
3013 0004          0004
3014 0000          HLT

```

```

/BSE FAILED TO SET AC 9 AC=0004

```

```

3015 0011          CLR
3016 1620          BSE+20
3017 0010          0010
3020 1460          SAE+20
3021 0010          0010
3022 0000          HLT

```

```

/BSE FAILED TO SET AC 8 AC=0010

```

```

3023 0011          CLR
3024 1620          BSE+20
3025 0020          0020
3026 1460          SAE+20
3027 0020          0020
3030 0000          HLT

```

```

/BSE FAILED TO SET AC 7 AC=0020

```

```

3031 0011          CLR
3032 1620          BSE+20
3033 0040          0040
3034 1460          SAE+20
3035 0040          0040
3036 0000          HLT

```

```

/BSE FAILED TO SET AC 6 AC=0040

```

```

3037 0011          CLR
3040 1620          BSE+20

```

3041	0100	0100
3042	1400	SAE+20
3043	0100	0100

```
3044 0000          HLT          /BSE FAILED TO SET AC 5 AC=0100
3045 0011          CLR
3046 1620          BSE+20
3047 0200          0200
3050 1460          SAE+20
3051 0200          0200
3052 0000          HLT          /BSE FAILED TO SET AC 4 AC=0200
3053 0011          CLR
3054 1620          BSE+20
3055 0400          0400
3056 1460          SAE+20
3057 0400          0400
3060 0000          HLT          /BSE FAILED TO SET AC 3 AC=0400
3061 0011          CLR
3062 1620          BSE+20
3063 1000          1000
3064 1460          SAE+20
3065 1000          1000
3066 0000          HLT          /BSE FAILED TO SET AC 2 AC=1000
3067 0011          CLR
3070 1620          BSE+20
3071 2000          2000
3072 1460          SAE+20
3073 2000          2000
3074 0000          HLT          /BSE FAILED TO SET AC 1 AC=2000
3075 0011          CLR
3076 1620          BSE+20
3077 4000          4000
3100 1460          SAE+20
3101 4000          4000
3102 0000          HLT          /END OF BSE TEST 1, SKIP TO BSE TEST 2
                                   /BSE FAILED TO SET AC 0 AC=4000
/
/BSE TEST 2 WILL TRY AND SET ALL BITS
/
3103 1020          LDA+20
3104 7776          7776
3105 1620          BSE+20
3106 7777          7777
3107 0450          ABE
3110 0000          HLT          /BSE FAILED TO SET AC11 AC=7777
3111 1020          LDA+20
3112 7775          7775
3113 1620          BSE+20
3114 7777          7777
3115 0450          ABE
3116 0000          HLT          /BSE FAILED TO SET AC10 AC=7777
3117 1020          LDA+20
3120 7773          7773
```

/PDP-12 CP TEST PART 2 SKIP AND DATA HANDLING MAINDEC D0AB PAL10 V141 29-OCT-69 1110 PAGE 41-1

3121 1620 BSE+20

3122	7777	7777	
3123	0450	AZE	
3124	0000	HLT	/BSE FAILED TO SET AC09 AC=7777
3125	1020	LDA+20	
3126	7767	7767	
3127	1620	BSE+20	
3130	7777	7777	
3131	0450	AZE	
3132	0000	HLT	/BSE FAILED TO SET AC08 AC=7777
3133	1020	LDA+20	
3134	7757	7757	
3135	1620	BSE+20	
3136	7777	7777	
3137	0450	AZE	
3140	0000	HLT	/BSE FAILED TO SET AC07 AC=7777
3141	1020	LDA+20	
3142	7737	7737	
3143	1620	BSE+20	
3144	7777	7777	
3145	0450	AZE	
3146	0000	HLT	/BSE FAILED TO SET AC06 AC=7777
3147	1020	LDA+20	
3150	7677	7677	
3151	1620	BSE+20	
3152	7777	7777	
3153	0450	AZE	
3154	0000	HLT	/BSE FAILED TO SET AC05 AC=7777
3155	1020	LDA+20	
3156	7577	7577	
3157	1620	BSE+20	
3160	7777	7777	
3161	0450	AZE	
3162	0000	HLT	/BSE FAILED TO SET AC04 AC=7777
3163	1020	LDA+20	
3164	7377	7377	
3165	1620	BSE+20	
3166	7777	7777	
3167	0450	AZE	
3170	0000	HLT	/BSE FAILED TO SET AC03 AC=7777
3171	1020	LDA+20	
3172	6777	6777	
3173	1620	BSE+20	
3174	7777	7777	
3175	0450	AZE	
3176	0000	HLT	/BSE FAILED TO SET AC02 AC=7777
3177	1020	LDA+20	
3200	5777	5777	

```

3201 1020      BSE+20
3202 7777      7777
3203 0450      AZE
3204 0000      HLT                /BSE FAILED TO SET AC01 AC=7777

3205 1020      LDA+20
3206 3777      3777
3207 1620      BSE+20
3210 7777      7777
3211 0450      AZE                /END OF BSE TESTS, SKIP TO BCO TEST 1
3212 0000      HLT                /BSE FAILED TO SET AC00 AC=7777

/BCO TEST 1 BCO WILL COMPLEMENT CORRESPONDING BITS OF THE AC
/
3213 0011      CLR
3214 1660      BCO+20
3215 0001      0001
3216 1460      SAE+20
3217 0001      0001
3220 0000      HLT                /BCO FAILED TO COMPLEMENT AC 11 TO A ONE

3221 0011      CLR
3222 1660      BCO+20
3223 0002      0002
3224 1460      SAE+20
3225 0002      0002
3226 0000      HLT                /BCO FAILED TO COMPLEMENT AC 10 TO A ONE

3227 0011      CLR
3230 1660      BCO+20
3231 0004      0004
3232 1460      SAE+20
3233 0004      0004
3234 0000      HLT                /BCO FAILED TO COMPLEMENT AC 9 TO A ONE

3235 0011      CLR
3236 1660      BCO+20
3237 0010      0010
3240 1460      SAE+20
3241 0010      0010
3242 0000      HLT                /BCO FAILED TO COMPLEMENT AC 8 TO A ONE

3243 0011      CLR
3244 1660      BCO+20
3245 0020      0020
3246 1460      SAE+20
3247 0020      0020
3250 0000      HLT                /BCO FAILED TO COMPLEMENT AC 7 TO A ONE

3251 0011      CLR
3252 1660      BCO+20
3253 0040      0040

```

3254	1460	SAE+20	
3255	0040	0040	
3256	0000	HLT	/BCO FAILED TO COMPLEMENT AC 6 TO A ONE
3257	0011	CLR	
3260	1660	BCO+20	
3261	0100	0100	
3262	1460	SAE+20	
3263	0100	0100	
3264	0000	HLT	/BCO FAILED TO COMPLEMENT AC 5 TO A ONE
3265	0011	CLR	
3266	1660	BCO+20	
3267	0200	0200	
3270	1460	SAE+20	
3271	0200	0200	
3272	0000	HLT	/BCO FAILED TO COMPLEMENT AC4 TO A ONE
3273	0011	CLR	
3274	1660	BCO+20	
3275	0400	0400	
3276	1460	SAE+20	
3277	0400	0400	
3300	0000	HLT	/BCO FAILED TO COMPLEMENT AC3 TO A ONE
3301	0011	CLR	
3302	1660	BCO+20	
3303	1000	1000	
3304	1460	SAE+20	
3305	1000	1000	
3306	0000	HLT	/BCO FAILED TO COMPLEMENT AC2 TO A ONE
3307	0011	CLR	
3310	1660	BCO+20	
3311	2000	2000	
3312	1460	SAE+20	
3313	2000	2000	
3314	0000	HLT	/BCO FAILED TO COMPLEMENT AC1 TO A ONE
3315	0011	CLR	
3316	1660	BCO+20	
3317	4000	4000	
3320	1460	SAE+20	
3321	4000	4000	
3322	0000	HLT	/BCO FAILED TO COMPLEMENT AC0 TO A ONE
3323	1020	LDA+20	
3324	0001	0001	
3325	1660	BCO+20	
3326	0001	0001	
3327	0450	AZE	
3330	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC11 TO A ZERO
3331	1020	LDA+20	

3332	0002	0002	
3333	1660	BCO+20	
3334	0002	0002	
3335	0450	AZE	
3336	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC10 TO A ZERO
3337	1020	LDA+20	
3340	0004	0004	
3341	1660	BCO+20	
3342	0004	0004	
3343	0450	AZE	
3344	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC9 TO A ZERO
3345	1020	LDA+20	
3346	0010	0010	
3347	1660	BCO+20	
3350	0010	0010	
3351	0450	AZE	
3352	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC8 TO A ZERO
3353	1020	LDA+20	
3354	0020	0020	
3355	1660	BCO+20	
3356	0020	0020	
3357	0450	AZE	
3360	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC7 TO A ZERO
3361	1020	LDA+20	
3362	0040	0040	
3363	1660	BCO+20	
3364	0040	0040	
3365	0450	AZE	
3366	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC6 TO A ZERO
3367	1020	LDA+20	
3370	0100	0100	
3371	1660	BCO+20	
3372	0100	0100	
3373	0450	AZE	
3374	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC5 TO A ZERO
3375	1020	LDA+20	
3376	0200	0200	
3377	1660	BCO+20	
3400	0200	0200	
3401	0450	AZE	
3402	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC4 TO A ZERO
3403	1020	LDA+20	
3404	0400	0400	
3405	1660	BCO+20	
3406	0400	0400	
3407	0450	AZE	
3410	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC3 TO A ZERO

3411	1020	LDA+20	
3412	1000	1000	
3413	1660	BCO+20	
3414	1000	1000	
3415	0450	AZE	
3416	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC2 TO A ZERO
3417	1020	LDA+20	
3420	2000	2000	
3421	1660	BCO+20	
3422	2000	2000	
3423	0450	AZE	
3424	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC1 TO A ZERO
3425	1020	LDA+20	
3426	4000	4000	
3427	1660	BCO+20	
3430	4000	4000	
3431	0450	AZE	
3432	0000	HLT	/BCO FAILED TO RECOMPLEMENT AC0 TO A ZERO
3433	0011	CLR	
3434	1020	LDA+20	
3435	7776	7776	
3436	1460	SAE+20	
3437	7776	7776	
3440	0000	HLT	/BCO FAILED AC=7776
3441	0011	CLR	
3442	1660	BCO+20	
3443	7775	7775	
3444	1460	SAE+20	
3445	7775	7775	
3446	0000	HLT	/BCO FAILED AC=7775
3447	0011	CLR	
3450	1660	BCO+20	
3451	7773	7773	
3452	1460	SAE+20	
3453	7773	7773	
3454	0000	HLT	/BCO FAILED AC=7773
3455	0011	CLR	
3456	1660	BCO+20	
3457	7767	7767	
3460	1460	SAE+20	
3461	7767	7767	
3462	0000	HLT	/BCO FAILED AC=7767
3463	0011	CLR	
3464	1660	BCO+20	
3465	7757	7757	
3466	1460	SAE+20	
3467	7757	7757	

3470	0000	HLT	/BCO FAILED AC=7737
3471	0011	CLR	
3472	1660	BCO+20	
3473	7737	7737	
3474	1460	SAE+20	
3475	7737	7737	
3476	0000	HLT	/BCO FAILED AC=7737
3477	0011	CLR	
3500	1660	BCO+20	
3501	7677	7677	
3502	1460	SAE+20	
3503	7677	7677	
3504	0000	HLT	/BCO FAILED AC=7677
3505	0011	CLR	
3506	1660	BCO+20	
3507	7577	7577	
3510	1460	SAE+20	
3511	7577	7577	
3512	0000	HLT	/BCO FAILED AC=7577
3513	0011	CLR	
3514	1660	BCO+20	
3515	7377	7377	
3516	1460	SAE+20	
3517	7377	7377	
3520	0000	HLT	/BCO FAILED AC=7377
3521	0011	CLR	
3522	1660	BCO+20	
3523	6777	6777	
3524	1460	SAE+20	
3525	6777	6777	
3526	0000	HLT	/BCO FAILED AC=6777
3527	0011	CLR	
3530	1660	BCO+20	
3531	5777	5777	
3532	1460	SAE+20	
3533	5777	5777	
3534	0000	HLT	/BCO FAILED AC=5777
3535	0011	CLR	
3536	1660	BCO+20	
3537	3777	3777	
3540	1460	SAE+20	
3541	3777	3777	
3542	0000	HLT	/BCO FAILED AC=3777
3543	1020	LDA+20	
3544	7777	7777	
3545	1660	BCO+20	
3546	0001	0001	

3547	1460	SAE+20	
3550	7776	7776	
3551	0000	HLT	/BCO FAILED AC=7776
3552	1020	LDA+20	
3553	7777	7777	
3554	1660	BCO+20	
3555	0002	0002	
3556	1460	SAE+20	
3559	7775	7775	
3560	0000	HLT	/BCO FAILED AC=7775
3561	1020	LDA+20	
3562	7777	7777	
3563	1660	BCO+20	
3564	0004	0004	
3565	1460	SAE+20	
3566	7773	7773	
3567	0000	HLT	/BCO FAILED AC=7773
3570	1020	LDA+20	
3571	7777	7777	
3572	1660	BCO+20	
3573	0010	0010	
3574	1460	SAE+20	
3575	7767	7767	
3576	0000	HLT	/BCO FAILED AC=7767
3577	1020	LDA+20	
3600	7777	7777	
3601	1660	BCO+20	
3602	0020	0020	
3603	1460	SAE+20	
3604	7757	7757	
3605	0000	HLT	/BCO FAILED AC=7757
3606	1020	LDA+20	
3607	7777	7777	
3610	1660	BCO+20	
3611	0040	0040	
3612	1460	SAE+20	
3613	7737	7737	
3614	0000	HLT	/BCO FAILED AC=7737
3615	1020	LDA+20	
3616	7777	7777	
3617	1660	BCO+20	
3620	0100	0100	

3621 1460 SAE+20
3622 7677 7677
3623 0000 HLT /BCO FAILED AC=7677

3624 1020 LDA+20
3625 7777 7777
3626 1660 BCO+20
3627 0200 0200
3630 1460 SAE+20
3631 7577 7577
3632 0000 HLT /BCO FAILED AC=7577

3633 1020 LDA+20
3634 7777 7777
3635 1660 BCO+20
3636 0400 0400
3637 1460 SAE+20
3640 7377 7377
3641 0000 HLT /BCO FAILED AC=7377

3642 1020 LDA+20
3643 7777 7777
3644 1660 BCO+20
3645 1000 1000
3646 1460 SAE+20
3647 6777 6777
3650 0000 HLT /BCO FAILED AC=6777

3651 1020 LDA+20
3652 7777 7777
3653 1660 BCO+20
3654 2000 2000
3655 1460 SAE+20
3656 5777 5777
3657 0000 HLT /BCO FAILED AC=5777

3660 1020 LDA+20
3661 7777 7777
3662 1660 BCO+20
3663 4000 4000
3664 1460 SAE+20
3665 3777 3777
3666 0000 HLT /BCO FAILED AC=3777

/ADA TEST 1 (ADA ARITHMETIC IS 1'S COMPLEMENT)

3667	1020	ADATST, LDA+20	
3670	0001	0001	
3671	1120	ADA+20	
3672	0001	0001	
3673	1400	SAE+20	
3674	0002	0002	
3675	0000	HLT	/ADA CARRY AC11-10 FAILED AC=0002
3676	1020	LDA+20	
3677	0002	0002	
3700	1120	ADA+20	
3701	0002	0002	
3702	1400	SAE+20	
3703	0004	0004	
3704	0000	HLT	/ADA CARRY AC10-9 FAILED AC=0004
3705	1020	LDA+20	
3706	0004	0004	
3707	1120	ADA+20	
3710	0004	0004	
3711	1400	SAE+20	
3712	0010	0010	
3713	0000	HLT	/ADA CARRY AC9-8 FAILED AC=0010
3714	1020	LDA+20	
3715	0010	0010	
3716	1120	ADA+20	
3717	0010	0010	
3720	1400	SAE+20	
3721	0020	0020	
3722	0000	HLT	/ADA CARRY AC8-7 FAILED AC=0020
3723	1020	LDA+20	
3724	0020	0020	
3725	1120	ADA+20	
3726	0020	0020	
3727	1400	SAE+20	
3730	0040	0040	
3731	0000	HLT	/ADA CARRY AC 7-6 FAILED AC=0040
3732	1020	LDA+20	
3733	0040	0040	
3734	1120	ADA+20	
3735	0040	0040	
3736	1400	SAE+20	
3737	0100	0100	
3740	0000	HLT	/ADA CARRY AC6-5 FAILED AC=0100
3741	1020	LDA+20	
3742	0100	0100	
3743	1120	ADA+20	
3744	0100	0100	
3745	1400	SAE+20	
3746	0200	0200	

/POP=12 CP TEST PART 2 SKIP AND DATA HANDLING MAINDEC D0AB PAL10 V141 29=OCT=69 1110 PAGE 50=1
3747 0000 HLT /ADD CARRY AC5=4 FAILED AC=0200

```

3750 1020      LDA+20
3751 0200      0200
3752 1120      ADA+20
3753 0200      0200
3754 1400      SAE+20
3755 0400      0400
3756 0000      HLT          /ADA CARRY AC4=3 FAILED AC=0400

3757 1020      LDA+20
3760 0400      0400
3761 1120      ADA+20
3762 0400      0400
3763 1400      SAE+20      /TEST PARTIALLY COMPLETE; CHANGE IF
3764 1000      1000
3765 0000      HLT          /ADA CARRY AC3=2 FAILED AC=1000

/6141 TEST
3766 0002      PDP
3767 5770      5000,+1=2000 /JMP I ,+1
3770 4030      4030
      4020      *4020
/MINOR START LINC MODE,
4020 0002      PDP
4021 5622      5600,+1      /JMP I ,+1
4022 0020      0020
4023 0016      NOP
4024 0000      HLT          /TO HERE IF 6141 FAILS
      4030      *4030
/ADA TEST 1 CONT,
4030 6141      LINC
4031 1020      LDA+20
4032 1000      1000
4033 1120      ADA+20
4034 1000      1000
4035 1400      SAE+20
4036 2000      2000
4037 0000      HLT          /ADA CARRY AC2=1 FAILED AC=2000

```

4040 1020 LDA+20
4041 2000 2000
4042 1120 ADA+20
4043 2000 2000
4044 1400 SAE+20
4045 4000 4000
4046 0000 HLT

/ADA CARRY AC1=0 FAILED AC=4000

4047 1020 LDA+20
4050 4000 4000
4051 1120 ADA+20
4052 4000 4000
4053 1400 SAE+20
4054 0001 0001
4055 0000 HLT

/END OF ADA TESTS, SKIP TO SET TEST 1

/END AROUND CARRY FAILED AC=0001

/SET TEST SET BETA REGISTER = OPERAND

4056	0011	CLR	
4057	0061	SETTST, SET+20+1	/SET B REGISTER 0 TO 0000
4060	0000	0000	
4061	1440	SAE	
4062	0001	0001	
4063	0000	HLT	/SET CAN'T LOAD 0000 INTO B REGISTER AC=0000
4064	0061	SET+20+1	
4065	0001	0001	
4066	1020	LDA+20	
4067	0001	0001	
4070	1440	SAE	
4071	0001	0001	
4072	0000	HLT	/SET CAN'T LOAD 0001 INTO B REGISTER AC=0001
4073	0061	SET+20+1	
4074	0002	0002	
4075	1020	LDA+20	
4076	0002	0002	
4077	1440	SAE	
4100	0001	0001	
4101	0000	HLT	/SET CAN'T LOAD 0002 INTO B REGISTER AC=0002
4102	0061	SET+20+1	
4103	0004	0004	
4104	1020	LDA+20	
4105	0004	0004	
4106	1440	SAE	
4107	0001	0001	
4110	0000	HLT	/SET CAN'T LOAD 0004 INTO B REGISTER AC=0004
4111	0061	SET+20+1	
4112	0010	0010	
4113	1020	LDA+20	
4114	0010	0010	
4115	1440	SAE	
4116	0001	0001	
4117	0000	HLT	/SET CAN'T LOAD 0010 INTO B REGISTER AC=0010
4120	0061	SET+20+1	
4121	0020	0020	
4122	1020	LDA+20	
4123	0020	0020	
4124	1440	SAE	
4125	0001	0001	
4126	0000	HLT	/SET CAN'T LOAD 0020 INTO B REGISTER AC=0020
4127	0061	SET+20+1	
4130	0040	0040	
4131	1020	LDA+20	
4132	0040	0040	
4133	1440	SAE	
4134	0001	0001	
4135	0000	HLT	/SET CAN'T LOAD 0040 INTO B REGISTER AC=0040

4136	0061	SET+20+1	
4137	0100	0100	
4140	1020	LDA+20	
4141	0100	0100	
4142	1440	SAE	
4143	0001	0001	
4144	0000	HLT	/SET CAN'T LOAD 0100 INTO B REGISTER AC=0100
4145	0061	SET+20+1	
4146	0200	0200	
4147	1020	LDA+20	
4150	0200	0200	
4151	1440	SAE	
4152	0001	0001	
4153	0000	HLT	/SET CAN'T LOAD 0200 INTO B REGISTER AC=0200
4154	0061	SET+20+1	
4155	0400	0400	
4156	1020	LDA+20	
4157	0400	0400	
4160	1440	SAE	
4161	0001	0001	
4162	0000	HLT	/SET CAN'T LOAD 0400 INTO B REGISTER AC=0400
4163	0061	SET+20+1	
4164	1000	1000	
4165	1020	LDA+20	
4166	1000	1000	
4167	1440	SAE	
4170	0001	0001	
4171	0000	HLT	/SET CAN'T LOAD 1000 INTO B REGISTER AC=1000
4172	0061	SET+20+1	
4173	2000	2000	
4174	1020	LDA+20	
4175	2000	2000	
4176	1440	SAE	
4177	0001	0001	
4200	0000	HLT	/SET CAN'T LOAD 2000 INTO B REGISTER AC=2000
4201	0061	SET+20+1	
4202	4000	4000	
4203	1020	LDA+20	
4204	4000	4000	
4205	1440	SAE	
4206	0001	0001	
4207	0000	HLT	/SET CAN'T LOAD 4000 INTO BE REGISTER AC=4000
4210	0061	SET+20+1	
4211	7777	7777	
4212	1020	LDA+20	
4213	7777	7777	
4214	1440	SAE	
4215	0001	0001	

4216	0000	HLT	/SET CAN'T LOAD 7777 INTO B REGISTER AC=7777
4217	0061	SET+20*1	
4220	5252	5252	
4221	1020	LDA+20	
4222	5252	5252	
4223	1440	SAE	
4224	0001	0001	
4225	0000	HLT	/SET CAN'T LOAD 5252 INTO B REGISTER AC=5252
4226	0061	SET+20*1	
4227	2525	2525	
4230	1020	LDA+20	
4231	2525	2525	
4232	1440	SAE	
4233	0001	0001	
4234	0000	HLT	/SET CAN'T LOAD 2525 INTO B REGISTER AC=2525
4235	0062	SET+20*2	
4236	0000	0000	
4237	0011	CLR	
4240	1440	SAE	
4241	0002	0002	
4242	0000	HLT	/SET CAN'T LOAD 0000 INTO 2 AC=0000
4243	0062	SET+20*2	
4244	7777	7777	
4245	1020	LDA+20	
4246	7777	7777	
4247	1440	SAE	
4250	0002	0002	
4251	0000	HLT	/SET CAN'T LOAD 7777 INTO 2 AC=7777

```
4252 0065      SET+20+5
4253 0000      0000
4254 0011      CLR
4255 1440      SAE
4256 0005      0005
4257 0000      HLT          /SET CAN'T LOAD 0000 INTO 5 AC=0000

4260 0065      SET+20+5
4261 7777      7777
4262 1020      LDA+20
4263 7777      7777
4264 1440      SAE
4265 0005      0005
4266 0000      HLT          /SET CAN'T LOAD 7777 INTO 5 AC=7777

4267 0066      SET+20+6
4270 0000      0000
4271 0011      CLR
4272 1440      SAE
4273 0006      0006
4274 0000      HLT          /SET CAN'T LOAD 0000 INTO 6 AC=0000

4275 0066      SET+20+6
4276 7777      7777
4277 1020      LDA+20
4300 7777      7777
4301 1440      SAE
4302 0006      0006
4303 0000      HLT          /SET CAN'T LOAD 7777 INTO 6 AC=7777

4304 0067      SET+20+7
4305 0000      0000
4306 0011      CLR
4307 1440      SAE
4310 0007      0007
4311 0000      HLT          /SET CAN'T LOAD 0000 INTO 7 AC=0000

4312 0067      SET+20+7
4313 7777      7777
4314 1020      LDA+20
4315 7777      7777
4316 1440      SAE
4317 0007      0007
4320 0000      HLT          /SET CAN'T LOAD 7777 INTO 7 AC=7777
```

4321	0070	SET+20+10	
4322	0000	0000	
4323	0011	CLR	
4324	1440	SAE	
4325	0010	0010	
4326	0000	HLT	/SET CAN'T LOAD 0000 INTO 10 AC=0000
4327	0070	SET+20+10	
4330	7777	7777	
4331	1020	LOA+20	
4332	7777	7777	
4333	1440	SAE	
4334	0010	0010	
4335	0000	HLT	/SET CAN'T LOAD 7777 INTO 10 AC=7777
4336	0071	SET+20+11	
4337	0000	0000	
4340	0011	CLR	
4341	1440	SAE	
4342	0011	0011	
4343	0000	HLT	/SET CAN'T LOAD 0000 INTO 11 AC=0000

4344	0071	SET+20+11	
4345	7777	7777	
4346	1020	LDA+20	
4347	7777	7777	
4350	1440	SAE	
4351	0011	0011	
4352	0000	HLT	/SET CAN'T LOAD 7777 INTO 11 AC=7777
4353	0072	SET+20+12	
4354	0000	0000	
4355	0011	CLR	
4356	1440	SAE	
4357	0012	0012	
4360	0000	HLT	/SET CAN'T LOAD 0000 INTO 12 AC=0000
4361	0072	SET+20+12	
4362	7777	7777	
4363	1020	LDA+20	
4364	7777	7777	
4365	1440	SAE	
4366	0012	0012	
4367	0000	HLT	/SET CAN'T LOAD 7777 INTO 12 AC=7777
4370	0073	SET+20+13	
4371	0000	0000	
4372	0011	CLR	
4373	1440	SAE	
4374	0013	0013	
4375	0000	HLT	/SET CAN'T LOAD 0000 INTO 13 AC=0000
4376	0073	SET+20+13	
4377	7777	7777	
4400	1020	LDA+20	
4401	7777	7777	
4402	1440	SAE	
4403	0013	0013	
4404	0000	HLT	/SET CAN'T LOAD 7777 INTO 13 AC=7777

4405	0074	SET+20*14	
4406	0000	0000	
4407	0011	CLR	
4410	1440	SAE	
4411	0014	0014	
4412	0000	HLT	/SET CAN'T LOAD 0000 INTO 14 AC=0000
4413	0074	SET+20*14	
4414	7777	7777	
4415	1020	LDA+20	
4416	7777	7777	
4417	1440	SAE	
4420	0014	0014	
4421	0000	HLT	/SET CAN'T LOAD 7777 INTO 14 AC=7777
4422	0075	SET+20*15	
4423	0000	0000	
4424	0011	CLR	
4425	1440	SAE	
4426	0015	0015	
4427	0000	HLT	/SET CAN'T LOAD 0000 INTO 15 AC=0000
4430	0075	SET+20*15	
4431	7777	7777	
4432	1020	LDA+20	
4433	7777	7777	
4434	1440	SAE	
4435	0015	0015	
4436	0000	HLT	/SET CAN'T LOAD 7777 INTO 15 AC=7777

```

4437 0076      SET+20*16
4440 0000      0000
4441 0011      CLR
4442 1440      SAE
4443 0016      0016
4444 0000      HLT          /SET CAN'T LOAD 0000 INTO 16 AC=0000

```

```

4445 0076      SET+20*16
4446 7777      7777
4447 1020      LDA+20
4450 7777      7777
4451 1440      SAE
4452 0016      0016
4453 0000      HLT          /SET CAN'T LOAD 7777 INTO 16 AC=7777

```

```

4454 0077      SET+20*17
4455 0000      0000
4456 0011      CLR
4457 1440      SAE
4460 0017      0017
4461 0000      HLT          /SET CAN'T LOAD 0000 INTO 17 AC=0000

```

```

4462 0077      SET+20*17
4463 7777      7777
4464 1020      LDA+20
4465 7777      7777
4466 1440      SAE
4467 0017      0017
4470 0000      HLT          /SET CAN'T LOAD 7777 INTO 17 AC=7777

```

/SCR TEST SCALE RIGHT INTO AC AND MQ

```

4471 0011      CLR
4472 1020      LDA+20
4473 4000      4000
4474 0340      SCR
4475 1460      SAE+20
4476 4000      4000
4477 0000      HLT          /SCR 0 FAILED AC=4000 MQ=0000

```

```

4500 1020      LDA+20
4501 4000      4000
4502 0341      SCR+1
4503 1460      SAE+20
4504 6000      6000
4505 0000      HLT          /SCR FAILED BIT 1 AC=6000 MQ=0000

```

```

4506 1020      LDA+20
4507 4000      4000
4510 0342      SCR+2
4511 1460      SAE+20
4512 7000      7000
4513 0000      HLT          /SCR FAILED BIT 2 AC=7000 MQ=0000

```

4514	1020	LDA+20	
4515	4000	4000	
4516	0343	SCR+3	
4517	1460	SAE+20	
4520	7400	7400	
4521	0000	HLT	/SCR FAILED BIT 3 AC=7400 MQ=0000
4522	1020	LDA+20	
4523	4000	4000	
4524	0344	SCR+4	
4525	1460	SAE+20	
4526	7600	7600	
4527	0000	HLT	/SCR FAILED BIT 4 AC=7600 MQ=0000
4530	1020	LDA+20	
4531	4000	4000	
4532	0345	SCR+5	
4533	1460	SAE+20	
4534	7700	7700	
4535	0000	HLT	/SCR FAILED BIT 5 AC=7700 MQ=0000
4536	1020	LDA+20	
4537	4000	4000	
4540	0346	SCR+6	
4541	1460	SAE+20	
4542	7740	7740	
4543	0000	HLT	/SCR FAILED BIT 6 AC=7740 MQ=0000
4544	1020	LDA+20	
4545	4000	4000	
4546	0347	SCR+7	
4547	1460	SAE+20	
4550	7760	7760	
4551	0000	HLT	/SCR FAILED BIT 7 AC=7760 MQ=0000
4552	1020	LDA+20	
4553	4000	4000	
4554	0350	SCR+10	
4555	1460	SAE+20	
4556	7770	7770	
4557	0000	HLT	/SCR FAILED BIT 8 AC=7770 MQ=0000

4560	1020	LDA+20	
4561	4000	4000	
4562	0351	SCR+11	
4563	1460	SAE+20	
4564	7774	7774	
4565	0000	HLT	/SCR FAILED BIT 8 AC=7774 MQ=0000
4566	1020	LDA+20	
4567	4000	4000	
4570	0352	SCR+12	
4571	1460	SAE+20	
4572	7776	7776	
4573	0000	HLT	/SCR FAILED BIT 9 AC=7776 MQ=0000
4574	1020	LDA+20	
4575	4000	4000	
4576	0353	SCR+13	
4577	1460	SAE+20	
4600	7777	7777	
4601	0000	HLT	/SCR FAILED BIT 10 AC=7777 MQ=0000
4602	1020	LDA+20	
4603	4000	4000	
4604	0354	SCR+14	
4605	0005	QAC	
4606	1460	SAE+20	
4607	2000	2000	
4610	0000	HLT	/SCR FAILED BIT 11 TO 20 AC=7777 MQ=4000
4611	0011	CLR	
4612	1020	LDA+20	
4613	4000	4000	
4614	0355	SCR+15	
4615	0005	QAC	
4616	1460	SAE+20	
4617	3000	3000	
4620	0000	HLT	/SCR FAILED Z1 AC=7777 MQ=6000
4621	0011	CLR	
4622	1020	LDA+20	
4623	4000	4000	
4624	0356	SCR+16	
4625	0005	QAC	
4626	1460	SAE+20	
4627	3400	3400	
4630	0000	HLT	/SCR FAILED Z2 AC=7777 MQ=7000
4631	0011	CLR	
4632	1020	LDA+20	
4633	4000	4000	
4634	0357	SCR+17	
4635	0005	QAC	
4636	1460	SAE+20	
4637	3600	3600	
4640	0000	HLT	/SCR FAILED Z3 AC=7777 MQ=7400

4641	0011	CLR	
4642	1020	LDA+20	
4643	6000	6000	
4644	0357	SCR+17	
4645	0005	QAC	
4646	1460	SAE+20	
4647	3700	3700	
4650	0000	HLT	/SCR FAILED Z4 AC=7777 MQ=7600
4651	0011	CLR	
4652	1020	LDA+20	
4653	7000	7000	
4654	0357	SCR+17	
4655	0005	QAC	
4656	1460	SAE+20	
4657	3740	3740	
4660	0000	HLT	/SCR FAILED Z5 AC=7777 MQ=7700
4661	0011	CLR	
4662	1020	LDA+20	
4663	7400	7400	
4664	0357	SCR+17	
4665	0005	QAC	
4666	1460	SAE+20	
4667	3760	3760	
4670	0000	HLT	/SCR FAILED Z6 AC=7777 MQ=7740
4671	0011	CLR	
4672	1020	LDA+20	
4673	7600	7600	
4674	0357	SCR+17	
4675	0005	QAC	
4676	1460	SAE+20	
4677	3770	3770	
4700	0000	HLT	/SCR FAILED Z7 AC=7777 MQ=7760
4701	0011	CLR	
4702	1020	LDA+20	
4703	7700	7700	
4704	0357	SCR+17	
4705	0005	QAC	
4706	1460	SAE+20	
4707	3774	3774	
4710	0000	HLT	/SCR FAILED Z8 AC=7777 MQ=7770
4711	0011	CLR	
4712	1020	LDA+20	
4713	7740	7740	
4714	0357	SCR+17	
4715	0005	QAC	
4716	1460	SAE+20	
4717	3776	3776	

/SCR FAILED BIT 9 AC=7777 MQ=7774

HLT

4720 0000

4721	0011	CLR	
4722	1020	LDA+20	
4723	7760	7760	
4724	0357	SCR+17	
4725	0005	QAC	
4726	1460	SAE+20	
4727	3777	3777	
4730	0000	HLT	/SCR FAILED BIT 10 AC=7777 MQ=7776
4731	0011	CLR	
4732	1020	LDA+20	
4733	7770	7770	
4734	0357	SCR+17	
4735	0005	QAC	
4736	1460	SAE+20	
4737	3777	3777	
4740	0000	HLT	/SCR FAILED BIT 11 AC=7777 MQ=7776
4741	0011	CLR	
4742	1020	LDA+20	
4743	0001	0001	
4744	0361	SCR+20+1	
4745	0005	QAC	
4746	1460	SAE+20	
4747	2000	2000	
4750	0000	HLT	/SCR +20 FAILED TO SET Z0
4751	0472	LZE+20	
4752	0000	HLT	/SCR +20 FAILED TO SET LINK
4753	0011	CLR	
4754	1020	LDA+20	
4755	7777	7777	
4756	0334	ROR+14+20	/LOADS Z 7777
4757	1020	LDA+20	
4760	7776	7776	
4761	0341	SCR+1	
4762	1460	SAE+20	
4763	7777	7777	
4764	0000	HLT	/SCR FAILED BIT 1
4765	0005	QAC	
4766	1460	SAE+20	
4767	1777	1777	
4770	0000	HLT	/SCR UPSET Z REGISTER
4771	0011	CLR	
4772	1020	LDA+20	
4773	1777	1777	
4774	0341	SCR+1	
4775	1460	SAE+20	
4776	0777	0777	
4777	0000	HLT	/SCR FAILED BIT 2 AC=0777

```
5000 0011 CLR
5001 1020 LDA+20
5002 7760 7760
5003 0357 SCR+17
5004 0005 QAC
5005 1460 SAE+20
5006 3777 3777
5007 0000 HLT /SCR FAILED BIT 10 AC=7777 MQ=7776

5010 0011 CLR
5011 1020 LDA+20
5012 7770 7770
5013 0357 SCR+17
5014 0005 QAC
5015 1460 SAE+20
5016 3777 3777
5017 0000 HLT /SCR FAILED BIT 11 AC=7777 MQ=7776

5020 0011 CLR
5021 1020 LDA+20
5022 0001 0001
5023 0361 SCR+20+1
5024 0005 QAC
5025 1460 SAE+20
5026 2000 2000
5027 0000 HLT /SCR +20 FAILED TO SET 20

5030 0472 LZE+20
5031 0000 HLT /SCR +20 FAILED TO SET LINK

5032 0011 CLR
5033 1020 LDA+20
5034 7777 7777
5035 0334 ROR+14+20 /LOADS ≠ 7777
5036 1020 LDA+20
5037 7776 7776
5040 0341 SCR+1
5041 1460 SAE+20
5042 7777 7777
5043 0000 HLT /SCR FAILED BIT 1

5044 0005 QAC
5045 1460 SAE+20
5046 1777 1777
5047 0000 HLT /SCR UPSET ≠ REGISTER

5050 0011 CLR
5051 1020 LDA+20
5052 1777 1777
5053 0341 SCR+1
5054 1460 SAE+20
5055 0777 0777
5056 0000 HLT /SCR FAILED BIT 2 AC=0777
```

5057	1020	LDA+20	
5060	0777	0777	
5061	0341	SCR+1	
5062	1460	SAE+20	
5063	0377	0377	
5064	0000	HLT	/SCR FAILED BIT 3 AC=0377
5065	1020	LDA+20	
5066	0377	0377	
5067	0341	SCR+1	
5070	1460	SAE+20	
5071	0177	0177	
5072	0000	HLT	/SCR FAILED BIT 4 AC=0177
5073	1020	LDA+20	
5074	0177	0177	
5075	0341	SCR+1	
5076	1460	SAE+20	
5077	0077	0077	
5100	0000	HLT	/SCR FAILED BIT 5 AC=0077
5101	1020	LDA+20	
5102	0077	0077	
5103	0341	SCR+1	
5104	1460	SAE+20	
5105	0037	0037	
5106	0000	HLT	/SCR FAILED BIT 6 AC=0037
5107	1020	LDA+20	
5110	0037	0037	
5111	0341	SCR+1	
5112	1460	SAE+20	
5113	0017	0017	
5114	0000	HLT	/SCR FAILED BIT 7 AC=0017
5115	1020	LDA+20	
5116	0017	0017	
5117	0341	SCR+1	
5120	1460	SAE+20	
5121	0007	0007	
5122	0000	HLT	/SCR FAILED BIT 8 AC=0007
5123	1020	LDA+20	
5124	0007	0007	
5125	0341	SCR+1	
5126	1460	SAE+20	
5127	0003	0003	
5130	0000	HLT	/SCR FAILED BIT 9 AC=0003

5131	1020	LDA+20	
5132	0003	0003	
5133	0341	SCR+1	
5134	1460	SAE+20	
5135	0001	0001	
5136	0000	HLT	/SCR FAILED BIT 10 AC=0001
5137	1020	LDA+20	
5140	0001	0001	
5141	0341	SCR+1	
5142	0450	AZE	
5143	0000	HLT	/SCR FAILED BIT 11 AC=0000

/

/LDH TEST 1, TEST BOTH HALVES USING FIXED NUMBERS
/TEST LDH RIGHT HALF FLOAT A ONE WITH NOISE NUMBERS IN
/THE UNUSED HALF A NEW FLOAT A ZERO

5144	1300	LDH	
5145	5147	,+2	
5146	0456	SKP	
5147	5200	5200	
5150	1460	SAE 20	
5151	0000	0000	
5152	0000	HLT	/LDH FAILED AC=0000 MEM=5200
5153	1300	LDH	
5154	5156	,+2	
5155	0456	SKP	
5156	2501	2501	
5157	1460	SAE 20	
5160	0001	0001	
5161	0000	HLT	/LDH FAILED BIT 11 AC=0001 MEM=2501
5162	1300	LDH	
5163	5165	,+2	
5164	0456	SKP	
5165	5202	5202	
5166	1460	SAE 20	
5167	0002	0002	
5170	0000	HLT	/LDH FAILED BIT 10 AC=0002 MEM=5202
5171	1300	LDH	
5172	5174	,+2	
5173	0456	SKP	
5174	2504	2504	
5175	1460	SAE 20	
5176	0004	0004	
5177	0000	HLT	/LDH FAILED BIT 09 AC=0004 MEM=2504
5200	1300	LDH	
5201	5203	,+2	
5202	0456	SKP	
5203	5210	5210	
5204	1460	SAE 20	
5205	0010	0010	
5206	0000	HLT	/LDH FAILED BIT 08 AC=0010 MEM=5210
5207	1300	LDH	
5210	5212	,+2	
5211	0456	SKP	
5212	2520	2520	
5213	1460	SAE 20	
5214	0020	0020	
5215	0000	HLT	/LDH FAILED BIT 07 AC=0020 MEM=2520

5216	1300	LDH	
5217	5221	,+2	
5220	0456	SKP	
5221	5240	5240	
5222	1460	SAE 20	
5223	0040	0040	
5224	0000	HLT	/LDH FAILED BIT 00 AC=0040 MEM=5240
5225	1300	LDH	
5226	5230	,+2	
5227	0456	SKP	
5230	2577	2577	
5231	1460	SAE 20	
5232	0077	0077	
5233	0000	HLT	/LDH FAILED AC=0077 MEM=2577
5234	1300	LDH	
5235	5237	,+2	
5236	0456	SKP	
5237	5276	5276	
5240	1460	SAE 20	
5241	0076	0076	
5242	0000	HLT	/LDH FAILED AC=0076 MEM=5276
5243	1300	LDH	
5244	5246	,+2	
5245	0456	SKP	
5246	2575	2575	
5247	1460	SAE 20	
5250	0075	0075	
5251	0000	HLT	/LDH FAILED AC=0075 MEM=2575
5252	1300	LDH	
5253	5255	,+2	
5254	0456	SKP	
5255	5273	5273	
5256	1460	SAE 20	
5257	0073	0073	
5260	0000	HLT	/LDH FAILED AC=0073 MEM=5273
5261	1300	LDH	
5262	5264	,+2	
5263	0456	SKP	
5264	2567	2567	
5265	1460	SAE 20	
5266	0067	0067	
5267	0000	HLT	/LDH FAILED AC=0067 MEM=2567
5270	1300	LDH	
5271	5273	,+2	
5272	0456	SKP	
5273	5257	5257	
5274	1460	SAE 20	
5275	0057	0057	
5276	0000	HLT	/LDH FAILED AC=0057 MEM=5257

5277	1300	LDH	
5300	5302	,*2	
5301	0456	SKP	
5302	2537	2537	
5303	1460	SAE 20	
5304	0037	0037	
5305	0000	HLT	/LDH FAILED AC=0037 MEM=2537

/

/LDH TEST
/TEST LDH LEFT HALF

5306	1300	LDH	
5307	1311	,*2=4000	
5310	0456	SKP	
5311	0000	0000	
5312	1460	SAE 20	
5313	0000	0000	
5314	0000	HLT	/LDH FAILED AC=0000 MEM=0000

5315	1300	LDH	
5316	1320	,*2=4000	
5317	0456	SKP	
5320	0152	0152	
5321	1460	SAE 20	
5322	0001	0001	
5323	0000	HLT	/LDH FAILED BIT 05 AC=0001 MEM=0152

5324	1300	LDH	
5325	1327	,*2=4000	
5326	0456	SKP	
5327	0225	0225	
5330	1460	SAE 20	
5331	0002	0002	
5332	0000	HLT	/LDH FAILED BIT 04 AC=0002 MEM=0225

5333	1300	LDH	
5334	1336	,*2=4000	
5335	0456	SKP	
5336	0452	0452	
5337	1460	SAE 20	
5340	0004	0004	
5341	0000	HLT	/LDH FAILED BIT 03 AC=0004 MEM=0452

5342	1300	LDH	
5343	1345	,*2=4000	
5344	0456	SKP	
5345	1025	1025	
5346	1460	SAE 20	
5347	0010	0010	
5350	0000	HLT	/LDH FAILED BIT 02 AC=0010 MEM=1025

5351	1300	LDH	
5352	1354	,*2=4000	

5353 0456
5354 2052
5355 1460
5356 0020
5357 0000

SKP
2052
SAE 20
0020
HLT

/LDH FAILED BIT 01 AC=0020 MEM=2052

5360 1300
5361 1363
5362 0456
5363 4025
5364 1460
5365 0040
5366 0000

LDH
. *2=4000
SKP
4025
SAE 20
0040
HLT

/LDH FAILED BIT 00 AC=0040 MEM=4025

5367 1300
5370 1372
5371 0456
5372 7752
5373 1460
5374 0077
5375 0000

LDH
. *2=4000
SKP
7752
SAE 20
0077
HLT

/LDH FAILED AC=0077 MEM=7752

5376	1300	LDH	
5377	1401	,*2=4000	
5400	0456	SKP	
5401	7625	7625	
5402	1460	SAE 20	
5403	0076	0076	
5404	0000	HLT	/LDH FAILED AC=0076 MEM=7625
5405	1300	LDH	
5406	1410	,*2=4000	
5407	0456	SKP	
5410	7552	7552	
5411	1460	SAE 20	
5412	0075	0075	
5413	0000	HLT	/LDH FAILED AC=0075 MEM=7552
5414	1300	LDH	
5415	1417	,*2=4000	
5416	0456	SKP	
5417	7325	7325	
5420	1460	SAE 20	
5421	0073	0073	
5422	0000	HLT	/LDH FAILED AC=0073 MEM=7325
5423	1300	LDH	
5424	1426	,*2=4000	
5425	0456	SKP	
5426	6752	6752	
5427	1460	SAE 20	
5430	0067	0067	
5431	0000	HLT	/LDH FAILED AC=0067 MEM=6752
5432	1300	LDH	
5433	1435	,*2=4000	
5434	0456	SKP	
5435	5725	5725	
5436	1460	SAE 20	
5437	0057	0057	
5440	0000	HLT	/LDH FAILED AC=0057 MEM=5725
5441	1300	LDH	
5442	1444	,*2=4000	
5443	0456	SKP	
5444	3752	3752	
5445	1460	SAE 20	
5446	0037	0037	/END OF LDH TEST SKIP TO STA TEST
5447	0000	HLT	/LDH FAILED AC=0037 MEM=3752

/STA TEST

5450	0011	CLR	
5451	1000	STA+20	
5452	0000	0000	
5453	1440	SAE	
5454	5452	,=2	
5455	0000	HLT	/STA FAILED AC=0000 MEM=0000
5456	1400	SAE+20	
5457	0000	0000	
5460	0000	HLT	/AC CHANGED AC=0000
5461	1020	LDA+20	
5462	7777	7777	
5463	1000	STA+20	
5464	0000	0000	
5465	1440	SAE	
5466	5464	,=2	
5467	0000	HLT	/STA FAILED AC=7777 MEM=7777
5470	1400	SAE+20	
5471	7777	7777	
5472	0000	HLT	/AC CHANGED AC=7777
5473	1020	LDA+20	
5474	5252	5252	
5475	1000	STA+20	
5476	0000	0000	
5477	1440	SAE	
5500	5476	,=2	
5501	0000	HLT	/STA FAILED AC=5252 MEM=5252
5502	1400	SAE+20	
5503	5252	5252	
5504	0000	HLT	/AC CHANGED AC=5252
5505	1020	LDA+20	
5506	2525	2525	
5507	1000	STA+20	
5510	0000	0000	
5511	1440	SAE	
5512	5510	,=2	
5513	0000	HLT	/STA FAILED AC=2525 MEM=2525
5514	1400	SAE+20	
5515	2525	2525	/END OF STA TEST SKIP ADM TEST
5516	0000	HLT	/AC CHANGED AC=2525

/ADM TEST ADM ARITHMETIC IS 1'S COMPLEMENT

5517	0011	CLR	
5520	1040	STA	
5521	5523	,+2	
5522	1100	ADM+20	
5523	0000	0000	
5524	1440	SAE	

5525	5523	,=2	
5526	0000	HLT	/ADM FAILED AC=0002
5527	1020	LDA*20	
5530	7777	7777	
5531	1040	STA	
5532	5534	,+2	
5533	1160	ADM*20	
5534	0000	0000	
5535	1440	SAE	
5536	5534	,=2	
5537	0000	HLT	/ADM FAILED AC=0004
5540	1020	LDA*20	
5541	5252	5252	
5542	1040	STA	
5543	5545	,+2	
5544	1160	ADM*20	
5545	0004	0004	
5546	1440	SAE	
5547	5545	,=2	
5550	0000	HLT	/ADM FAILED AC=0010
5551	1020	LDA*20	
5552	2525	2525	
5553	1040	STA	
5554	5556	,+2	
5555	1160	ADM*20	
5556	0010	0010	
5557	1440	SAE	
5560	5556	,=2	
5561	0000	HLT	/ADM FAILED AC=0020

/
/XSK SKIP TEST XSK IS TESTED BY FLOATING A ZERO THRU A FIELD OF 1777
/XSK SKIPS ON (Y)=1777

5562	0061	SET+20+1	
5563	0000	0000	
5564	0201	XSK 1	
5565	0456	SKP	
5566	0000	HLT	/XSK SKIPPED ON 0000
5567	0062	SET+20+2	
5570	1776	1776	
5571	0202	XSK 2	
5572	0456	SKP	
5573	0000	HLT	/XSK SKIPPED ON 1776
5574	0063	SET+20+3	
5575	1775	1775	
5576	0203	XSK 3	
5577	0456	SKP	
5600	0000	HLT	/XSK SKIPPED ON 1775
5601	0064	SET+20+4	
5602	1773	1773	
5603	0204	XSK 4	
5604	0456	SKP	
5605	0000	HLT	/XSK SKIPPED ON 1773
5606	0065	SET+20+5	
5607	1767	1767	
5610	0205	XSK 5	
5611	0456	SKP	
5612	0000	HLT	/XSK SKIPPED ON 1767
5613	0066	SET+20+6	
5614	1757	1757	
5615	0206	XSK 6	
5616	0456	SKP	
5617	0000	HLT	/XSK SKIPPED ON 1757
5620	0067	SET+20+7	
5621	1737	1737	
5622	0207	XSK 7	
5623	0456	SKP	
5624	0000	HLT	/XSK SKIPPED ON 1737
5625	0070	SET+20+10	
5626	1677	1677	
5627	0210	XSK 10	
5630	0456	SKP	
5631	0000	HLT	/XSK SKIPPED ON 1677
5632	0071	SET+20+11	
5633	1577	1577	
5634	0211	XSK 11	

/PDP-12 CP TEST PART 2 SKIP AND DATA HANDLING MAINDEC D0AB PAL10 V141 29-OCT-69 1110 PAGE 72-1

5635 0456 SKP
5636 0000 HLT

/XSK SKIPPED ON 1977

5637	0072	SET+20+12	
5640	1377	1377	
5641	0212	XSK 12	
5642	0456	SKP	
5643	0000	HLT	/XSK SKIPPED IN ERROR A=1377
5644	0073	SET+20+13	
5645	0777	0777	
5646	0213	XSK 13	
5647	0456	SKP	
5650	0000	HLT	/XSK SKIPPED IN ERROR A=0777
5651	0074	SET+20+14	
5652	1777	1777	
5653	0214	XSK 14	
5654	0000	HLT	/XSK FAILED TO SKIP A=1777

/XSK INDEX TEST 2 XSK WILL INDEX THE B REGISTER BY ONE

5655	0061	SET+20+1	
5656	0000	0000	
5657	0221	XSK+20+1	
5660	1020	LDA+20	
5661	0001	0001	
5662	1460	SAE+20	
5663	0001	0001	
5664	0000	HLT	/XSK INDEX FAILED BIT11 AC=0001 B1=0001
5665	0062	SET+20+2	
5666	0001	0001	
5667	0222	XSK+20+2	
5670	1020	LDA+20	
5671	0002	0002	
5672	1460	SAE+20	
5673	0002	0002	
5674	0000	HLT	/XSK INDEX FAILED BIT10 AC=0002 B2=0002
5675	0063	SET+20+3	
5676	0003	0003	
5677	0223	XSK+20+3	
5700	1020	LDA+20	
5701	0004	0004	
5702	1460	SAE+20	
5703	0004	0004	
5704	0000	HLT	/XSK INDEX FAILED BIT9 AC=0004 B3=0004
5705	0064	SET+20+4	
5706	0007	0007	
5707	0224	XSK+20+4	
5710	1020	LDA+20	
5711	0010	0010	
5712	1460	SAE+20	
5713	0010	0010	
5714	0000	HLT	/XSK INDEX FAILED BIT8 AC=0010 B4=0010
5715	0065	SET+20+5	
5716	0017	0017	
5717	0225	XSK+20+5	
5720	1020	LDA+20	
5721	0020	0020	
5722	1460	SAE+20	
5723	0020	0020	
5724	0000	HLT	/XSK INDEX FAILED BIT7 AC=0020 B5=0020
5725	0066	SET+20+6	
5726	0037	0037	
5727	0226	XSK+20+6	
5730	1020	LDA+20	
5731	0040	0040	
5732	1460	SAE+20	

/PDP-12 CP TEST PART 2 SKIP AND DATA HANDLING MAINDEC DBAB PAL10 V141 29-OCT-69 1110 PAGE 74-1

5733 2040
5734 2000
0040
HLT

/XSK INDEX FAILED BIT6 AC=0040 B6=0040

5735	0067	SET+20+7	
5736	0077	0077	
5737	0227	XSK+20+7	
5740	1020	LDA+20	
5741	0100	0100	
5742	1460	SAE+20	
5743	0100	0100	
5744	0000	HLT	/XSK INDEX FAILED BIT5 AC=0100 B7=0100
5745	0077	SET+20+17	
5746	0177	0177	
5747	0237	XSK+20+17	
5750	1020	LDA+20	
5751	0200	0200	
5752	1460	SAE+20	
5753	0200	0200	
5754	0000	HLT	/XSK INDEX FAILED BIT4 AC=0200 B17=0200
5755	0076	SET+20+16	
5756	0377	0377	
5757	0236	XSK+20+16	
5760	1020	LDA+20	
5761	0400	0400	
5762	1460	SAE+20	
5763	0400	0400	
5764	0000	HLT	/XSK INDEX FAILED BIT3 AC=0400 B16=0400
5765	0075	SET+20+15	
5766	0777	0777	
5767	0235	XSK+20+15	
5770	1020	LDA+20	
5771	1000	1000	
5772	1460	SAE+20	
5773	1000	1000	
5774	0000	HLT	/XSK INDEX FAILED BIT2 AC=1000 B15=1000
5775	0002	PDP	
5776	5777	5000,+1	/JMP I ,+1
5777	6001	6001	

```
6001      *6001
           /STH TEST
           /RIGHT HALF

6001 6141      LINC
6002 1020      LDA+20
6003 5201      5201
6004 1340      STH
6005 6007      ,+2
6006 0456      SKP
6007 2500      2500
6010 1020      LDA+20
6011 2501      2501
6012 1440      SAE
6013 6007      ,=4
6014 0000      HLT                /STH FAILED AC=2501

6015 1020      LDA+20
6016 2502      2502
6017 1340      STH
6020 6022      ,+2
6021 0456      SKP
6022 5200      5200
6023 1020      LDA+20
6024 5202      5202
6025 1440      SAE
6026 6022      ,=4
6027 0000      HLT                /STH FAILED AC=5202

6030 1020      LDA+20
6031 5204      5204
6032 1340      STH
6033 6035      ,+2
6034 0456      SKP
6035 2500      2500
6036 1020      LDA+20
6037 2504      2504
6040 1440      SAE
6041 6035      ,=4
6042 0000      HLT                /STH FAILED AC=2504

6043 1020      LDA+20
6044 2510      2510
6045 1340      STH
6046 6050      ,+2
6047 0456      SKP
6050 5200      5200
6051 1020      LDA+20
6052 5210      5210
6053 1440      SAE
6054 6050      ,=4
6055 0000      HLT                /STH FAILED AC=5210
```

6056	1020	LDA+20
6057	5220	5220
6060	1340	STH
6061	6063	,+2
6062	0456	SKP
6063	2500	2500
6064	1020	LDA+20
6065	2520	2520
6066	1440	SAE
6067	6063	,=4
6070	0000	HLT

/STH FAILED AC=2520

6071	1020	LDA+20
6072	2540	2540
6073	1340	STH
6074	6076	,+2
6075	0456	SKP
6076	5200	5200
6077	1020	LDA+20
6100	5240	5240
6101	1440	SAE
6102	6076	,=4
6103	0000	HLT

/STH FAILED AC=5240

6104	1020	LDA+20
6105	5276	5276
6106	1340	STH
6107	6111	,+2
6110	0456	SKP
6111	2500	2500
6112	1020	LDA+20
6113	2576	2576
6114	1440	SAE
6115	6111	,=4
6116	0000	HLT

/STH FAILED AC=2576

6117	1020	LDA+20
6120	2575	2575
6121	1340	STH
6122	6124	,+2
6123	0456	SKP
6124	5200	5200
6125	1020	LDA+20
6126	5275	5275
6127	1440	SAE
6130	6124	,=4
6131	0000	HLT

/STH FAILED AC=5275

6132	1020	LDA+20
6133	5273	5273
6134	1340	STH
6135	6137	,+2
6136	0456	SKP
6137	2500	2500
6140	1020	LDA+20
6141	2573	2573
6142	1440	SAE
6143	6137	,=4
6144	0000	HLT

/STH FAILED AC=2573

6145	1020	LDA+20
6146	2567	2567
6147	1340	STH
6150	6152	,+2
6151	0456	SKP
6152	5200	5200
6153	1020	LDA+20
6154	5267	5267
6155	1440	SAE
6156	6152	,=4
6157	0000	HLT

/STH FAILED AC=5267

6160	1020	LDA+20
6161	5257	5257
6162	1340	STH
6163	6165	,+2
6164	0456	SKP
6165	2500	2500
6166	1020	LDA+20
6167	2557	2557
6170	1440	SAE
6171	6165	,=4
6172	0000	HLT

/STH FAILED AC=2557

6173	1020	LDA+20
6174	2537	2537
6175	1340	STH
6176	6200	,+2
6177	0456	SKP
6200	5200	5200
6201	1020	LDA+20
6202	5237	5237
6203	1440	SAE
6204	6200	,=4
6205	0000	HLT

/STH FAILED AC=5237

```

                                /LDH TEST
                                /LEFT HALF
6206 1020                      LDA+20
6207 2501                      2501
6210 1340                      STH
6211 2213                      ,+2=4000
6212 0456                      SKP
6213 0052                      0052
6214 1020                      LDA+20
6215 0152                      0152
6216 1440                      SAE
6217 6213                      ,=4
6220 0000                      HLT                                /STH FAILED AC=0001

6221 1020                      LDA+20
6222 5202                      5202
6223 1340                      STH
6224 2226                      ,+2=4000
6225 0456                      SKP
6226 0025                      0025
6227 1020                      LDA+20
6230 0225                      0225
6231 1440                      SAE
6232 6226                      ,=4
6233 0000                      HLT                                /STH FAILED AC=0002

6234 1020                      LDA+20
6235 2504                      2504
6236 1340                      STH
6237 2241                      ,+2=4000
6240 0456                      SKP
6241 0052                      0052
6242 1020                      LDA+20
6243 0452                      0452
6244 1440                      SAE
6245 6241                      ,=4
6246 0000                      HLT                                /STH FAILED AC=0004

6247 1020                      LDA+20
6250 5210                      5210
6251 1340                      STH
6252 2254                      ,+2=4000
6253 0456                      SKP
6254 0025                      0025
6255 1020                      LDA+20
6256 1025                      1025
6257 1440                      SAE
6260 6254                      ,=4
6261 0000                      HLT                                /STH FAILED AC=0010
```

6262	1020	LDA+20	
6263	2520	2520	
6264	1340	STH	
6265	2267	,+2=4000	
6266	0456	SKP	
6267	0052	0052	
6270	1020	LDA+20	
6271	2052	2052	
6272	1440	SAE	
6273	6267	,=4	
6274	0000	HLT	/STH FAILED AC=0020
6275	1020	LDA+20	
6276	5240	5240	
6277	1340	STH	
6300	2302	,+2=4000	
6301	0456	SKP	
6302	0025	0025	
6303	1020	LDA+20	
6304	4025	4025	
6305	1440	SAE	
6306	6302	,=4	
6307	0000	HLT	/STH FAILED AC=0040
6310	1020	LDA+20	
6311	2577	2577	
6312	1340	STH	
6313	2315	,+2=4000	
6314	0456	SKP	
6315	0052	0052	
6316	1020	LDA+20	
6317	7752	7752	
6320	1440	SAE	/SKIP TO SHO TEST 1
6321	6315	,=4	
6322	0000	HLT	/STH FAILED AC=7752

```

/SRO TEST 1
6323 1020 LDA+20
6324 0000 0000
6325 4327 STC ,+2=2000
6326 1520 SRO+20
6327 0000 0000
6330 0000 HLT /SRO SKIP FAILED
6331 1000 LDA
6332 6327 ,=3
6333 1460 SAE+20
6334 0000 0000
6335 0000 HLT /SRO ROTATE FAILED AC=0000

6336 1020 LDA+20
6337 4000 4000
6340 4342 STC ,+2=2000
6341 1520 SRO+20
6342 0000 0000
6343 0000 HLT /SRO SKIP FAILED
6344 1000 LDA
6345 6342 ,=3
6346 1460 SAE+20
6347 2000 2000
6350 0000 HLT /SRO ROTATE FAILED AC=2000

6351 1020 LDA+20
6352 2000 2000
6353 4355 STC ,+2=2000
6354 1520 SRO+20
6355 0000 0000
6356 0000 HLT /SRO SKIP FAILED
6357 1000 LDA
6360 6355 ,=3
6361 1460 SAE+20
6362 1000 1000
6363 0000 HLT /SRO ROTATE FAILED AC=1000

6364 1020 LDA+20
6365 1000 1000
6366 4370 STC ,+2=2000
6367 1520 SRO+20
6370 0000 0000
6371 0000 HLT /SRO SKIP FAILED
6372 1000 LDA
6373 6370 ,=3
6374 1460 SAE+20
6375 0400 0400
6376 0000 HLT /SRO ROTATE FAILED AC=04000

6377 1020 LDA+20
6400 0400 0400
6401 4403 STC ,+2=2000
6402 1520 SRO+20
6403 0000 0000
6404 0000 HLT /SRO SKIP FAILED
```

6405	1000	LDA	
6406	6403	,=3	
6407	1460	SAE+20	
6410	0200	0200	
6411	0000	HLT	/SRO ROTATE FAILED AC=0200
6412	1020	LDA+20	
6413	0200	0200	
6414	4416	STC ,+2+2000	
6415	1520	SRO+20	
6416	0000	0000	
6417	0000	HLT	/SRO SKIP FAILED
6420	1000	LDA	
6421	6416	,=3	
6422	1460	SAE+20	
6423	0100	0100	
6424	0000	HLT	/SRO ROTATE FAILED AC=0100
6425	1020	LDA+20	
6426	0100	0100	
6427	4431	STC ,+2+2000	
6430	1520	SRO+20	
6431	0000	0000	
6432	0000	HLT	/SRO SKIP FAILED
6433	1000	LDA	
6434	6431	,=3	
6435	1460	SAE+20	
6436	0040	0040	
6437	0000	HLT	/SRO ROTATE FAILED AC=0040
6440	1020	LDA+20	
6441	0040	0040	
6442	4444	STC ,+2+2000	
6443	1520	SRO+20	
6444	0000	0000	
6445	0000	HLT	/SRO SKIP FAILED
6446	1000	LDA	
6447	6444	,=3	
6450	1460	SAE+20	
6451	0020	0020	
6452	0000	HLT	/SRO ROTATE FAILED AC=0020
6453	1020	LDA+20	
6454	0020	0020	
6455	4457	STC ,+2+2000	
6456	1520	SRO+20	
6457	0000	0000	
6460	0000	HLT	/SRO SKIP FAILED
6461	1000	LDA	
6462	6457	,=3	
6463	1460	SAE+20	
6464	0010	0010	

6465	0000	HLT	/SRO ROTATE FAILED AC=0010
6466	1020	LDA+20	
6467	0010	0010	
6470	4472	STC ,+2-2000	
6471	1520	SRO+20	
6472	0000	0000	
6473	0000	HLT	/SRO SKIP FAILED
6474	1000	LDA	
6475	6472	,=3	
6476	1460	SAE+20	
6477	0004	0004	
6500	0000	HLT	/SRO ROTATE FAILED AC=0004
6501	1020	LDA+20	
6502	0004	0004	
6503	4505	STC ,+2-2000	
6504	1520	SRO+20	
6505	0000	0000	
6506	0000	HLT	/SRO SKIP FAILED
6507	1000	LDA	
6510	6505	,=3	
6511	1460	SAE+20	
6512	0002	0002	
6513	0000	HLT	/SRO ROTATE FAILED AC=0002
6514	1020	LDA+20	
6515	0002	0002	
6516	4520	STC ,+2-2000	
6517	1520	SRO+20	
6520	0000	0000	
6521	0000	HLT	/SRO SKIP FAILED
6522	1000	LDA	
6523	6520	,=3	
6524	1460	SAE+20	
6525	0001	0001	
6526	0000	HLT	/SRO ROTATE FAILED AC=0001
6527	1020	LDA+20	
6530	3776	3776	
6531	4533	STC ,+2-2000	
6532	1520	SRO+20	
6533	0000	0000	
6534	0000	HLT	/SRO SKIP FAILED
6535	1000	LDA	
6536	6533	,=3	
6537	1460	SAE+20	
6540	1777	1777	
6541	0000	HLT	/SRO ROTATE FAILED AC=1777

6542	1020	LDA+20	
6543	5774	5774	
6544	4546	STC ,+2-2000	
6545	1520	SRO+20	
6546	0000	0000	
6547	0000	HLT	/SRO SKIP FAILED
6550	1000	LDA	
6551	6246	, -3	
6552	1460	SAE+20	
6553	2776	2776	
6554	0000	HLT	/SRO ROTATE FAILED AC=6777
6555	1020	LDA+20	
6556	6774	6774	
6557	4561	STC ,+2-2000	
6560	1520	SRO+20	
6561	0000	0000	
6562	0000	HLT	/SRO SKIP FAILED
6563	1000	LDA	
6564	6561	, -3	
6565	1460	SAE+20	
6566	3376	3376	
6567	0000	HLT	/SRO ROTATE FAILED AC=
6570	1020	LDA+20	
6571	7374	7374	
6572	4574	STC ,+2-2000	
6573	1520	SRO+20	
6574	0000	0000	
6575	0000	HLT	/SRO SKIP FAILED
6576	1000	LDA	
6577	6574	, -3	
6600	1460	SAE+20	
6601	3576	3576	
6602	0000	HLT	/SRO ROTATE FAILED AC=
6603	1020	LDA+20	
6604	7474	7474	
6605	4607	STC ,+2-2000	
6606	1520	SRO+20	
6607	0000	0000	
6610	0000	HLT	/SRO SKIP FAILED
6611	1000	LDA	
6612	6607	, -3	
6613	1460	SAE+20	/SKIP TO SHD TEST 1
6614	3636	3636	
6615	0000	HLT	/SRO ROTATE FAILED AC=

```

/SHD TEST 1
6616 1020 LDA+20
6617 0010 0010
6620 1400 SHD
6621 6624 ,+3 2000
6622 0000 HLT /SHD FAILED AC=0010 MEM=0000
6623 0456 SKP
6624 0000 0000

6625 1020 LDA+20
6626 0020 0020
6627 1400 SHD
6630 6633 ,+3 2000
6631 0000 HLT /SHD FAILED AC=0020 MEM=0000
6632 0456 SKP
6633 0000 0000

6634 1020 LDA+20
6635 0040 0040
6636 1400 SHD
6637 6642 ,+3 2000
6640 0000 HLT /SHD FAILED AC=0040 MEM=0000
6641 0456 SKP
6642 0000 0000

6643 1020 LDA+20
6644 0001 0001
6645 1400 SHD
6646 6651 ,+3 2000
6647 0000 HLT /SHD FAILED AC=0001 MEM=0000
6650 0456 SKP
6651 0000 0000

6652 1020 LDA+20
6653 0002 0002
6654 1400 SHD
6655 6660 ,+3 2000
6656 0000 HLT /SHD FAILED AC=0002 MEM=0000
6657 0456 SKP
6660 0000 0000

6661 1020 LDA+20
6662 0004 0004
6663 1400 SHD
6664 6667 ,+3 2000
6665 0000 HLT /SHD FAILED AC=0004 MEM=0000
6666 0456 SKP
6667 0000 0000

6670 1400 SHD
6671 6674 ,+3 2000
6672 0000 HLT /SHD FAILED AC=0004 MEM=1000
6673 0456 SKP
6674 1000 1000
```

6675	1400	SHD	
6676	6701	,+3 2000	
6677	0000	HLT	/SHD FAILED AC=0004 MEM=2000
6700	0456	SKP	
6701	2000	2000	
6702	1400	SHD	
6703	6706	,+3 2000	
6704	0000	HLT	/SHD FAILED AC=0004 MEM=4000
6705	0456	SKP	
6706	4000	4000	
6707	1400	SHD	
6710	6713	,+3	
6711	0000	HLT	/SHD FAILED AC=0004 MEM=0040
6712	0456	SKP	
6713	0040	0040	
6714	1400	SHD	
6715	6720	,+3 2000	
6716	0000	HLT	/SHD FAILED AC=0004 MEM=0100
6717	0456	SKP	
6720	0100	0100	
6721	1400	SHD	
6722	6725	,+3 2000	
6723	0000	HLT	/SHD FAILED AC=0004 MEM=0200
6724	0456	SKP	
6725	0200	0200	
6726	1400	SHD	
6727	6732	,+3 2000	
6730	0000	HLT	/SHD FAILED AC=0004 MEM=0400
6731	0456	SKP	
6732	0400	0400	
6733	1400	SHD	
6734	6737	,+3	
6735	0000	HLT	/SHD FAILED AC=0004 MEM=0002
6736	0456	SKP	
6737	0002	0002	
6740	1400	SHD	
6741	6744	,+3	
6742	0456	SKP	
6743	0000	HLT	/SHD FAILED AC=0004 MEM=0004
6744	0004	0004	
6745	1400	SHD	
6746	6751	,+3	
6747	0000	HLT	/SHD FAILED AC=0004 MEM=0010
6750	0456	SKP	
6751	0010	0010	

6752	1400	SHD	
6753	6756	,+3	
6754	0000	HLT	/SHD FAILED AC=0004 MEM=0020
6755	0456	SKP	
6756	0020	0020	
6757	1020	LDA+20	
6760	0020	0020	
6761	1400	SHD	
6762	6765	,+3	
6763	0000	HLT	/SHD FAILED AC=0020 MEM=0000
6764	0456	SKP	
6765	0000	0000	
6766	1020	LDA+20	
6767	0040	0040	
6770	1400	SHD	
6771	6774	,+3	
6772	0000	HLT	/SHD FAILED AC=0040 MEM=0000
6773	0456	SKP	
6774	0000	0000	
6775	0011	CLR	
6776	1400	SHD	
6777	7002	,+3	
7000	0000	HLT	/SHD FAILED AC=0000 MEM=0001
7001	0456	SKP	
7002	0001	0001	
7003	1020	LDA+20	
7004	0002	0002	
7005	1400	SHD	
7006	7011	,+3	
7007	0000	HLT	/SHD FAILED AC=0002 MEM=0000
7010	0456	SKP	
7011	0000	0000	
7012	1020	LDA+20	
7013	0004	0004	
7014	1400	SHD	
7015	7020	,+3	
7016	0000	HLT	/SHD FAILED AC=0004 MEM=0000
7017	0456	SKP	
7020	0000	0000	
7021	1020	LDA+20	
7022	0010	0010	
7023	1400	SHD	
7024	7027	,+3	
7025	0000	HLT	/SHD FAILED AC=0010 MEM=0000
7026	0456	SKP	
7027	0000	0000	

/SHD TEST

7030	1020	LDA+20	
7031	5201	5201	
7032	1400	SHD	
7033	7036	,+3	
7034	0000	HLT	/SHD FAILED AC=5200 MEM=0000
7035	0456	SKP	
7036	0000	0000	
7037	1020	LDA+20	
7040	2577	2577	
7041	1400	SHD	
7042	7045	,+3	
7043	0000	HLT	/SHD FAILED AC=2577 MEM=0001
7044	0456	SKP	
7045	0001	0001	
7046	1020	LDA+20	
7047	5201	5201	
7050	1400	SHD	
7051	7054	,+3	
7052	0000	HLT	/SHD FAILED AC=5201 MEM=5200
7053	0456	SKP	
7054	5200	5200	

/LAM TEST LAM ARITHMETIC IS 2'S COMPLEMENT

7055	0011	CLR	
7056	5060	STC ,+2=2000	
7057	1220	LAM+20	
7060	0000	0000	
7061	1460	SAE+20	
7062	0000	0000	
7063	0000	HLT	/LAM FAILED AC=0000 MEM=0001 L=0
7064	1020	LDA+20	
7065	4000	4000	
7066	0261	ROL+20*1	
7067	5071	STC ,+2=2000	
7070	1220	LAM+20	
7071	0000	0000	
7072	1460	SAE+20	
7073	0001	0001	
7074	0000	HLT	/LAM FAILED AC=0001 MEM=0001
7075	1020	LDA+20	
7076	4000	4000	
7077	0261	ROL+20*1	
7100	5104	STC ,+4=2000	
7101	1020	LDA+20	
7102	0001	0001	
7103	1220	LAM+20	
7104	0000	0000	
7105	1460	SAE+20	
7106	0002	0002	
7107	0000	HLT	/LAM FAILED AC=0002
7110	1020	LDA+20	
7111	4000	4000	
7112	0261	ROL+20*1	
7113	5117	STC ,+4=2000	
7114	1020	LDA+20	
7115	0003	0003	
7116	1220	LAM+20	
7117	0000	0000	
7120	1460	SAE+20	
7121	0004	0004	
7122	0000	HLT	/LAM FAILED AC=0004
7123	1020	LDA+20	
7124	4000	4000	
7125	0261	ROL+20*1	
7126	5132	STC ,+4=2000	
7127	1020	LDA+20	
7130	0007	0007	
7131	1220	LAM+20	
7132	0000	0000	
7133	1460	SAE+20	
7134	0010	0010	

/PDP-12 CP TEST PART 2 SKIP AND DATA HANDLING MAINDEC D0AB PAL10 V141 29-OCT-69 1110 PAGE 89-1

7135 0000 HLT /LAM FAILED AC=0010

7136	1020	LDA+20	
7137	4000	4000	
7140	0261	ROL+20+1	
7141	5145	STC ,+4-2000	
7142	1020	LDA+20	
7143	0017	0017	
7144	1220	LAM+20	
7145	0000	0000	
7146	1460	SAE+20	
7147	0020	0020	
7150	0000	HLT	/LAM FAILED AC=0020

7151	1020	LDA+20	
7152	4000	4000	
7153	0261	ROL+20+1	
7154	5160	STC ,+4-2000	
7155	1020	LDA+20	
7156	0037	0037	
7157	1220	LAM+20	
7160	0000	0000	
7161	1460	SAE+20	
7162	0040	0040	
7163	0000	HLT	/LAM FAILED AC=0040

7164	1020	LDA+20	
7165	4000	4000	
7166	0261	ROL+20+1	
7167	5173	STC ,+4-2000	
7170	1020	LDA+20	
7171	0077	0077	
7172	1220	LAM+20	
7173	0000	0000	
7174	1460	SAE+20	
7175	0100	0100	
7176	0000	HLT	/LAM FAILED AC=0100

7177	1020	LDA+20	
7200	4000	4000	
7201	0261	ROL+20+1	
7202	5206	STC ,+4-2000	
7203	1020	LDA+20	
7204	0177	0177	
7205	1220	LAM+20	
7206	0000	0000	
7207	1460	SAE+20	
7210	0200	0200	
7211	0000	HLT	/LAM FAILED AC=0200

7212	1020	LDA+20	
7213	4000	4000	
7214	0261	ROL+20+1	
7215	5221	STC ,+4-2000	
7216	1020	LDA+20	
7217	0377	0377	
7220	1220	LAM+20	
7221	0000	0000	
7222	1460	SAE+20	
7223	0400	0400	
7224	0000	HLT	/LAM FAILED AC=0400
7225	1020	LDA+20	
7226	4000	4000	
7227	0261	ROL+20+1	
7230	5234	STC ,+4-2000	
7231	1020	LDA+20	
7232	0777	0777	
7233	1220	LAM+20	
7234	0000	0000	
7235	1460	SAE+20	
7236	1000	1000	
7237	0000	HLT	/LAM FAILED AC=1000
7240	1020	LDA+20	
7241	4000	4000	
7242	0261	ROL+20+1	
7243	5247	STC ,+4-2000	
7244	1020	LDA+20	
7245	1777	1777	
7246	1220	LAM+20	
7247	0000	0000	
7250	1460	SAE+20	
7251	2000	2000	
7252	0000	HLT	/LAM FAILED AC=2000
7253	1020	LDA+20	
7254	4000	4000	
7255	0261	ROL+20+1	
7256	5262	STC ,+4-2000	
7257	1020	LDA+20	
7260	3777	3777	
7261	1220	LAM+20	
7262	0000	0000	
7263	1460	SAE+20	
7264	4000	4000	
7265	0000	HLT	/LAM FAILED AC=4000
7266	1020	LDA+20	
7267	4000	4000	
7270	0261	ROL+20+1	
7271	5275	STC ,+4-2000	
7272	1020	LDA+20	
7273	7777	7777	

7274	1220	LAM+20	
7275	0000	0000	
7276	1460	SAE+20	
7277	0000	0000	
7300	0000	HLT	
7301	0472	LAE+20	
7302	0000	HLT	/LAM FAILED AC=0000

/
/COM TEST
/

7303	1020	LDA+20	
7304	5252	5252	
7305	0017	COM	
7306	1460	SAE+20	
7307	2525	2525	
7310	0000	HLT	/COM FAILED AC=2525

7311	0017	COM	
7312	1460	SAE+20	
7313	5252	5252	
7314	0000	HLT	/COM FAILED AC=5252

7315	1020	LDA+20	
7316	7777	7777	
7317	0017	COM	
7320	1460	SAE+20	
7321	0000	0000	
7322	0000	HLT	/COM FAILED AC=0000

7323	0017	COM	
7324	1460	SAE+20	
7325	7777	7777	
7326	0000	HLT	/COM FAILED AC=7777

/STC TEST

7327	1020	LDA+20	
7330	5252	5252	
7331	4000	STC+0000	
7332	0450	AZE	
7333	0000	HLT	/STC FAILED TO CLEAR AC=0000

7334	1020	LDA+20	
7335	5252	5252	
7336	1440	SAE	
7337	0000	0000	
7340	0000	HLT	/STC FAILED TO STORE PROPER NUMBER

7341	1020	LDA+20	
7342	2525	2525	
7343	5777	STC+1777	
7344	0450	AZE	
7345	0000	HLT	/STC FAILED TO CLEAR AC=0000

7346	1020	LDA+20	
7347	2525	2525	
7350	1440	SAE	
7351	1777	1777	
7352	0000	HLT	/STC FAILED TO STORE PROPER NUMBER

7353	1020	LDA+20	
7354	2525	2525	
7355	4000	STC+0000	
7356	1020	LDA+20	
7357	2525	2525	
7360	1440	SAE	
7361	0000	0000	
7362	0000	HLT	/STC FAILED TO STORE PROPER NUMBER

7363	1020	LDA+20	
7364	5252	5252	
7365	5777	STC+1777	
7366	1020	LDA+20	
7367	5252	5252	
7370	1440	SAE	
7371	1777	1777	
7372	0000	HLT	/STC FAILED TO STORE PROPER NUMBER

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7373 0011      CLR
7374 3424      ADD K2525=4000
7375 3425      ADD K2526=4000
7376 1460      SAE 20
7377 5253      5253
7400 0000      HLT          /ADD FAILED AC=5253

7401 0011      CLR
7402 3425      ADD K2526=4000
7403 3424      ADD K2525=4000
7404 1460      SAE 20
7405 5253      5253
7406 0000      HLT          /ADD FAILED AC=5253
7407 3426      ADD K0000=4000
7410 3426      ADD K0000=4000 /TO CLEAR FILE
7411 0002      PDP          /TO PMODE
7412 2230      ISZ CTR=5400+200 /ISZ CTR (RING BELL 4096 TIMES)
7413 5215      5000,+2-2400+200 /JMP ,+2
7414 5217      5000 BELL=2400+200 /JMP BELL
7415 5616      BACK, 5000,+1-2000+200 /JMP I ,+1
7416 0033      0033 /RETURN TO SECOND TEST
7417 7300      BELL, CLL CLA
7420 1231      TAD KBELL=6400+200 /TAD KBELL
7421 6046      TLS
7422 7300      CLL CLA
7423 5215      5000 BACK=2400+200 /JMP BACK
7424 2525      K2525, 2525
7425 2526      K2526, 2526
7426 0000      K0000, 0000
7427 0000      TALLY, 0
7430 0000      CTR, 0
7431 0207      KBELL, 0207
S
    
```


ADA	1100	SRO	1500
ADATST	3667	STA	1040
ADD	2000	START	0020
ADM	1140	STC	4000
AND	0000	STH	1340
AP0	0451	SXL	0400
ATR	0014	TAD	1000
AZE	0450	TALLY	7427
BACK	7415	TLS	6046
BCL	1540	XSK	0200
BCO	1640		
BELL	7417		
BSE	1600		
CLA	7200		
CLL	7100		
CLR	0011		
CML	7020		
COM	0017		
CTR	7430		
DCA	3000		
FLO	0454		
HLT	0000		
IBZ	0453		
IOT	0513		
ISZ	2000		
K0000	7426		
K2525	7424		
K2526	7425		
KBELL	7431		
KST	0415		
LAM	1200		
LAS	7604		
LDA	1000		
LDH	1300		
LINC	6141		
LZE	0452		
MUL	1240		
NOP	0016		
PDP	0002		
QAC	0005		
QLZ	0455		
ROL	0240		
ROR	0300		
RTA	0015		
RTL	7006		
SAE	1440		
SCR	0340		
SET	0040		
SETTST	4057		
SHD	1400		
SKP	0456		
SNS	0440		

ERROR

