

23

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IDENTIFICATION

PRODUCT CODE : MAINDEC-12-D8CA-D-(D)
PRODUCT NAME : KW12-~~R~~EAL TIME CLOCK DIAGNOSTIC
DATE CREATED : OCTOBER 1, 1969
AUTHOR : JAMES KELLY
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Mnemonic : KW12TST

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ABSTRACT

The KW-12 diagnostic program verifies the correct operation of the buffer preset register, the clock counter register, the clock control register, the clock enable register, the IO bus interface, and the clock input channels. The test once started halts, only in case of an error or operator intervention.

REQUIREMENTS

Storage

Locations 0--3200 in bank 0 are utilized.

Equipment

PDP-12--with KW-12 option

Program Loading

- a) If the Binary Loader is in memory, proceed to step b. Otherwise, load the binary loader into memory.
- b) Set Left Switches=7777₈
- c) Set: Right Switches=400C₈
- d) Press IO preset and start Left Switches
- e) Turn Reader on

General Description

The ability to transfer all numbers between the AC and the clock registers is thoroughly tested. All modes of the KW-12 operation are tested. The clock counter is operated at the five crystal controlled rates and at the rate of input channel 1. External KW-12 inputs are tested with the selector switch turned to line frequency. There are four test options of which one is to eliminate testing of the AD-12 fast SAM instruction which is affected by mode bit Ø of the KW-12.

Operation Procedure

- a) Load programs with binary loader
- b) Select option by setting right switches as follows:
 - 1) Bit Ø (1) suppress test completion alarm
 - 2) Bit 5 (1) suppress print pass completion printing
 - 3) Bit 8 (1) suppress test of AD-12 fast SAM instructionNormal operation on a PDP-12C is with right switches=ØØØØ
- c) Set Selector switches on KW-12 panels to line frequency.
- d) Set Left Switches=Ø2ØØ

- e) If AD-12 fast SAM instructions is to be tested, set KNOB 0 to extreme counterclockwise and KNOB 1 to extreme clockwise.
- f) Set mode key on PDP-8 mode, press ID preset, and start Left Switches.

Test Operation

After start; at location $\emptyset 2\emptyset\emptyset$ the program performs 39 tests per, pass, halting only in the case of an error. At the end of each pass, which requires approximately 30 seconds, the letter K is typed on the teletype unless suppressed by the right switch setting. If after 30 seconds the program fails to complete a pass the operator should stop the computer and check the location counter against the program listing as the program is in a counting loop which indicates a failure of the counter, the time house, or an external input channel.

After 16 complete passes of the test program, the program will cease testing and sound a distinctive whistle on the PDP-12 speaker, unless this mode is suppressed by the right switch setting.

Options:

There are 4 options available selected by the right switches.

<u>Right Switch Setting</u>	<u>Description of Option</u>
$\emptyset\emptyset\emptyset$	Tests AD-12 fast SAM prints letter <u>K</u> after every pass of program after 16 passes of program quits test and sounds completion alarm on speaker
$1\emptyset\emptyset$	Suppresses test of AD-12 fast SAM
$2\emptyset\emptyset$	Suppresses typing of <u>K</u> after every pass of program
$4\emptyset\emptyset$	Allows program to repeat indefinitely

All combinations of options are legal.

Errors

- a) Error Halts--If the computer halts check the listing for explanation of the halt.
- b) Failure of the counter time base or an external input channel can cause the program to loop indefinitely through a 2 or 3 instruction loop. If the program fails to complete a pass in approximately 30 seconds, the operator should stop the machine and check the location counter against the listing to determine if the program is waiting for a counter overflow or external input channel.

Manual Test

When the computer is halted, the run light is out, it is possible to check the advancement of the clock counter manually as follows:

- a) Set mode Switch to PDP-8 mode
- b) Set Left Switches equal to 6137
- c) Press IO preset and DO alternately

After every press of the DO Switch, the clock counter will be read into the AD? Each press of IO preset will clear the AC and advance the clock counter one or two counts. Therefore, by noting the reading of the AC after each DO, the fact that the clock counter advanced may be ascertained.

TESTS

The following--tests are performed in the order listed below:

<u>Test #</u>	<u>Description</u>
TST 20	Does AC change after a transfer to the Buffer Preset Register?
TST 21	Does the Buffer Preset Register Jam into the AC?
TST 22	Can the Buffer Preset Register be cleared to $\emptyset\emptyset\emptyset$?
TST 23	Do all numbers transfer between the AC and the Buffer Preset Register?
TST 24	Do random numbers transfer between the AC and the Buffer Preset Register?
TST 25	Does reading the Buffer Preset Register change its content?
TST 26	Can the Buffer Preset Register gate perform at maximum speed?
TST 27	Can the Buffer Preset Register survive checkerboard patterns?
TST 28	Can the Buffer Preset Register handle random complement patterns?
TST 29	Does executing the CLEN instruction affect the AC?
TST 30	Does the Buffer Preset Register change after a transfer to the clock counter register?
TST 31	Can the clock counter be read using the 6137 instruction?
TST 32	Can the clock counter be cleared?
TST 33	Do all numbers transfer between the Buffer Preset Register and the clock counter register?
TST 34	Do random numbers transfer between the Buffer Preset Register and the clock counter register?
TST 35	Does reading the clock counter register change its CONTENTS?

TST 37 Can the Buffer Preset Register be ORED into the clock counter register?

TST 38 Can the clock counter register be loaded with mode 2(Ø) in error?

TST 39 Can the clock counter be loaded with mode 1 (1) in error?

T~~A~~T 3Ø Does rapid actuating of the mode gates affect counter?

TEST 31 This is a general gate shaking test of the mode flip flops.

TEST 32 Does mode bit 2 changing from 1 Ø clear the clock counter register?

TST 4Ø Does the overflow of the clock counter register set the overflow flip flop?

TST 41A This is a general test of the overflow flip flop.

T~~E~~T 4 This is a series of tests. Labeled TST 41 through TST 49B that check each bit of the counter.

TEST 5 Does the clock counter register count at all rates?

ITSTØ1 Does input channel 1 cause a proper interrupt?

INPTØ1 This is a simulated input test for channel 3.

ITSTØ2 Does input channel 2 cause a proper interrupt?

ITSTØ3 Does input channel 3 cause a proper interrupt?

INPTØ2 This is a simulated input test for channel 2.

INPTØ3 This is a simulated input test for channel 3.

INPTØ4 This is a test of the external inputs for channels 1, 2, 3 which includes a test of the M503 schmitt triggers.

TSM This is a test of the affect of mode bit Ø(1) on the FAST sample instruction.

TSM1 Is the fast SAM instruction affected by mode bit Ø(Ø)?

TCNT1 Does IO preset clear the rate bits?

TCNT2 Does IO preset clear the overflow flip flop,
 the enable flip flops, and the mode flip flop?

TMOD1 Does Mode bit 1(1) work properly?

TMOD3 Does mode bit 1(1) and mode bit 2 (1)
 work properly?

clv

/MAINDEC 12-08 CA-D-(0)
 /SUPER KILLER FOR CLUCKS

0131	CLS#0131	
0132	CLLR#0132	
0133	CLAS#0133	
0134	CLE#0134	
0135	CLSA#0135	
0136	CLBA#0136	
0137	CLCA#0137	
0138	*1	
02 1	0213	JMP I RETURN
0224	*22	
0220	SEND,	0
0221	RXED,	3
0222	REGA,	3
0223	K0100,	0100
0224	K0100,	0100
0225	7777	M0001, -1
0226	0001	K0001, 1
0227	7776	M0022, -2
0230	0003	K0003, 0203
0231	7774	M0024, -4
0232	0007	K0007, 0207
0233	0017	K0017, 0217
0234	0037	K0037, 0237
0235	0077	K0077, 0277
0236	0177	K0177, 0177
0237	0377	K0377, 0377
0242	0777	K0777, 0777
0241	1777	K1777, 1777
0242	3777	K3777, 3777
0243	7777	K7777, 7777
0244	7770	M0010, -10
0245	7760	M0020, -20
0246	7740	M0040, -40
0247	7730	M0100, -100
0250	7600	M0200, -200
0251	7400	M0400, -400
0252	7000	M1000, -1000
0253	6000	M2000, -2000
0254	4000	M4000, -4000
0255	4000	K4000, 4000

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2475	7404	RNAL	TAA	RNA	RNAUON
2476	7405	RNA	TAA	RVA	RAVIA
2477	7406	RVA	TAA	RVA	RVA
2478	7407	RVA	TAA	RVA	RVA
2479	7408	RVA	TAA	RVA	RVA
2480	7409	RVA	TAA	RVA	RVA
2481	7410	RVA	TAA	RVA	RVA
2482	7411	RVA	TAA	RVA	RVA
2483	7412	RVA	TAA	RVA	RVA
2484	7413	RVA	TAA	RVA	RVA
2485	7414	RVA	TAA	RVA	RVA
2486	7415	RVA	TAA	RVA	RVA
2487	7416	RVA	TAA	RVA	RVA
2488	7417	RVA	TAA	RVA	RVA
2489	7418	RVA	TAA	RVA	RVA
2490	7419	RVA	TAA	RVA	RVA
2491	7420	RVA	TAA	RVA	RVA
2492	7421	RVA	TAA	RVA	RVA
2493	7422	RVA	TAA	RVA	RVA
2494	7423	RVA	TAA	RVA	RVA
2495	7424	RVA	TAA	RVA	RVA
2496	7425	RVA	TAA	RVA	RVA
2497	7426	RVA	TAA	RVA	RVA
2498	7427	RVA	TAA	RVA	RVA
2499	7428	RVA	TAA	RVA	RVA
2500	7429	RVA	TAA	RVA	RVA
2501	7430	RVA	TAA	RVA	RVA
2502	7431	RVA	TAA	RVA	RVA
2503	7432	RVA	TAA	RVA	RVA
2504	7433	RVA	TAA	RVA	RVA
2505	7434	RVA	TAA	RVA	RVA
2506	7435	RVA	TAA	RVA	RVA
2507	7436	RVA	TAA	RVA	RVA
2508	7437	RVA	TAA	RVA	RVA
2509	7438	RVA	TAA	RVA	RVA
2510	7439	RVA	TAA	RVA	RVA
2511	7440	RVA	TAA	RVA	RVA
2512	7441	RVA	TAA	RVA	RVA
2513	7442	RVA	TAA	RVA	RVA
2514	7443	RVA	TAA	RVA	RVA
2515	7444	RVA	TAA	RVA	RVA
2516	7445	RVA	TAA	RVA	RVA
2517	7446	RVA	TAA	RVA	RVA
2518	7447	RVA	TAA	RVA	RVA
2519	7448	RVA	TAA	RVA	RVA
2520	7449	RVA	TAA	RVA	RVA
2521	7450	RVA	TAA	RVA	RVA
2522	7451	RVA	TAA	RVA	RVA
2523	7452	RVA	TAA	RVA	RVA
2524	7453	RVA	TAA	RVA	RVA
2525	7454	RVA	TAA	RVA	RVA
2526	7455	RVA	TAA	RVA	RVA
2527	7456	RVA	TAA	RVA	RVA
2528	7457	RVA	TAA	RVA	RVA
2529	7458	RVA	TAA	RVA	RVA
2530	7459	RVA	TAA	RVA	RVA
2531	7460	RVA	TAA	RVA	RVA
2532	7461	RVA	TAA	RVA	RVA
2533	7462	RVA	TAA	RVA	RVA
2534	7463	RVA	TAA	RVA	RVA
2535	7464	RVA	TAA	RVA	RVA
2536	7465	RVA	TAA	RVA	RVA
2537	7466	RVA	TAA	RVA	RVA
2538	7467	RVA	TAA	RVA	RVA
2539	7468	RVA	TAA	RVA	RVA
2540	7469	RVA	TAA	RVA	RVA
2541	7470	RVA	TAA	RVA	RVA
2542	7471	RVA	TAA	RVA	RVA
2543	7472	RVA	TAA	RVA	RVA
2544	7473	RVA	TAA	RVA	RVA
2545	7474	RVA	TAA	RVA	RVA
2546	7475	RVA	TAA	RVA	RVA
2547	7476	RVA	TAA	RVA	RVA
2548	7477	RVA	TAA	RVA	RVA
2549	7478	RVA	TAA	RVA	RVA
2550	7479	RVA	TAA	RVA	RVA
2551	7480	RVA	TAA	RVA	RVA
2552	7481	RVA	TAA	RVA	RVA
2553	7482	RVA	TAA	RVA	RVA
2554	7483	RVA	TAA	RVA	RVA
2555	7484	RVA	TAA	RVA	RVA
2556	7485	RVA	TAA	RVA	RVA
2557	7486	RVA	TAA	RVA	RVA
2558	7487	RVA	TAA	RVA	RVA
2559	7488	RVA	TAA	RVA	RVA
2560	7489	RVA	TAA	RVA	RVA
2561	7490	RVA	TAA	RVA	RVA
2562	7491	RVA	TAA	RVA	RVA
2563	7492	RVA	TAA	RVA	RVA
2564	7493	RVA	TAA	RVA	RVA
2565	7494	RVA	TAA	RVA	RVA
2566	7495	RVA	TAA	RVA	RVA
2567	7496	RVA	TAA	RVA	RVA
2568	7497	RVA	TAA	RVA	RVA
2569	7498	RVA	TAA	RVA	RVA
2570	7499	RVA	TAA	RVA	RVA
2571	7500	RVA	TAA	RVA	RVA
2572	7501	RVA	TAA	RVA	RVA
2573	7502	RVA	TAA	RVA	RVA
2574	7503	RVA	TAA	RVA	RVA
2575	7504	RVA	TAA	RVA	RVA
2576	7505	RVA	TAA	RVA	RVA
2577	7506	RVA	TAA	RVA	RVA
2578	7507	RVA	TAA	RVA	RVA
2579	7508	RVA	TAA	RVA	RVA
2580	7509	RVA	TAA	RVA	RVA
2581	7510	RVA	TAA	RVA	RVA
2582	7511	RVA	TAA	RVA	RVA
2583	7512	RVA	TAA	RVA	RVA
2584	7513	RVA	TAA	RVA	RVA
2585	7514	RVA	TAA	RVA	RVA
2586	7515	RVA	TAA	RVA	RVA
2587	7516	RVA	TAA	RVA	RVA
2588	7517	RVA	TAA	RVA	RVA
2589	7518	RVA	TAA	RVA	RVA
2590	7519	RVA	TAA	RVA	RVA
2591	7520	RVA	TAA	RVA	RVA
2592	7521	RVA	TAA	RVA	RVA
2593	7522	RVA	TAA	RVA	RVA
2594	7523	RVA	TAA	RVA	RVA
2595	7524	RVA	TAA	RVA	RVA
2596	7525	RVA	TAA	RVA	RVA
2597	7526	RVA	TAA	RVA	RVA
2598	7527	RVA	TAA	RVA	RVA
2599	7528	RVA	TAA	RVA	RVA
2600	7529	RVA	TAA	RVA	RVA

D8CA-D(D)

V141 DE 12-5879

PAL14

V141

10-OCT-69

10:51 PAGE 3

2	013	R14,	6823
3	7420	K15,	7120
4	2152	R1C,	2455
5	213	K2222,	4200
6	301	K2322,	302
7	112	K0722,	702
8	1274	PNTA,	0054
9	1010	PNTB,	0059
10	1034	PNTC,	0000
11	1020	RETURN,	0
12	2100	K1224,	1030
13	2222	K9222,	5202
14	2150	K2022,	2004
15	2120	K3222,	3200
16	2127	K0620,	0220
17	2124	K7722,	7700
18	4202	K4122,	4122
19	5122	K5222,	5202
20	4125	K0650,	2202
21	420	K0620,	0220
22	350	TST27A,	TST27
23	100	TST35A,	TST35
24	0033	TST32A,	TST32
25	1011	TST38A,	TST38
26	0014	KW214,	0014
27	0004	K0624,	0004
28	2133	PNTD,	0000
29	2135	PNTE,	LOCE
30	2137	PNTF,	LOCF
31	2161	PNTG,	LOCG
32	2172	PNTH,	LOCH
33	2202	PVTI,	LOCI
34	1-32	TST49X,	TST49A
35	1-17	TST49Y,	TST49+13
36	1-10	K2310,	0010
37	1-40	K0640,	240
38	1-400	K0420,	0420
39	1030	K0500,	2500
40	5000	K6000,	6000
41	5055	K5555,	5555
42	2510	IPT04,	INPT04
43	2400	TSMA,	TSM
44	2473	TSM1A,	TSM1
45	2044	TCNT2A,	TCNT2
46	1210	TST41B,	TST41A
47	1000	K2600,	0600
48	2126	INT01,	INPT01
49	0002	K0622,	0002
50	3027	COUNTX,	COUNT
51	1062	TST31X,	TST31
52	177	*	
53	177	SKP	

D8CA-0-(b)

/M4I DEC 12-69

PAL10 V141

12-OCT-69

10105 PAGE 4

#2xx

/MAJOR START B + DE, ALPA
 /TEST 21 TEST BUFFER AND PRESET REGISTER DATA INTERCHANGE
 /CLAB#6105 AC TO CLOCK PRESET REGISTER
 /ULPA#6106 CLOCK PRESET REGISTER TO AC
 /DOES AC CHANGE AFTER A TRANSFER TO BUFFER REG?

12.6	1-51	UCA I COUNTX	
12.1	72-6	TST2x, CLA CLA	
12.2	1-22	TAD REGA	/GET A NUMBER-BINARY UPCOUNT SEQUENCE 0 THRU 7777
12.3	6133	CLAB	/LOAD BUFFER
12.4	3421	DCA RXED	/STORE WHAT WAS LEFT IN AC
12.5	1-21	TAD RXED	/FETCH IT
12.6	7541	DIA	/INVERT CONTENTS OF AC
12.7	1-22	TAD REGA	/SUBTRACT SEND
12.8	7540	SZA CLA	/EQUAL?
12.9	7542	HLT	/NO HALT CLAB CHANGED AC, EXAMINE CELL 22 FOR TEST NUMBER
12.10	2-22	ISZ REGA	/CHANGE TEST NUMBER
12.11	5214	JMP TST20+1	/DO TEST 4096 TIMES

/DOES BUFFER DATA JAM INTO THE AC

1214	72-6	TST21, CLA CLL	
1215	3224	DCA SEND	/0 SEND REG
1216	6-33	CLAB	/SET BUFFER AND PRESET REGISTER TO 0000
1217	7242	CLA CMA	/SET AC TO 7777
1218	6136	CLBA	/JAM BUFFER PRESET (0000) OVER AC (7777)
1219	3-21	UCA RXED	/SAVE AC
1220	1-21	TAD RXED	/RESTORE AC
1221	7040	SZA CLA	/DID AC BECOME (0000)?
1222	7542	HLT	/CLBA FAILED TO CLEAR THE AC
1223	2-22	ISZ REGA	
1224	5214	JMP TST21	/DO TEST 4096 TIMES

/DOES SIGNAL CLR BUF FUNCTION

1225	7240	TST22, CLA CMA	
1226	6133	CLAB	/SET BUFF#7777
1227	73-2	CLA CLL	/CLEAR AC
1228	6133	CLAB	/LOAD BUFFER TO ALL ZEROS
1229	3224	DCA SEND	/SAVE AC
1230	6136	CLBA	/READ BUFFER AND PRESET REGISTER
1231	3421	UCA RXED	/SAVE TEST VALUE
1232	1-21	TAD RXED	/RESTORE IT
1233	7542	SZA CLA	/DID BUFFER AND PRESET REGISTER GET CLEARED BY CLR CNT?
1234	7422	HLT	/CLR BUF FAILED TO CLEAR THE BUFFER
1235	2-22	ISZ REGA	/
1236	5217	JMP TST22	/DO TEST 4096 TIMES

/DO ALL NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY

1243	7311	TST23*	CLA CLL	
1244	3426	DCA	SEND	/SEND REG
1245	1622	TAD	SEND	/GET TEST NUMBER
1246	6133	CLAB		/SEND IT
1247	7212	CIA		
1248	6130	CLBA		/RETRIEVE IT
1249	3421	DCA	RXED	/SAVE IT
1250	1621	TAD	RXED	/RESTORE IT
1251	7241	CIA		/COMPLEMENT
1252	1622	TAD	SEND	/ADD TEST NUMBER
1253	7542	SZA CLA		/WERE THEY EQUAL?
1254	7542	HLT		/AC - BUFFER TO AC DATA TRANSFER FAILED
1255	2222	ISZ	SEND	/INCREMENT TEST NUMBER
1256	5455	JMP	TST23+2	/DO TEST 4096 TIMES

/DO RANDOM NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY

1261	4426	TST24*	JMS	RANDOM	/LOAD BUFFER AND PRESET REGISTER WITH A RANDOM NUMBER
1262	3422	DCA	SEND		/SAVE IT
1263	1622	TAD	SEND		/RESTORE IT
1264	6133	CLAB			/SEND IT
1265	4256	JMS	RANDOM		/LOAD THE AC WITH A RANDOM NUMBER
1266	6136	CLBA			/READ BACK RANDOM NUMBER FROM BUFFER PRESET REGISTER
1267	3421	DCA	RXED		/SAVE TEST RETURN
1268	1621	TAD	RXED		/RESTORE IT
1269	7241	CIA			/COMPLEMENT
1270	1622	TAD	SEND		/SUBTRACT TEST NUMBER
1271	7542	SZA CLA			/EQUAL?
1272	7542	HLT			/AC - BUFFER - AC DATA INTERCHANGE FAILED
1273	2222	ISZ	REGA		
1274	5451	JMP	TST24		/DO TEST 4096 TIMES

/DOES READING THE BUFFER CHANGE ITS CONTENTS

23.1	6135	TST25*	JMS	RANDOM	/GET RANDOM NUMBER
23.2	6136	DCA	SEND	SEND	/SAVE IT
23.3	6132	TAO	SEND	-	/RESTORE IT
23.4	6133	CLAB	-	-	/SEND IT
23.5	6135	JMS	RANDOM	-	/LOAD AC WITH A RANDOM NUMBER
23.6	6136	CLBA	-	-	/BRING BACK TEST NUMBER
23.7	6136	JMS	RANDOM	-	/LOAD AC WITH A RANDOM NUMBER
23.8	6136	CLBA	-	-	/READ BUFFER AGAIN
23.9	3421	DCA	RXED	-	/SAVE TEST VALUE
23.10	1421	TAO	RXED	-	/RESTORE IT
23.11	7441	CIA	-	-	/COMPLEMENT
23.12	1422	TAO	SEND	-	/SUBTRACT TEST NUMBER
23.13	7442	SZA CLA	-	-	/EQUAL
23.14	7442	HLT	-	-	/CLBA CHANGED THE CONTENTS OF THE BUFFER
23.15	2422	ISZ	REGA	-	-
23.16	5277	JMP	TST25	-	/DO TEST 4096 TIMES

/CAN THE GATES FUNCTION AT HIGH SPEED

23.17	7440	TST26*	CLA CLL	-	-
23.18	3422	DCA	SEND	-	-
23.19	1422	TAO	SEND	-	-
23.20	6133	CLAB	-	-	-
23.21	6136	CLBA	-	-	-
23.22	6133	CLAB	-	-	-
23.23	6136	CLBA	-	-	-
23.24	6133	CLAB	-	-	-
23.25	6136	CLBA	-	-	-
23.26	6133	CLAB	-	-	-
23.27	6136	CLBA	-	-	-
23.28	6133	CLAB	-	-	-
23.29	6136	CLBA	-	-	-
23.30	6133	CLAB	-	-	-
23.31	6136	CLBA	-	-	-
23.32	6133	CLAB	-	-	-
23.33	6136	CLBA	-	-	-
23.34	6133	CLAB	-	-	-
23.35	6136	CLBA	-	-	-
23.36	6133	CLAB	-	-	-
23.37	6136	CLBA	-	-	-
23.38	6133	CLAB	-	-	-
23.39	6136	CLBA	-	-	-
23.40	6133	CLAB	-	-	-
23.41	6136	CLBA	-	-	-
23.42	6133	CLAB	-	-	-
23.43	6136	CLBA	-	-	-
23.44	6133	CLAB	-	-	-
23.45	6136	CLBA	-	-	-
23.46	6133	CLAB	-	-	-
23.47	6136	CLBA	-	-	-
23.48	3421	DCA	RXED	-	-
23.49	1421	TAO	RXED	-	-
23.50	7441	CIA	-	-	-
23.51	1422	TAO	SEND	-	-
23.52	7442	SZA CLA	-	-	-
23.53	7442	HLT	-	-	/BUF FAILED TO TOGGLE AT HIGH SPEED
23.54	2422	ISZ	SEND	-	-
23.55	5321	JMP	TST26+2	-	/DO TEST 4096 TIMES

1/MAT-DEC 12-1977

D8CA-D-(D)

PAL10 V141

10-10T-69

10:55 PAGE 7

VCA THE BUFFER SURVIVE CHECKERBOARD

4311	7433	TST27A	CLAB	
4312	7442	TAC	RXED	/SAVE TEST PATTERN
4313	7441	VCA	SEND	/RESTORE IT
4314	7440	TAC	SEN	
4315	7433	VCA		
4316	7435	VCA		
4317	7440	VCA		
4318	7435	VCA		
4319	7435	VCA		
4320	7442	VCA		
4321	7442	VCA		
4322	7433	VCA		
4323	6130	VCA		
4324	7442	VCA		
4325	6133	VCA		
4326	6135	VCA		
4327	7442	VCA		
4328	6133	VCA		
4329	7433	VCA		
4330	7435	VCA		
4331	7435	VCA		
4332	7435	VCA		
4333	7440	VCA		
4334	7435	VCA		
4335	7442	VCA		
4336	6130	VCA		
4337	6133	VCA		
4338	7435	VCA		
4339	7442	VCA		
4340	7440	VCA		
4341	7433	VCA		
4342	7435	VCA		
4343	7435	VCA		
4344	7435	VCA		
4345	7442	VCA		
4346	6130	VCA		
4347	7440	VCA		
4348	3421	VCA	RXED	/SAVE FINAL PATTERN
4349	1421	TAC	RXEU	/RESTORE IT
4350	7441	VCA		/COMPLEMENT
4351	7441	TAC	SEND	/SUBTRACT TEST PATTERN
4352	7441	VCA		/EQUAL?
4353	1420	TAC	SEN	/BUFFER FAILED CHECKBOARD TEST
4354	7440	SEN	CLA	/DO TEST 4096 TIMES
4355	7442	VCA		
4356	6122	TSE	REGA	
4357	5525	VCA	TST27A	/CROSS PAGE REF TO TST27

08CA D/D

MAY DEC 12 1969

FILE# V141

LCT-CT-69

12:55 PAGE 8

/* THE BUFFER SURVIVE RANDOM COMPLEMENT PATTERNS

1000	3-04	TAD	CIA	CLAB	/GE GENERATE A RANDOM NUMBER
1001	3-05	TAD	SEND	CIA	/SAVE IT
1002	3-06	TAD	SEND	CLAB	/RESTORE IT
1003	3-07			CLAB	
1004	3-08			CIA	
1005	3-09			CLAB	
1006	3-10			CLAB	
1007	3-11			CIA	
1008	3-12			CLAB	
1009	3-13			CLAB	
1010	3-14			CIA	
1011	3-15			CLAB	
1012	3-16			CLAB	
1013	3-17			CIA	
1014	3-18			CLAB	
1015	3-19			CLAB	
1016	3-20			CIA	
1017	3-21			CLAB	
1018	3-22			CLAB	
1019	3-23			CIA	
1020	3-24			CLAB	
1021	3-25			CLAB	
1022	3-26			CIA	
1023	3-27			CLAB	
1024	3-28			CLAB	
1025	3-29			CIA	
1026	3-30			CLAB	
1027	3-31			CLAB	
1028	3-32			CIA	
1029	3-33			CLAB	
1030	3-34			CLAB	
1031	3-35			CIA	
1032	3-36			CLAB	
1033	3-37			CLAB	
1034	3-38			CIA	
1035	3-39			CLAB	
1036	3-40			CLAB	
1037	3-41			CIA	
1038	3-42			CLAB	
1039	3-43			CLAB	
1040	3-44			CIA	
1041	3-45			CLAB	
1042	3-46			CLAB	
1043	3-47			CIA	
1044	3-48			CLAB	
1045	3-49			CLAB	
1046	3-50			CIA	
1047	3-51			CLAB	
1048	3-52			CLAB	
1049	3-53			CIA	
1050	3-54			CLAB	
1051	3-55			CLAB	
1052	3-56			CIA	
1053	3-57			CLAB	
1054	3-58			CLAB	
1055	3-59			CIA	
1056	3-60			CLAB	
1057	3-61			CLAB	
1058	3-62			CIA	
1059	3-63			CLAB	
1060	3-64			CLAB	
1061	3-65			CIA	
1062	3-66			CLAB	
1063	3-67			CLAB	
1064	3-68			CIA	
1065	3-69			CLAB	
1066	3-70			CLAB	
1067	3-71	OCA	RXED		/SAVE FINAL PATTERN
1068	3-72	TAD	RXED		/RESTORE IT
1069	3-73	CIA			/COMPLEMENT
1070	3-74	TAD	SEND		/SUBTRACT TEST PATTERN
1071	3-75	SZ4 CLA			/EQUAL?
1072	3-76	SLT			/BUFFER FAILED RANDOM COMPLEMENT PATTERN
1073	3-77	IS4	REGA		
1074	3-78	JMP	TS126		/DO TEST 4096 TIMES

D8CA-D-6)

1111 DEC 12-69

PAGE 16 V141 12-OCT-69 10:55 PAGE 9

517 2-42

NP

/CLC#6134 AC TO CLOCK ENABLE REGISTER
 /REG CLR, AFFECT THE AC

521	7-42	TST24, CLL CLA	
522	7-42	CLA SEND	/CLEAR SEND REG
523	7-42	TAD SEND	/RESTORE TEST NUMBER
524	7-41	CLA RXED	/DOES CLEN AFFECT AC
525	7-41	TAD RXED	/SAVE AC
526	7-41	CIA	/RESTORE IT
527	7-40	TAD SEND	/COMPLEMENT
528	7-40	SEA CLA	/SUBTRACT TEST NUMBER
529	7-32	HLT	/EQUAL?
530	7-20	ISZ SEND	/AC TO CLOCK ENABLE REG CHANGED AC
531	5-22	JMP TST29+2	/INCREMENT TEST NUMBER

/TEST3: PRESET REGISTER AND COUNTER DATA INTERCHANGE
 /CLSA#6135 STATUS REGISTER TO AC
 /CLLR#6132 AC TO CLOCK CONTROL REGISTER

/DOES BUFFER CHANGE AFTER A TRANSFER TO THE COUNTER

534	7-62	TST30, CLL CLA	
535	3-20	CLA SEND	/CLEAR SEND REG
536	7-35	CLSA	/CLEAR STATUS
537	7-30	CLA CLL	
538	7-20	TAD SEND	/RESTORE TEST NUMBER
539	7-13	CLAB	/LOAD BUFFER PRESET REGISTER WITH A BINARY UPCOUNT NUMBER
540	7-22	CLA CLL	
541	6-32	CLLR	/STOP CLOCK, SET ALL MODES=0
542	6-23	TAD K2100	/MODE CONTROL REG BIT 2=1
543	6-132	CLLR	/SET MODE 2, ENABLING CLR LOAD CNT
544	7-20	CLA	
545	7-25	TAD K2200	/AC BIT 4=1, SIMULATE CLR OFLOW ON 6134
546	6-134	CLEN	/TRANSFER PRESET COUNT TO CLOCK COUNTER
547	7-36	CLBA	/READ THE BUFFER
548	7-21	CLA RXED	/SAVE IT
549	7-21	TAD RXED	/RESTORE IT
550	7-41	CIA	/COMPLEMENT
551	7-20	TAD SEND	/SUBTRACT TEST NUMBER
552	7-40	SEA CLA	/EQUAL?
553	7-32	HLT	/TRANSFER FROM BUFFER TO COUNTER CHANGES BUFFER
554	7-20	ISZ SEND	/INCREMENT TEST NUMBER
555	5-30	JMP TST30+2	

/MAY 1981 DEC 12-5877

PAC17 141 12-00T-69

10:55 PAGE 16

/VALUES ON INTER DATA JAM THE BUFFER AND AC
 /CLEAR CLOCK COUNTER TO PRESET REGISTER, THEN PRESET REG TO AC

z 3	5 132	TST31, S1SA	AC CLEAR STATUS
z 3	5 134	CLA CLL	/LOAD BUFFER TO 0000
z 3	5 135	CLAB	/STOP CLOCK, SET ALL MODES#0
z 3	5 132	CLLR	/SET AC 05=1
z 3	5 135	TAD K2100	/SET MODE 2#1, THEREBY CLEARING CLOCK COUNTER
z 3	5 132	CLLR	/ENABLE INTERRUPT ON OVERFLOW
z 3	5 132	CLLR	/SET AC 7777
z 3	5 134	CLEN	/SET BUFFER 7777 AND AC
z 3	5 133	CLA CMA	/READ COUNTER
z 3	5 133	CLAH	/SAVE COUNT
z 3	5 137	CLCA	/RESTORE IT
z 3	5 131	CLA RXED	/ZERO?
z 3	5 131	TAD RXED	/COUNTER FAILED TO JAM 0000 INTO 7777
z 3	5 130	SZB CLA	/DO TEST 4096 TIMES
z 3	5 132	HLT	/CROSS PAGE REFERENCE TO TST31
z 3	5 132	ISF REGA	/ZERO SEND FOR NEXT TEST
z 3	5 132	JMP I TST31X	
z 3	5 132	CLA SEND	
/DOES SIGNAL CLR CNT WORK			
z 3	5 132	TST32, S1SA	AC CLEAR STATUS
z 3	5 133	CLA CMA CLL RAR	/SET AC=3777
z 3	5 133	CLAB	/SET BUFFER TO 3777 (USE 3777 SO WE DON'T SET OVERFLOW FLOP)
z 3	5 132	CLAH	
z 3	5 133	TAD K2200	/ENABLE LOAD COUNT GATES
z 3	5 134	CLCA	/LOAD COUNTER TO 3777 (GENERATE LOAD CNT)
z 3	5 131	CLA CLL	
z 3	5 132	CLLR	/ZERO MODE 2
z 3	5 133	TAD K2100	/SET AC 05=1
z 3	5 132	CLLR	/SET MODE 2, THEREBY GENERATING "CLC CLR CNT"
z 3	5 132	CLA CLL	
z 3	5 134	CLCA	/READ THE COUNTER
z 3	5 134	TAD RXED	/SAVE IT
z 3	5 131	TAD RXED	/RESTORE IT
z 3	5 131	SZB CLA	/ZERO?
z 3	5 132	HLT	/CLR CNT FAILED TO CLEAR THE COUNTER FROM 3777 TO 0000
z 3	5 132	ISF REGA	/DO TEST 4096 TIMES
z 3	5 132	JMP I TST32A	/INDIRECT REFERENCE TO TST32

/MAT-DEC 12-1979

D8CA-D-(0)

PAL10 V141 1-MINUTE-69

10:55 PAGE 11

/DO ALL NUMBERS TRANSFER BETWEEN THE BUFFER AND COUNTER

6650	6650	TST33,	CLSA	/CLEAR STATUS
6651	7100		CLB CLL	
6652	1421		TAD SEND	/LOAD AC WITH TEST NUMBER
6653	6232		CLAB	/SET BUFFER TO TEST NUMBER
6654	7344		CLB CLL	
6655	6132		CLLR	/STOP CLOCK, SET ALL MODES=0
6656	2223		TAD X0100	/SET AC 05=1
6657	6232		CLLR	/GENERATE "CLR CNT"
6658	7212		CLB	
6659	3125		TAD K0200	/SET AC 04=1
6660	6234		CLEN	/GENERATE "LOAD CNT"
6661	6237		CLCA	/COUNTER TO AC
6662	3021		UCA RXED	/SAVE IT
6663	1421		TAD RXED	/RESTORE IT
6664	7241		CIA	/COMPLEMENT
6665	1422		TAD SEND	/SUBTRACT TEST NUMBER
6666	7042		SEA CLA	/EQUAL?
6667	7442		HLT	/BUFFER TO COUNTER DATA INTERCHANGE FAILED
6668	2420		ISZ SEND	/INCREMENT TEST NUMBER
6669	5225		JMP TST33	

/DO RANDOM NUMBERS TRANSFER BETWEEN BUFFER AND COUNTER

6671	435	TST34,	JMS RANDOM	/GET RANDOM NUMBER
6672	6133		CLAB	/LOAD BUFFER RANDOM
6673	3422		UCA SEND	/SAVE TEST NUMBER
6674	6135		CLSA	/CLEAR CLOCK STATUS
6675	7212		CLB	/CLEAR AC
6676	6132		CLLR	/STOP CLOCK, SET ALL MODES=0
6677	1423		TAD K0100	/SET AC 05=1
6678	6132		CLLR	/GENERATE "CLR CNT"
6679	7212		CLB	
6680	1420		TAD K0200	/SET AC 04=1
6681	6134		CLEN	/GENERATE "LOAD CNT"
6682	4325		JMS RANDOM	/GET RANDOM NUMBER
6683	6133		CLAB	/LOAD BUFFER RANDOM
6684	4226		JMS RANDOM	/LOAD AC RANDOM
6685	6137		CLCA	/READ COUNTER
6686	3021		UCA RXED	/SAVE TEST VALUE
6687	1421		TAD RXED	/RESTORE IT
6688	7241		CIA	/COMPLEMENT
6689	1422		TAD SEND	/SUBTRACT TEST NUMBER
6690	7042		SEA CLA	/EQUAL?
6691	7442		HLT	/BUFFER TO COUNTER RANDOM DATA INTERCHANGE FAILED
6692	2422		ISZ REGA	/DO TEST 4096 TIMES
6693	5421		JMP TST34	

12-08CA-D-(V)

/MAY 1968

HAL14

v141

15-JULY-69

10:55 PAGE 12

/USES READING THE COUNTER CHANGE ITS STATE.

2701	4000	TST30*	JMS	RANDOM	/GET RANDOM TEST NUMBER
2702	7400		CLAB		/SEND IT TO BUFFER
2703	3400		DOA	SEND	/SAVE IT
2704	6132		CLLR		/STOP CLOCK, SET ALL MODES=0
2705	1423	TAD		K2100	/SET AC 05=1
2706	2432		CLLR		/GENERATE "CLR CNT"
2707	6132		CLSA		/CLEAR CLOCK STATUS
2708	7200		CLA		
2709	1423	TAD		K2200	/SET AC 04=1
2710	6134		CLEN		/GENERATE "LOAD CNT"
2711	4205	JMS		RANDOM	/GET RANDOM NUMBER
2712	6405		CLAB		/SEND IT TO BUFFER
2713	4000	JMS		RANDOM	/GET RANDOM NUMBER
2714	4000		CLCA		/READ CLOCK COUNTER
2715	6137	JMS		RANDOM	/GET RANDOM NUMBER
2716	4006		CLAB		/SEND IT TO BUFFER
2717	6133	JMS		RANDOM	/GET RANDOM NUMBER
2718	4006		CLCA		/READ CLOCK COUNTER
2719	6137	TAD		RXED	/SAVE IT
2720	3421		TAD	RXED	/RESTORE IT
2721	7401	CIA			/COMPLEMENT
2722	5426	TAD	SEND		/SUBTRACT TEST NUMBER
2723	7640	SEA CLA			/EQUAL?
2724	7402	FLT			(CLCA) READ THE COUNTER CHANGES THE COUNTERS STATE
2725	2442	ISZ	REGA		/DO TEST 4095 TIMES
2726	5525	JMP I	TST35A		/CROSS PAGE REF TO TST35

/CALL THE RLF TO COUNTER AND COUNTER TO BUF FUNCTION AT HIGH SPEED

2732	4000	TST30*	JMS	RANDOM	/GET RANDOM NUMBER
2733	6135		CLAB		/SEND IT TO BUFFER
2734	3406		DOA	SEND	/SAVE IT
2735	7200		CLA		
2736	6132		CLLR		/STOP CLOCK
2737	1423	TAD		K2100	/SET AC 05=1
2738	6132		CLLR		/GENERATE "CLR CNT"
2739	6135		CLSA		/CLEAR CLOCK STATUS
2740	7200		CLA		
2741	1423	TAD		K2200	/SET AC 04=1
2742	6134		CLEN		/GENERATE "LOAD CNT"
2743	6137		CLCA		/READ COUNTER
2744	2442	ISZ	REGA		/DO THIS 4096 TIMES
2745	5535	JMP	TST36+3		
2746	3421	DOA	RXED		/SAVE FINAL NUMBER
2747	2421	TAD	RXED		/RESTORE IT
2748	7401	CIA			/COMPLEMENT
2749	1423	TAD	SEND		/SUBTRACT TEST NUMBER
2750	7342	SEA CLA			/EQUAL?
2751	7402	FLT			/THE BUFFER COUNTER BUFFER DATA INTERCHANGE FAILED AT HIGHSPEED

1/MAI DEC 12-77

PALIV

V141

1A-00T-69

10:55 PAGE 13

/0005 (LOAD CNT) PERFORM LOGIC OR

1711	7422	TST37X	CLA CLL	
1712	6132	CLLR		
1713	6133	TAD	K0100	/SET AC 05=1
1714	6132	CLLR		/GENERATE "CLR CNT"
1715	6132	CLSA		/CLEAR CLOCK STATUS
1716	6132	JMS	RANDOM	/GET RANDOM TEST NUMBER
1717	6133	CLAB		/LOAD BUFFER WITH A RANDOM NUMBER
1718	6132	BCA	SEND	/SAVE IT
1719	6132	TAD	K0200	/SET AC 04=1
1720	6134	CLEN		/LOAD COUNTER FROM THE BUFFER REGISTER: GENERATE "LOAD CNT"
1721	7310	CLA CLL		
1722	1-22	TAD	SEND	/GET TEST NUMBER
1723	7422	CMA		/COMPLEMENT
1724	6133	CLAB		/LOAD BUFFER WITH THE COMPLEMENT OF THE PREVIOUS NUMBER
1725	7310	CLA CLL		
1726	1-2	TAD	K0200	/SET AC 04=1
1727	6134	CLEN		/LOAD COUNTER (OR) IN COMPLEMENT OF THE FIRST NUMBER
1728	6137	CLCA		/READ COUNTER.
1729	6121	BCA	RXED	/SAVE IT
1730	1-21	TAD	RXED	/RESTORE IT
1731	7422	CMA		/CONVERT TO ALL ZEROS FOR TESTING
1732	7422	SEA CLA		/ZERO?
1733	7422	HLT		/THE (LOAD CNT) SIGNAL FAILED TO "OR" DATA INTO COUNTER
1734	2-22	ISZ	REGA	/DO TEST 4096 TIMES
1735	5012	JMP I	TST37X	/INDIRECT REF TO TST37
1736	7-22	SKP		
1737	7755	TST37X, TST37		/DEF. OF TST37X

/TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 2 (0)

1738	7422	TST35X	CLA	
1739	6133	CLAB		/CLEAR BUFFER
1740	6132	CLLR		/CLEAR ALL MODES
1741	1-23	TAD	K2100	/SET AC 05=1
1742	6132	CLLR		/GEN. "CLR CNT"
1743	6132	CLSA		/CLEAR STATUS
1744	6132	JMS	RANDOM	/GET RANDOM NUMBER
1745	6133	CLAB		/SEND IT TO BUFFER
1746	3-21	BCA	SEND	/SAVE IT
1747	6132	CLLR		/STOP CLOCK, SET ALL MODES=0
1748	1-23	TAD	K2100	/SET AC 05=1
1749	6132	CLLR		/GENERATE "CLR CNT"
1750	7223	CLA		
1751	6132	CLLR		/SET ALL MODES=0
1752	1-20	TAD	K0200	/SET AC 04=1
1753	6134	CLEN		/TRY TO GENERATE "LOAD CNT"
1754	6137	CLCA		/GET COUNTER
1755	6137	BCA	RXED	/SAVE IT
1756	3-21	TAD	RXED	/RESTORE IT
1757	1-21	SEA CLA		/WAS IT ZERO?
1758	7422	HLT		/LOAD CNT GATES FUNCTIONED WITH MODE 2=0 IN ERROR
1759	2-22	ISZ	REGA	/DO TEST 4096 TIMES

at 9.450

/MAI DEC 12 1969

PALIC V141

18-OCT-69

10:55 PAGE 14

08CA -D (D)

/TEST LOAD CNT GENERATION GATES (CUR CLOCK RATE) MODE 1(1)

1 100	4 70	TESTSK, JMS	RANDOM	/GET RANDOM NUMBER
1 101	6133	CLAB		/SEND IT TO BUFFER
1 102	3420	ODA	SEND	/SAVE IT
1 103	1195	TAD	K0200	/SET AC 04,05=1
1 104	6132	CLLR		/GENERATE "CLR CNT", SET MODE 1 AND 2 =1
1 105	6135	CLSA		/CLEAR CLOCK STATUS
1 106	7422	CLA		/CLEAR AC
1 107	1102	TAD	K2200	/SET AC 04=1
1 108	6134	CLRY		/TRY TO GENERATE "LOAD CNT"
1 109	6137	CLCA		/READ COUNTER
1 110	3421	ODA	RXED	/SAVE TEST VALUE
1 111	1021	TAD	RXED	/RESTORE IT
1 112	7640	SZA CLA		/ZERO?
1 113	7422	HLT		/LOAD CNT GATES FUNCTIONED WITH MODE 1=1 IN ERROR
1 114	6132	ISZ	REGA	/DO TEST 4096 TIMES
1 115	5240	JMP	TST39	

/GLITCH TEST OF LOAD CNT GATES

1 100	4 70	TESTSK, JMS	RANDOM	/GET RANDOM NUMBER
1 101	6133	CLAB		/SEND IT TO BUFFER
1 102	3420	ODA	SEND	/SAVE IT
1 103	1195	TAD	K0200	/SET AC 04=1
1 104	6132	CLLR		/SET MODE 1=1
1 105	7640	CLA		/CLEAR AC
1 106	1146	TAD	K0300	/SET AC 04,05=1
1 107	6132	CLLR		/SET MODE 2=1
1 108	7640	CLA		
1 109	2022	ISZ	REGA	/DO THIS 4096 TIMES
1 110	5240	JMP	-7	
1 111	6137	CLCA		/READ COUNTER
1 112	5241	ODA	RXED	/SAVE IT
1 113	1021	TAD	RXED	/RESTORE IT
1 114	7640	SZA CLA		/ZERO?
1 115	7422	HLT		/THE MODE REGISTER CAUSES ILLEGAL LOAD COUNTER

08CA

D-(D)

/MAT DEC 12-1977

PAGE: v141

17-0CT-69

10:55 PAGE 15

GENERAL GATE SHIFTING TEST OF THE MODE FLIP FLOPS

1110	4 23	TEST31, AND	SEND IT	/GET RANDOM NUMBER
1111	1-23	CLA	RXED	/SEND IT TO BUFFER
1112	3-26	CLA	SEND	/SAVE IT
1113	1-22	CLA	REDA	/GET TEST COUNTER
1114	4 1-3	RTL		/ROTATE TWO LEFT
1115	2 1-3	RTL		/ROTATE TWO LEFT
1116	3 1-3	RTL		/ROTATE TWO LEFT
1117	0 1-7	AND	K2700	/INSURE THAT MODE 0,1,2=1
1118	2-32	CLEAR		/SEND RANDOM NUMBER TO CONTROL REGISTER
1119	7-40	CMA		/COMPLEMENT
1120	1-17	AND	K2702	/INSURE THAT MODE 0,1,2=1
1121	5-32	CLEAR		/SET TO COMPLEMENT OF THE NUMBER
1122	2-22	ISZ	REGA	/DO THIS 4096 TIMES
1123	5 1-3	UMP	TEST31+3	
1124	2-36	CLSA		/GET TEST VALUE FROM BUFFER
1125	0-21	CLA	RXED	/SAVE IT
1126	1-21	TAG	RXED	/RESTORE IT
1127	7-41	CLA		/COMPLEMENT
1128	1-26	TAG	SEND	/SUBTRACT TEST NUMBER
1129	2-40	SZA CLA		/EQUAL?
1130	7-42	HLT		/BUFF CHANGED IN ERROR
1131	0-37	CLOA		/READ COUNTER
1132	3-21	CLA	RXED	/SAVE IT
1133	1-21	TAG	RXED	/RESTORE IT
1134	2-40	SZA CLA		/STILL ZERO?
1135	7-42	HLT		/COUNTER CHANGED IN ERROR

8CA -D-6)

/MAI-DEC 19-1971

PAL16 V141 17-OCT-69

10:55 PAGE 16

/GOES MODE 2 1-0 CLK CNT?

1132 7425 TST52, JNS HANJUM /GET RANDOM NUMBER
 1133 7423 CLAB /SEND IT TO BUFFER
 1134 7420 CLA SENJ /SAVE IT
 1135 7432 CLLR /ZERO MODE 2
 1136 7423 TAD K0100 /AC 05=1
 1137 7432 CLER /GENERATE "CLR CNT"
 1138 7420 CLA /CLEAR AC
 1139 7425 TAD K2200 /SET AC 04=1
 1140 7424 CLEN /GENERATE "LOAD CNT"
 1141 7420 CLA /2 MODE 2
 1142 7424 CLER /READ COUNTER
 1143 7420 CLCA /SAVE IT
 1144 7432 CLLR /CLEAR BUF OR OVERFLOW WILL RELOAD CNT
 1145 7427 CLCA RXED
 1146 7421 CLA RXED /RESTORE IT
 1147 7433 CLAB RXED /COMPLEMENT
 1148 7421 TAD RXED /SUBTRACT TEST NUMBER
 1149 7420 CLA SENJ /EQUAL?
 1150 7420 SZA CLA /MODE 2 0-1 DID IT
 1151 7422 HLT
 1152 7423 TAD K0100 /SET AC 05=1
 1153 7432 CLLR /GENERATE "CLR CNT"
 1154 7427 CLCA /READ COUNTER
 1155 7421 CLA RXED /SAVE IT
 1156 7421 TAD RXED /RESTORE IT
 1157 7420 CLA SENJ /ZERO?
 1158 7421 SZA CLA /MODE 2 0-1 FAILED
 1159 7422 HLT
 /TEST 41 TEST OF SKIP OVERFLOW AND INTERRUPT
 /
 /GOES COUNTER OVERFLOW SET OVERFLOW FLOP
 /

1160 7420 NOP
 1161 7420 NOP
 1162 7420 NOP
 1163 7422 TST42, CLA CLL /CLEAR STATUS
 1164 7422 CLLR /SET AC 05=1
 1165 7423 TAD K0100 /0 TO COUNTER
 1166 7422 CLLR /CLEAR CLOCK STATUS
 1167 7422 CLSA /SET AC=4000
 1168 7430 CLA CLL CML RAR /SET BUFFER TO 4000
 1169 7423 CLAB /CLEAR ALL MODES
 1170 7422 TAD K2200 /LOAD CNT (00)=1; 1 TO OVERFLOW
 1171 7423 CLER /SET AC 05=1
 1172 7420 CLA CLL /GEN "CLR CNT"
 1173 7420 CLAB /GET STATUS OF CLOCK
 1174 7422 CLA CLL /OVERFLOW NOT SET
 1175 7422 CLAB
 1176 7422 CLA CLL
 1177 7423 TAD K0100
 1178 7423 CLEN
 1179 7420 CLA CLL
 1180 7420 CLAB
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PROJECT REFILE 10-1912

3211	222	152
3212	5024	122
3213	7422	222
3214	5024	122
3215	7422	222
3216	5024	122
3217	222	152

25213	7-22	25214	7-22
25215	7-22	25216	7-22

1821 2122 1822 2213 1823 2314

12-DBCH-B-13 PAGE 16-1 10-OCT-69 V141 PA-12

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1 MAI 5 DEG ← 2832 PAL10 V141 12-OCT-69 10:55 PAGE 17

```

1215 7400 NOR
1216 7500 /DUES CLSA (6135) CLEAR OVERFLOW FLOP
1217 6132 TST41A, CLA CLL
1218 6132 CLLR
1219 1023 TAD K2100 /CLEAR ALL MODES
1220 6132 CLLR
1221 6132 /GEN "CLR CNT"
1222 6135 CLSA
1223 7330 CLA CLL CMY RAR
1224 6133 CLAB /CLEAR CLOCK STATUS
1225 7300 CLA CLL
1226 1125 TAD K2200 /SET BUF=4000 OCTAL
1227 6134 OLEN
1228 7320 CLA CLL
1229 6133 CLAB
1230 6132 CLLR
1231 1023 TAD K2100 /ZERO BUF.
1232 6132 /CLEAR ALL MODES
1233 1023 CLLR
1234 6132 TAD K2100 /SET AC 05=1
1235 7300 CLA CLL
1236 6135 CLSA /GEN "CLR CNT"
1237 7300 CLA CLL
1238 6135 CLSA /GET STATUS BIT 0=1
1239 7710 SPA CLA /GET STATUS BIT 0=0
1240 7402 HLT /CLSA FAILED TO CLEAR OVERFLOW FLOP

/
/TEST OVERFLOW SKIP
/
1243 7300 CLA CLL
1244 6132 CLLR
1245 1023 TAD K2100 /CLEAR ALL MODES
1246 6132 CLLR
1247 6135 CLSA /SET AC 05=1
1248 7330 CLA CLL CMY RAR
1249 6133 CLAB /GEN "CLR CNT"
1250 7300 CLA CLL
1251 1105 TAD K2200 /CLEAR CLOCK STATUS
1252 6134 OLEN
1253 7300 CLA CLL /SET BUF=4000 OCTAL
1254 6133 CLAB
1255 7300 CLLR
1256 6133 CLAB /GEN LOAD CNT
1257 6132 CLLR
1258 1023 TAD K2100 /CLR BUF,
1259 6132 CLLR /CLEAR ALL MODES
1260 1023 TAD K2100 /AC 05=1
1261 6132 CLLR /GEN "CLR CNT"
1262 7300 CLA CLL
1263 6131 CLSK
1264 7412 SKP
1265 7402 HLT /CLOCK PRESET DIDN'T 0 OVERFLOW ENAB

```

/TEST FOR NO INTERRUPT

1255	1210	TAD	PNTA
1257	0-10	LDA	RETURN
1270	0-14	104	
1271	7400	NOP	
1272	0012	IOP	
1273	7410	SKP	
1274	7422	LDA#1	HLT

/ILLEGAL INTERRUPT OVERFLOW=1 OVERFLOW ENABLE=0

/SET INT ENABLE

1272	1223	TAD	K0100
1275	C134	CLN	
1277	7300	CLA CLL	
1300	6131	CLSK	
1301	7402	HLT	

/TURN ON CLOCK OVERFLOW INT

/CLSK FAILED TO SKIP OVERFLOW=1 EN OVF INT=1

/TEST FOR CLOCK INTERRUPT

1302	1211	TAD	PNTB
1303	3213	LDA	RETURN
1304	6021	10n	
1305	7000	NOP	
1306	6002	IOP	
1307	7402	HLT	

/CLOCK INT FAILED TO INTERRUPT

12-08CA-D-(D)

/MAINDEC 44-874

PAL10 V141

10-OCT-69

10:55 PAGE 19

/TEST WITH FLAG UP ZERO OVERFLOW INT ENABLE

1314 7400 LOOC, CLA CLL
1311 6134 OLEN
1312 6131 CLSK
1313 7417 SKP
1314 7402 HLT

/OVERFLOW ENABLE WON'T ZERO

19-055-47

7.50

/TEST WITH FLAG ZERO OVERFLOW SET

1315 1125 TAD K0100
1316 6134 OLEN
1317 7320 CLA CLL
1318 6132 CLLR
1319 6132 CLSA /STOP THE CLOCK
1320 7320 CLA CLL /READ AND ZERO FLAG
1321 6131 CLSK
1322 7417 SKP
1323 7402 HLT

/BAD INTERRUPT CONDITION STILL EXISTS

/TEST INT OVERFLOW#2

1326 1112 TAD PNTC
1327 3115 DCA RETURN
1328 6001 ION
1329 7000 NOP
1330 6402 IOF
1331 7410 SKP
1332 7422 LOOC, HLT /ILLEGAL CLOCK INTERRUPT
1333 2222 ISZ REGA /DO INTERRUPT TEST 4096 TIMES
1334 5555 JMP I TST41B /CROSS PAGE REF TO TST41A

12-B8CA-D-(D)

/MAT/DEC 12-829

PAL10

V141

19-OCT-69

10:55 PAGE 20

/

/TEST4: COUNTER CARRY TESTING

/COUNTER RESET SUCH THAT CLOCK CNT RAISES BIT IN QUESTION

/DOES BIT 11 SET UP

1337	7200	CLA	
1340	6132	CLLR	/CLEAR ALL MODES
1341	6133	CLAB	/CLEAR BUF
1342	1023	TAD K100	/SET AC 05=1
1343	6132	CLLR	/GEN "CLR CNT"
1344	6133	CLSA	/CLEAR STATUS
1345	7222	CLA	
1346	3022	DCA REGA	
1347	3022	DCA SEND	
1350	6133	CLAB	
1351	1035	TAD K2000	/MODE 1 100 HZ RATE
1352	6134	CLEN	
1353	7002	CLA CLL	
1354	1024	TAD K5100	
1355	6132	CLLR	
1356	6137	CLCA	/READ COUNTER
1357	3021	DCA RXED	
1358	1021	TAD RXED	
1361	1029	TAD M0001	
1362	7050	SNA CLA	
1363	5357	JMP ,+4	
1364	2022	1SE REGA	
1365	5356	JMP ,-7	/WAIT SOME MORE
1366	7022	HLT	/BIT 11 FAILED TO GET SET BY A CLOCK PULSE

/DOES BIT 10 SET UP

1367	7200	CLA	
1370	6132	CLLR	
1371	6133	CLAB	
1372	1023	TAD K0100	
1373	6132	CLLR	
1374	6133	TST41, CLSA	
1375	7200	CLA	
1376	3022	DCA REGA	
1377	1026	TAD K0001	
1400	6133	CLAB	
1401	3020	DCA SEND	
1402	1025	TAD K0200	
1403	6134	CLEN	
1424	7000	CLA CLL	
1425	1024	TAD K5100	
1426	6132	CLLR	
1427	6137	CLCA	
1428	3021	DCA RXED	
1429	1021	TAD RXED	
1432	1027	TAD M0002	
1433	7050	SNA CLA	
1434	5220	JMP ,+4	

MAIN INDEX ~~46-3447~~ PAL16 V141 10-OCT-69 10:55 PAGE 20-1

/BIT 16 FAILED TO GET SET BY COUNTING

$$x^* = \left\{ \begin{array}{ll} 0 & \text{if } x \in \Omega \setminus \overline{\Omega_0} \\ \frac{1}{2} & \text{if } x \in \Omega_0 \end{array} \right.$$

Figure 1. The effect of the number of nodes on the performance of the proposed method.

/BIT # FILED TO GET SET BY COUNTING

WCOES 811 SET 10

12 - 6824 - C - (CD) /MALES 30-39 46-55 114-124 0.142 0.142 1.00-1.69

12-0000000000000000
12-0000000000000000

PAL13 V141 10-001-69 10:55 PAGE 21-1

152 HE94

411 41P

411 41P

411 41P

411 41P

411 41P

411 41P

/811 & FAILED TO GET SET BY COUNTING

WCOES E11 5 SET 6

/BIT ? FILED TO GET SET BY COUNTING

1	2522	7-22
2	2531	7-22
3	2532	7-22
4	2533	7-22
5	2534	7-22
6	2535	7-22
7	2536	7-22
8	2537	7-22
9	2538	7-22
10	2539	7-22
11	2540	7-22
12	2541	7-22
13	2542	7-22
14	2543	7-22
15	2544	7-22
16	2545	7-22
17	2546	7-22
18	2547	7-22
19	2548	7-22
20	2549	7-22
21	2550	7-22
22	2551	7-22
23	2552	7-22
24	2553	7-22
25	2554	7-22
26	2555	7-22
27	2556	7-22
28	2557	7-22
29	2558	7-22
30	2559	7-22
31	2560	7-22
32	2561	7-22
33	2562	7-22
34	2563	7-22
35	2564	7-22
36	2565	7-22
37	2566	7-22
38	2567	7-22
39	2568	7-22
40	2569	7-22
41	2570	7-22
42	2571	7-22
43	2572	7-22
44	2573	7-22
45	2574	7-22
46	2575	7-22
47	2576	7-22
48	2577	7-22
49	2578	7-22
50	2579	7-22
51	2580	7-22
52	2581	7-22
53	2582	7-22
54	2583	7-22
55	2584	7-22
56	2585	7-22
57	2586	7-22
58	2587	7-22
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60	2589	7-22
61	2590	7-22
62	2591	7-22
63	2592	7-22
64	2593	7-22
65	2594	7-22
66	2595	7-22
67	2596	7-22
68	2597	7-22
69	2598	7-22
70	2599	7-22
71	2600	7-22
72	2601	7-22
73	2602	7-22
74	2603	7-22
75	2604	7-22
76	2605	7-22
77	2606	7-22
78	2607	7-22
79	2608	7-22
80	2609	7-22
81	2610	7-22
82	2611	7-22
83	2612	7-22
84	2613	7-22
85	2614	7-22
86	2615	7-22
87	2616	7-22
88	2617	7-22
89	2618	7-22
90	2619	7-22
91	2620	7-22
92	2621	7-22
93	2622	7-22
94	2623	7-22
95	2624	7-22
96	2625	7-22
97	2626	7-22
98	2627	7-22
99	2628	7-22
100	2629	7-22
101	2630	7-22
102	2631	7-22
103	2632	7-22
104	2633	7-22
105	2634	7-22
106	2635	7-22
107	2636	7-22
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109	2638	7-22
110	2639	7-22
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112	2641	7-22
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115	2644	7-22
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117	2646	7-22
118	2647	7-22
119	2648	7-22
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121	2650	7-22
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124	2653	7-22
125	2654	7-22
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127	2656	7-22
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129	2658	7-22
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138	2667	7-22
139	2668	7-22
140	2669	7-22
141	2670	7-22
142	2671	7-22
143	2672	7-22
144	2673	7-22
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146	2675	7-22
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271	2800	7-22
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403	2932	7-22
404	2933	7-22
405	2934	7-22
406	2935	7-22
407	2936	7-22
408	2937	7-22
409		

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ALL INFORMATION CONTAINED
HEREIN IS UNCLASSIFIED
DATE 10-12-2012 BY SP2

20:55 PAGE 22-1
12-00169 1141 PAL13 PEGE 22-1
/AII 6 FAILED TO GET SET BY COUNTING

AF 130 5 110 230 A

18-1030-14 18-1030-14 18-1030-14 18-1030-14 18-1030-14

REGA	ISL	15252
*+4	USA	15253
SNA	CLIA	15254
REGC	REGC	15255
TAB	REGC	15256
REGD	REGD	15257
REGE	REGE	15258
REGF	REGF	15259
REGG	REGG	15260
REGH	REGH	15261
REGI	REGI	15262
REGJ	REGJ	15263
REGK	REGK	15264
REGL	REGL	15265
REGM	REGM	15266
REGN	REGN	15267
REGO	REGO	15268
REGP	REGP	15269
REGQ	REGQ	15270
REGR	REGR	15271
REGS	REGS	15272
REGT	REGT	15273
REGU	REGU	15274
REGV	REGV	15275
REGW	REGW	15276
REGX	REGX	15277
REGY	REGY	15278
REGZ	REGZ	15279
REGA	REGA	15280
REGB	REGB	15281
REGC	REGC	15282
REGD	REGD	15283
REGE	REGE	15284
REGF	REGF	15285
REGG	REGG	15286
REGH	REGH	15287
REGI	REGI	15288
REGJ	REGJ	15289
REGK	REGK	15290
REGL	REGL	15291
REGM	REGM	15292
REGN	REGN	15293
REGO	REGO	15294
REGP	REGP	15295
REGQ	REGQ	15296
REGR	REGR	15297
REGS	REGS	15298
REGT	REGT	15299
REGU	REGU	15300
REGV	REGV	15301
REGW	REGW	15302
REGX	REGX	15303
REGY	REGY	15304
REGZ	REGZ	15305

CF 135 + 118 5300

/SIT 5 FAILED TO GET SET BY COUNTING

1513 7112

HLT

/S11 A FILED TO GET SET BY COUNTING

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10:55

PAGE 23-1

12-1001-69

V141

PAL10

MAI SEC 42-423

11 - DECEMBER 1969

(A)

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12 1591-L-10

/MAY DEC 22-1977

PAUL

V141

10-MOT-69

10:45 PAGE 24

/NODES BIT 3 SET UP

1650	7200	CLA
1651	6132	CLLR
1652	6133	CLAB
1653	1-23	TAD K0100
1654	6132	CLLR
1655	6133	TST48, CLSA
1656	7200	CLA
1657	6132	DCA REGA
1658	1-37	TAD K2377
1659	6133	CLAB
1660	3-22	DCA SEND
1661	1172	TAD K0200
1662	6134	CLEN
1663	7200	CLA CLL
1664	1-24	TAD K5110
1665	6132	CLLR
1666	6133	CLCA
1667	3021	DCA RXED
1668	1-21	TAD RXED
1669	1-21	TAD M2A00
1670	7050	SNA CLA
1671	567-	JMP +44
1672	2422	ISZ REGA
1673	5655	JMP -7
1674	7422	HLT

/BIT 3 FAILED TO GET SET BY COUNTING

/NODES BIT 2 SET UP

1675	7200	CLA
1676	6132	CLLR
1677	6133	CLAB
1678	1-23	TAD K0100
1679	6132	CLLR
1680	6133	TST49, CLSA
1681	7200	CLA
1682	3422	DCA REGA
1683	1-21	TAD K2377
1684	6133	CLAB
1685	3020	DCA SEND
1686	1160	TAD K0200
1687	6134	CLEN
1688	7200	CLA CLL
1689	1-24	TAD K5110
1690	6132	CLLR
1691	6133	CLCA
1692	3-22	DCA RXED
1693	1-21	TAD RXED
1694	1-22	TAD M1000
1695	7050	SNA CLA
1696	5241	JMP I TST49X
1697	2422	ISZ REGA

/CROSS TO TST49X
/BACK TO TST49+13

/MAIL:DEC 28-1969
12-1624 • C-10
2735 53-2 PAL12 V141 10:55 PAGE 24-1
2735 53-2 JAP 1 15149Y
/S1T 2 FAILED TO GET SET BY COUNTING

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/SIT 1 FILED TO GET SET BY COUNTING

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2025 RELEASE UNDER E.O. 14176

2025 RELEASE UNDER E.O. 14176
D- (D)

HLT

12-001-69

V141

10155 PAGE 25-1

/BIT # FILED TO GET SET BY COUNTING

12- DEC A. D- (D)

PALIN V141 12- OCT-69

10:55 PAGE 26

/ TESTER DOES COUNTER COUNT NORMALLY AND AT ALL RATES
/
/ IN ALL COUNT RATES FUNCTIONS

212	1-24	TAD	K1000	
213	2-32	CLLR		/SET 400KC RATE
214	7-30	CLA CLL		
215	6-35	CLSA		/READ STATUS
216	7-30	SMA CLA		
217	5-15	JMP	,+2	/WAIT FOR OVERFLOW
220	1-16	TAD	K2000	
221	5132	CLLR		
222	7320	CLA CLL		/SET 100KC RATE
223	6130	CLSA		
224	7120	SMA CLA		
225	5223	JMP	,+2	/WAIT FOR OVERFLOW
226	1-17	TAD	K5000	
227	5132	CLLR		/SET 10KC RATE
228	7000	CLA CLL		
229	6135	CLSA		
230	7120	SMA CLA		
231	5231	JMP	,+2	
234	1220	TAD	K7700	/PRESET THE CLOCK
235	6203	CLAB		/FOR 100 CPS TEST
236	7200	CLA		
237	1-21	TAD	K4100	/SET 1KC RATE
238	6132	CLLR		
239	7320	CLA CLL		
240	6-35	CLSA		
241	7-30	SMA CLA		
242	5-242	JMP	,+2	
245	1024	TAD	K5100	/SET 100 CPS RATES
246	5132	CLLR		
247	7320	CLA CLL		
248	6135	CLSA		
249	7-20	SMA CLA		
250	5250	JMP	,+2	
253	7000	CLA CLL		
254	1124	TAD	K8020	/SET AC 07=1
255	5134	OLEN		/ENABLE INPUT CHAN1
256	7-20	CLA		
257	1147	TAD	K6000	/SET INPUT RATE CHAN1=60HZ
258	6132	CLLR		
259	7320	CLA CLL		
260	6135	CLSA		
263	7-20	SMA CLA		
264	5252	JMP	,+2	

/ SET INPUT CHAN 1 INTERRUPT CHAN 1

/

2152	1-03	ITST 1, TAU	P070	
2155	3-23	JCA	RETURN	/SET UP INTERRUPT RETURN
2157	2-23	TAQ	K0060	/ENABLE INPUT AND INTERRUPT
2170	5-24	CLEV		
2171	5-32	CLR		/SIMULATE INPUT CHANNEL ONE
2172	6-11	TOV		/WAIT
2173	7-02	OP		/NO INTERRUPT ERROR
2174	74-2	ALT		
2175	81-4	LOCO,	AND K0020	/CLEAR INTERRUPT ENABLE SET SIMULATE INPUT
2175	6134	CLEV		
2177	7002	CLA CLL		
2180	1134	TAQ	P07E	
2181	3113	JCA	RETURN	
2182	6-11	TOV		
2183	6-03	CLSA		/CLEAR CLOCK STATUS
2184	7610	SKP CLA		
2185	7572	LOCE,	ALT	/INTERRUPT IN ERROR

/TEST INPUT CHANNEL INTERRUPT CHAN 3

2111 1-51 1TSTS, TAU PNTI
2113 3113 DCA RETURN /SET UP INTERRUPT RETURN
2114 1430 TAU K2V43
2115 6124 CLEN
2116 5412 CLLR
2117 0404 IDN /WAIT
2118 7413 NOP /NO INTERRUPT
2119 7402 HLT

2170 0-20 LOCH, AND K2W21 /CLEAR INTERRUPT ENABLE
2173 6134 CLEN
2174 7360 CLA CLL
2175 1245 TAU PNTI
2176 3115 DCA RETURN
2177 5411 IDN /CLEAR CLOCK STATUS
2178 0-30 CLSA

2211 7610 SKP CLA
2212 7162 LOCH, HLT /INTERRUPT IN ERROR

12-5616 - L - (L)
/MAI/DEC 42-9477

PA-1 V141

12-OCT-69

10:55 PAGE 30

/
/SIM INPUT TESTS CHAN 2
/

2213	7000	..OP	
2214	7000	NOP	
2215	7000	NOP	
2216	6000	10F	/INT OFF
2217	7000	NOP	
2218	7000	NOP	
2219	7000	NOP	
2220	7000	NOP	
2221	7000	NOP	
2222	7000	NOP	
2223	7000	NOP	
2224	7000	NOP	
2225	7000	NOP	
2226	7000	NOP	
2227	7000	NOP	
2228	7000	NOP	
2229	7000	NOP	
2230	7000	NOP	
2231	7000	NOP	
2232	1100	INPT#2, TAD	K0014
2233	6100	CLEN	/ENABLE CHAN 2
2234	6100	CLLR	/SET EVENT FLOP
2235	7000	NOP	
2236	7000	NOP	
2237	7000	NOP	
2238	7000	NOP	
2239	6100	CLLR	/SET PREVENT FLOP
2240	7000	CLA	
2241	7000	CLL	
2242	7000	NOP	
2243	6100	CLEN	
2244	6100	CLSA	
2245	3000	DCA	SEND
2246	6100	CLSA	
2247	8100	AND	K0014
2248	3000	DCA	RXED
2249	1000	TAD	RXED
2250	7000	SZA CLA	
2251	7000	HLT	/CLSA DOESN'T 0 INPUT CHANNEL
2252	1000	TAD	SEND
2253	7000	CIA	
2254	1000	TAD	K0014
2255	7000	SZA CLA	/SUBTRACT SET
2256	7000	HLT	
2257	7000	REGA	/BOTH PRE-EVENT AND EVENT NOT SET
2258	2000	ISZ	REGA
2259	5000	JMP	INPT#2

/
/SI* INPUT TESTS CHAN 1
/
2203 1124 INPT03, TAO K0020
2204 6134 CLE
2207 6132 CLLR /SET EVENT FLOP
2208 7400 NOP
2209 7401 NOP
2210 7400 NOP
2205 7400 NOP
2204 6132 CLLR /SET PREVENT FLOP
2203 7200 CLA
2206 7100 CLL
2207 7400 NOP
2200 6134 CLEN
2201 6130 CLSA
2202 3620 DCA SEND
2203 6135 CLSA
2204 0123 AND KR050
2205 3621 DCA RXED
2206 1021 TAO RXED
2207 7640 SZA CLA
2300 7402 HLT /CLSA DOESN'T @ INPUT CHANNEL

2301 1024 TAO SEND
2302 7041 CIA
2303 1123 TAO K0060 /SUBTRACT SET
2304 7640 SZA CLA
2305 7502 HLT /BOTH PRE-EVENT AND EVENT NOT SET
2306 7640 NOP
2307 7000 NOP
2308 7600 NOP
2311 2022 ISZ REGA /DO TEST 4096 TIMES
2312 5714 JMP I .+2 /INDIRECT REF. TO INPT03
2313 7410 SKP
2314 2255 INPT03

/TEST OF INPUT CHANNEL #3

/REGS OF CHAN1,CHAN2,CHAN3 SET TO LINEFREQ

2320	5-22	L8PT04, CLSA	/CLEAR STATUS
2321	7-22	CLA CLL	
2322	6-32	CLLR	/CLEAR ALL MODES
2323	2-33	TAU K0013	
2324	6134	CLEN	/ENABLE CHAN3 INPUT AND INTER.
2325	7222	CLA	
2326	6131	CLSK	/SKIP ON CLOCK INTER.
2327	5222	JMP ,+2	/WAIT
2328	6233	CLSA	/GET CLOCK STATUS
2329	3421	DCA RXE0	/SAVE IT
2330	1221	TAU RXE0	/RESTORE IT
2331	7241	CLA	
2332	1151	TAU K0022	
2333	7-140	SZA CLA	
	7-12	HLT	/INTERRUPT BUT CHAN 1 /EVENT FLOP NOT SET

/TEST OF INPUT CHANNEL 2

2334	6135	CLSA	/CLEAR STATUS
2335	7330	CLA CLL	
2336	6132	CLLR	/ZERO ALL MODES
2337	1-31	TAU K0014	/ENAB. CHAN. 2 INPUT AND /INTERRUPT FLOPS
2338	6134	CLEN	
2339	7220	CLA	
2340	6131	CLSK	/CHECK FOR CLOCK INTER.
2341	5221	JMP ,+2	/WAIT
2342	6230	CLSA	/GET STATUS
2343	3-21	DCA RXE0	/SAVE IT
2344	1-21	TAU RXE0	/RESTORE IT
2345	7241	CLA	
2346	1143	TAU K0010	
2347	7540	SZA CLA	
2348	7-12	HLT	/INTERRUPT BUT CHAN 2 /EVENT FLOP NOT SET

/TEST OF INPUT CHAN 1

2353	6135	CLSA	/CLEAR STATUS
2354	7060	CLA CLL	
2355	6232	CLLR	/CLEAR ALL MODES
2356	1123	TAU K0030	/ENAB. CHAN1 INPUT
2357	6134	CLEN	/AND INTER.
2358	7222	CLA	
2359	6131	CLSK	/CHECK FOR CLOCK INTER.
2360	5220	JMP ,+2	/WAIT
2361	6230	CLSA	/GET CCLK STATUS
2362	3-21	DCA RXE0	/SAVE IT
2363	1-21	TAU RXE0	/RESTORE IT
2364	7241	CLA	
2365	1144	TAU K0040	
2366	7542	SZA CLA	

/MAINTAIN 12-28227 PAGE 32-1
10:55 10-001469 V141 PAL12 HLT /INTER, BUT CHAN 1 EVENT
/FLOOR NOT SET
1212 A2448 TAA AE6A TAA AE6A TAA AE6A TAA AE6A
/INDIRECT REF, TO IPT04
/OC TEST 128 TIMES
S2A CLA S2A CLA S2A CLA S2A CLA
IPT04
2777 4-552 2777 4-552 2777 4-552 2777 4-552

/*TEST OF SAMPLE MODE

2401	LINCP6141		/START LINC MODE
2402	CLR=0111		/CLEAR AC AND LINC
2403	ESF#Y4224		/ENAB SPEC. IN REG.
2404	SAN2#2121		/READ KNOB 2
2405	SAN1#2121		/READ KNOB 1
2406	STA#1#42		/STORE AC
2407	LOAD#1021		/LOAD AC
2408	POP#02822		/ENTER PDP-8 MODE
2409	7014	CSR	/IF RIGHT SW BIT 2(1)
2410	7010	STL	/SKIP FAST SAM TEST
2411	7012	SPA	
2412	2042	JMP 1 ,+2	/INDIRECT REF TO TCNT1
2413	7513	SKP	
2414	2055	TCNT1	
2415	6141	TSM,	/ENTER LINC MODE
2416	0011	LINC	
2417	0011	CLR	
2418	0014	ESF	/CLEAR SPEC. IN REG.
2419	0010	SAM0	/READ KNOB ZERO
2420	0002	POP	
2421	3020	DCA SEND	
2422	6141	LINC	
2423	0101	SAN1	/READ KNOB 1
2424	0011	CLR	/CLEAR AC
2425	1420	LOAD	
2426	0103	FLD	
2427	0004	ESF	/ENABLE FAST SAM
2428	0002	POP	/ENTER PDP-8 MODE
2429	6135	CLSA	/CLEAR CLOCK STATUS
2430	7300	CLA CLL	
2431	1142	TAD K0400	/SET MODE DIT0#1
2432	6132	CLLR	
2433	7300	CLA CLL	
2434	0101	LINC	/ENTER LINC MODE
2435	0100	SAM0	/FAST SAM SET THEREFORE
2436	0100	POP	/READ IN VALUE OF KNOB1
2437	1420	RXED	/AS THIS WAS LAST CONVER
2438	0021	DCA RXED	/SION
2439	1421	TAD RXED	
2440	7041	CIA	
2441	7040	CLA	
2442	7042	SEND	/COMPARE IT
2443	7040	SEA CLA	
2444	7410	SKP	
2445	7412	RET	/READING FAST SAM
2446	1040	K0200	/INITIATED CONVERSION
2447	0232	CLLR	/IN ERROR
2448	1040	TAD K0200	/MODE 2(1),0(1)

2449 7000 CLA CIA CML RAM
 2445 6103 CLAB /SET BUFF=4000
 2447 7004 CIA
 2448 1105 CIA 11200
 2451 6104 CIA /LOAD CTN FROM BUF
 2452 7007 CLA
 2453 6105 CLAB /CLR BUF
 2454 7008 CLA
 2455 6102 CLBR /CLEAR ALL MODES
 2456 1140 TAG K6200
 2457 6152 CLBR /SET OVERFLOW MODE 0(1)
 2458 6141 LINC /ENTER LINC MODE
 2459 6142 SAM2 /SAMPLE KNOB 0
 2460 6132 PDP /ENTER PDP-8 MODE
 2463 3121 DCA RXED /STORE
 2464 1021 TAG RXED /RESTORE
 2465 7041 CIA
 2466 3120 TAG SEN
 2467 7044 SZA CLA
 2470 7402 MLT /CONVERSION NOT INITIATED BY OVFLO
 2471 2022 ISZ REGA /DO TEST 4096 TIMES
 2472 5552 JMP I TSM /CROSS PAGE REF TO TSM
 /CHECK THAT MODE 2(2),1(1),2(1) DO NOT AFFECT
 /SAM
 2473 7200 TSM1, CLA /ZERO ALL MODES
 2474 6132 CLBR
 2475 1126 TAG K3300 /MODE 1(1),2(1),0(0)
 2477 6141 LINC /ENTER LINC MODE
 2500 0111 CLA
 251 6104 ESF /ZERO SPEC. IN. REG.
 252 0100 SAM2 /SAMPLE KNOB 0
 253 0006 PDP
 254 3020 DCA SEN0
 255 6141 LINC
 256 0101 SAM1 /SAMPLE KNOB 1
 257 1022 LDA1
 258 2100 Z100
 2511 0024 ESF /SET FAST SAM FLOP
 2512 0102 SAM0 /GET KNOB 1 SETTING
 2513 0002 PDP /ENTER PDP MODE
 2514 3021 DCA RXED /STORE
 2515 1021 TAG RXED /RECEIVE
 2516 7041 CIA
 2517 1040 TAG SEN0 /COMPARE
 2520 7042 SZA CLA
 2521 7010 SKP
 2522 7012 MLT /FAST SAM NOT SET
 2523 6141 LINC /ENTER LINC MODE
 2524 2102 SAM2 /READ KNOB 0
 2525 0002 PDP /ENTER PDP MODE
 2526 3021 DCA RXED /STORE
 2527 1021 TAG RXED /RESTORE

YAMAL DEG 32-873 PALLI V141 17-507-69 10155 PAGE 34-1

AMAI DEC 12-1979

PAL12 V141 14-OCT-69 10:55 PAGE 35

/DOES TO PRESET CLEAR OVFLD, ENABLES, RATES AND MODES

/PROGRAMED TO PRESET USED

/IS COUNTER WORKING

2550 74	TOUT1, CLA	/CLEAR AC
2551 6130	CLLR	/CLEAR ALL MODES
2552 0	CLLR	/CLEAR ALL ENABLES
2553 141	TAC K5000	
2554 84	CLCA	/SET RATE=10KHZ
2555 6130	CLCA	/READ COUNTER
2556 3020	DCA SEND	/STORE
2557 1147	TAC K6400	
2558 76-1	IAC	
2559 744	SZA	
2560 5346	JMP ,=2	/WAIT LOOP 4.92 MSEC
2561 6137	CLCA	/READ COUNTER AGAIN
2562 7041	CIA	
2563 1020	TAC SEND	/COMPARE
2564 7042	SZA CLA	
2565 7412	SKP	
2566 7400	HLT	/COUNTER NOT WORKING /WITH RATE BITS 1+2 SET

/NOW DO IO PRESET CHECK IF RATE BITS 1,2 CLEAR

2567 6141	LINC	/ENTER LINC MODE
2568 1020	LDAI	
2569 0020	0020	
2570 0044	ESF	/DO IO PRESET
2571 2002	PDP	/ENTER PDP MODE
2572 6137	CLCA	/GET COUNTER
2573 3020	DCA SEND	/STORE
2574 1147	TAC K6400	
2575 7042	NOP	
2576 7400	NOP	
2577 7401	NOP	
2578 7401	IAC	
2579 744	SZA	
2580 5372	JMP ,=2	/WAIT LOOP 4.92 MSEC
2581 6137	CLCA	/READ COUNTER AGAIN
2582 7041	CIA	
2583 1020	TAC SEND	/COMPARE
2584 7042	SZA CLA	
2585 7402	HLT	/IO PRESET FAILED TO /CLEAR RATE BITS 1,2
2586 6132	CLLR	/CLEAR ALL MODES

/NOA CHECK RATE BIT 0
 /CLEAR SEE IF COUNT LINKS AT 1KHZ RATE

2513	72	CLR		/CLEAR AC
2514	6132	CLR		/CLEAR ALL MODES
2515	6204	CLR		/CLEAR ENABLES
2516	1002	TAD	K4000	
2517	6132	CLR		/SET RATE=1KHZ
2518	6137	CLRA		/READ COUNTER
2519	3000	DOA	SEND	
2520	7404	NOP		
2521	7402	1AC		
2522	7442	SZA		
2523	5213	JMP	,+2	/WAIT LOOP 16 MSEC
2524	6137	CLCA		/READ COUNTER
2525	7041	CIA		
2526	1002	TAD	SEND	/COMPARE
2527	7442	SZA		
2528	7421	SCP		
2529	7422	HLT		

/COUNTER NOT WORKING
 /WITH RATE BIT 0 SET

/NOA DO IO PRESET AND SEE IF BIT 1 CLEARED

2530	6141	L1-C		/ENTER LINC MODE
2531	1222	LCAL		
2532	8001	2003		
2533	0004	ESF		/DO IO PRESET
2534	2003	P7		/ENTER PDP MODE
2535	6137	CLCA		/READ COUNTER
2536	3000	DOA	SEND	/STORE
2537	7402	NOP		
2538	7401	1AC		
2539	7442	SZA		
2540	5234	JMP	,+2	/WAIT 16 MSEC
2541	6137	CLCA		/READ COUNTER AGAIN
2542	7041	CIA		
2543	1222	TAD	SEND	/COMPARE
2544	7042	SZA CLA		
2545	7422	HLT		

/RESETS OVERFLOW AND OVFL0 INT, FLOP
 /CLEAR WITH IO PRESET

2546	7216	TCON2, CLA		/CLEAR AC
2547	6132	CLR		/CLEAR ALL MODES
2548	1023	TAD	K2100	
2549	6132	CLR		/SET MODE 2(1)
2550	6135	CLSA		/CLEAR STATUS
2551	7200	CLA		
2552	1005	TAD	K4000	
2553	6133	CLAS		/SET BUF TO 4000
2554	7402	C		
2555	1002	TAD	K1200	
2556	6134	CLEN		/LOAD COUNTER
2557	7400	CLA		
2558	6103	CLAB		/ZERO BUF
2559	6132	CLR		/CLEAR ALL MODES

/MHI DEC 12-1973 PAL12 V141 1A-300T-69 12:55 PAGE 36-1

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L-100

PALY V141

12

-OCT-69

10:55 PAGE 37

2772	7443	SVA CLA	
2773	7444	SVA	
2774	7442	ALT	/OVFL0 STILL SET AFTER IO /PRESET
/TEST OVFL0 INT & ENABLE			
2775	7428	CLA	/CLEAR AC
2776	7423	TAD	K1200
2777	6132	CLLR	
2778	6135	CLSA	/SET MODE 2(1)
2779	7420	CLA	/CLEAR STATUS
2780	1455	TAD	K4K20
2781	6133	CLAB	
2782	7420	CLA	/SET BUF PRESET REG.
2783	1115	TAD	K0200
2784	6134	CLEN	
2785	7420	CLA	/LOAD CNT WITH 4000
2786	7420	CLM	
2787	7420	CLA	
2788	1423	TAD	K0100
2789	6134	CLEN	
2790	6141	LINC	/SET INT,
2791	1420	LDAT	/ENTER LINE MODE
2792	6120	K220	
2793	6120	ESF	/DO IO PRESET
2794	6120	FDP	/ENTER PDP MODE
2795	7400	CLA	
2796	6132	CLLR	/CLEAR ALL MODES
2797	7423	TAD	K0100
2798	6132	CLLR	
2799	6131	CLSK	/GEN.
2800	7410	SKP	
2801	7442	ALT	/OVFL0 INT,
			/SET AFTER IO PRESET
/DOES IO PRESET CLEAR INPUT ENABLE FLOPS			
2796	7400	CLA	
2797	6132	CLLR	/CLEAR ALL MODES
2798	1420	TAD	K0077
2799	6134	CLEN	
2800	6135	CLSA	/ENABLE INPUTS TO ALL CHAN
2801	6141	LINC	/CLEAR STATUS
2802	1420	LDAT	/ENTER LINE MODE
2803	6120	K220	
2804	6120	ESF	/DO IO PRESET
2805	6120	FDP	/ENTER PDP MODE
2806	7400	CLA	
2807	1435	TAD	K0077
2808	6132	CLLR	/SIMULATE INPUTS ON ALL CHAN

2743	7440	NOP	
2744	7442	NOP	
2745	7442	NOP	
2746	7440	NOP	
2747	7440	NOP	
2750	7440	NOP	
2751	6432	CLLR	/SIM INPUTS ON ALL CHAN
2752	7440	NOP	
2753	7440	NOP	
2754	7440	NOP	
2755	7440	NOP	
2756	7440	NOP	
2757	7440	NOP	
2760	7440	CLA	
2761	6135	CLSA	/GET STATUS
2762	7440	SEA	
2763	7440	HLT	
2764	7440	CLA	
		/DOES IO PRESET CLEAR MODE 2	
2765	6133	CLAB	
2766	6132	CLLR	
2767	1023	TAD K0100	/CLEAR MODES
2770	6132	CLLR	
2771	6141	LINC	/SET MODE 2(1) - CLR CNT
2772	1020	LDI	/ENTER LINC MODE
2773	0020	0020	
2774	0024	ESF	
2775	2002	PDP	/DO IO PRESET
2776	7440	CLA	/ENTER PDP MODE
2777	1120	TAD K5555	
3000	6133	CLAB	/LOAD BUF WITH 5555
3001	7440	CLA	
3002	1105	TAD K2200	
3003	6134	CLEN	
3004	6137	CLCA	/GEN LOAD CNT
3005	7710	SPA CLA	/LOAD CNT TO AC
3006	7440	HLT	
		/MODE 2 NOT CLEARED	
		/BY IO PRESET	
		/DOES IO PRESET CLEAR MODE 0	
3007	7424	OSR	
3010	7406	RTL	
3011	7510	SPA	
3012	5254	JMP INDEX	
3013	7200	CLA	
3014	6132	CLLR	
3015	6141	LINC	/CLEAR ALL MODES
3016	0100	SAM0	/ENTER LINC MODE
3017	2002	PDP	/READ KNOB 0
3020	3020	DCA SEND	
3021	6141	LINC	
3022	0101	SAM1	
3023	0002	PDP	/READ KNOB 1
			/ENTER PDP MODE

/M2140EC 42-3842-
17 - 7220 - 1242 - 0111
PAGE 38-1
10:55 10-OCT-69 PAGE 38-1
GLA K2422 /SET MODE 0(1)
CLL2 L110 /ENTER LINE MODE
6141 6227 3825 3825 3825 3825 3825

/MAI-DEC 12-0897

PAL10

V141

10-OCT-69

10:55 PAGE 39

3230	1422	LDAI	
3231	2022	0020	
3232	1414	ESF	/DO IO PRESET
3233	1422	LDAI	
3234	0100	0100	/ENABLE FAST SAM
3235	2204	ESF	
3236	1422	SAM0	/READ KNOB 1=FAST S. MODE
3237	0002	PDP	/ENTER PDP MODE
3240	7041	CIA	
3241	1020	TAD SEND	
3242	7640	SZA CLA	
3243	7410	SKP	
3244	7402	HLT	/FAST SAM NOT SET
3245	6141	LINC	/ENTER LINC MODE
3246	2100	SAM0	/READ KNOB 0
3247	0002	PDP	/ENTER PDP MODE
3250	7041	CIA	
3251	1422	TAD SEND	
3252	7640	SZA CLA	
3253	7422	HLT	/MODE 0 NOT CLEARED
3254	2222	INDEX, ISZ REGA	/DO TEST 4096 TIMES
3255	5554	JMP I TCNT2A	/CROSS PAGE RER TO TCNT2
3256	6141	LINC	
3257	1422	LDAI	
3258	0020	0020	
3259	0004	ESF	/DO IO PRESET
3260	0402	PDP	

3103	7200	CLA	
3104	7200	/DOES MODE 1(1) WORK	
3105	6132	TMO01, CLA	
3106	6133	CLLR	/CLEAR ALL MODES
3107	4056	JMS RANDOM	/CLEAR BUF
3108	3020	OCA SEND	/GET RANDOM NUM
3109	1020	TAD SEND	
3110	6133	CLAB	/SEND RANDOM NUM TO BUF
3111	7200	CLA	
3112	1023	TAD K0100	
3113	6132	CLLR	/GEN "CLR CNT"
3114	6135	CLSA	/CLEAR CLOCK STATUS
3115	7200	CLA	
3116	1105	TAD K2200	
3117	6134	CLEN	/GEN LOAD CNT
3118	6132	CLLR	/SET MODE BIT 1(1)
3119	7200	CLA	
3120	6133	CLAB	/CLEAR BUF
3121	1123	TAD K0060	
3122	6134	CLEN	/ENABLE INPT 1 AND INT CHAN1
3123	6131	CLSK	/SKP ON CLOCK INT
3124	5027	JMP , -1	
3125	6135	CLSA	/CLEAR STATUS
3126	7200	CLA	
3127	7003	NOP	
3128	6136	CLBA	/GET BUF
3129	7041	CIA	
3130	1020	TAD SEND	/COMPARE
3131	7040	SZ4 CLA	
3132	7942	HLT	/CHAN 1 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3133	6134	CLEN	/CLEAR ENABLES
3134	6135	CLSA	/CLEAR CLOCK STATUS
3135	7200	CLA	
3136	6133	CLAB	/CLEAR BUF
3137	1101	TAD K0014	
3138	6134	CLEN	/ENABLE CHAN 2 INPUT AND INT
3139	6131	CLSK	/SKP ON CLOCK INT
3140	5027	JMP , -1	
3141	6135	CLSA	/CLEAR STATUS
3142	7000	CLA	
3143	7000	NOP	
3144	6130	CLBA	/GET BUF
3145	7041	CIA	
3146	1020	TAD SEND	/COMPARE
3147	7040	SZ4 CLA	
3148	7942	HLT	/CHAN2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3149	6134	CLEN	/CLEAR ENABLE
3150	6135	CLSA	/CLEAR STATUS
3151	7200	CLA	
3152	6133	CLAB	/CLEAR BUF
3153	1030	TAD K0003	

3147 6154 CLEN /ENABLES CHAN 3 INPUT AND INT
 3151 6131 CLSK /SKIP ON CK INT
 3151 5000 JMP , -1
 3152 6155 CLSA /CLEAR CLOCK STATUS
 3153 7000 CLA
 3154 7200 NOP
 3155 7000 NOP
 3156 6130 CLBA /GET BUF
 3157 7041 CIA
 3158 1022 TAD SEND /COMPARE
 3159 7040 SZA CLA
 3160 7000 HLT /CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
 /TEST MODE 1(1) AND MODE 2(1)
 3163 6154 TMOD3, CLEN /CLEAR ENABLES
 3164 1136 TAD K0300
 3165 1114 TAD K1000 /START CNT RATE=400KHZ - MODE 1(1) AND 2(1)
 3166 6132 CLLR /WAIT
 3167 7000 NOP
 3168 7000 NOP
 3169 7000 NOP
 3170 7000 NOP
 3171 7000 CLA
 3172 7000 TAD K0300 /STOP CNT - MODE 1(1) AND 2(1)
 3173 7000 CLLR
 3174 1140 CLCA /GET CNT
 3175 6132 CLCA /STORE
 3176 6137 DCA SEND
 3177 3022 CLSA /CLEAR BUF
 3202 6130 CLSA
 3201 7200 CLA
 3202 6133 CLAB /ENABLE CHAN1 INPUT AND INT
 3203 1123 TAD K0260 /SKP ON CLOCK INT
 3204 6134 CLEN /CLEAR CLOCK STATUS
 3205 6131 CLSK
 3206 5205 JMP , -1
 3207 6130 CLSA /GET BUF
 3208 7200 CLA
 3209 6133 CLBA /COMAPRE
 3210 7041 CIA
 3211 1020 TAD SEND /CHAN1 FAILED TO CAUSE CNT TO BUF TRANSFER
 3212 7040 SZA CLA
 3213 7402 HLT /CLEAR ENABLES
 3214 6134 CLEN /CLEAR STATUS
 3215 6135 CLSA /CLEAR BUF
 3216 7200 CLA
 3217 6133 CLAB /ENABLE CHAN 2 INPUT AND INT
 3218 1131 TAD K0K14 /SKP ON CLOCK INT
 3219 6134 CLEN /CLEAR STATUS
 3220 6131 CLSK
 3221 5224 JMP , -1
 3222 6130 CLSA /CLEAR STATUS
 3223 7000 CLA
 3224 7000 NOP
 3225 7000 NOP
 3226 6136 CLBA /GET BUF
 3227 7041 CIA

MAIL DEC-12-1977
12-3872-2-2-2-2
PAL12A V149 2E-001-69
20155 PAGE A1-1
ACOMPARA
S23 LLL
TAD SEIN
COLLEGE ENARLES
ZOHAN 2 INPUT FAILED TO CAUSE QNT TO BUF TRANSFER

3240	6153	CLSA	
3241	7107	CLA	
3242	6103	CLAR	
3243	5401	TAU	K2463
3244	6104	CLEN	/CLEAR BUF
3245	6131	CLKS	/ENABLES CHAN3 INPUT AND INT
3246	5245	JMP ,+1	/SKP ON CLOCK INT
3247	6107	CLSA	/CLEAR CLOCK STATUS
3248	7402	CLA	
3249	7400	NOP	
3250	7402	NOP	
3251	6103	CLSA	
3252	7402	CLA	
3253	6103	NOP	
3254	7401	CLIA	
3255	1022	TAU SEND	/COMPARE
3256	7042	SZA CLA	
3257	7402	HLT	/CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3258	6137	CLCA	/GET CNT
3259	7041	SZA CLA	
3260	7402	HLT	/CHAN3 INPUT FAILED TO CLEAR CNT
3261	7400	NOP	
3262	7402	NOP	
3263	7400	NOP	
3264	7402	NOP	
3265	7404	OSR	
3266	7404	RAL	
3267	7116	SPA CLA	/IF RIGHT SWITCHES BIT 1(1) SUPPRESS PRINTING OF K
3270	5300	JMP ,+12	
3271	6141	LINC	
3272	1021	LOAD	
3273	0313	0313	
3274	0672	PDP	
3275	6446	TLS	
3276	6241	TSF	
3277	5276	JMP ,+1	
3300	7200	CLA	
3301	1321	TAU COUNT	
3302	7301	IAC	
3303	3327	DCA COUNT	
3304	1321	TAU COUNT	
3305	7241	CLA	
3306	1124	TAU K2420	
3307	7740	SZA CLA CLL	
3310	5330	JMP IOPRE	
3311	3327	DCA COUNT	
3312	7404	OSR	
3313	7112	SPA CLA	
3314	5350	JMP IOPRE	
3315	1144	WHISTLE, TAU K00442	
3316	7422	SNL	
3317	5010	JMP ,+2	
3318	7100	CLL	
3321	1026	TAU K0001	
3322	1140	TAU K2420	
3323	7422	SNL	
3324	5322	JMP ,+2	

MAILED DECO 42-499 - FILED - OCT 1969
PAGE 42-1
10:55 10-10-69
TOP SECRET
3320 1020 1010 1000 1000 1000 1000 1000

10:55 PAGE 43
10-DEC-69 V141 PAL12 L-10
/MAI DEC 02 1969

AMAT DECEMBER-999

PAL10 V141 10-OCT-69

10:55 PAGE 43-2

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1961 DEC 26 1969

PAL12 0141 10-OCT-69

23165 PAGE 43-3

CL	0-05	KOJO	0122	TST12	2044	TST49X	0141
CL	0-05	KOJO	0124	TST12A	0154	TST49Y	0142
CLG	0111	KOJO	0119	TEST31	1261	WHISTL	3315
CLG	0111	KOJO	0120	TEST31	1120		
COL	0-05	KOJO	0147	TST32	1132		
COL	0-05	KOJO	0123	TMO31	3264		
COS	0110	KOJO	0043	TMO33	3163		
COS	0-05	L001	1020	TS4	2426		
COU T	0007	L00C	6141	TS41	2473		
COU TX	0101	L00A	1274	TS41A	2153		
ESF	0-04	L00B	1312	TS4A	0152		
INET	3024	L00C	1334	TST2E	2201		
INF 1	2205	L00D	2775	TST21	2214		
INP102	2442	L00E	2100	TST22	0227		
INP103	2225	L00F	2151	TST23	0243		
INP104	2810	L00G	2161	TST24	2261		
INTP	1257	L00H	2172	TST25	0277		
IPPE	3551	L00I	2202	TST26	0317		
IP1	0121	MZ-21	3225	TST27	0360		
ITST 1	2-03	MZ-02	0227	TST27A	0125		
ITST 2	2141	M0004	2231	TST28	0440		
ITST 3	2102	M0110	0744	TST29	0520		
K0231	0-05	M0020	0045	TST30	0534		
K0232	0-05	M0040	0046	TST31	0562		
K0233	0-05	M0100	0047	TST31X	0162		
K0234	0-05	M0200	0250	TST32	0603		
K0235	0-05	M0400	0051	TST32A	0127		
K0236	0-05	M1700	2052	TST33	0625		
K0237	0-05	M2000	0053	TST34	0651		
K0238	0-05	M4000	2254	TST35	0700		
K0239	0-05	P00	2202	TST35A	0126		
K0237	0-05	PNTA	0116	TST36	0732		
K0240	0-05	PNTB	0111	TST37	0756		
K025	0-05	PNTC	0112	TST37X	1010		
K0271	0-05	P10	2133	TST38	1011		
K0272	0-05	P1TE	0134	TST38A	1132		
K0277	0-05	PNTF	0100	TST39	1040		
K028	0-05	PNTG	0136	TST40	1167		
K03	0-05	PNTH	0137	TST40X	1214		
K0377	0-05	PNTI	0140	TST41A	1374		
K042	0-05	RANDOM	0056	TST41A	1216		
K0521	0-05	RESA	0022	TST41B	0155		
K0677	0-05	RETURN	0113	TST42	1425		
K0757	0-05	RVA	0102	TST43	1456		
K0777	0-05	R-V	0103	TST44	1507		
K1177	0-05	RVC	0104	TST45	1540		
K1777	0-05	RXC0	0021	TST46	1571		
K2077	0-05	SAC0	0101	TST47	1622		
K2777	0-05	SAC1	0101	TST48	1653		
K3777	0-05	SEV0	0328	TST49	1704		
K411	0-05	STA	1746	TST49A	1735		
K4120	0-05	T0-T1	2536	TST49B	1766		

34 CORE 05

RUN-TIME: 07 SECONDS

LINKS GEN: 1301 >

ENDRS GEN: 1301 >

/MAINDEQ/98-3844-
0-D8C0-6-42J

12:55 PAGE 43-A

10-001-69

V141

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