KP8/I
POWER FAILURE OPTION FUNCTIONAL DESCRIPTION

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Instruction times, operating speeds and the like are included in this manual for reference only; they are not to be taken as specifications.

KP8/I POWER FAILURE

INTRODUCTION

This PDP-8/I option provides an interrupt signal to the computer, and allows computer operation for a fixed time after a primary power interruption. With proper programming, an interrupt from the KP8/I insures data storage of the several machine registers of interest (accumulator, link, program counter, etc) in core memory. With the option enabled, restoration of power restarts the computer at memory location 0000_8 after a suitable voltage stabilization delay. A program subroutine, entered when power returns, places the previously stored data back in the proper registers. The option can be disabled to prevent this restart.

The KP8/I option consists of an M703 integrated-circuit module partially controlled by the PDP-8/I G826 Regulator and Power Detector Module. Both modules are contained within the processor logic frame.

The referenced PDP-8/I drawings in this book are located in Volume II of the PDP-8/I Maintenance Manual.

Logic Description (Refer to Figure 1)

The following paragraphs describe the sequence of events occurring when power is interrupted. The basic power-fail programming technique is also described.

When primary power is removed, a detection circuit in the G826 Module (Regulator and Power Detector, drawing BS-8I-0-13) reacts to a decrease in the +5 Vdc voltage, and generates a low logic level, $\overline{\text{SHUT DOWN}}$. This signal sets the KP8/I PWR LOW flag flip-flop (drawing BS-KP8I-0-1). PWR LOW(0) generates a $\overline{\text{TT INT}}$ signal (drawing BS-8I-0-12 and BS-8I-0-10). A program interrupt occurs if the processor interrupt facility is enabled. The interrupt is effected in the usual manner, with a search subroutine using the octal instruction 6102 (SPL, Skip on Power Low) to enable the $\overline{\text{PWR SKIP}}$ gate signal to locate the interrupting source. The $\overline{\text{PWR SKIP}}$ gate is enabled by PWR LOW(1), the power-fail device selection code (10_8, from MB03 through MB08), and the interrogation timing signal IOP2(1). $\overline{\text{PWR SKIP}}$ generates a $\overline{\text{TT SKIP}}$ signal (drawing BS-8I-0-12 and BS-8I-0-10) which allows entry into the power fail service subroutine shown in Figure 1. The service routine stores the contents of the AC, MQ and SC (with EAE option), Link, PC, and Save Field Register (extended memory). When any program interrupt occurs, and the interrupt facility is enabled, the contents of the PC are automatically stored in location 0000_8; therefore, the TAD 0000_8 is performed to bring the PC word into the AC for storage in memory. Finally, a JMP instruction to address X is stored in location 0000_8, and the HLT instruction is executed. Address X is the starting location of the restart program. A HLT instruction must end the power fail service routine.

The time for search and execution of the above subroutine is provided by the 1-ms single-shot delay activated by the $\overline{\text{SHUT DOWN}}$ signal. It activated low output, STOP OK, inhibits the Regulator Control of the G826 Module and allows further machine operation. After the 1-ms delay, the STOP OK signal returns high; the Regulator Control disables the memory voltage; and STOP OK and $\overline{\text{POWER OK}}$ combine to clear the RUN

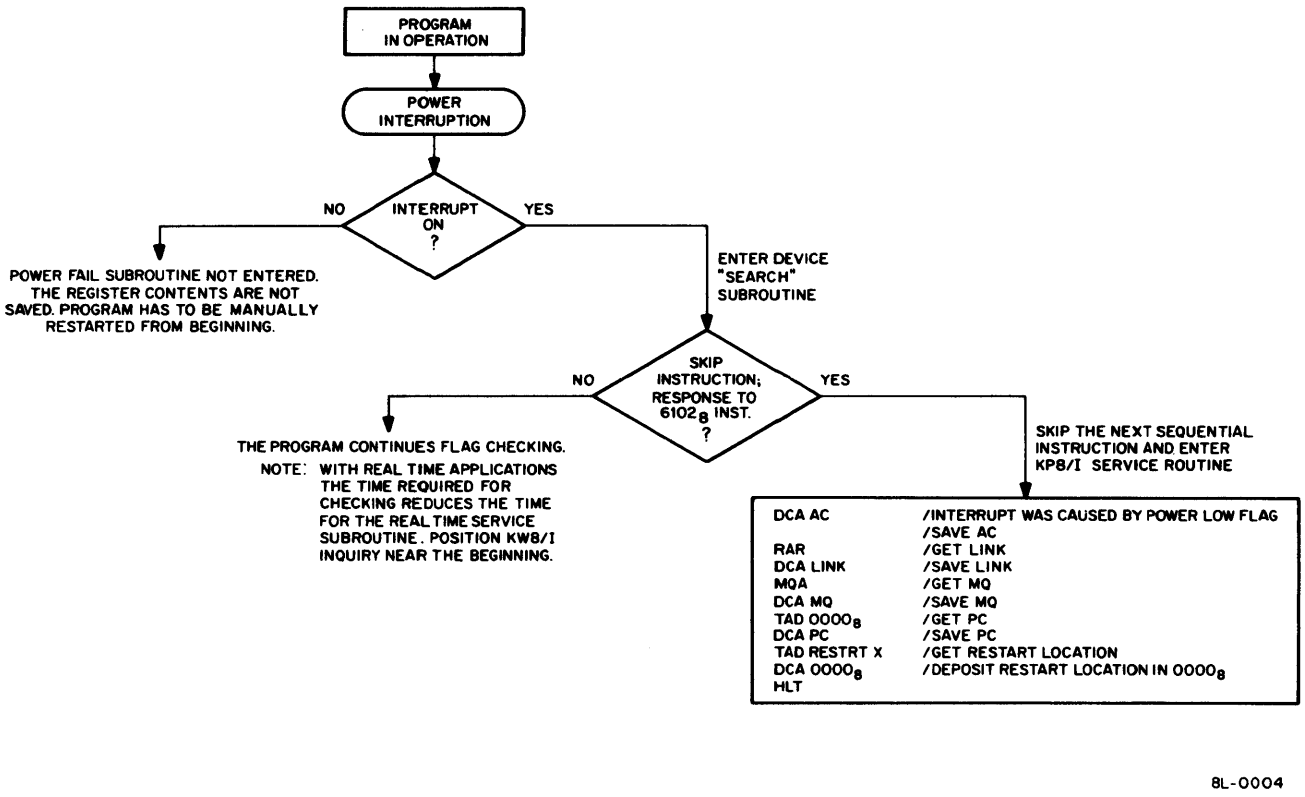


Figure 1 Automatic Restart Program Events

flip-flop is at the next processor time pulse TP3 (drawing BS-8I-0-2).

Restoration of primary power applies initializing signals throughout the PDP-8/I to clear the major timing and machine-state flip-flops, including PWR LOW. For the machine to begin, however, a restart signal must be generated. The integrating 300-ms single shot delay, shown in Dwg. No. D-BS-KP8/I-0-1, is enabled when a normal +5 Vdc voltage is detected (both $\overline{\text{SHUT DOWN}}$, and STOP OK are high logic levels). If no additional power interruptions occur, the single shot will time out and try to generate the restart signal. The microswitch contained on the M703 Module handle can be set to OFF to inhibit this pulse, or set to ON to allow it.

If a 1-ms $\overline{\text{RESTART}}$ pulse is generated, this signal acts as a $\overline{\text{KEY ST}}$ signal in activating the manual function timing generator, by producing the same signals, KEY ST and KEY ST + EX + DP (drawing BS-8I-0-3). A 0000_8 starting address is forced by $\overline{\text{RESTART}}$ inhibiting the enabling of the PC register to the MA register during MFTS1(1) (drawing BS-8I-0-4). Program events are noted in Figure 2.

NOTE

A JMP or JMS instruction must be in location 0000_8 to provide a known next address instead of utilizing the unknown PC register contents.

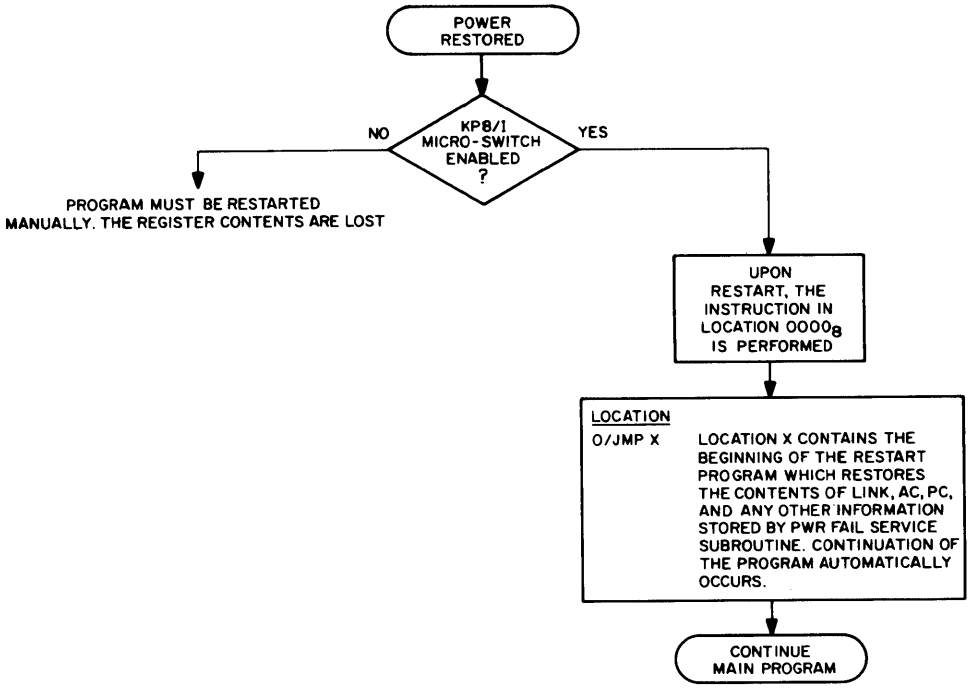
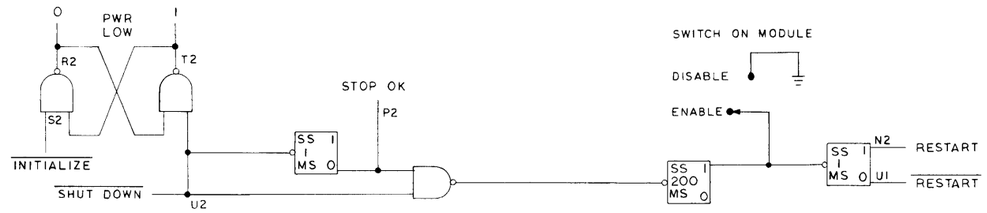
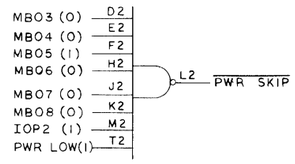


Figure 2 Typical Power Failure Program Service Routine

NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

M703
A04





Dwg. No. D-BS-KP8/I-0-1 Schematic Diagram