

**DRV11-B**  
**general purpose DMA**  
**interface user's manual**

digital pdp11/03

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**interface user's manual**

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# CONTENTS

	Page	
<b>CHAPTER 1</b>	<b>INTRODUCTION</b>	
1.1	GENERAL DESCRIPTION . . . . .	1-1
1.2	SPECIFICATIONS . . . . .	1-2
1.3	RELATED LITERATURE . . . . .	1-4
<b>CHAPTER 2</b>	<b>INSTALLATION</b>	
2.1	GENERAL . . . . .	2-1
2.2	SYSTEM CONSIDERATIONS . . . . .	2-1
2.2.1	LSI-11 Bus Loading . . . . .	2-1
2.2.2	Power Requirements . . . . .	2-1
2.2.3	Priority Requirements . . . . .	2-1
2.2.4	Space Requirements . . . . .	2-1
2.3	USER I/O CABLES . . . . .	2-1
2.4	DEVICE ADDRESS SELECTION . . . . .	2-2
2.5	INTERRUPT VECTOR ADDRESS SELECTION . . . . .	2-2
2.6	MODULE INSTALLATION . . . . .	2-3
2.7	INITIAL TURN-ON . . . . .	2-5
2.8	DIAGNOSTIC PROGRAM . . . . .	2-5
<b>CHAPTER 3</b>	<b>BASIC OPERATION</b>	
3.1	GENERAL . . . . .	3-1
3.2	FUNCTIONAL DESCRIPTION . . . . .	3-1
3.2.1	DRV11-B Registers . . . . .	3-1
3.2.1.1	Word Count Register (WCR) . . . . .	3-1
3.2.1.2	Bus Address Register (BAR) . . . . .	3-1
3.2.1.3	Control/Status Register (CSR) . . . . .	3-1
3.2.1.4	Input and Output Data Buffer Registers (DBRs) . . . . .	3-3
3.2.2	User Interface Lines . . . . .	3-3
3.2.3	LSI-11 Bus Lines . . . . .	3-4
3.2.4	User's I/O Device to LSI-11 Memory Transfer (DATO or DATOB) . . . . .	3-6
3.2.4.1	Interrupts . . . . .	3-7
3.2.5	LSI-11 Memory to User's Device Transfers (DATIO or DATI) . . . . .	3-7
3.3	TIMING . . . . .	3-8
<b>CHAPTER 4</b>	<b>PROGRAMMING</b>	
4.1	GENERAL . . . . .	4-1
4.2	PROGRAMMING INSTRUCTIONS . . . . .	4-1
4.3	DRV11-B REGISTERS . . . . .	4-1
4.3.1	WCR . . . . .	4-1
4.3.2	BAR . . . . .	4-1
4.3.3	CSR . . . . .	4-1
4.3.4	DBRs . . . . .	4-1

## CONTENTS (Cont)

		Page
4.4	PROGRAM INTERRUPTS . . . . .	4-2
4.4.1	Word Count Overflow . . . . .	4-2
4.4.2	CSR ERROR Bit (Bit 15) . . . . .	4-2
4.5	FUNCTION AND STATUS BITS . . . . .	4-2

## ILLUSTRATIONS

Figure No.	Title	Page
1-1	DRV11-B Simplified Interface Diagram . . . . .	1-2
2-1	DRV11-B Connector and Switch Locations . . . . .	2-3
2-2	DRV11-B Device Address Select Format . . . . .	2-3
2-3	DRV11-B Interrupt Vector Address Select Format . . . . .	2-4
2-4	DRV11-B Connector Pin Assignments . . . . .	2-4
3-1	DRV11-B Block Diagram . . . . .	3-2
3-2	DMA DATO/DATOB Data Flow Diagram . . . . .	3-6
3-3	DMA DATIO/DATI Data Flow Diagram . . . . .	3-8
3-4	DRV11-B Single Cycle, User-Initiated, Timing Diagram . . . . .	3-9
3-5	DRV11-B Single Cycle, Program-Initiated, Timing Diagram . . . . .	3-10
3-6	DRV11-B Burst Mode, User-Initiated, Timing Diagram . . . . .	3-11
3-7	DRV11-B Burst Mode, Program-Initiated, Timing Diagram . . . . .	3-12
4-1	CSR Format . . . . .	4-2

## TABLES

Table No.	Title	Page
2-1	Recommended Cable Assemblies . . . . .	2-2
3-1	C0, C1 Codes . . . . .	3-4
4-1	CSR Bit Functions . . . . .	4-3

# CHAPTER 1

## INTRODUCTION

### 1.1 GENERAL DESCRIPTION

The DRV11-B is a general-purpose direct memory access (DMA) interface for transferring 16-bit data words directly between the LSI-11 memory and a user's I/O device. Data Transfer Out (DATO) or Data Transfer In (DATI) takes place via the LSI-11 bus after a DMA request, where the DRV11-B becomes bus master. Burst modes, byte addressing, and read-modify-write operation (DATIO) are possible with the DRV11-B. The DRV11-B features switch-programmable device and vector addresses and 40-pin connectors which provide for simple interfacing to the user's I/O device.

Five registers are contained within the DRV11-B:

- Word Count Register (WCR)
- Bus Address Register (BAR)
- Control/Status Register (CSR)
- Input and Output Data Buffer Registers (DBRs).

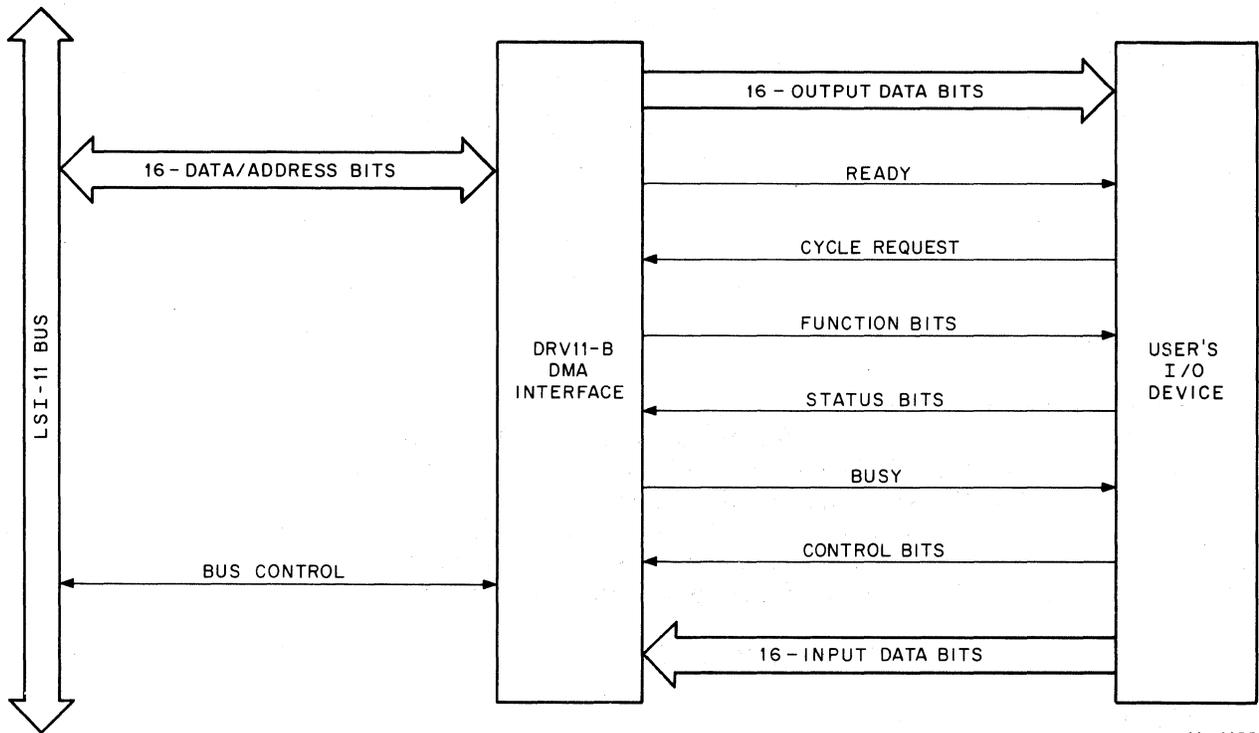
The CSR and DBRs are word- and byte-addressable, whereas the WCR and BAR are only word-addressable.

DRV11-B operation is initialized under program control by:

1. Loading the WCR with the 2's complement of the number of transfers
2. Loading the BAR with the first address to or from which data is to be transferred
3. Loading the CSR with the desired function bits.

Data transfers may now proceed under the control of the DRV11-B DMA logic.

Figure 1-1 shows the primary interface signals between the DRV11-B and the user's I/O device. DMA input (DATI) or output (DATO) data transfers take place when the processor clears READY. For a DATO cycle (DRV11-B to memory transfer), the user's I/O device presets the CONTROL BITS (word count increment enable, bus address increment enable, C1, C0, A00, and ATTN), and asserts CYCLE REQUEST to gain use of the LSI-11 bus. When CYCLE REQUEST is asserted, input data is latched into the input DBR, the CONTROL BITS are latched into the DRV11-B DMA control, and BUSY goes low. (A DATI cycle memory to DRV11-B transfer is handled in a similar manner, except that the output data is latched into the output DBR during the bus cycle.)



11-4155

Figure 1-1 DRV11-B Simplified Interface Diagram

When the DRV11-B becomes bus master, a DATO or DATI cycle is performed directly to or from the LSI-11 memory location specified by the BAR. At the end of each cycle, the WCR and BAR are incremented and BUSY goes high while READY remains low. A second DATO or DATI cycle is performed when the user's I/O device again asserts CYCLE REQUEST. DMA transfers will continue asynchronously until the WCR increments to zero, at which time READY goes high and the DRV11-B generates an interrupt (if interrupt enable is set) to the LSI-11 processor.

If burst mode is selected (SINGLE CYCLE low), only one CYCLE REQUEST is required for the complete synchronous transfer of the specified number of data words.

## 1.2 SPECIFICATIONS

The following specifications and particulars are for informational purposes and are subject to change without notice.

### Physical

Quad-height, single width, extended length module

### Dimensions

8-1/2 in. L, 10-1/2 in. H, 1/2 in. W  
(21.6 cm L, 26.7 cm H, 1.27 cm W)

### Weight

13 oz. (370 gr)

User I/O Connections

Two (2) 40-pin connectors

Mounting Requirements

Plugs directly into LSI-11 backplane or LSI-11 expansion backplane

**Electrical**

Logic Power Requirements

+5 V  $\pm$  5% @ 1.9 A (nominal)

LSI-11 Bus Loading

Presents one bus load

User Loading

Input Data Lines

1 TTL unit load each

HIGH = Logic one

LOW = Logic zero

Input Control Lines

1 TTL unit load each

HIGH = Logic one

LOW = Logic zero

Output Data Lines

10 TTL unit loads (drive) each

HIGH = Logic one

LOW = Logic zero

Output Control Lines

10 TTL unit loads (drive) each

HIGH = Logic one

LOW = Logic zero

Module Type

M7950

Operational

Transfer Mode

DMA or program-controlled with interrupts

Data Transfer Rate

Up to 250,000 16-bit words per second in single cycle mode

Up to 500,000 16-bit words per second in burst mode

**Environmental**

Temperature

Storage:  $-40^{\circ}$  to  $66^{\circ}$  C ( $-40^{\circ}$  to  $150^{\circ}$  F)

Operating:  $5^{\circ}$  to  $50^{\circ}$  C ( $41^{\circ}$  to  $122^{\circ}$  F)

Relative Humidity

10% to 95% noncondensing

### **1.3 RELATED LITERATURE**

In addition to the M7950 print set, the *LSI-11 PDP-11/03 User's Manual* and the *LSI-11 PDP-11/03 Processor Handbook* contain useful information for installing and operating the DRV11-B general-purpose DMA interface. Handbooks may be ordered from the nearest Digital Equipment Corporation Sales Office.

## CHAPTER 2

### INSTALLATION

#### 2.1 GENERAL

Installation of the DRV11-B general-purpose DMA interface consists of selecting the device and interrupt vector addresses and then inserting the interface into an LSI-11 processor system.

#### 2.2 SYSTEM CONSIDERATIONS

Before installing the DRV11-B into an LSI-11 system, consideration must be given to bus loading, power, priority, and space requirements.

##### 2.2.1 LSI-11 Bus Loading

The DRV11-B presents one bus load to the LSI-11 bus. Fifteen (15) bus loads can be handled by the LSI-11 bus; therefore, the user must determine the LSI-11 bus load when installing additional LSI-11 modules.

##### 2.2.2 Power Requirements

The DRV11-B requires  $+5\text{ V} \pm 5\%$  @ 1.9 A (nominal). Power for the DRV11-B is obtained from the LSI-11 system power supply.

##### 2.2.3 Priority Requirements

Each device on the LSI-11 bus has an interrupt and DMA priority based on its relative position from the processor. Since the user may install the DRV11-B on the bus along with other devices that use the same interrupt or DMA priority, the user must bear in mind that when more than one device is requesting service, the device electrically nearest the LSI-11 microprocessor has the highest priority and will be serviced first. In addition, if the REV11 DMA refresh option is used, the REV11 must be at a priority level higher than that of the DRV11-B. Refer to the *LSI-11 PDP-11/03 User's Manual, Appendix G* for detailed information on the REV11 options.

##### 2.2.4 Space Requirements

The DRV11-B requires four module slots. Of the four slots, the A and B module fingers must interface to the LSI-11 bus. The C and D fingers maintain interrupt and DMA grant continuity as well as power and ground.

#### 2.3 USER I/O CABLES

The DRV11-B has two 40-pin connectors which provide the interface to the user's device. Two cable assemblies are required. It is recommended that cable assemblies from Table 2-1 be used to connect the DRV11-B to the user's device. The listed cables are terminated (one or both ends) with H856 40-pin connectors that mate with the connectors on the DRV11-B. Cable selection is determined by the type of connections used on the user's device. The desired cable length (XX) must be specified when ordering. (Lengths longer than 50 feet are not recommended for use with the DRV11-B.) Cables may be ordered from the nearest Digital Equipment Corporation Sales Office. Non-standard length cables may be ordered at additional cost.

**Table 2-1 Recommended Cable Assemblies**

Cable No.	Connectors	Type	Standard Lengths (ft./m.)
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25, 50 ft. 0.305, 1.830, 3.050, 3.66, 6.100, 7.625, 15.250 m.
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50 ft. 1.830, 3.050, 4.575, 7.625, 15.250 m.

## 2.4 DEVICE ADDRESS SELECTION

The DRV11-B contains five registers:

- the WCR
- the BAR
- the CSR
- the input DBR
- the output DBR.

These registers must be addressed for data and status transfers between the DRV11-B and the LSI-11 processor. The two (2) DBRs use the same address. The register addresses are sequential by even numbers and are as follows:

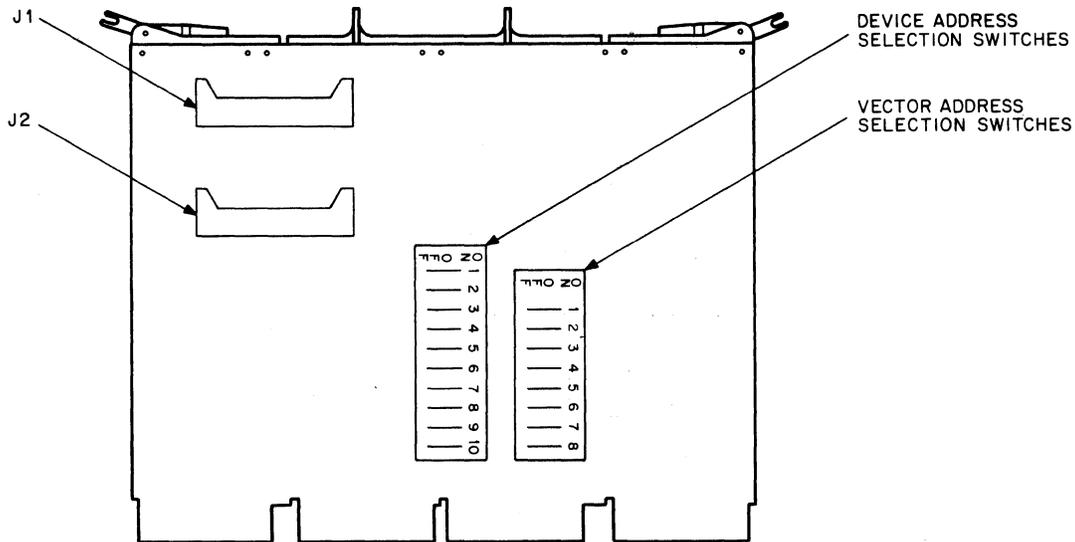
Register	BBS7	Octal Address
WCR	1	XXXXX0
BAR	1	XXXXX2
CSR	1	XXXXX4
DBRs	1	XXXXX6

The assigned DMA interface base address is  $772410_8$ . The user selects a base address for assignment to the WCR and sets the device address selection switches on the DRV11-B module to decode this address. The remaining BAR, CSR, and DBR addresses are then properly decoded by the module as they are received from the LSI-11 processor.

Figure 2-1 shows the location of the device address selection switches on the DRV11-B module. Switches are set to the ON (closed) position for bits to be decoded as "ONE" bits in the base address. Bits decoded as "ZERO" bits in the address have their switches set to the OFF (open) position. Figure 2-2 shows the address select format and presents the switch-to-bit relationship for the device address selection switches.

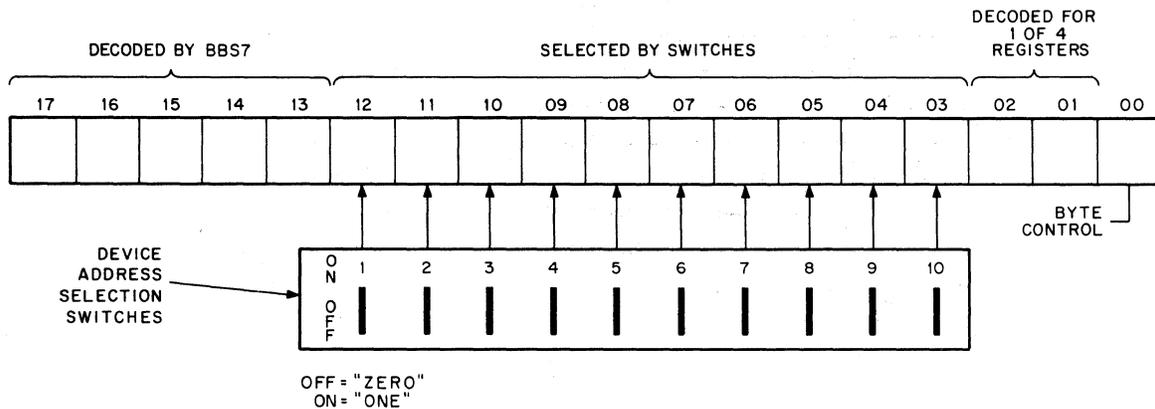
## 2.5 INTERRUPT VECTOR ADDRESS SELECTION

Vector addresses  $0-1774_8$  are reserved for LSI-11 system users. The DRV11-B is assigned vector address  $124_8$ . The user selects the interrupt vector address by means of switches on the DRV11-B module. Figure 2-1 shows the location of the vector address selection switches. Vector address selection switches are set to the ON (closed) position for bits to be encoded as "ONE" bits in the vector address. Bits encoded as "ZERO" bits in the address have their switches set to the OFF (open) position. Figure 2-3 shows the address select format and presents the switch-to-bit relationship for the vector address selection switches.



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Figure 2-1 DRV11-B Connector and Switch Locations

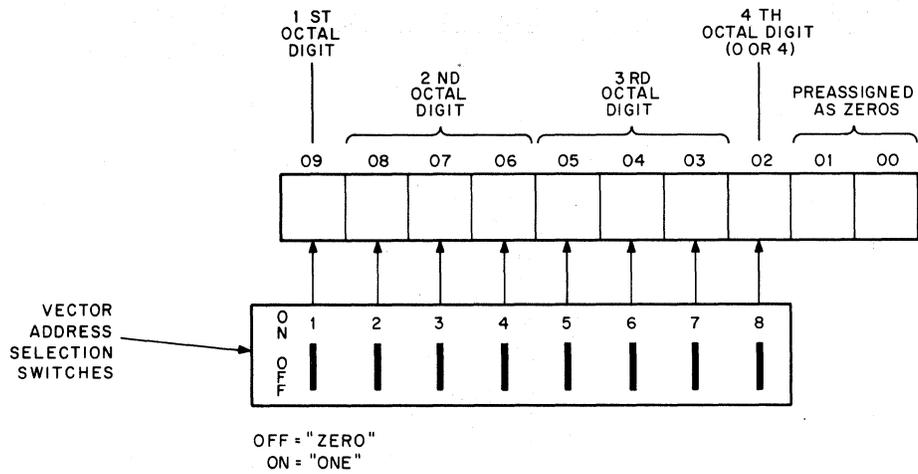


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Figure 2-2 DRV11-B Device Address Select Format

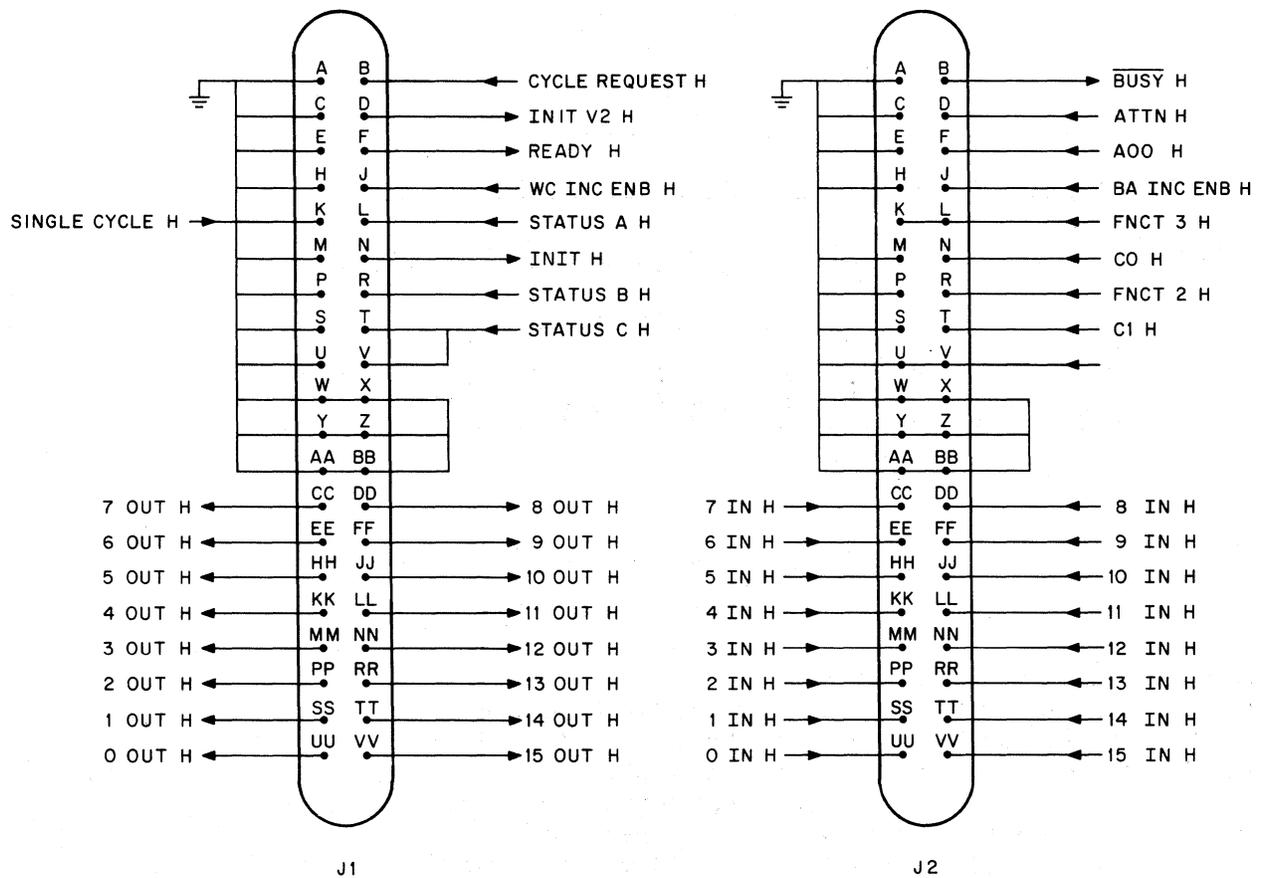
## 2.6 MODULE INSTALLATION

With the exception of the first four slots (the LSI-11 processor always occupies the first slots), the DRV11-B can be installed into any four slots (Paragraph 2.2.4) of the LSI-11 backplane. However, if REV11 DMA refresh option is used, the DRV11-B must be at a lower priority than the REV11. When inserting the module into the backplane, make sure that the deep notch on the module seats against the connector block rib. *Do not insert or remove the module with power applied.* After performing the initial turn-on (Paragraph 2.7), connect the user's I/O cables to J1 and J2 on the DRV11-B I/O connectors. Connector locations for the DRV11-B are shown in Figure 2-1. Pin assignments for J1 and J2 are shown in Figure 2-4 and are specified in Paragraph 1.2.



11-4185

Figure 2-3 DRV11-B Interrupt Vector Address Select Format



11-4159

Figure 2-4 DRV11-B Connector Pin Assignments

## 2.7 INITIAL TURN-ON

After completing the module installation, turn on the LSI-11 and initialize the system. With no I/O cables connected, and using the LSI-11 terminal and operating procedures, perform the following:

1. Load the addresses of the WCR, BAR, CSR, and DBRs through the system terminal and examine the locations. The terminal will indicate the following:

WCR contents will be 000000  
BAR contents will be 000001  
CSR contents will be 127200  
DBR contents will be 177777

2. The WCR and BAR can be loaded with data from the system terminal and the corresponding data read back on the terminal. BAR bit 0 will read as a one (1) with no I/O cables connected.

The user's I/O device cables can now be connected to the DRV11-B (Figure 2-1).

## 2.8 DIAGNOSTIC PROGRAM

The check procedure performed in Paragraph 2.7 does not completely verify the operation of the DRV11-B. Complete module operation can be verified through the use of the diagnostic software program MAINDEC-MD-11-DVDRA-PB. The program can be loaded into the LSI-11 system by means of a paper tape reader or a terminal. A BC08R maintenance cable (not longer than 50 ft) is required to loop the DBR output to the DBR input for checking the I/O data path. A complete description of the diagnostic software program and its implementation is provided in MAINDEC-MD-11-DVDRA-D.

## CHAPTER 3

### BASIC OPERATION

#### 3.1 GENERAL

This chapter contains a functional description of the DRV11-B. The DRV11-B registers are described as well as user device and bus operations necessary to perform DMA transfers. Figure 3-1 is a block diagram of the DRV11-B. All descriptions are written to this diagram. The chapter ends with a brief description of the timing associated with DMA transfers.

#### 3.2 FUNCTIONAL DESCRIPTION

##### 3.2.1 DRV11-B Registers

The DRV11-B contains five (5) registers:

- Word Count Register (WCR)
- Bus Address Register (BAR)
- Control Status Register (CSR)
- Input and Output Data Buffer Registers (DBRs).

**3.2.1.1 Word Count Register (WCR)** – The WCR is a 16-bit read/write register that controls the number of transfers. This register is loaded (under program control) with the 2's complement of the number of words to be transferred. At the end of each transfer, the word count register is incremented. When the contents of the WCR is incremented to zero, transfers are terminated, READY is set, and if enabled, an interrupt is requested. The WCR is word-addressable only.

**3.2.1.2 Bus Address Register (BAR)** – The BAR is a 15-bit read/write register. This register is loaded (under program control) with a bus address (not including address bit 0) which specifies the location to or from which data is to be transferred. The BAR is incremented after each transfer and can be incremented across 32K memory boundaries via the extended address feature of the DRV11-B. Systems with only 16 address bits will “wrap-around” to location zero when the extended address bits are incremented. The BAR is word-addressable only.

**3.2.1.3 Control/Status Register (CSR)** – The CSR is a 16-bit register used to control the functions and monitor the status of the interface. Bit 00 is a write-only bit and always reads as a zero. Bits 01–06, and bits 08 and 12 are read/write bits, while bits 07, 09–11, and 13–15 are read-only bits. Bit 14 can be written to a zero. Bits 04 and 05 are the extended addressing bits. CSR bit functions are fully described in Chapter 4. The CSR is both byte- and word-addressable.

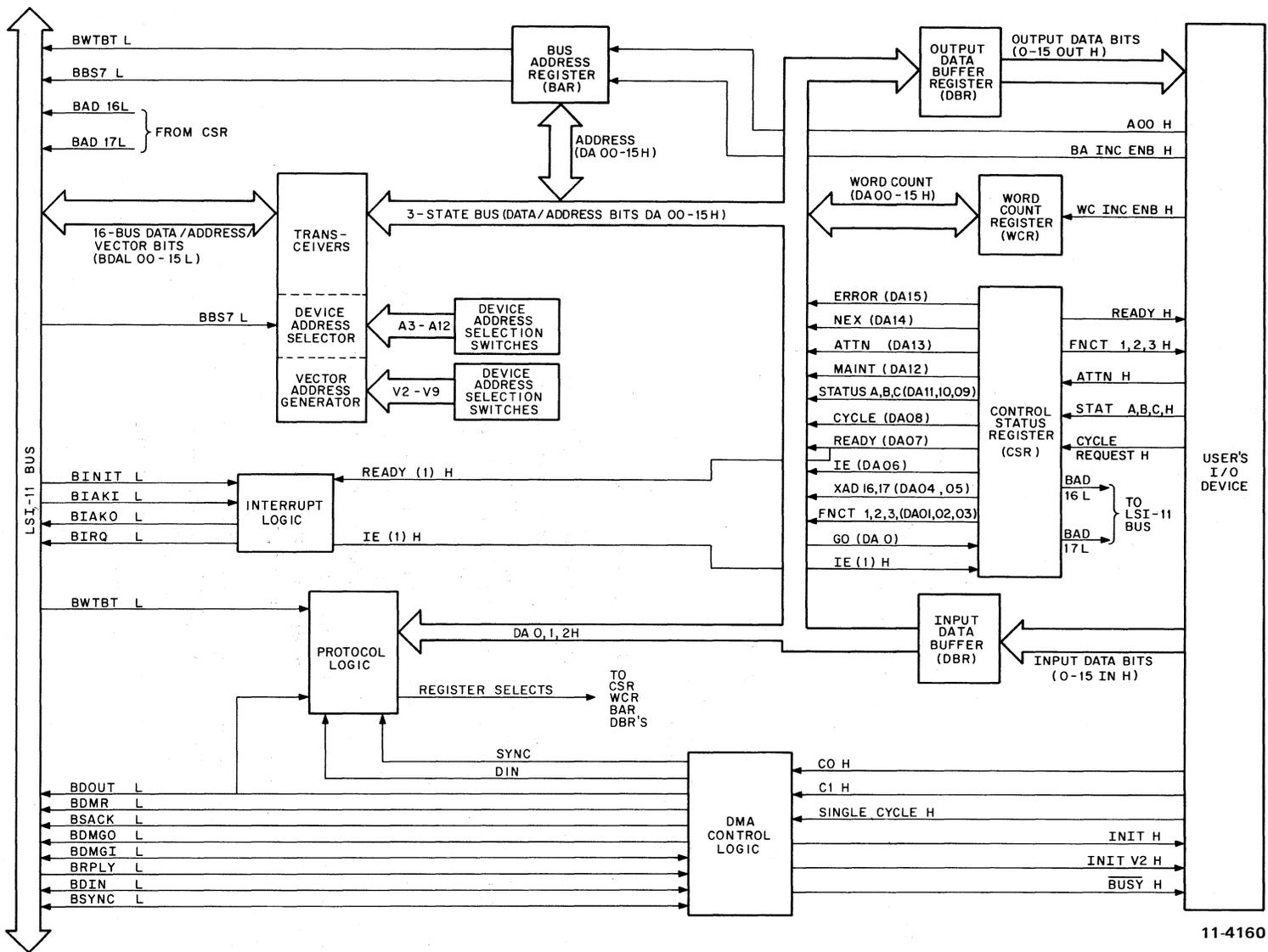


Figure 3-1 DRV11-B Block Diagram

**3.2.1.4 Input and Output Data Buffer Registers (DBRs)** – The two DBRs are 16-bit registers. The input DBR is a read-only register; the output DBR is a write-only register. Data is loaded into the input DBR by the user's device and subsequently transferred to memory under DMA control by the DRV11-B, or under program control by the LSI-11 processor. Conversely, data is written into the output DBR from memory under DMA control by the DRV11-B, or under program control by the LSI-11 processor, and read by the user's device. The input and output DBRs interface to the user's device by means of two separate 40-pin I/O connectors. These connectors may be cabled together (for maintenance purposes) to function as a read/write register. The input and output DBRs share the same bus address and are byte- and word-addressable.

**3.2.2 User Interface Lines**

There are 50 interface lines (25 per connector) between the DRV11-B and the user's I/O device. Of these lines, 32 are I/O data lines, 3 are for status, and 15 are for control. A brief description of these interface lines follows:

<b>Mnemonic</b>	<b>Description</b>
00 OUT – 15 OUT	16 TTL data output lines from the DRV11-B. One = high.
00 IN – 15 IN	16 TTL data input lines from the user's device. One = high.
STATUS A, B, C	Three TTL status input lines from the user's device. The function of these lines is defined by the user.
FUNCT 1, 2, 3	Three TTL output lines to the user's device. The function of these lines is defined by the user.
INIT	One TTL output line; used to initialize the user's device.
INIT V2	One TTL output line; present when INIT is asserted or when FUNCT 2 is written to a one. Used for interprocessor buffer applications.
A00	One TTL input line from the user's device. This line is normally high for word transfers. During byte transfers this line controls address bit 00.
BUSY	One TTL output line to the user's device. BUSY is low when the DRV11-B DMA control logic is requesting control of the LSI-11 bus or when a DMA cycle is in progress. A low-to-high transition indicates end of cycle.
READY	One TTL output line to the user's device. When the READY line goes low DMA transfers may be initiated by the user's device.
C0, C1	Two (2) TTL input lines from the user's device. These lines control the LSI-11 bus cycle for DMA transfers. C0, C1 codes for the four (4) possible bus cycles are listed in Table 3-1.

**Mnemonic****Description****Table 3-1 C0, C1 Codes**

<b>Bus Cycle</b>	<b>C0</b>	<b>C1</b>
DATI	0	0
DATIP	1	0
DATO	0	1
DATOB	1	1

SINGLE CYCLE

One TTL input line from the user's device. This line is internally pulled high for normal DMA transfers. For burst mode operation SINGLE CYCLE is driven low by the user's device.

**CAUTION**

When single cycle is driven low, total system operation is affected because the LSI-11 bus becomes dedicated to the DMA device and other devices, including the MOS memory refresh function, cannot use the bus.

WC INC ENB

One TTL input line from the user's device. This line is normally high to enable incrementing the DRV11-B word counter. Low inhibits incrementing.

BA INC ENB

One TTL input line from the user's device. This line is normally high to enable incrementing the bus address counter. Low inhibits incrementing.

CYCLE REQUEST

One TTL input line from the user's device. A low-to-high transition of this line initiates a DMA request.

ATTN

One TTL input line from the user's device. This line is driven high to terminate DMA transfers, to set READY and request an interrupt if the interrupt enable bit is set.

**3.2.3 LSI-11 Bus Lines**

There are 34 LSI-11 bus signal lines used by the DRV11-B; 16 of these are multiplexed and bidirectional lines which carry data and address bits. Two lines are used for extended address bits, while 16 lines are used for control signals. A brief description of the 34 bus lines follows:

**Mnemonic****Description**

BDAL 0 - BDAL 15

16 bus data/address lines. An address is first placed on these lines followed by the data. These lines are asserted when driven low.

BAD 16, 17

Two (2) bus lines used to address beyond 32K of memory by the DRV11-B. These lines are asserted when low.

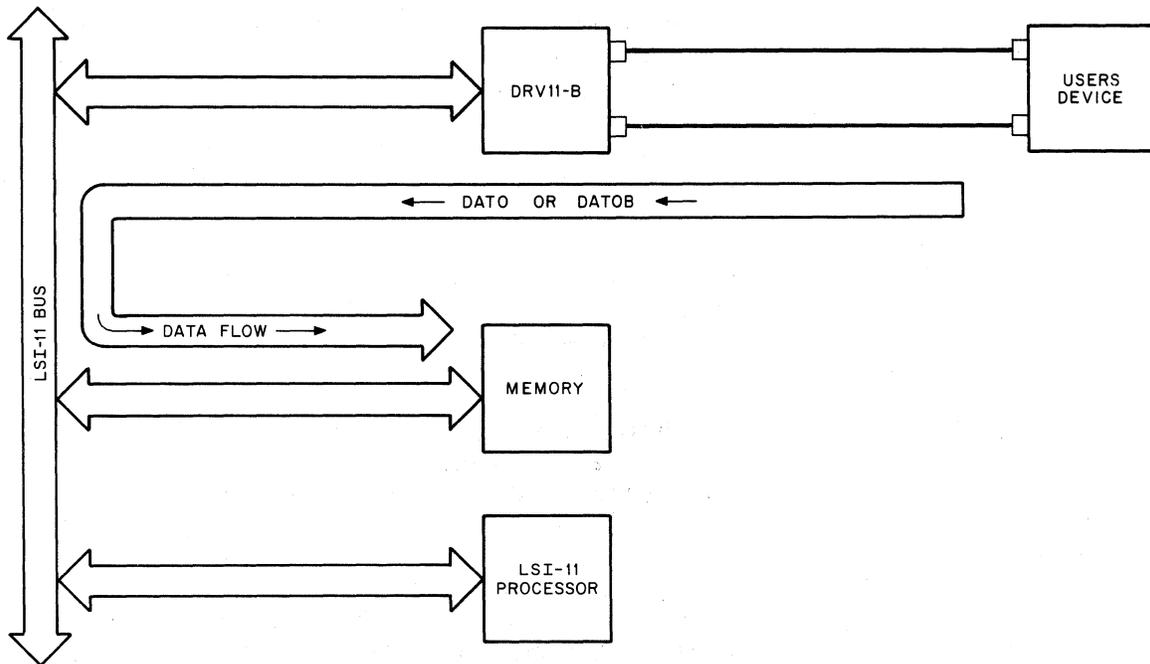
BDOUT

One bus line; when asserted (low) indicates that data is available on the BDAL lines and an output transfer (with respect to the bus master) is taking place.

<b>Mnemonic</b>	<b>Description</b>
BRPLY	One bus line; asserted (low) in response to BDIN or BDOUT and in response to BIAK transactions. It is generated by the slave device for address recognition.
BDIN	One bus line; when asserted (low) during BSYNC time, indicates an input transfer (with respect to the bus master). Requires a BRPLY response. BDIN is asserted when the bus master is ready to accept data from the slave. When asserted without BSYNC, indicates that an interrupt operation is occurring.
BSYNC	One bus line; asserted (low) by the bus master to indicate that it has placed an address on the BDAL lines. The transfer is in progress until BSYNC is negated (high).
BWTBT	One bus line; asserted (low) during address time to indicate that an output sequence (DATO or DATOB) is to follow. BWTBT is also asserted during data time for byte addressing during a DATOB.
BIRQ	One bus line; device asserts (low) this line when its interrupt enable, interrupt request, and ready flip-flops are set. BIRQ informs the LSI-11 processor that service is requested.
BIAKI, BIAKO	Two bus lines; one (1) is interrupt acknowledge in, the other is interrupt acknowledge out. BIAKI is generated by the LSI-11 processor in response to BIRQ. The processor asserts (low) BIAKO which is routed to the BIAKI pin of the first device on the bus. If the device is not requesting an interrupt BIAKO is passed (as BIAKI) to the next device.
BBS7	One bus line; asserted (low) by the LSI-11 processor when addressing a device for program-controlled transfers. The DRV11-B can assert BBS7 and address other devices on the LSI-11 bus without processor intervention.
BDMGi, BDMGO	Two bus lines; one is DMA grant in, the other is DMA grant out. The LSI-11 processor generates BDMGO which is routed to the BDMGI pin of the first bus device. If the device is requesting the bus, it will inhibit passing BDMGO to the next bus device. If the device is not requesting the bus, it will pass BDMGO (as BDMGI) to the next device.
BINIT	One bus line; asserted (low) by the LSI-11 processor to initialize or clear devices connected to the LSI-11 bus.
BSACK	One bus line; BSACK is asserted (low) by a DMA device in response to the LSI-11 processor's BDMGO signal, indicating that the DMA device is bus master.
BDMR	One bus line; a device asserts this signal for DMA requests and to become bus master.

### 3.2.4 User's I/O Device to LSI-11 Memory Transfer (DATO or DATOB)

Data transfers from the user's I/O device to the LSI-11 memory are DMA transfers. Figure 3-2 illustrates the data flow for a DMA DATO or DATOB cycle. Referring to Figure 3-1, DMA transfers are initialized under program control by loading the DRV11-B WCR (in 2's complement) with a count equal to the number of words to be transferred; loading the BAR with the starting memory address for word storage; and setting the CSR for transfers.



11-4187

Figure 3-2 DMA DATO/DATOB Data Flow Diagram

When the GO bit of the CSR is written to a "one," READY goes low and the user's I/O device conditions the A00, BA INC ENB, WC INC ENB, ATTN, SINGLE CYCLE (high for normal DMA transfers), and the C0, C1 (refer to Table 3-1) lines, and then asserts CYCLE REQUEST. The INPUT DATA BITS and control bits (C0, C1 and SINGLE CYCLE) are latched into the respective DRV11-B registers. CYCLE REQUEST sets CYCLE and causes the DRV11-B to assert BDMR which makes an LSI-11 bus request and causes BUSY to go low. In response to BDMR, the processor asserts BDMGO which is received as BDMGI. The DRV11-B becomes bus master and asserts BSACK and negates BDMR. The processor then terminates the bus grant sequence by negating BDMGO.

As bus master, the DRV11-B performs a DATO or DATOB bus cycle by placing the memory address on BDAL lines, asserting BWTBT, and then asserting BSYNC. The LSI-11 memory decodes the address; then, the DRV11-B removes the address from the BDAL lines, negates BWTBT (BWTBT will remain active for a DATOB) and then places the user's input data on the BDAL lines and asserts BDOUT. Memory receives the data and asserts BRPLY. In response to BRPLY, the DRV11-B negates BDOUT and then removes the user's input data from the BDAL lines. Memory now negates BRPLY, the bus cycle is terminated, and the bus is released when the DRV11-B negates BSACK and BSYNC.

At the end of the first transfer, the DRV11-B WCR and BAR are incremented, BUSY goes high, while READY remains low. With BUSY high and READY low, the user's I/O device can initiate another DATO or DATOB cycle by again asserting CYCLE REQUEST. DMA transfers can continue until the WCR increments to zero and generates an interrupt request, if the interrupt enable bit is set.

**3.2.4.1 Interrupts** – When the WCR increments to zero, READY goes high and the DRV11-B generates an interrupt request (if the interrupt circuits are enabled). The LSI-11 processor responds to the interrupt request (BIRQ) by asserting BDIN followed by BIAKI (interrupt acknowledge). BIAKI is received by the DRV11-B and in response places a vector address on the BDAL lines, asserts BRPLY, and negates BIRQ. The LSI-11 processor receives the vector address and negates BDIN and BIAKI. The DRV11-B now negates BRPLY, while the processor exits from the main program and enters a service program for the DRV11-B as indicated by the vector address.

Interrupt requests from the DRV11-B occur for the following conditions:

1. When the WCR increments to zero – this is a normal interrupt at the end of a designated number of transfers.
2. When the user's I/O device asserts ATTN – this is a special condition interrupt which may be defined by the user to override the WCR.
3. When a nonexistent memory location is addressed by the DRV11-B – this special condition interrupt is produced when no BRPLY is received from the LSI-11 memory.

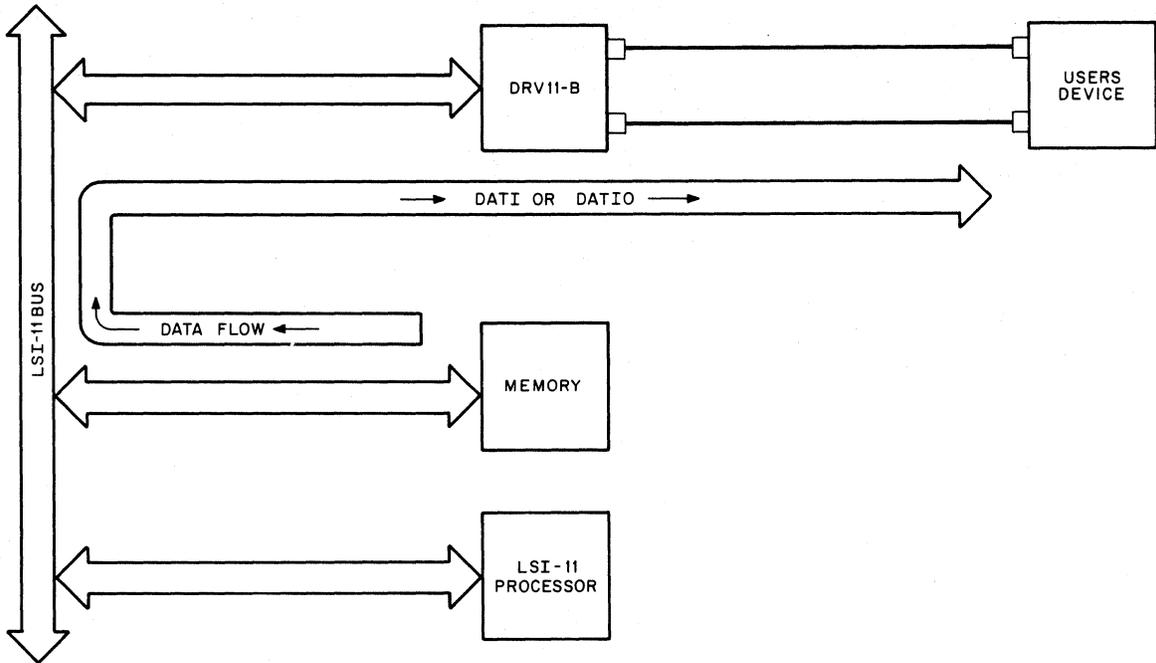
Interrupts are explained in greater detail in Chapter 4 of this manual.

### **3.2.5 LSI-11 Memory to User's Device Transfers (DATIO or DATI)**

DMA transfers from the LSI-11 memory to the user's I/O device occur in a manner similar to that described for user's I/O device to memory transfers. Figure 3-3 illustrates the data flow for a DMA DATIO or DATI cycle. Under program control, the DRV11-B WCR (Figure 3-1) is loaded with a count equal to the number of transfers, while the BAR is loaded with the starting address from which the first word will come; the CSR is set for transfers.

With the CSR set, READY goes low and the user's I/O device conditions the C0, C1 lines (refer to Table 3-1) for a DATI or a DATIO and conditions the WC INC ENB, BA INC ENB, ATTN, SINGLE CYCLE (high for normal DMA transfers), and asserts CYCLE REQUEST. BUSY from the DRV11-B goes low and the user's control bits are latched into the DRV11-B. The DRV11-B then asserts BDMR which makes a bus request. When the request is arbitrated as described in Paragraph 3.2.4, the DRV11-B becomes bus master.

When the DRV11-B becomes bus master, a DATI or DATIO bus cycle is performed (a DATI is described). The DRV11-B places the address of the memory location from which the first word is taken on the BDAL lines and asserts BSYNC. Memory decodes and latches the address. The DRV11-B then removes the address from the BDAL lines and asserts BDIN. Input data is now placed on the BDAL lines by the memory and the memory asserts BRPLY. The input data is accepted by the DRV11-B and BDIN is negated. Memory negates BRPLY and the DRV11-B negates BSACK and BSYNC to terminate the bus cycle and release the bus. The OUTPUT DATA BITS for the user's I/O device are stored in the DRV11-B output data buffer register. These bits can be read by the user's device at the low-to-high transition of BUSY.



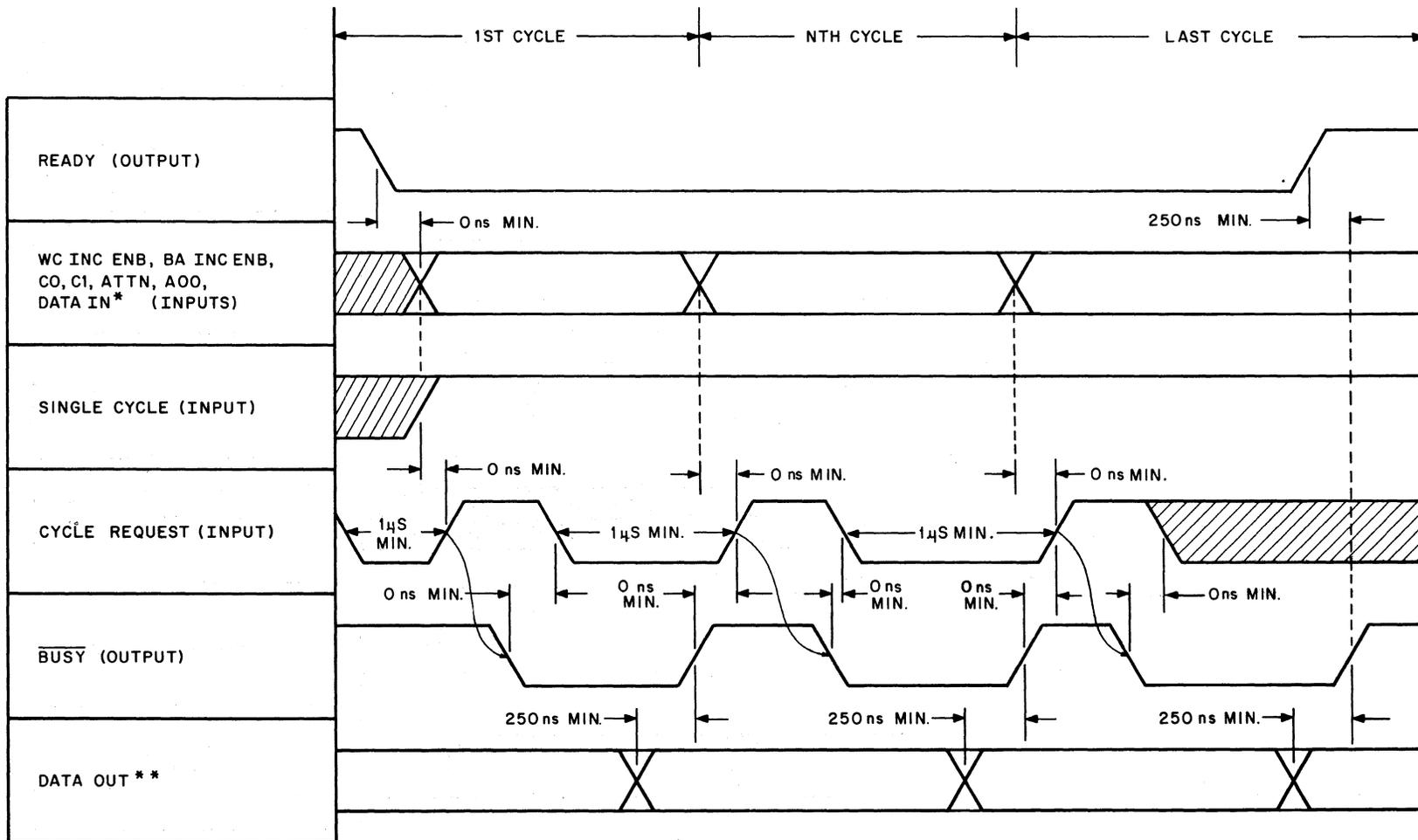
11-4188

Figure 3-3 DMA DATIO/DATI Data Flow Diagram

At the end of the first transfer, the DRV11-B WCR and BAR are incremented, BUSY goes high, while READY remains low. The user's device can initiate another DATI or DATIO cycle by again setting CYCLE REQUEST. DMA transfers to the user's device can continue until the WCR increments to zero and causes an interrupt request to be generated (Paragraph 3.2.4.1).

### 3.3 TIMING

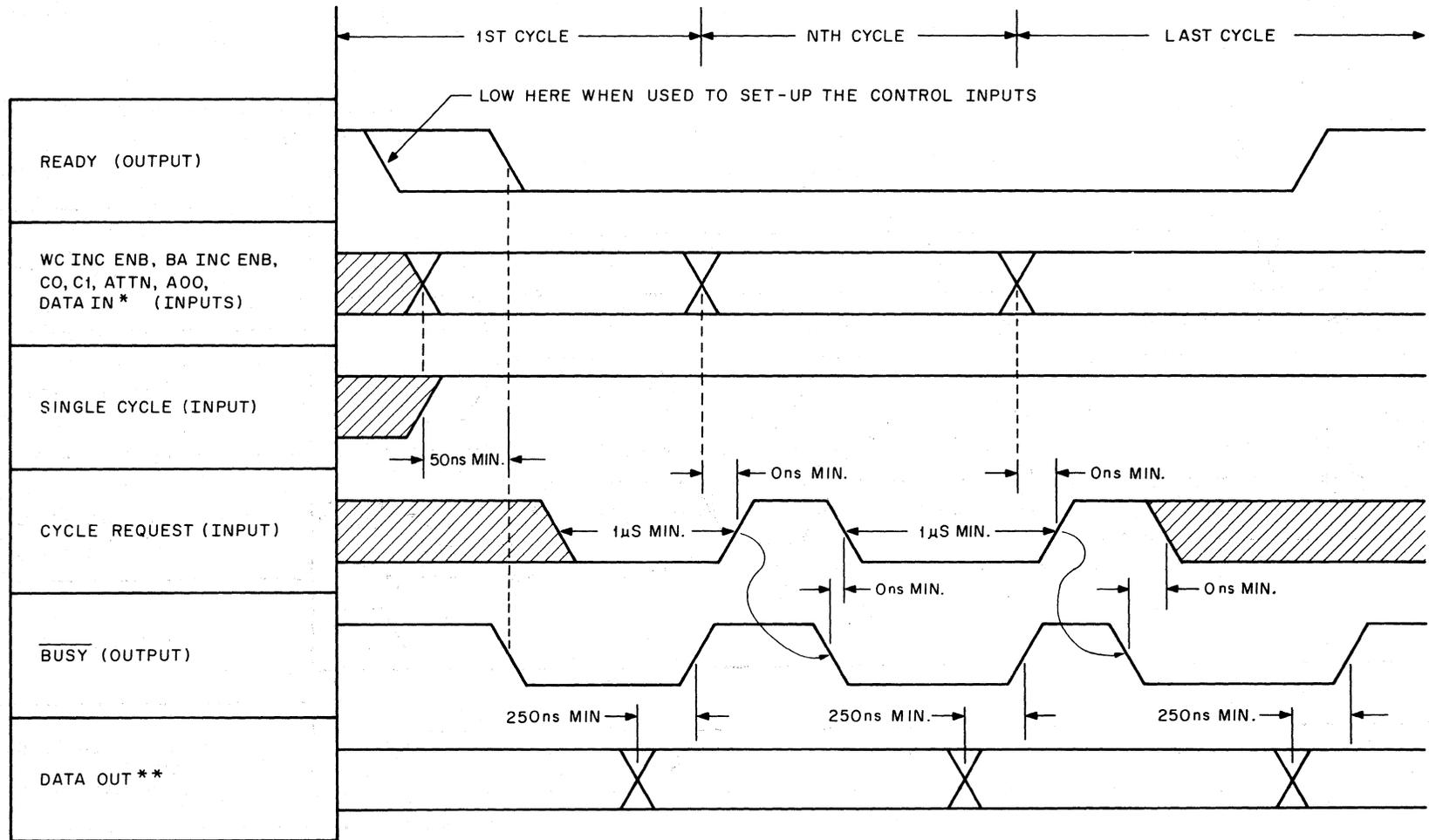
Input and output timing for the DRV11-B is shown in Figures 3-4 through 3-7. The timing diagrams show user signal timing for single cycle and burst mode operations which can be either program- or user-initiated.



LEGEND:

- \* = DATO OR DATOB BUS CYCLE; C1 = 1
- \*\* = DATI OR DATIO BUS CYCLE; C1 = 0

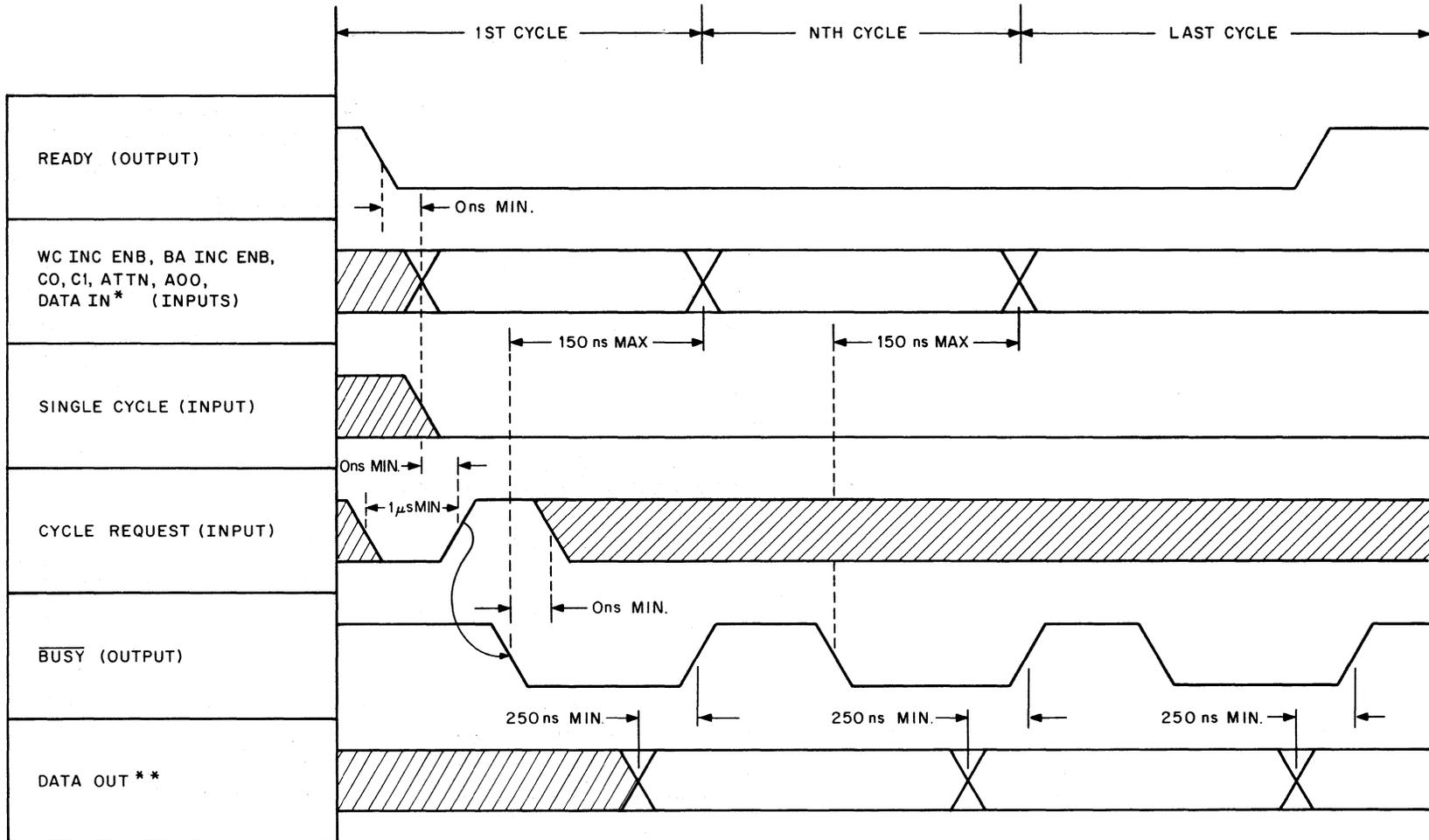
Figure 3-4 DRV11-B Single Cycle, User-Initiated, Timing Diagram



LEGEND:

- \* = DATO OR DATOB BUS CYCLE; C1 = 1
- \*\* = DATI OR DATIO BUS CYCLE; C1 = 0

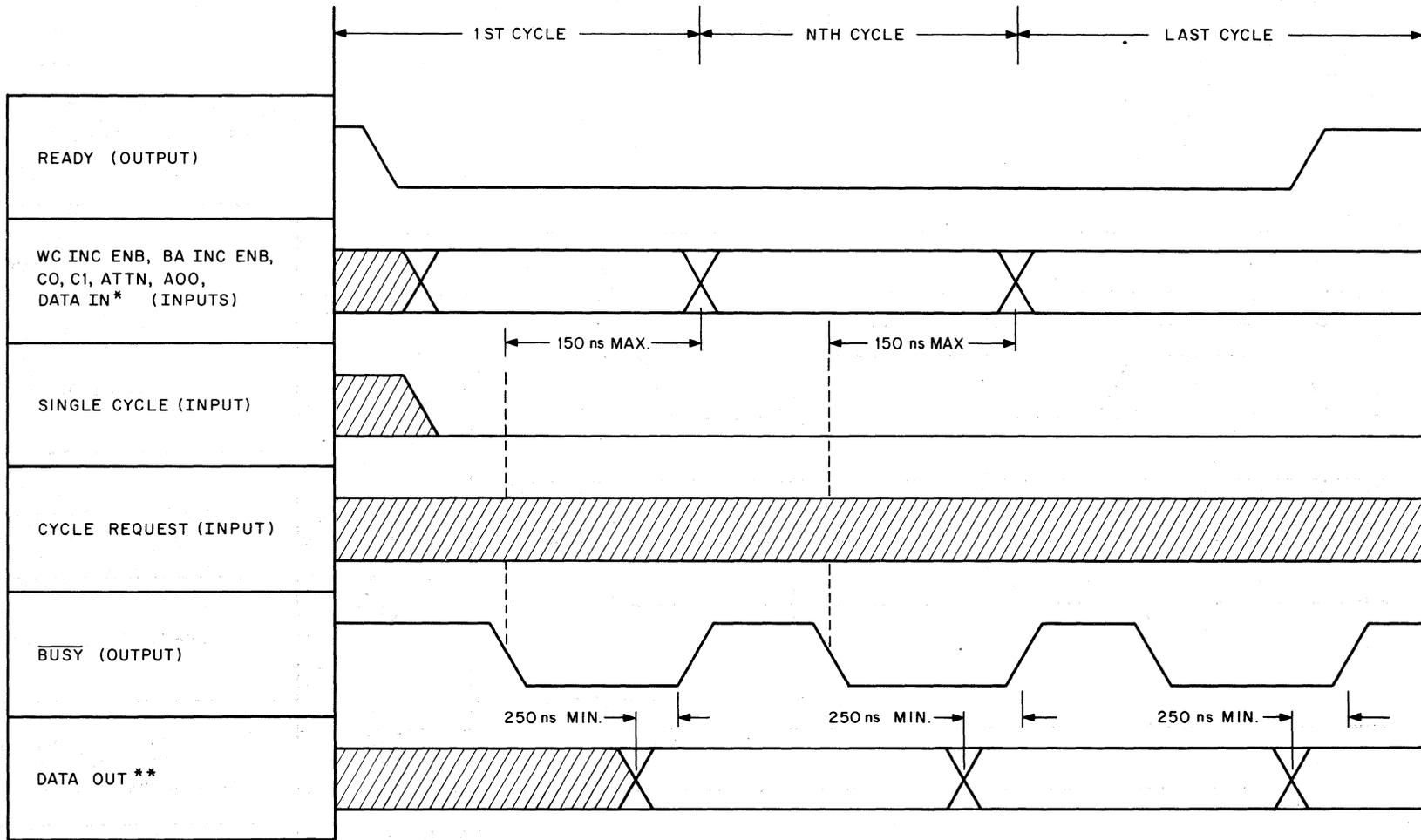
Figure 3-5 DRV11-B Single Cycle, Program-Initiated, Timing Diagram



LEGEND:

- \* = DATO OR DATOB BUS CYCLE; C1 = 1
- \*\* = DATI OR DATIO BUS CYCLE; C1 = 0

Figure 3-6 DRV11-B Burst Mode, User-Initiated, Timing Diagram



LEGEND

- \* = DATO OR DATOB BUS CYCLE; C1 = 1
- \*\* = DATI OR DATIO BUS CYCLE; C1 = 0

Figure 3-7 DRV11-B Burst Mode, Program-Initiated, Timing Diagram

## CHAPTER 4

### PROGRAMMING

#### 4.1 GENERAL

This chapter presents basic programming information for the DRV11-B. The types of programming instructions, the use of the registers, program interrupts, and special program considerations are presented.

#### 4.2 PROGRAMMING INSTRUCTIONS

All programming instructions used for the LSI-11 processor may be used for programming the DRV11-B.

#### 4.3 DRV11-B REGISTERS

Five registers are used by the DRV11-B:

- Word Count (WCR)
- Bus Address (BAR)
- Control/Status (CSR)
- Input and Output Data Buffers (DBRs).

The input and output data buffer registers share the same bus address while WCR, BAR and CSR have unique addresses.

##### 4.3.1 WCR

Load the 16-bit WCR with the 2's complement (negative number) of DMA data transfers. At the end of each DMA cycle, the WCR is incremented by one. When the last transfer is made, the WCR is incremented to zero and an interrupt is requested. The WCR is not byte-addressable.

##### 4.3.2 BAR

Load the 15-bit BAR with the address that specifies the memory location into which the first word is written, or from which the first word is read. Following the transfer of each word, the BAR is incremented by two, to point to the next higher sequential memory word location. If the BAR overflows, it will increment the extended address bits and "wrap-around" to location zero. Address bit A00, used for byte transfers, is driven by the user's device. The BAR is not byte-addressable.

##### 4.3.3 CSR

The 16-bit CSR is monitored for interface status and loaded with control bits. The CSR is byte-addressable. Figure 4-1 shows the CSR bit assignments. The function of each bit is described in Table 4-1.

##### 4.3.4 DBRs

The DBRs hold the 16-bit data words for transfer to memory from the user's I/O device (input DBR), or from the memory to the user's I/O device (output DBR). Both DBRs share the same bus address and are word- and byte-addressable.

#### 4.4 PROGRAM INTERRUPTS

DRV11-B interrupts are enabled by setting bit 06 (IE) of the CSR when the GO bit (bit 00) is issued (Figure 4-1 and Table 4-1). Interrupts can occur for the following reasons:

1. Word count overflow (normal interrupt)
2. CSR ERROR bit (bit 15) set (special condition)

##### 4.4.1 Word Count Overflow

An interrupt request is generated when the DRV11-B WCR increments to zero and produces WC OFLO (word count overflow). WC OFLO sets READY in the CSR at the end of the DMA cycle.

##### 4.4.2 CSR ERROR Bit (Bit 15)

The CSR ERROR bit can set for two possible reasons:

1. when bit 14 (NEX) of the CSR is set, or
2. when CSR bit 13 (ATTN) is set.

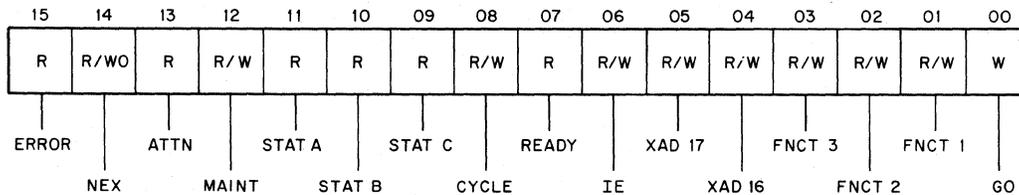
CSR bit 14 is set when a nonexistent (NEX) memory location is addressed and a reply from the addressed location is not received within 15  $\mu$ s.

Bit 14 will set if a DATO bus cycle does not occur 30  $\mu$ s after performing a DATIO bus cycle.

ATTN bit 13 sets the CSR ERROR bit when the user's I/O device drives ATTN high. ATTN is a user-defined function which can be utilized to generate an interrupt request.

#### 4.5 FUNCTION AND STATUS BITS

There are three function bits (FNCT 1, 2, 3) and three status bits (STAT A, B, C) which the user can employ (at his option) to control and indicate the status of the DMA transfers and/or the user interface. The function bits (CSR bits 01, 02, and 03) can be used to transfer control data to the user's interface via the OUTPUT DATA BIT lines of the DRV11-B. The status bits (CSR bits 09, 10, and 11) can be used to indicate that status information is on the DRV11-B INPUT DATA BIT lines.



**LEGEND:**

- R = Read only
- R/W = Read / Write
- R/WO = Read / Write to 0
- W = Write only. Always reads as a 0.

11-4186

Figure 4-1 CSR Format

**Table 4-1 CSR Bit Functions**

Bit	Function
00	<p>GO: Write-only bit; always reads as a zero.</p> <ol style="list-style-type: none"> <li>1. Causes READY to be sent to the user's device, indicating that a command has been issued.</li> <li>2. Allows DMA operation.</li> </ol>
01, 02, 03	<p>FNCT 1, 2, 3: Read/write bits.</p> <ol style="list-style-type: none"> <li>1. Three output bits available for user-defined functions.</li> <li>2. Cleared by INIT.</li> </ol>
04, 05	<p>XAD16, 17: Read/write bits. Two bits used for extended addressing. Bits 04 and 05 increment with the address count when the BAR "wraps-around" to zero.</p>
06	<p>IE: Read/write bit.</p> <ol style="list-style-type: none"> <li>1. Enables interrupts to occur when READY is set.</li> <li>2. Cleared by INIT.</li> </ol>
07	<p>READY: Read-only bit. Indicates that the DRV11-B is able to accept a new command. Set by INIT, WCOFLO, ERROR; cleared by GO (bit 00).</p>
08	<p>CYCLE: Read/write bit. CYCLE is used to prime a DMA bus cycle; set by CYCLE REQUEST, cleared during DMA cycle, INIT.</p>
09, 10, 11	<p>STAT A, B, C: Read-only bits. Three device status input bits that indicate the state of the DSTAT A, B, and C user signals.</p>
12	<p>MAINT: Read/write bit. Maintenance bit for use with the MAINDEC diagnostic.</p>
13	<p>ATTN: Read-only bit. Indicates the state of the ATTN user signal; sets READY, ERROR.</p>
14	<p>NEX: Read/write to zero bit.</p> <ol style="list-style-type: none"> <li>1. Nonexistent memory; indicates that as bus master, the DRV11-B did not receive BRPLY or that a DATIO cycle was not completed.</li> <li>2. Sets ERROR.</li> <li>3. Cleared by INIT or by writing it to a zero.</li> </ol>

**Table 4-1 CSR Bit Functions (Cont)**

<b>Bit</b>	<b>Function</b>
15	<p data-bbox="513 338 841 369"><b>ERROR:</b> Read-only bit.</p> <ol data-bbox="578 401 1438 804" style="list-style-type: none"><li data-bbox="578 401 1438 558">1. Indicates one of the following special conditions:<ol data-bbox="703 464 951 558" style="list-style-type: none"><li data-bbox="703 464 951 495">a. NEX (bit 14)</li><li data-bbox="703 520 951 558">b. ATTN (bit 13)</li></ol></li><li data-bbox="578 583 1438 615">2. Sets READY (bit 7) and causes an interrupt if IE (bit 6) is set.</li><li data-bbox="578 646 1438 804">3. Cleared by removing the special condition as follows:<ol data-bbox="703 709 1308 804" style="list-style-type: none"><li data-bbox="703 709 1308 741">a. NEX is cleared by writing bit 14 to a zero.</li><li data-bbox="703 766 1308 804">b. ATTN is cleared by the user device.</li></ol></li></ol>

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