AA-V523A-TV

Rainbow™ 100

PC100 System Module Specification

digital equipment corporation

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1.0 SYSTEM MODULE OVERVIEW

PC100 System Module is the basic intelligence of the system and provides the means for interconnection of all options. This module includes the following features:

1. 8088 CPU
2. Z80A CPU
3. 64KB Shared Dynamic Memory
4. 2KB Z80A Private RAM
5. 24KB ROM
6. 256 x 4 Non-Volatile Memory (NVM)
7. DC011, DC012 Video Electronics
8. Asynchronous/Bisynchronous Communications Port
9. Printer Port
10. Keyboard Interface
11. Floppy Controller
12. Option expansion capability
    - Extended communications
    - Color graphics
    - Extended memory (64/192 KB)

1.1 BLOCK DIAGRAM

The following figure represents the block diagram for the system module.

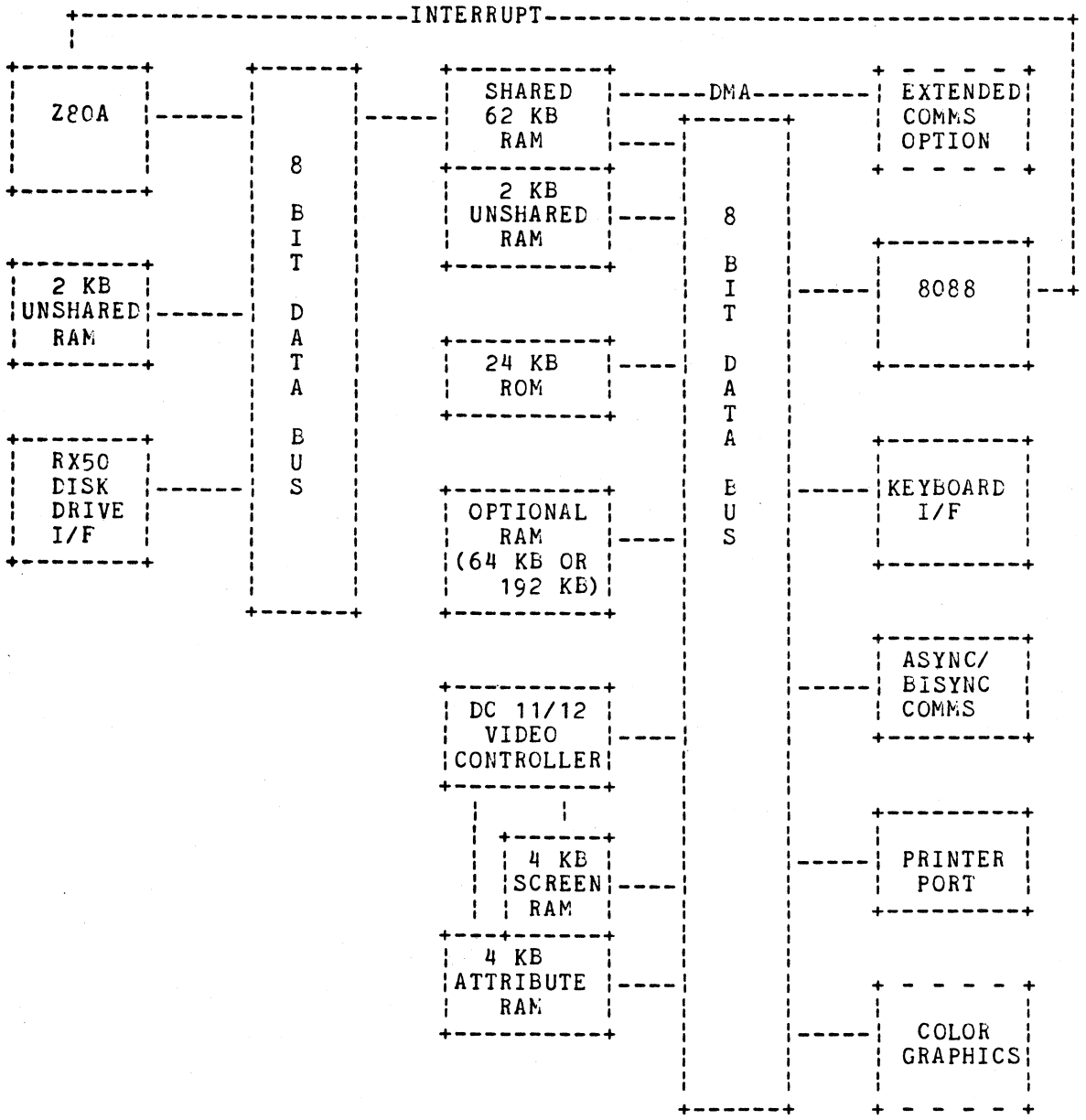


Figure 1. System Module Block Diagram

2.0 SYSTEM MODULE FUNCTIONAL SPECIFICATION

The PC100 includes a two-processor architecture based on the simultaneous operation of an 8088 and a Z80A CPU. These CPUs operate from and transfer data through a shared block of 62KB of RAM. In addition to this block of shared memory, each processor has its own memory and peripheral circuitry.

In addition to running application/user software, each processor supports a portion of the needed functions of the computer. The Z80A processor performs the functions required to read/write the floppy disks. The 8088 handles the video output, keyboard I/O, printer port and the communications as well as any other options.

2.1 8088 SYSTEM

2.1.1 8088 CPU

The 8088 microprocessor on the module controls nearly everything except the floppy disk. The 8088 microprocessor runs from a clock of 4.815 MHz (208 nS cycle) and controls the following:

- Video
- Keyboard
- Printer
- Communication line
- Optional graphics board
- Optional extended communications board
- Memory

1. 64KB dynamic memory (62KB shared)
2. 24KB ROM
3. 4KB video screen memory (static)
4. 4KB video attribute memory (static)
5. 256 X 4 non-volatile memory (NVM) with shadow RAM
6. 64KB or 192KB optional unshared dynamic memory

2.1.2 Memory

The various memory available to the 8088 consists of ROM, RAM, and non-volatile RAM.

2.1.2.1 **Shared Memory** - The standard 64KB bank of memory is shared with the Z80A processor. However, the Z80A is unable to address (and therefore can't modify) the first 2KB portion of this bank. Therefore, the 8088 keeps its interrupt vectors and some other information safe from being affected by a Z80A application. No parity generation/detection is implemented with the 64KB shared RAM.

If there is no contention for the shared RAM at the time of an 8088 access, no wait states are required for the cycle. If the RAM is busy due to a refresh cycle or a Z80A memory cycle, which was initiated prior to the 8088's request, wait states will occur until the request can be filled. Refresh has the highest priority for memory cycles. The 8088 has approximately equal priority with the Z80A except that the Z80A wins all ties.

2.1.2.2 **ROM** - There is 24KB of ROM (three sockets) on the module which is re-addressable by the 8088. The 24KB contains both Z80A code and 8088 code for diagnostics, bootstrap, and VT102 emulation. The code for the Z80A must be moved into shared memory by the 8088 in order to be executed by the Z80A.

No wait states are required when the 8088 accesses this memory; however, because the circuitry assumes that all memory is dynamic RAM, wait states will be excecuted whenever refresh cycles are in progress.

Supported ROMs are of the 2732/2764 pinout variety, with access times <= 450 ns.

2.1.2.3 **4KB Screen Memory And 4KB Attribute Memory** - There is screen and attribute memory available to the 8088 that allows it to control what is on the CRT display. This memory is available to the 8088 90% of the time. In the remaining 10%, the DC011 and DC012 have access to this memory and prohibit the 8088 from access. Wait states to the 8088 will occur during refresh cycles and while the DC011 and DC012 are using the memory. The worst case time in which the 8088 can be held in a wait state due to contention with the DC011 and DC012 is 65 microseconds.

2.1.2.4 **256 x 4 NVM With Shadow RAM** - The PC100 mother board contains 1024 bits of non-volatile memory that is organized 256 x 4. The NVM, as it is called, is located on the 8088 CPU bus at address 0ED000H through 0ED0FFH and the data path to the device is through data bits 0, 1, 2, and 3. Phantom images of the NVM exist from address 0ED100H through 0EDFFFH.

The device contains a 256 x 4 bit static RAM that performs as any other static memory. The device also contains a 256 x 4 bit non-volatile memory that is overlaid with the 256 x 4 bit static memory. On initialization, the 8088 does a RECALL of the NVM which places that data into the static memory. At this time, any read or write to the memory occurs to the static memory. The RECALL is done via a bit in the Diagnostic Write register. On power-up, this bit is a 0, and is set to a 1 by the firmware.

To perform a RECALL, the bit is set to a 0 and then set back to 1. The minimum width for this pulse is 450 ns. The data is available immediately after the RECALL bit is reset. On power-up, the RECALL bit is a 0 to prevent spurious data from being stored into the device. Therefore, the RECALL bit must be set to a 1 by software after power-up.

The data that is in the static memory portion can be stored in the NVM by the 8088 CPU via the PROGRAM NVM bit also located in the Diagnostic Write register. This bit is also set to a 0 on power-up. To perform a PROGRAM NVM operation, the bit is set to a 1 and then back to a 0. This pulse has a minimum width of 100 ns. Once the PROGRAM NVM bit has met the minimum pulse width it can be removed, however, the device cannot be accessed by the CPU for 10 ms. At this time, the device is in the process of storing the data into the NVM. There is no indication to the CPU that the device is done other than 10 ms has passed. If another operation is done on the device during those 10 ms, it will be ignored. Once the operation is started, it cannot be terminated unless the power is turned off. In this case, data in the device is not valid.

2.1.2.5 **Unshared Dynamic Memory (Optional)** - The module can be optionally expanded with 64KB or 192KB of memory for use by the 8088. If installed, this memory is always available and never requires wait states (except when the memory cycle contends with a refresh cycle).

2.1.3 8088 I/O Map

The 8088 I/O map follows:

PORT H	FUNCTION	
00H	Interrupts Z80A Flop	(Write)
00H	Clears 8088 Interrupt Flop	(Read)
02H	Communications and LED Register	WO
02H	General Communications Status Register	RO
04H	DC011 Write Register	WO
06H	Communications Bit Rate Register	WO
0AH	Maintenance Port	WO
0AH	Maintenance Port	RO
0CH	DC012 Write Register	WO
0EH	Printer Bit Rate Register	WO
10H	Keyboard Data Register(8251A)	RO/WO
11H	Keyboard Control/Status Register(8251A)	RO/WO
20H-2FH	Ext. Comm. Option/Option Select 1	
40H	Comm Data Reg. (7201)	RO/WO
41H	Printer Data Reg. (7201)	RO/WO
42H	Comm Control/Status Reg. (7201)	RO/WO
43H	Printer Control/Status Reg. (7201)	RO/WO
50H-5FH	Graphics Option Select	R/W
60H-6FH	Ext. Comm. Option/Option Select 2	

2.1.4 8088 Memory Map

Figure 2 shows the 8088's memory map.

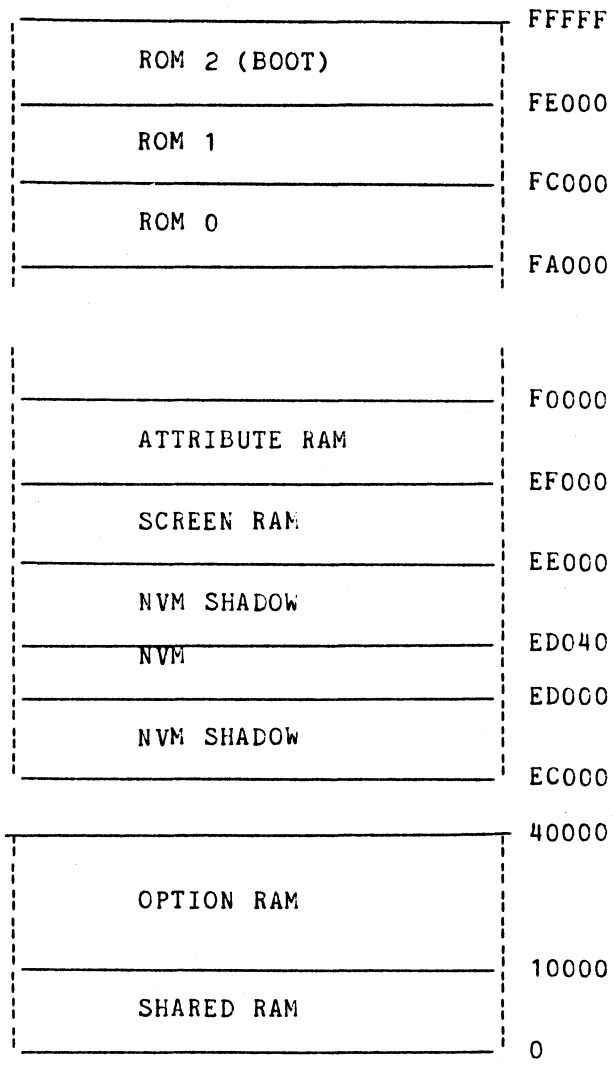


Figure 2. 8088 Memory Map

2.1.5 8088 Interrupts

The following table lists the 8088 interrupts.

Priority	Interrupt Source	Interrupt Vector Type (Hex)	Interrupt Vector Address (Hex)
Highest	Vertical Frequency Interrupt	20	80
↑	DMA Controller Interrupt (from Optional Extended Comm. Board)	23	8C
¦	Graphics Interrupt	22	88
¦	Comm./Printer (7201) Interrupt	24	90
¦	Extended Comms Interrupt (optional)	25	94
¦	Keyboard (8251A) Interrupt	26	98
Lowest	Interrupt from Z80A	27	9C

2.1.6 Video Subsystem: 8088

The video subsystem resides on the mother board and is controlled by the 8088. The subsystem provides fully VT100-compatible video features.

2.1.6.1 General Video Features - The video subsystem supports the following features:

1. 24 line x 83 column display
2. 24 line x 137 column display
3. Smooth scrolling (full screen and split screen)
4. Double height lines
5. Double width lines
6. Reverse video
7. Bold
8. Blinking
9. Underline
10. Composite video output
11. ROM-resident character patterns

The double height and double width attributes may be selected on a line by line basis. The other attributes (reverse, bold, blink, and underline) may be selected on a character-by-character basis.

2.1.6.2 **Composite Video Output** - The composite video output provides RS170 like output generated by combining the video signal with a composite sync signal.

Note

> The use of dc coupling is not in strict agreement with RS170. To agree with RS170, the output load would require a 10 uf capacitor in series with the output. Failing this, the 2 ma dc short circuit current requirement is violated. This presents no problem with most monitors which are in fact ac coupled.

The composite video output has the following nominal characteristics:

1. Output impedance = 75 ohms, dc-coupled
2. Sync level = 0 V
3. Black level = approximately 0.3 V when loaded with 75 ohms
4. White level = approximately 1.0 V with a 75 ohm load
5. The composite sync waveform conforms to EIA RS170 standards. The vertical interval is composed of six equalizing pulses, six vertical sync pulses, and six more equalizing pulses. The timing is as follows:

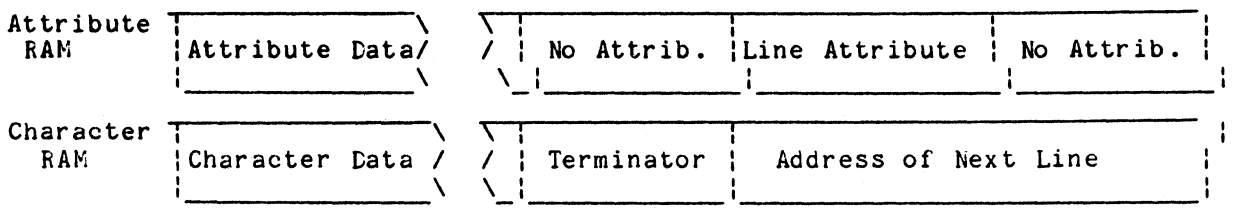
Equalizing pulse width	= 2.33 microseconds + 50 ns
Vertical pulse width	= 27.28 us + 200 ns
Horizontal pulse width	= 4.71 us + 50 ns
Horizontal blank width	= 11.84 us + 50 ns/80 column mode
	= 12.34 us + 50 ns/132 column mode
Front Porch	= 1.54 us + 50 ns

2.1.6.3 **Video Memory** - The video subsystem has 4KB of screen RAM and 4KB of attribute RAM. Only the four LSbs of the attribute RAM are actually looked at by the video subsystem.

2.1.6.4 **Video Processor (DC011 And DC012)** - When accessing the screen (DC011 and DC012) RAM, the video processor generates the 12-bit address for a particular byte in the lower 4KB bank (character RAM). The corresponding byte in the upper 4KB bank (attribute RAM) is selected also. The two bytes are passed to the video processor in parallel. The video processor uses the character code to index into a character generator and uses the attribute information to modify the video data.

The contents of the screen RAM directly control the display of the lines and characters. This region of memory contains the displayable characters, their attributes the line attributes, and the addresses that link one line to the next. The microprocessor modifies and updates this information in the intervals between the video processor's DMAs.

The video processor begins reading the screen RAM at the start of RAM (location 0EE000H) following each vertical reset. Three bytes of control data are located at the end of each line of characters. The first byte, called the terminator, is FF hex and is a unique character that the video processor recognizes as the end of the line. The next two bytes form an address (low byte followed by high byte) which points to the first character of the next line to be displayed. The byte of attributes which corresponds to the low byte of the address contains three bits of line attributes which are applied to the line being pointed to.



The bits are assigned in the following manner:

	D7	D6	D5	D4	D3	D2	D1	D0
Char. Attrib.	Unused	Unused	Unused	Unused	Not Under Line	Not Blink	Not Bold	Rev. Video
Char. Data	Alt. Char Set	Code for Character						
Line Attrib.	Unused	Unused	Unused	Unused	Unused	Double Width	Double Height	Scroll Region

(Smooth) scroll region - if set, this line scrolls: if not set, it doesn't

Double Height	Double Width	Result
0	0	bottom half double height
0	1	top half double height
1	0	double width
1	1	normal height, normal width

2.1.6.5 DC011 Programming Information - The DC011 video-timing chip can be accessed by the 8088 (WRITE-ONLY) at I/O address 4. The DC011 must be programmed with the desired refresh rate and column mode on power-up and after any mode changes. To program the DC011, write two of the following four codes:

Code	Configuration
00	80 column mode sets
10	132 column mode interlaced mode
20	60 Hz mode resets
30	50 Hz mode interlaced mode

Interlaced/non-interlaced mode is determined by the order in which 80/132 column and 50/60 Hz are set. Every time the DC011 is programmed, its internal timing chain is reset. Because this will cause the screen to jump, the DC011 should be programmed only if absolutely necessary. For example, the following two instructions will set the DC011 to 80-column, 60 Hz, no interlace:

```
MOV AX,2000H
OUT DC011,AX
```

Note

> When 80-column mode is selected, the video processor is actually capable of displaying 83 columns in single width mode or 41 columns in double width/height mode. When 132-column mode is selected, 137 columns can be displayed in single width mode or 68 columns in double width/height mode.

2.1.6.6 DC012 Programming Information - The DC012 video control chip can be accessed by the 8088 (WRITE-ONLY) at I/O address 0CH. The following codes are defined for the DC012:

Code	Result
00	set scroll latch LSBs to 00
01	set scroll latch LSBs to 01
02	set scroll latch LSBs to 10
03	set scroll latch LSBs to 11
04	set scroll latch MSBs to 00
05	set scroll latch MSBs to 01
06	set scroll latch MSBs to 10
07	set scroll latch MSBs to 11
08	toggle blink flip flop
09	clear vertical frequency interrupt
0A	set reverse field on
0B	set reverse field off
0C	not supported
0D	set basic attribute to reverse video w/ 24 lines and set blink flip-flop off.
0E	not supported
0F	set basic attribute to reverse video w/48 lines and set blink flip-flop off.

On power-up, the DCC12 can be programmed to bring it to a known state. Typically, codes 0C, 04, 09, 0B, and CD will be programmed at power-up time.

The value to which the scroll latch is set determines what scan row the first line of a scrolling region starts on. Likewise, it determines the last scan row displayed for the last line in a scrolling region.

For example, when the latch is set to zero (the degenerate case), the first line of the scroll region starts at scan row zero (so the line is completely visible).

The last line of the scrolling region terminates at scan row 9 (so this line is also completely visible). When the scroll latch is non-zero, for example 5, the first line of the scrolling region starts with scan row 5 (so only the bottom half of the line is visible). The last line of the scrolling region terminates at scan row 4 (so only the top half of the line is visible).

If on each successive frame, the scroll latch is incremented from 0 through 9 and back to 0 again, the screen appears to smooth scroll from bottom to top (assuming that line linkages and line attributes are properly handled). On the other hand, if the scroll latch is decremented from 0 to 9 then down through 0, the screen appears to smooth scroll from top to bottom (again assuming that all line linkages and line attributes are properly handled).

A scrolling region is defined as a group of lines with their scrolling attributes set, surrounded by lines whose scrolling attribute is not set. Note that the scrolling attribute for a line resides in the line pointer information at the end of the previous line. Also, the first line on the screen (the one at RAM location 0), has its scrolling attribute reset by definition. Also note that the definition of a scrolling region does not preclude the definition of more than one scrolling region per screen, although that is of dubious value.

Whenever the scroll latch is non-zero, each scrolling region on the screen requires an extra (scrolling) line to be linked in. For example, if the scrolling region is 10 lines long, when the scroll latch is set non-zero there will have to be an 11th line linked in. If scrolling up (incrementing the scroll latch), the line must be linked in at the bottom. When the scroll latch is incremented back to 0 again, the top line of the scrolling region must be unlinked. When scrolling down (decrementing the scroll latch), new lines must be linked in at the top of the scroll region and unlinked down at the bottom.

All line linking/unlinking should be done during the vertical blanking interval (after the vertical frequency interrupt is rung). In 60Hz mode, there are two blanked lines at the beginning of the screen (the line at RAM location 0, and the line that it points to).

The first line (at location 0) is guaranteed to have been read by the time that the interrupt service routine is entered; any changes to this line will not affect the screen until the next frame time.

However, the second line will not be read for over 500 microseconds after asserting the interrupt.

If it is to be changed, it must be changed very soon after entering the interrupt service routine in order to guarantee that the change will be visible in the current frame.

Therefore, if the first visible line on the screen is involved in the scroll region and is being either linked in or unlinked, then the vertical interrupt routine must guarantee that its pointer (which resides in the second invisible line) is changed within approximately 500 usec after the ringing of the interrupt.

The modification of the scroll latch is much less time critical than this. Since the scroll latch is loaded by the DC012 by the vertical reset at the beginning of each frame, the only requirement is that the scroll latch be modified before the next frame begins.

Note

> The scroll latch value is the value that will be used during the next frame rather than the current frame.

2.1.6.7 Character Generator ROM - The character generator is a 4K x 8 ROM with access time $\leq$ 300 nS. The standard ROM is a 2732A UVPROM. The ROM holds 255 characters corresponding to character codes 0-FE (hex) (character code FF is reserved for use as a terminator by the video subsystem). The character codes 0-FE correspond to addresses 0-FE0 in the character generator ROM (the final hex digit of the address indicates which scan row of the character is being addressed).
The following table relates the scan number to the scan address:

Scan Address	Character Scan Number
F	1 (Normally blank)
0	2 (Top of normal upper case character)
1	3
2	4
3	5
4	6
5	7
6	8 (Bottom of normal uppercase character)
7	9 Normal descenders (Underline scan)
8	10 Normal descenders
9-E	Unused (never displayed)

Each byte of information in the ROM at a valid scan address represents 8 bits of horizontal scan information. The low order bit is a fill bit; it is used not only as the rightmost bit in the character bit but also fills in the right hand space between characters (this inter-character space is two dots wide in 80 column mode and one dot wide in 132 column mode).

Scan Number	Character Generator Bit Positions 76543210007654321000	Scan Address
1	--------------------	F
2	---#----------------	0
3	--#-#---------------	1
4	-#---#----#-####----	2
5	#-----#---##----#---	3
6	######---##----#---	4
7	#-----#---#-####----	5
8	#-----#---#---------	6
9	----------#---------	7
10	----------#---------	8

2.1.7 Diagnostic Registers

The following registers are for the purpose of controlling diagnostics for the PC100.

2.1.7.1 Diagnostic Write Register: 8088 - This write only register (Port Address 0A hex) is used for diagnostic control purposes. Also contained in this register is a bit for the loopback of all communications transmit signals to the receive signals.

1. Bit 0 - This bit is used to reset the Z80A CPU from the 8088 side. This signal is active at power-up.
2. Bit 1 - When reset, the display will be blanked.
3. Bit 2 - When low, mother board video is selected. When high, graphics board video is selected.
4. Bit 3 - When high, this bit enables testing of the parity circuitry on the optional memory board.
5. Bit 4 - Diagnostic loopback - see Diagnostic Read Register. See subhead 2.1.7.4
6. Bit 5 - Comm. Loopback maintenance bit. See subhead 2.1.7.2.
7. Bit 6 - PROGRAM (write) NVM.
8. Bit 7 - RECALL (read) NVM.

2.1.7.2 COMM LOOPBACK Maintenance Bit - The COMM LOOPBACK bit is a maintenance bit that is cleared on power-up. This bit sets up loopback for the three serial ports to allow testing. The port loopbacks are done in such a way that bit rate errors of one port can be detected by another.

The following table shows how the signals are routed.

PORT LOOPBACK = 0	PORT LOOPBACK = 1	
SIGNAL SOURCE FROM	SIGNAL SOURCE FROM	SIGNAL INPUT TO
COMM RCV DATA	COMM TXD	COMM RXD
PRT RCV DATA	KBD TXD	PRT RDATA
KBD RCV DATA	PRT TXD	KBD RXD

2.1.7.3 DIAGNOSTIC LOOPBACK Maintenance Bit - The DIAGNOSTIC LOOPBACK bit is a maintenance bit that is cleared on power-up. This bit, when set to 1, allows the floppy data separator and the serial video output to be tested through the use of the printer port. The following table shows how the signals are routed.

DIAGNOSTIC LOOPBACK = 0	DIAGNOSTIC LOOPBACK = 1	
SIGNAL SOURCE FROM	SIGNAL SOURCE FROM	SIGNAL INPUT TO
PRT RDATA (J2)	VIDEO OUT	PRT RXD (7201)
PRT RXTXC	500 KHZ	PRT RXTXC (7201)
MASTER CLK	250 KHZ	VIDEO CLK (DC011)
FLOPPY RAW DATA	PRT TXD (7201)	FLOPPY DATA SEPARATOR

During Diagnostic Loopback, the -TEST input of the 8088 is connected to the interrupt output of the MPSC. Thus, using the 8088's WAIT instruction in a polled I/O loop, the diagnostic firmware will be able to keep up with the 500 Kb data rate on the MPSC.

2.1.7.4 Diagnostic Read Register: 8088 - This register (Port address 0A Hex) is used to read a select number of signals for diagnostics.

1. Bit 0 - This bit represents the state of bit 0 of the Diagnostic Write Register (Z RESETL).
2. Bits 1-3 - Manufacturing test straps.
3. Bit 4 - Represents the state of bit 4 of the Diagnostic Write Register. (Diagnostic loopback H)
4. Bit 5 - This bit represents the state of bit 5 of the Diagnostic Write Register (port loopback H).
5. Bit 6 - This bit represents the state of the bit 6 of the Diagnostic Write Register (PROGRAM NVM).
6. Bit 7 - This bit represents the state of the bit 7 of the Diagnostic Write Register (RECALL NVM).

2.1.7.5 **General/Diagnostic Control/Status Register: Z80A** - This 8-bit register/buffer holds a variety of information bits for the Z80A.

2.1.7.5.1 **General/Diagnostic Control - Z80A Port Address 21 (and 20)Hex -**

1. ZFLIP L - When this signal is low, address line 15 of the Z80A is inverted. In this case, the 2K unshared RAM appears at address 8000 rather than at 0. The signal is low whenever the Z80A is reset. It can be set high by writing to the general/diagnostic control register at 21 hex. It can be reset by writing to address 20 hex.

2. Bits 0 - 3 - These bits are connected to the digital to analog converter. (Future option).

3. Bits 4 - 6 - These bits are connected to the LEDs.

2.1.7.5.2 **General/Diagnostic Status Register - Z80A Port Address 21 Hex -**

1. Bit 0 - ZFLIP L - This bit is the read back for ZFLIP L in the General Diagnostic Control Register.

2. Bit 1 - INTZ80L - This bit reads the INTZ80 bit that is sent by the 8088 to interrupt the Z80A.

3. Bit 2 - INT88L - This bit reads the INT88 bit that is sent by the Z80A to interrupt the 8088.

4. Bit 3 - Status of the READY L coming from the floppy.

5. Bit 4 - This bit reflects the status of the DIRECTION signal from the 1793 going to the floppy. Used to control step direction.

6. Bit 5 - This bit reflects the status of the TRACK 0 signal coming from the floppy. Indicates the head is on the track 0 position.

7. Bit 6 - This bit reflects the status of the WRITE GATE signal from the 1793. Used to gate write pulses to the floppy drive.

8. Bit 7 - This bit reflects the status of the STEP signal from the 1793 which is used to step the floppy read/write head in or out on the drive.

2.1.7.6 **Printer Port Interface** - This is a general purpose printer port which provides an RS423 interface compatible with DEC printers. EIA signals supported are:

- Transmit Data
- Receive Data
- Data Terminal Ready
- Clear to Send always asserted
- Data Set Ready always asserted

Software programmable bit rates supported are:

- 75
- 150
- 300
- 600
- 1200
- 2400
- 4800
- 9600

Software-programmable character formats supported are 5-8 bits/character with 1, 1-1/2, or 2 stop bits/character. Parity may be selected as odd, even or none. Software should support XON/XOFF restraint protocol for this port. The D-type 25-pin female EIA printer connector physically resides on the mother board in the normal printer port location and attaches directly to a printer. No null modem is necessary. DSR and CTS are always asserted.

Printer Port Interface Connector

Pin No.	Signal Description	Mnemonic	Direction
1	Protective Ground	PROT GND	------
2	Transmit Data	TXD	Input
3	Receive Data	RXD	Output
5	Clear to Send	CTS	Output *
6	Data Set Ready	DSR	Output *
7	Signal Ground	GND	------
20	Data Terminal Ready	DTR	Input

Note

*This output is always asserted high.

2.1.7.6.1 Printer Bit Rate/Communication Clock Source Register - Bits 0,1, and 2 of this write-only register specify the printer bit rate (16X clock) according to the following table:

Bit Rate Of 16X Clock	D2	D1	D0
75	0	0	0
150	0	0	1
300	0	1	0
600	0	1	1
1200	1	0	0
2400	1	0	1
4800	1	1	0
9600	1	1	1

Bit D3 specifies the communication clock source as follows:

Source	D3
Internal	0
External	1

2.1.7.7 **Communications Port** - This port is used to communicate to another computer. It has full modem support and supports the same signals as the VT102. U.S. and European full- and half-duplex modems can be supported by this port. The port has ASYNC as well as BISYNC modes with a RS423 (V.24/V.28) physical interface conforming to CCITT V.21, V.22 and V.23. Break detection by this port is supported.

The bit rates are set by writing a byte to port 6. The low nibble of the byte (D0 - D3) controls receive bit rate and the high nibble (D4 - D7) controls the transmit bit rate according to the following table:

Nibble Value	Bit Rate	Nibble Value	Bit Rate
0	50	8	1200
1	75	9	1800
2	110	A	2000
3	134.5	B	2400
4	150	C	3600
5	200	D	4800
6	300	E	9600
7	600	F	19200

All bit rates are software selectable. Transmit and receive bit rates may be selected independently from the available bit rates. Signals supported are:

1. Receive Data
2. Transmit Data
3. Secondary Transmit Data
4. Request to Send
5. Secondary Request to Send
6. Clear to Send
7. Secondary Clear to Send
8. Receive Line Signal Detect
9. Secondary Receive Line Signal Detect/Speed Indicator (Bell 212A)
10. Ring Indicator
11. Data Set Ready
12. Speed Select

2.1.7.7.1 **Communications Status Register: 8088** - The following read-only register (Port Address 02 hex) holds the status of the modem control lines on the COMM's port and two interrupt lines, one from each CPU.

1. Bit 0 - This bit reflects the status of the Ring Indicator line of the communications port.

2. Bit 1 - This bit reflects the status of the Speed Indicator line or the Secondary Receive Line Signal Detect of the communications port.

3. Bit 2 - This bit reflects the status of the Data Set Ready line of the communications port.

4. Bit 3 - This bit reflects the status of the Clear To Send line of the communications port.

5. Bit 4 - This bit reflects the status of the Receive Line Signal Detect of the communications port.

6. Bit 5 - This bit reflects the status of MHFU Enable L.

7. Bit 6 - This bit reflects the status of the INT 88 L bit which is generated by the Z80A to interrupt the 8088 CPU.

8. Bit 7 - This bit reflects the status of the INT Z80A L bit which is generated from the 8088 to interrupt the Z80A CPU.

2.1.7.7.2 **Communications Control Register: 8088** - The following write-only register (Port Address 02 hex) controls the modem lines on the COMM port as well as four LEDs.

1. Bit 0 - This bit controls the Speed Select line of the communications port.

2. Bit 1 - This bit controls the Secondary Request To Send line of the communications port.

3. Bit 2 - This bit controls the Data Terminal Ready line of the communications port.

4. Bit 3 - This bit controls the Request To Send line of the communications port.

5. Bit 4 - When written with a 0, lights a LED.

6. Bit 5 - When written with a 0, lights a LED.

7. Bit 6 - When written with a 0, lights a LED.

8. Bit 7 - When written with a 0, lights a LED.

2.1.8 Massive Hardware Foul-up Detection

There is a watchdog timer on the mother board which is intended to detect situations in which the 8088 has lost most of its sanity. If the 8088 does not acknowledge the vertical frequency interrupt within approximately 108 milliseconds, a reset signal is applied to the 8088 for 108 milliseconds. This causes the 8088 to begin executing code at FFFF:0.

MHFU detection is disabled by writing to the DC012 at port address 10C hex. It is enabled by writing the DC012 at port address 0C hex. The enable/disable status may be read from bit 5 of the communications status register (port address 02). When the firmware begins executing at location FFFF:0, it should assume a power up reset if MHFU is disabled, and a MHFU reset if MHFU is enabled.

2.2 Z80A SYSTEM

The following describes the section of the system controlled by the Z80A.

2.2.1 Z80A CPU

The module includes one Z80A microprocessor, which runs from a clock of 4.012 MHz. The Z80A alone has access to the floppy disk interface and thus is responsible for controlling the floppy (via programmed I/O) for all applications.

2.2.2 Z80A Shared Memory

The Z80A has available to it 64 KB RAM which is divided into 62 KB shared and 2KB unshared memory. Accesses to the shared portion of memory select the corresponding address in the standard bank of 64K DRAMS. Accesses to the unshared memory select a private 2Kx8 byte-wide static RAM.

2.2.3 Z80A Private RAM

The unshared RAM may be accessed by the Z80A at any time without any wait states. If the shared RAM is "busy" at the time of a Z80A access, the Z80A will execute wait states until the RAM is free. The RAM is considered "busy" when an 8088 cycle or a refresh cycle is in progress or is pending. In addition to wait cycles due to contention, all M1 cycles from the shared RAM have one extra wait cycle due to the timing for this sort of machine cycle. In any case, the Z80A is held in a wait state for no longer than 2.5 microseconds, unless the bundle board causes contention. If both processors are executing out of the shared memory, the Z80A cannot reliably access the floppy disk (i.e., lost data errors will often result).

2.2.4 Z80A I/O Map

Port	Function	
00H	Clear Interrupt to Z80A (Read)	
00H	Interrupts 8088 (Write)	
21H	Disk Diagnostic Read Register	RO
21H	Disk Diagnostic Write Register	WO
40H	Disk Control Read Register	RO
40H	Disk Control Write Register	WO
60H	FDC Status Register	RO
60H	FDC Control Register	WO
61H	FDC Track Register	R/W
62H	FDC Sector Register	R/W
63H	FDC Data Register	R/W

Note

The above Z80A I/O ports are re-mapped within their own pages and are also re-mapped starting at 80H. Writing Diagnostic Write Register at address 21H will reset ZFLIP. Writing the Diagnostic Write Register at address 20H will set ZFLIP.

2.2.5 Z80A Memory Map

Figure 3 shows the Z80A memory map:

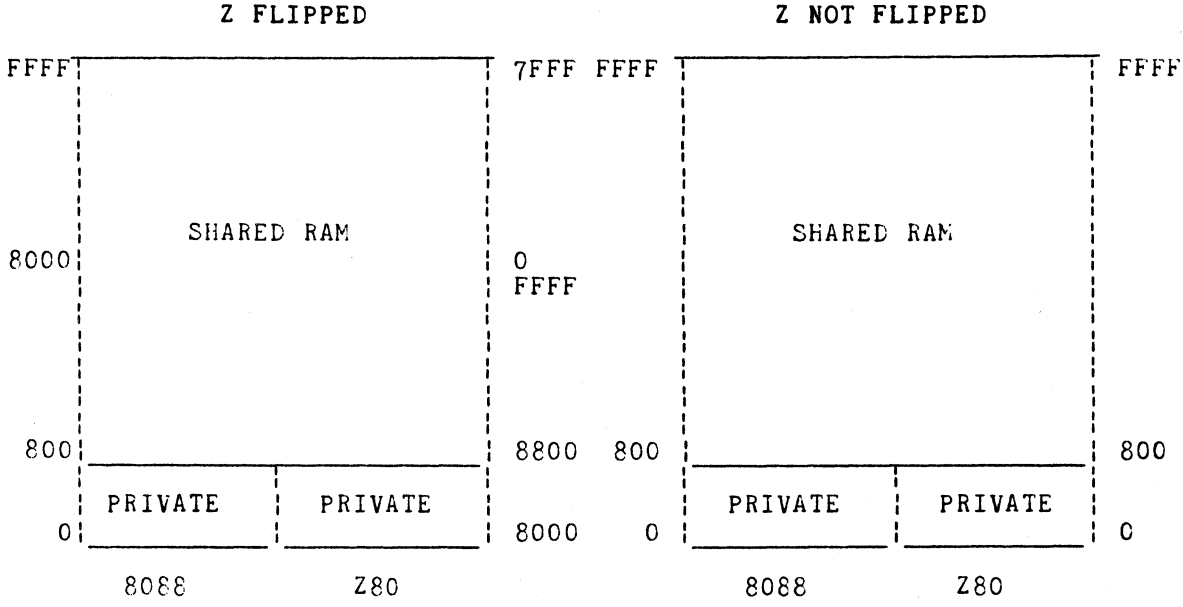


Figure 3. Z80A Memory Map

2.2.6 Z80A Cycle Time

The clock time on the Z80A is 249.2375 nS. Unshared memory accesses have no wait states. Shared memory accesses have wait states on M1 cycles and for cycles in which there is contention between devices accessing the shared RAM. Contention exists because of refresh cycles and 8088 cycles.

2.2.7 Z80A Interrupts

The only interrupts are interprocessor interrupts from the 8088 CPU. The vector placed on the bus is F7 (hex) which causes a RST 30 instruction to be executed in interrupt mode 0.

2.2.8 Floppy Controller Module

The floppy controller module is not optional. It is a separate module that connects to the mother board via J7.

The interface is designed to control up to four 5-1/4 inch platters with one or two surfaces. The controller supports soft-sectored double-density diskettes using a PLL circuit. Single- or double-sided drives are supported. The interface adheres to drive capability and signal definition of the ANSI standard interface for mini-floppy drives.

The floppy controller block diagram is shown in Figure 4.

2.3 Z80A/8088 INTERRUPT FLAGS

Each CPU has a D-type flop that is used to interrupt the other CPU.

1. INT Z80A flag is set when the 8088 writes to I/O port 0. The flag can be cleared by the Z80A only via a read of I/O port 0. The data is irrelevant. The firmware should clear this flag on power-up.

2. INT 88 flag is set when the Z80A writes to I/O port 0. The flag can be cleared by the 8088 only via a read of I/O port 0. The data in either case is irrelevant. The firmware should clear this flag on power-up.

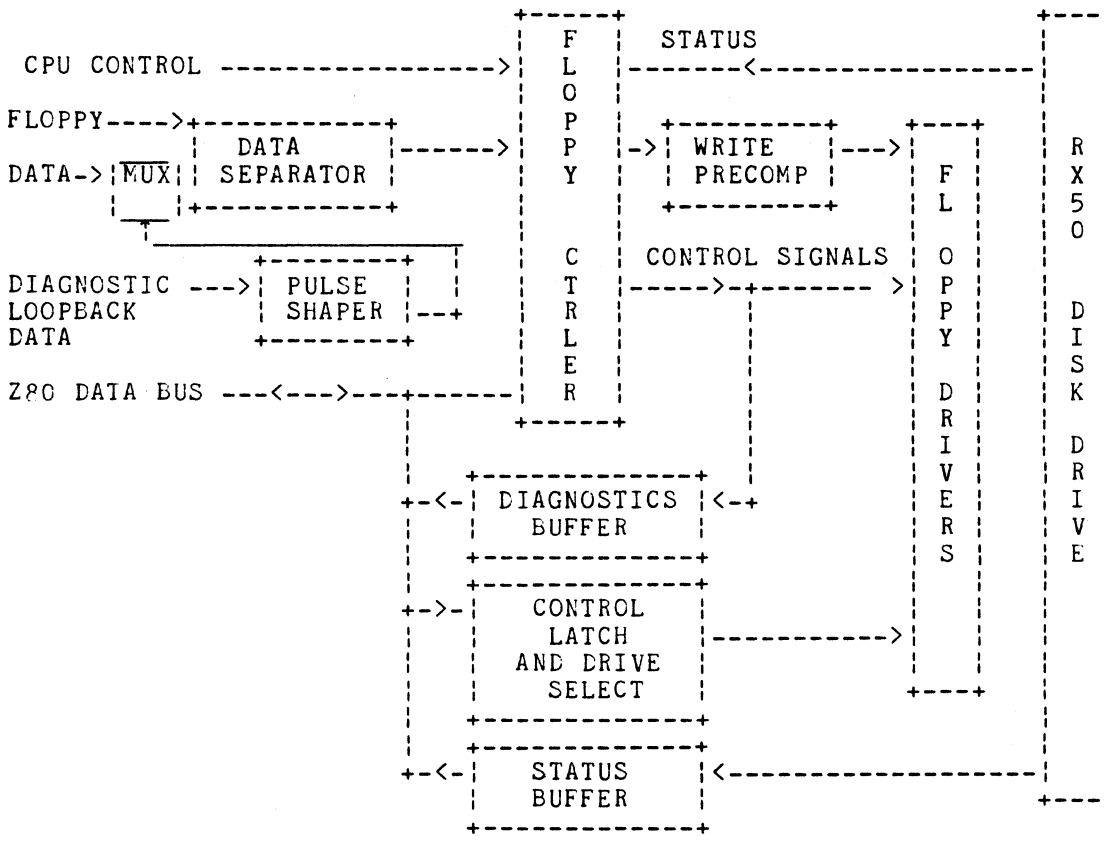


Figure 4. Floppy Controller Block Diagram

3.0 CONNECTOR PINOUTS AND DESCRIPTIONS

3.1 POWER INTERFACE CONNECTOR

The power connector on the mother board is a 13-pin in-line connector with the following pinout:

1 ACOK — This signal indicates the presence or absence of valid ac power entering the power supply. When valid ac power is present, this signal will be high (open circuit) and when the ac power is lower than the required minimum input voltage, this signal will be low (short circuit to logic ground).

2 UNUSED

3 Key — This pin must be missing from the mother board.

4 — -12V OUT

5,6 — +12.1V OUT

7,8,9 — +5.1V OUT

10,11, 12,13 — DC Power Return Signal Ground

3.2 VIDEO INTERFACE CONNECTOR

This connector is a 15-pin D-type female connector supplying interface signals and power to the PC100 monitor and keyboard with the following pinout:

Pin	Name	Description
1	Blue Shield	Ground connector for blue gun shield
2	Green Shield	Ground connector for green gun shield
3	Red Shield	Ground connector for red gun shield
4	Mono Shield	Ground connector for B/W video gun shield
5,6	GND	+12V returns
7,8	+12V	+12V DC to monitor and keyboard
9	Blue	Composite blue gun output
10	Green output	Composite green gun output; also monochrome text
11	Red	Composite red gun output
12	Mono video	Composite B/W video output
13,14	KBD TX data	RS423 serial data to keyboard
15	KBD RCV data	RS423 serial data from keyboard

3.3 EXTENDED COMMUNICATIONS OPTION CONNECTOR

The extended communications option uses two 40-pin connectors. Refer to Table 1 for pin numbers and signals:

Table 1. Extended Communications Option Connectors

J4		J5	
Pin No.	**Signal**	**Pin No.**	**Signal**
1	INIT L	1	BAD0
2	-12 V	2	SHD0
3	EXCOMMS PRES L	3	BAD1
4	+12 V	4	SHD1
5	DMAC INTR L	5	BAD2
6	GND	6	SHD2
7	EXCOMMS SEL 1L	7	BAD3
8	+12 V	8	SHD3
9	EXCOMMS REQ L	9	BAD4
10	Not used	10	SHD4
11	Not used	11	BAD5
12	+5 V	12	SHD5
13	Not used	13	BAD6
14	+5 V	14	SHD6
15	Not used	15	BAD7
16	+5 V	16	SHD7
17	Not used	17	A0
18	GND	18	SHMA0
19	Not used	19	A1
20	GND	20	SHMA1
21	Not used	21	A2
22	GND	22	SHMA2
23	EXCOMMS INTRL L	23	A3
24	GND	24	SHMA3
25	EXCOMMS ACK L	25	EXCOMMS SEL 2L
26	GND	26	SHMA4
27	2.5 MHZ	27	+5 V
28	GND	28	SHMA5
29	05A H	29	+5 V
30	Not used	30	SHMA6
31	05C L	31	+5 V
32	Not used	32	SHMA7
33	BWR 88 H	33	GND
34	Not used	34	SHRAM RAS L
35	BRD 88 H	35	GND
36	Not used	36	SHRAM CAS L
37	05C H	37	GND
38	Not used	38	EXCOMMS SH WR L
39	Not used	39	Not used
40	e H	40	Not used

3.4 MEMORY OPTION CONNECTOR

The memory option connects to the mother board via a 52-pin connector (J6). Table 2 lists the pin numbers, signals and dc loading.

Table 2. Memory Option Connector

J6 Pin No.	Signal	DC Signal Load (mA/uA)
1	GND	
2	GND	
3	GND	
4	RAS88H	-12/300
5	RESERVED	
6	A6	-2/40
7	A15	-2/40
8	A1	-2/40
9	A13	-2/40
10	A8	-2/40
11	A3	-2/40
12	A10	-2/40
13	A0	-2/40
14	A14	-2/40
15	A7	-2/40
16	A2	-2/40
17	A5	-2/40
18	A9	-2/40
19	A12	-2/40
20	MUX88H	-8/200
21	A11	-2/40
22	A4	-2/40
23	RFSH RAS H	-6/150
24	PARITY TEST H	-.4/20
25	+5 V	
26	PARITY ERROR L	+8/-400
27	+5 V	
28	+5 V	
29	MEMORY PRESENT L	(GROUND)
30	ADDRESS EN L	-2/50
31	DO RFSH L	-.4/40
32	S64K2 L	-2/50
33	RFSH DONE H	-1.6/40
34	INIT L	-2/50
35	+5 V	
36	BAD7	*
37	CAS88H	-10/2 50
38	BAD6	*
39	R/-DT	-.6/40
40	BAD5	*
41	BRD88H	-4.4/120
42	BAD4	*

Table 2. Memory Option Connector (Continued)

J6 Pin No.	Signal	DC Signal Load (mA/uA)
43	S64K3 L	-2/50
44	BAD3	*
45	BWR88 H	-10/250
46	BAD2	*
47	S64K1 L	-2/50
48	BAD1	*
49	GND	
50	BAD0	*
51	GND	
52	GND	

Note

*OFF STATE = -200 uA/+10 uA; ON STATE = +24 mA/-15 mA

3.5 COMMUNICATIONS INTERFACE CONNECTOR

Pin Number	Signal Description	Mnemonic
1	Protective Ground	PROT GND
2	Transmit Data	XMIT DATA
3	Receive Data	REC DATA
4	Request To Send	RTS
5	Clear To Send	CTS
6	Data Set Ready	DSR
7	Signal Ground	GND
8	Receive Line Signal Det.	RLSD
9	Not Used	N/U
10	Not Used	N/U
11	Not Used	N/U
12	Speed Indicator/Secondary Receive Line Signal Det.	SI/SRLSD
13	Secondary Clear To Send	SCTS
14	Secondary Transmit Data	SXMIT DATA
15	Send Clock	SEND CLK
16	Not Used	N/U
17	Receive Clock	REC CLK
18	Not Used	N/U
19	Secondary Request To Send	SRTS
20	Data Terminal Ready	DTR
21	Not Used	N/U
22	Ring Indicator	RI
23	Speed Select	SPDSEL
24	Not Used	N/U
25	Not Used	N/U

4.0 POWER REQUIREMENTS

1. +5 Vdc +/- 5% @ 4.0 A max.
2. +12 Vdc +/- 10% @.3 A max.
3. -12 Vdc +/- 10% @ .3 A max.

5.0 PHYSICAL DIMENSIONS - MODULE

The mother board is a modified hex module with the following nine connectors:

J1	Communications Connector 25-pin	D-male
J2	Printer Connector 25-pin	D-female
J3	Video/Keyboard Connector 15-pin	D
J4	Extended Comms Connector 40-pin	
J5	Extended Comms Connector 40-pin	
J6	Memory Option Connector 52-pin	
J7	Graphics Option Connector 40-pin	
J8	Power Connector 13-pin	
J9	Floppy Controller Pin 40-pin	

The dimensions are: 10.4 inch high; 14.0 inch long; 1.0 inch high

6.0 RELIABILITY GOALS

The module will meet a 12,000 hour MTBF.

7.0 SYSTEM MODULE ENVIRONMENTAL SPECIFICATIONS

8.0 APPLICABLE STANDARDS

DEC STD 102	Environmental Standard, Class B
UL 478	Electronic Data Processing Units and Systems
CSA C22.2, No. 54	Canadian Electronic Code, Part II, Safety Standards for Electrical Equipment
IEC 485	Safety of Data Processing Equipment
EIA RS170	Electrical Performance Standards - Monochrome Television Studio Facilities

CCITT Recommendation V.24	List of Definitions for Interchange Circuit Between Data Terminal Equipment and Data Circuit Terminating Equipment
CCITT Recommendation V.28	Electrical Characteristic for Unbalanced Double-Current Interchange Circuits
DEC STD 119	Product Safety Standard

9.0 DOCUMENTS SOURCE

1. Zilog's Z80A CPU Specifications
2. Zilog's Z80A Technical Manual
3. Zilog's Z80A Programming Manual
4. Zilog's Z80A CPU Programmer's Reference Guide
5. Intel's 8251A Programmable USART Specifications
6. Intel's iAPX 86, 88 User's Manual
7. Intel's iAPX 88 Book
8. DEC VT100 Technical Manual (information) (DC011 and DC012 Technical Description)
9. Intel's Peripheral Design Handbook (8251 and 8274 programming information)

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