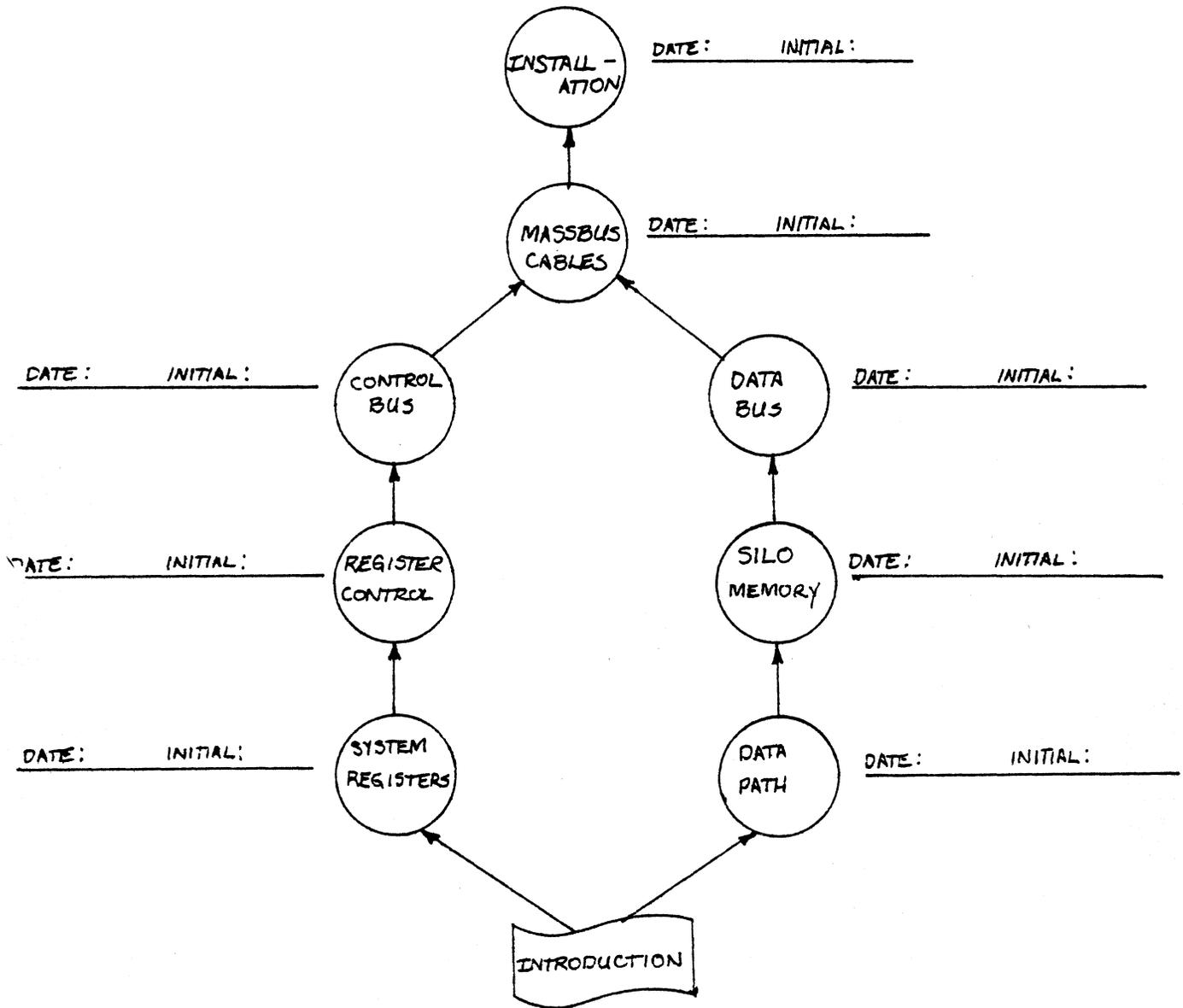


RH-11 PERIPHERAL CONTROLLER
COURSE CONTROL DOCUMENTS

COURSE MAP & PROGRESS PLOTTER



This course of instruction is based on a method called Criterion Referenced Instruction. It is a "do-it-at-your-own-rate" type of course, but more than that it is the result of a study of needs. The needs as expressed by your job. The amount of information to be presented will be no more, or no less, than what is required for you to do your job. Therefore, you can be assured that all the absolutely necessary ingredients that you should obtain in the course will be presented to you. From a job analysis came the course objectives which you will find at the beginning of each unit. These objectives not only told us how to draft up the course, but tell you what is expected of you. Testing of each unit is done under the criterion idea, which simply means you are checked only on what the objectives asked for no more, no less. No more off-the-wall garbage questions or "who cares" question. The questions are not geared to fail you but to check your new-found knowledge of the things the unit objectives want. And remember, you know what they are before you take the unit.

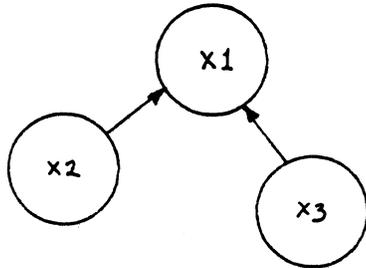
To better orient you new-comers to this type of course, I will explain the items you will find in the course.

I. Course Map

This is found on the first page of this document and show how the different units, or modules, relate of one another. Some of the rules regarding usage of these modules would be:

- A. Before beginning to study a module complete all prerequisites for that module.

Example:



You can't study X1 until units X2 and X3 have been completed and checked off by your course administrator. However, X2 or X3 could be started with because neither of them has prerequisites of their own.

- B. The location of the module on the map is a suggestion as to the approximate point in the course where it would be most meaningful. Where there is no sequence shown, (no arrows leading into a module) you are free to study the modules in any order you desire.
- C. As you complete each unit shade the module in on the map to make it an easy reference as to where you are in the course.

II. Modules

- A. Each module reflects an area on the course map.
- B. Read over all introductory comments before doing any activities in the module.
- C. Study only one module at a time.

- D. Be sure to read the objective and sample test item so that you know what you are looking for in the unit.
- E. If you feel you can complete the objective by answering the criterion test items without doing the activities assigned in the unit, by all means, ask the course administrator for the test.
- F. If you are not sure of your competence in that area, read over the module and its reading resource.
- G. Work through the module at your own rate of speed.
- H. Do not forget with this type of classroom environment, you may confer with your colleagues. You will not be chastised by the instructor for talking in class. It is recommended. Therefore, two rooms are assigned to accommodate those who desire quiet and those who desire to confer.

III. Resources

- A. Resources, or other reference material will be listed within the module. Do not forget that the course administrator is also a "resource of information" and so may be your peers. The module itself is a resource, and any other appropriate manuals that you may have.
- B. Do not feel compelled to consult all of the above as it will tend to tire as well as bore you. Consult only what you need to succeed in each module. If you still do not understand the material, the course administrator will have time to work with you one-on-one.

IV. Tests

- A. Take them when you feel you are ready.
- B. If you feel able to take a criterion test without studying the modules, than ask for the test. You may be asked to offer some evidence of competence before being given the test.
- C. If you happen to not perform accurately on any of the tests, you may, after further study, and at the course administrator's discretion, be asked to complete the same, or a similar test.
- D. After completion of a test, give it to the course administrator, and if the administrator feels you have performed at a satisfactory level, you may look over the self-evaluation sheet to compare your answers with our answers. Any discrepancies can then be worked out between you and the administrator at this time.

V. Personal Progress Summary

- A. This is a sheet found on the course map, (1st page), which the course administrator will initial and date at the successful completion of each module for your personal records.

VI. Master Progress Plotter

- A. This is a sheet the course administrator has which will tell him at a glance just what kind of pace everyone is taking as they work on completing the course. The plotter is updated as the administrator signs off the personal progress summary.

Last Words

If you begin to feel on occasion that there is too much reading, you are probably doing one or more of the following:

- A. Spending too much time on one problem before asking for help.
- B. Working through all available resources listed in a module instead of only those needed to develop the skill as outlined in the objective.
- C. Using only the printed materials as the primary resource instead of using colleagues and course administrator.
- D. Dragging yourself through resource material that is uninteresting or difficult. It could be that you have an alternative source.

This course is designed for you in mind. We have given you enough alternative so that you may progress at what you want to cover at your own rate. (Up to a point!)

There is a quiet room when you want to study in quiet, and there is a conference room in which you may discuss some things with your colleagues or the course administrator. If you don't feel like studying for the moment, you can take a break to wake yourself up. You don't have to punish yourself by sitting for hours at a time.

Any problems? Ask questions!

Now look over the course map and you will find that after you complete the introduction module, you have a choice to make.

INTRODUCTION

The following module is your starting point in this course of learning. It supplies you with the background information as the "why's" of a massbus, the "hows" of its use, and a scope of its inner workings. After reading over this you will undoubtedly have many questions. These questions should all be answered in the modules that follow this.

Using the course map as a guide, select then the module that interests you first and then continue on with the course.

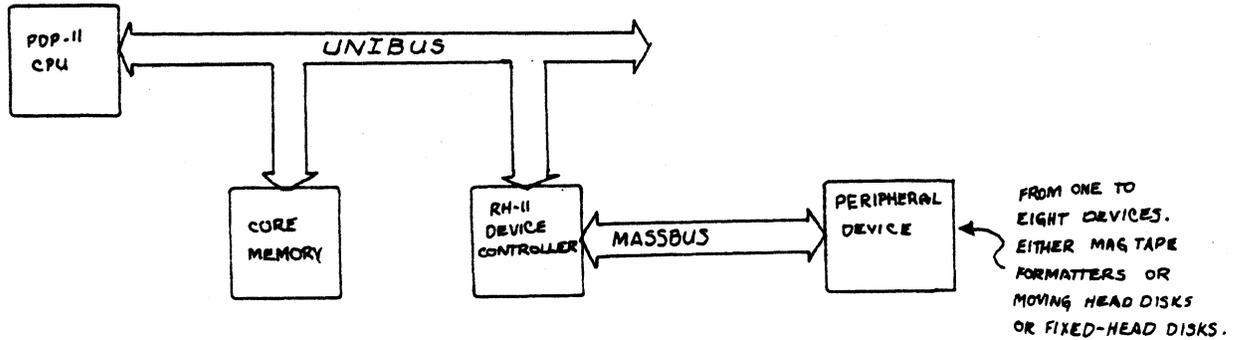
The Massbus is the name for DEC's new peripheral or I/O bus for the newer hi-speed Mass storage devices being designed. Devices such as the RS03/RS04 fixed-head disk, the RP04/05/06 disk drives, the TU16 Mag-tape transports and the RK06 cartridge disk will be the users of this new busing system.

This new busing system offers standard communications to/from the devices and its controllers. All the afore-mentioned devices communicate with a standardized set of signals to a controller known as the RH-11. The RH11, by virtue of its design, is capable of controlling any of the devices with no changes to the logic. This means to you, learning requirements of only one controller instead of 7 separate ones! That in itself is great, but there are more advantages to the system with the name of massbus.

In addition to a standard set of communication lines between the RH-11 and any device, the RH-11 itself can be a dual-bus communicator to the processor. Two separate buses can be

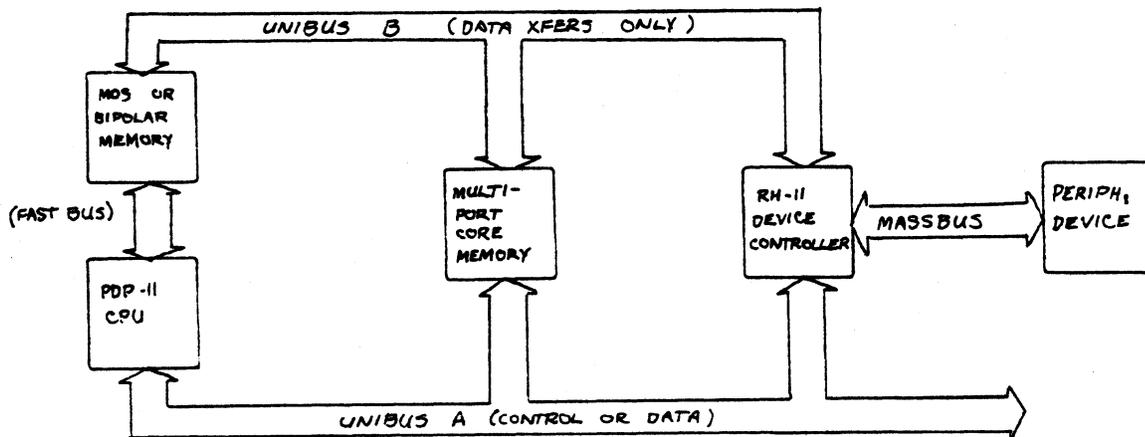
utilized to send or receive data. One to core, and the other perhaps to a MOS, or BI-POLAR memory. Or....perhaps with special systems engineering, two buses to a dual-ported core memory. This type of thinking leads up to all kinds of possibilities that never before could be realized with the present structure of the Unibus.

Let us take a look at a few diagrams to illustrate what I am talking about.



This drawing represents the conventional hook-up to the Unibus system using the RH-11 as a standard peripheral controller like the TC-11 for the DECTape, or the RK-11D for the cartridge disk etc.

The next illustration shows you the dual-Unibus feature that is possible with 11/45 installations:

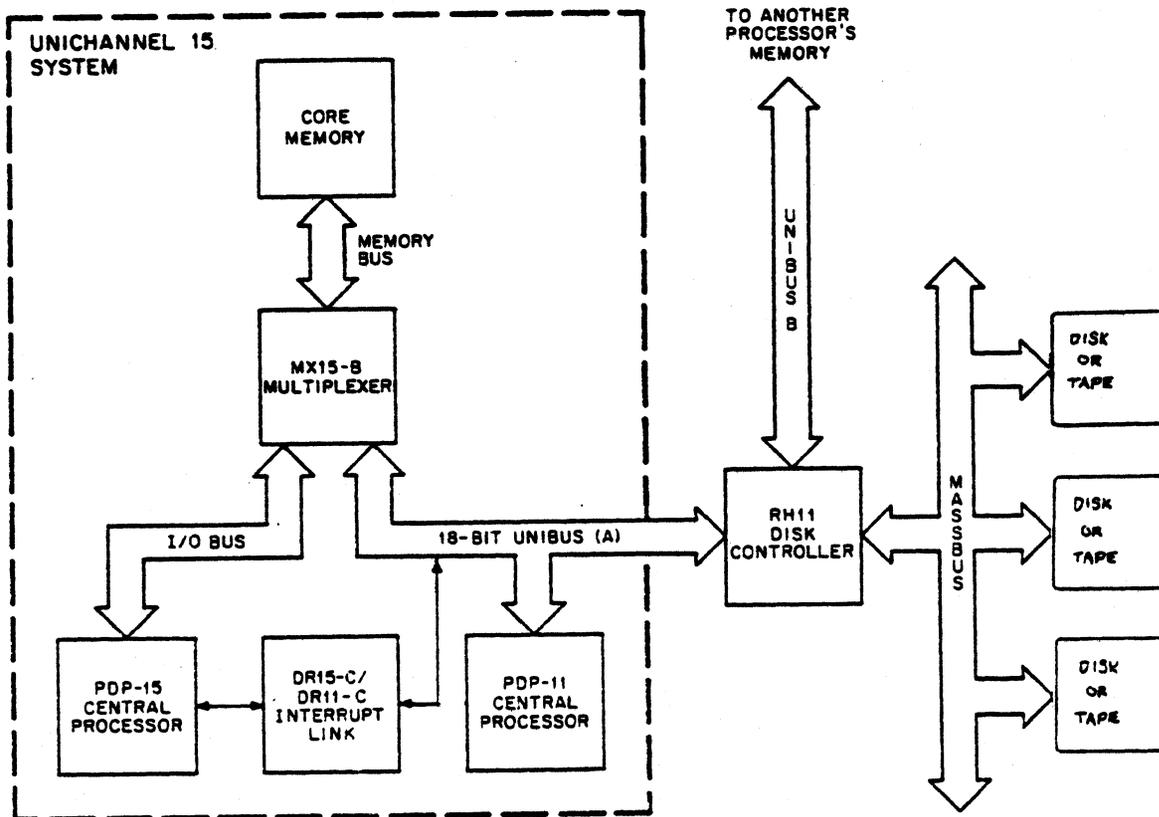


Notice that the two Unibuses are not exactly equal in capabilities. Unibus "A" is capable of issuing commands via accessing registers as well as data N.P.R.'s.

Unibus "B" however, cannot be a controlling bus because it can never access any registers within the RH-11. Bi-polar, or MOS Memory by themselves are not capable of causing any command initiation, so that leaves only data to be transferred over the bus cables after being commanded to do so over Unibus "A". Time is still saved however, because during the time N.P.R.'s are transferring data on "B", communication can take place with other devices on Unibus "A". Such as dectape rolling in a program, or an RK05 can be accessing data.

Shown here is a third alternative in the selection of a use for the massbus system. With two buses from the RH-11 to the processor this could mean that one of the buses could be cables to a Unichannel 15 system which would have a larger PDP-15 as a "master" processor communicating to an 11 processor as a "slave" or, I/O processor. This in turn talks to an RH-11 as well as any other peripheral such as an RK05/RK-11E.

Note that Unibus "B" could be doing data transfers to a completely separate processor's core memory, but keep in mind with this type of system, the processor on Unibus "A" is master. He tells the RH-11 what to do. If that involves transferring data to the second processor on Unibus "B" then the RH-11 does it. The point is that the processor on Unibus "B" can never tell the RH-11 what to do (or where to get off!) (or, go!)



These are but a few of the possibilities that can be thought of utilizing the new Massbus concept. By now you should be aware of the fact that the peripheral devices themselves are completely divorced from the processors. These devices then, with no changes to the logic, can be installed on any product line processor just as long as a Massbus controller is available to communicate with the processor.

As of now, there is an RH-11, and an RH-10, with no plans for an RH-15. (Due to the availability of a system shown in the third diagram). The 11/70 has its own type of RH called appropriately, an RH-70.

Each of these RH's in turn is capable of controlling a variety of peripheral devices with no changes to its logic. The only thing that is not possible with the RH's is to run these different peripheral types on the same massbus controller. Physically possible as far as the RH-11 is concerned, but due to the system software, not feasible.(at least at the present time.)

Let us now take a look inside this RH-11 to see generally what makes it tick. This will be only on a basic, introductory level as there are separate modules to encompass these points in more detail.

First of all these two buses that were mentioned, Unibus "A" and Unibus "B". In an effort to speed up through-put from peripheral to core, the capability exists in the RH-11 to do what is known as "back-to-back N.P.R. memory reference cycles." That mouthful

simply means that with one N.P.R. request and subsequent grant, two words will be transferred in succession using MSYN and SSYN as gating signals. At the completion of the two successive transfers BBUSY lets the other devices know when they can use the UNIBUS. This is possible all because of BBUSY staying "up" at the end of transfer "one" signaling the RH-11 to send the address and "C" line information for the second word transfer. This method is faster for the massbus peripherals because no wait time is encountered for the second word transfer to do its requesting and arbitration, etc.

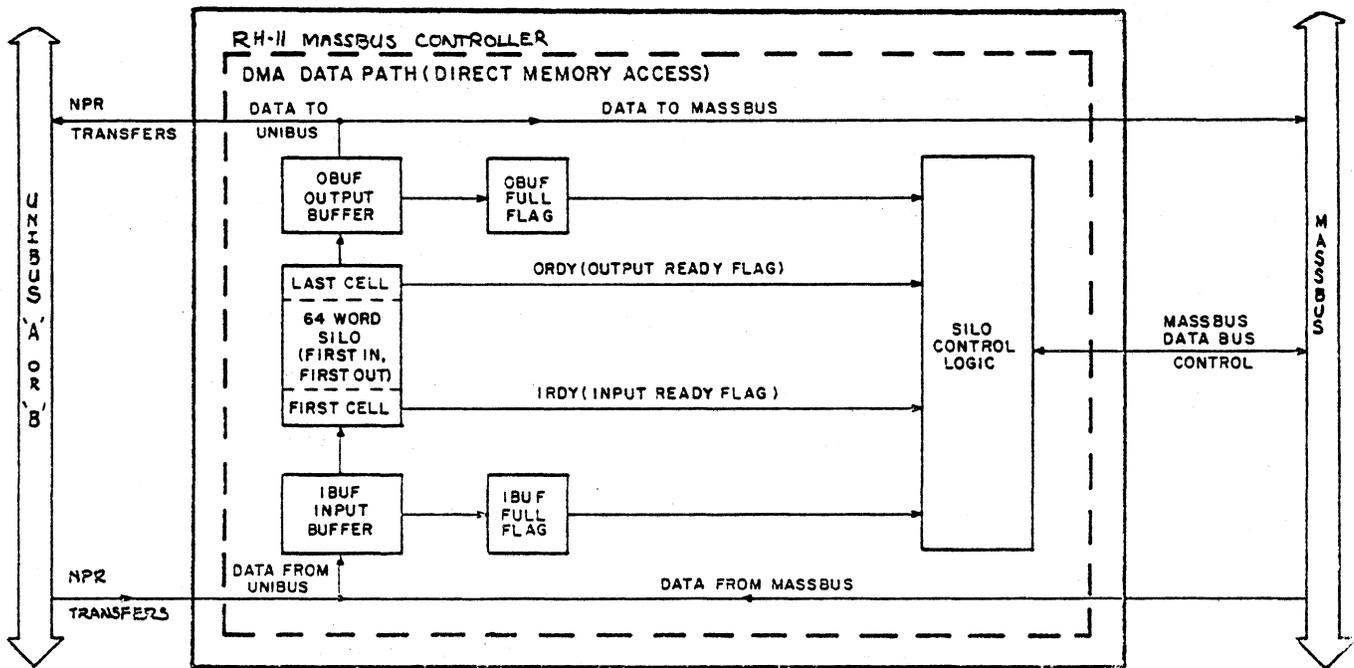
Two was chosen as the maximum number of cycles because of the back-log it would create on the Unibus of other non-Massbus devices attempting to use it. This mode of operation is normal for Unibus "A" only but can be de-selected via jumper on one of the modules.

Unibus "B" handles the data transfers differently. It has what is known as bus "hog" mode. This means that once the N.P.R. request and subsequent grant has been made, BBUSY stays up continuously so that the words may be transferred as fast as the memory can accept them. Considering that could be bi-polar memory with a super-fast cycle time, a 4K word transfer could be done in a short order. This wouldn't make any difference if the peripherals in question were slow, but this mode is especially made for the new hi-speed disks, where the word transfer rates are from 2-4 usec each. This compares with other disks presently being used by DEC which have the range of

7-16 usec per word.

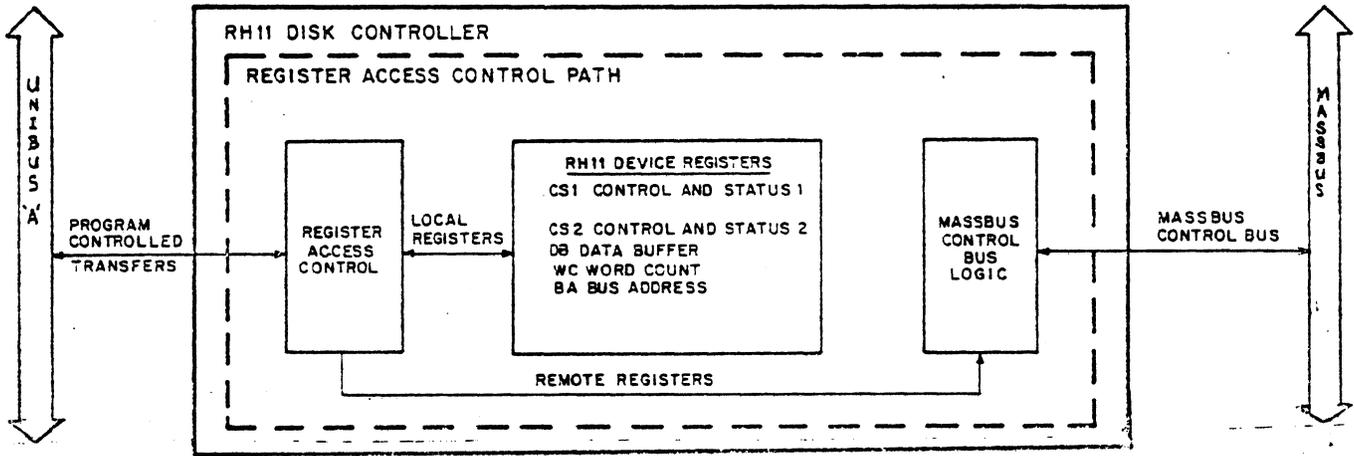
With these speeds in the spotlight, it now becomes obvious that if all the data had to be handled on Unibus "A", and Bus "A" already has a wide assortment of other peripherals on it, the system could become overloaded, tied-up, I/O bound, and whatever other name you can come up with. Since not all systems can utilize a Unibus "B", something else has to be done to the RH-11 to make it operate on a standard Unibus with a fast peripheral. That something else is called a SILO MEMORY.

The silo is a 64 x 18-bit word MOS-type memory that buffers the data and eases the timing differences between the Unibus and Massbus speeds. Between the peripheral device and the RH-11, Data is being transferred at a synchronous rate of between 2-4 usec per word (depending upon the disk being used) and a place is needed to put them while N.P.R.'s (which occur at an asynchronous rate) take them away.



Shown here is a simplified diagram of how the RH-11 transfers words to/from the Unibus. Add to the silo an input register and an output register, and the buffering capability becomes a total of 66 words. Detailed operation of this data path is covered in a later module. For those of you familiar with the RP11-C Disk Controller, the silo memory there is nearly the same as that in this application. And, conversely, when you learn how this works, you will know the concepts behind the RP11-C's usage of the silo.

In order to control this RH-11, it becomes necessary to add registers. (Like the one that is needed that stores the bit that informs the RH-11 to transfer the data on Unibus "B" instead of Unibus "A").



As the drawing above shows, Unibus "A" can transfer register information to/from the RH-11. The registers that are contained within the RH-11 are noted. Depending upon what the peripheral device is there will be eight to fifteen other registers in the sub-system contained with the device logic. Any program controlled transfers to the peripheral register in question must be relayed by the RH-11 to the peripheral device over the Massbus. Detailed information on registers and register selection are handled in separate modules.

The RH-11 is capable of communicating with a wide variety of devices, so a standard set of interfacing signals were assigned names that would cover every facet of communication regardless of the device type. (i.e., RS04, RP04, TU16, RK06?)

A clear understanding of this standard communication set will enable you to interpret the "action" that transpires between any of these devices and the massbus control.

The first thing to do in order to make it easier to explain, is to divide the interfacing into two groups of signals. In the first group is the Control bus which is responsible for transferring information to or from the registers in the peripheral device itself. (See previous page diagram). This bus is discussed in a separate learning activity from the other group called the Data Bus. As its name implies the interfacing signals on this Data Bus communicate the data from memory that is to go on the disk or tape. (Refer back 2 pages to the diagram).

Additional Resources:

RHP04 Maintenance Manual pages 1-1 to 1-8 up to paragraph 1.3.2.4
TJU16 Maintenance Manual pages 1-1 to 1-6 up to paragraph 1.4
RJS04 Maintenance Manual pages 1-1 to 1-6 up to paragraph 1.4

These are some of the points you should have gathered from the reading, answer them by referring back to the module if you cannot answer them from memory.

1. How many buses comprise the cabling system known as Massbus?
2. Write their name(s).
3. Can data be transferred on more than one Unibus?
4. Write a brief description of the function of the SILO.
5. How many different types of peripheral devices can be controlled by RH-11 controllers?
6. How many devices can be run from the RH-11?
7. How many different device types can be controlled by one RH-11 on the same massbus?
8. What is meant by "back-to-back N.P.R. Memory Reference Cycles?"
9. Which Unibus can transfer control (programming) information to the RH-11?

If you cannot answer the questions, or you have questions of your own, ask the course administrator for help.

You have your choice from here as to which module to select. Refer now to the course map and get going!

RH-11
SYSTEM REGISTERS

SYSTEM REGISTERS

OBJECTIVES:

1. Given a list of RH-11 Sub-system registers and a list of register definitions, be able to write the number of the register that corresponds to the definition in the space provided beside the definition with 100% accuracy.
2. Given the terms "LOCAL" and "REMOTE" write a brief (25 words) description of how these words apply to mass bus system registers. Your answer should include the reason why the nomenclature is used.
3. Write a brief summary of the differences between the word count register and drive word count register from memory. Your answer should include why two registers are required for massbus operation.

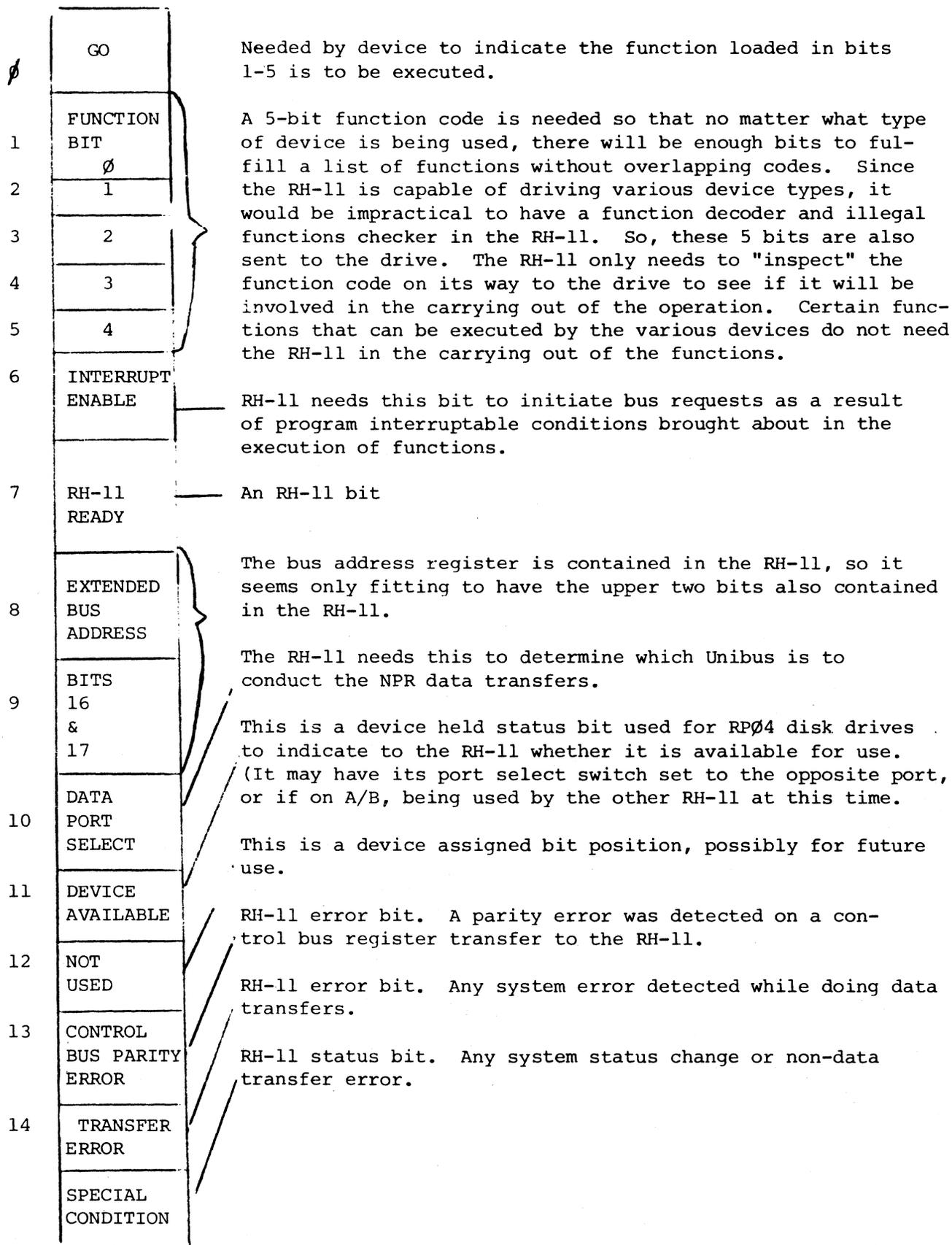
WHAT TO DO:

Read over the following test describing the RH-11 registers keeping in mind what the objectives are looking for. When you are done, glance over the pages in the maintenance manual pointed out in "additional References". When you feel you can complete the objectives ask for the criterion test and then continue on.

SYSTEM REGISTERS

In this module you will be introduced to the massbus system of registers. After all, it is the registers in any peripheral subsystem that enables the subsystem to function relatively independent of the central processor. We cannot discuss them all because most of the sub-system registers are contained within the particular devices themselves stuck at the end of a long cable known as the MASSBUS. These registers then, will be discussed at a time where you will be learning about a particular storage device (i.e. RSØ4, RPØ4, TUL6, RKØ6) these registers do have a generalized name, a label if you will, that I would like you to know about. Any register contained within the logic confines of the mass-storage device is called a REMOTE Register.

To see the reasoning behind this label, simply reference everything in the sub-system from the controller. If all registers outside the controller are called remote, then it stands to reason that the RH-11 registers shall be called LOCAL. This is concept number one to learn of massbus registers. Now for the registers themselves...we find upon an investigation that there are 4½ local registers. What! 4½! What sort of nonsense is this? It seems that the register we have all grown to know and love as a control and status register when we were fooling around with the Unibus, is also around here on a massbus device as well. All of the basic components of a C & S register as we knew them on the Unibus were maintained. Items such as the GO bit, ERR (bit 15) and READY are still needed. The point is, that some of these bits the devices themselves need to operate, while some of the bits the controller needs. I'll demonstrate with an illustration of the register:



Most of the types of information you see above, you have run across before in other control and status registers. With this register, due to the design of the

Massbus system, the register has to be shared between the RH-11 and corresponding remote device. That's how the total number of registers came to be some number plus a $\frac{1}{2}$. Now for the rest of the controller-required registers.

To start with, we will consider another control and status register.

Massbus devices have more control and status type information to be stored, so the need for a second register arises. Call the above a description of control and status #1. Meanwhile, back at control and status #2.....

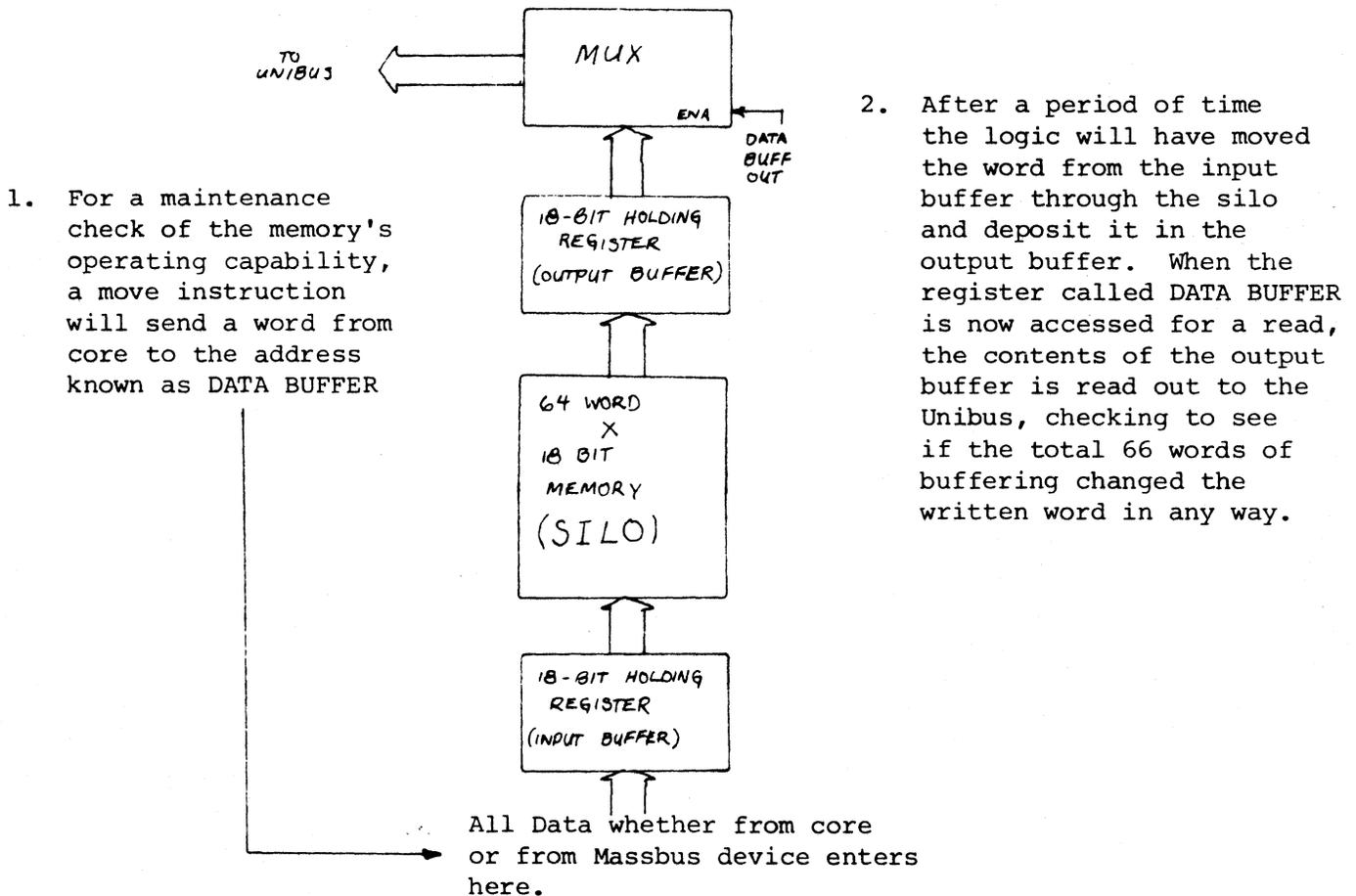
0	UNIT # BIT 0	The unit, or device number of the peripheral that is being, or was last, accessed. The RH-11 has a place for this information because it is possible for the RH-11 to be controlling one unit performing a data transfer, and be accessing a second drive's register. The unit number is always necessary to write into or read out of device register, but is not necessary to perform the data transfer function. So...the information stored in these three bit positions is that of the number of the device that is, or was, being register accessed. It is <u>not</u> necessarily representative of the device currently performing an operation unless you have a one device sub-system.
1	1	
2	2	
3	BUS ADDR INCRE- MENT INHIBIT	
4	PARITY TEST	
5	SYSTEM REGISTER CLEAR	
6	SILO INPUT READY	The rest of the bit positions are not important that you memorize, for you can look up their usage in the maintenance manual, when the occasion arises that you need to.
7	SILO OUTPUT READY	What is important is that you grasp for concept as to the use or uses of the RH-11 registers.
8	DATA BUS PARITY ERR.	For now just note that the rest of the register is made up of RH-11 errors (bits 8-15) and a few status bits for the RH-11 (bits 6-7) and a few commands (bits 3-5).
9	MISSED XFER ERROR	
10	PROGRAM ERROR	
11	NON-EXIST MEMORY	
12	NON-EXIST DISK	
13	UNIBUS PARITY ERROR	
14	WRITE CHECK ERROR	
15	DATA LATE ERROR	

The third register we will ponder is the BUS ADDRESS register. Just about everyone knows that the function of this register is to contain an address of a core location that the NPR transfer is to take place. Also remember that the upper two bit positions for this address is stored in the CS1 register.

To summarize: This register is no different than those you are already familiar with in other more conventional DEC controllers.

The fourth register to ponder is the data buffer. It is listed as a separate register only for the purpose of checking out the silo memory in the RH-11. In other words, a maintenance tool.

In a simplified block diagram we can see its function more clearly:



This is really the only time this register would be accessed directly by the program. During data reads and writes, N.P.R. cycles automatically reference the correct registers without the software being involved. Therefore, to utilize the software address for DATA BUFFER would be of no value except to examine the contents of a previous deposit.

Go back now and glance at the CS2 bit chart. Bit 6 reflects the SILO's ability to accept a word into it, while bit 6 shows you when the SILO has a word ready to be moved out of it.

The last programmable register in the RH-11 is the WORD COUNT register. You have seen registers of this type used before in other DEC controllers where the two's complement of the number of words to be transferred is stored there so that the controller knows when to stop requesting NPR transfers.

There is another register contained within the RH-11 but is not accessible to the programmer. This register's responsibility is to count the number of word transfers that occur on the MASSBUS. Its name will be the DRIVE WORD COUNT REGISTER. It is necessary because of the large data buffering that takes place in the RH-11 by way of the SILO memory. Another factor is the extreme difference between the two data transfer rates. That of the UNIBUS (occurring asynchronously) and that of a peripheral (occurring synchronously).

In order to make the silo effective, it should be filled first from the Unibus before initiating any transfers on the Massbus. This means that a "head start" is given the Unibus, and the word count register has already been incremented by a factor of 66. Keeping that in mind, it should occur to you that as transfers

occur on the Massbus, the word count register will overflow long before it is time to stop transferring data on the massbus. (Because of the words left in the Silo). Hence, a need for a drive word count register to keep the RH-11 "active" even through word count overflow has already occurred when performing a data write operation. The drive word count register count register can do this because it is loaded with the same value as the word count register at the same time the word count is written in. Its count is changed every time a Massbus cycle occurs, and when it overflows the logic knows it is done. Detailed operation is shown to you in the silo module.

The purpose is all you are looking for right now, just keep the concepts in mind.

Additional Resources:

RJSØ4 Maintenance Manual, Pg. 3-5 paragraph 3.6 CS1
3.7 paragraph 3.7 WC
3.8 paragraph 3.8 BA
3.9 paragraph 3.10 CS2
3.17 paragraph 3.15 DB

RJPØ4 Maintenance Manual, Pg. 4.3 paragraph 4.6 CS1
4-6 paragraph 4.7 WC
4-6 paragraph 4.8 BA
4.23 paragraph 4.15 DB
4-8 paragraph 4.10 CS2

TJU16 Maintenance Manual Pg.3-10 paragraph 3.6.1. CS1
3-10 paragraph 3.6.2 WC
3-10 paragraph 3.6.3 BA
3-14 paragraph 3.6.5 CS2

SYSTEMS REGISTERS
CRITERION TEST

In the space following the below definitions, write in the number that corresponds to the correct register name.

I.

- | | | |
|--------------------------|---|-------|
| 1. Control and Status #1 | A. Defines the number of the word transfer that are to take place on the Unibus | _____ |
| 2. Control and Status #2 | | |
| 3. Bus Address Register | | |
| 4. Word Count Register | | |
| 5. Drive Word Count | B. Contains the output of the silo memory when reading | _____ |
| 6. Data Buffer | | |
| | C. A register that contains the device unit number to be operated on. | _____ |
| | | |
| | D. Defines the completion of a Write Operation. | _____ |
| | | |
| | E. Contains information as to where the data transfer is to take place in core. | _____ |
| | | |
| | F. This register is shared by both device and RH-11. | _____ |
| | | |
| | G. This register contains most RH-11 error indications. | _____ |
| | | |
| | H. Where you would go to find the function being performed. | _____ |
| | | |
| | I. Where you would go to find out the status of the silo. | _____ |

SYSTEMS REGISTERS
CRITERION TEST (cont'd)

II. Write a brief description of the terms "LOCAL" and "REMOTE" as to how these words apply to Massbus Register terminology. Include in your answer why the nomenclature is used.

III. Write a brief summary of the differences between the word count register and the drive word count register. Include in your answer the reason why two registers are needed.

RH-11
REGISTER CONTROL

INTRODUCTION

In this lesson you will find out just exactly how the RH-11 handles the UNIBUS address selection inputs when accessing SUB-SYSTEM registers. All control bus signal transmission is also generated in this unit giving you an excellent view of 50% of the RH-11 logic in block diagram form.

OBJECTIVES

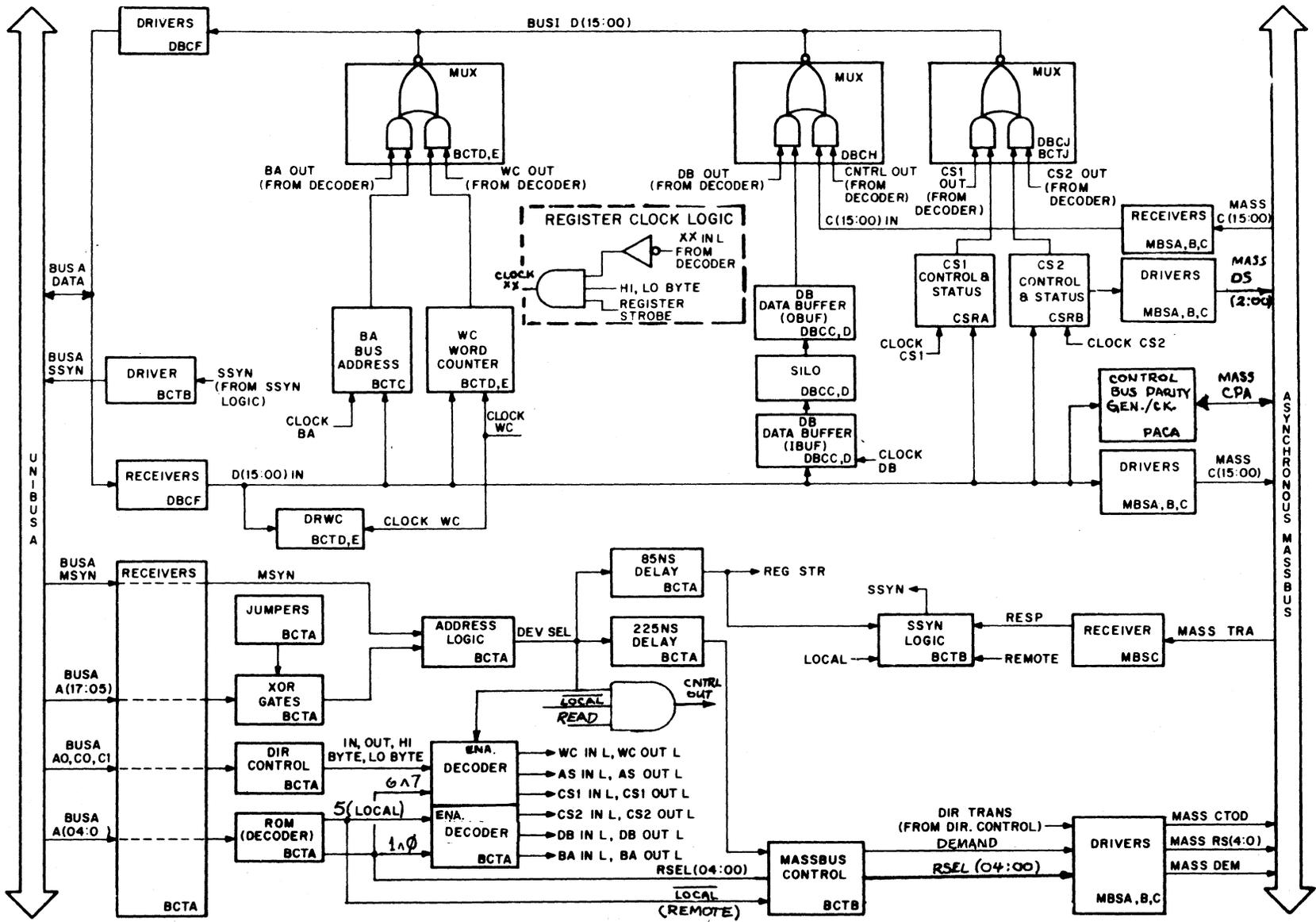
Given the "RH-11 Register Control Path" block diagram, trace through the following functions:

- A. Write to a local register
- B. Write to a remote register
- C. Read from a local register
- D. Read from a remote register

Given the "Massbus Device Register Selection" Diagram, specify the register select code and proper jumper configuration for any RH-11 sub-system register specified.

WHAT TO DO:

Read over all the material in this lesson, be sure you understand what is expected of you in the objectives, read over the additional reading (if desired) or discuss this with a colleague, then take the test and continue!



Register Control Path

REGISTER CONTROL PATH:

If you will observe the block diagram, this is everything you have always wanted to know about how the RH-11 logic accesses registers, but were afraid to ask!

Starting at the left-hand side, UNIBUS "A" serves as the input from the program attempting to communicate with a register. The address of the desired register arrives to the receivers in lower-left, and the most significant bits are tapped off to XOR gates to determine if the activity occurring on the UNIBUS concerns the RH-11. (or one of its associated MASSBUS peripherals). If there is a favorable comparison, the address logic outputs "DEV SElected" and starts a pair of delays to time out and acts as an enable in a couple of places.

Meanwhile, the lower bits of the address are routed to a 32 x 8-bit ROM to act as a register decoder. Considering all future possible designs and devices, it was established that the figure of 32 registers would be sufficient.

The 8-bit output of the ROM, consists of a 5-bit RS (register-select) code for use of the MASSBUS peripherals to decode their registers.

Also, bits 0, 1, 6 & 7 feed a RH-11 decoder in order to decode the local register selection. The left-over (bit 5), determines where that register

is local or remote.

(to see this a little more clearly refer to the "Massbus Device Register Selection" diagram on the next page)

So far we have taken any UNIBUS address (772046 for example) broken down into its binary equivalent; (111 111 010 000 100 110) applied bits five through 17 to some XOR gates, 4 through 1 to the ROM, and received an output of 00101 as a RS code to the MASSBUS, and the ROM told us it was a remote register. (After you ABSORB that, kindly back up to the "Register Control Path" block diagram and continue reading.

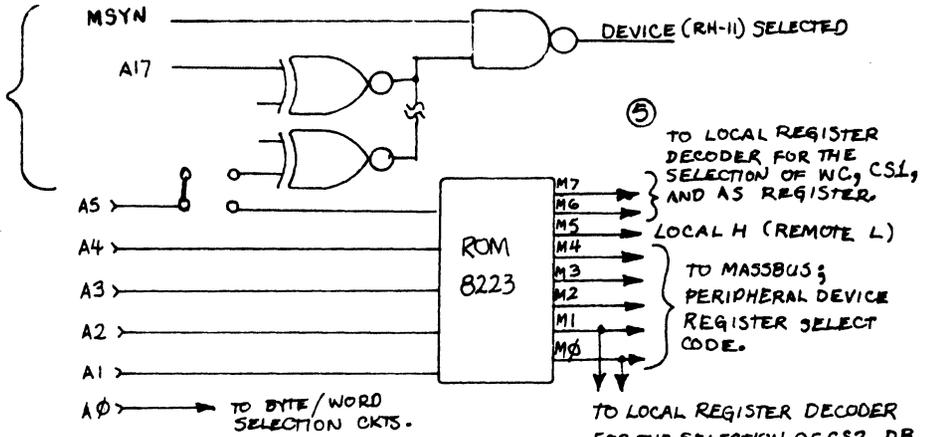
REGISTER WRITES

While all this decoding was going on, the two delays are in the process of timing out. If a local register rite was indicated, the trailing edge of the 85ns delay clocks the appropriate register (see example in dotted area on diagram) and the data sitting on the Unibus data lines is gated into it.

If a remote register write were indicated, the data on the Unibus data lines would be placed on the MASSBUS "c" lines along with a parity bit from the parity generating CKTS. Add to this the device unit number contained in the CS2 reg., and the translation of the Unibus C1 and C0 lines, (called CTOD) to inform the device of the fact that it is supposed to be a register write. Couple all of this with the RS outputs from the ROM, the desired peripheral has everything it needs to load a register except the gating signal.

① XOR GATES ARE USED WITH THE UPPER ADDRESS BITS (AS WITH THE OTHER DEC CONTROLLERS) TO DECODE THE BASE ADDRESS TO FIND OUT IF THIS HARDWARE DEVICE IS BEING REQUESTED BY THE PROGRAM.

② ADDRESS LINE A5 IS JUMPER SELECTABLE TO THESE XOR GATES OR TO THE ROM DEPENDING UPON THE QUANTITY OF REGISTERS IN THE SUB-SYSTEM.



③ THE TU16 AND RS04 DEVICES WILL HAVE JUMPERS TO THE XOR

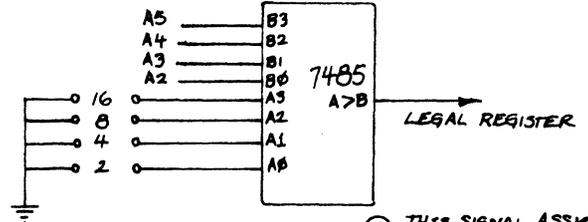
④ THE RP04 WILL BE JUMPERED TO THE ROM. 5 LINES ARE NEEDED TO DECODE THE 20 REGISTERS.

⑥ ADDRESS LINES 2,3,4 AND 5 ARE SIMULTANEOUSLY FED TO A MAGNITUDE COMPARATOR FOR COMPARISON OF A "JUMPERED-IN" MAXIMUM NUMBER OF REGISTERS ON THE SUB-SYSTEM.

RP04 = 20 REG. = 16 # 4 OUT

RS04 = 12 REG. = 8 # 4 OUT

TU16 = 14 REG. = 8, 4, # 2 OUT



⑦ THIS SIGNAL ASSISTS IN THE GENERATION OF "DEMAND" FOR ALL REMOTE REGISTER OPERATIONS.

INPUT TO ROM ADDRESS LINES A5 TO A1

* INDICATES RH-11, OR "LOCAL" REGISTERS. ALL OTHERS ARE REMOTE. THIS IS INDICATED BY THE M5 OUTPUT.

REGISTER SELECT PROM - 23040A1 (8223)									
OCTAL ADDR	LOC/REM			RSEL4		RSEL2		RSEL0	
	M7	M6	M5	M4	M3	M2	M1	M0	M0
00	L	L	L	L	L	L	L	L	L
* 01	H	L	H	L	L	L	L	H	H
* 02	H	H	H	L	L	L	L	L	L
* 03	H	H	L	L	L	H	L	H	H
* 04	H	H	H	L	L	L	L	H	L
05	H	H	L	L	L	L	L	L	H
06	H	H	L	L	L	L	H	L	L
07	L	H	L	L	L	H	L	L	L
10	H	H	L	L	L	H	H	H	H
* 11	H	H	H	L	L	L	L	H	H
12	H	H	L	L	L	L	H	H	H
13	H	H	L	L	L	H	H	L	L
14	H	H	L	L	H	L	L	L	L
15	H	H	L	L	H	L	L	L	H
16	H	H	L	L	H	L	H	L	L
17	H	H	L	L	H	L	H	H	H
20	H	H	L	L	H	H	L	L	L
21	H	H	L	L	H	H	L	L	H
22	H	H	L	L	H	H	H	L	L
23	H	H	L	L	H	H	H	H	H
24	H	H	L	H	L	L	L	L	L
25	H	H	L	H	L	L	L	L	H
26	H	H	L	H	L	L	H	L	L
27	H	H	L	H	L	L	H	H	H
30	H	H	L	H	L	H	L	L	L
31	H	H	L	H	L	H	L	L	L
32	H	H	L	H	L	H	H	L	L
33	H	H	L	H	L	H	H	H	H
34	H	H	L	H	H	L	L	L	L
35	H	H	L	H	H	L	L	L	H
36	H	H	L	H	H	L	H	L	L
37	H	H	L	H	H	L	H	H	H

UNIBUS ADDRESSES

REGISTER MNEMONIC	UNIBUS ADDRESSES		
	FIXED-HEAD DISK	MAG-TAPE	MOVING HEAD DISK
	RS04	TU16	RPC4
CSI	772040	772440	776700
WC	772042	772442	776702
BA	772044	772444	776704
DA V FC	772046	772446	776706
CS2	772050	772450	776710
DS	772052	772452	776712
ER1	772054	772454	776714
AS	772056	772456	776716
LA V CK	772060	772460	776720
DB	772062	772462	776722
MR	772064	772464	776724
DT	772066	772466	776726
SN		772470	776730
OF VTC		772472	776732
DC			776734
CC			776736
ER2			776740
ER3			776742
EC1			776744
EC2			776746
MASSBUS (06)			
MASSBUS (05)			
MASSBUS (01)			
MASSBUS (02)			
MASSBUS (04)			
MASSBUS (07)			
MASSBUS (03)			
MASSBUS (06)			
MASSBUS (10)			
MASSBUS (11)			
MASSBUS (12)			
MASSBUS (13)			
MASSBUS (14)			
MASSBUS (18)			
MASSBUS (16)			
MASSBUS (17)			
MASSBUS (20)			
MASSBUS (21)			
MASSBUS (22)			
MASSBUS (23)			
MASSBUS (24)			
MASSBUS (25)			
MASSBUS (26)			
MASSBUS (27)			
MASSBUS (30)			
MASSBUS (31)			
MASSBUS (32)			
MASSBUS (33)			

UNUSED POSSIBLE FUTURE ADDRESSES.

After the 225NS delay times out, this gating signal is produced and named DEMAND. The selected device receives this, loads the register and replies with TRA, (TRANSFER). Upon receipt of TRA, the RH-11 logic produces the UNIBUS signal SSYN. (Remote register \wedge TRA=SSYN) for the local register write, SSYN was produced as a result of LOCAL \wedge REG.STR.

Register Reads

To accomplish one of these, the same decoding takes place as before except that the C1 and C0 lines dictate a Read Operation so one of the 3 MUX's at the top of the page will be gated to accept the contents from the desired register and place it on an internal BUS (BUSI D(15:00)). From there UNIBUS drivers send it to where the program specifies, along with SSYN. (REG.STR \wedge LOCAL). If that were a remote register read, the RS code at the ROM would be sent on the MASSBUS along with CTOD, DEVICE-SELECT and finally DEMAND. The selected peripheral device accepts all this information and replies with TRA, which is now used as a gating signal for the contents of the register read in the device. This information reaches the RH-11 via the MASSBUS "C" lines and goes to the MUX at the top center of the page. This MUX is gated with CNTRL OUT and the register information finds itself on the internal bus going to the UNIBUS, with SSYN being the gating signal. This register information sent on the "C" lines was also parity checked by the RH-11.

That s really all there is to the logic that handles the system registers. If any clarification is needed, there is of course, a source of information in

your colleagues, the course administrator, or the manual:

RJSØ4 Maintenance Manual, pages 4-1 to 4-3

with block diagrams on pages 4-2, 4-4 and 4-5.

TJU16 Maintenance Manual, pages 5-1 to 5-3

with block diagrams on pages 5-2, 5-4, and 5-5.

RJPØ4 Maintenance Manual pages 5-1 to 5-3

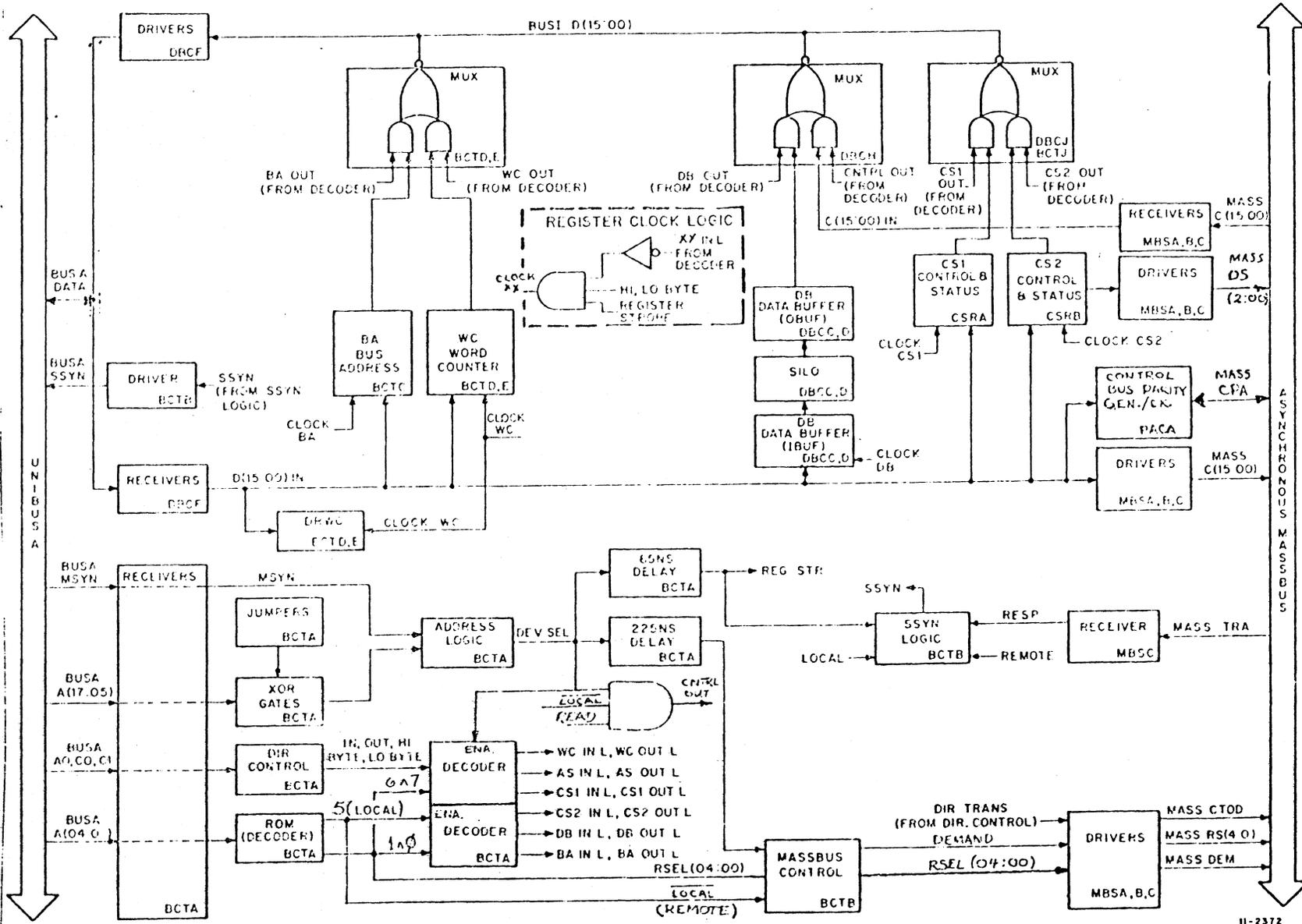
with block diagrams on pages 5-2, 5-4, and 5-5.

REGISTER CONTROL PATH
CRITERION TEST

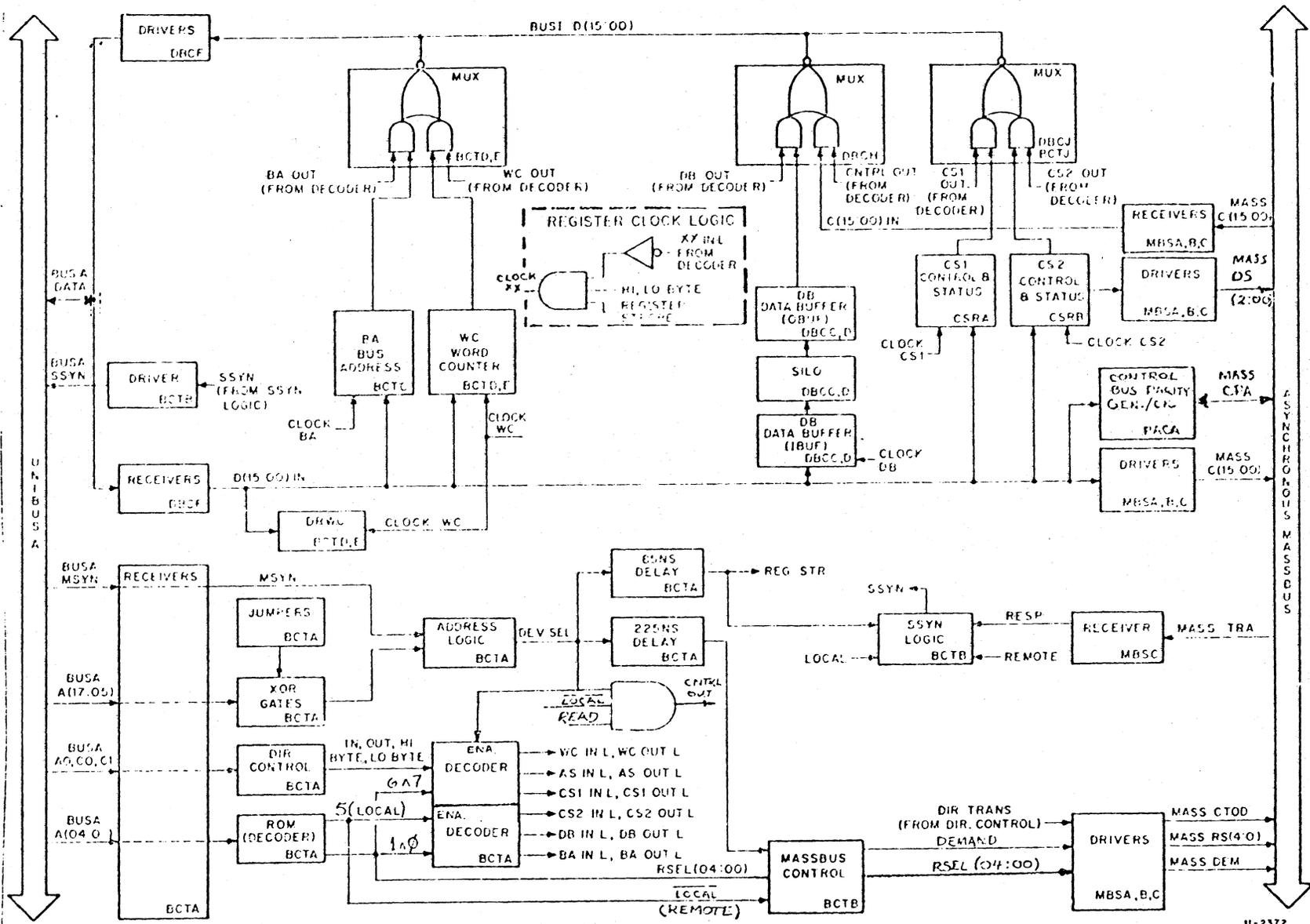
- I. Using the colored pencils and the 4 copies of the block diagrams, trace through a write to a remote register on one of the four diagrams, write to a local register on another of the blocks, and read operations from a local and remote register on the other two diagrams with 100% accuracy in 10 minutes.

- II. Using the hand-out "MASSBUS Device Register Selection" answer the following questions:
 - A. Using the D S (Drive Status) register, in the TU16, as an example, supply the following information:
 1. The UNIBUS address
 2. Register select code
 3. Specify whether or not A5 must be jumpered to XOR gate or to ROM
 4. The jumpers which must be in on the magnitude comparator.

19

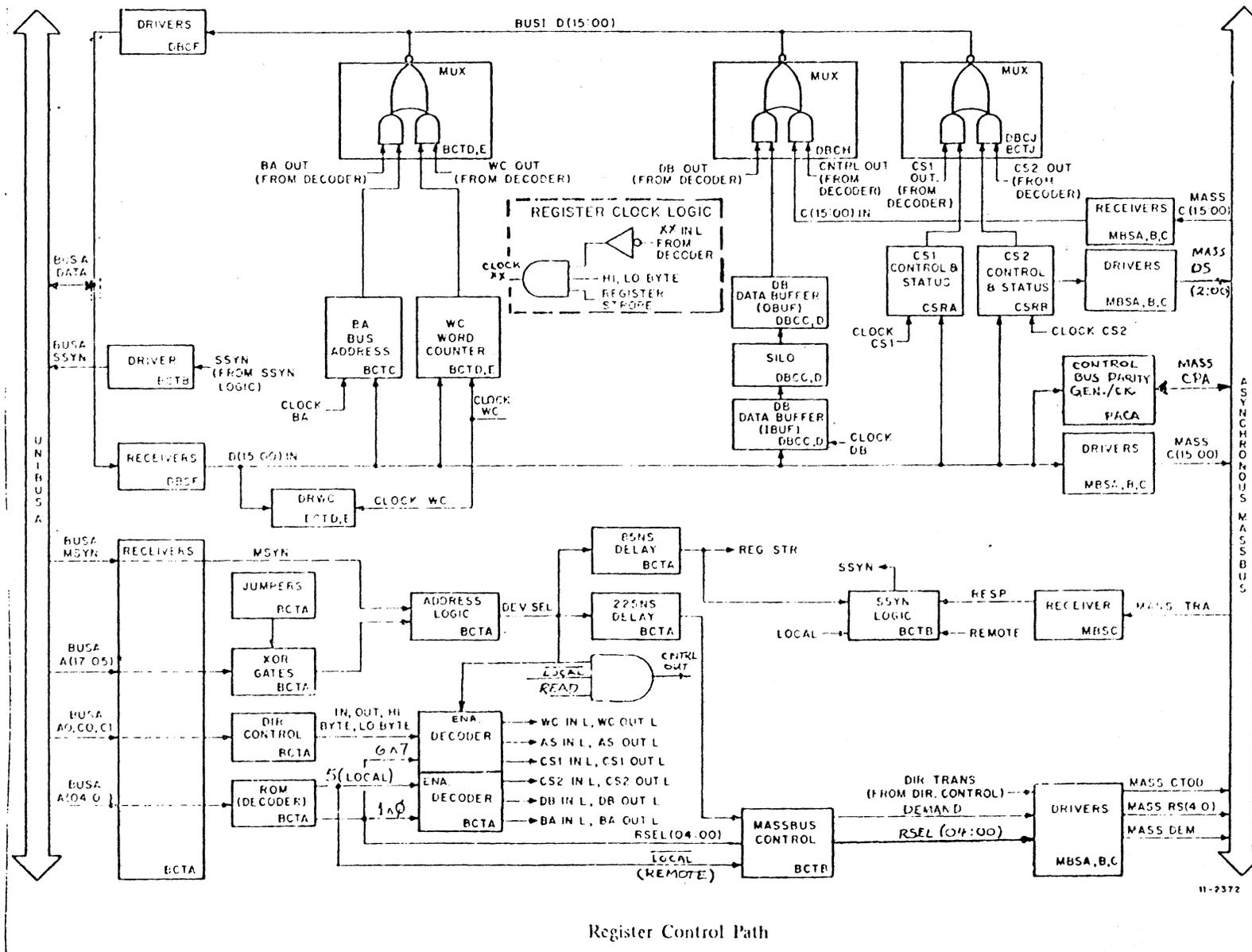


Register Control Path

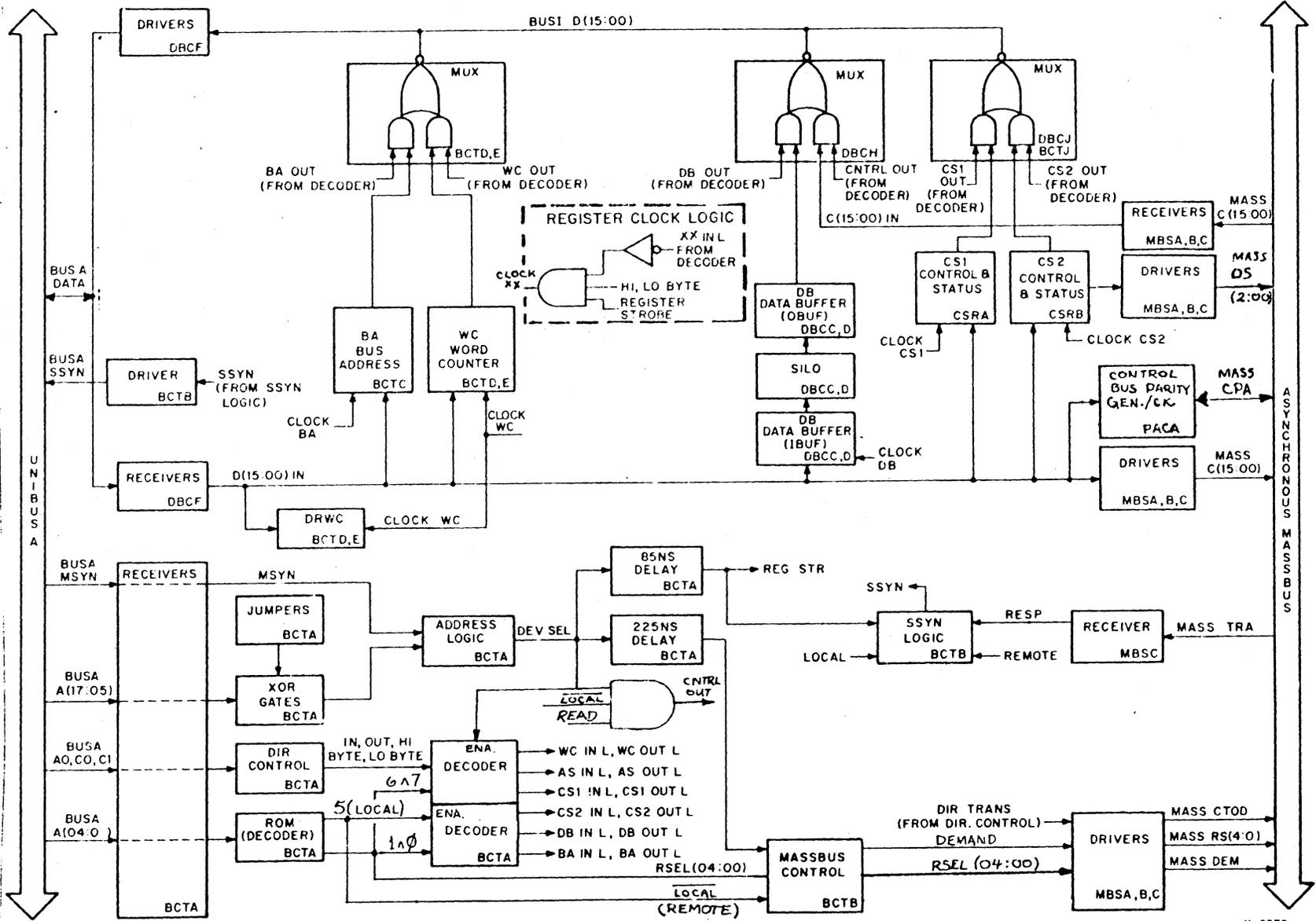


Register Control Path

20

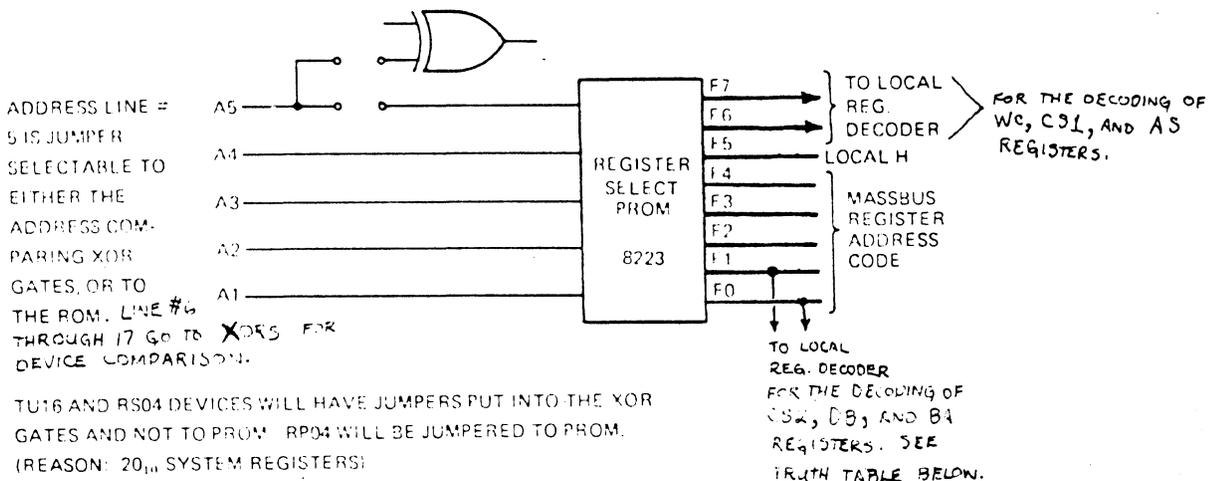


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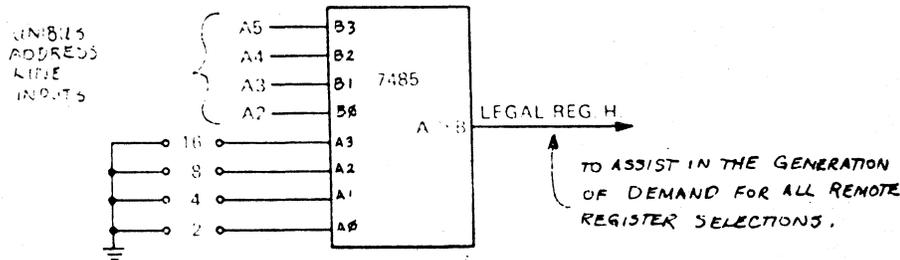
Register Control Path

MASSBUS DEVICE REGISTER SELECTION



ADDRESS LINES 2, 3, 4 AND 5 ARE SIMULTANEOUSLY FED TO A MAGNITUDE COMPARATOR (7485) FOR COMPARISON OF A "JUMPERED-IN" NUMBER OF MAXIMUM REGISTERS ON SYSTEM.

i.e., RP04 HAS 20₁₀ REGISTERS; JUMPERS 16 & 4 WILL BE OUT.
 RS04 HAS 12₁₀ REGISTERS; JUMPERS 8 & 4 WILL BE OUT.
 TU16 HAS 14₁₀ REGISTERS; JUMPERS 8,4 & 2 WILL BE OUT.



INPUT TO ROM FROM ADDRESS L AS: A7

* INDICATES RHII, OR LOCAL REG. ALL OTHERS ARE 'REMOTE', OR IN THE DEVICE ITSELF. THIS IS INDICATED BY THE M5 OUTPUT

OCTAL ADDR	M7	M6	M5	M4	M3	M2	M1	M0
00	L	L	L	L	L	L	L	L
01	L	L	L	L	L	L	L	L
02	L	L	L	L	L	L	L	L
03	L	L	L	L	L	L	L	L
04	L	L	L	L	L	L	L	L
05	L	L	L	L	L	L	L	L
06	L	L	L	L	L	L	L	L
07	L	L	L	L	L	L	L	L
08	L	L	L	L	L	L	L	L
09	L	L	L	L	L	L	L	L
10	L	L	L	L	L	L	L	L
11	L	L	L	L	L	L	L	L
12	L	L	L	L	L	L	L	L
13	L	L	L	L	L	L	L	L
14	L	L	L	L	L	L	L	L
15	L	L	L	L	L	L	L	L
16	L	L	L	L	L	L	L	L
17	L	L	L	L	L	L	L	L
18	L	L	L	L	L	L	L	L
19	L	L	L	L	L	L	L	L
20	L	L	L	L	L	L	L	L
21	L	L	L	L	L	L	L	L
22	L	L	L	L	L	L	L	L
23	L	L	L	L	L	L	L	L
24	L	L	L	L	L	L	L	L
25	L	L	L	L	L	L	L	L
26	L	L	L	L	L	L	L	L
27	L	L	L	L	L	L	L	L
28	L	L	L	L	L	L	L	L
29	L	L	L	L	L	L	L	L
30	L	L	L	L	L	L	L	L
31	L	L	L	L	L	L	L	L
32	L	L	L	L	L	L	L	L
33	L	L	L	L	L	L	L	L
34	L	L	L	L	L	L	L	L
35	L	L	L	L	L	L	L	L
36	L	L	L	L	L	L	L	L
37	L	L	L	L	L	L	L	L

REGISTER ALIASES	FIXED-HEAD DISK	MAG-TAPE	MOVING HEAD DISK
CS1	772040	772440	776700
WC	772042	772442	776702
BA	772044	772444	776704
DA V FC	772046	772446	776706
CS2	772050	772450	776710
DS	772052	772452	776712
ER1	772054	772454	776714
AS	772056	772456	776716
LA V CK	772060	772460	776720
DB	772062	772462	776722
MR	772064	772464	776724
DT	772066	772466	776726
SN	772470	772470	776730
OF VTC		772472	776732
DC			776734
CC			776736
ER 2			776740
ER 3			776742
EC1			776744
EC2			776746

UNIBUS ADDRESS RANGE ADDRESSES.

INTERFACING THE CONTROL BUS

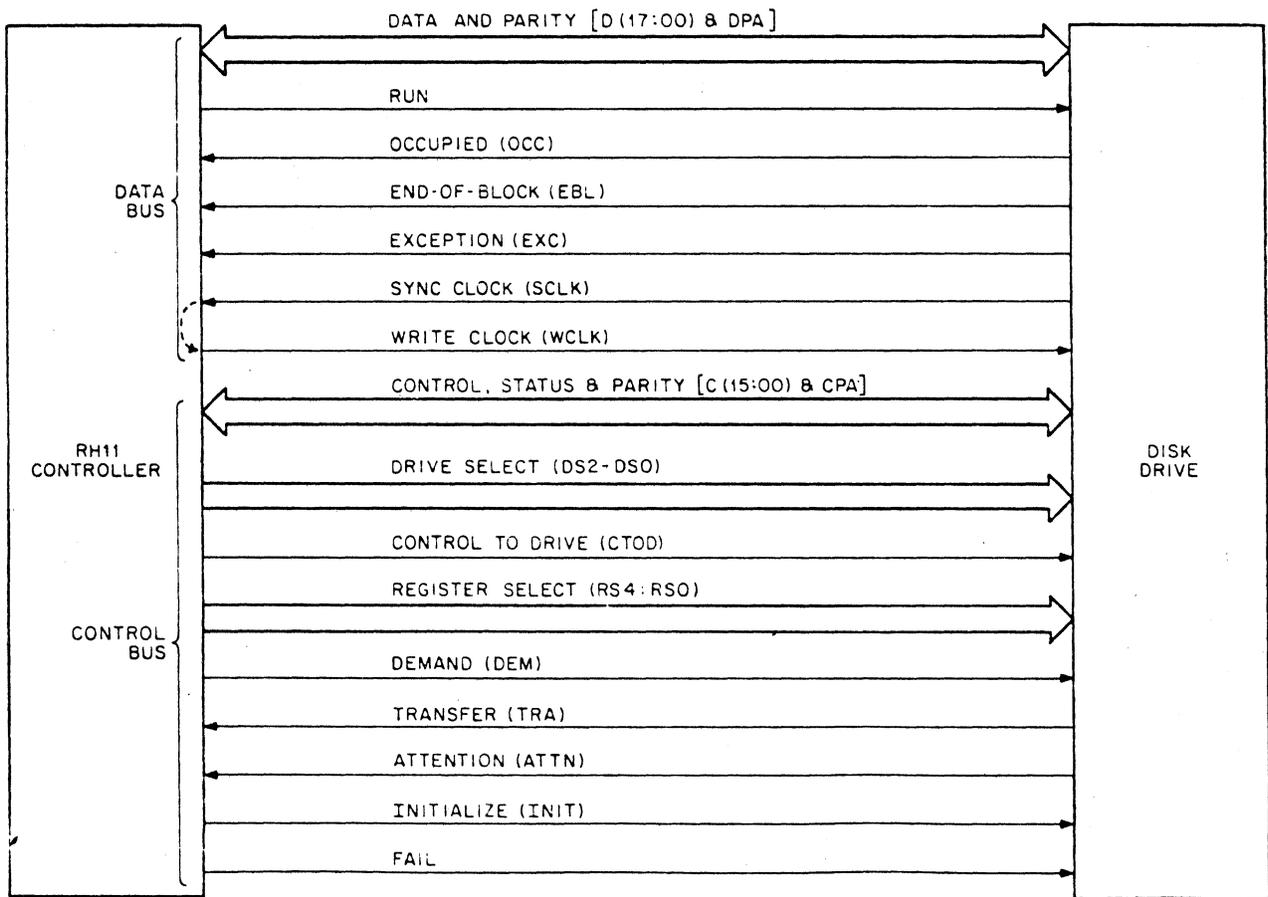
INTERFACING THE CONTROL BUS

OBJECTIVE

Given a list of massbus interfacing signals and a list of definitions, match the name of the signal with its appropriate definition from memory within a time period of 5 minutes.

SAMPLE TEST ITEM

In the space provided adjacent to the definition, write in the letter that corresponds to the signal name it defines.



11-2512

Massbus Interface Lines

CONTROL BUS -

The sort of information that falls under the category of being transferred over the control bus might be status, error, function codes, addresses and the like. Everything, in fact, EXCEPT the data that is to be written or read on the magnetic medium. Therefore a portion of this control bus is made up of 16 "C" lines (C for Control) that this sort of information can transverse. Parity checking/generating is done both in the RH-11 and the possible devices, so a separate control bus parity bit is needed in addition to the 16 C-lines.

Since the RH-11 controller can be cabled to more than one device at a time, there must be a method of determining which peripheral massbus device is to have its registers acted upon. Three lines therefore, are set aside to contain a binary code of the requested unit number. (DS-Device Select lines). Continuing on, once the device is selected via a comparison within the device itself, the logic must be informed which way the register transfer is to take place. If we were dealing with the Unibus we would look to the C1 and CØ lines to govern this direction. On the massbus, the RH-11 controller will assert a signal called CTOD. (A derivitive of C1 & CØ) this simply means that if the program is attempting to load a function code, for example, the transfer is to take place from Controller TO Drive. If status information were requested from a device register, the signal would be negated because the transfer is from drive to controller.

This now begins up another point. Now that the device is selected and knows which direction the transfer is to take place, which of the possible

registers is to be accessed?5 more lines are needed then to cover all possible types of devices and their registers. These 5 lines will be used to contain a Register Select code. (This code is really just a re-interpretation by the RH-11 of the Unibus Address Lines).

The device now has all the control information it needs to carry out the register transfer but one. It knows which register the information will be acted on; (RS lines) which direction the transfer is to take place; (CTOD) it also knows where this information will be coming from or sent to (C-lines). That one missing ingredient is a gating signal sent from the RH-11 to request that the transfer take place. (Remember MSYN on the good ol' UNIBUS?) This gating signal is called DEMand, and it basically is a derivative of MSYN. And, like MSYN, it will require a reply from the mass-bus device as to the device's acceptance of the command to read or write a register. This signal is called TRAnsfer, and is generated as a result of a short delay triggered by DEM and being selected. (Good comparison of DS lines to unit switch.)

Some examples: A register write is to take place. The RH-11 controller would have had to send DS, RS, CTOD, and the information to be loaded into a register on the C-lines to know which of them is being requested. Then, after a short deskewing delay, DEM is asserted to inform the device that "Here comes the data". The device, in this example is expected to respond with TRA to let the RH-11 know that there is a device "out there" that is selected, and that it accepts the information sent to it.

A second example involves a register read of status information. The RH-11 must send over DS, RS, CTOD and allow a short period of time for unit #

selection & decoding before asserting DEM which is now acting as a request for a transfer. If the unit # agrees, then the device accesses the desired register and sends it out to the massbus C-lines with the gating signal called TRA so the RH-11 can know that it, in fact, did respond to the command to read a register.

This completes the discussion of all that is required to communicate register information to/from a massbus device and the RH-11. There are, however, three more signals we will mention here due to their affect on the system.

One of them is INITIALize (which you must have heard of before, SOMEWHERE".) and another is MASSFAIL. The latter is a reflection on the ability of the RH-11 to accurately send/receive data by monitoring the power supply that governs operation of the RH-11 logic. The third is a signal called ATTENTION. This signal is only asserted by the massbus devices when any of them demand a program interrupt due to the completion of functions that the RH-11 did not partake in, or a change in the device's status that would require an interrupt. This is a separate wire on the mass-bus cables that goes to all eight devices. When the interrupt is processed all that is known is that the RH-11 with some mag-tapes, or disks on it caused the interrupt to the program. What is not known is which device out of the possible eight caused the interrupt nor why.

This is the reason that there is an attention summary register in each of the peripheral devices. This register consists of one flip-flop representing the attention status of that device.

When the program wishes to read the contents of the attention summary register, the MOV command to the RH-11 issues a remote register read, and since we are dealing with only one flip-flop, or bit position in each drive, the normal condition of selecting only one drive for the register operation is bypassed. For this one special case all eight devices are accessed for the remote register read.

Within each device then the particular unit number of that device gates the attention status out on the massbus "C" line that equals the unit number. Therefore eight devices send out their attention status on a different "C"-line to be examined by the program.

As a further aid in assisting the program to find out what is going on, there is within each device, a status register, an error register, a drive type register and for some, a serial number register.

These registers should be discussed in some other detail when you discuss the peripheral device itself.

Well that's it for this lesson - - Get any questions you have unanswered - - answered and then continue.

ADDITIONAL RESOURCES:

RJSØ4 Maintenance Manual, Page 2-1 paragraph 2.3

TJU16 " " " "

RJPØ4 " " " "

RSØ4 Service Manual, page 2-1, paragraph 2.2.1

INTERFACING THE CONTROL BUS
CRITERION TEST

Directions: In the space provided beside the list of definitions, write in the number of the corresponding signal name that matches that definition.

- | | | |
|------------------------|--|-------|
| 1. ATTN | A. A signal that aligns the logic in the device to write into a register rather than read. | _____ |
| 2. Transfer | B. A code which aligns the logic as to which device register is to be operated on. | _____ |
| 3. "c" lines | C. A signal which will clear out all device registers when asserted. | _____ |
| 4. INIT | D. A code which will inform the device logic as to which one of the 8 possible devices is being requested to do a register transfer. | _____ |
| 5. Demand | E. A signal which is used to denote whether the information being transferred contains an even number of logical "ones" in it. | _____ |
| 6. DS lines | F. A group of lines assigned on the bus to carry the designated register information. | _____ |
| 7. CTOD | G. A signal which will generate a software interrupt due to device status changes. | _____ |
| 8. RS lines | H. A signal which informs the device of a bad RH-11 power supply. | _____ |
| 9. MASSFAIL | I. A signal that will act as a transfer reply to the command of transferring register information. | _____ |
| 10. Control Bus Parity | J. A signal which will inform the device logic that a transfer is taking place. | _____ |

RH-11
DATA PATH

INTRODUCTION

You have, at this point in time, covered enough material on this Massbus Controller to start block diagramming the data path for this device. In completing this module you will be more prepared to tackle the engineering drawings (if needed) because you have at your disposal 4 block diagrams which show you the overview of the whole data paths, (this lesson) and then an individual block diagram for each of the 3 data transfer functions (next lesson) showing you a more complete "picture" of the silo operation, NPR initiation, and device transfer termination.

Each of these "blocks" also contains the engineering drawing page number for future reference.

DATA PATH

Objective

- I. Given the "DMA DATA PATH" block diagram, with a list of the functional block names and a list of the block definitions, match the name of the signal with its appropriate definition.

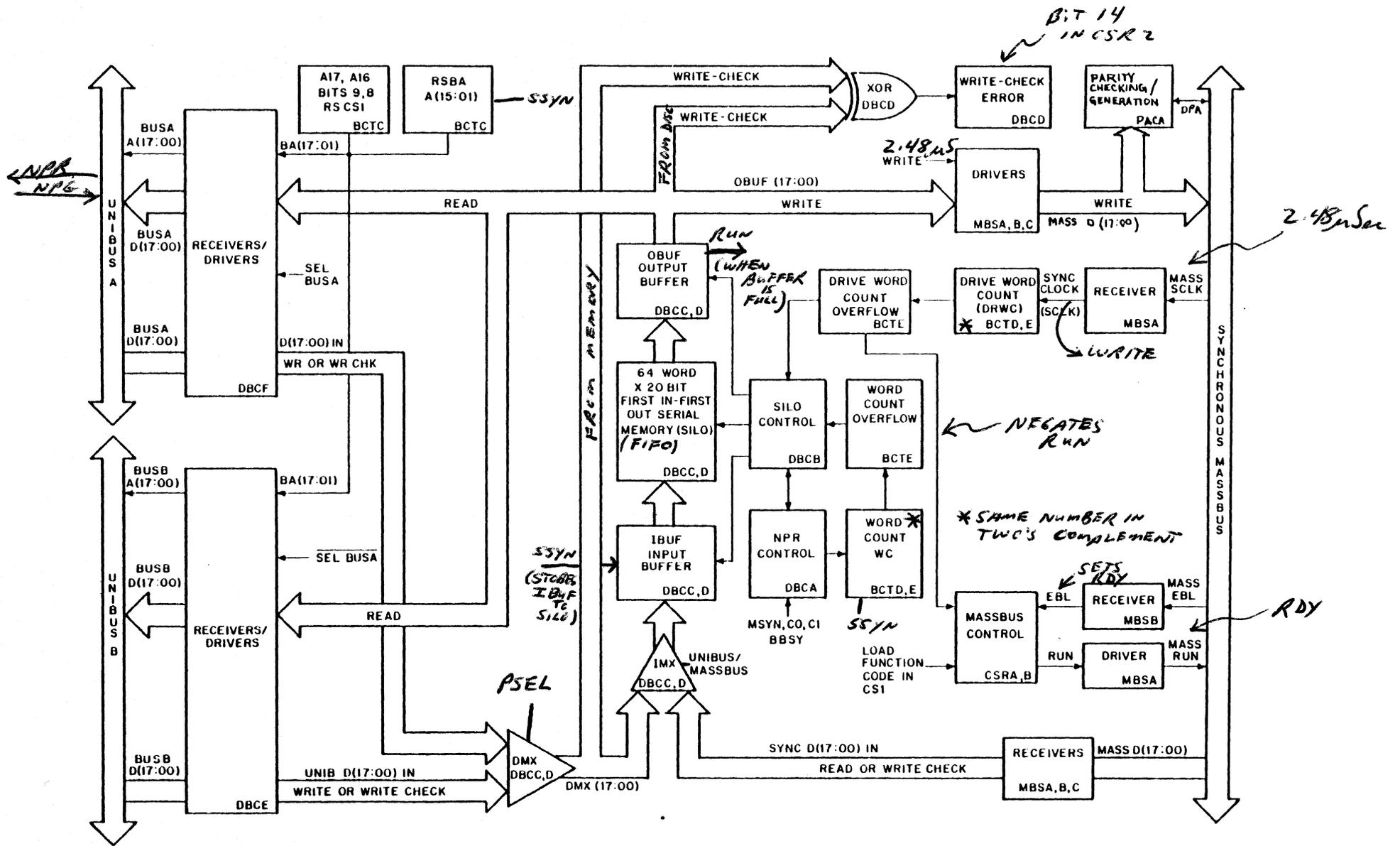
- II. Given the "DMA DATA PATH" block diagram, briefly describe the purpose of the two Unibus inputs and how the program would select them.

The above questions should be completed within 10 minutes with no errors.

What to do

Basically, read over the material on the data paths to get a good handle on the basic circuits involved, study the block diagram, look over the additional reading pages assigned in the back, (read them if you feel you have to, but if you feel the presentation within this module is sufficient to learn about the data paths concepts, then there is no need).

Next re-read the objectives, see if you can fulfill them, and when you can, ask for the criterion exam. Do not forget, however, that while working on these lessons, group discussions are not only permitted but encouraged.



DMA Data Path Block Diagram

SSYN: CLOCK DATA TO IBUF
 INCR WORD COUNT REG BY ONE
 INCR BUSS ADDR REG BY TWO

DATA PATHS

The "Heart" of this device's data path, is the 64 x 20 bit memory that is responsible for the "easing" of the vast timing differences between the data transfer rate that occurs on the UNIBUS and the data transfer rate on the MASSBUS.

The newer Hi-speed disk drives approach the practical operating limit of the UNIBUS. This increases the odds considerably that words will get lost in the data shuffle if there were no place to "stack" them until such time as it is convenient to transfer them. This "stacking" device consists of a FAIRCHILD made, MOS-type memory (DEC 3341) called a SILO. This silo is a first-in, first-out device that is also currently being utilized in the RP11-C/E disk pack controller.

The 3341 chip is a serial memory. This means that words are not random accessed, they are sequenced through. Built right into the chip there is logic that enables it to keep track of the next location to fill as well as the next available location to be emptied. It is also asynchronous in that it can be both filling and emptying simultaneously.

The manufacturer makes them in 64 x 4 bit sizes, so we wire 5 of these chips in parallel to obtain our desired word length of 18 bits (Convenient for connecting to a Unichannel 15 system). These chips require -12 volts for operation, so on one of the two hex-boards in the RH-11 there is a silo power supply which drops the available -15 to a smooth -12. It has

no over - or - under voltage protection however. If the systems -15V is too high, then the silo power is too high, and, POOF! The worst! or, at the very least, erratic operation. The moral of the story is keep your system -15 at -15V. If you find problems with the RH-11, check the -15 coming in, and if too high, adjust it and check out the RH-11 with the diagnostics. If still bad first prove that the silo works. There are routines within the diagnostics to check it, and check it well.

Let us now take a look at this Silo and how it fits into the scheme of things. The enclosed "DMA DATA PATHS" block diagram shows the silo almost in the middle of the page. (This block by the way, is a re-print out of the RH-11 manual with just a few corrections).

The silo is the receiver of data for a read as well as for a write function. Its input is a multiplexor (IMX) that is gated with the appropriate function code (write from Unibus, read from Massbus). Data arriving for a write function comes by way of either Unibus "A" or Unibus "B" depending upon the program selection (Bit 10 of CS1) and, of course, the system configuration. The data is gated through the DMX (Data Multiplexor) with the help of this bit, and then sent to the IMX.

The Input Multiplexor then sends the data word to a holding register called the Input Buffer where the silo control logic moves the word to the silo (unless it is already full).

The silo chips with their built-in logic moves the word through the 64 locations to an Output Buffer Register. The silo combined with these two registers just named, comprise a data buffer of 66 words.

Output Buffer contents are then sent to the massbus drivers in the case of a write data function, or to the Unibus drivers in case of a read data function.

The NPR cycles are initiated by the status of the silo INBUF or OUTBUF registers, (to be discussed in next lesson in detail) while the Massbus cycles are initiated by the requests from the peripheral device itself. This request line is called SYNC CLOCK. (For synchronous)

The bus address is represented on this block because it is needed for the NPR's (all 18 bits of it). There are two word count registers represented because of the difference in the timing between the input to the silo and the output from the silo. It is very conceivable to have word count overflow but still have words within the silo to transfer.

As an addition, to check against the possibility of dropping bits on the massbus, a parity checker/generator is installed in the RH-11 on its own double height module.

To take care of the write check function the device handles it as a combination of a read and a write. The peripheral device is told to read, and so it sends data to the silo via

the IMX. These words pass through the silo, and upon arriving at the output buffer, wait for a word to arrive from memory. In other words, the RH-11 handles everything as if it were a read data function, but when it comes time to do an NPR it initiated a DATI instead of a DATO. The memory word then, would be arriving over one of the buses until arrival at the DMX. From here it goes directly to the XOR comparison gates which already have the contents of the OUTBUF at their disposal.

The data from memory does not reach the device, and the data from the device does not reach memory. The two words are checked for equality only.

The block diagram only shows you the path the data must take as it passes through the RH-11 interface on its way to the peripheral or memory. An in-depth view of how the silo works is shown on the other three block diagrams in the next lesson.

ADDITIONAL RESOURCES

RJS04 Maintenance Manual Pages 4-3 through 4-11

RJP04 Maintenance Manual Pages 5-3 through 5-11

TJU16 Maintenance Manual Pages 5-3 through 5-11

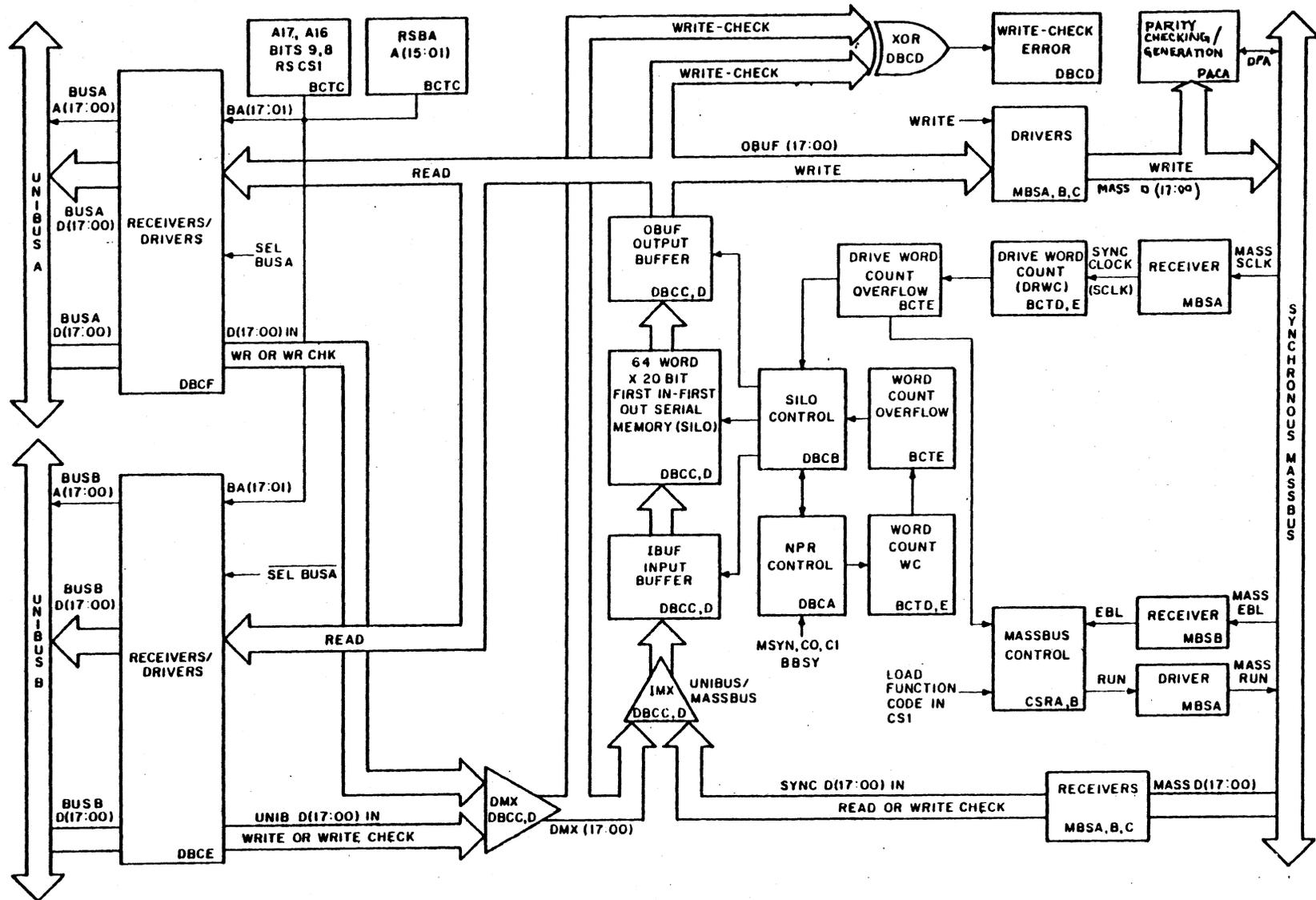
DATA PATHS
 CRITERION TEST
 page one of two
 -15 MINUTES ALLOCATED-

I. In the space provided beside the definitions in the right hand column, write the letter equivalent to the block diagram terms using the "DMA DATA PATH" block diagram, as a reference.

- | | | |
|-----------------------------|---|-------|
| A. Receivers/Drivers @ DBCF | 1. Provides a gating path for either Unibus "A" or "B" on a write data or write check functions. | _____ |
| B. XOR @ DBCD | | |
| C. SILO @ DBCC,D | 2. The start command to the peripheral device. | _____ |
| D. DMX @ DBCC,D | | |
| E. WORD COUNT @ BCTD,E | 3. A storage area to allow words to "stack" reducing the event of data late errors. | _____ |
| F. IMX @ DBCC,D | | |
| G. OBUF @ DBCC,D | 4. The place where comparisons are done. | _____ |
| H. MASS RUN | | |
| I. MASS EBL | 5. A signal sent from the device that requests the data words from the RH-11. | _____ |
| J. MASS SCLK | | |
| | 6. A storage place for the program count of the words left to transfer. | _____ |
| | 7. Provides a gating path for either the words from memory or the words from the peripheral device. | _____ |
| | 8. Signal from the device to indicate that it is at the end of a defined data block. | _____ |
| | 9. The gating path for Unibus "A" data. | _____ |
| | 10. The storage area for the next word to be transferred. | _____ |

DATA PATHS
CRITERION TEST
page two of two

II. Using your "DMA DATA PATHS" block diagrams, briefly describe the purpose of the two unibus inputs and how the program goes about selecting the.



DMA Data Path Block Diagram

SILO MEMORY OPERATION

Here is the follow-up lesson to the data paths. Contained in this lesson are 3 block diagrams that will point out to you:

1. How READY is generated and subsequently dropped.
2. How RUN is generated and subsequently dropped.
3. How the SILO accepts/respects data.
4. What SYNC CLOCK does in the RH-11.
5. What EBL does in the RH-11.
6. The function of the two word count registers.
7. How NPR's are initiated for Write/Read operations.

Ready? If not, take a 10 minute break come back and start.

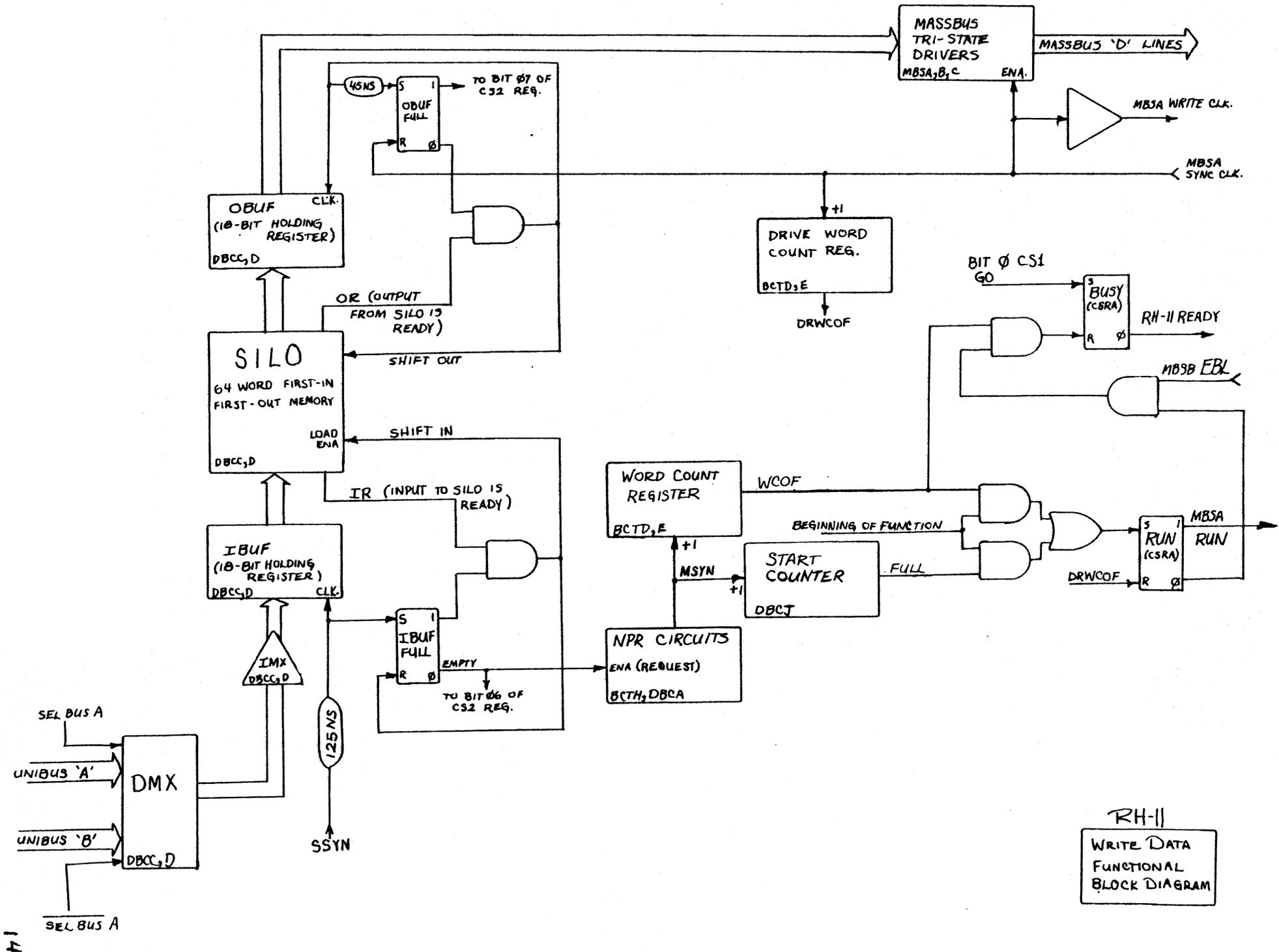
SILO OPERATION

OBJECTIVE:

Given the 3 data transfer function block diagrams:

1. List all the conditions necessary to initiate NPR's.
2. List all the conditions necessary to fill the silo.
3. List the conditions necessary to empty the silo.
4. Describe the difference between the way the RH-11 handles data for a read data function as opposed to a write check function.
5. Write a brief description of the use for write clock.
6. Specify what informs the peripheral device to stop requesting Massbus Transfers.

TIME LIMIT: 15 minutes



RH-II
WRITE DATA
FUNCTIONAL
BLOCK DIAGRAM

WRITE FUNCTION

The first event to occur will be an NPR to get the first word from memory. MSYN is generated via the NPR circuits because it is a write function and the IBUF Full F/F says the IBUF register is empty. The resultant MSYN increments the start counter. This counter will help to generate the massbus signal RUN to the device. The counter is jumper selectable to one of three capacities. "FULL", "HALF", or QUARTER". This allows the optimum utilization of the silo taking into consideration the different peripheral-type speeds. Normal installation (so far) is for all the devices to use "FULL". This means that RUN will not be sent to the device until the silo contains 64 words. (Or the word count has overflowed!) This ensures that the Unibus, which operates asynchronously, gets a 64 word head start on the mass bus which operates at a synchronous rate. After all, isn't that the purpose of the silo?

Upon arrival of a data word from memory, the IBUF FULL F/F set. Logic will then be monitoring the condition of the silo's first input location. If IR is asserted and IBUF full is set, a signal is generated that transfers that word to the SILO simultaneously clearing IBUF FULL. If the word count has not overflowed, then the same conditions are met as before and another NPR is generated.

The cycle continues. NPR's keep on being generated as the IBUF keeps emptying. As the silo keeps accepting new words, the old ones keep moving to the next successive location within the silo.

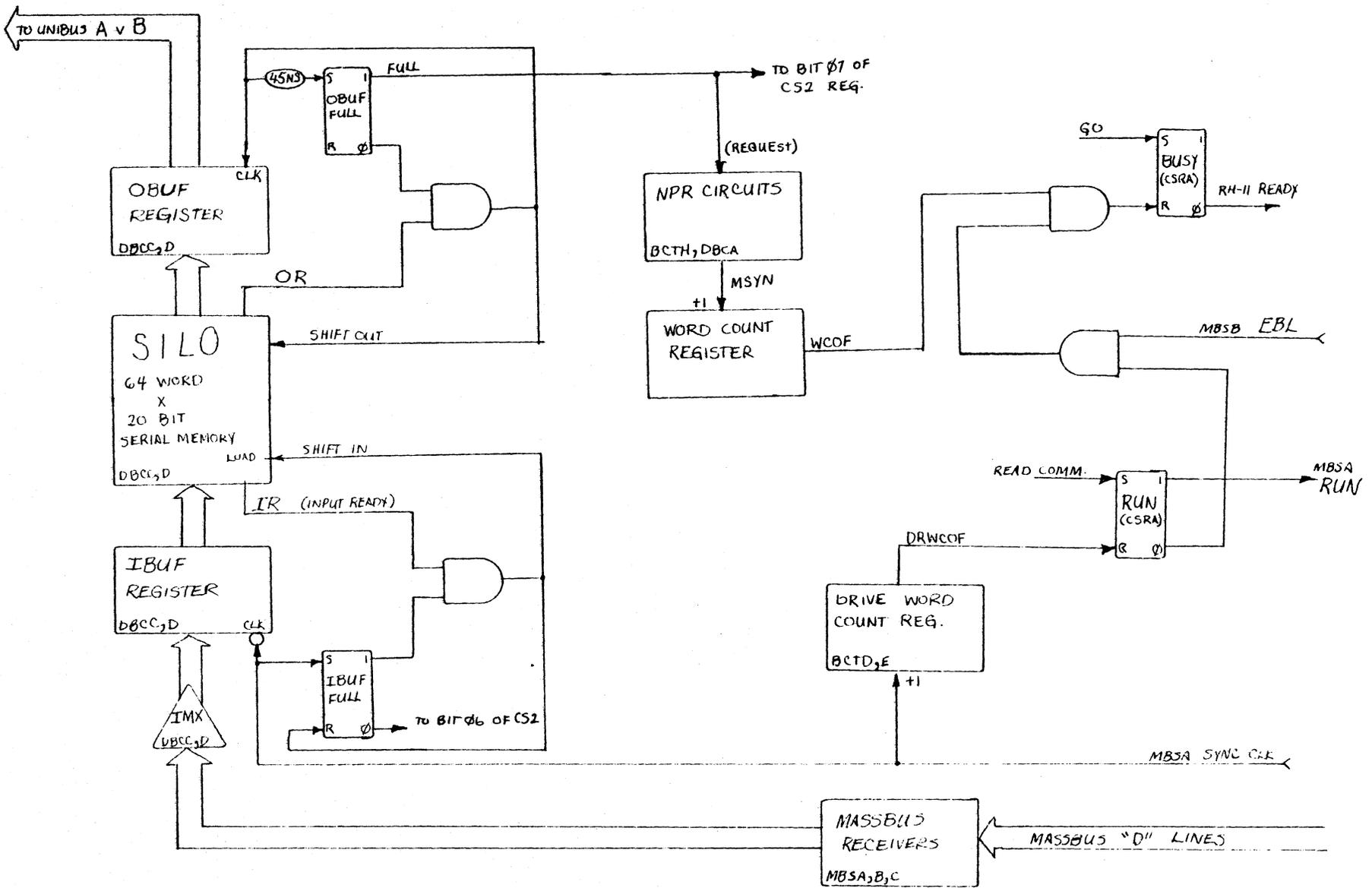
As the first word reaches the other end of the silo, Output Ready is generated and that causes a move to the OBUF Reg.

Words start "stacking" within the silo as it continues to fill at the Unibus NPR rate. At some point, the silo cannot generate input ready because the first location cannot be emptied. (It is FULL!) This in turn causes a cessation of NPR's (temporarily). At about the same time, the start counter had incremented to the "FULL" state, and now RUN is sent to the disks to initiate the search for the desired sector, or to the magtape to initiate tape movement through the inter-record gap.

When the devices are ready to write, SYNC CLK is sent to the RH-11, and if you are following on the block: (1) Generates WRITE CLOCK which gates the word to the device. (2) Enables the massbus drivers to send the word. (3) Increments the drive word count register. (4) Resets OBUF FULL F/F to start the silo moving words again. (Shift Out)

We have now initiated massbus data transfer cycles by generating RUN. The device, when ready, then sends sync clocks to request a word from the silo and the RH-11 responds with Write Clock. All the time this is going on, the NPR logic is monitoring the silo's condition and will generate NPR cycles as long as word count overflow has not occurred and the IBUF is empty.

Some of the extra points to remember: First, that "run" determines when the devices start so that when the hardware has written a block of data (for disks only) and there are still more words to write, RUN sets up the device logic to write in the next available block. Conversely, the lack of RUN at the completion of a hardware block means "stop writing" to the devices. Got all that? If not review, or ask, or read, or discuss, but do something because READ is next.



RH-11
READ DATA
FUNCTIONAL
BLOCK DIAGRAM

READ

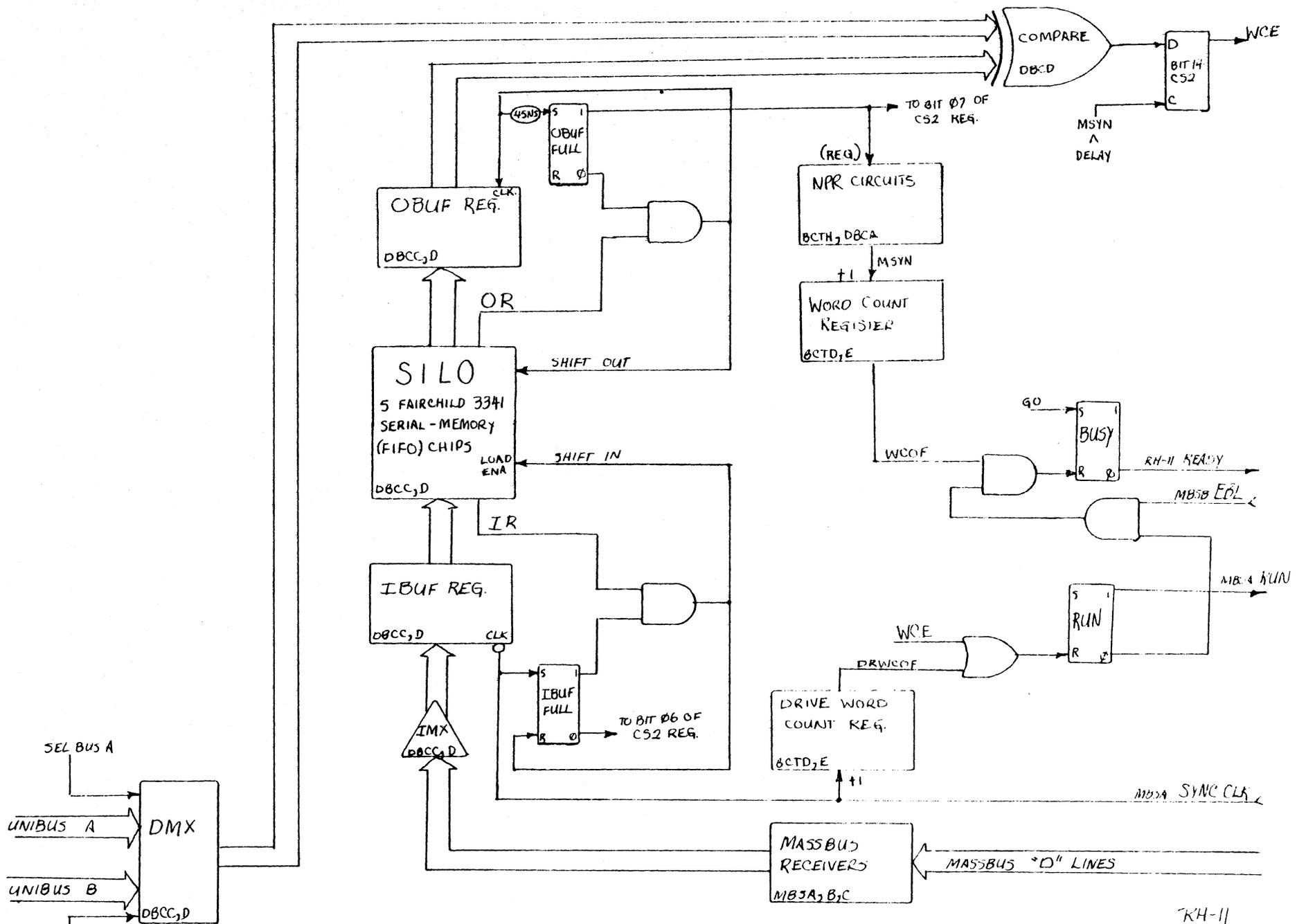
To initiate reading, RUN is again asserted, but without the aid of the start counter. When the device is subsequently ready to transfer the first word over, the RH-11 is notified by the presence of SYNC clock.

Sync Clock will then increment the drive word count, and, at its trailing edge load the IBUF REG. and set IBUF FULL. The silo sequence from here is the same as in a write function.

The exception is the generation of NPR's. Instead of requesting a word when IUF is EMPTY as in the write function, the NPR's are generated when the OBUF is full.

Note that in the write function and read function both, the drive word count register determines the status of the massbus signal RUN. If, during a write function, the word count overflows, and you are at the end of a disk sector, that doesn't mean you have finished due to the silo still containing words to be written. RUN is still asserted if you will note, because "DRWCOF" has not occurred. The next sector will then finish up with the word count, then RUN combined with the device "EBL" and "WCOF" act together to assert ready by dropping "BUSY".

The same philosophy holds true for a read function. This time however drive word count overflows FIRST negating "RUN". To be considered "READY" though, it is still necessary to have "WCOF" from the Unibus and an "EBL" from the drive.



KH-11
WRITE CHECK
FUNCTIONAL
BLOCK DIAGRAM

WRITE CHECK

This block is identical to the read block with the exception that the NPR's generated are "DATI's" instead of "DATO's". This brings a word in from memory to the "DMX" where it is compared with the word presently in the OUTBUF Reg.

SUMMARY

These block diagrams serve to "point the way" in following the action within the RH-11 without having to "gate chase" everything. It also is much easier to reference a block diagram in the future, than to tackle the engineering drawings cold when working on a problem.

Any further study on the subject can be done by you after you have mastered the basic concepts.

One other point: I made no mention of it in this module, but in the "INTRODUCTION TO MASSBUS" it was stated that the NPR's done by the RH-11 would be of a "back-to-back memory reference" type for Unibus "A", and a "BUS HOG" mode for Unibus "B". This still holds true, and in the additional resources you will find it explained if you wish details of logic operation.

ADDITIONAL RESOURCES:

RJSØ4 Maintenance Manual pages 4-3 through 4-11
with flow charts starting on page 4-11.

RJPØ4 Maintenance Manual pages 5-3 through 5-11
with flow charts starting on page 5-11.

TJU16 Maintenance Manual pages 5-3 through 5-11
with flow charts starting on page 5-11.

After clearing up unanswered questions with additional reading or the Course Administrator, check back over the objectives. When you are ready, ask for the test on the area, and continue.

Keep up the good work!!

SILO OPERATIONS
CRITERION TEST
Page two of two

- IV. Using all of the block diagrams, what informs the peripheral devices to stop requesting massbus transfers, and how was it brought about?

INTERFACING THE DATA BUS

INTERFACING THE DATA BUS

OBJECTIVE:

Given a list of massbus interfacing signals and a list of definitions, match the name of the signal with its appropriate definition from memory within a time period of 5 minutes.

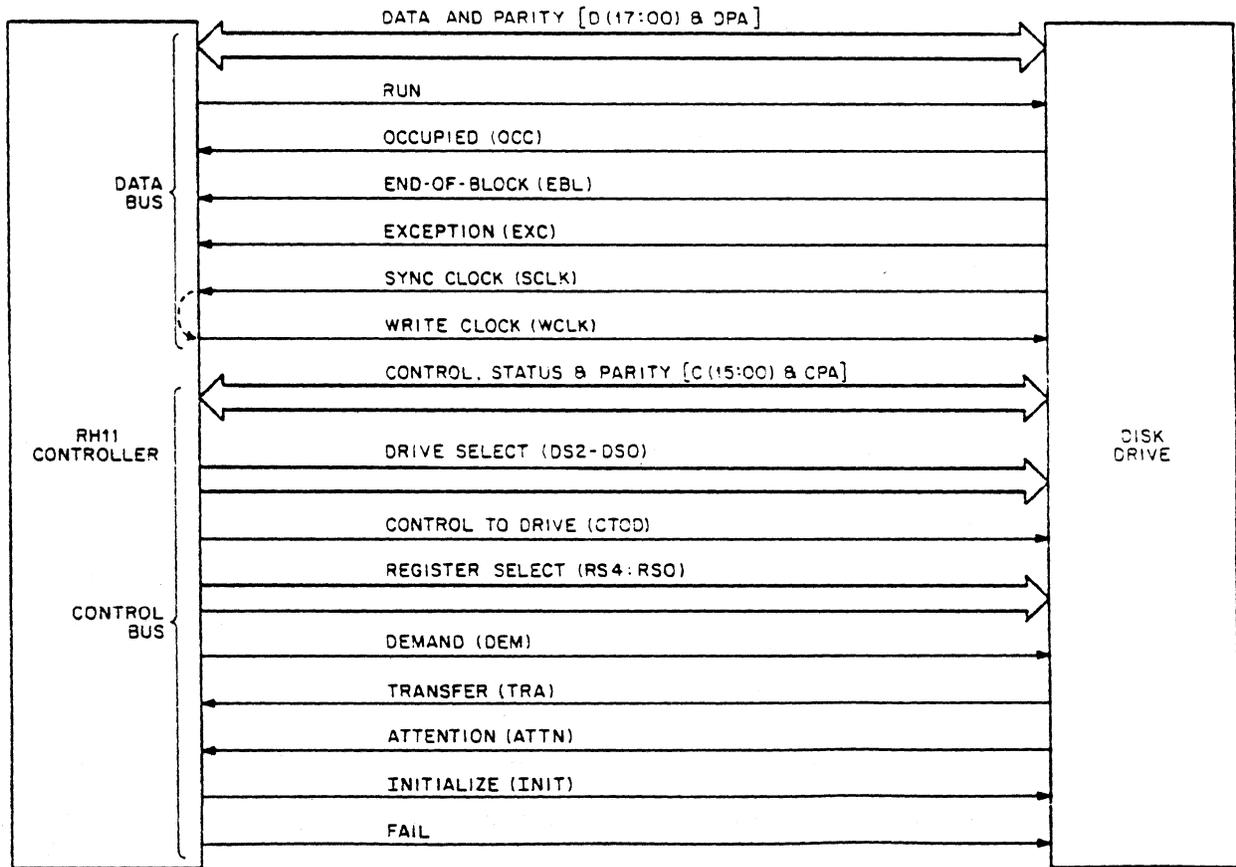
SAMPLE TEST ITEM:

In the space provided adjacent to the definition, write in the letter that corresponds to the signal name it defines.

WHAT TO DO:

Read over enough of the material, either in this learning module, or using any of the listed manuals and its associated illustration and explanation to get a good "feel" or "understanding" of the type of communication that takes place between a controller (RH-11) and one of its 8 devices when transferring data to/from core memory. The selection of which one of the 8 devices is to handle data is done by the device registers themselves and therefore covered within the module entitled "Interfacing the Control Bus".

Remember, we are only concerned with the communication that must take place, not with the data flow through the RH-11 or the device. When you feel confident in being able to describe the interfacing signals' purpose in the communication of data, then ask for the criterion test on this area.



11-2512

Massbus Interface Lines

DATA BUS

As its name implies, this is the path the stored information takes on its way to the magnetic medium, or to core memory. Any information that may be written or read from a device register is handled by another grouping of signals called the control bus. At the present time we are only concerned with the communication to make the data bus active.

First, we will need 18 "D" lines (D for data) to enable the 18-bit data word to transverse the cables on its way to/from the RH-11. 18 bits are used in order to be capable of inserting the mass storage device on just about any DEC family of C.P.U.'s with little or no change. As far as the 11-family goes, the upper two bits will always be zeros.

Parity is checked a word at a time on this bus as well as the control bus, so another signal wire is needed to send/receive this parity information itself. (DPA - Data Parity) this makes the data portion of the bus 19 bits wide.

In addition to the "path" for data to flow on, we will need some controlling signals to coordinate this venture.

The first to be discussed is a signal called RUN. Run will be asserted by the RH-11 to signify to the device that it may start the already programmed function because the RH-11 is now ready. The GO bit had that dubious function in the previous UNIBUS controllers, but cannot do it now because the large data buffering capabilities in the mass controller, changes the data transfer timing.

(More on this in the lesson DATA PATHS). So, right now, note that the devices do not start moving tape or searching for the desired sectors until RUN initiates them to do so.

Another term deemed necessary by the engineers is called OCCupied (for, "DATA BUS BUSY"). Just as soon as the respective massbus devices respond to the programmed function code that desires data to be moved, OCC is asserted by the device to inform the RH-11 of its intent to carry out the function. It does this by knocking down an error that is in the process of being timed out. This error is known as Missed XFer.

The signal we have been waiting for is here. This is the one that requests the transfer of one word whether it be from the RH-11 to the device, or from the device to the RH-11. This signal is called Sync CLK (Short for Synchronous Clock). Of course the device is the responsible party for generating it. It knows when the word has been read and ready to be sent to the RH-11. It knows when it is time to write the word on the medium. When each of these conditions are ready, the RH-11 is informed with SYNC CLK.

When performing a read operation, the leading edge of SCLK triggers the RH-11 and the trailing edge strobes the data across the cables into the RH-11. When a write function is being performed, the device informs the RH-11 of its readiness to accept a word for writing, but the cables on the massbus may be short, or very long, depending upon the system configuration. This means the device does not know when to expect the word back from the RH-11, so another term is needed as a gating signal. It is sent from the RH-11 upon receipt of sync clk to inform the device that the word it requested has arrived. Let us call this term Write Clock.

It is simply sync clock turned around and retransmitted back to the device. There will be enough sync clocks generated to fill a sector in the disks, or write a record on tape.

The sector or record continues to be read or written until the devices sense that it is at the End of Block. This signal informs the RH-11 of that fact.

Any errors that may be found by the device are sent to the RH-11 in the form of a signal called EXception. Certain specific errors can cause a premature EBL in an attempt to terminate the operation. These errors are stored in the device's own error register. That does it. All communications for any device to xfer data to the RH-11 has been shown to you. Between this module and the one on "Interfacing the Control Bus" you have, or will have all the information necessary to know how an RH-11 talks to any type of peripheral.

ADDITIONAL RESOURCES FOR THIS ACTIVITY:

RJSØ4 Maintenance Manual, page 2-1, paragraph 2.2

TJU16 Maintenance Manual, page 2-1, paragraph 2.2

RJPØ4 Maintenance Manual, page 2-1, paragraph 2.2

RSØ4 Service Manual, page 2-3, paragraph "Data Bus is Defined as Follows"

INTERFACING THE DATA BUS
Criterion Test

DIRECTIONS: In the space provided beside the list of definitions, write in the corresponding signal name that matches that definition.

- | | | | |
|---|-----------|--|-------|
| 1 | EBL | A. A signal when asserted gates the word from the RH-11 to the peripheral device. | _____ |
| 2 | "D" lines | | |
| 3 | WCLK | B. A signal which is used to denote whether the information being transferred contains an even number of logical "ones" in it. | _____ |
| 4 | DPA | | |
| 5 | SYNC CLK | | |
| 6 | EXC | C. A signal used to inform the RH-11 of its intent to carry out the already programmed function. | _____ |
| 7 | OCC | | |
| 8 | RUN | D. A group of lines assigned on the bus to carry the data to be transferred. | _____ |
| | | E. A signal which informs the device logic as to when to start the programmed function. | _____ |
| | | F. A signal sent by the device to designate that the end of a logical record has been reached. | _____ |
| | | G. A signal that is used by the device to request that a word be transferred | _____ |
| | | H. A signal that denotes to the RH-11 that the device doing the data transfer has encountered an error. | _____ |

MASSBUS CABLING

MASSBUS CABLES

OBJECTIVES:

Given the massbus transceiver logic diagrams for a massbus device and the RH-11, be able to signal trace through the diagrams.

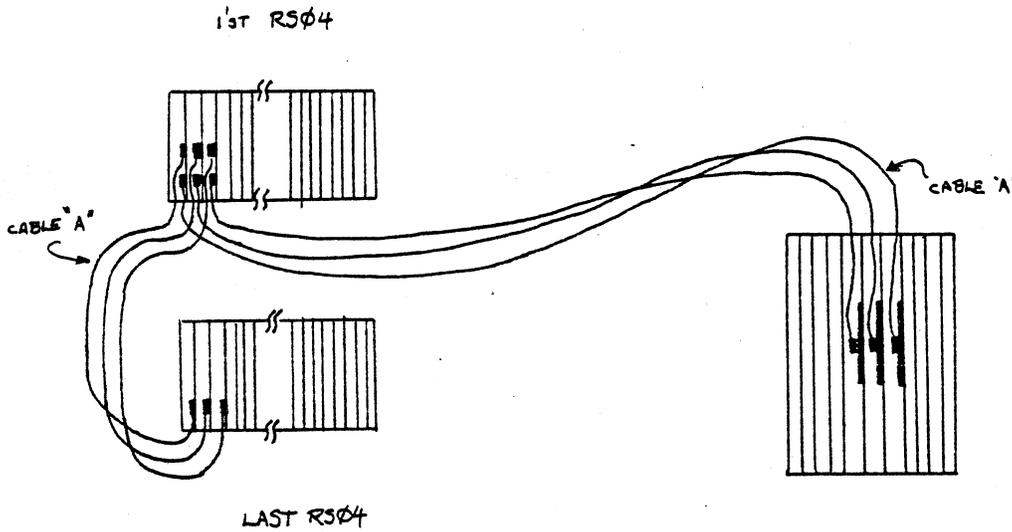
Your ability will be demonstrated by labeling on the diagrams the inputs, outputs, and voltage levels in-between to a 90% accuracy.

WHAT TO DO:

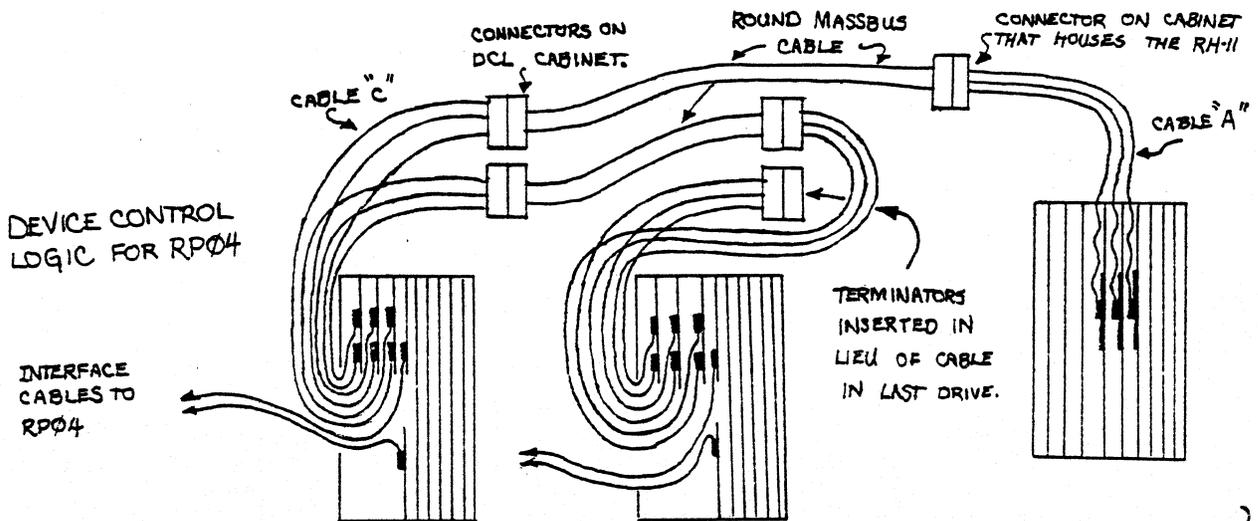
Read over the module in its explanation of the cables and their transceivers. In it will be examples of signal transmission to/from the RH-11. When you have finished, you can look over some of the supplementary material if you desire. The important thing to remember is you are doing this module to help you later on when troubleshooting massbus devices. There are some new concepts that you may or may not be familiar within signal transmission. (Depending on your own background). We will get into tri-state logic devices, dual differential line-driving and other such sundry points, so...Pay Attention!

MASSBUS CABLES

Functionally, the interfacing between the RH-11 and a representing device consists of 3 40 - pin BCO6-R cables with 3-M BERG-type connectors at the ends. They come in various lengths to accommodate the varied peripheral devices. On any one system there may be a maximum cable length of 120 feet from the RH-11 to the last device on the bus. A typical installation is illustrated below using the RS04 as an example:



EXAMPLE RP04 CABLING

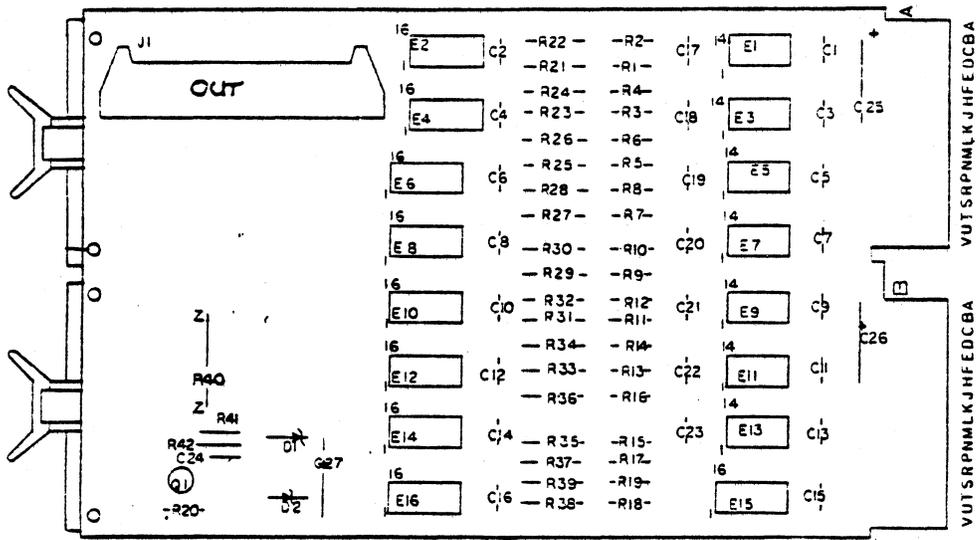


All commands discussed in earlier modules are sent on the three cables and routed by way of M5904 massbus transceiver modules. (One per cable). These cables plug directly into connectors mounted on the modules themselves. (see illustrations, next page).

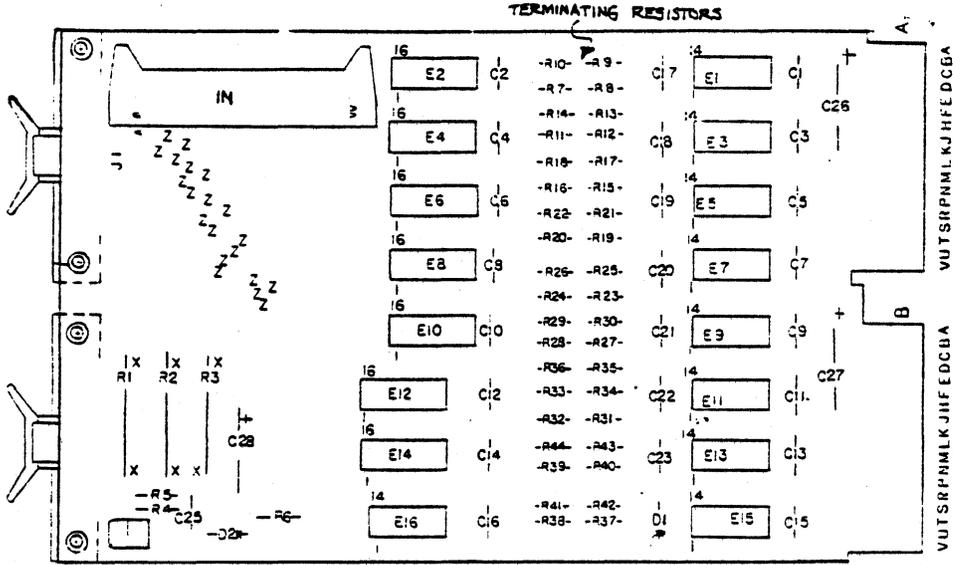
At the other end of the cables we find two varieties of M5903 device transceivers (makes no difference what the peripheral is). The M5903-YA was designed to automatically terminate the massbus. Note the lack of an "out" connector and the presence of terminating resistors. This board would be placed in the last device on the massbus along with two more for the other cables. Preceding drives would have the M5903-YA's. There is a special "mini-terminator" called an H870 that now sits in the "out" cable connector of the last device's M5903 to terminate the bus.

Earlier designed M5903's also did not have switch S1 (shown in the lower left hand corner of the module). This switch gives you the capability of troubleshooting the massbus devices in the event of a "hung" device preventing massbus communications. In the UNIBUS world you would be pulling Unibus cables and moving the terminator to determine the faulty device that is "hanging" the processor. In massbus-land those types of problems can be troubleshot with the flick of switch S1 (on all 3 modules). The device is now non-existent with reference to the other devices on the massbus. This is due to the fact that the driver chips used on these transceivers are of a TRI-STATE variety. 75113's output hi's and lo's and also offer a hi-impedance "open" state to a bus.

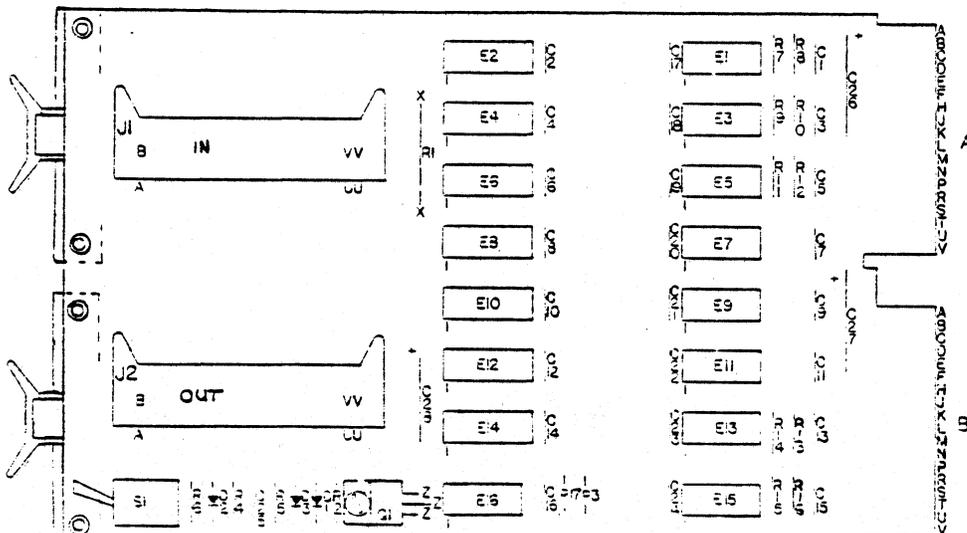
M5904



M5903 YA



M5903

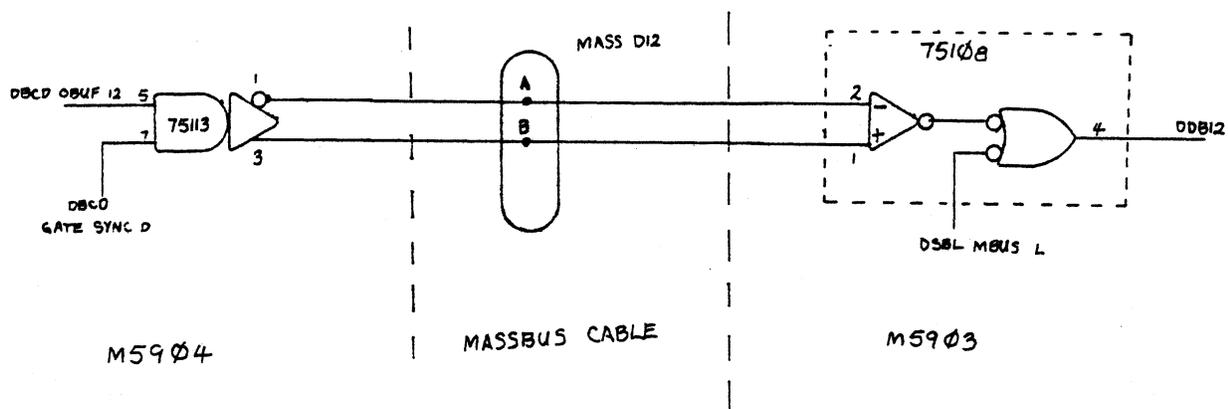


When in this third state, as I have said, it appears to be not there. There are 3 ways in which it can be brought to this state. One way is to remove power to the device it is in. The second way is to use the switch. It removes the power to the chips only on that module. The third way is to remove the logic gating term that enables it. Examples are to follow.

These tri-state 75113's are matched with 75107B's or 75108's as receivers. Signal transmission between the two is of a balanced-line differential driving type.

This simply means that a pair of wires will be utilized to send one logic bit along the cable. This is done to keep noise from being induced as sometimes happens on the Unibus. The two wires tend to cancel any noise spikes. With this dual-differential line driving system, it is possible to have longer cables. As I have already mentioned the maximum length determined by the engineers is 120 feet.

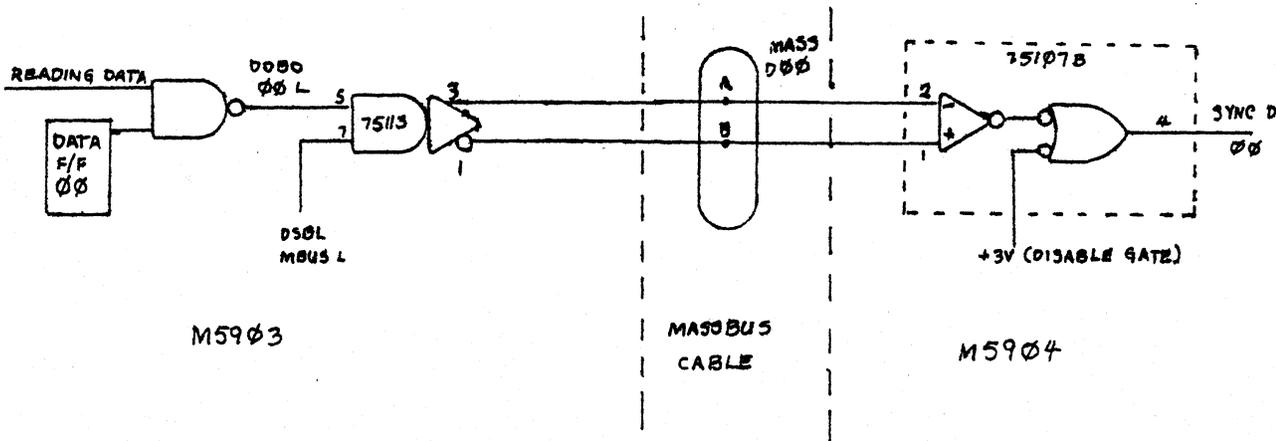
The method of operation is simple: the receivers are designed to "look" for a phase-difference between the two wires in order to decode logic ones and zeros.



To send data from RH-11 to device, the driver (75113) must be gated with a high. What better signal to use in gating the data, or synchronous, bus than "Gate Sync D H?" If this signal is present and the data (Pin 5) is a logical "one", then Pin 1 goes "Lo" and Pin 3 goes "Hi". At the device, the 75108 receiver chip requires a more positive signal at Pin 1 than at Pin 2 in order to output a "Hi" at Pin 4. This is providing of course the "Disable Gate" is not asserted. The end result of all this was that a high sent at the RH-11 turned into a high at the device. In the middle were a pair of wires that had a particular phase difference.

Let us take the opposite condition now. The signal to be sent (OBUF 12) is now lo, representing the logical "zero". Pin 1 now goes "Hi" and Pin 3 goes "Lo". The receiver at the other end of the cable now sees Pin 1 as LESS POSITIVE than Pin 2. The result? A Lo at Pin 4. Or "a zero to be sent = a zero out of the receiver." Even though Confucius did not say that it is still a good thing to remember.

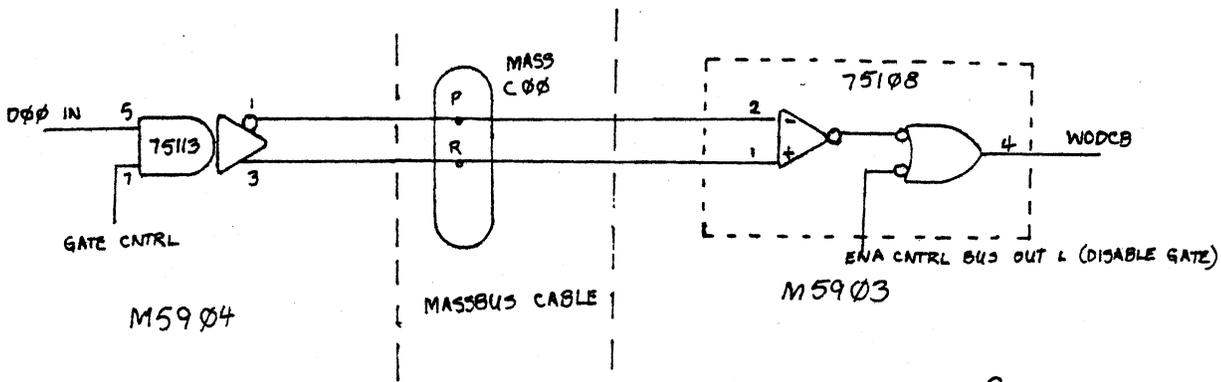
Let us now look at the rest of the ways signals transverse the Massbus. The first example was that of the RH-11 sending data to the device. Be sure you understand that completely before continuing on with the second example which is that of a device sending data to the RH-11:



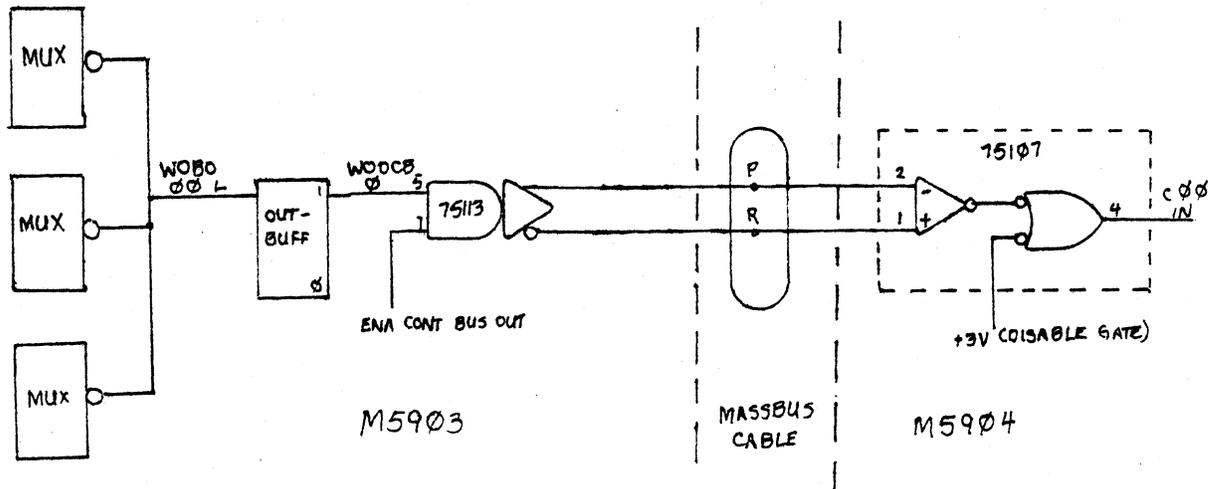
Notice in this example the bubbled output of the driver feeds the opposite input of the receiver. No matter....Keep in mind the axiom stated in the first example: The receiver requires a more positive signal at pin 1 than at pin 2 to decode the fact that a logical "one" was sent.

In the example, the input is labeled "DDBO 00L." That, however is the result of signal inversion through a gate. A "one" out of the data F/F is still received as a "one" in the receiver because of the axiom.

These examples so far are with the Data Bus. Does the Control Bus operate the same way? Let us see:



AND THE OTHER DIRECTION ON THE CONTROL BUS ?



Yes! (after a few signal inversions) Data to be transferred is contained in the multiplexors and is sent over a wired - or bus (assertions would then be low true). The output buffer would then accumulate the information and relay it to the drivers.

Data transmitted from device to RH-11 over the control bus then, goes through much the same type of signal inversion process as did the data bus.

The whole purpose of showing you these was to make it easier for you to interpret signal transmissions that occur on the mass bus.

Overall it looks pretty confusing, but look at it only one point at a time.

The "point" now is the operation of the drivers and receivers and the consequent voltage levels that should appear on the bus.

No matter what the signal names are that surround the gates, if the input to the driver is high, then the non-bubbled output of the driver goes HI and the bubbled output goes LO. ALWAYS!

In the case of the last example, the signal to be transmitted to the RH-11 is stored in inverting multiplexors. H \longrightarrow L. The output buffer F/F monitoring that bit would not set and consequently would send a LO to the input to the driver.

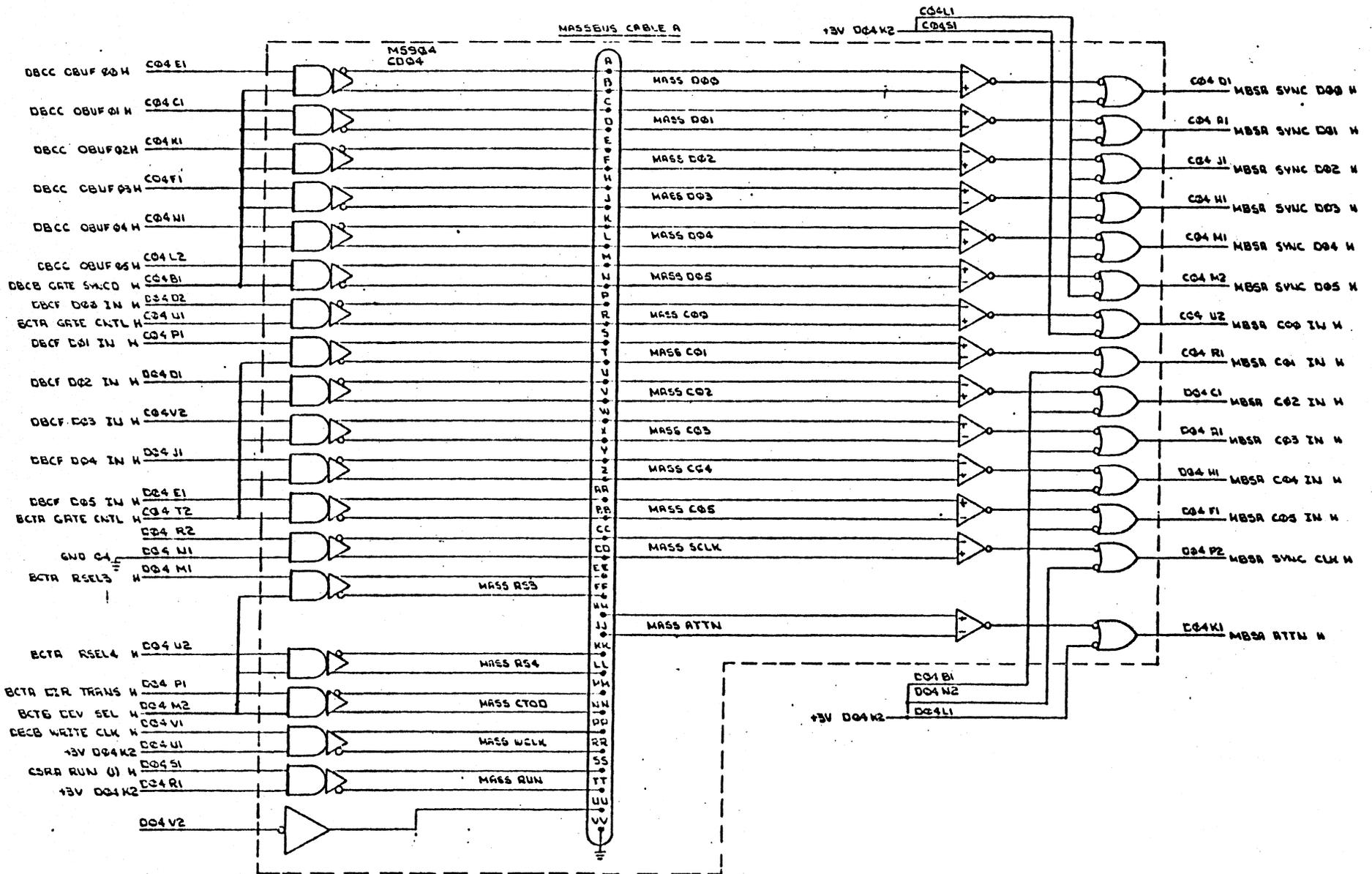
These diagrams are for examples. The actual engineering drawing looks a little different. Each drawing will represent a transceiver module (M5904 or M5903). The 75113 tri-state drivers are on the left and the 75101 receivers are shown on the right. The cable of course is in the center. To send a signal from controller to drive, a 75113 is enabled and drives a balanced line output to the cable where you following all this, leave this drawing and dig out the M5903 drawing, and come in to that page in the center (via the cable) and go to the right to the appropriate receiver.

ADDITIONAL RESOURCES:

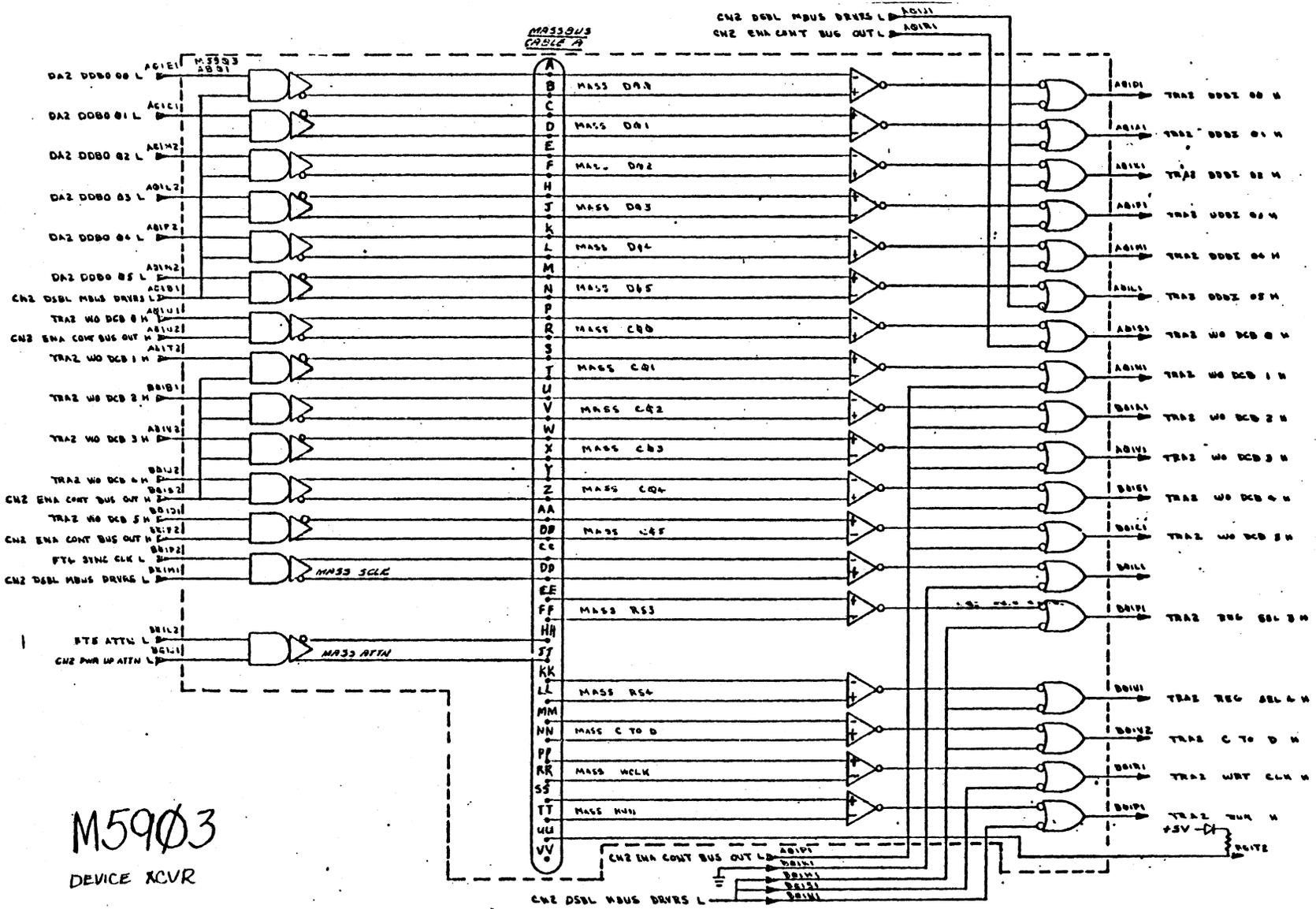
RJS04 Maintenance Manual pages 2-4, and 2-5 paragraph 2.5
5-21 paragraph 5.21
5-35 paragraph 5.27

RJP04 Maintenance Manual pages 2-5, paragraph 2.7
6-31, paragraph 6.21
6-35, paragraph 6.27

TJUL6 Maintenance Manual pages 2-4, paragraph 2.5
6-31, paragraph 6.21
6-35, paragraph 6.27



M5904 RH-II XCVR



M5903
DEVICE RCVR

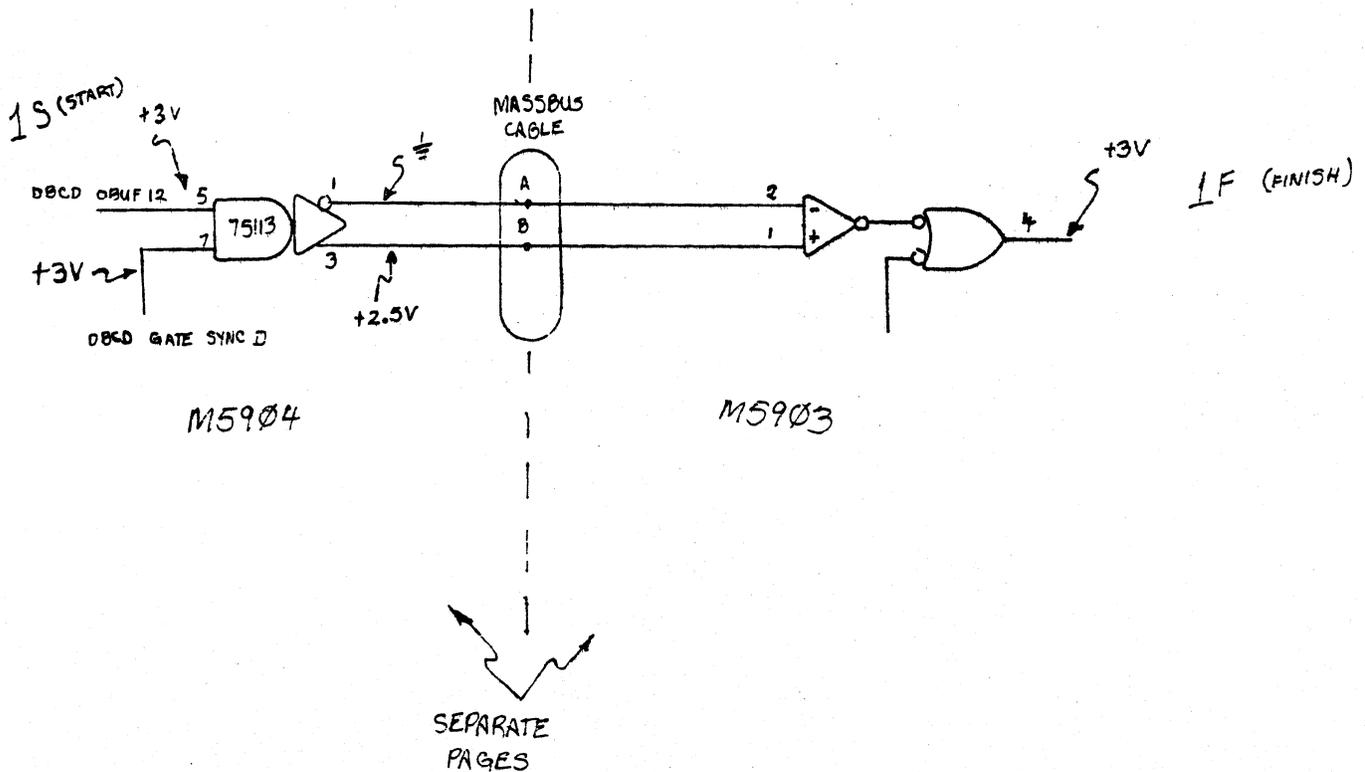
MASSBUS CABLES CRITERION EXAM

Using the attached Massbus transceiver logic diagrams for a massbus and the RH-11, trace the following signals through the diagrams:

1. FT5 ATTN L
2. DA2 DDBØ Ø3L
3. BCTA RSEL 3 H
4. DBCF DØ3 IN H

Label the attached diagrams with the following information:

- A. The starting point with a 1S for ATTN, 2S for DDBØ Ø3L etc.
- B. All voltages on the appropriate lines.
- C. The finish at the receiver output with a 1F for ATTN, 2F for DDBØ Ø3L etc.



RH-11
INSTALLATION

OBJECTIVES:

- I. Given the installation procedures for the RH-11 and the component layout diagrams for the M9300 UNIBUS "B" terminator, the M7295 Bus Control Module and the M7294 data buffer module, draw in the appropriate jumpers as if to install these boards in a pre-configured system with 100% accuracy.

- II. Given the installation procedure for the RH-11 answer basic questions relating to the installation such as cable, location, board placement, etc.

In this lesson you are going to see what is involved with installing one of these RH-11's into an existing system. The first item we will need is the appropriate RH-11 maintenance manual. You might have noticed while doing the previous learning modules, that the titles of your respective manuals were that of the device name with a "J" added. This is the sub system name for the RH-11 controller plus one device. If you were ordering one you could specify "RH-11" and that's all you would get. Likewise you would order an RP04, and that's what you would receive. But if you ordered a TJU16, you would receive one RH-11, one TU16, MAG tape transport, and one TM02 master "RH-to-TU" interface.

This means that the manual is custom tailored for your needs with a particular sub-system instead of writing a generalized manual to try and handle all the device needs.

So...with this in mind, open up your XJXX XXXX system maintenance manuals to the chapter that says:

INSTALLATION AND MAINTENANCE.

Read over the procedures listed in the chapter up to the paragraph describing the small peripheral controller slots. Here there is a change. These slots are not recommended for use anymore as they have a tendency to put too much of a drain on the +5V - Regulators in the system box. Do ensure the grant continuity cards are in however, (and, right-side up!)

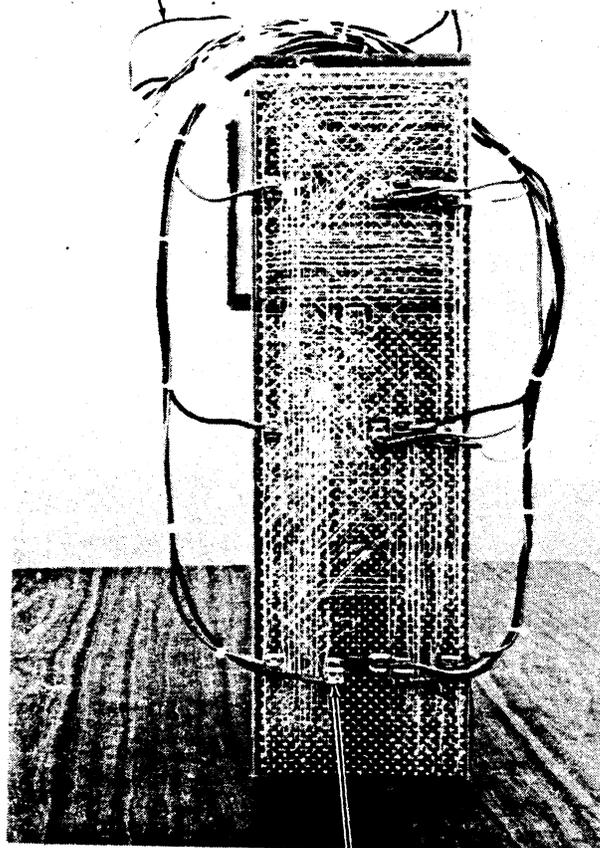
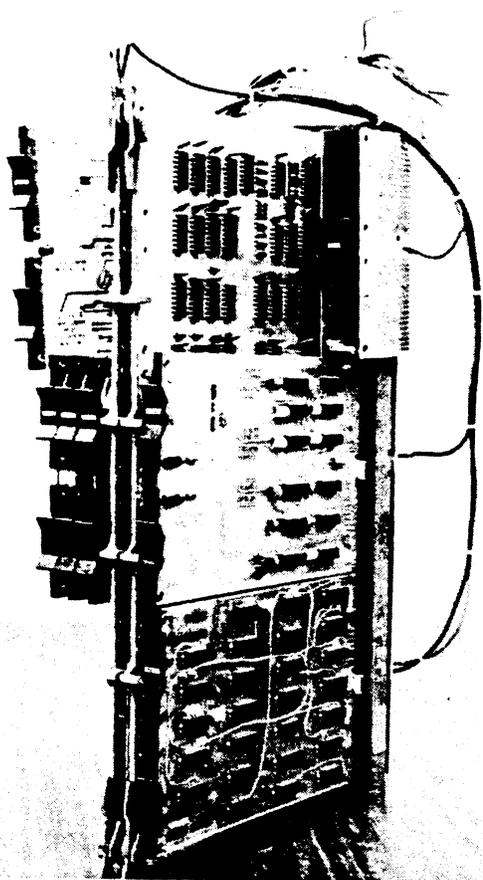
That's all we can show you here until you actually go in and install one yourself. In person! Neatness will count here as there are close tolerances inside these expander boxes (CPU Boxes as well) between the backplane and the system power supplies. Those power cables must be NEATLY dressed back with cable ties. All push-on lugs must have plastic wire protectors on them also. The incoming voltages must be right on (especially the -15V for the silo chips).

Once you complete the criterion exam portion of this module, you can see by the course map that there are no more modules to do. No adjustments to perform, no diagnostics to run, (not until you take a specific MASSBUS peripheral) only a visual check-out of the jumpering and card placement. Two of these cards contain the bulk of the logic. (M7294 and M7295). Basically speaking, one is for register control while the other is data control This only leaves the module that handles MASSBUS parity, the module that comprises the control and status register, and the 3 transceivers plus cables.

With a little bit of thought in what this device does, section by section, you should be able to isolate problems to a module to do some substitution.

TWO POWER
DISTRIBUTION CABLES

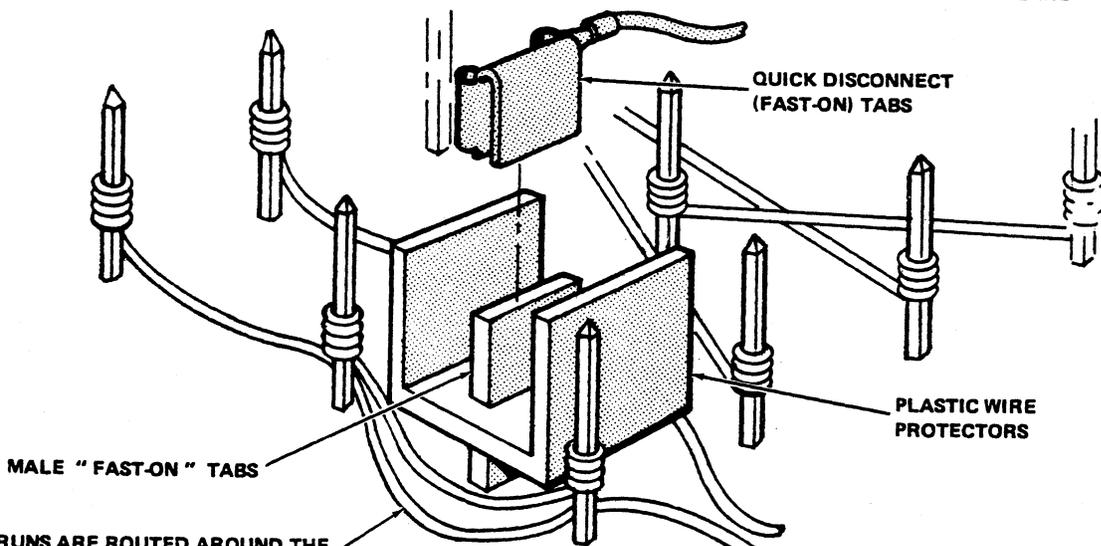
MATE-N-LOCK
CONNECTORS



THE RH-11 ASSEMBLY

QUICK-DISCONNECT (FAST-ON) TABS

BACKPLANE



MALE "FAST-ON" TABS

QUICK DISCONNECT
(FAST-ON) TABS

PLASTIC WIRE
PROTECTORS

WIRE RUNS ARE ROUTED AROUND THE
WIRE PROTECTORS TO KEEP THE "FAST-ON" TABS
FROM PINCHING THEM.

INSTALLATION CRITERION TEST

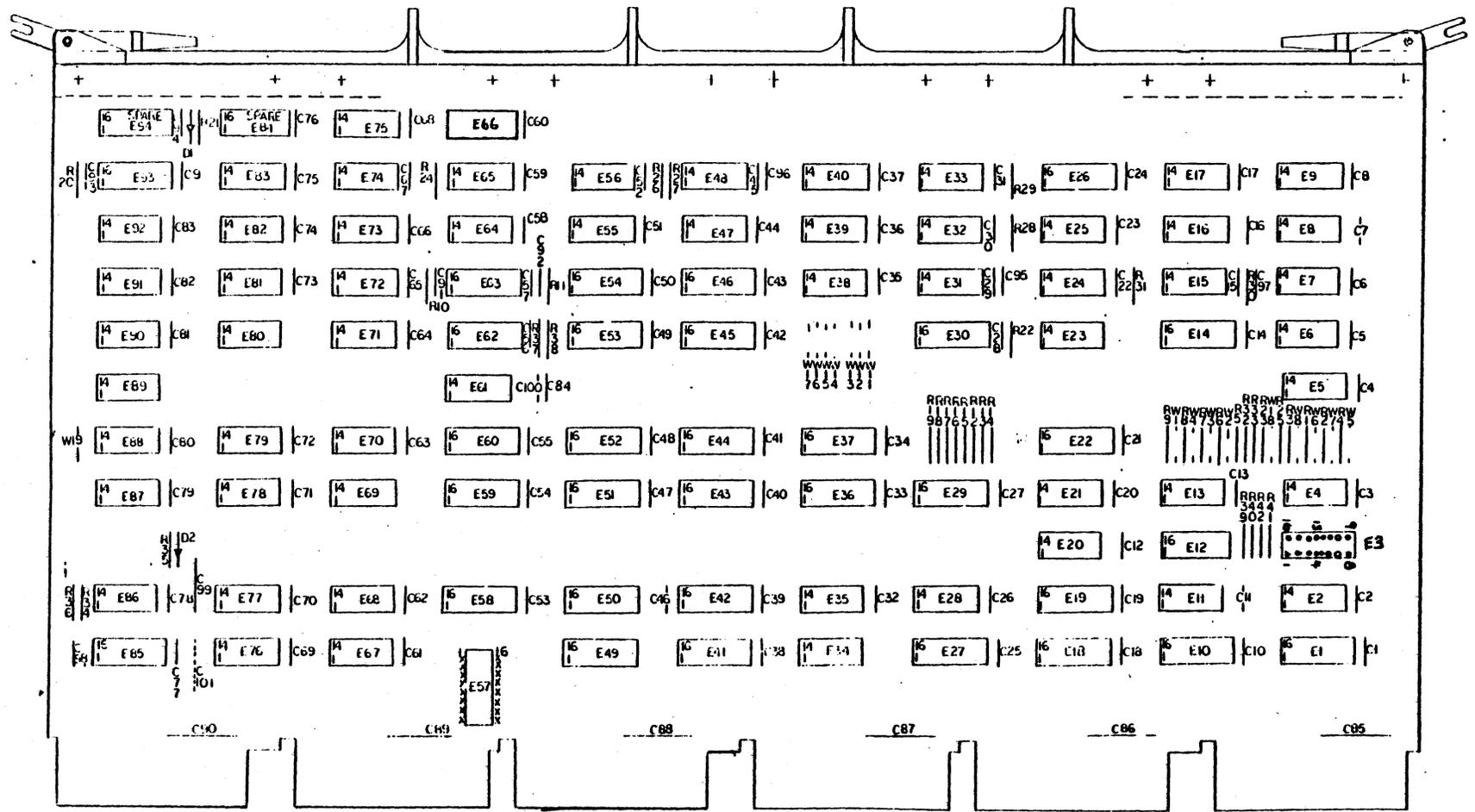
- I. Using the installation chapter in your RH manual and the available module layouts, draw in all the jumpers necessary to represent these modules working in the representative system below:

An 11/45 with Bi-polar memory, to be used on unibus "B", the RH-11 must be installed by itself in a separate expander box, and the processor has no NPR latency feature installed.

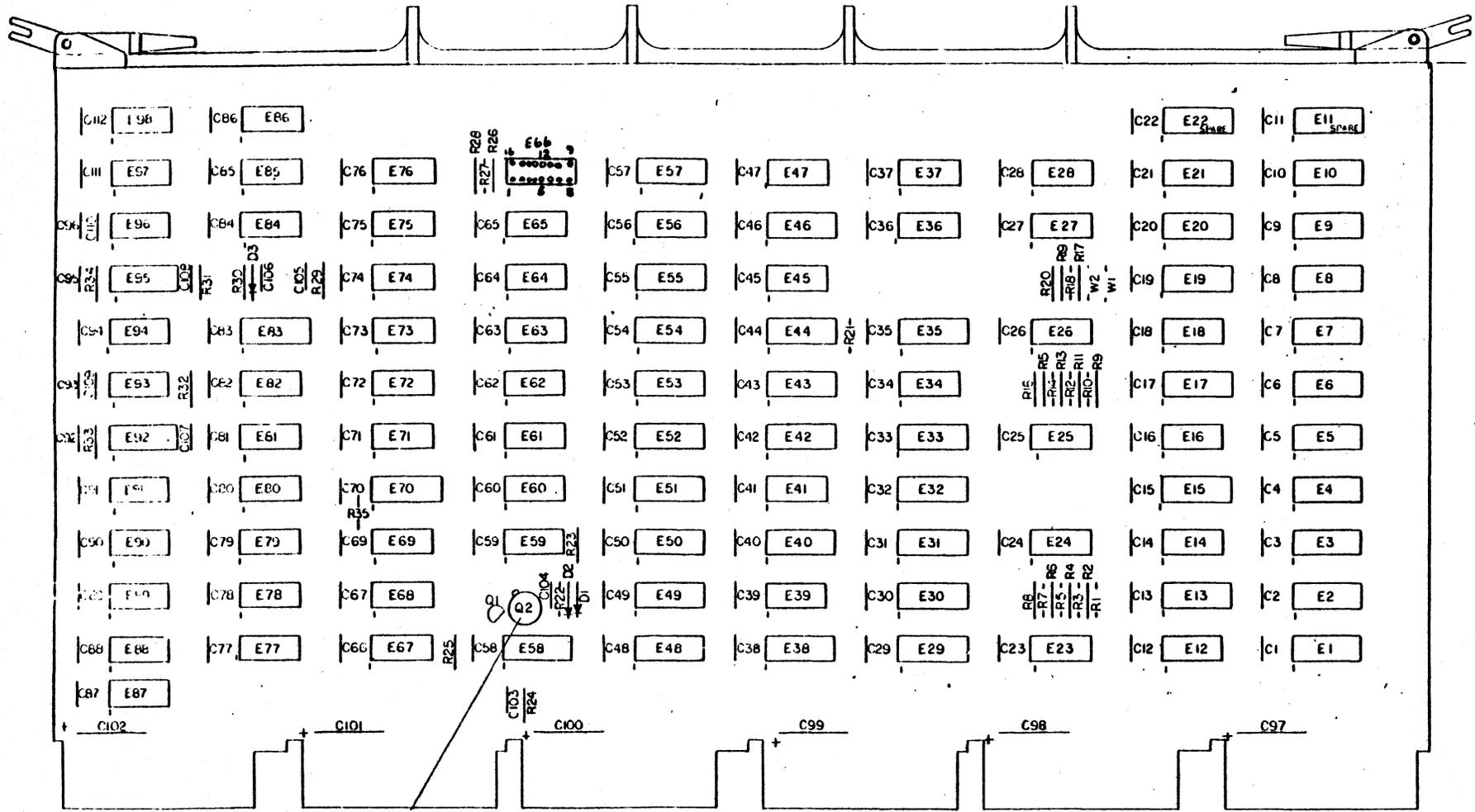
- II. Answer the following questions about the installation of this RH-11:

- A. What must be done with the power fail drivers?
- B. Looking at the modules as installed in the backplane, is the 7294 module to the left or right of the 7295?
- C. What determines which way the MASSBUS cables go into their connectors?

M7295
 BUS CONTROL
 MODULE



M7294
 DATA BUFFER
 (SILO) MODULE



M9300
 UNIBUS 'B'
 TERMINATOR
 BOARD

