PRELIMINARY SPECIFICATION

1100/PDP-8 INTERFACE

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1. INTRODUCTION

The Digi-Data PDP-8 interface is designed to provide plug-to-plug compatible read/write magnetic tape drives for the PDP-8 family of computers, using the MINIDEK line of reader/recorders with formatting electronics.

From one to four MINIDEK transports may be operated, under program control, with this single interface card.

2. ELECTRICAL INTERFACE

The interface conforms to all electrical interface specifications for the MINIDEK series, and for the PDP-8 positive I/O bus.

3. LOGIC LEVELS

A. Internal

All TTL High True

1 = True = 2.5 to 5.5 Volt

0 = False = 0.0 to 0.4 Volt

B. External

All TTL/DTL compatible defined by interface specifications for PDP-8 positive I/O bus and MINIDEK bus.

4. PHYSICAL AND ENVIRONMENTAL

The interface consists of a single printed-circuit card with dimensions identical to the cards within the 1100 recorder.

Pin allocations for the MINIDEK bus signals are identical to those on the NRZI formatter card.

Pin allocations for the PDP-8 bus shall be chosen to allow simple cabling into the PDP-8.

Plus 5.0 volts regulated and adequate cooling are assumed available in all proposed installations.

5. GENERAL DESCRIPTION

One of four MINIDEK transports may be selected under program control. The interface and formatting electronics are shared by the four transports, and hence only one transport may be performing an operation at any given time. (Rewinding is an exception which will be covered below).

When connected to the PDP-8 external I/O bus, the interface will respond to 2 (two) external device addresses, one for command/status transfers, and one for data transfers. The two addresses to which the interface responds are chosen, at installation time, by jumpers installed on the printed-circuit card.

The only limitation imposed upon the choice of the device addresses is that they be adjacent addresses which are identical in all but the least significant bit, for example:

64	110	100
65	110	101

The following pair of addresses cannot be used:

41	100	001
42	100	010

since they are not identical in all but the least significant bit.

Subject only to this limitation, any pair of addresses may be chosen from 0 through 77 (Octal).

In all cases, the lower of the two addresses, (with the least significant bit a zero), is used for command/status transfers, and the higher address (with the least significant bit a one), is used for data transfers.

In general, data transfers are invalid until the appropriate command transfer (read, write, etc.) has been executed, to initialize tape motion.

6. PROGRAMMING

(Ref. Digital Equipment Corp. "Small Computer Handbook", 1971, Chapter 5, Principles of Programmed I/O Transfers).

MB0	1	2	3	4	5	6	7	8	9	10	MB11
1	1	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

6_8 Specifies I/O Instruction — Device Address — Generate IOT Pulse

In general, if information is to be transferred to or from the peripheral device, the transfer is to or from the accumulator register to or from the device. Thus, on outputs to the device, the information to be transferred must be placed in the accumulator prior to the I/O instruction, and, on inputs, the information transferred will be in the accumulator after the I/O instruction.

Let us assume, for this example, that the addresses chosen for the interface are:

34 (011 100) for command/status transfers
35 (011 101) for data transfers

Let us first examine command/status transfers. All command transfers output the accumulator contents to the interface control logic. The status transfer inputs status information to the accumulator. With the addresses we have chosen, ALL command/status instructions are as follows:

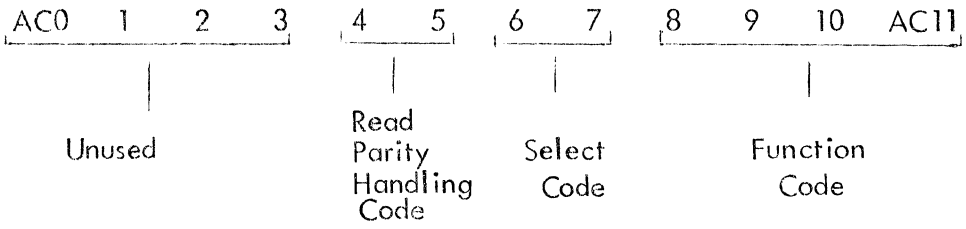
MB0	1	2	3	4	5	6	7	8	9	10	MB11
1	1	0	0	1	1	1	0	0	1	1	1
	6			3			4			7	

6_8 Specifies I/O Instruction — Addresses Control Logic of Interface — Generates Necessary I/O Pulses

This instruction will always serve to transfer the 12-bit contents of the accumulator to the control logic section of the interface. The contents of the accumulator will then be decoded to determine whether the function to be performed is a command for tape action or for status input.

In either case, the appropriate action is taken, and the next sequential instruction skipped, if the command is acceptable under present conditions.

The content of the accumulator, and its significance in command/status transfers, is as follows:



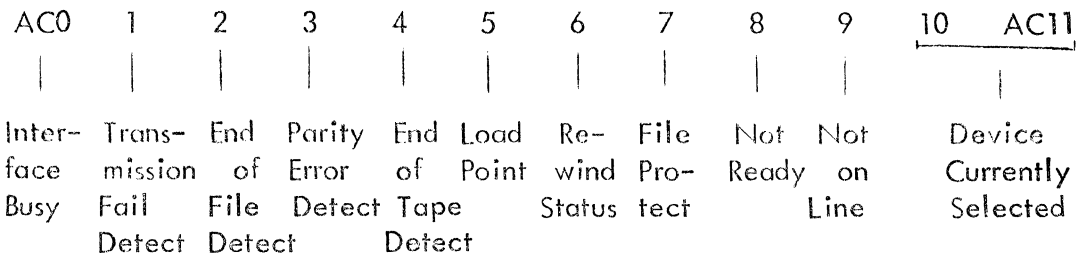
Function Code

The function code informs the control logic what operation is desired. (Clear, write, etc.). Some of the functions are always accepted by the control logic, the operation performed, and the next location skipped. Other functions may be rejected if current conditions prohibit execution of the desired operation. When such rejection occurs, no action is taken, and the next sequential location is not skipped. The program should read status, after such rejection, to determine the cause.

The function codes are listed below:

Octal	Binary	Function
0	0000	Read Status
1	0001	Clear Interface
2	0010	Start Read
3	0011	Start Write
4	0100	Start Write with Extended Gap
5	0101	Skip Forward to next IRG
6	0110	Skip Forward to next file mark
7	0111	Skip Reverse to next IRG
10	1000	Skip Reverse to next file mark
11	1001	Rewind to load point
12	1010	Go offline
13	1011	Write file mark
14	1100	Select one of four transports
15	1101	Skip if transport ready
16	1110	Unused
17	1111	Unused

Function	Description
Read Status	The current content of the status register is transferred to the accumulator. This instruction is always accepted. The status information pertains to the currently selected tape transport. The content of the accumulator, after the execution of the read status instruction, is explained here.



The descriptions above are for a "1" in the bit described.

Clear Interface	All motion, status, and control flip-flops are cleared. The device select bits are unchanged. This instruction is always accepted, and is used primarily for initial clearing, status register clearing, escaping from a faulty transport (one which is off-line, etc.)
Start Read	Initiates forward motion and read operation. The data flag (the flag associated with the data transfer address) will be set when each character is read from the tape, indicating it is being held in the formatter buffer register. When a data transfer I/O instruction is executed, transferring the character into the accumulator, the flag will be cleared. A character arriving from the tape when the flag is still set (from the previous character) will set the transmission fail status bit, as will a data transfer instruction when the flag has not been set. Thus if the computer is early or late a transmission failure is detected.

Start Write	Initiates write operation. The data flag is set immediately to indicate the necessity of supplying the first character to be written. Forward motion does not begin until this character is transferred. As with the read operation, the flag is set and cleared character-by-character, and loss of synchronization will set the transmission fail status bit. However, when the last character to be written has been transferred, the computer stops sending and this absence is detected to generate the inter-record gap. Data sent after this operation begins will be ignored, and will set the transmission fail flip-flop. This instruction will be accepted only when the tape is at rest, on line, and not file protected.
Start Write with Extended Gap	Same as start write except extended gap is written as described in MINIDEK specifications.
Skip Forward to IRG	Reads next record without setting parity error status, transmission fail status, or data flag. Data transfers during skip, which should not be programmed, will result in clearing the accumulator.
Skip Forward to next File Mark	Same as skip to next IRG, except skips to file mark.
Skip Reverse to Next IRG	Same as skip forward to next IRG, except reverse motion not accepted if at load point.
Skip Reverse to next File Mark	Same as skip reverse to next IRG except skips to file mark. All skip commands are accepted only when the tape is on line and at rest.
Rewind to Load Point	Initiates rewind to load point. Accepted only when tape is on line, at rest, and not already at load point.
Go Offline	Places selected transport in off-line mode. Accepted only when tape is at rest and on line.

Write File Mark	Writes file mark. Accepted only when tape is at rest, on line, and not file protected.
Select	Selects one of four transports using select code bits. Not accepted if interface busy status bit set.
Skip if Transport Ready	Skips next instruction if the transport is ready, used to detect block transfer complete.
Select Code	2 bit code to select 1 of 4 transports. These bits are ignored on all commands except the "select" command.
Parity Handling Code	2 bit code to select 1 of 4 modes of parity handling. These bits are ignored on all commands except the "start read" command. The parity handling code is set to zero by a "clear interface" command.

On all reads, the 8 data bits are transferred into accumulator bits 4 through 11, with the least significant data bit in accumulator bit 11.

The four combinations of the parity handling code, and their significance, is as follows:

00	Transfers zeroes to accumulator bit 3.
01	Transfers computed read parity to accumulator bit 3.
10	Transfers parity error to accumulator bit 3. (Only characters with incorrect parity will have a "one" in bit 3.)
11	Transfers parity error detect status bit to accumulator bit 3. (First character with incorrect parity, and all succeeding characters, regardless of parity, have a "one" in accumulator bit 3.

Now let us examine device transfers. There are two instructions to the device. Assuming the addresses we have chosen, they are:

Skip if data flag on

MB0	1	2	3	4	5	6	7	8	9	10	MB11
1	1	0	0	1	1	1	0	1	0	0	1

6_8 Specifies 1/0 Instruction

Addresses Device

Specifies Skip if Data Flag on

Transfer data

MB0	1	2	3	4	5	6	7	8	9	10	MB11
1	1	0	0	1	1	1	0	1	1	1	0

6_8 Specifies 1/0 Instruction

Addresses Device

Specifies Transfer Data