CIR 10/70

CONTINUOUS

INTERFACE REQUIREMENTS

DSR 1300, 1400 & 1500 SERIES

INPUTS

IC COMPATIBLE (STANDARD) Typical driver for T^2L is SN 7401 with 1.5k to +5VDC. For DTL any element with 2k output to +5VDC.

Logic Ø = -0.5 VDC to +0.5 VDC, less than 10 ua sink

Logic 1 = +3.0 VDC to +6.0 VDC, into nominal 3.0k ohm impedance to ground

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DATA	(6 lines - 7/track) (8 lines - 9/track)	Positive level, coincident with or spanning record command, to record NRZI "one"
RECORD		50 usec to 100 usec positive pulse records input data on tape. Maximum 10 usec after slew clock
PARITY SELECT (7/track)		Zero level to write odd parity, positive level to write even parity
INITIATE IRG		Minimum 50 usec to 100 usec positive pulse, writes (CRCC, 9/track and) LRCC on tape at four character spaces (and 8 character spaces, 9/track), inserts minimum .75 inches (.55 inches, 9/track) erased tape gap, must be coincident with last record command
REMOTE EOF		Minimum 150 usec to 200 usec positive pulse, minimum 900 msec between actuations; generates internal IRG routine, then writes tape mark and generates second internal IRG routine
REMOTE REWIND		Positive level maintains rewind, zero level terminates (1400) Positive pulse starts rewind, BOT internally stops. Positive level causes rewind past BOT. Use EOT to reset level. (1300 & 1500) (4.7k impedance both options)
POWER		105-125 VAC, 50-60 Hz
*REVERSE COMMAND		Positive level to enable synchronous reverse tape motion, zero level to enable synchronous forward tape motion
RUN/STOP		Positive level causes recorder to move tape (subject to status of REVERSE COMMAND input), zero level halts tape motion. In Record mode, stop can be commanded coincident with IRG command. The tape will stop after completing compatible gap space
* WRITE DISABLE		Positive level disables record process

OUTPUTS

IC COMPATIBLE (STANDARD)

Logic Ø = Maximum +0.5 VDC, 10 ma sink capability

Logic 1 = Nominal +5.0 VDC, 600 ohm source impedance (consult factory for other levels)

GAP IN PROCESS	Positive level during gap insertion
BOT SIGNAL	Nominal 2 msec positive pulse occurring when trailing edge of BOT reflective marker is sensed (bi-directional)
EOT SIGNAL	Positive level for duration EOT reflective marker is sensed (bi-directional)
BROKEN TAPE	Positive level when tape improperly loaded
DC POWER	+12VDC (2 pct regulation), -7 VDC (10 pct regulation), DC common (consult factory for available power)
HCEC ODD PARITY ERROR (optional)	Positive level, nominally 50 usec after record command, only if character being recorded on tape is even parity, output maintained until subsequent record command or initiate IRG, zero output when character is odd parity, and during IRG; positive level if head voltage fails or the unit is operated in rewind or read modes
HCEC EVEN PARITY ERROR (optional)	Positive level, nominally 50 usec after record command, only if character being recorded on tape is odd parity, output maintained until subsequent record command or initiate IRG. Zero output when character is even parity and during IRG; positive level if head voltage fails or the unit is operated in rewind or read modes
SLEW CLOCK	Nominal 50 usec positive pulse occurring at slew rate of recorder, first clock nominally 30 msec after initiating slew operation from halt, zero output during IRG, reverse operation, EOF routine, BOT routine & READ mode (Write Disable)
*DATA (6 lines + parity, 7/track) (8 lines + parity, 9/track)	10 usec positive pulse, coincident with clock, when bit is present, de-skewed
*READ CLOCK	Nominal 10 usec positive pulse
*READ EVEN PARITY	Nominal 10 usec positive pulse, coincident with clock; only occurs when character parity is even
*READ ODD PARITY	Nominal 10 usec positive pulse, coincident with clock; only occurs when character parity is odd

*Standard features with read option

Rack Model - MS3102A-28-21P (Amphenol or Equivalent)

Portable Model - DC-37S (Cinch-Jones or Equivalent)

A	1	RECORD
B	2	STEP (Incremental)
C	3	INITIATE IR GAP
D	4	Not used
E	5	PARITY SELECT (See Note 3)
F	6	DATA BIT 1 (LSB)
G	7	2
H	8	4
J	9	8
K	10	A
L	11	DATA BIT B(MSB)
M	12	REMOTE START (Incremental)
N	13	REMOTE STOP (Incremental)
P	14	REMOTE REWIND
R	15	HCEC ODD PARITY ERROR (optional)
S	16	HCEC EVEN PARITY ERROR (optional)
T	17	IR GAP IN PROCESS
U	18	EOT SIGNAL
V	19	BOT SIGNAL
W	20	SLEW CLOCK (optional Incremental)
X	21	REMOTE EOF
Z	22	OVERFLOW (Incremental Buffer)
a	23	READY (Incremental Buffer)
b	24	ERROR (Incremental Buffer)
c	25	
d	26	
e	27	
f	28	
g	29	-7VDC
h	30	BROKEN TAPE
j	31	SLEW COMMAND (optional, Incremental), RUN/STOP (Continuous)
k	32	
m	33	See note 2
n	34	+12VDC
p	35	DC COMMON
r	36	AC COM (optional)
s	37	SWITCHED AC LINE (optional)

7 Track

9 Track

DATA BIT 7 (LSB)

6

5

4

3

2

1

DATA BIT 0 (MSB)

NOTES:

1. Mating connectors supplied
2. Pin 33 of portable unit tied to chassis
3. Wire to +12V for Even Parity, DC Com for Odd)

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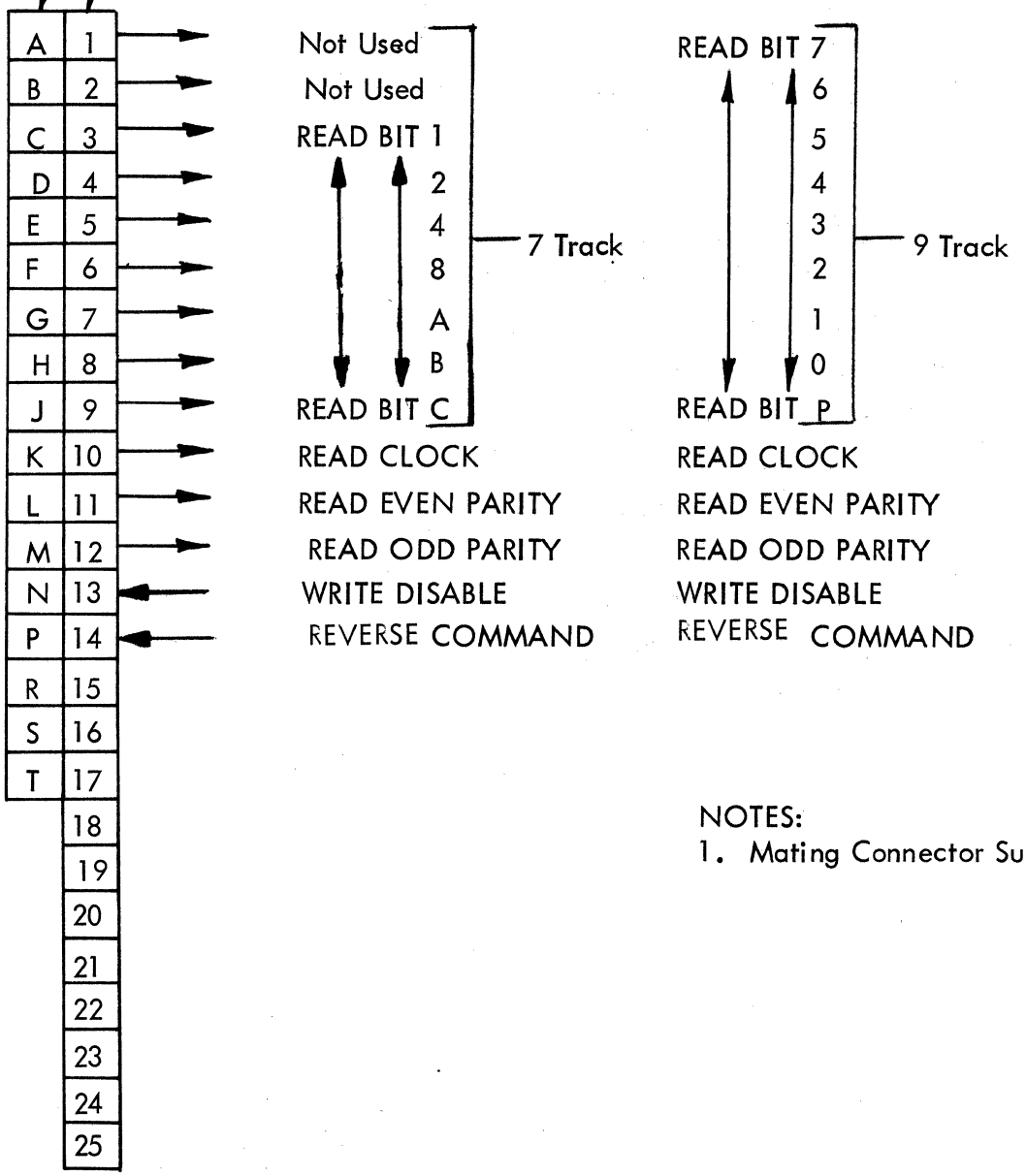
LA-0102

CONNECTOR PIN ASSIGNMENT

MS3102-20-29P (Amphenol or Equivalent) - Rack Model

DC-25S (Cinch-Jones or Equivalent) - Portable Model



NOTES:
1. Mating Connector Supplied

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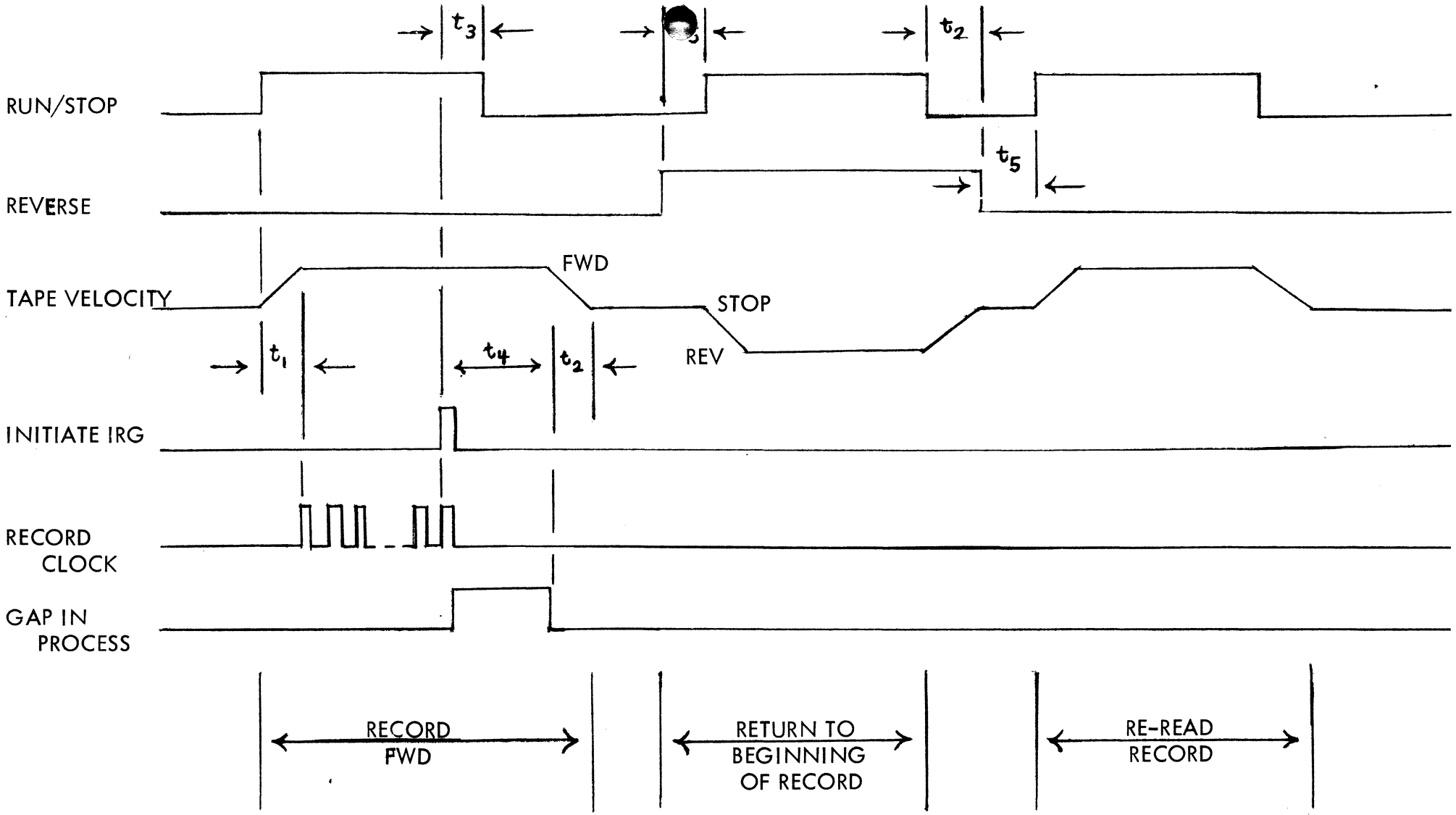
PIN ASSIGNMENT, READBACK
CONNECTOR J-15



$t_1 \approx$ 30 m sec

$t_2 \approx$ 30 m sec

$\emptyset < t_3 < t_4$

$t_4 =$ f (tape speed & density)

$t_5 =$ 50 msec

DIGI-DATA CORPORATION

BASIC TIMING DIAGRAM
SLEW READ/WRITE
October, 1970