IR 10/70

INCREMENTAL
INTERFACE REQUIREMENTS
DSR 1300, 1400, & 1500 SERIES

INPUTS

IC COMPATIBLE (STANDARD) Typical driver for T^2L is SN 7401 with 1.5k to +5VDC. For DTL any element with 2k output to +5VDC.

Logic Ø = -5.0 VDC to +0.5 VDC, less than 10 ua sink

Logic 1 = +3.0 VDC to +6.0 VDC, into nominal 3.0k ohm impedance to ground

HIGH LEVEL (OPTION)

Logic Ø = -0.5 VDC to +0.5 VDC, less than 10 ua sink

Logic 1 = +6.0 VDC to +18.0 VDC, into nominal 15k ohm impedance to ground

DATA (6 lines - 7/track) (8 lines - 9/track)	Positive level, coincident with or spanning record command, to record NRZI "one". Zero level during IRG sequence.
RECORD	Minimum 50 usec positive pulse, return to zero minimum 50 usec before reactuation, records input data on tape
STEP	Minimum 50 usec positive pulse, return to zero minimum 750 usec before reactuation, increments tape one character space (4.7k impedance both options)
PARITY SELECT (7/Track)	Zero level to write odd parity, positive level to write even parity
INITIATE IRG	Minimum 50 usec positive pulse, return to zero minimum 2 msec before reactuation, writes CRCC (9/track) and LRCC on tape at four character spaces and 8 character spaces (9/track) respectively, inserts minimum .6 inches (9/track) or .75 inches (7/track) erased tape gap, can be coincident with last step command during incremental operation
REMOTE START	Minimum 50 usec positive pulse, advances tape at slew speed (stops at BOT marker)
REMOTE STOP	Minimum 50 usec positive pulse, stops tape advance when in BOT mode (overrides remote start)
REMOTE EOF	50 usec to 1 msec positive pulse, minimum 750 msec between reactuations; generates internal IRG routine, then writes tape mark and generates second internal IRG routine
REMOTE REWIND	Positive level maintains rewind, zero level terminates (1400) Positive pulse starts rewind, BOT internally stops. Positive level causes rewind past BOT. Use EOT to reset level. (1300) (4.7k impedance both options)
POWER	105-125 VAC, 50-60 Hz
SLEW COMMAND (optional)	Minimum 50 usec positive pulse, causes recorder to advance tape in slew mode, positive level at end of IRG insertion causes recorder to continue in slew mode while zero level will cause the recorder to halt (See Application Note)
* REVERSE	Positive level to enable synchronous reverse tape motion, zero level to enable synchronous forward tape motion
*WRITE DISABLE	Positive level disables write

OUTPUTS

IC COMPATIBLE (STANDARD)

Logic Ø = Maximum +0.5 VDC, 10 ma sink capability

Logic 1 = Nominal +5.0 VDC, 600 ohm source impedance (consult factory for other levels)

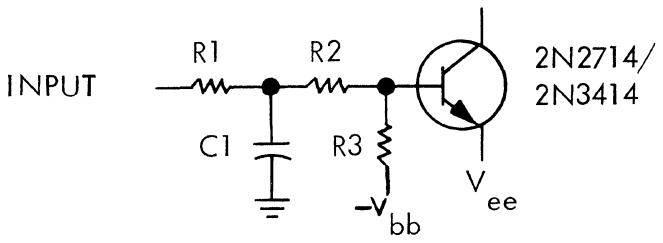
HIGH LEVEL (OPTION)

Logic Ø = Maximum +0.5 VDC, 10 ma sink capability

Logic 1 = +12 VDC, 1.5k ohm source impedance

GAP IN PROCESS	Positive level during gap insertion, starting 3 msec after IRG cmd
BOT SIGNAL	Nominal 2 msec positive pulse occurring when BOT reflective marker is sensed (bi-directional)
EOT SIGNAL	Positive level for duration EOT reflective marker is sensed (bi-directional)
BROKEN TAPE	Positive level when tape not loaded over head
DC POWER	+12VDC (2 pct regulation), -7VDC (10 pct regulation), DC common (consult factory for available power)
HCEC ODD PARITY ERROR	Positive level, nominally 50 usec after record command, only if character being recorded on tape is even parity, output maintained until subsequent record command or initiate IRG, zero output when character is odd parity, and during IRG; positive level if head voltage fails or the unit is operated in rewind or read modes
HCEC EVEN PARITY ERROR	Positive level, nominally 50 usec after record command, only if character being recorded on tape is odd parity, output maintained until subsequent record command or initiate IRG. Zero output when character is even parity and during IRG; positive level if head voltage fails or the unit is operated in rewind or read modes
SLEW CLOCK (optional)	Nominal 50 usec positive pulse occurring at slew rate of recorder (1.0 to 2.5k Hz nominal) first clock approximately 30 msec after initiating slew operation from halt, zero output during IRG
* DATA (6 lines + parity 7/track) (8 lines + parity 9/track)	Nominal 10 usec positive pulse when bit is present, deskewed
* READ CLOCK	Nominal 10 usec positive pulse nominally coincident with data
* READ EVEN PARITY	Nominal 10 usec positive pulse, nominally coincident with data; only occurs when character parity is even
* READ ODD PARITY	Nominal 10 usec positive pulse, nominally coincident with data; only occurs when character parity is odd

* Standard features with read option

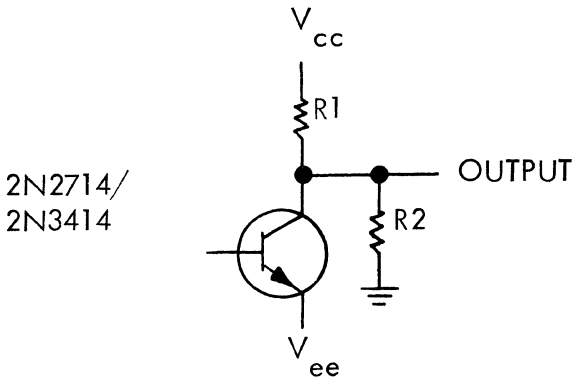


	LOW* LEVEL	HIGH* LEVEL
R1	1.5K	1.5K
R2	1.5K	15K
R3	15K	47K
C1	.001uf	.001 uf

STANDARD INPUT INTERFACE

$0VDC \leq V_{ee} \leq 0.2VDC$

$6.0VDC \leq V_{bb} \leq 8.0VDC$



	LOW* LEVEL	HIGH* LEVEL
R1	1.5K	1.5K
R2	1.0K	—

$0VDC \leq V_{ee} \leq 0.2VDC$

$11.5VDC \leq V_{cc} \leq 12.5VDC$

STANDARD OUTPUT INTERFACE

All resistors 1/4 watt, 5PCT, Metal Film; all capacitors disk ceramic, 10 PCT.
Consult factory for alternate values.

* Low Level - IC Compatible (Standard)
* High Level (Option)

Rack Model - MS3102A-28-21P (Amphenol or Equivalent)

Portable Model - DC-37S (Cinch-Jones or Equivalent)

A	1	RECORD
B	2	STEP
C	3	INITIATE IR GAP
D	4	Not used
E	5	PARITY SELECT (See Note 3)
F	6	DATA BIT 1 (LSB)
G	7	2
H	8	4
J	9	8
K	10	A
L	11	DATA BIT B(MSB)
M	12	REMOTE START
N	13	REMOTE STOP
P	14	REMOTE REWIND
R	15	HCEC ODD PARITY ERROR (optional)
S	16	HCEC EVEN PARITY ERROR (optional)
T	17	IR GAP IN PROCESS
U	18	EOT SIGNAL
V	19	BOT SIGNAL
W	20	SLEW CLOCK (optional)
X	21	REMOTE EOF
Z	22	
a	23	
b	24	
c	25	
d	26	
e	27	
f	28	
g	29	-7VDC
h	30	BROKEN TAPE
j	31	SLEW COMMAND (optional)
k	32	
m	33	See note 2
n	34	+12VDC
p	35	DC COMMON
r	36	AC COM (optional)
s	37	SWITCHED AC LINE (optional)

7 Track

9 Track

DATA BIT 7 (LSB)

6

5

4

3

2

1

DATA BIT 0 (MSB)

NOTES:

1. Mating connectors supplied
2. Pin 33 of portable unit tied to chassis
3. Wire to +12V for Even Parity, DC Com for Odd)

DIGI-DATA CORP.
BLADENSBURG, MD.

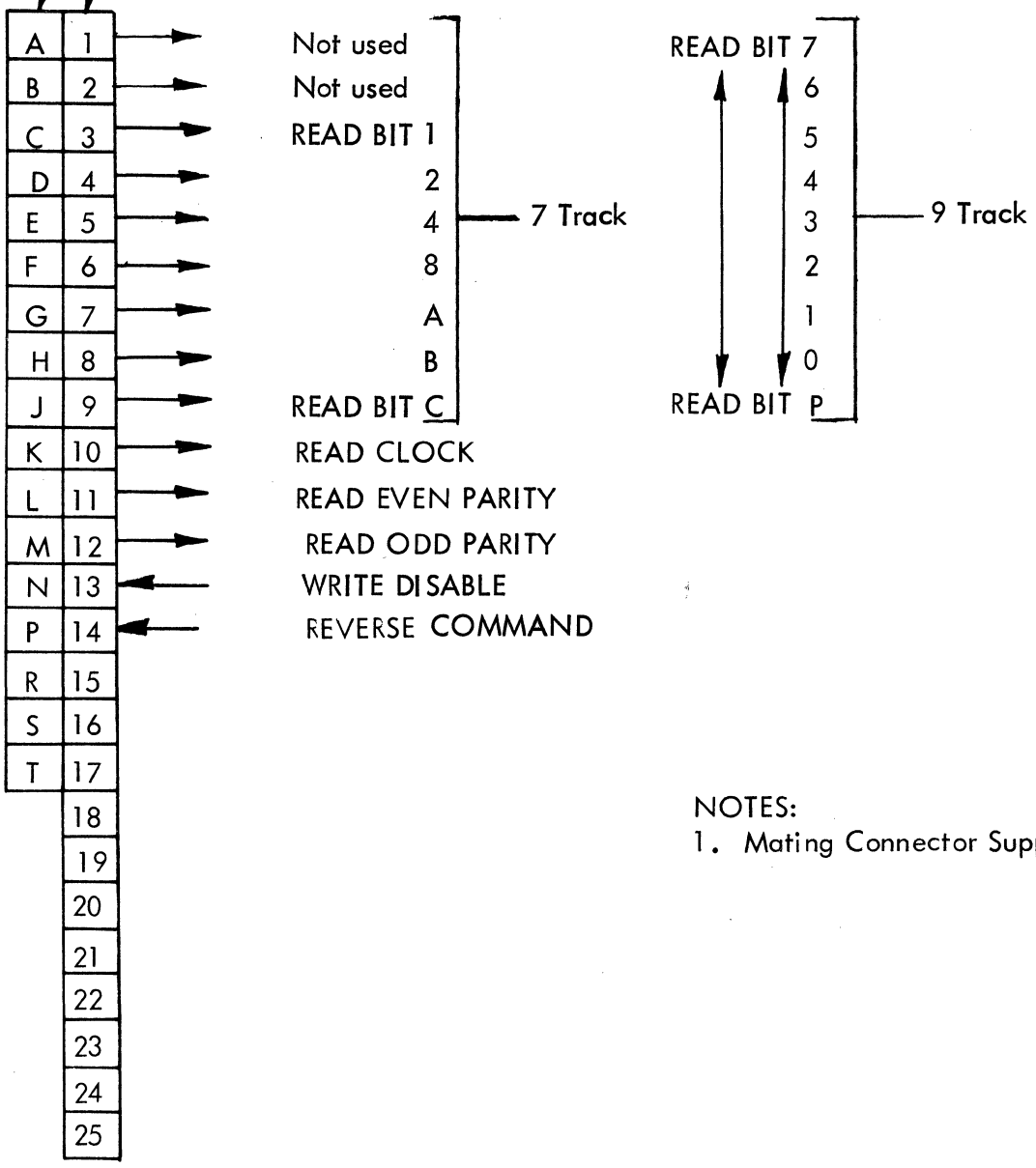
SHEET 1 OF 1 LA-0102 Rev. E

CONNECTOR PIN ASSIGNMENT - J1
(Incremental)

PIN ASSIGNMENT, READBACK
CONNECTOR J-15 (Incremental)

MS3102-20-29P (Amphenol or Equivalent) - Rack Model

DC-25S (Cinch-Jones or Equivalent) - Portable Model



NOTES:
1. Mating Connector Supplied