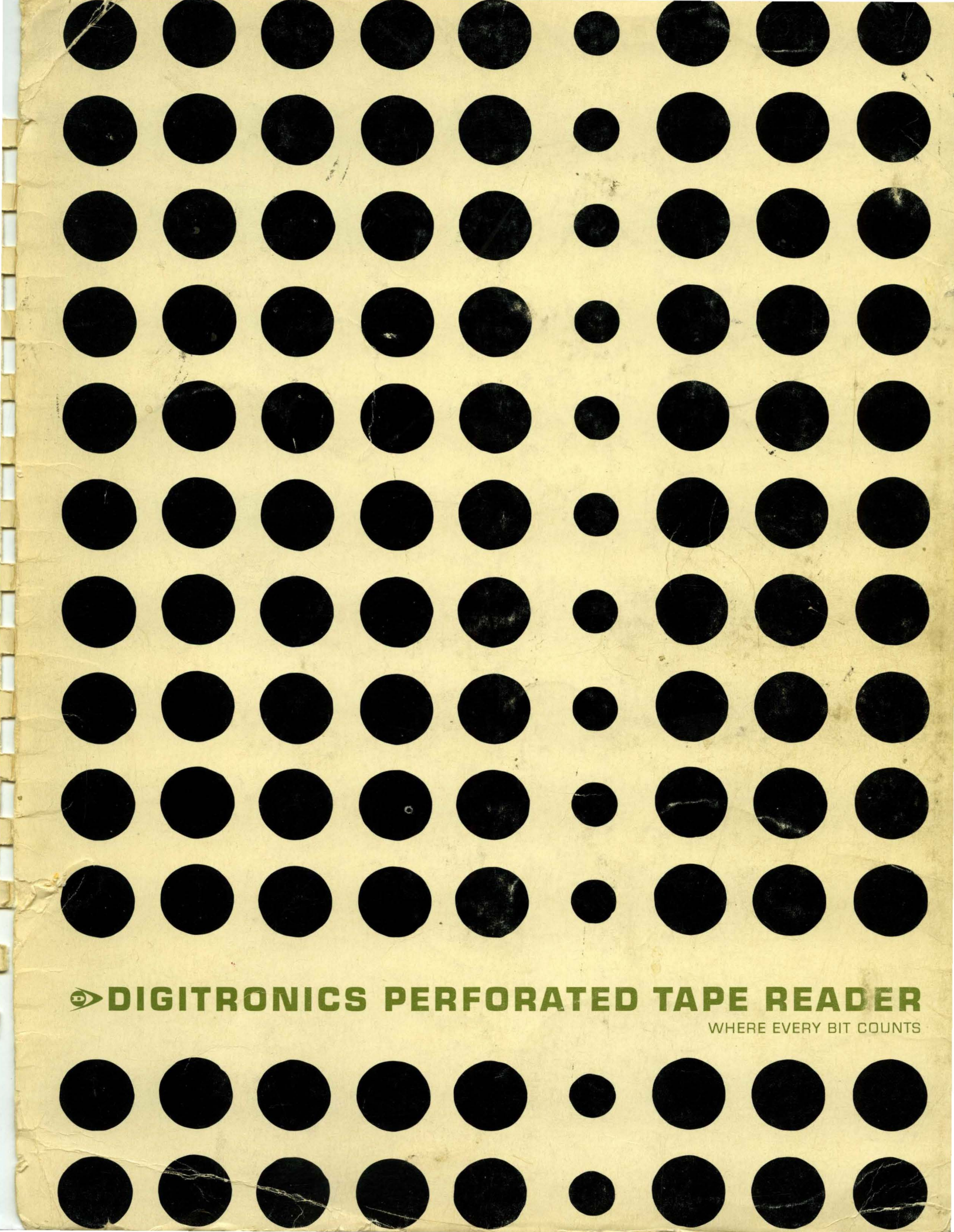
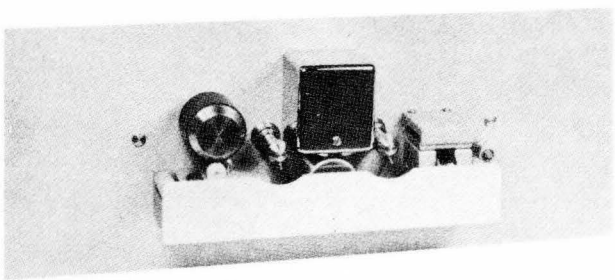


DIGITRONICS PERFORATED TAPE READER

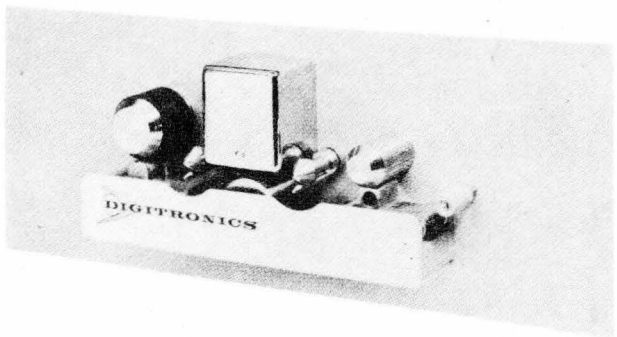
WHERE EVERY BIT COUNTS

PERFORATED TAPE READER

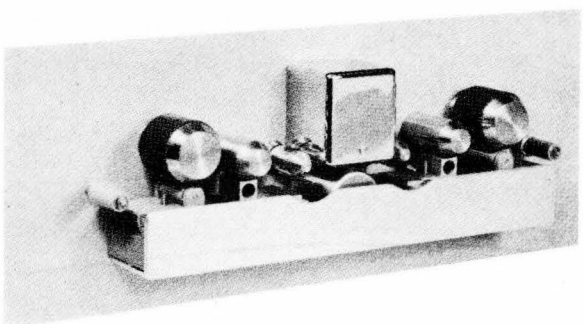
MODELS 3500 AND B3500
SERIAL NUMBER #



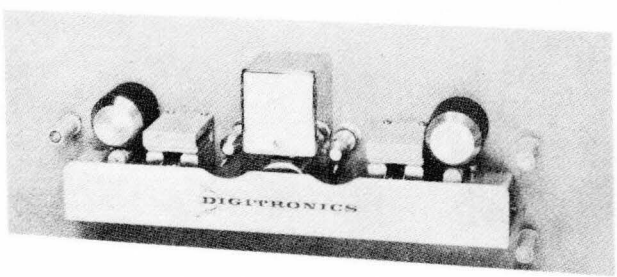
3500 HIGH SPEED BRAKE



3500 STANDARD BRAKE



B3500 STANDARD BRAKE



B3500 HIGH SPEED BRAKE

FEBRUARY, 1963

DIGITRONICS CORP.
ONE ALBERTSON AVENUE • ALBERTSON, NEW YORK • PHONE HT 4-1000

. . . pioneers in data processing technology

PREFACE

This preface will serve to acquaint the customer with information contained in this instruction manual. Immediately following this preface is the Manufacturing Specification (MS) to which this machine was built. The checks in the "CHECK" column of the MS indicate the options selected when the machine was ordered. The MS will indicate the variations particular to this unit. The Theory of Operation Section contains the Theory of Operation for all standard options. Refer only to those portions of the manual applicable to your machine. Special customer options not covered in the manual will be covered by an addendum located behind the MS as required.

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

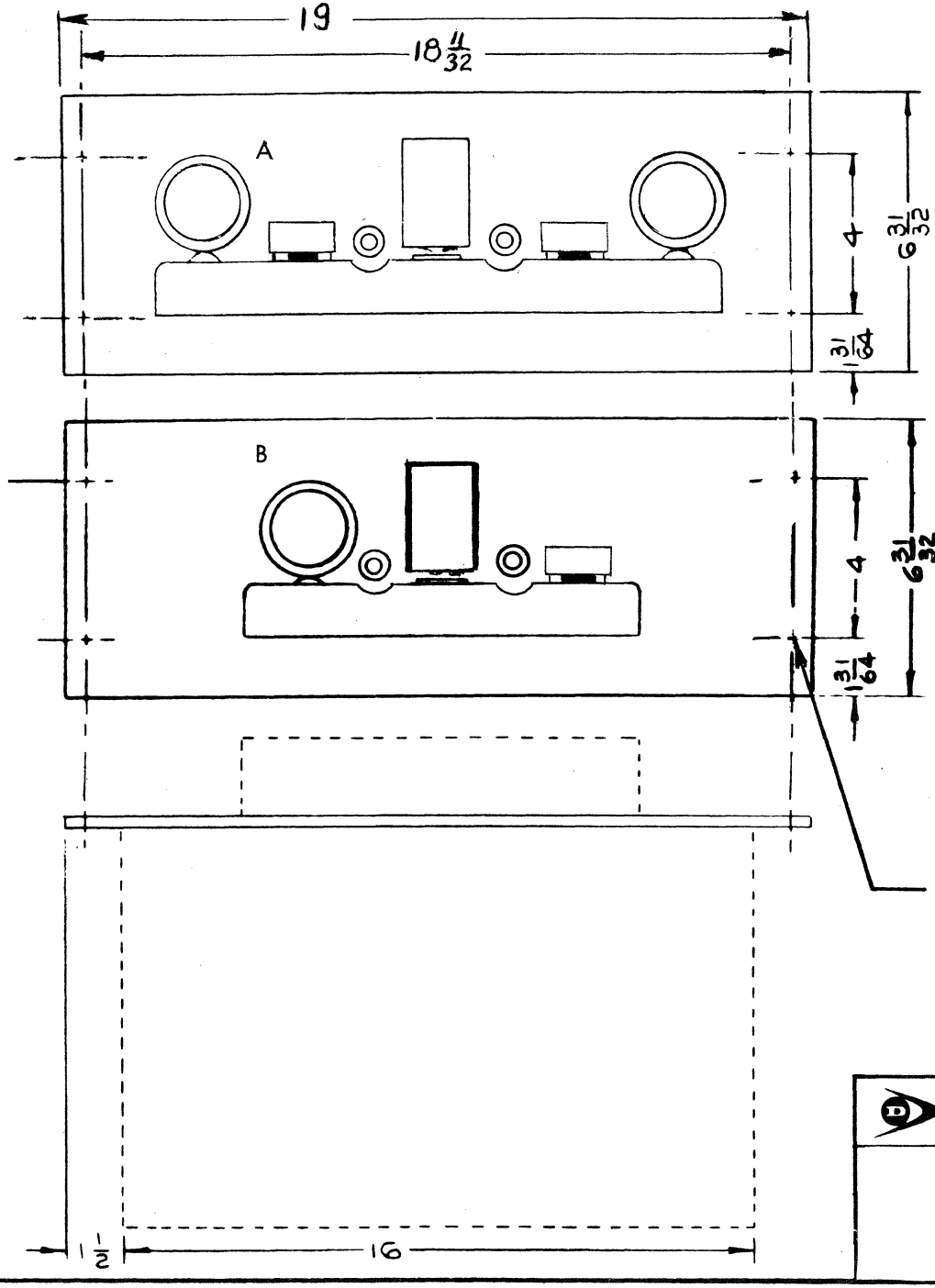
TABLE OF CONTENTS

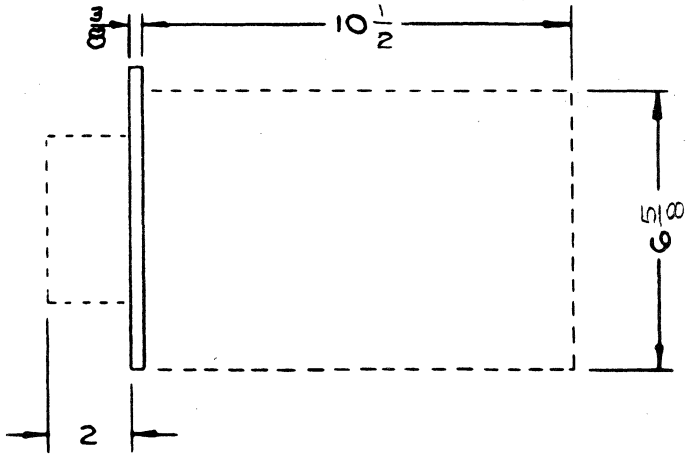
LIST OF TABLES

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS





A - FRONT PANEL B3500
B - FRONT PANEL 3500

Typical hole will accomodate #10 screws spaced to fit RETMA racks.

DIGITRONICS
ALBERTSON, NEW YORK

MODELS 3500 & B3500 TAPE READERS
OUTLINE DRAWING
FIGURE 1-1

SECTION I

INTRODUCTION AND DESCRIPTION

1-1 GENERAL

This handbook contains subject matter required to understand and service Digitronics Models 3500 and B3500 Perforated Tape Readers.

Section I outlines the physical and electrical description of the readers and their associated components.

Section II outlines the necessary installation and operation procedures.

Section III of this handbook describes the Theory of Operation. This section is divided into two sub-sections: Logic Analysis which describes equipment operation using logic symbology and Circuit Analysis in which each symbol used in the logical description is discussed at the electronic circuit level.

Section IV describes the inspection, maintenance and lubrication. This section also outlines the necessary electrical and mechanical adjustment and alignment procedures.

Section V contains an illustrated parts breakdown of the major assemblies and a replaceable electrical parts list.

1-2 PURPOSE OF THE EQUIPMENT

The Models 3500 and B3500 are completely transistorized units which provide up to 8 channels of digital information from opaque perforated tape. Model B3500 is bi-directional; that is, tape transport is either from left-to-right or from right-to-left. Model 3500 is uni-directional; that is, tape transport is from right-to-left.

1-3 APPLICATIONS OF THE EQUIPMENT

The outputs of the equipment may be used with digital computers, numerically controlled machine tools, high speed printers, and other instrumentation.

1-4 EQUIPMENT CAPABILITIES

Table 1-1 lists the equipment capabilities which are available on the units as standard features.

TABLE 1-1 EQUIPMENT CAPABILITIES

CAPABILITY	DESCRIPTION
1. Tape Channel Capacity	This reader is capable of handling tapes of 11/16 in. to 1 in. (5, 6, 7, and 8 channel) interchangeably. Three-position adjustable tape guides conform to the tape width used.
2. Type of Tape	Paper or Mylar tape, .004 to .005 in. thick. Tapes with up to 40% transmissivity are acceptable. With slight adjustment to the pinch roller/brake assemblies tapes from .0025 to .008 may be used.
3. External Start/Stop Control	Start and stop inputs on the connector J-1 can be triggered in 3 ways: (1) Contact closure. (2) Applying a dc voltage that will bring the input line from -6 volts to 0 volts. (3) Applying a 6 volt positive pulse lasting a minimum of 10 microseconds, or a 6 volt negative pulse lasting a minimum of 20 microseconds (positive going edge accomplishes the triggering).
4. Direction of Read	The Model B3500 can read tape in either direction. The Model 3500 is limited to reading in the right-to-left direction.

1-5 OPTIONS AVAILABLE

Table 1-2 lists the options which may be incorporated into the Model 3500 or B3500. Customer options are in no way limited to this table.

TABLE 1-2 OPTIONS AVAILABLE

OPTIONS	DESCRIPTION
1. Speeds Available — To select the proper speed, see diagrams CC2227 and BC2314.	Speed In Char/Sec: 100, 100/300, 125, 125/250, 150, 200, 200/400, 200/800, 250, 250/500, 250/1000, 300, 300/600, 400, 400/800, 450, 450/900, 500, 500/1000, 500/2000, 600, 800, 900, 1000, 1200, 2000, 333.3/1000
2. Low Speed Brake — Stopping Distance When stop pulse is given within 50 microseconds after the leading edge of the sprocket hole.	(1) On character upon command or on the stop character when used at speeds to 250 char/sec. (2) Between characters upon command when used at speeds from 250 char/sec to 500 char/sec.
3. High Speed Brake — Stopping Distance When stop pulse is given within 50 microseconds after the leading edge of the sprocket hole.	(1) On character upon command or on the stop character when used at speeds up to and including 500 char/sec. (2) Before the next character when used at speeds from 500 char/sec up to and including 1000 char/sec.
4. Gated Amplifiers	The data channel amplifiers may be gated internally with the sprocket signal.

TABLE 1-2 Cont'd. OPTIONS AVAILABLE

OPTIONS	DESCRIPTION
5. Ungated Amplifiers	If the ungated option is required the data channels are not gated with the sprocket signal. Note that in both cases (gated and ungated) the sprocket signal is present at the input/output connector J-1.
6. Logic Levels	Data Amplifiers / Hole Output Cur. / No/Hole Output Cur. -10V Hole, 0V no/hole / 5 ma / — +10V Hole, 0V no/hole / 5 ma / — 0V Hole, -10V no/hole / — / 5 ma 0V Hole, +10V no/hole / — / 5 ma Sprocket Shaper / Hole Output Cur. / No/Hole Output Cur. -10V Hole, 0V no/hole / 10 ma / — +10V Hole, 0V no/hole / 10 ma / — 0V Hole, -10V no/hole / — / 10 ma 0V Hole, +10V no/hole / — / 10 ma
7. Stop Character Memory	With this option the unit provides retention of the stop character, which may be recirculated through external equipment, until a start pulse is received.

1-6 SYSTEM REQUIREMENTS

Table 1-3 lists the system requirements.

TABLE 1-3 SYSTEM REQUIREMENTS

INPUT	DESCRIPTION	
Input Power	115V AC 60 CPS 1 PH 150 W	
External Control Signals	1. DC Forward:	Ground the DC input Pin "Y" of J-1
	2. DC Stop:	Ground the DC input Pin "a" of J-1
	3. Pulsed Forward: applied to pin "Z" of J-1	(1) Positive going edge of a positive signal having an amplitude of +5 volts minimum and remain at +5 volts for a minimum of 10 usec. (2) Positive going edge of a negative signal having an amplitude of -5 volts minimum and having been at -5 volts for a minimum of 20 usec.
	4. Pulsed Stop: applied to pin "b" of J-1	(1) Positive going edge of positive signal having an amplitude of +5 volts minimum and remain at +5 volts for a minimum of 10 usec. (2) Positive going edge of a negative signal having an amplitude of -5 volts minimum and having been at -5 volts for a minimum of 20 usec.
(B3500 only)	5. DC Reverse:	Ground the dc input Pin "W" of J-1

TABLE 1-3 Cont'd. SYSTEM REQUIREMENTS

INPUT	DESCRIPTION	
External Control Signals (B3500 only)	6. Pulsed Reverse: applied to pin "X" of J-1	(1) Positive going edge of positive signal having an amplitude of +5 volts minimum and which remains at +5 volts for a minimum of 10 usec. (2) Positive going edge of a negative signal having an amplitude of -5 volts minimum and which has been at -5 volts for a minimum of 20 usec.

1-7 EQUIPMENT DESCRIPTION

Two major component systems comprise the Model 3500 and B3500 tape readers: (1) Tape Drive system consists of two drive capstans and two pinch rollers with associated solenoids; (1 on 3500) two brakes with associated solenoids; (1 on 3500) two adjustable tape guides; and associated packaged electronic circuitry; (2) Tape Read system consists of a photo-electric read head with exciter lamp and the associated packaged electronic circuitry. All mechanical components of the tape drive system and the tape read system photodiode read head assembly are mounted on 6 31/32 inch high by 19 inch long panel designed for installation in a standard 19 inch rack or tray. The electronic packages with associated hardware are mounted on a 16 inch by 10 inch by 2 1/2 inch chassis physically connected to the rear of the reader panel. AC power, external start/stop signals, and all the output signals are applied to the unit through connector P-1.

1-8 TAPE DRIVE SYSTEM

B3500 The tape drive system (figure 5-5A B3500) consists of two tape drive capstans which are belt driven by a synchronous hysteresis motor (figure 5-4) located at the rear of the tape reader panel; two pinch rollers and their associated solenoids; two tape guide rollers; two adjustable tape guide posts with associated arms; and two brakes. The tape rides on a tape guide roller and passes between a pinch roller and tape drive capstan and a braking surface. Two tape guide posts, one on each side of the photo-electric read head serve to guide the tape over the read head. From the read head, the tape passes between another braking surface and a pinch roller-capstan assembly, and then over another tape

guide roller. When the tape drive system is in forward motion, the pinch roller capstan assembly pulls the tape from right-to-left. When the tape drive system is in reverse motion, the other pinch roller capstan assembly pulls tape from left-to-right.

3500 The tape drive system (figure 5-5) consists of one tape drive capstan which is belt driven by a synchronous hysteresis motor located at the rear of the tape reader panel, (figure 5-4) one pinch roller and associated solenoid, two tape guide rollers, adjustable tape guide posts with associated arms, and one brake. The low speed brake (figure 5-9) has an associated solenoid while the high speed brake (figure 5-10) is a self-contained unit. Two tape guide posts, one on each side of the photo-electric read head serve to guide the tape between the read head. From the read head the tape passes between a pinch roller, capstan assembly, and then over another tape guide roller. When the tape drive system is in motion, the pinch roller/capstan assembly on the left side of the read head pulls the tape from right-to-left.

1-9 TAPE STARTING AND STOPPING

The tape is set into motion by a forward or reverse command, either dc or pulsed, which energizes the pinch roller solenoid. With the pinch roller solenoid energized, the pinch roller moves upward and presses the tape against the continuously rotating tape drive capstan which pulls the tape over the read head. In stopping tape motion, a stop command, either dc or pulsed, causes the pinch roller solenoid to de-energize and the brake to energize. When a low speed brake is used, energizing the brake solenoid causes the brake bracket to move upwards, pressing the tape against the non-rotating brake drum. When a high speed brake is used, the stop command energizes the high speed brake coil which in turn causes the armature to be pulled down against the stationary brake surface, stopping tape movement.

1-10 DRIVE MOTOR

The drive motor (figure 5-4) is a single phase, 60 CPS, 115 volt synchronous hysteresis motor. The motor is equipped with a reduction pulley that drives both capstan pulleys. An endless belt is used to transmit the driving power from the reduction pulley to the capstan pulley. AC power is supplied to the motor through connector P4. Motor direction differs in Models 3500 and B3500. As viewed from the front, the B3500 motor rotates counterclockwise while the 3500 motor rotates clockwise.

1-11 TAPE READ SYSTEM

The photodiode read head is a nine-channel photodiode unit. Eight photodiodes of the unit are used to read character information from the tape and the other photodiode is used to read sprocket holes in the tape. Illumination of the head is accomplished by use of a dc operated, 10 watt exciter lamp. The lamp directs the light through an aperture in the exciter lamp cover to the photodiode read head. When the tape is in motion, it passes between the read head exciter lamp and the surface of the read head photodiodes. The exciter lamp receives dc power through connector P5 (figure 5-1) from the reader power supply. A separate connector cable P2 (figure 5-1) connects the photodiode head to the dc source and a nine-channel amplifier located on the reader chassis assembly. In the event of photodiode failure, the read head assembly should be sent back to the factory intact.

NOTE

Under no circumstances should the photodiodes be removed from the read head assembly.

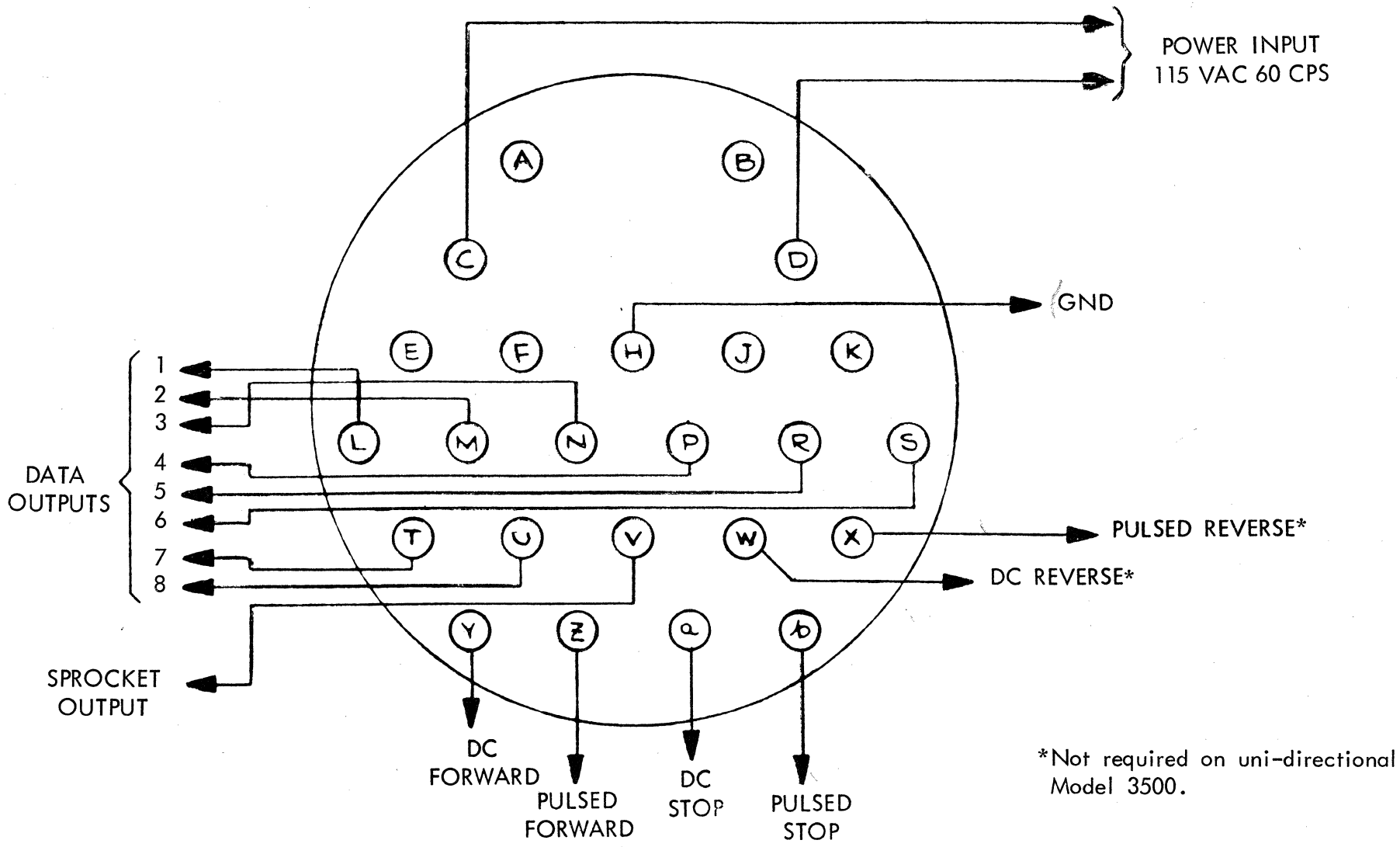


FIGURE 2-1 Connector Cable P1 Wiring Diagram

SECTION II

INSTALLATION AND PREPARATION FOR USE

2-1 GENERAL

This section contains the necessary installation and preparatory procedures for operating the 3500 and B3500 tape readers. Each model is shipped in a reinforced packing case designed to provide maximum protection during transportation. Upon unpacking the unit, a visual inspection should be accomplished to ascertain whether the unit had sustained any damage in transit. Special attention should be given to the exciter lamp and read head unit during this inspection.

2-2 INSTALLATION

There are no special procedures necessary when installing the reader in its permanent equipment housing. The unit operates equally well mounted in either a standard 19 inch vertical relay rack or a 19 inch horizontal mounting frame. When the reader is mounted apart from other units, no special ventilation or air-conditioning is necessary. However, when located near heat-producing equipment it is necessary to provide adequate means of cooling the unit (forced air fans - air conditioning). Operating temperature 77° ±35° F.

2-3 PREPARATION FOR USE

2-4 PRE-OPERATIONAL PROCEDURES

The pre-operational procedures required for the readers are contained in Table 2-1. Wire connector P1 in accordance with Figure 2-1.

TABLE 2-1 PRE-OPERATIONAL PROCEDURES

STEP	PROCEDURE	RESULTS
1.	Connect a 115V AC source to J-1 on reader chassis.	a. Capstan motor starts operating. b. Exciter lamp lights. c. DC power supply is energized.
2.	Check dc power supply outputs.	a. +15 volts at SPA-A Pin "B" b. -15 volts at SPA-A Pin "D" c. -30 volts at SPA-A Pin "A"

TABLE 2-1 Cont'd. PRE-OPERATIONAL PROCEDURES

STEP	PROCEDURE	RESULTS
2. Cont'd.	-10V hole 0V no/hole 0V hole +10V no/hole or +10V hole 0V no/hole 0V hole -10V no/hole	d. -5.5 ±.2 volts from Standoff #9 to Gnd. or +5.5 ±.2 volts from Standoff #9 to Gnd.
3.	Insert a loop of tape DC FORWARD RUN Connect a ground potential to J1-Y	a. Forward pinch roller solenoid energizes. b. Brake solenoids de-energize. c. Tape moves from right-to-left.
4.	DC STOP Connect a ground potential to J1-a	a. Forward pinch roller solenoid de-energizes. b. Forward brake solenoid energizes. c. Tape stops.
5.	PULSED FORWARD RUN Apply the positive edge of a +5 volt 10 usec signal or the positive edge of a -5 volt 20 usec signal to J1-Z.	a. Forward pinch roller solenoid energizes. b. Forward brake solenoid de-energizes. c. Tape moves from right-to-left.
6.	PULSED STOP Apply the positive edge of a +5 volt 10 usec signal or the positive edge of a -5 volt 20 usec signal to J1-b.	a. Forward pinch roller solenoid de-energizes. b. Forward brake solenoid energizes. c. Tape stops.

TABLE 2-1 Cont'd. PRE-OPERATIONAL PROCEDURES

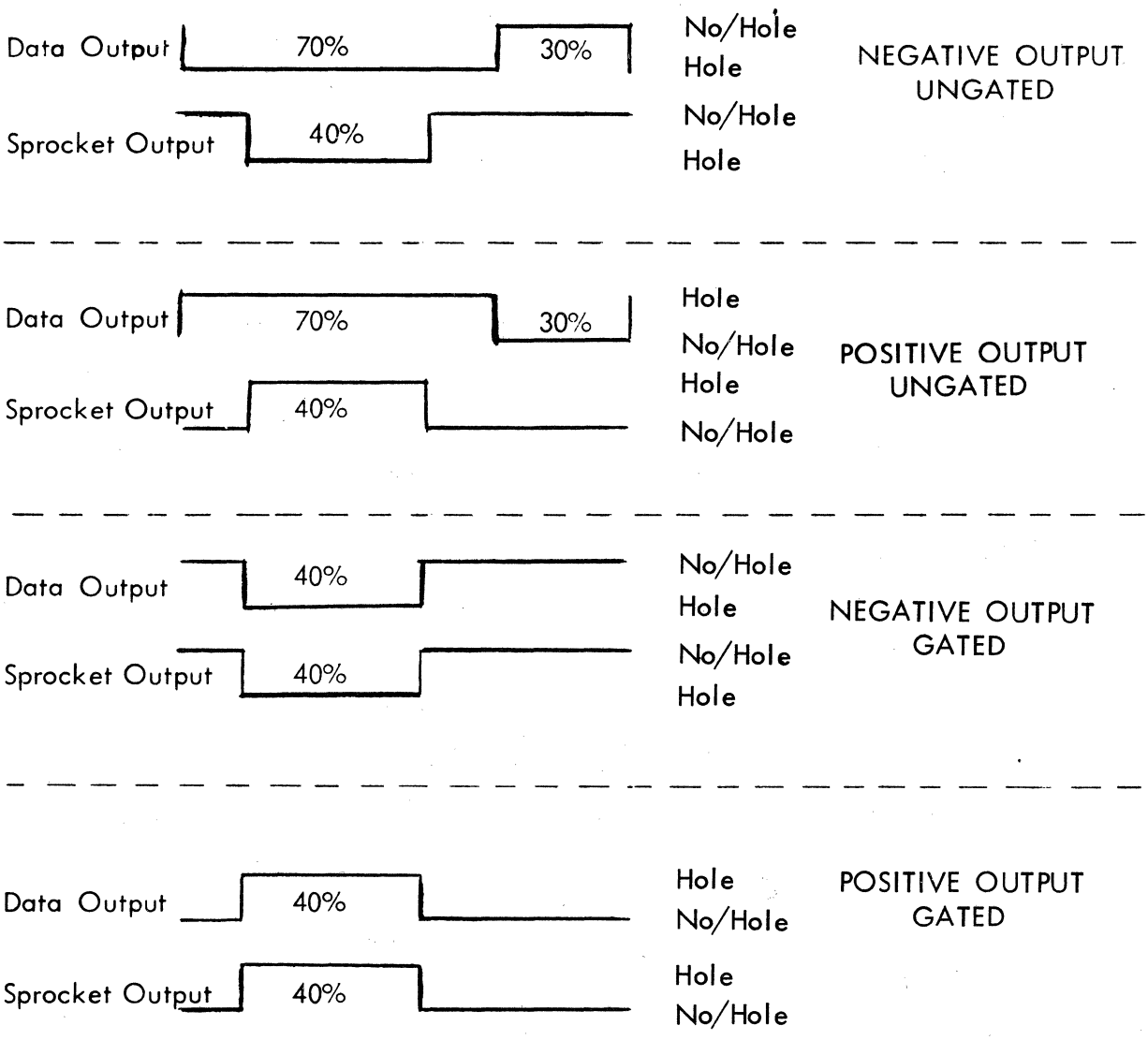
STEP	PROCEDURE	RESULTS
7.	DC REVERSE (B3500 only) Connect a ground potential to J1-W.	a. Reverse pinch roller solenoid energizes. b. Brake solenoids de-energize. c. Tape moves from left-to-right.
8.	Perform Step 6. (B3500 only)	a. Reverse pinch roller de-energizes. b. Reverse brake energizes. c. Tape stops.
9.	PULSED REVERSE (B3500 only) Apply the positive edge of a +5 volt 10 usèc signal or the positive edge of a -5 volt 20 usec signal to J1-X	a. Reverse pinch roller solenoid energizes. b. Brake solenoids de-energize. c. Tape moves from left-to-right.
10.	Perform Step 8. (B3500 only)	Same as Step 8.

2-5 PERFORMANCE CHECKOUT PROCEDURES

The performance checkout procedures for the readers are contained in Table 2-2.

TABLE 2-2 PERFORMANCE CHECKOUT PROCEDURES

STEP	PROCEDURE	RESULTS
1.	Wire cable connector P1 as indicated in figure 2-1 and connect to J1.	
2.	Insert loop of tape with all channels punched.	



NOTE 1: All of the above waveshapes are taken from TP3, of individual amps., which correspond to the signals available at J-1.

NOTE 2: Due to propagation effects, the data outputs in the GATED mode are between 1 — 2 usec shorter in duration than the sprocket output.

FIGURE 2-2 TYPICAL READER OUTPUT WAVESHAPES

TABLE 2-2 Cont'd. PERFORMANCE CHECKOUT PROCEDURES

STEP	PROCEDURE	RESULTS
3.	Operate external equipment to provide start and stop signal.	Tape motion starts and stops as programmed.
4.	UNGATED READ AMPLIFIERS With reader operating and tape in motion observe sprocket channel output waveshape using oscilloscope synchronized internally, and the ten divisions across the face of the oscilloscope representing one period.	The waveshape should be negative or positive (depending on output) for 40% +3%, -5% of the overall period (four divisions). See figure 2-2.
5.	With reader operating and tape in motion observe all data channels (Test Point #3 on all cards) using oscilloscope synchronized internally and the ten divisions across the face of the oscilloscope representing one period. (And tape fully punched)	The waveshapes should show a negative or positive hole time (depending on output) of 70%. See figure 2-2.
6.	Using the dual trace option, synchronize the oscilloscope externally with each data channel. a. With the oscilloscope channel A probe, observe the waveshape of each channel. b. With the oscilloscope channel B probe, observe the sprocket channel waveshape and compare the physical relationship between the two signals.	The sprocket channel output should be effectively centered in the data channel output. See figure 2-2 for idealized waveshape relationship. Repeat steps 6a and 6b for all data channels. (Use test point #3 on the sprocket channel card and test point #3 for each data channel card.)

TABLE 2-2 Cont'd. PERFORMANCE CHECKOUT PROCEDURES

STEP	PROCEDURE	RESULTS
7.	GATED READ AMPLIFIERS With reader operating observe each data channel separately at Test Point #3.	The waveshape should be negative or positive (depending on logic output) for 40% +3%; -5% of the overall period (four divisions). See figure 2-2.
8.	Repeat Step 5 using Test Point #2 on all cards.	Same result as in Step 5 with hole time of opposite polarity.
9.	Repeat Step 6 a. and b. and Step 7.	The data channel output signals and the sprocket channel outputs should coincide. See figure 2-2 for idealized waveshape relationship. Repeat steps 6 and 7 for each data channel.

SECTION III

THEORY OF OPERATION

3-1 GENERAL

This section describes the logics and circuitry of the 5 types of model 3500 and B3500 perforated tape readers. The special option, Stop Character Memory (SCM), is also discussed in this section.

3-2 SIGNAL TERMINOLOGY - TAPE READ SYSTEM

Signal terminology consists of the terms logical "1" and logical "0" usually abbreviated "1" and "0" respectively. Logical "1" will correspond to hole condition and logical "0" will correspond to no/hole condition. Listed below are the 4 type outputs available from the data channel amplifiers for the model 3500 or B3500.

	OUTPUTS			
LOGICAL "1" HOLE	-10V	0V	+10V	0V
LOGICAL "0" NO-HOLE	0V	-10V	0V	+10V

3-3 SIGNAL TERMINOLOGY - TAPE DRIVE SYSTEM

For the tape drive systems, logical "1" will represent a -6 volt signal for both B3500 and 3500 Models, and logical "0" will represent approximately 0 volts. This terminology was employed to insure compatibility with all units.

3-4 SYMBOL TERMINOLOGY

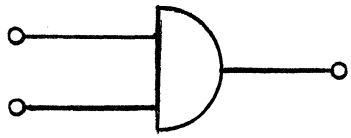
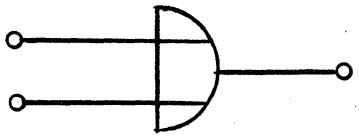
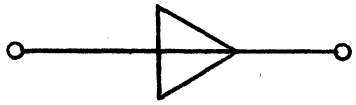
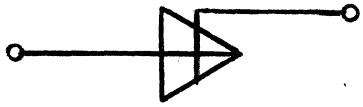
The symbols contained in the Table 3-1 are used throughout Digitronics logics and may be used as a guide to understanding all Digitronics equipment.

3-5 POWER SUPPLY (See Figure 3-1 and 3-2)

The power supply operates on 115V, single phase AC power and draws 150 watts of power. The power supply provides +15V, -15V, -30V, bias voltage for the photodiodes, and an exciter lamp voltage supply.

The AC power is applied through input/output connector J-1 to the capstan motor and power transformer B-T53. The capstan motor is a synchronous drive motor with a smooth rotor which provides uniform tape motion. Power transformer B-T53 has two secondaries; a low voltage center-tapped winding to provide the positive and negative 15V DC supply, and a winding to provide -30V DC to the DRIVE and BRAKE solenoids.

TABLE 3-1 LOGIC SYMBOLS

SYMBOL	NOMENCLATURE
	Gate or "AND" Gate
	Buffer or "OR" Gate
	NON-INVERTING AMPLIFIER
	INVERTER

Diodes CR2A, CR2B, CR3A, and CR3B provide full wave rectification for use in the +15V DC, -15V DC, bias and exciter lamp supply. Diodes Cr1A and CR1B provide negative half-wave rectification for use in the -30V DC supply.

Diodes CR3A and CR3B apply -15V DC through the RC filtering network R16-C2, R1-C1 and through plug P5 pin 2 to one side of the exciter lamp. The RC filtering network provides the -15V DC to the rest of the reader and also through connector J3 to the plug-in module (P3). This plug-in module supplies regulated bias for the photodiode. This bias is in accordance with Table 2-1, Step 2. (See Note 2 on figure 3-2 - DH718.)

Diodes CR2A and CR2B apply +15V DC through to the RC filtering network R2-C3; R3-C4; and resistor network R5, R6, and R7 to plug J5 pin 1 the other side of the exciter lamp. The RC filtering network provides the +15V DC to the reader and a +15 volt line to connector P3 for supplying the +5.5V bias in accordance with Table 2-1, Step 2. (See Note 2 on figure 3-2 - DH718.) The exciter lamp is connected across J5 in parallel with Zener diode (MOTOROLA 50M10Z5). This diode is used to regulate the voltage applied to the exciter lamp. R5 and R6 provide adjustment of the voltage to the Zener diode, while R7 is used to adjust the voltage applied to the exciter lamp.

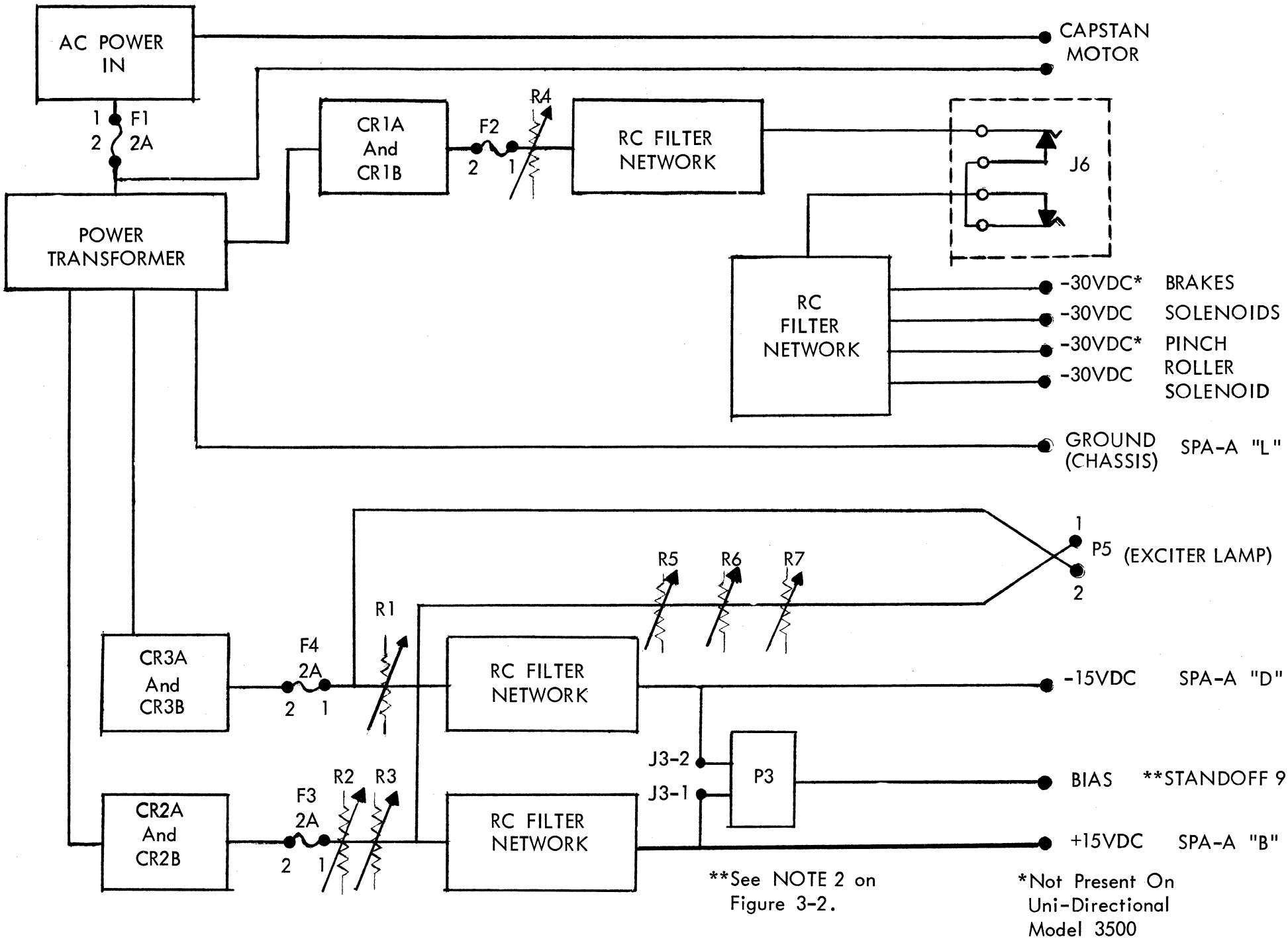


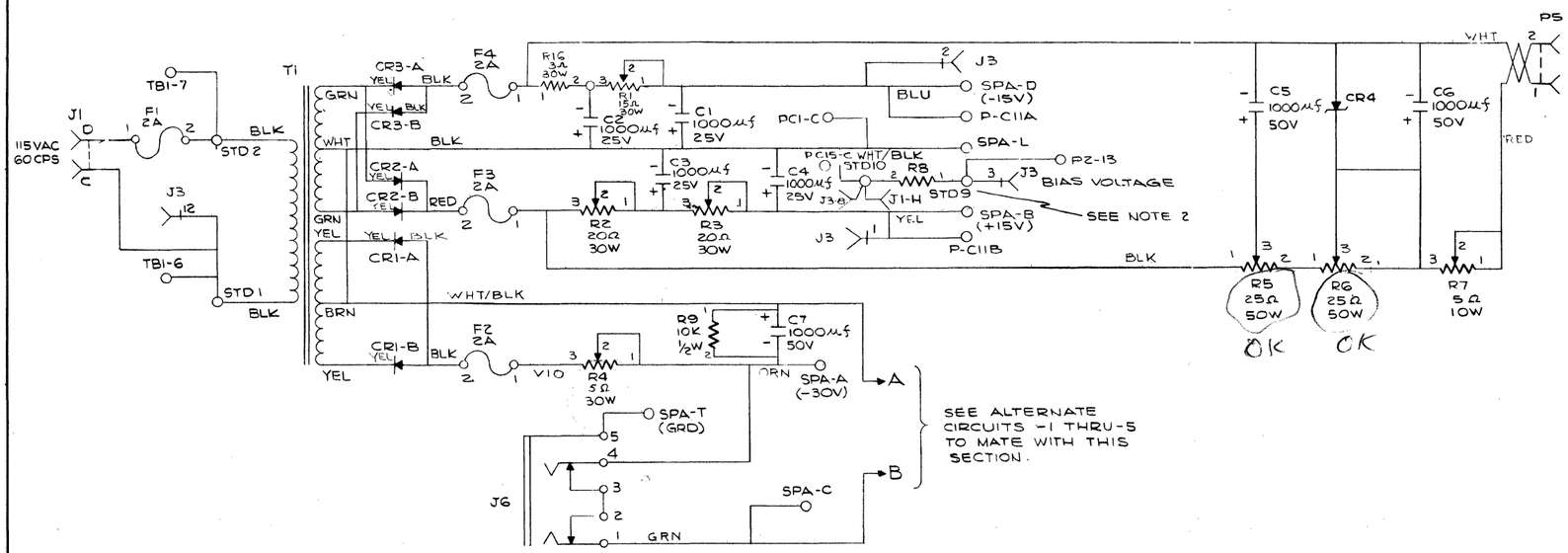
FIGURE 3-1 POWER SUPPLY BLOCK DIAGRAM

Diodes CR1A and CR1B apply a -30V DC through adjustable resistor R4, the RC filtering network R9-C7 and connector J6 to one of the speed-up networks -1 -2 -3 -4 or -5 (Table 3-2). The speed-up networks provide 600 ma (1.5 amp for brakes in option -2 and -4) at -30V DC to the brake and drive circuits on the SPA-A card. Connector J6 may be used in conjunction with Digitronics Perforated Tape Handlers. The Model 6070 may be used to provide rewind of the tape once it has been read.

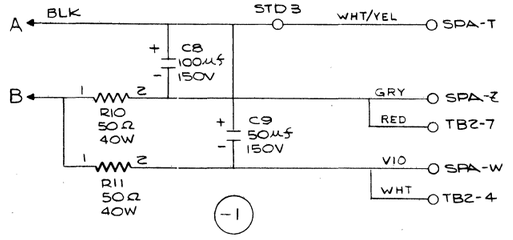
TABLE 3-2 POWER SUPPLY OPTIONS

OPTION NO. D-H718-	USED ON
-1	Uni-Directional, Standard Brakes
-2	Uni-Directional, Hi-Speed Brakes
-3	Bi-Directional, Standard Brakes
-4	Bi-Directional, Hi-Speed Brakes
-5	Bi-Directional, Hi-Speed Brakes (Double Braking System)

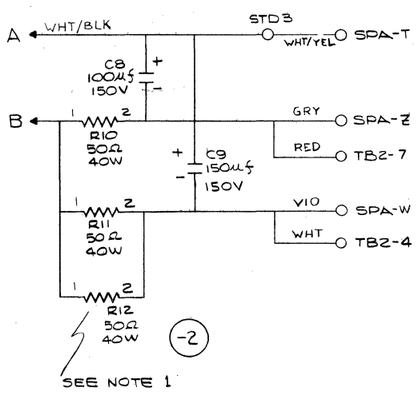
QUAN.	DESCRIPTION	REF. STD.	DRWG. NO.	ITEM



SEE ALTERNATE CIRCUITS -1 THRU-5 TO MATE WITH THIS SECTION.

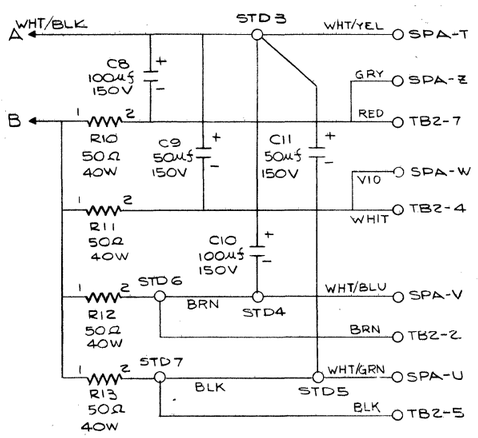


UNI-DIRECTIONAL, STANDARD BRAKES

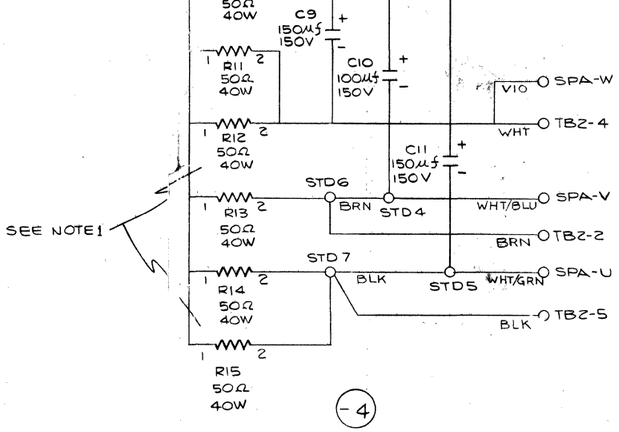


UNI-DIRECTIONAL, HI-SPEED BRAKES

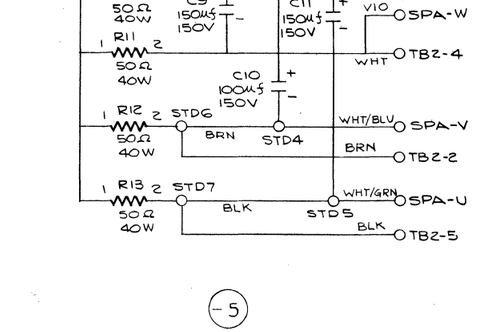
SCHEMATIC	WIRE AS PER	ADDITIONAL WIRING SHEET
D-H718- 1	D-K400-66	B-K 304 -1
" -2	"	" -2
" -3	"	" -3
" -4	"	" -4
" -5	"	" -5



BI-DIRECTIONAL, STANDARD BRAKES



BI-DIRECTIONAL, HI-SPEED BRAKES



BI-DIRECTIONAL, HI-SPEED BRAKES (DOUBLE BRAKING SYSTEM)

NOTES:
1. R12 ON[-2] AND R12 & R15 ON -4 USED ON[LY] IN READERS EQUIPPED WITH HI[-] SPEED BRAKES.
2. BIAS VO[LTA]GE AT STD 9 MAY BE EITHER [-]5.5V OR +5.5V DEPENDING ON WHIC[H] CONFIGURATION OF P3 (PARTIC[U]LARIZING PLUG) IS IN USE.

DIGITRONICS
ALBERTSON, NEW YORK

TITLE:
3-2
SCHEMATIC
POWER SUPPLY

FIRST USED ON:

SHEET ____ OF ____

DRAWING NO.
D-H 718

3-6 LOGIC ANALYSIS

As shown in the logic block diagrams, figure 3-26 and 3-27, the unit contains a tape read system and a tape drive system. The tape read system (fig. 3-27) consists of a sprocket channel shaper, an auxiliary amplifier, and 8 data channel amplifiers. The tape drive system (figure 3-26) consists of start/stop amplifiers, start/stop control flip-flop, forward/reverse control flip-flop, power amplifier and coil driver.

The block diagrams show the wiring connection between the various cards. Numbers in the hexagonal boxes indicate test points. The numbers not in hexagonal boxes correspond to the physical location of each card in the card slot on top of reader chassis. The single letters on the diagram and referred to in quotes in the circuit analysis pertain to the socket pin numbers of the cards on the card sockets. As an aid in trouble shooting, the internal logic levels, "1" and "0", may be converted to voltage levels. Logical "1" equals -6 volts and logical "0" equals 0 volts.

3-7 LOGIC OUTPUT SYSTEM (See Figure 3-27)

The following paragraphs describe the various options of the Logic Output System. Refer to Figure 3-27, LOGIC OUTPUT SYSTEM BLOCK DIAGRAM, while referring to the paragraphs below.

3-8 -10 VOLT HOLE, 0 VOLT NO HOLE OUTPUT (OPTION 1A)

The reader equipped with this option contains the following cards:

Sprocket Channel Amplifier	PSE-A	1 each
Auxiliary Amplifier	AAA-1	1 each
Data Channel Amplifier	PGF-A	8 each

Refer to the LOGIC OUTPUT SYSTEM BLOCK DIAGRAM (fig. 3-27).

Circuit A logically represents the PSE-A sprocket amplifier and the AAA-1 auxiliary amplifier located in positions 9 and 10 of the circuit card holder on the reader chassis. Circuit C represents the data channel amplifier PGF-A located in positions 1 through 8 of the circuit card holder on the reader chassis. The logical description of the two circuits follow:

NOTE

Logical "1" equal to a -level (Hole Output)
Logical "0" equal to a ground level (No/Hole Output)

(1) Logical Operation Of PSE-A and AAA-1 Cards

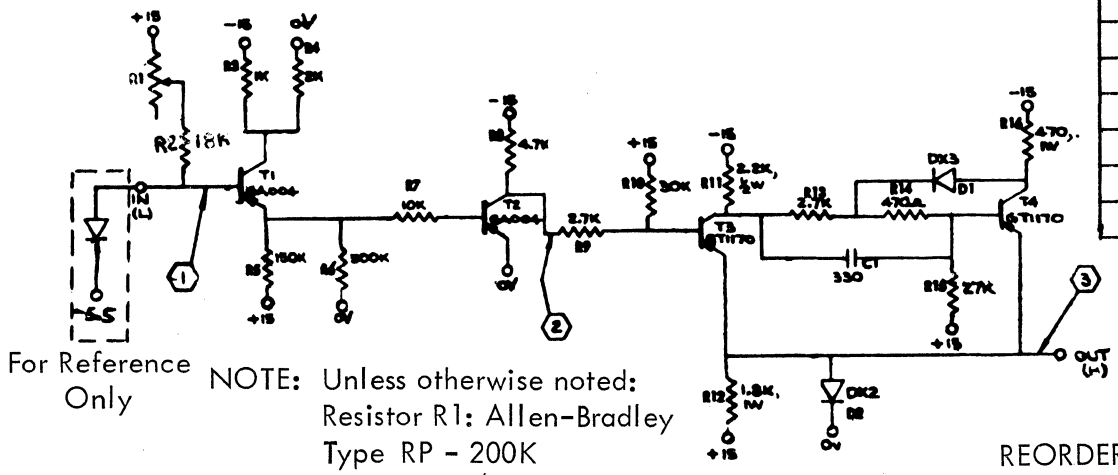
When the sprocket photodiode reads a hole, a logical "1" signal is applied through the non-inverting amplifier (EF) to the base of the first inverter/amplifier. This first stage inverts the signal to a logical "0" and applies it to the second inverter (ST). The second inverter shapes, as well as inverts the signal and applies the logical "1" signal to the input (Pin "L") of the auxiliary amplifier card AAA-1.

When the AAA-1 card receives the output of the PSE-A card, through pin "L" (AAA-1), the signal is applied to an inverter/amplifier on the AAA-1 card. The logical "0" output of this inverter/amplifier is called "-PSP"; this signal remains at "0" for the duration of the sprocket hole after which it reverts to a logical "1". "-PSP" is then applied through connector J-3 to the eight data channel amplifiers and to the second inverter on the AAA-1 card (Note table at bottom of figure 3-2 showing wiring of the plug P-3). The second inverter on the AAA-1 card inverts the signal and applies it as a logical "1" signal to the input/output connector J-1 as the sprocket signal "PSP". This signal remains at "1" for the duration of the sprocket hole, after which it reverts to a logical "0". The "-PSP" signal is used to shape and time the data channel output signals with the sprocket signal so that all 8 data channels start and end at the same time. The signal "PSP" can be used to gate the external equipment.

(2) Logical Operation Of Data Channel Amplifier PGF-A

When any of the 8 data channel photodiodes reads a hole, it conducts. This applies an input logical "1" signal to the non-inverting amplifier on the data channel PGF-A card. The non-inverted signal is then applied to an inverter which, in turn, applies a logical "0" to one of the inputs of the "OR" gate for the duration of the hole time. It is here that the sprocket signal "-PSP" is combined with the data channel signal.

The function of the sprocket signal is to shape and time the data channel signal. The output of the gate is applied through the second inverter/amplifier to the output portion of the card and then to the input/output connector J1, (see figure 2-1 for location of the 8 data channel output signals on the input/output connector). For an electrical circuit analysis of the PSE-A, AAA-1, and PGF-A, see electrical circuit analysis following the logical description in this section.



PIN	SIGNAL
A	-15
B	+15
C	0V
D	
E	
F	
H	OUT
J	
K	
L	IN

For Reference Only

NOTE: Unless otherwise noted:
Resistor R1: Allen-Bradley
Type RP - 200K
Resistors: 1/4W, 5%
Diodes: GTDX3

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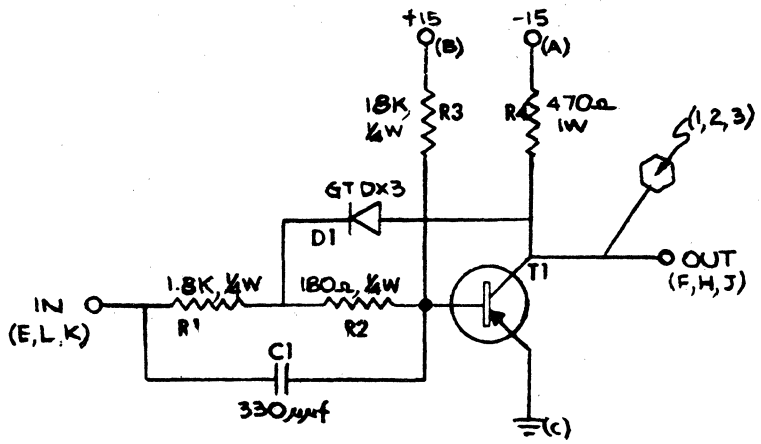
P.C. ASSEMBLY #B-C1400

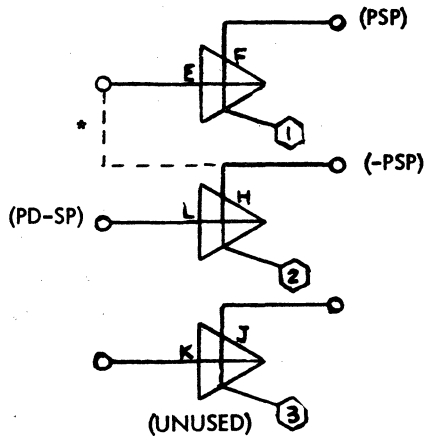
FIGURE 3-3 SCHEMATIC DIAGRAM - PSE-A

(3) Circuit Description Sprocket Amplifier/Shaper PSE-A (See Figure 3-3)

When the sprocket photodiode conducts during a hole condition, the negative signal produced by the photodiode is applied to the base of emitter follower (EF) T1. T1 couples this negative signal to the base of amplifier T2, turning it on. T2 applies this signal to the Schmitt trigger (ST) shaper transistors T3 and T4. The negative going voltage at the collector of T3 is coupled through a capacitor to the base of the emitter follower in T4. Conduction in T4 rises with the collector current being drawn through a emitter resistor common to both transistors. The increased current through this emitter resistor results in a negative going change in the emitter potential of T3. The cumulative effect of any increasingly positive base potential and increasingly negative emitter potential accelerates the drop in collector current of T3. The collector potential is thereby driven further negative, and is coupled through the input resistors to the base of transistor T4, with the

result that the conduction through T4 is further increased. This positive feedback effect, thus produces a rapid cutoff of the first stage while similarly abruptly driving the second stage towards saturation. The effect of the Schmitt trigger on the input signal is to produce a rapid rise and decay time at the leading and trailing edges of the sprocket signal. Thus, the Schmitt trigger shapes the input signal into a clean square wave. The output of the sprocket amplifier shaper PSE-A is therefore a clean -10 volt for a hole signal and 0 volts for a no-hole condition.





AUXILIARY AMPLIFIER → MODULE	"AAA-1"	"AAA-3"
0V OUTPUT TOLERANCE →	+0V, -0.5V	+0V, -0.2V
TRANSISTOR TYPE →	GT1170	PHILCO 2N598
PRINTED CIRCUIT ASSY # →	B-C416	B-C1543

* EXTERNAL CONNECTION

3 AMPLIFIERS PER MODULE

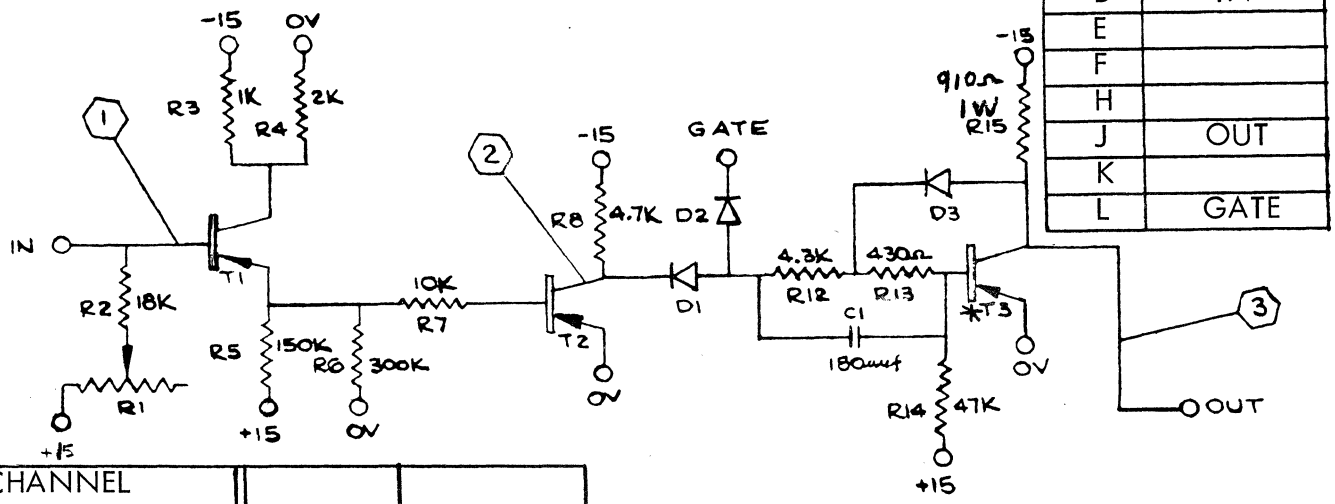
FIGURE 3-4 SCHEMATIC DIAGRAM - AAA-1 or AAA-3

(4) Circuit Description - Auxiliary Amplifier AAA-1 (See Figure 3- 4)

This auxiliary amplifier AAA-1 (figure 3-4) contains three separate circuits which may be wired together or used individually. When wired, as shown in the block diagram Fig. 3-27 and Fig. 3-4, the output of the PSE-A card is applied through pin "L" to the base of one of the transistors on the AAA-1 card. This signal turns on the

transistor, producing the 0 volt output "-PSP". This output is coupled to the 8 data channel amplifiers and to the next amplifier on the card. When this signal is applied to the second amplifier, which is normally conducting, the transistor turns off producing signal "PSP". Signal "PSP" is capable of applying 10V @ 10 ma into a 1K load.

PIN	SIGNAL
A	-15
B	+15
C	0V
D	IN
E	
F	
H	
J	OUT
K	
L	GATE



CHANNEL AMPLIFIER MODULE	PGF-A	PGL-A
0V OUTPUT TOLERANCE	+0V -0.5V	+0V -0.2V
*TRANSISTOR T3 TYPE	GT1170	PHILCO 2N598
RE-ORDER BY PRINTED CIRCUIT ASSEMBLY #	BC1407	BC1544

NOTE: Unless otherwise noted:
Resistor R1: Allen-Bradley Type RP - 200K
Resistors: 1/4W, 5%
Diodes: GTDX3

FIGURE 3-5 SCHEMATIC DIAGRAM - PGF-A or PGL-A

(5) Circuit Description Data Channel Amplifier PGF-A (See Figure 3-5)

This unit contains 8 data channel amplifiers type PGF-A (figure 3-5). Each of these amplifiers produce an output of -10 volts into a 2K load for a hole condition and 0 volt for a no-hole condition. These 8 outputs are applied directly to the input/output plug J-1, pins L, M, N, P, R, S, T, and U.

When any of the eight photodiodes reads a hole, it will conduct. This conduction applies a negative signal through emitter follower T1 to the base of amplifier T2, which also conducts. When T2 conducts, 0V is applied to one of the "OR" gate diodes, D1.

Transistor T3 will conduct when either a -6 volts ("-PSP") sprocket signal from the AAA-1 card or a -6 volt input from T2 is applied to its base; thus T3 is conducting until both the sprocket signal and T2's output goes positive. When this happens, T3 cuts off applying a negative signal at its output for the duration of the combined 0 volt inputs to the diodes. The sprocket hole is smaller than the data hole, therefore the duration of the sprocket signal will be shorter than that of the data signal. This causes the data signal to be gated by the sprocket signal. All eight data channel amplifiers receive the same sprocket signal. This assures that all data outputs will initiate and terminate at the same time.

3-9 -10 VOLTS HOLE 0 VOLTS NO/HOLE SCM (OPTION 1B)

The reader equipped with this option contains the following cards:

Sprocket Channel Amplifier	PSE-A	1 each
Auxiliary Amplifier	AAA-SCM	1 each
Data Channel Amplifier	PGE-A	8 each.

Refer to the LOGIC OUTPUT SYSTEM BLOCK DIAGRAM (Figure 3-27).

The table at the bottom of the diagram shows that option 1B (-10 VOLTS HOLE 0 VOLTS NO/HOLE SCM) uses circuits B and D. Circuit B logically represents the PSE-A Sprocket Amplifier and the AAA-SCM Auxiliary Amplifier located in slots 9 and 10 of the circuit card holder. Circuits D represent the Data Channel Amplifiers PGE-A located in card slots 1 through 8 of the circuit card holder. The logical description of these circuits is given below. The circuit analysis of each card is located behind the logical descriptions in this section.

NOTE

Logical "1" equal to a -level (Hole Output)
Logical "0" equal to a ground level (No/Hole Output)

(1) Logical Operation Of PSE-A & AAA-SCM Cards (Circuit B)

When the sprocket photodiode reads a hole, a logical "1" signal is applied through the non-inverting amplifier (EF) to the base of the first inverter/amplifier. This stage inverts the signal to a logical "0" and applies it to the second inverter (ST). The second inverter shapes, as well as inverts, the signal and applies this logical "1" signal to the input of the Auxiliary Amplifier card AAA-SCM.

When the AAA-SCM card receives the output of the PSE-A card, through pin "L" (AAA-SCM), the signal is applied to an inverter/amplifier on the AAA-SCM card. The logical "0" output of the inverter/amplifier is called "-PSP". This "-PSP" signal remains at "0" for the duration of the sprocket hole after which it reverts to a logical "1". This "-PSP" signal is then applied through connector J-3 to the eight data channel amplifiers and to the second inverter on the AAA-SCM card. (Note table at bottom of figure 3-27 showing wiring of the plug P-3.) The second inverter on the AAA-SCM card inverts the signal and applies it as a logical "1" signal to the input/output connector J-1 as the sprocket signal "PSP". This "PSP" signal remains at logical "1" for the duration of the sprocket hole, after which it reverts to a logical "0".

The "-PSP" signal is used to shape and time the data channel output signals with the sprocket signals so that all 8 data channels start and end at the same time. While the ungated readers contain this option, it is not wired into the connector J-3. (See table at bottom of figure 3-27 for gating or ungating the reader.) The "PSP" signal can be used to gate external equipment.

The second input to the "OR" gate, signal *"ST", is a logical "1" signal that is generated when the unit gets a stop command from Motion Control, package #14. This logical "1" input to the first inverter of the AAA-SCM card will produce a logical "0" "-PSP" signal through the first AAA-SCM inverter and a logical "1" "PSP" signal through the second inverter. These signals, "-PSP" and "PSP" will be maintained as an output of the AAA-SCM until the Motion Control section receives a start command.

(2) Logical Operation Of The Data Channel Amplifier PGE-A (Circuit D)

When any of the eight Data Channel photodiodes reads a hole, it will conduct. This applies an input logical "1" signal through the non-inverting amplifier (EF) to the "OR" gate. The "OR" gate applies the signal to the first inverter where the signal is inverted to a logical "0" and applied to an input of the "AND" gate. Input "L" of the "AND" gate receives "-PSP" (logical "0") and logical "0" from the first PSG-A inverter. When these signal levels are present as inputs to the "AND" gate, the output of the gate is logical "0". This logical "0", when applied to the second inverter, produces a logical "1". This logical "1" is applied in two places - (1) as an output of the card through input/output connector J1 pins L, M, N, P, R, S, T, and U; and (2) as feedback loop to the other input of the "OR" gate. This logical "1" input to the "OR"

gate maintains the output of the first inverter at logical "0", for as long as a logical "0" "-PSP" is applied to the other input of the "AND" gate and the output of the card is thus maintained at a logical "1" for the duration of the combined inputs. The output signals of the data cards will be maintained until start command is given. At this time, the "-PSP" will go to logical "1", thus cancelling the input logical "0" to first inverter.

(3) Circuit Description Sprocket Amplifier/Shaper PSE-A (See Figure 3-3)

When the sprocket photodiode conducts during a hole condition, the negative signal produced by the photodiode is applied to the base of emitter follower T1. T1 couples this negative signal to the base of amplifier T2, turning it on. T2 applies this signal to the Schmitt trigger shaper transistors T3 and T4. The negative going voltage at the collector of T3 is then coupled through a capacitor to the base of the emitter follower T4. Conduction in T4 rises with the collector current of T4 being drawn through an emitter resistor common to both transistors. The increased current through the emitter resistor results in a negative going change in the emitter potential of the first stage. The cumulative effect of any increasingly positive base potential and increasingly negative emitter potential accelerates the drop in collector current of T3. The collector potential of T3 is thereby driven further negative, and is coupled through the input resistors to the base of transistor T4, with the result that the conduction through T4 is further increased. This positive feedback effect, thus produces a rapid cutoff of the first stage while similarly abruptly driving the second stage towards saturation.

The effect of the Schmitt trigger on the input signal is to produce a rapid rise and decay time at the leading and trailing edges of the signal. Thus, the effect of the Schmitt trigger is to shape the input signal into a clean square wave. The output of the sprocket amplifier shaper PSE-A is therefore a clean negative 10 volt for a hole signal and 0 volts for a no/hole.

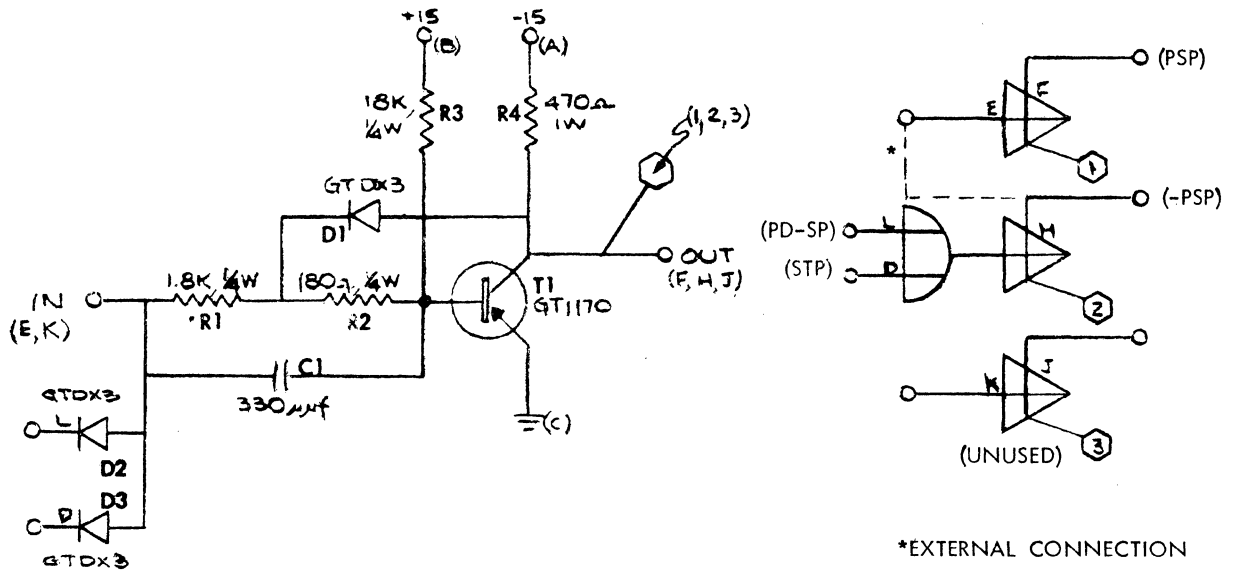
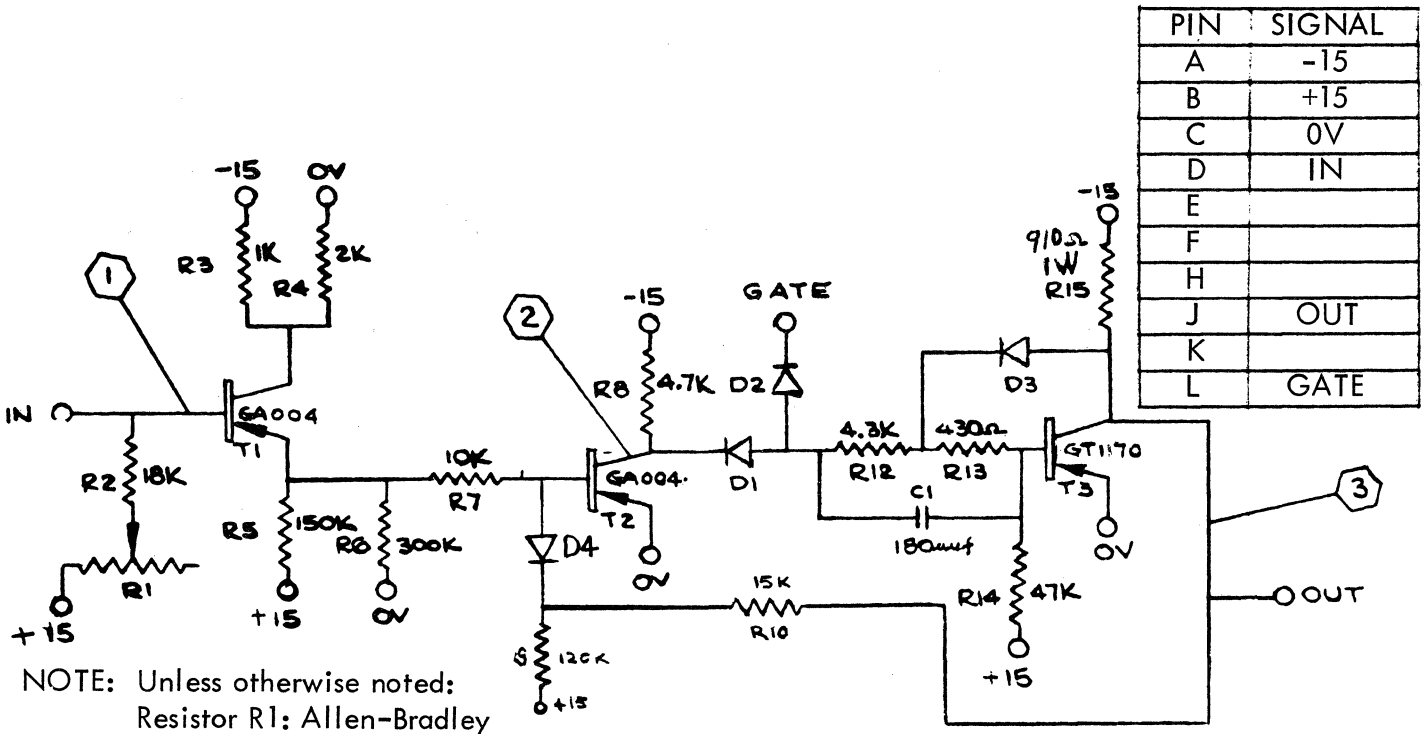


FIGURE 3-6 SCHEMATIC DIAGRAM - AAA-SCM

(4) Circuit Description Auxiliary Amplifier AAA-SCM (See Figure 3-6)

The AAA-SCM amplifier contains three separate amplifier circuits and an "OR" gate which may be wired together or used separately. When wired as shown in the block diagram (Figure 3-27, CKTB) the output of the PSE-A card ("-PSP") is applied through pin L of the "OR" gate to the inverter-amplifier. The "-PSP" output at pin H remains at 0 volts for the duration of the sprocket hole after which it returns to a negative level. This is then applied through connector J3 to the eight data channel amplifiers and to the second inverter on the AAA-SCM card. (Note table at bottom of Figure 3-27 showing wiring of plug P3.) The second inverter then produces an inverted output, -10 volts into a 1K load, for sprocket duration which is applied to the input-output connector J1 as the sprocket signal "PSP". It reverts to 0 volts for a no/hole condition.



NOTE: Unless otherwise noted:
Resistor R1: Allen-Bradley
Type RP - 200K
Resistors: 1/4W, 5%
Diodes: GTDX3

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FIGURE 3-7 SCHEMATIC DIAGRAM - PGE-A

(5) Circuit Description Data Channel Amplifiers PGE-A (See Figure 3-7)

This unit contains eight data channel amplifiers type PGE-A. Each of these amplifiers produce an output of -10 volts into a 2K load for a hole condition and 0V for a no/hole condition. These eight outputs are applied directly to the input/output jack J-1, Pins L, M, N, P, R, S, T, and V.

When any of the eight photodiodes read a hole, conduction occurs. This conduction applies a negative signal through emitter follower T1 to the base of amplifier T2, which also conducts. When T2 conducts, 0V is applied to one of the "AND" gate diodes, D1. Transistor T3 conducts when either a -10 volt ("-PSP") signal from the AAA-SCM card or -10 volt input from T2 is applied to its base, thus T3 is conducting until both the sprocket signal and T2's output goes positive. When this happens T3 cuts off applying a negative signal at the output for the duration of the combined positive inputs to the diodes.

When a stop signal is generated, the AAA-SCM card will generate "-PSP" (0V). This signal is normally the positive sprocket signal generated during a hole condition. This signal is applied through diode D2 to the base of the transistor T3. The output of the card will be maintained by the "-PSP" signal. If the card was in a no/hole condition when stop signal was generated, this 0V will be applied to the base of transistor T2 through the buffer diode D4. If the card was in a hole condition when the stop signal was generated, the negative output would be coupled through the buffer diode D4 to the base of transistor T2 holding T2 on till "-PSP" returns to a negative level. In either case the output of T2 would reflect the same output as it normally would receive from the photodiode. Thus, the output of the card would be effectively maintained even though the photodiode input was not conducting.

3-10 +10 VOLT HOLE, 0 VOLT NO HOLE OUTPUT (OPTION 1C)

This output requires the following cards:

Sprocket Channel Amplifier	PSG-A	1 each
Auxiliary Amplifier	BBB-1	1 each
Data Channel Amplifier	PGJ-A	8 each

Refer to the LOGIC OUTPUT SYSTEM BLOCK DIAGRAM (fig. 3-27) when reading the following description.

Circuit A logically represents the PSG-A sprocket amplifier and the BBB-1 auxiliary amplifier located in positions 9 and 10 of the circuit card holder on the rear of the chassis. Circuit C represents the data channel amplifier PGJ-A located in positions 1 through 8 of the circuit card holder on the reader chassis. The logical description of the two circuits follows:

NOTE

Logical "1" equal to a +level (Hole Output)
Logical "0" equal to a ground level (No/Hole Output)

(1) Logical Operation Of Sprocket Channel PSG-A and BBB-1 Amplifiers

When the sprocket photodiode reads a hole, a logical "1" signal is applied through the non-inverting amplifier (EF) to the base of the first inverter/amplifier. This stage inverts the signal to a logical "0" and applies it to a second inverter (ST). The second inverter shapes, as well as inverts the signal and applies the logical "1" signal to the input of the auxiliary amplifier card BBB-1.

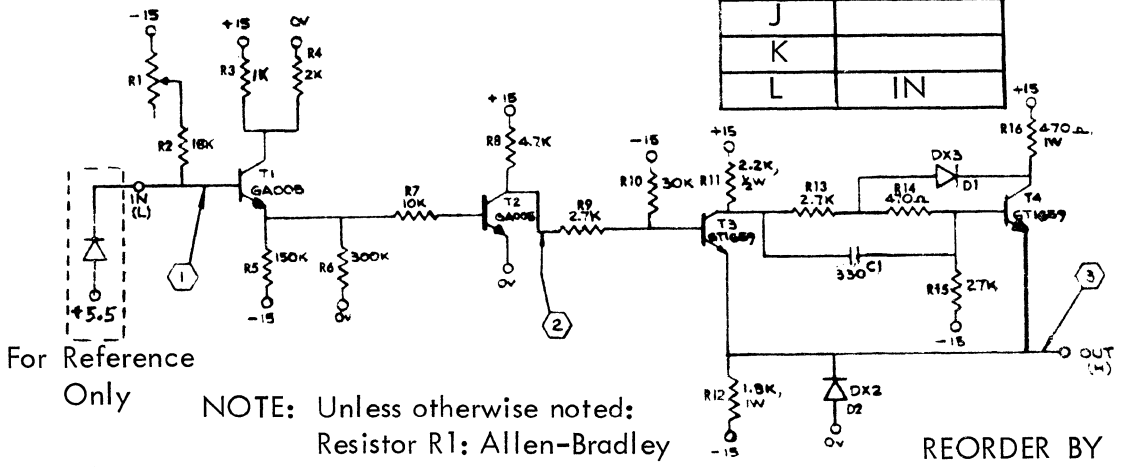
When the BBB-1 card receives the output of the PSG-A card through pin "L" (BBB-1), the signal is applied to an inverter/amplifier on the card. The logical "0" output of this inverter/amplifier is called "-PSP". This signal remains at "0" for the duration of the sprocket hole after which it reverts to a logical "1". The "-PSP" signal is then applied through connector J-3 to the eight data channel amplifiers and to the second inverter on the AAA-1 cards. (Note table at bottom of Figure 3-27 showing wiring of the J-3 plug.) The second inverter on the BBB-1 card inverts the signal and applies it as a logical "1" signal to the input/output connector J-1 as the sprocket signal "PSP". This signal remains at "1" for the duration of the sprocket hole after which it reverts to a logical "0".

The "0" level "-PSP" signal is used to shape and time the data channel output signals with the sprocket signal so that all 8 data channels start and end at the same time. The signal "PSP" may be used to gate the external equipment.

(2) Logical Operation Of Data Channel Amplifier PGJ-A

When any of the 8 data channel photodiodes reads a hole, they conduct. This applies an input logical "1" signal to the non-inverting (EF) amplifiers on the data channel PGJ-A cards. The unchanged signal is then applied to an inverter which applies a logical "0" to one of the inputs of the "OR" gates for the duration of the data hole. The logical "0" sprocket signal "-PSP" is applied to the other "OR" gate input which overrides the data channel signal. The function of the sprocket signal is to shape and time the data channel signal. The output of the gate is applied through a second inverter/amplifier to the output portion of the card and then to the input/output connector J-1. (See Figure 2-1 for location of the 8 data channel output signals on the input/output connector.) For an electrical circuit analysis of the PSG-A, BBB-1 and PGJ-A, see electrical circuit analysis following this logical description.

PIN	SIGNAL
A	+15
B	-15
C	0V
D	
E	
F	
H	OUT
J	
K	
L	IN



NOTE: Unless otherwise noted:
Resistor R1: Allen-Bradley
Type RP - 200K
Resistors: 1/4W, 5%
Diodes: GTDX3

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P.C. ASSEMBLY #B-C1399

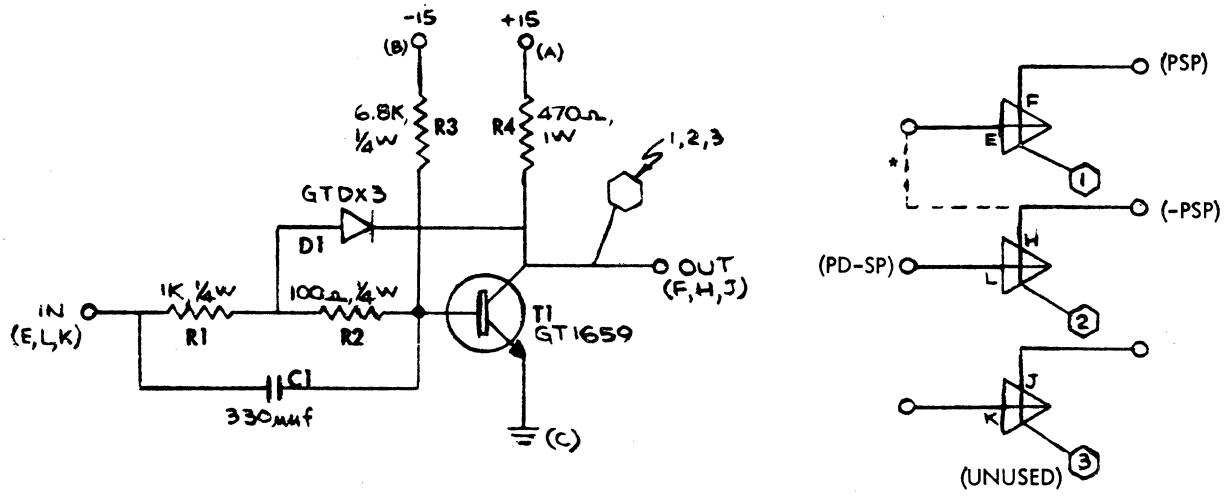
FIGURE 3-11 SCHEMATIC DIAGRAM - PSG-A

(3) Circuit Description Sprocket Amplifier/Shaper PSG-A (See Figure 3-11)

When the sprocket photodiode conducts during a hole condition, the positive signal produced by the photodiode is applied to the base of emitter follower (EF) T1. T1 couples this positive signal to the base of amplifier T2, turning it on. T2 applies this signal to the Schmitt (ST) trigger shaper transistors T3 and T4. The positive going voltage at the collector of T3 is coupled through a capacitor to the base of the emitter follower T4. Conduction in T4 rises with the collector current being drawn through the emitter resistor common to both transistors. The increased current through this emitter resistor results in a positive going charge in the emitter potential of the first stage. The cumulative

effect of an increasingly negative base potential and an increasingly positive emitter potential accelerates the drop in collector current of T3. The collector potential of T3 is thereby driven further positive, and is coupled through the input resistors to the base of transistor T4 with the result that the conduction through T4 is further increased. This positive feedback effect thus produces a rapid cutoff of the first stage while similarly abruptly driving the second stage towards saturation.

The effect of the Schmitt trigger on the input signal is to produce a rapid rise and decay time at the leading and trailing edges of the signal. Thus the effect of the Schmitt trigger is to shape the input signal into a clean square wave. The output of the sprocket amplifier shaper PSG-A is therefore a clean positive level for a hole signal and 0 volts for a no/hole condition.



3 AMPLIFIERS PER MODULE
PRINTED CIRCUIT ASSY #B-C699

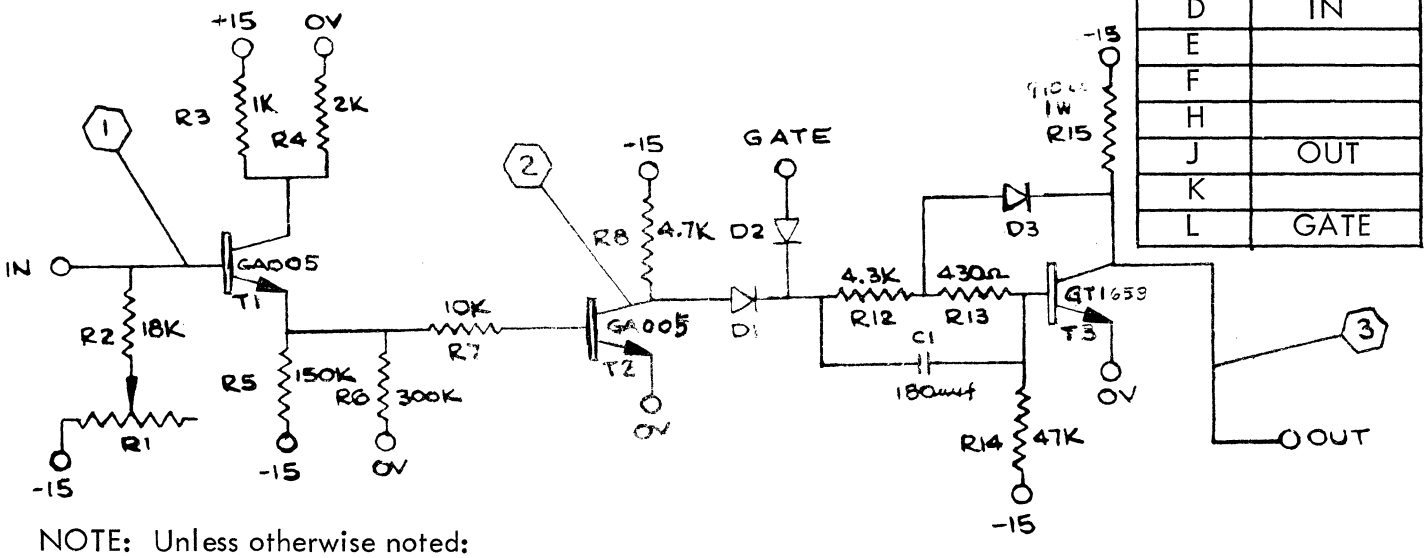
FIGURE 3-12 SCHEMATIC DIAGRAM - BBB-1

(4) Circuit Description Auxiliary Amplifier BBB-1 (See Figure 3-12)

This auxiliary amplifier, BBB-1, contains three separate circuits which may be wired together or used individually in this application only two circuits are used . When wired as shown in the block diagram Figure 3-27, the output of the PSG-A card is applied through pin "L"

to the base of one of the transistors. This signal turns on the transistor producing the 0 volt output, "-PSP". This output is coupled to the 8 data channel amplifiers and to the next amplifier on the card. When this signal is applied to the second amplifier, which is normally conducting, the transistor turns off producing signal "PSP". This signal, "PSP", is capable of delivering a 10 ma at +10 volts into a 1K load.

PIN	SIGNAL
A	-15
B	+15
C	0V
D	IN
E	
F	
H	
J	OUT
K	
L	GATE



NOTE: Unless otherwise noted:
Resistor R1: Allen-Bradley
Type RP - 200K
Resistors: 1/4W, 5%
Diodes: GTDX3

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FIGURE 3-13 SCHEMATIC DIAGRAM -PGJ-A

(5) Circuit Description Data Channel Amplifier PGJ-A (See Figure 3-13)

This unit contains eight data channel amplifiers. Each of these amplifiers, (Figure 3-13), produce an output of +10 volts into a 2K load for a hole condition and 0V for a no/hole condition. These eight outputs are applied directly to the input/output connector J-1, pins L, M, N, P, R, S, T, and U.

When any of the eight photodiodes read a hole, they conduct. This conduction applies a positive signal through emitter follower T1 to the base of amplifier T2, which also conducts. When T2 conducts, zero volts is applied to the plate of diode D1.

Transistor T3 will conduct until both a negative (0V) sprocket signal from the BBB-1 card and a 0V output from T2 are coincident at the junction of the two "AND" gate diodes, D1 and D2. When this occurs, T3 cuts off applying +10V at the output for the duration of the combined 0V inputs to the diodes. The sprocket hole is smaller than the data hole, therefore, the duration of the sprocket signal is shorter than that of the data signal. This causes the data signal to be gated by the sprocket signal. All eight data channel amplifiers receive the same sprocket signal. This assures that all data outputs will initiate and terminate at the same time.

3-11 0 VOLT HOLE, -10 VOLT NO HOLE OUTPUT (OPTION 1D)

This type output requires the following cards:

Sprocket Channel Amplifier	PSF-A	1 each
Auxiliary Amplifier	AAA-2	1 each
Data Channel Amplifier	PGH-A	8 each

Refer to the BLOCK DIAGRAM LOGIC SYSTEM (fig. 3-27) when reading the following description.

Circuit A logically represents the PSF-A sprocket amplifier and the AAA-2 auxiliary amplifier located in positions 9 and 10 of the circuit card holder on the reader chassis. Circuit E represents the data channel amplifier PGH-A located in positions 1 through 8 of the circuit card holder on the reader chassis. The logical description of the two circuits follow:

NOTE

Logical "1" equal to a -level (No/Hole Output)
Logical "0" equal to a ground level (Hole Output)

(1) Logical Operation Of PSF-A and AAA-2 Cards

When the sprocket photodiodes read a hole, a logical "0" signal is applied through the non-inverting amplifier (EF) to the base of the first inverter/amplifier. This first stage inverts the signal to a logical "1" and applies it to the second inverter (ST). The second inverter shapes, as well as inverts the signal and applies the logical "0" signal to the input of the auxiliary amplifier card AAA-2.

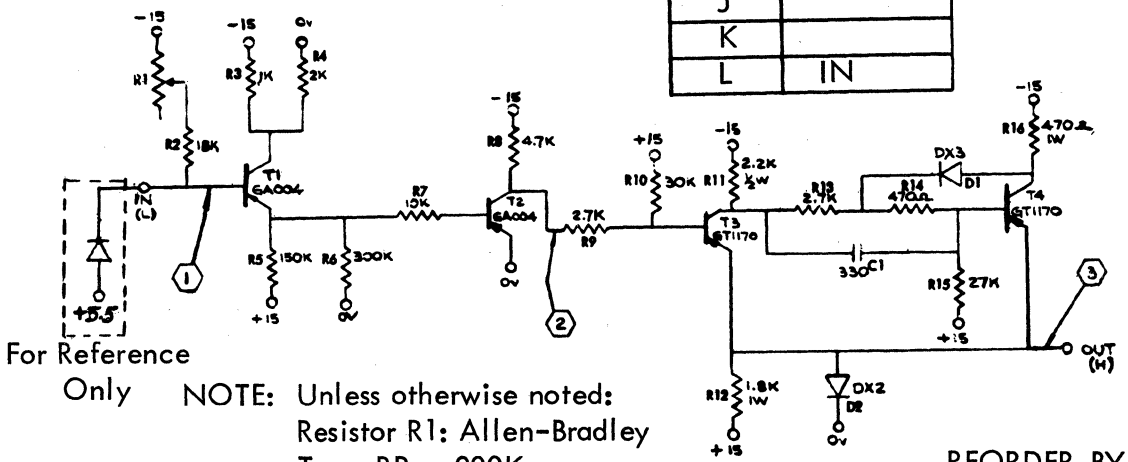
When the AAA-2 card receives the output of the PSF-A card through pin "L", the signal is applied to an inverter/amplifier on the AAA-2 card. The logical "1" output of this inverter/amplifier is called "-PSP". This signal remains at "1" for the duration of the sprocket hole after which it reverts to a logical "0". "-PSP" is then applied through connector J3 to the eight data channel amplifiers and to the second inverter on the AAA-2 cards. (Note table at bottom of Figure 3-27 showing wiring of the P3 plug.) The second inverter on the AAA-2 card inverts the signal and applies it as a logical "0" signal to the input/output connector J1 as the sprocket signal "PSP". This signal remains at "0" for the duration of the sprocket hole after which it reverts to a logical "1". The "-PSP" signal is used to shape and time the data channel output signals with the sprocket signal so that all 8 data channels start and end at the same time. The signal "PSP" may be used to gate external equipment.

(2) Logical Operation Of Data Channel Amplifier PGH-A

When any of the 8 data channel photodiodes read a hole, they conduct. This applies an input logical "0" signal to the non-inverting amplifiers on the data channel PGH-A cards. The unchanged signal is then applied to an inverter which applies a logical "1" to one of the inputs of the "AND" gate for the duration of the data hole.

The logical "1" sprocket signal "-PSP" is applied to the other "AND" gate input which overrides the data channel signal. The function of the sprocket signal is to shape and time the data channel signal. The output of the gate is applied through a second inverter/amplifier to the output portion of the card and then to the input/output connector J1. (See Figure 2-1 for location of the 8 data channel output signals on the input/output connector.) For an electrical circuit analysis of the PSF-A, AAA-2, and PGH-A, see electrical circuit analysis following this logical description.

PIN	SIGNAL
A	-15
B	+15
C	0V
D	
E	
F	
H	OUT
J	
K	
L	IN



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NOTE: Unless otherwise noted:
Resistor R1: Allen-Bradley
Type RP - 200K
Resistors: 1/4W, 5%
Diodes: GTDX3

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FIGURE 3-8 SCHEMATIC DIAGRAM - PSF-A

(3) Circuit Description Sprocket Amplifier/Shaper PSF-A (See Figure 3-8)

When the sprocket photodiode conducts during a hole condition, the positive signal produced by the photodiode is applied to the base of emitter follower (EF) T1. T1 couples this signal to the base of amplifier T2, turning it off. T2 applies a negative signal to the Schmitt trigger (ST) shaper transistors T3 and T4. The positive going voltage at the collector of T3 is coupled through a capacitor to the base of T4. Conduction in T4 decreases with the collector current being drawn through an emitter resistor common to both transistors. The decreased current through this common emitter resistor results in a positive going change in the emitter potential of the first stage. The cumulative effect of an increasingly negative base potential on T3 and increasingly positive emitter potential, accelerates the drop in collector of T3. The collector potential of T3 is thereby driven

further positive and is coupled through the input resistors to the base of transistor T4 with the result that the conduction through T4 is further decreased. This positive feedback effect thus produces a rapid cutoff of the second stage while similarly abruptly driving the first stage towards saturation.

The effect of the Schmitt trigger on the input signal is to produce a rapid rise and decay time at the leading and trailing edges of the signal. Thus, the effect of the Schmitt trigger is to shape the input signal into a clean square wave. The output of the sprocket amplifier shaper PSF-A is therefore a clean negative level for a no/hole and 0 volts for a hole.

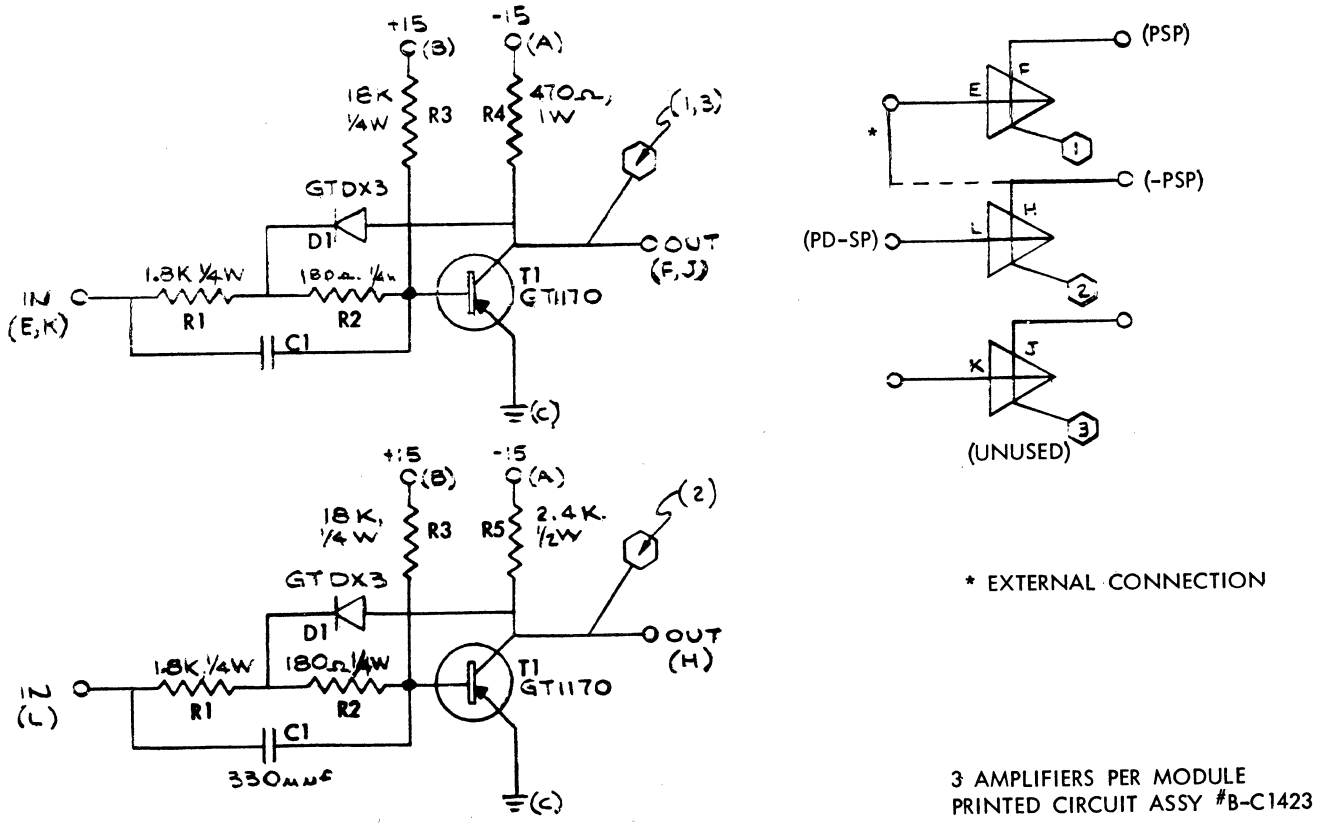
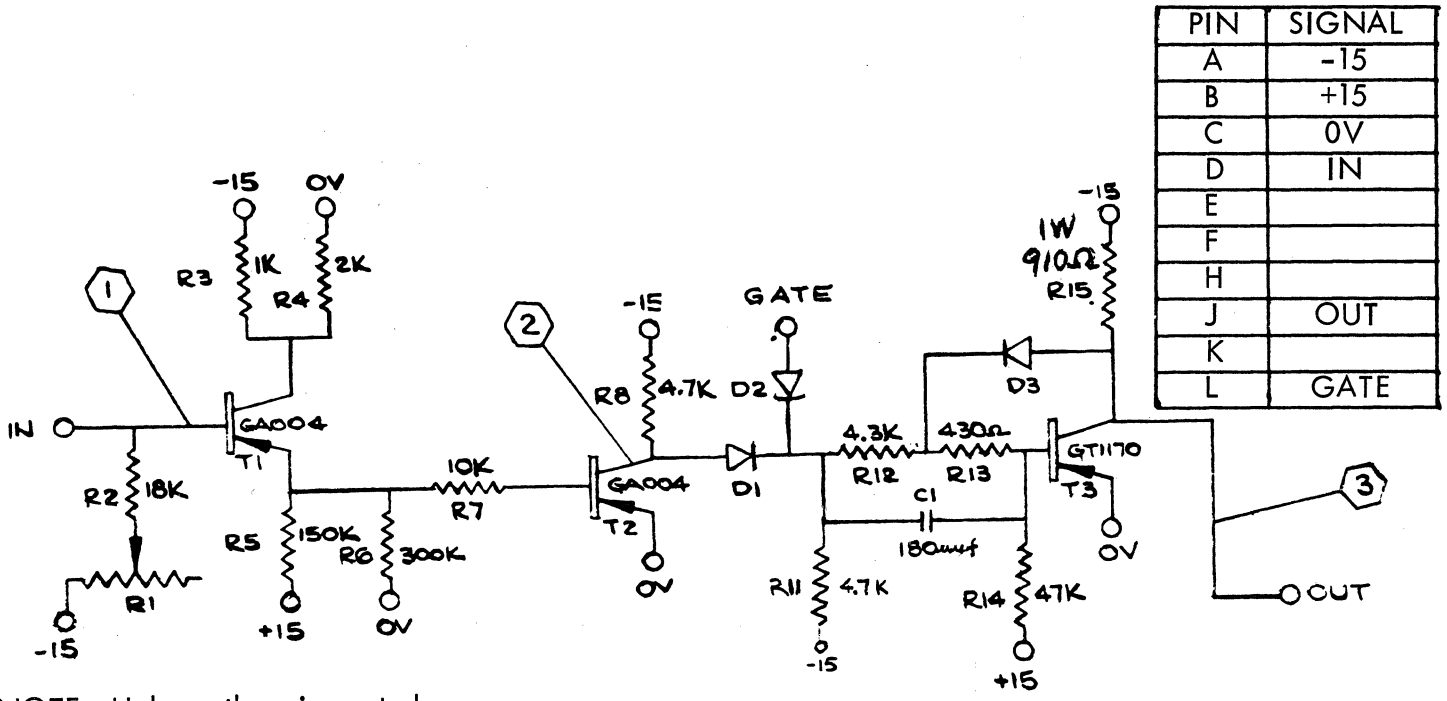


FIGURE 3-9 SCHEMATIC DIAGRAM - AAA-2

(4) Circuit Description Auxiliary Amplifier AAA-2 (See Figure 3-9)

This auxiliary amplifier, AAA-2, contains three separate circuits which may be wired together or used individually. In this application, only two circuits are used. When wired as shown in the block diagram (fig. 3-27), the output of the PSF-A card is applied through pin "L"

to the base of one of the transistors. This signal turns on the transistors. This signal turns on the transistor producing the "1" output "-PSP". This output is coupled to the 8 data channel amplifiers and to the next amplifier on the card. When this signal is applied to the second amplifier, which is normally non-conducting, the transistor turns on producing signal "PSP". The signal "PSP" is capable of supplying 10 ma at -10 volts into a 1K load for a no/hole condition.



NOTE: Unless otherwise noted:
Resistor R1: Allen-Bradley
Type RP - 200K
Resistors: 1/4W, 5%
Diodes: GTDX3

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FIGURE 3-10 SCHEMATIC DIAGRAM - PGH-A

(5) Circuit Description Data Channel Amplifier PGH-A (See Figure 3-10)

This unit contains eight data channel amplifiers (fig. 3-10). Each of these amplifiers produce an output of -10V into a 2K load for a no/hole condition and 0V for a hole condition. These eight outputs are applied directly to the input/output jack J1, pins L, M, N, P, R, S, T, and U.

When any of the eight photodiodes read a hole, conduction will occur. This conduction applies a positive signal through emitter follower T1 to the base of amplifier T2 which cuts off. When T2 cuts off, a negative voltage is applied to diode D1.

Transistor T3 will conduct only when the "1" state of "-PSP" is present at D2 and transistor T2 applies a negative signal to diode D1. Thus, T3 is cut off until both the sprocket channel amplifier and the data channel amplifiers are reading a hole. When this happens, T3 conducts applying a 0V signal at the output for the duration of the combined negative inputs to the diodes. The sprocket hole is smaller than the data hole, therefore, the duration of the sprocket signal will be shorter than the duration of the data signal. All eight data channel amplifiers receive the same sprocket signal. This assures that all data outputs will initiate and terminate at the same time.

3-12 0 VOLT HOLE, +10 VOLT NO/HOLE OUTPUT (OPTION 1E)

This type of output requires the following cards:

Sprocket Channel Amplifier	PSH-A	1 each
Auxiliary Amplifier	BBB-2	1 each
Data Channel Amplifier	PGK-A	8 each

Refer to the LOGIC OUTPUT SYSTEM BLOCK DIAGRAM(fig. 3-27) when reading the following description

Circuit A logically represents the PSH-A sprocket amplifier and the BBB-2 auxiliary amplifier located in positions 9 and 10 of the circuit card holder on the reader chassis. Circuit E represents the data channel amplifier PGK-A located in positions 1 through 8 of the circuit card holder on the reader chassis. The logical description of the two circuits follow:

NOTE

Logical "1" equal to a +level (No/Hole Output)
Logical "0" equal to a ground level (Hole Output)

(1) Logical Operation Of PSH-A and BBB-2 Cards

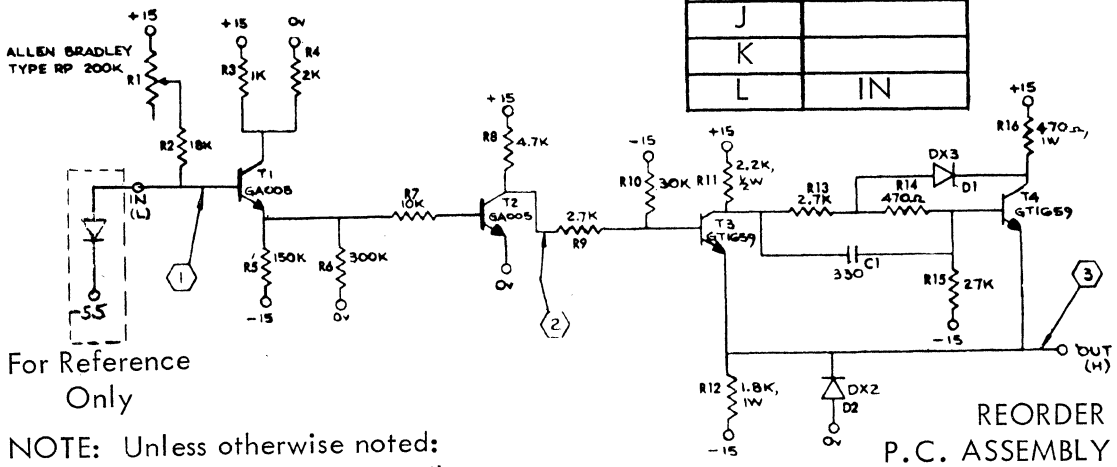
When the sprocket photodiodes read a hole, a logical "0" signal is applied through the non-inverting amplifier (EF) to the base of the first inverter/amplifier. This first stage inverts the signal to a logical "1" and applies it to the second inverter (ST). The second inverter shapes, as well as inverts the signal, and applies the logical "0" signal to the input of the auxiliary amplifier card BBB-2.

When the BBB-2 card receives the output of the PSH-A card through pin "L" (BBB-2), the signal is applied to an inverter/amplifier on the BBB-2 card. The logical "1" output of this inverter/amplifier is called "-PSP"; this signal remains at "1" for the duration of the sprocket hole after which it reverts to a logical "0". "-PSP" is then applied through connector J3 to the eight data channel amplifiers and to the second inverter on the BBB-2 card. (Note table at bottom of figure 3-27 showing wiring of the P3 plug.) The second inverter on the BBB-2 card inverts the signal and applies it as a logical "0" signal to the input/output connector J1 as the sprocket signal "PSP". This signal remains at "0" for the duration of the sprocket hole, after which it reverts to a logical "1". The "-PSP" signal is used to shape and time the data channel output signals with the sprocket signal so that all 8 data channels start and end at the same time. The signal "PSP" can be used to gate the external equipment.

(2) Logical Operation Of Data Channel Amplifier PGK-A

When any of the 8 data channel photodiodes read a hole, they conduct. This applies an input logical "0" signal to the non-inverting amplifiers (EF) on the data channel PGK-A cards. The unchanged signal is then applied to an inverter which applies a logical "1" to one of the inputs of the "AND" gate for the duration of the hole time. It is here that the sprocket signal "-PSP" is combined with the data channel signal. The function of the sprocket signal is to shape and time the data channel signal. The output of the gate is applied through second inverter/amplifier to the output portion of the card and then to the input/output connector J1. (See figure 2-1 for location of the 8 data channel signals on the input/output connector.) For an electrical circuit analysis of the PSH-A, BBB-2, and PGK-A, see electrical circuit analysis following this logical description.

PIN	SIGNAL
A	+15
B	-15
C	0V
D	
E	
F	
H	OUT
J	
K	
L	IN



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NOTE: Unless otherwise noted:
Resistor R1: Allen-Bradley
Type RP - 200K
Resistors: 1/4W, 5%
Diodes: GTDX3

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FIGURE 3-14 SCHEMATIC DIAGRAM - PSH-A

(3) Circuit Description Sprocket Amplifier/Shaper PSH-A (See Figure 3-14)

When the sprocket photodiode conducts during a hole condition, the negative signal produced by the photodiode is applied to the base of emitter follower (EF) T1. T1 couples this signal to the base of amplifier T2 turning it off. T2 applies this signal to the Schmitt trigger (ST) shaper transistors T3 and T4. The negative going voltage at the collector T3 is coupled through a capacitor to the base of the emitter follower in T4. Conduction in T4 decreases with the collector current being drawn through an emitter resistor common to both transistors. The decreased current through this emitter resistor results in a negative going change in the emitter potential of the first stage. The cumulative effect of any increasingly positive base potential and increasingly negative emitter potential accelerates the increase in collector current of T3.

The collector potential is thereby driven further negative, and is coupled through the input resistors to the base of transistor T4, with the result that the conduction thru T4 is further decreased. This positive feedback effect thus produces a rapid cutoff of the second stage while similarly abruptly driving the first stage towards saturation. The effect of the Schmitt trigger on the input signal is to produce a rapid rise and decay time at the leading and trailing edges of the sprocket signal. Thus, the effect of the Schmitt trigger is to shape the input signal into a clean square wave. The output of the sprocket amplifier shaper PSH-A is therefore a clean 0 volt for a hole signal and positive level for a no/hole condition.

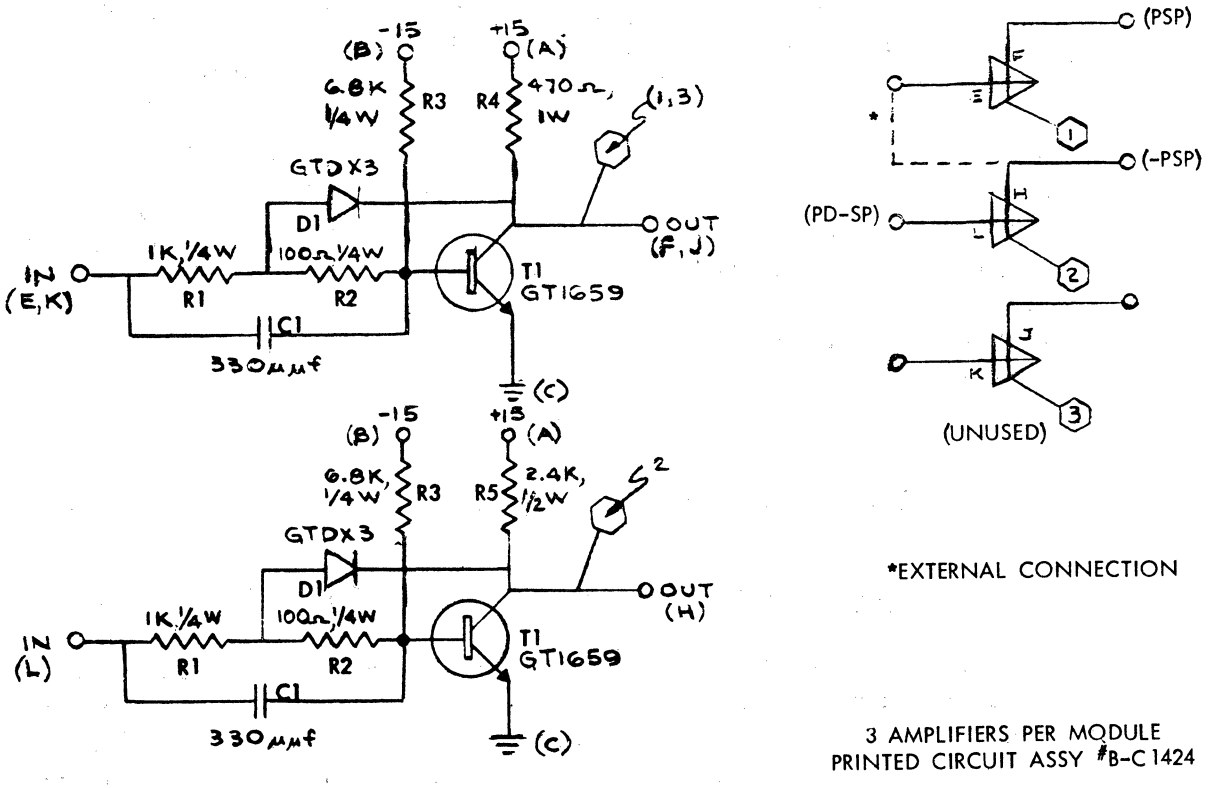
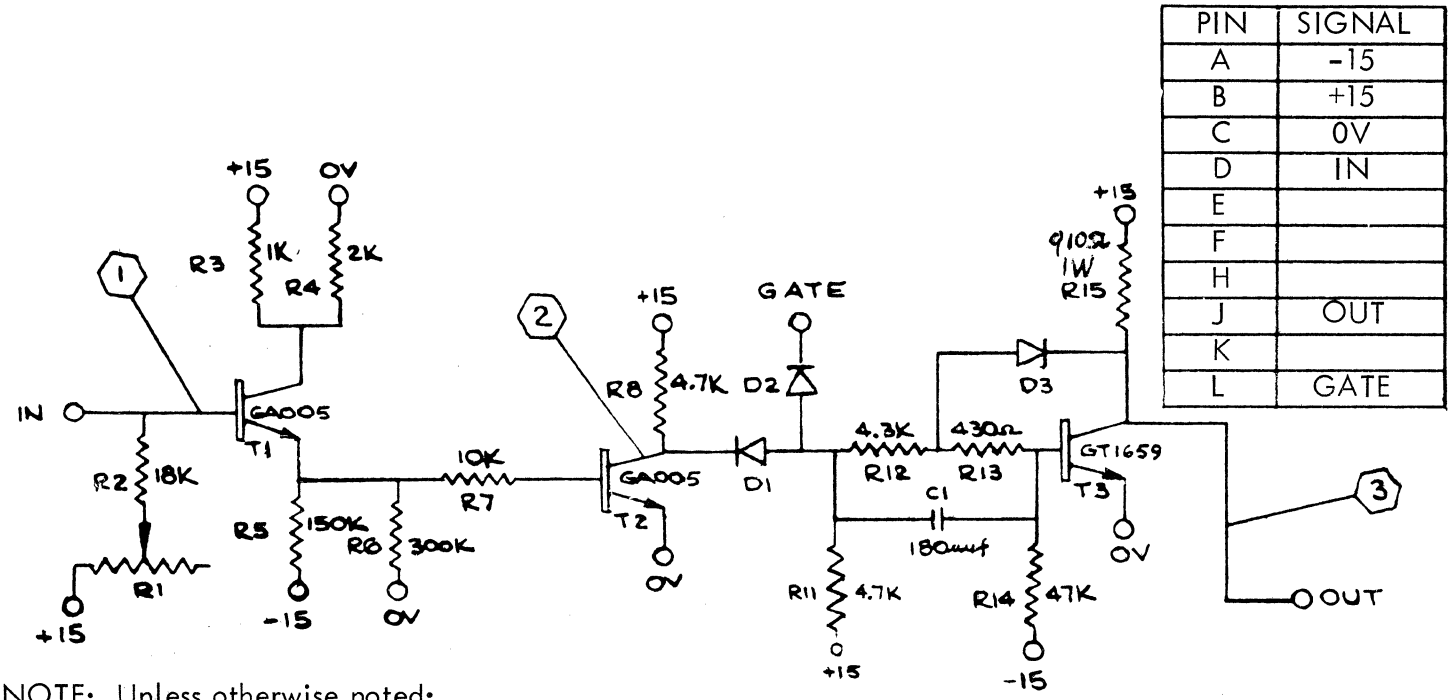


FIGURE 3-15 SCHEMATIC DIAGRAM - BBB-2

(4) Circuit Description Auxiliary Amplifier BBB-2 (See Figure 3-15)

This auxiliary amplifier, (figure 3-15), contains three separate circuits which may be wired together or used individually. When wired as shown in the block diagram, fig. 3-27 and fig. 3-15, the output of the PSH-A card is applied through pin "L" to the base of one of the

transistors. This signal turns off the transistor producing the "1" output "-PSP". This output is coupled to the 8 data channel amplifiers and to the next amplifier on the card. When this signal is applied to the second amplifier, which is normally cutoff, the transistor turns on producing signal "PSP". Signal "PSP" is capable of applying a 10 ma at -10 volts into a 1K load.



PIN	SIGNAL
A	-15
B	+15
C	0V
D	IN
E	
F	
H	
J	OUT
K	
L	GATE

NOTE: Unless otherwise noted:
Resistor R1: Allen-Bradley
Type RP - 200K
Resistors: 1/4W, 5%
Diodes: GTDX3

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FIGURE 3-16 SCHEMATIC DIAGRAM - PGK-A

(5) Circuit Description Data Channel Amplifier PGK-A (See Figure 3-16)

This unit contains eight data channel amplifiers type PGK-A (fig. 3-16). Each of these amplifiers produce an output of +10 volts into a 2K load for a no/hole condition and 0 volts for a hole condition. These eight outputs are applied directly to the input/output jack J1 pins L, M, N, P, R, S, T, and U.

When any of the eight photodiodes read a hole, it will conduct. This conduction applies a negative signal through emitter follower T1 to the base of amplifier T2 which cuts off. When T2 cuts off, a positive voltage is applied to one of the "AND" gate diodes, D1.

Transistor T3 will conduct only when a positive signal, ("-PSP"), from the BBB-2 card and a positive input from T2 is applied to the "AND" gate (D1, D2); thus T3 is cut off until both the sprocket amplifier and data amplifier are reading a hole. When this happens, T3 turns on producing 0 volt signal at the output for the duration of the combined positive inputs to the diodes. The sprocket hole is smaller than the data hole, therefore, the duration of the sprocket signal will be shorter than the data signal. This causes the data signal to be gated by the sprocket signal. All eight data channel amplifiers receive the same sprocket signal. This assures that all data outputs will initiate and terminate at the same time.

3-13 -10 VOLT HOLE, 0 VOLT NO/HOLE $^{-.2V}_{+0V}$ OUTPUT (OPTION 1F)

The reader equipped with this option contains the following cards:

Sprocket Channel Amplifier	PSE-A	1 each
Auxiliary Amplifier	AAA-3	1 each
Data Channel Amplifier	PGL-A	8 each

The operation of this option is exactly the same as the operation of option 1A with the exception of the logical "0" (0 volt) level. This option, 1F, maintains a tolerance of -.2 volts, +0 volts for any logical "0" produced as an output from the reader. With this exception in mind, turn to the description of option 1A and use it as the theory of operation for your machine.

3-14 MOTION CONTROL SYSTEM

The following paragraphs describe the various options of the Motion Control System. Refer to Figure 3-26, MOTION CONTROL BLOCK DIAGRAM, while referring to the paragraphs which follow.

3-15 UNI-DIRECTIONAL - STANDARD CONTROL (OPTION 2A)

The reader equipped with this option contains the following cards:

CARD NOMENCLATURE	CARD LOCATION
Start/Stop Amplifier SSA	In card slot #13
Run/Stop Flip-Flop FRA	In card slot #14
Power Amplifier SDC	In card slot #15
Coil Driver SPA-A-UNI	Large card under chassis

Refer to Figure 3-26, MOTION CONTROL BLOCK DIAGRAM.

There are two input signals which may be applied to the tape drive system through connector J1: RUN, this signal moves tape; and STOP, this signal halts tape.

When an input signal is applied through connector J1 to the SSA card, (figure 3-17), an output is applied to the start/stop flip-flop FRA. The dual outputs of the FRA card, (figure 3-18), are combined in the power amplifier SDC, (figure 3-24), and applied through the coil driver SPA-A-UNI, (figure 3-25). The coil driver is used to activate either the drive or brake solenoid and hold the coil de-activated. As a result, two conditions may be produced: RUN and STOP. These conditions are described below:

NOTE

The voltage equivalents of the logic levels used in the description below are 0 volts for a logical "0" and a negative level (approx. -6 volts) for a logical "1". For trouble shooting, convert logic levels to voltage levels to determine proper voltage levels at the test points.

(1) RUN

When a logical "0" signal is applied to pin "Y" or pin "Z" of connector J1, the start/stop amplifier, SSA, will produce a logical "1" output at pin "E". This "1" output is applied to the FRA flip-flop at "D".

When the FRA card receives the logical "1" output from the SSA card, the dual outputs of the FRA card are "1" at "F" and "0" at "H". This set of signals allows tape to RUN.

The dual outputs of the FRA card are combined in the power amplifier SDC and applied through the coil driver SPA-A-UNI. The coil driver applies a logical "0" to one side of the pinch roller solenoid through pin "Y" while holding the other side of the coil at a logical "1". At the same time, the SPA-A-UNI card also applies a logical "1" level to both sides of the brake coil to hold it de-activated.

NOTE

The outputs of the SPA-A are the only points where a logical "1" equals -30 volts and not -6 volts.

(2) STOP

When a logical "0" signal is applied to pin "a" and "b" of connector J1, the start/stop amplifier SSA will produce a logical "1" at pin "J". This "1" output is applied to the FRA flip-flop at "L".

When the FRA card receives the logical "1" output from the SSA card, the dual outputs of the FRA card are "0" at "F" and "1" at "H". This set of signals causes tape to STOP.

The dual outputs of the FRA are combined in the power amplifier, SDC, and applied through the coil driver SPA-A-UNI. The coil driver applies a logical "0" to one side of the brake solenoid through pin "X" while holding the other side of the coil at a logical "1". At the same time, the SPA-A-UNI card also applies a logical "1" level to both sides of the pinch roller solenoid coil to hold it de-activated.

Preset - This signal is generated only at initial turn on. The -15 volt pulse, 100 microseconds in duration, is generated on the SPA-A card and applied through pin "J" of the FRA card. The net result is to produce a STOP condition (see above) which will allow the capstan drive motor to come up to speed.

3-16 UNI-DIRECTIONAL - ONE LINE CONTROL (OPTION 2B)

The reader equipped with this option contains the following cards:

CARD DESCRIPTION	CARD LOCATION
Start/Stop Amplifier SSA	In card slot #13
Run/Stop Flip-Flop FRA-D	In card slot #14
Power Amplifier SDC	In card slot #15
Coil Driver SPA-A-UNI	Large card under chassis

Refer to Figure 3-26, MOTION CONTROL BLOCK DIAGRAM.

There are two signals which must be applied to the reader. Both input signals are applied through pin "Y" of connector J1. The input line to connector J1 pin "Y" will vary from logical "1" to "0" to produce the following conditions: RUN level equal to logical "0" at pin "Y"; STOP level equal to a logical "1" at pin "Y". The input must be a DC level.

When an input signal is applied through J1 to start/stop amplifier SSA, (figure 3-17), an output is applied to the control flip-flop FRA-D, (figure 3-19). The dual outputs of the FRA-D card are applied through the solenoid power amplifier SDC, (figure 3-24), to the coil driver SPA-A-UNI. The outputs of the SPA-A-UNI, (figure 3-25), card are used to activate the drive or brake solenoids. As a result, two conditions may be produced: RUN and STOP. These conditions are described below:

NOTE

The voltage equivalents of the logic levels used in the description below are 0 volts for a logical "0" and a negative level (approx. -6 volts) for a logical "1". For trouble shooting, convert logic levels to voltage levels to determine proper voltage levels at the test points.

(1) RUN

When a logical "0" signal is applied to pin "Y" of connector J1, the start/stop amplifier SSA will produce a logical "1" output at "E". This "1" output is applied to the FRA-D flip-flop at "D".

The FRA-D is not a true flip-flop since it does not maintain the signal applied to its inputs once that signal has been removed. Therefore, when a signal is applied to pin "D", the outputs will be maintained only for the duration of the input signal.

When the FRA-D card receives a logical "1" at pin "D", the dual outputs at "F" and "H" are "1" at "F" and "0" at "H". This set of signals is applied to the power amplifier SDC.

When the SDC card receives the signals from the FRA-D card, they are combined and applied through the coil driver SPA-A-UNI. The coil driver applies a logical "0" to one side of the pinch roller solenoid through pin "Y" while holding the other side of the coil at a logical "1". This activates the pinch roller solenoid. At the same time, the SPA-A-UNI card also applies a logical "1" level to both sides of the brake coil to hold it de-activated.

NOTE

The outputs of the SPA-A card are the only points where a logical "1" equals -30 volts and not -6 volts.

(2) STOP

When a logical "1" signal is applied to pin "Y" of connector J1, the start/stop amplifier SSA will produce a logical "0" output at "E". This logical "0" is applied to the FRA-D card at "D".

When the FRA-D card receives the logical "1" signal from the SSA card, the dual outputs of the FRA-D card are "0" at "F" and "1" at "H". This set of signals allows tape to STOP. The outputs of the FRA-D card are applied to the power amplifier SDC.

The signals from the FRA-D card are combined in the power amplifier SDC and applied through the coil driver SPA-A-UNI. The coil driver applies a logical "0" to one side of the brake solenoid through pin "X" while holding the other side of the coil at a logical "1". This activates the brake solenoid. At the same time, the SPA-A-UNI card also applies a logical "1" to both sides of the pinch roller solenoid coil to hold it de-activated.

Preset - This signal is generated only at initial turn on. The -15 volt pulse, 100 microseconds in duration, is generated on the SPA-A card and applied through pin "J" of the FRA-D card. The net result is to produce a STOP condition (see above) which will allow the capstan drive motor to come up to speed.

3-17 BI-DIRECTIONAL - STANDARD CONTROL (OPTION 2C)

The readers equipped with this option contain the following cards:

CARD NOMENCLATURE	CARD LOCATION
Start/Stop Amplifier SSA	In card slot #11 and 13
Forward/Reverse Flip-Flop FRB	In card slot #12
Run /Stop, Flip-Flop FRA	In card slot #14
Power Amplifier SDA	In card slot #15
Coil Driver SPA-A-BI	Large card under chassis

Refer to Figure 3-26, MOTION CONTROL BLOCK DIAGRAM

Readers equipped with this option require 3 input signals, through connector J1. Forward (FWD-DC, or FWD-PL), reverse (REV-DC, or REV-PL), and stop (ST-DC, or ST-PL). These signals are applied to the start/stop amplifier cards through connector J1 and may be applied as DC levels or as positive or negative pulses. When the external equipment applies a signal through connector J1 to the start/stop amplifiers SSA (figure 3-17) a signal is supplied to both the FRA (figure 3-18) flip-flop and the FRB flip-flop (with the exception of the stop condition at which time only the FRA card is given a signal). The FRA flip-flop is used to control STOP or RUN motion and the FRB flip-flop (figure 3-20) is used to control forward or reverse direction. Both of these cards produce 2 or more outputs. These outputs work in conjunction with each other to produce motion or stopping signals to the power amplifier SDA. The SDA amplifier (figure 3-22) is used to drive the coil driver (figure 3-25) SPA-A-BI. The power amplifier and coil driver are used to either move or stop the tape properly.

There are 4 conditions which may be produced: FORWARD RUN, FORWARD STOP, REVERSE RUN, REVERSE STOP. These signals are produced as a result of the input signals through connector J1 and result in the activation of a brake or drive solenoid while holding the other three solenoids de-activated. The four conditions are described below.

NOTE

The voltage equivalents of the logic levels used in the description below are 0 volts for a logical "0" and a negative level (approx. -6 volts) for a logical "1". For trouble shooting, convert logic levels to voltage levels to determine proper voltage levels at the test points.

(1) FORWARD RUN

When a logical "0" signal is applied to pin "Y" or pin "Z" to connector J1, the start/stop amplifier will produce a logical "1" output. This logical "1" output is applied to both the FRA and the FRB flip-flops at "D" of the FRA card and at "D" of the FRB card.

When the FRA card receives the logical "1" signal from the SSA card, the dual outputs at "F" and "H" are "1" at "F" and "0" at "H". This set of signals allows tape to RUN.

When the FRB card receives a logical "1" signal from "E" of the SSA card and a logical "1" from the FRA card, the three outputs of the flip-flop at "E", "F", and "K" are "0" at "E", "0" at "F", and "1" at "K". The set of signals is applied to the power amplifier SDA and the coil driver SPA-A-BI.

When the SDA power amplifier receives the signals from the FRA and FRB card, they are combined and applied through the coil driver SPA-A-BI. The coil driver SPA-A-BI applies a logical "0" to one side of the forward drive (pinch roller) solenoid through pin "Y" while holding the other side of the coil at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse brake solenoid, reverse drive solenoid, and forward brake solenoid to hold them de-activated.

NOTE

The outputs of the SPA-A are the only points where a logical "1" equals -30 volts and not -6 volts.

(2) FORWARD STOP

When a logical "0" signal is applied to pin "a" or pin "b" of connector J1, the start/stop amplifier SSA will produce a logical "1" output. This logical "1" signal is applied only to the FRA card at pin "L".

When the FRA card receives the logical "1" signal from the SSA card #13, the dual outputs at "F" and "H" are "0" at "F" and "1" at "H". This set of signals is applied to the power amplifier SDA and to the forward reverse flip-flop FRB.

To maintain a forward direction, the FRB card must have been in the FORWARD RUN condition prior to stop initiation. The FRB card receives a logical "0" signal at "L" from the FRA card. When this happens, the outputs at "E", "F", and "K" are "1" at "E", "0" at "F" since one of the inputs to the "OR" gate is at "1", and "1" at "K". This set of signals is applied to the power amplifier SDA and the coil driver SPA-A-BI.

When the SDA power amplifier receives the signals from the FRA and FRB cards, they are combined and applied through the coil driver SPA-A-BI.

The coil driver SPA-A-BI applies a logical "0" to one side of the forward brake solenoid through pin "X" while holding the other side at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse drive (pinch roller) solenoid, forward drive (pinch roller) solenoid, and reverse brake solenoid to hold them de-activated.

Preset - This signal is generated only at initial turn on. The -15 volt pulse, 100 microseconds in duration, is generated on the SPA-A card and applied through pin "J" of the FRA card. The net result is to produce a STOP condition (see above) which will allow the capstan drive motor to come up to speed.

(3) REVERSE RUN

When a logical "0" signal is applied to pin "W" or pin "X" of connector J1, the start/stop amplifier SSA will produce a logical "1" output. This logical "1" signal is applied to both the FRA and the FRB flip-flops at "E" of the FRA and "J" of the FRB.

When the FRA card receives a logical "1" signal from the SSA card #11, the dual outputs of the FRA card at "F" and "H" are "1" at "F" and "0" at "H". This set of signals is applied to the power amplifier SDA and the forward reverse flip-flop FRB.

When the FRB card receives a logical "1" from the SSA card and a logical "1" from the FRA card, the three outputs at "E", "F", and "K" are "1" at "E", "0" at "F" through the "1" at input "L", and "0" at "K". This set of signals is applied to the power amplifier SDA and the coil driver SPA-A-BI.

When the SDA power amplifier receives the signals from the FRA and FRB card, they are combined and applied through the coil driver SPA-A-BI.

The coil driver SPA-A-BI applies a logical "0" to one side of the reverse drive (pinch roller) solenoid through pin "S" while holding the other side of the coil at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse brake solenoid, forward drive solenoid, and forward brake solenoid to hold them de-activated.

(4) REVERSE STOP

When a logical "0" signal is applied to pin "a" or pin "b" of connector J1, the start/stop amplifier SSA will produce a logical "1" output. This logical "1" signal is applied only to the FRA card at pin "L".

When the FRA card receives the logical "1" signal from the SSA card #13, the dual outputs at "F" and "H" are "0" at "F" and "1" at "H". This set of signals is applied to the power amplifier SDA and to the forward/reverse flip-flop FRB.

To maintain a reverse direction, the FRB card must have been in the REVERSE RUN condition prior to stop initiation. The FRB card receives a logical "0" signal at "L" from the FRA card. When this happens the outputs at "E", "F", and "K" are "1" at "E", "1" at "F" since both inputs to the "OR" gate are at "0", and "1" at "K". This set of signals are applied to the power amplifier SDA and the coil driver SPA-A-BI.

When the SDA power amplifier receives the signals from the FRA and FRB cards, they are combined and applied through the coil driver SPA-A-BI.

The coil driver SPA-A-BI applies a logical "0" to one side of the reverse brake solenoid through pin "R" while holding the other side at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse drive (pinch roller) solenoid, forward drive (pinch roller) solenoid, and forward brake solenoid to hold them de-activated.

3-18 BI-DIRECTIONAL - TWO LINE CONTROL (OPTION 2D)

The reader equipped with this option contains the following cards:

CARD NOMENCLATURE	CARD LOCATION
Start/Stop Amplifier SSA	In card slot #11 and 13
Run /Stop Flip-Flop FRA-D	In card slot #14
Forward/Reverse Flip-Flop FRB	In card slot #12
Power Amplifier SDA	In card slot #15
Coil Driver SPA-A-BI	Large card under chassis

Refer to Figure 3-26, MOTION CONTROL BLOCK DIAGRAM.

There are two input signals which may be applied to the tape drive system through connector J1: Forward DC and Reverse DC. These signals are applied to the start/stop amplifiers through pins "W" and "Y" of J1. The signals must be applied as a pair to produce the three following combinations: "0" at "Y" with "1" at "W" (tape loop moves clockwise), and "1" at "Y" with "1" at "W" (tape loop stops from either direction).

When the external equipment applies a signal through connector J1 to the start/stop amplifier, (figure 3-17), a signal is applied to both the FRA-D flip-flop (figure 3-19) and the FRB flip-flop. The FRA-D flip-flop is used to control RUN or STOP motion and the FRB flip-flop (figure 3-20) is used to control forward or reverse direction. Both of these cards produce two or more outputs. These outputs work in conjunction with each other to produce motion or stopping signals. The FRA-D and FRB flip-flops apply their motion and direction signals to the solenoid power amplifier SDA. The SDA amplifier (figure 3-22) is used to drive the solenoid coil driver SPA-A-BI (figure 3-25). The solenoid amplifier and coil driver are used to activate the proper drive or brake solenoid which will either move or stop tape. There are 4 conditions which may be produced: FORWARD RUN, FORWARD STOP, REVERSE RUN, and REVERSE STOP.

TWO LINE CONTROL

	Motion Conditions FWD	REV	STP
DC INPUT J-1 Pin "Y"	"0"	"1"	"1"
DC INPUT J-1 Pin "W"	"1"	"0"	"1"

NOTE

The voltage equivalents of the logic levels used in the description below are 0 volts for a logical "0" and a negative level (approx. -6 volts) for a logical "1". For trouble shooting, convert logic levels to voltage levels to determine proper voltage levels at the test points.

(1) FORWARD RUN

When the DC inputs apply a logical "0" through J1 pin "Y" to "D" on the SSA #13 and a logical "1" through J1 pin "W" to "L" of SSA #11, the output of the two cards are "1" at "E" SSA #13 and "0" at "J" SSA #11. These outputs are applied to both the FRA-D and the FRB cards.

When the FRA-D card receives a "1" at "D" and a "0" at "E" the dual outputs at "F" and "H" are "1" at "F" and "0" at "H". This set of signals, when applied to the FRB and SDA cards, will allow tape to RUN.

When the FRB card receives a "1" at "D", a "0" at "J", and a "1" at "L", the three outputs at "E", "F", and "K" are "0" at "E", "0" at "F" and "1" at "K". This set of signals is applied to the power amplifier SDA and the coil driver SPA-A-BI.

When the SDA power amplifier receives the signals from the FRA and FRB card, they are combined and applied through the coil driver SPA-A-BI.

The coil driver SPA-A-BI applies a logical "0" to one side of the forward drive (pinch roller) solenoid through pin "Y" while holding the other side of the coil at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse brake solenoid, forward drive solenoid, and forward brake solenoid to hold them de-activated.

(2) FORWARD STOP

When the DC inputs to pins "Y" and "W" J1 apply a logical "1" to "D" of SSA #13 and "L" of SSA #11, the outputs of the SSA cards are "0" at "E" (SSA) #13 and "0" at "J" SSA #11. These outputs are applied to both the FRA-D and the FRB cards.

When the FRA-D card receives a "0" at input "D" and "0" at input "E", the dual outputs of the FRA-D at "F" and "H" are "0" at "F" and "1" at "H". This set of signals allows tape to STOP.

When the FRB card receives the three "0" level signals from the SSA card and the FRA-D card, the outputs of the FRB card will remain at the levels inserted during the FORWARD RUN condition, that is "0" at "E", "0" at "F", and "1" at "K". This set of signals is applied to the power amplifier SDA and the coil driver SPA-A-BI.

The coil driver SPA-A-BI applies a logical "0" to one side of the forward brake solenoid through pin "X" while holding the other side at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse drive (pinch roller) solenoid, forward drive (pinch roller) solenoid, and reverse brake solenoid to hold them de-activated.

Preset - This signal is generated only at initial turn on. The -15 volt pulse, 100 microseconds in duration, is generated on the SPA-A card and applied through pin "J" of the FRA-D card. The net result is to produce a STOP condition (see above) which will allow the capstan motor to come up to speed.

(3) REVERSE RUN

When the DC inputs at J1 pins "Y" and "W" apply a logical "1" to "D" of SSA #13 and logical "0" to "L" of SSA #11, the outputs of the SSA cards are "0" at "E" SSA #13 and "1" at "J" SSA #11. These outputs are applied to both the FRA-D and the FRB cards.

When the FRA-D card receives a "1" input at "E" and a "0" input at "D", the dual outputs of the FRA-D card at "F" and "H" are "1" at "F" and "0" at "H". This set of signals allows tape to RUN.

When the FRB card receives a "0" input at "D", a "1" input at "J", and a "1" input at "L", the three outputs of the card at "E", "F", and "K" are "1" at "E", "1" at "F", and "0" at "K". This set of signals is applied to the power amplifier SDA and the coil driver SPA-A-BI.

When the SDA power amplifier receives the signals from the FRA and FRB card, they are combined and applied through the coil driver SPA-A-BI.

The coil driver SPA-A-BI applies a logical "0" to one side of the reverse drive (pinch roller) solenoid through pin "S" while holding the other side of the coil at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse brake solenoid, forward drive solenoid, and forward brake solenoid to hold them de-activated.

(4) REVERSE STOP

When the DC inputs to J1 pins "Y" and "W" apply a "1" to "D" of SSA #13 and "L" of SSA #11, the outputs of the SSA cards are "0" at "E" SSA #13 and "0" at "J" SSA #11. These outputs are applied to both the FRA-D and the FRB cards.

When the FRA-D card receives a "0" at input "D" and a "0" at input "E", the dual output of the FRA-D at "F" and "H" are "0" at "F" and "1" at "H". This set of signals, when applied to the FRB and SDA cards, will cause tape to STOP.

To maintain a reverse direction, the FRB card must have been in the REVERSE RUN condition prior to stop initiation. The FRB card receives a logical "0" signal at "L" from the FRA card. When this happens the outputs at "E", "F", and "K" are "1" at "E", "1" at "F" since both inputs to the "OR" gate are at "0", and "1" at "K". This set of signals are applied to the power amplifier SDA and the coil driver SPA-A-BI.

When the SDA power amplifier receives the signals from the FRA and FRB cards, they are combined and applied through the coil driver SPA-A-BI.

The coil driver SPA-A-BI applies a logical "0" to one side of the reverse brake solenoid through pin "R" while holding the other side at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse drive (pinch roller) solenoid, forward drive (pinch roller) solenoid, and forward brake solenoid to hold them de-activated.

3-19 BI-DIRECTIONAL - TWO BRAKE CONTROL (OPTION 2E)

The reader equipped with this option contains the following cards:

CARD NOMENCLATURE

Start/Stop Amplifier SSA	In card slot #11 and 13
Forward/Reverse Flip-Flop FRB-H	In card slot #12
Run /Stop Flip-Flop FRA	In card slot #14
Solenoid Driver Amplifier SDA-H	In card slot #15
Solenoid Coil Driver SPA-A-BI	Large card under chassis

Refer to Figure 3-26, MOTION CONTROL BLOCK DIAGRAM.

Readers equipped with this option require 3 input signals through connector J1: forward (FWD-DC or FWD-PL), reverse (REV-DC or REV-PL), and stop (ST-DC or ST-PL). These three signals are applied to the start/stop amplifier cards. Note that the signals may be applied as DC levels or as positive going or negative going pulses.

When the external equipment applies a signal through connector J1 to the start/stop amplifiers, SSA (figure 3-17) the output signals are applied to both the FRA and FRB-H flip-flops. The FRA (figure 3-18) is used to control RUN and STOP motion and the FRB-H (figure 3-21) is used to control FORWARD and REVERSE direction. Both of these cards produce two or more outputs. These outputs work in conjunction with each other to produce motion or stopping signals. The FRA and FRB-H apply their motion and stopping signals to the solenoid power amplifier SDA-H. The SDA-H power amplifier (figure 3-24) is used to drive the solenoid coil driver SPA-A-BI. The coil driver SPA-A-BI (figure 3-25) is used to activate the proper drive and brake solenoids which will either move or stop tape. There are four conditions which may be produced: FORWARD RUN, FORWARD STOP, REVERSE RUN, and REVERSE STOP.

NOTE

The voltage equivalents of the logic levels used in the description below are 0 volts for a logical "0" and a negative level (approx. -6 volts) for a logical "1". For trouble shooting, convert logic levels to voltage levels to determine proper voltage levels at the test points.

(1) FORWARD RUN

When a logical "0" signal is applied to pin "Y" or pin "Z" of connector J1, the start/stop amplifier SSA #13 will produce a logical "1" output. This logical "1" is applied to both the FRA and FRB-H flip-flops at "D" of the FRA card and "D" of the FRB-H card.

When the FRA card receives the logical "1" signal from the SSA #13 card, the dual outputs at "F" and "H" are "1" at "F" and "0" at "H". This set of signals allows tape to RUN.

When the FRB-H card receives "1" at "D", "0" at "J", and "1" at "L", the three outputs of the flip-flop at "E", "F", and "K" are "0" at "E", "0" at "F" and "1" at "K". These signals allow tape to RUN in the forward direction.

The signals from the FRA and FRB-H cards are combined in the power amplifier SDA-H and applied through the coil driver SPA-A-BI.

The coil driver SPA-A applies a logical "0" to one side of the forward drive (pinch roller) solenoid through pin "Y" while holding the other side of the coil at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse brake solenoid, forward brake solenoid and reverse drive (pinch roller) solenoid to hold them de-activated.

NOTE

The outputs of the SPA-A are the only points where a logical "1" equals -30 volts and not -6 volts.

(2) FORWARD STOP

When a logical "0" signal is applied to either pin "a" or "b" of connector J1, the start/stop amplifier SSA #13 will produce a "1" output. This output is applied through pin "J" of the SSA #13 to pin "L" of the FRA card only.

When the FRA card receives the "1" signal from the SSA #13, the dual outputs of the FRA card at "F" and "H" are "0" at "F" and "1" at "H". This set of signals allows tape to STOP.

The FRB-H card receives the logical "0" at "L" from "F" of the FRA card. The input logical "0" is inverted and applied to output "F" of the FRB-H card. This logical "1" output at "F" is applied to the coil driver to activate the reverse brake whenever a STOP command is given. The other two outputs "E" and "K" remain at the same level set during the FORWARD RUN condition, thus, the outputs of the cards are "0" at "E", "1" at "F" and "1" at "K". The configuration of the FRB-H differs slightly from that of the standard FRB card in that the secondary line from pin "K" has been removed. (See figure 3-27, CKT. C and C1.) This line normally supplies a logical "1" which would hold the reverse brake solenoid de-energized during the forward stop condition if the line were installed.

The signals from the FRA and FRB-H are combined in the power amplifier SDA-H. The configuration of the SDA-H is slightly different from the standard SDA card in that the secondary line from pin "D" has been removed. (See figure 3-27, CKT. D1 and D2.) This line supplies a logical "1" which would hold the forward brake de-energized during the reverse stop condition if the line were installed. Thus, whenever a stop command is given, the power amplifier SDA-H and flip-flop FRB-H combine the input signals and apply these signals to the coil driver SPA-A-BI to energize both brakes simultaneously.

The coil driver SPA-A applies a logical "0" to one side of both brake solenoids through pins "X" and "R", while holding the other side of the coil at a logical "1". This activates the solenoids simultaneously. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse drive (pinch roller) solenoid and forward drive (pinch roller) solenoid to hold them de-activated.

Preset - This signal is generated only at initial turn on. The -15 volt pulse, 100 microseconds in duration, is generated on the SPA-A card and applied through pin "J" of the FRA card. The net result is to produce a STOP condition (see above) which will allow the capstan drive motor to come up to speed.

(3) REVERSE RUN

When a logical "0" is applied to pins "W" or "X" of connector J1, the start/stop amplifier SSA #11 will produce an output logical "1" at pin "J". This output is applied to both the FRA card at pin "E" and the FRB-H card at pin "J".

When the FRA card receives the logical "1" signal from the SSA card, the dual outputs of the FRA card at "F" and "H" are "1" at "F" and "0" at "H". This set of signals allows tape to RUN.

When the FRB-H card receives the logical "1" signal from SSA card #11 at pin "J" and a logical "1" from "F" of the FRA card, the three outputs of the FRB-H at "E", "F", and "K" are "1" at "E", "0" at "F", and "0" at "K". These signals allow tape to RUN in the REVERSE direction.

The signals from the FRA and FRB-H cards are combined in the power amplifier SDA-H and applied through the coil driver SPA-A-BI.

The coil driver SPA-A applies a logical "0" to one side of the reverse drive (pinch roller) solenoid through pin "S" while holding the other side of the coil at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse brake solenoid, forward brake solenoid and forward drive (pinch roller) solenoid to hold them de-activated.

(4) REVERSE STOP

When a logical "0" signal is applied to either pin "a" or "b" of connector J1, the start/stop amplifier SSA #13 will produce a logical "1" output. This output is applied through pin "J" of the SSA card #13 to pin "L" of the FRA card only.

When the FRA card receives the logical "1" signal from the SSA card #13, the dual outputs of the FRA card at "F" and "H" are "0" at "F" and "1" at "H". This set of signals causes tape to STOP.

When the FRB-H card receives the logical "0" at "L" from the FRA card, the input logical "0" is inverted and applied to output "F" of the FRB-H card. The other two outputs "E" and "K" remain at the same level set during the REVERSE RUN condition, thus, the outputs of the card are "1" at "E", "1" at "F", and "0" at "K". The logical "1" output at "F" is applied to the coil driver to energize the reverse brake whenever a STOP command is given. The configuration of the FRB-H differs slightly from that of the standard FRB card in that the secondary line from pin "D" has been removed. (See figure 3-27, CKT. C and C1.) This line normally supplies a logical "1" which would hold the reverse brake de-energized during the FORWARD STOP condition if the line were installed.

The signals from the FRA and FRB-H cards are combined in the power amplifier SDA-H. The configuration of the SDA-H is slightly different from that of the standard SDA card, (See figure 3-27, CKT. D1 and D2.), in that the secondary line from pin "D" has been removed. This line supplies a logical "1" which would hold the forward brake de-energized during the REVERSE STOP condition if the line were installed. Thus, whenever a STOP command is given, the power amplifier SDA-H and the FRB-H flip-flop combine input signals and apply these signals to the SPA-A-BI.

The coil driver SPA-A applies a logical "0" to one side of both brake solenoids through pins "X" and "R", while holding the other side of the coil at a logical "1". This activates the solenoids. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse drive (pinch roller) solenoid and forward drive (pinch roller) solenoid to hold them de-activated.

3-20 BI-DIRECTIONAL TWO LINE CONTROL & TWO BRAKE SYSTEM (OPTION 2F)

The reader equipped with this option contains the following cards:

CARD NOMENCLATURE	CARD LOCATION
Start/Stop Amplifier SSA	In card slot #11 and 13
Run /Stop Flip-Flop FRA-D	In card slot #14
Forward/Reverse Flip-Flop FRB-H	In card slot #12
Power Amplifier SDA-H	In card slot #15
Coil Driver SPA-A-BI	Large card under chassis

Refer to Figure 3-26, MOTION CONTROL BLOCK DIAGRAM.

There are two input signals which may be applied to the tape drive system through connector J1: Forward DC and Reverse DC. These signals are applied to the start/stop amplifiers through pins "W" and "Y" of J1. The signals must be applied as a pair to produce the three following combinations: "0" at "Y" with "1" at "W" (tape loop moves counterclockwise), "1" at "Y" with "0" at "W" (tape loop moves clockwise), and "1" at "Y" with "1" at "W" (tape loop stops from either direction).

When the external equipment applies the signals through connector J1 to the start/stop amplifiers, SSA (figure 3-17) the outputs are applied from SSA card #13 pin "E" and from SSA card #11 pin "J" to both the FRA-D card and the FRB-H card. The FRA-D flip-flop (figure 3-19) is used to control RUN or STOP motion while the FRB-H (figure 3-21) is used primarily to control FORWARD or REVERSE direction. Card FRB-H, in conjunction with card SDA-H, are used to activate both brakes at the same time during a STOP condition. The FRA-D and FRB-H apply motion and direction signals to the power amplifier SDA-H. The primary function of the SDA-H (figure 3-23) card is to combine motion and direction commands and apply them to the coil driver card SPA-A-BI. The coil driver SPA-A-BI (figure 3-25) is used to activate the proper drive or brake solenoids by applying ground signals (0 volts) to one side of the coil and holding the remaining solenoids de-energized. There are four conditions which may be produced as a result of applying the three combinations of input signals: FORWARD RUN, FORWARD STOP, REVERSE RUN, and REVERSE STOP.

NOTE

The voltage equivalents of the logic levels used in the description below are 0 volts for a logical "0" and a negative level (approx. -6 volts) for a logical "1". For trouble shooting, convert logic levels to voltage levels to determine proper voltage levels at the test points.

TWO LINE CONTROL

	Motion Conditions FWD	REV	STP
DC INPUT J-1 Pin "Y"	"0"	"1"	"1"
DC INPUT J-1 Pin "W"	"1"	"0"	"1"

(1) FORWARD RUN

When the DC inputs to J1 apply a logical "0" through J1 pin "Y" to "D" of card SSA #13 and logical "1" through J1 pin "W" to "L" of card SSA #11, the outputs of the two cards are "1" at "E" SSA #13 and "0" at "J" SSA #11. The outputs are applied to both the FRA-D and the FRB-H cards.

When the FRA-D card receives a "1" at "D" and a "0" at "E", the dual output at "F" and "H" are "1" at "F" and "0" at "H". This set of signals, when applied to the FRB-H and the SDA-H, will allow tape to RUN.

When the FRB-H card receives "1" at "D", "0" at "J" and "1" at "L", the three outputs at "E", "F" and "K" are "0" at "E", "0" at "F", and "1" at "K". These signals are applied to the power amplifier SDA-H and to the coil driver SPA-A-BI.

The signals from the FRA-D card and the FRB-H card are combined in the power amplifier SDA-H and applied through coil driver SPA-A-BI.

The coil driver SPA-A applies a logical "0" to one side of the forward drive (pinch roller) solenoid through pin "Y" while holding the other side of the coil at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse brake solenoid, forward brake solenoid and reverse drive (pinch roller) solenoid to hold them de-activated.

NOTE

The outputs of the SPA-A are the only points where a logical "1" equals -30 volts and not -6 volts.

(2) FORWARD STOP

When the DC inputs to J1 pins "Y" and "W" apply a logical "1" to "D" of SSA #13 and "L" of SSA #11, the outputs of the SSA cards are "0" at "E" SSA #13 and "0" at "J" SSA #11. These outputs are applied to both the FRA-D card and the FRB-H card.

When the FRA-D card receives a "0" at input "D" and a "0" at input "E", the dual output of the FRA-D at "F" and "H" are "0" at "F" and "1" at "H". This set of signals allows tape to STOP.

When the FRB-H card receives the three "0" level signals from the SSA cards and the FRA-D card, the two outputs "E" and "K" remain at the same levels set during the FORWARD RUN condition, but the level at "L" changes from "1" to "0". This input logical "0" is inverted and applied at "F" as a logical "1". The "1" output at "F" is applied to the coil driver to energize the reverse brake whenever a STOP command is given. Thus the outputs of the card are: "0" at "E", "1" at "F", and "1" at "K". The configuration of the FRB-H card differs slightly from that of the standard FRB card in that the secondary line from pin "D" has been removed. (See figure 3-27, CKT. C and C1.) This line normally supplies a logical "1" which would hold the reverse brake de-energized during the FORWARD STOP condition if the line were installed.

The signals from the FRA-D card and the FRB-H card are combined in the power amplifier SDA-H. The configuration of the SDA-H differs slightly from the standard SDA in that the secondary line from pin "D" has been removed. This line supplies a logical "1" which would hold the forward brake solenoid de-energized during the REVERSE STOP condition if the line were installed.

Whenever a STOP command is given, the signals from the FRA-D and the FRB-H are combined in the power amplifier SDA-H. The signals from the SDA-H and FRB-H are applied through the coil driver SPA-A-BI.

The coil driver SPA-A applies a logical "0" to one side of both brake solenoids through pins "X" and "R", while holding the other side of the coil at a logical "1". This activates the solenoids simultaneously. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse drive (pinch roller) solenoid and forward drive (pinch roller) solenoid to hold them de-activated.

Preset - This signal is generated only at initial turn on. The -15 volt pulse, 100 microseconds in duration, is generated on the SPA-A card and applied through pin "J" of the FRA-D card. The net result is to produce a STOP condition (see above) which will allow the capstan drive motor to come up to speed.

(3) REVERSE RUN

When the DC inputs to J1 apply a logical "1" to pin "Y" and a logical "0" to pin "W", the outputs of the two SSA cards are "1" at "J" and "0" at "E". The outputs are applied to both the FRA-D card and the FRB-H card.

When the FRA-D card receives a "0" at "D" and a "1" at "E", the dual output at "F" and "H" are "1" at "F" and "0" at "H". This set of signals, when applied to the FRB-H card and SDA-H card, will cause tape to RUN.

When the FRB-H card receives "0" at "D", "1" at "J" and "1" at "L", the three outputs at "E", "F" and "K" are "1" at "E", "0" at "F", and "0" at "K". These signals allow tape to RUN in the reverse direction.

The signals from the FRA-D card and the FRB-H card are combined in the power amplifier SDA-H and applied through the coil driver SPA-A-BI.

The coil driver SPA-A applies a logical "0" to one side of the reverse drive (pinch roller) solenoid through pin "Y" while holding the other side of the coil at a logical "1". This activates the solenoid. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse brake solenoid, forward brake solenoid and forward drive (pinch roller) solenoid to hold them de-activated.

(4) REVERSE STOP

When the DC inputs to J1 pins "Y" and "W" apply a logical "1" to "D" of SSA #13 and "L" of SSA #11, the outputs of the SSA cards are "0" at "E" SSA #13 and "0" at "J" SSA #11. These outputs are applied to both the FRA-D card and the FRB-H card.

When the FRA-D card receives a "0" at "D" and a "0" at "E", the dual output of the FRA-D at "F" and "H" are "0" at "F" and "1" at "H". The set of signals allows tape to STOP.

When the FRB-H card receives the three "0" level signals from the SSA card and the FRA-D card, the two outputs "E" and "K" remain at the same level set during the REVERSE RUN condition, but the level at "L" changes from "1" to "0". This input logical "0" is inverted and applied at "F" as a logical "1". The "1" output at "F" is applied to the coil driver SPA-A-BI to energize the reverse brake whenever a STOP command is given. Thus the outputs of the FRB-H card are: "0" at "E", "1" at "F", and "1" at "K". The configuration of the FRB-H card differs slightly from that of the standard FRB card in that the secondary line from pin "D" has been removed. (See figure 3-27, CKT. C and C1.) This line normally supplies a logical "1" which would hold the reverse brake de-energized during the FORWARD STOP condition if the line were installed.

The signals from the FRA-D card and the FRB-H card are combined in the power amplifier SDA-H. The configuration of the SDA-H, like the FRB-H, is slightly different from the standard SDA card in that the secondary line from pin "D" has been removed. This line supplies a logical "1" which would hold the forward brake solenoid de-energized during the REVERSE STOP condition if the line were installed. Thus, due to the action of the FRB-H and the SDA-H cards, both brakes will be energized whenever a STOP command is given.

The signals from the FRA-D and FRB-H are combined in the SDA-H and applied through the coil driver SPA-A-BI.

The coil driver SPA-A applies a logical "0" to one side of both brake solenoids through pins "X" and "R", while holding the other side of the coil at a logical "1". This activates the solenoids. At the same time, the SPA-A-BI also applies a logical "1" to both sides of the reverse drive (pinch roller) solenoid and forward drive (pinch roller) solenoid to hold them de-activated.

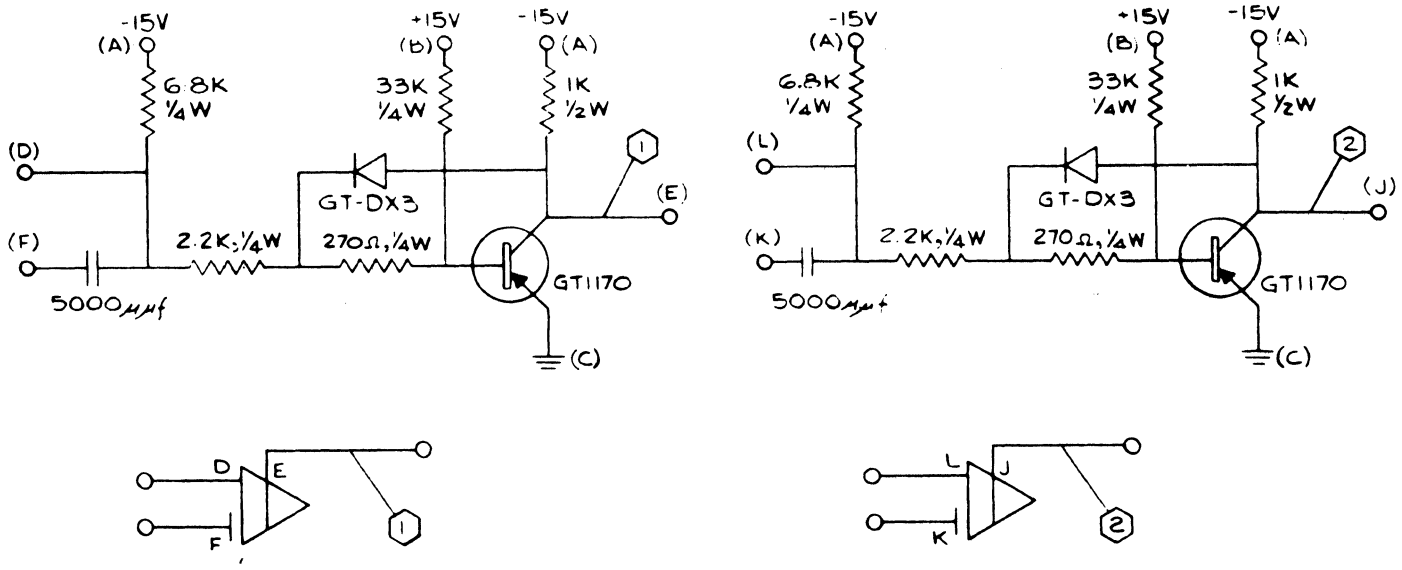


FIGURE 3-17 SCHEMATIC DIAGRAM - SSA

P.C. ASSEMBLY B-C417

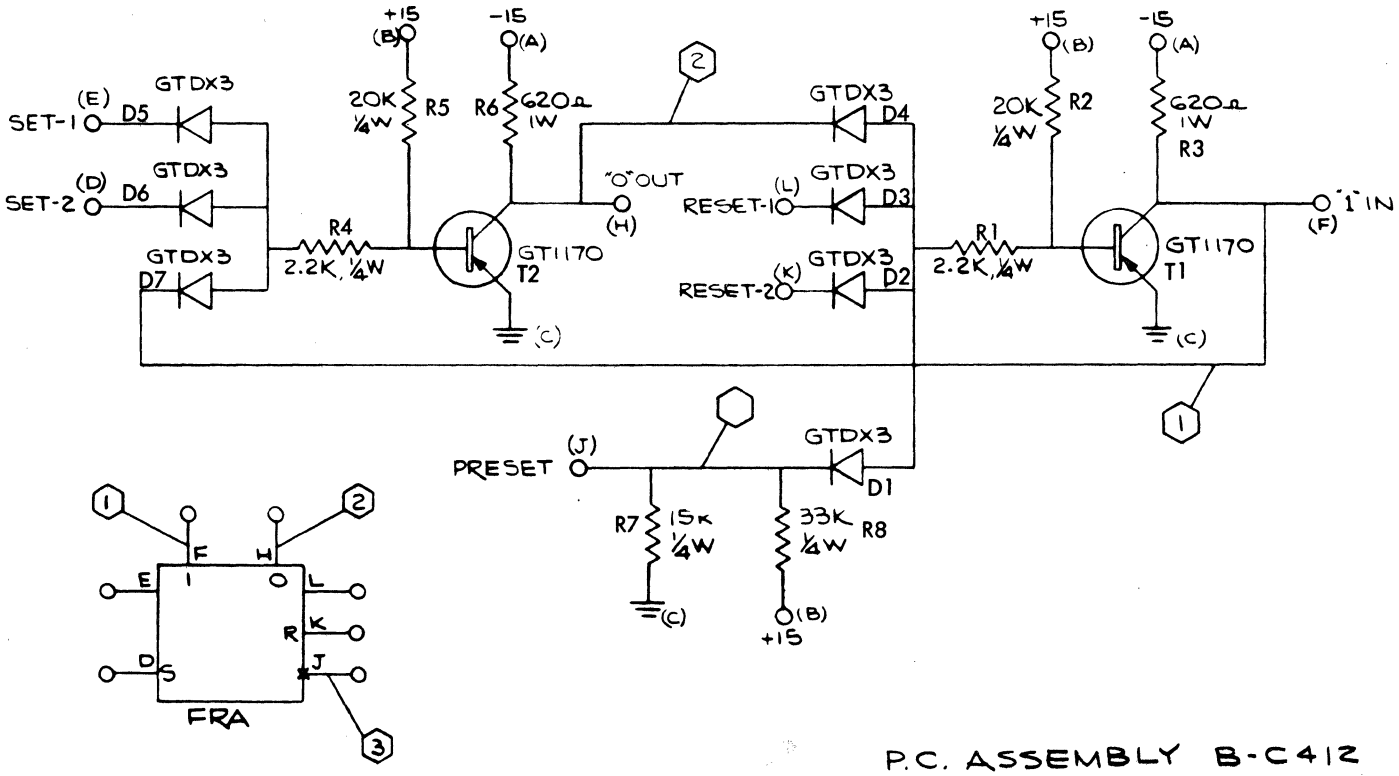


FIGURE 3-18 SCHEMATIC DIAGRAM - FRA

P.C. ASSEMBLY B-C412

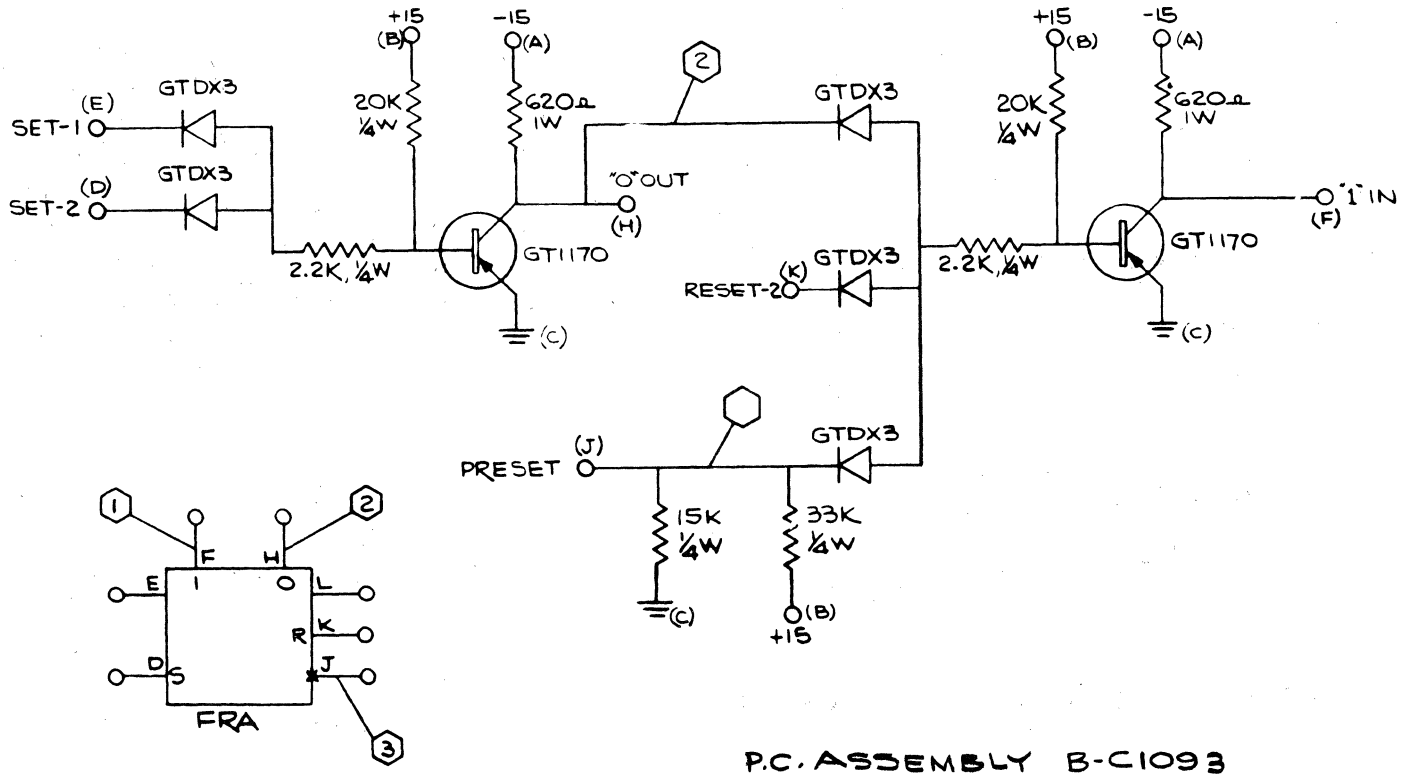


FIGURE 3-19 SCHEMATIC DIAGRAM - FRA-D

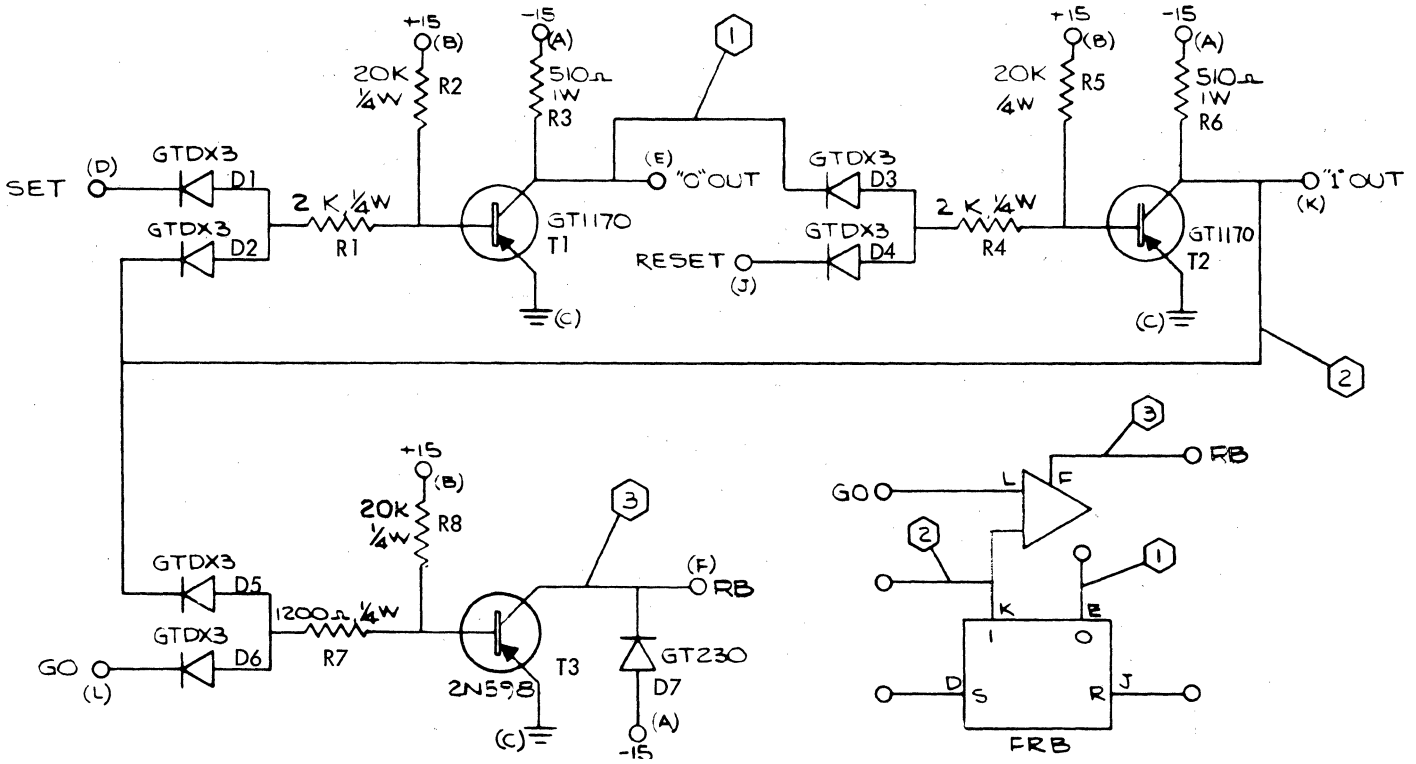


FIGURE 3-20 SCHEMATIC DIAGRAM - FRB

P.C. ASSEMBLY NO. B-C411

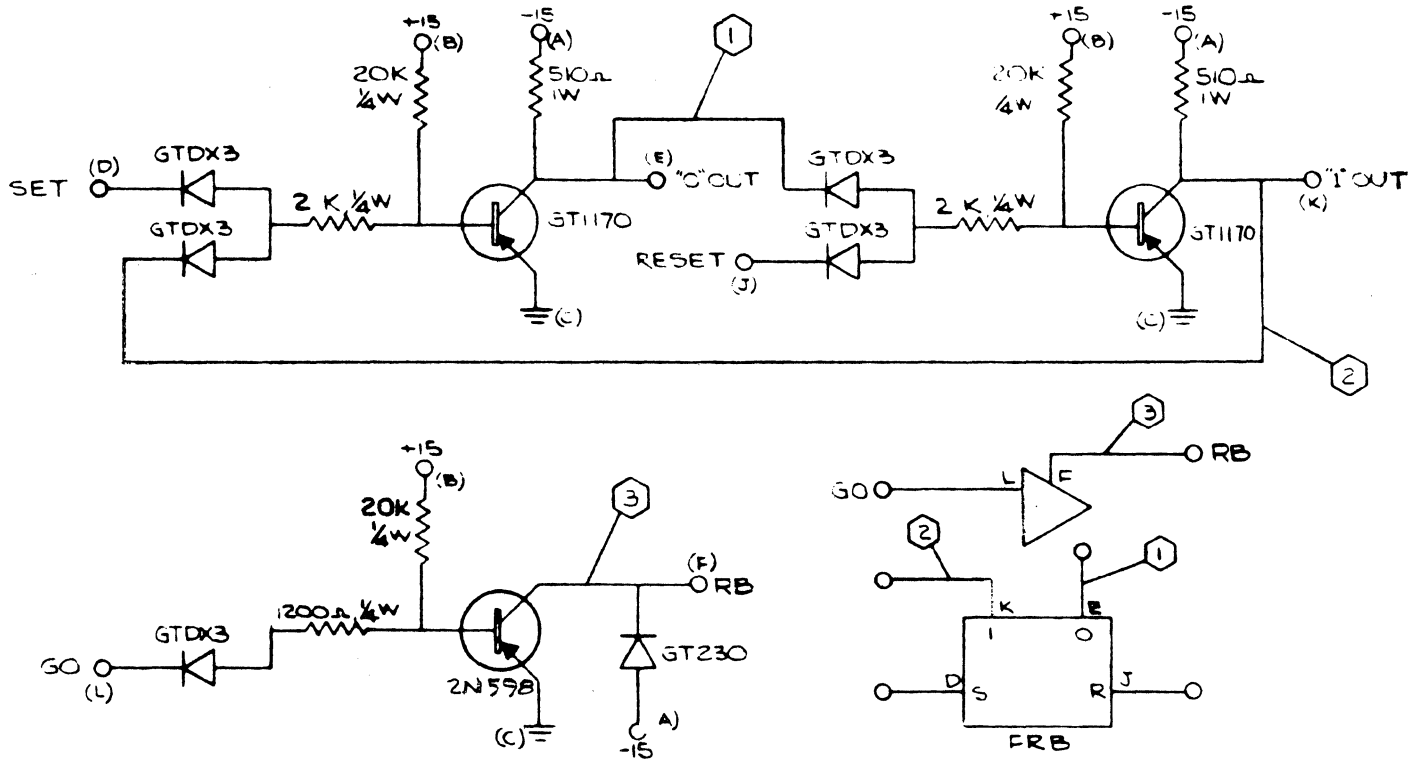


FIGURE 3-21 SCHEMATIC DIAGRAM - FRB-H

P.C. ASSEMBLY NO. B-C 1312

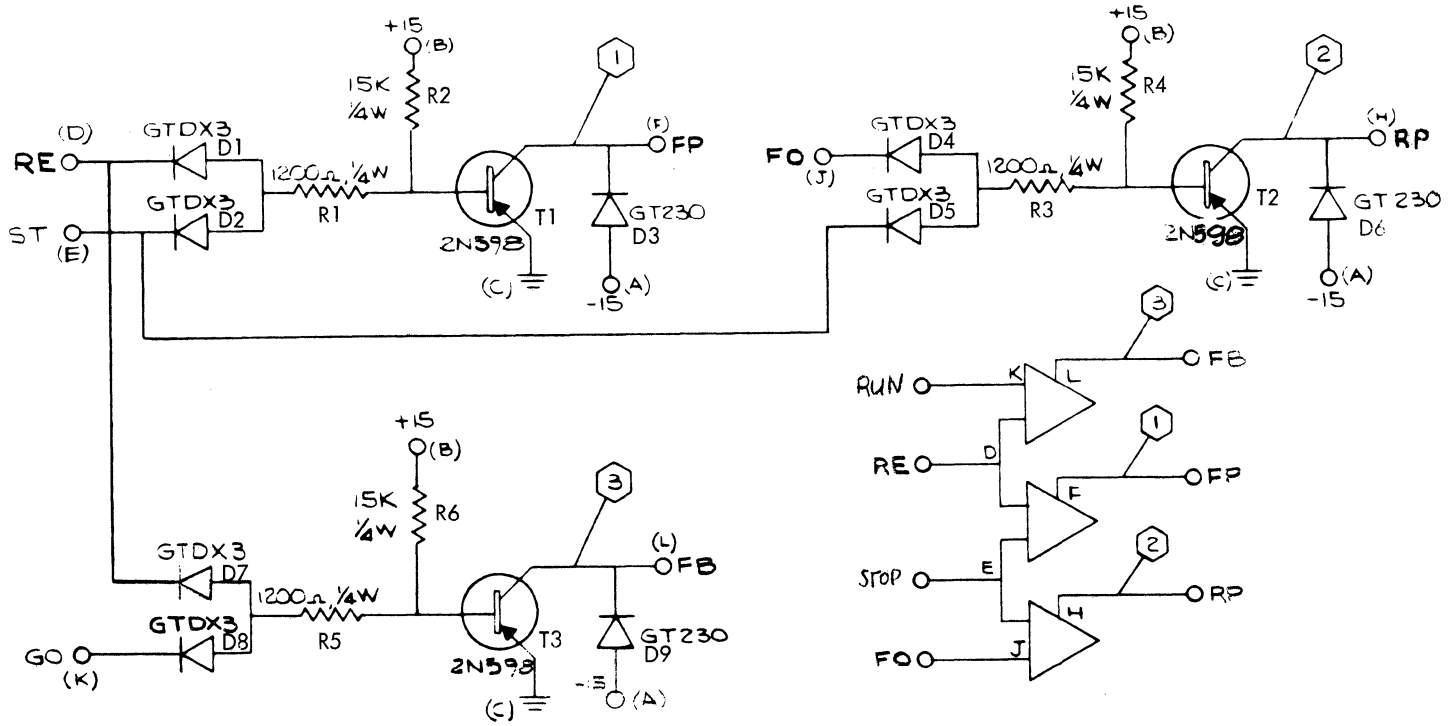


FIGURE 3-22 SCHEMATIC DIAGRAM - SDA

P.C. ASSEMBLY NO B-C 413

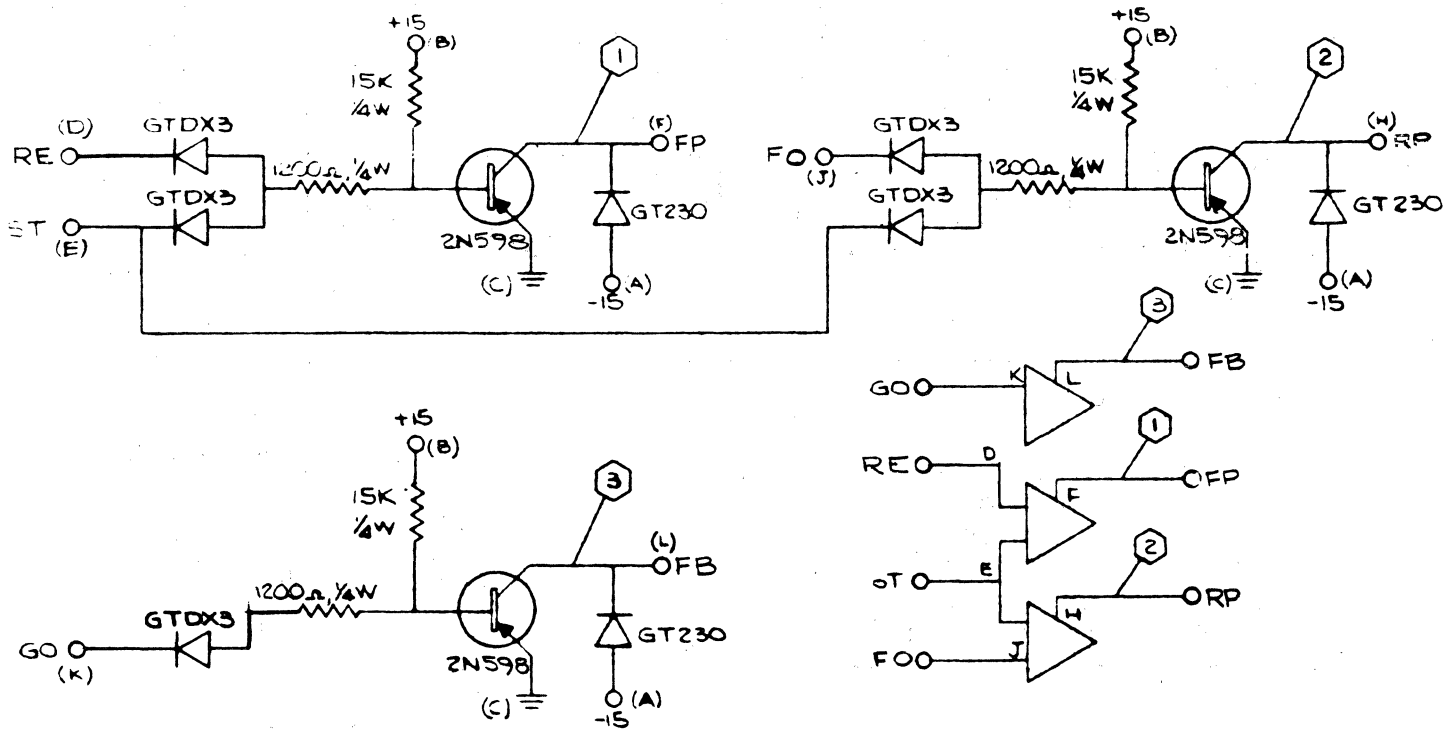


FIGURE 3-23 SCHEMATIC DIAGRAM - SDA-H

P.C. ASSEMBLY NO. B-C 1313

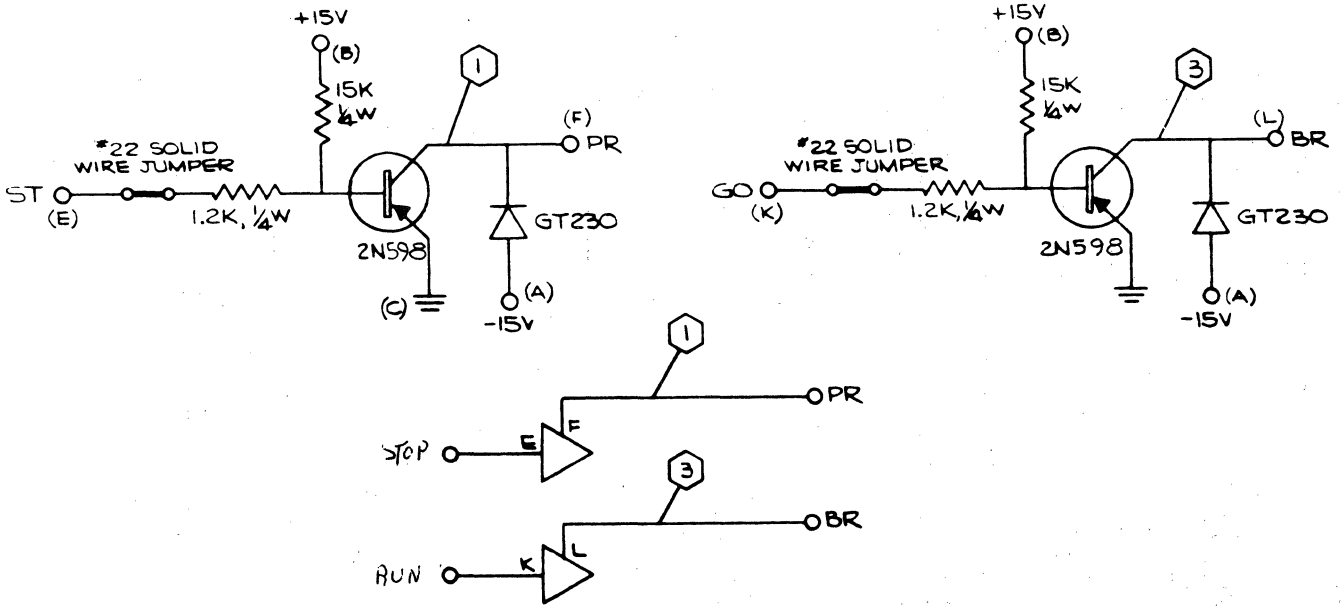
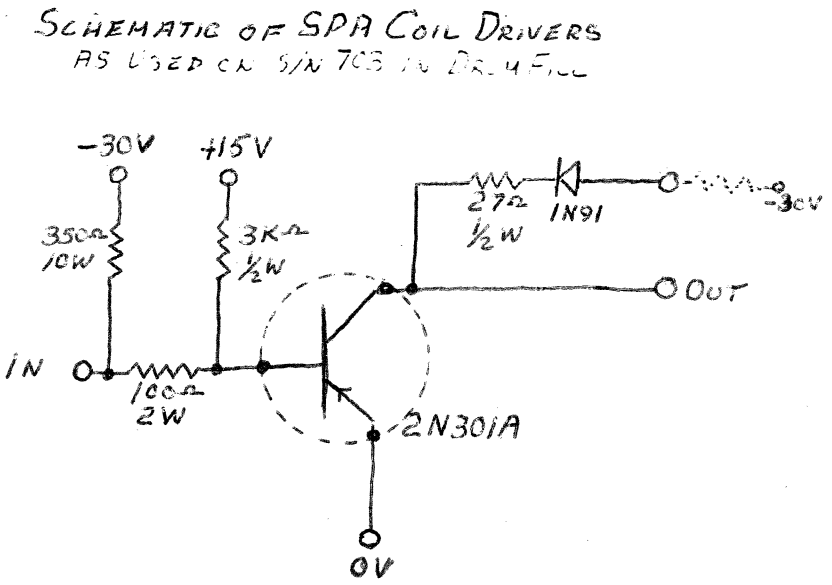


FIGURE 3-24 SCHEMATIC DIAGRAM - SDC

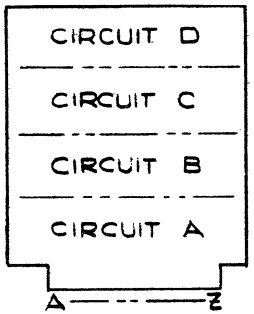
P.C. ASSEMBLY B-C628



PIN	SIGNAL
A	-30V
B	+15V
C	
D	-15V
E	
F	IN - D REV. BRK
H	IN - C REV. PINCH
J	IN - B FWD BRK
K	
L	
M	PRE
N	IN - A FWD. PINCH
P	
R	OUT - D REV. BRK
S	OUT - C REV. PINCH
T	0V
U	
V	
W	
X	OUT - B FWD BRK.
Y	OUT - A FWD PINCH
Z	

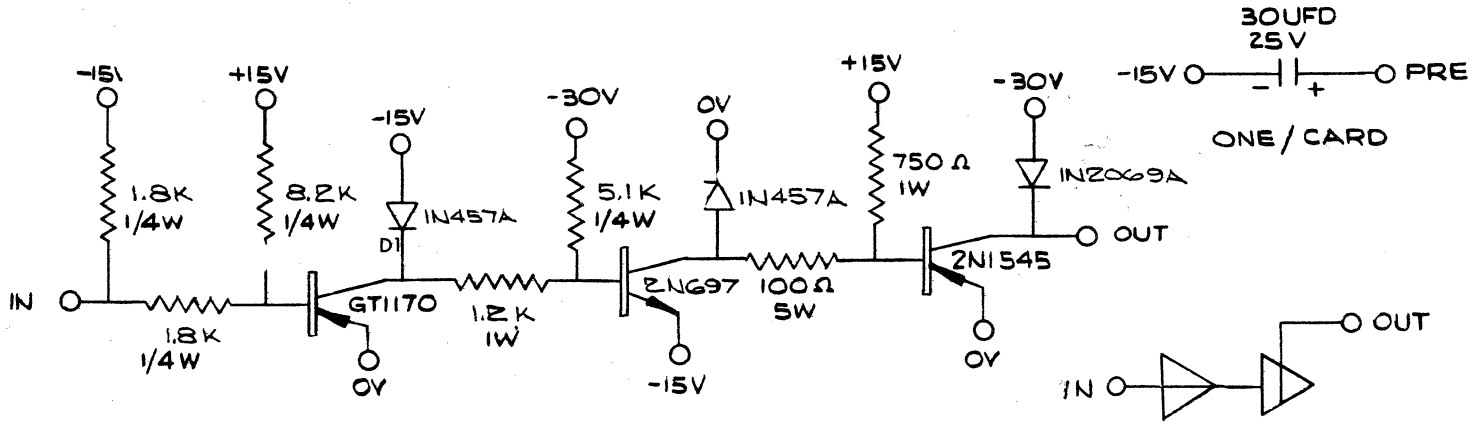
DWG NO	CIRCUIT	DIRECTION	ASSEMBLY
B-H542-1	"A" AND "B"	UNI	C-C1367-1
B-H542-2	"A, B, C AND D"	BI	C-C1367-2

"A" CIRCUIT = FORWARD PINCH ROLLER
"B" " = FORWARD BRAKE
"C" " = REVERSE PINCH ROLLER
"D" " = REVERSE BRAKE



ASSEMBLY C-C1367

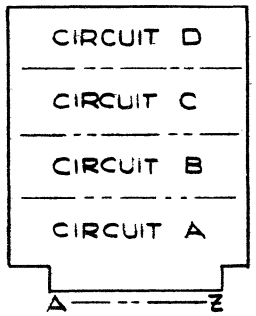
FIGURE 3-25 SCHEMATIC DIAGRAM - SPA-A-BI and SPA-A-UNI



PIN	SIGNAL
A	-30V
B	+15V
C	
D	-15V
E	
F	IN - D *Rev. Brk*
H	IN - C *Rev. Pinch*
J	IN - B *Fwd Brk*
K	
L	
M	PRE
N	IN - A *Fwd. Pinch*
P	
R	OUT - D *Rev. Brk*
S	OUT - C *Rev. Pinch*
T	0V
U	
V	
W	
X	OUT - B *Fwd Brk.*
Y	OUT - A *Fwd Pinch*
Z	

DWG NO	CIRCUIT	DIRECTION	ASSEMBLY
B-H542-1	"A" AND "B"	UNI	C-C1367-1
B-H542-2	"A, B, C AND D"	BI	C-C1367-2

"A" CIRCUIT = FORWARD PINCH ROLLER
"B" " = FORWARD BRAKE
"C" " = REVERSE PINCH ROLLER
"D" " = REVERSE BRAKE

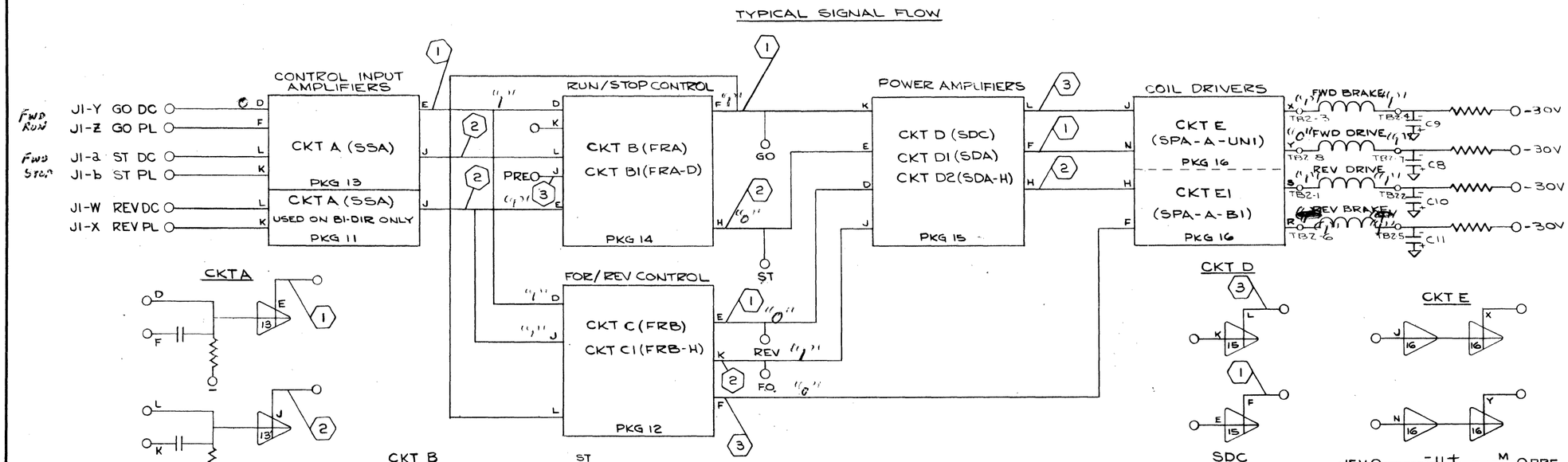


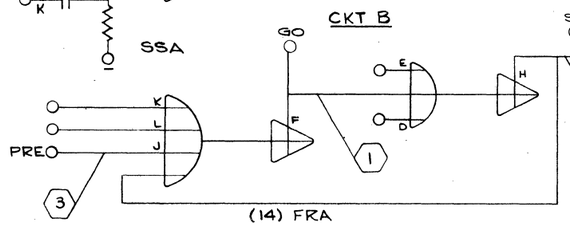
ASSEMBLY C-C1367

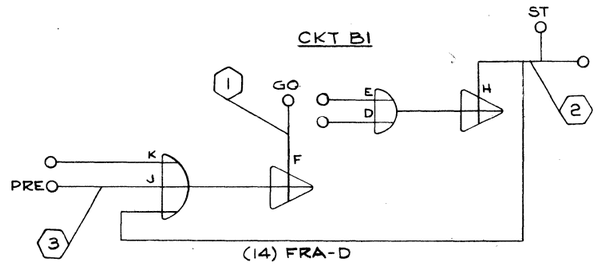
FIGURE 3-25 SCHEMATIC DIAGRAM - SPA-A-BI and SPA-A-UNI

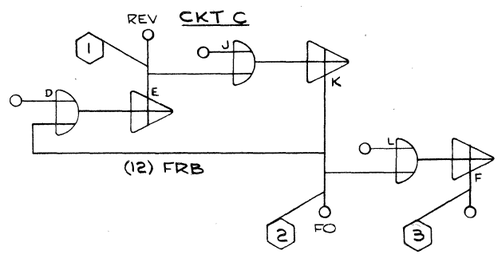
QUAN.	DESCRIPTION	REF. STD.	DRWG. NO.	ITEM

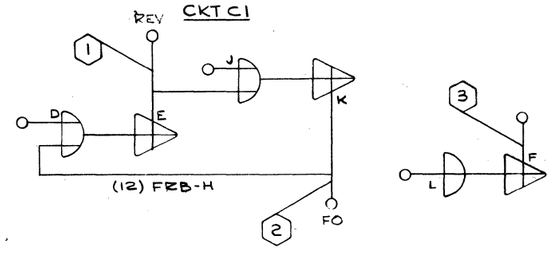
TYPICAL SIGNAL FLOW

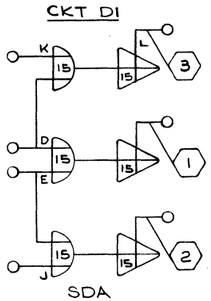


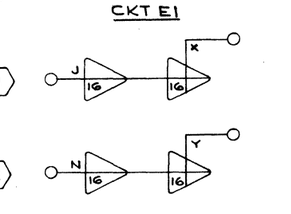


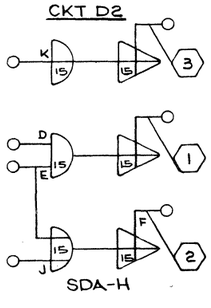


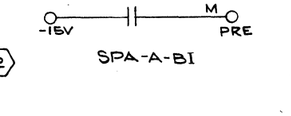












M.S. NO.	ITEM NO.	CKT.A	CKT.B	CKT.B1	CKT.C	CKT.C1	CKT.D	CKT D1	CKT.D2	CKT.E	CKT E1
MS128	2A	✓	✓				✓			✓	
MS128	2B	✓		✓			✓			✓	
MS128	2C	✓	✓		✓			✓			✓
MS128	2D	✓		✓	✓			✓			✓
MS128	2E	✓	✓			✓			✓		✓
MS128	2F	✓		✓		✓			✓		✓

DIGITRONICS
ALBERTSON, NEW YORK

TITLE:
FIGURE 3-26
BLOCK DIAGRAM
MOTION CONTROL SYSTEM

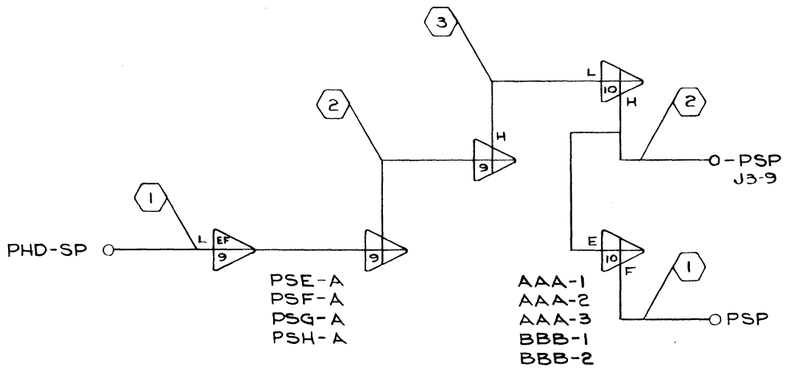
FIRST USED ON: 10015

SHEET 1 OF 1

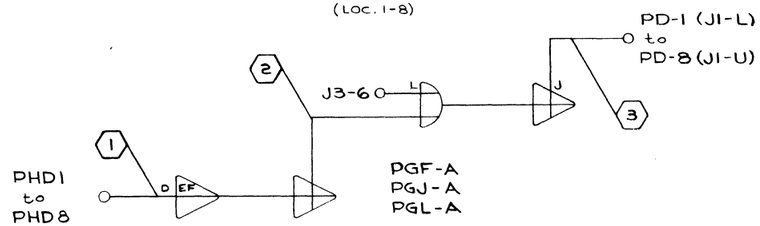
DRAWING NO. C-G643

QUAN.	DESCRIPTION	REF. STD.	DRWG. NO.	ITEM

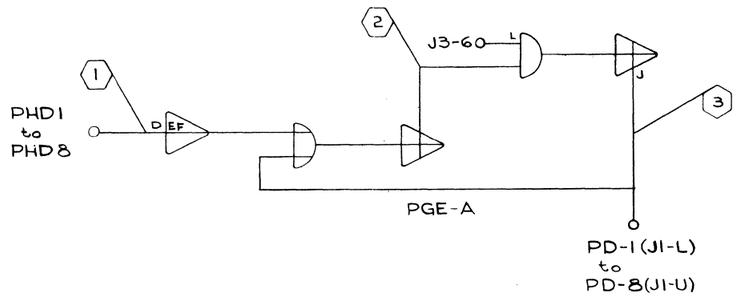
CKT A



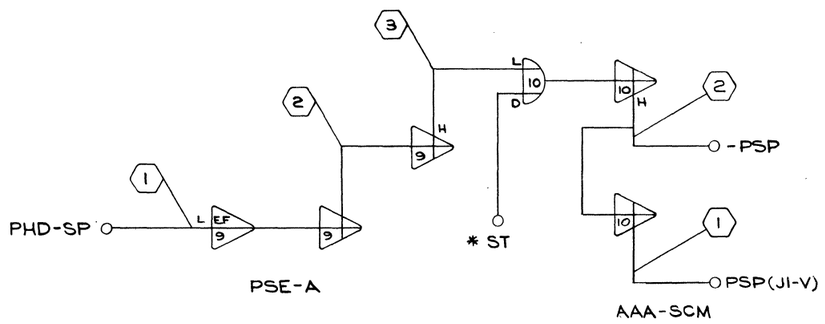
CKT C
(LOC. 1-8)



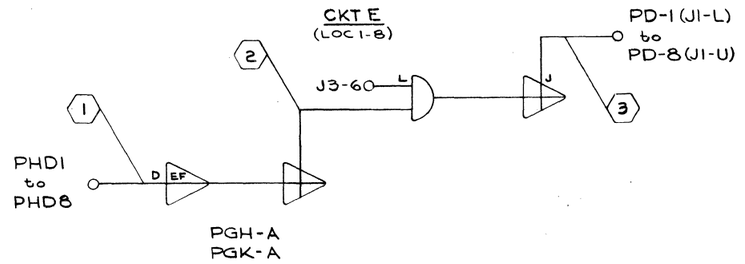
CKT D
(LOC. 1-8)



CKT B



CKT E
(LOC 1-8)



M.S. NO.	ITEM NO.	CKT A	CKT B	CKT C	CKT D	CKT E	J3 JUMPER CONNECTIONS GATED	J3 JUMPER CONNECTIONS UNGATED
MS-128	1A	✓		✓			J3-6 TO J3-9	J3-6 TO J3-8
MS-128	1B		✓		✓		J3-6 TO J3-9	J3-6 TO J3-8
MS-128	1C	✓		✓			J3-6 TO J3-9	J3-6 TO J3-8
MS-128	1D	✓				✓	J3-6 TO J3-9	J3-6 TO J3-2
MS-128	1E	✓				✓	J3-6 TO J3-9	J3-6 TO J3-2
MS-128	1F	✓		✓			J3-6 TO J3-9	J3-6 TO J3-1

J3 SIGNAL CONNECTIONS (REF)	
SIGNAL	PIN
-PSP	9
PKG 1-8 PINL	6
+15V	1
-15V	2
0V	8

*GENERATED BY MOTION CONTROL SYSTEM (PKG. 14)

DIGITRONICS
ALBERTSON, NEW YORK

TITLE:
3-27
BLOCK DIAGRAM
LOGICS OUTPUT SYSTEM

FIRST USED ON: 10015

SHEET 1 OF 1

DRAWING NO. C-G642

SECTION IV

MAINTENANCE

4-1 GENERAL

This section describes the periodic inspection, lubrication, cleaning, and adjustment procedures. Adherance to the procedures outlined in this section ensures operating reliability and minimizes failures.

4-2 PERIODIC INSPECTION

The periodic inspection checks should be performed according to the schedule in Table 4-1. The inspection period is based on an 8 hour day/5 day week and this should be adjusted in accordance with customer usage.

TABLE 4-1 PERIODIC INSPECTION

DAILY	MONTHLY	SEMI-ANNUALLY
1. Read Head 2. Tape Guides 3. Roller Bearings 4. Pinch Roller 5. Capstan 6. Brake Clean as required (Digitronics Cleaning Kit MS-133)	1. Pinch Roller and Capstan Gap 2. Brake Block and Brake Gap (Low speed brake) 3. Endless Belt Tension 4. Spring Tension on Endless Belt Idler arm 5. Pinch Roller and Capstan locknut adjustment 6. Brake Drum Assembly and Brake (Low speed brake) locknut adjustment	1. All moving parts for wear 2. Data Channel outputs 3. Sprocket Channel output 4. Power Supply Voltages

4-3 LUBRICATION

No lubrication of the unit is required. All bearings, including drive motor bearing, are permanently lubricated and require no attention. Double-shielded ball bearings are used throughout the tape transport system to prevent the entry of dust. When a bearing indicates any sign of sticking, it should be replaced.

4-4 CLEANING

When inspection reveals that components of the unit require cleaning, the Digitronics Cleaning Kit (MS-133) provides a convenient brush and solvent. Alternatively, a cotton swab or lint-free cloth may be used with a solvent such as N-Amyl Alcohol.

4-5 CAPSTAN ROLLER

The capstan roller should be cleaned as required with the Digitronics Cleaning Kit or N-Amyl Alcohol to remove accumulated lint and other foreign material.

4-6 ADJUSTMENT PROCEDURES

The adjustment procedures for the tape readers are given in paragraphs 4-7 thru 4-15. The procedures are divided into two categories: electrical and mechanical. When the visual and operational checks indicate that the unit is malfunctioning or in danger of failing, corrective maintenance is performed. The procedures outlined in this section will assist in maintaining trouble-free operation.

4-7 SPECIAL TOOLS AND REQUIREMENTS

The following test equipment is required to perform the electrical and mechanical adjustments.

Mechanical Adjustments

(1) Starett Feeler Gauge or Equivalent
(2) Set Allen Wrenches
(3) Spring Scale 1 - 10 lbs.

Electrical Adjustments

(1) Tektronic Type 535 oscilloscope with dual trace option or equivalent
(2) VTVM or equivalent

4-8 ELECTRICAL ADJUSTMENTS

The individual reader circuits, especially the eight photodiode amplifier circuits, are independent, therefore when one circuit requires adjustment, the others may not need adjustment, however, they should be checked for uniformity. The adjustable circuits in the reader are:

(1) Paper tape sprocket channel amplifier and shaper

(2) Paper tape data channel amplifiers

(3) Power supply
   a. -15 volts DC supply (adjust R1)
   b. +15 volts DC supply (adjust R2 and R3)
   c. -30 volts DC supply (adjust R4)
   d. Zener diode supply (adjust R5 and R6)
   e. Exciter lamp (adjust R7)

4-9 PAPER TAPE SPROCKET CHANNEL AMPLIFIER AND SHAPER

The paper tape sprocket channel amplifier and shaper is adjusted as follows:

(1) Insert loop of 8-channel tape with all channels punched.

(2) Apply AC power.

(3) Apply a start signal (pulsed or dc).

(4) Synchronize oscilloscope internally with ten divisions across the face of the oscilloscope representing one period.

(5) Observe waveshape at test point #3 of printed circuit card 9.
   a. PSE-A type sprocket amplifier - waveshape is negative (-10 volts) for 40% (four divisions) of the period and positive (zero volts) for 60% (six divisions).
   b. PSF-A type sprocket amplifier - waveshape is positive (zero volts) for 40% (four divisions) of the period and negative (-10 volts) for 60% (six divisions).
   c. PSG-A type sprocket amplifier - waveshape is positive (+10 volts) for 40% (four divisions) of the period and negative (zero volts) for 60% (six divisions).
   d. PSH-A type sprocket amplifier - waveshape is negative (zero volts) for 40% (four divisions) of the period and positive (+10 volts) for 60% (six divisions).

(6) Potentiometer R1 on the individual printed circuit cards is used to adjust the waveforms to these relationships.

4-10 PAPER TAPE DATA CHANNEL AMPLIFIERS

The adjustment of the paper tape read amplifiers is accomplished as follows:

(1) Insert loop of eight channel tape, all channels punched. (See Figure 4-2)

(2) Apply AC power to unit.

(3) Apply a start signal (pulsed or dc).

(4) Synchronize the oscilloscope internally with the ten divisions across the face of the oscilloscope representing one period.

(5) Observe waveshapes at test points 2 and 3 of the data channel amplifiers. The listing that follows are typical examples of the output of the individual data amplifiers used in the reader.
Note: Test point 1 shows the output of the photodiode particular to that channel.

a. PGF-A, PGL-A & PGE-A data channel amplifier

Gated - (1) A 0 volt pulse should be observed at test point 2 for 70% (seven divisions) of the period when a hole condition exists.

(2) A -10 volt pulse should be observed at test point 3 for 40% (four divisions) of the period when a hole condition exists.

Ungated - (1) A 0 volt pulse should be observed at test point 2 for 70% (seven divisions) of the period when a hole condition exists.

(2) A -10 volt pulse should be observed at test point 3 for 70% (seven divisions) of the period when a hole condition exists.

b. PGH-A Data channel amplifier

Gated - (1) A -10 volt pulse should be observed at test point 2 for 70% (seven divisions) of the period when a hole condition exists.

(2) A 0 volt pulse should be observed at test point 3 for 40% (four divisions) of the period when a hole condition exists.

Ungated - (1) A -10 volt pulse should be observed at test point 2 for 70% (seven divisions) of the period when a hole condition exists.

(2) A 0 volt pulse should be observed at test point 3 for 70% (seven divisions) of the period when a hole condition exists.

c. PGJ-A Data channel amplifier

Gated - (1) A 0 volt pulse should be observed at test point 2 for 70% (seven divisions) of the period when a hole condition exists.

(2) A +10 volt pulse should be observed at test point 3 for 40% (four divisions) of the period when a hole condition exists.

Ungated - (1) A 0 volt pulse should be observed at test point 2 for 70% (seven divisions) of the period when a hole condition exists.

(2) A +10 volt pulse should be observed at test point 3 for 70% (seven divisions) of the period when a hole condition exists.

d. PGK-A Data channel amplifier

Gated - (1) A +10 volt pulse should be observed at test point 2 for 70% (seven divisions) of the period when a hole condition exists.

(2) A 0 volt pulse should be observed at test point 3 for 40% (four divisions) of the period when a hole condition exists.

Ungated - (1) A +10 volt pulse should be observed at test point 2 for 70% (seven divisions) of the period when a hole condition exists.

(2) A 0 volt pulse should be observed at test point 3 for 70% (seven divisions) of the period when a hole condition exists.

(6) Adjust potentiometer R1 on the individual printed circuit cards when the indicated waveshape for a specific reader is not observed.

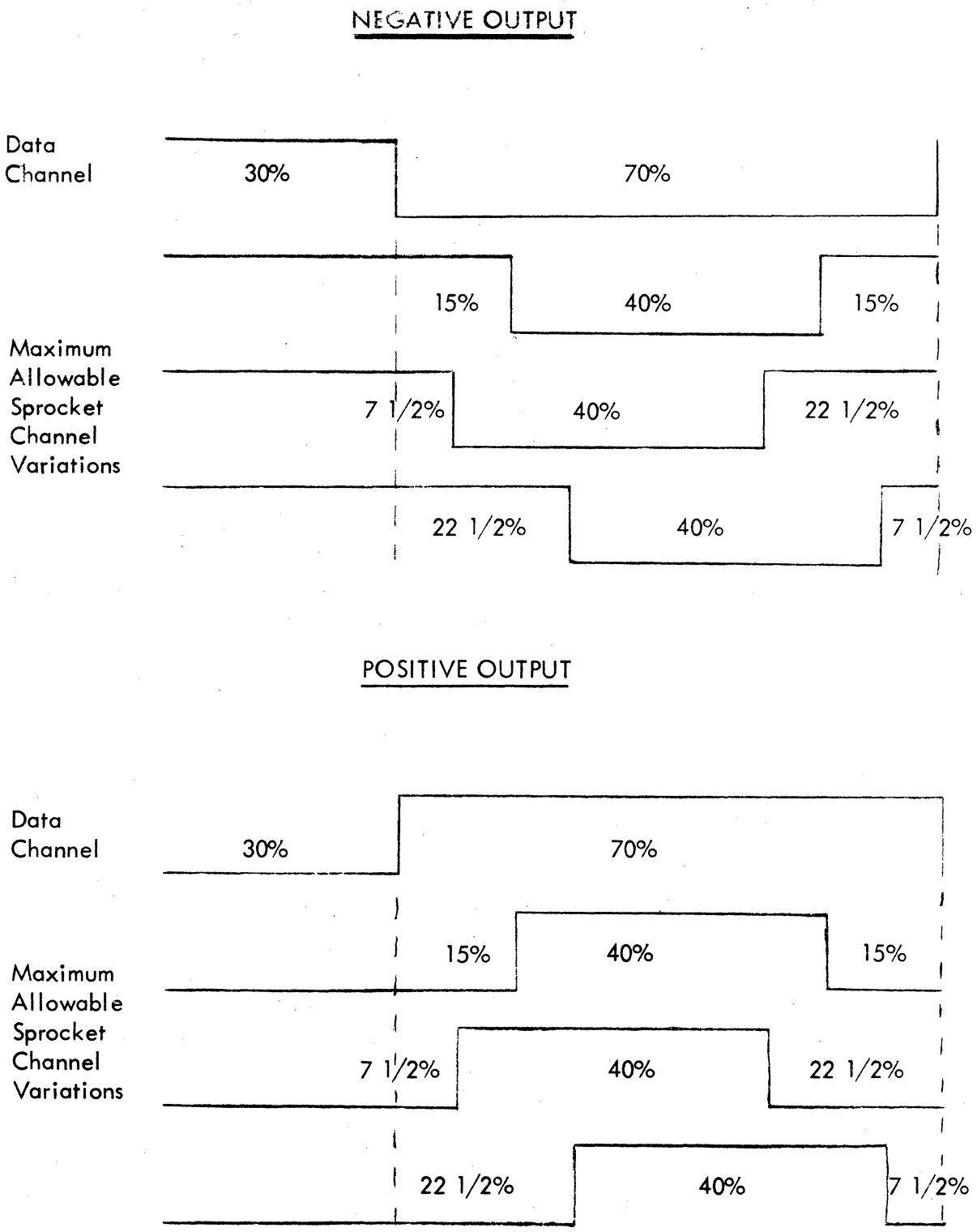


Figure 4-1 Maximum Allowable Sprocket Channel to Data Channel Ratio

4-11 SIGNAL COMPARISON TEST

The following test ensures that the sprocket pulses are effectively centered in the data pulses. After completing the procedural steps outlined in paragraph 4-9 and 4-10, perform the following steps:

(1) Using the dual trace option of the oscilloscope, synchronize the oscilloscope with any data channel output.

(2) With the oscilloscope channel A probe, observe the waveshape of the data channel used for synching.

(3) With the oscilloscope channel B probe, observe the sprocket channel waveshape and compare the physical relationship between the two signals. See Figure 4-1 for idealized waveshape relationships.

(4) Repeat steps 2 and 3 for all data channels.

If a data channel differs from the optimum requirements of 70% or the sprocket channel differs from the optimum requirement of 40%, the alignment of the associated circuits should be rechecked.

Various factors such as badly punched tape, cumulative tolerances or skewing may add together to cause drift in the sprocket to data hole ratio. This drift is acceptable within certain limitations. Figure 4-1 shows the maximum acceptable limits into which the sprocket signal may fall and still perform its gating function. Note that a 40% sprocket signal falls no less than 7 1/2% of either edge of the data signal. This is the maximum allowable limit for the sprocket channel variation. If the sprocket channel cannot be brought within these acceptable limits by readjustment of the sprocket signal and data signals, the Read Head Assembly should be returned to the factory for replacement.

4-12 POWER SUPPLY

The reader power section supplies all the necessary dc power for the operation of the data channel amplifiers and tape motion controls. Variable resistors are pre-set prior to shipping and require no further attention until a replacement is performed.

(1) -15 Volt DC Supply

Connect a VTVM to chassis ground and pin "D" on the SPA-A card connector. If -15 volts not present, adjust R1 to -15 volts ± 0.1V.

(2) +15 Volt DC Supply

Connect a VTVM to chassis ground and pin "B" on the SPA-A card connector. If +15 volts not present, adjust R2 and R3 to +15 volts ±0.1V.

(3) -30 Volt DC Supply

Connect a VTVM to chassis ground and pin "A" on the SPA-A card connector. If -30 volts not present, adjust R4 to -30 volts ±0.1V.

(4) Zener Diode Supply

R5 and R6 should be adjusted only when the zener diode is replaced.

Adjustment Procedure - Adjust R5 and R6 so that a change from 80 volts to 90 volts AC at the input will cause the voltage across zener diode to increase no more than 0.4 volts. When the input line voltage changes from 90 volts to 100 volts, the increase across the zener diode should be less than 0.2 volts. For a line voltage change of 90 volts to 130 volts, the voltage across the zener diode should not vary more than 0.3 volts.

(5) Exciter Lamp

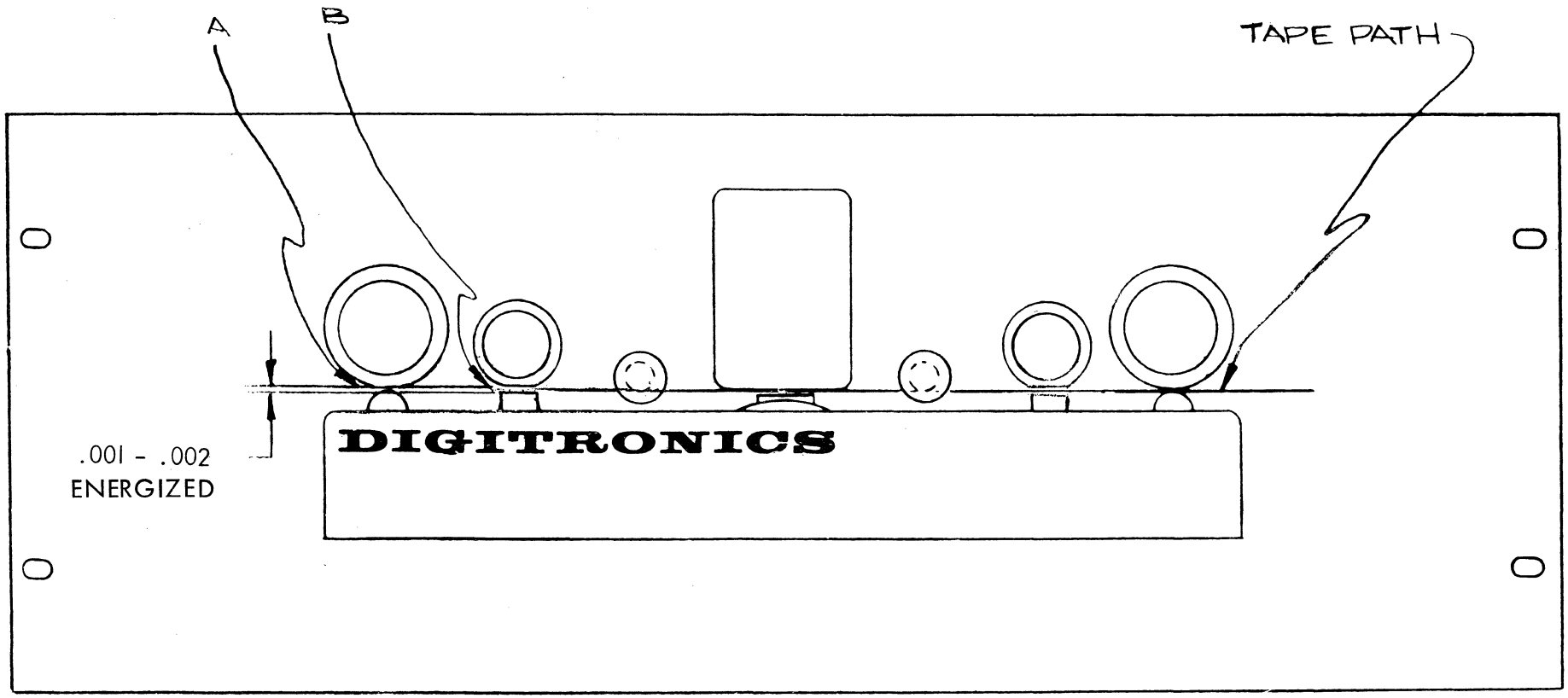
Connect a VTVM across J5-1 and J5-2. Adjust R7 for a reading of 8.5 volts dc.

(6) Photodiode Bias Supply

There is no adjustment of the photodiode bias. Connector P3 provides regulation of the bias through a zener diode and resistor R8. The photodiode bias potential is checked as follows:

Connect VTVM across standoff 9 to ground.

a. For units using negative bias meter reading should be -5.5 volts dc (See note 2 on Figure 3-2).
b. For units using positive bias meter reading should be +5.5 volts dc (See note 2 on Figure 3-2).



A - Pinch Roller/Capstan Gap
B - Brake Bracket/ Brake Drum Gap

DIGITRONICS
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TITLE:

FIGURE 4-2
ADJUSTMENT TOLERANCES
PINCH ROLLER AND LOW SPEED BRAKE

4-13 MECHANICAL ADJUSTMENT

The outlined procedural steps are for adjustment of capstan to pinch roller and low speed brake to brake drum assembly. Units using the high speed brake require no brake adjustment; however, it should be checked to ascertain that the armature rests evenly on core structure.

4-14 PINCH ROLLER & LOW SPEED BRAKE GAP ADJUSTMENT

NOTE

The following clearances are factory adjusted by Digitronics Corporation prior to delivery and should remain set. However, it is recommended that the clearances be checked at intervals suggested in Table 4-1.

(1) Gap Check

a. Disconnect the capstan drive motor connector P-4.

b. Energize the pinch roller solenoid by applying the proper tape start signal to the reader.

c. Check that the gap between the capstan and the pinch roller is between .001 and .002 TIR (True Indicated Reading).

d. Perform the above steps for the other pinch roller if unit is a bi-directional model.

e. A similar clearance should exist between the brake drum assembly and the brake bracket on those readers employing the low speed brake.

f. Reconnect P-4.

(2) Gap Adjust

If adjustment becomes necessary, perform the following steps:

a. Remove the engraved coverplate by taking out the two screws located on the underside of the coverplate.

b. Each solenoid block is secured to the panel by two #10 socket-head screws. Loosen the screws associated with the particular solenoid block to be adjusted.

c. Remove the drive motor connector P-4.

d. Energize the pinch roller (or low speed brake) to be adjusted by applying the proper tape start signal to the reader.

e. Use a feeler gauge to establish the correct clearance and adjust the solenoid block. While holding the feeler gauge in place, tighten the socket head screws securely.

f. Reconnect P-4.

g. Check for proper operation with a loop of tape.

h. Apply start and stop signals to reader to ascertain correct solenoid operation.

4-15 PINCH ROLLER & LOW SPEED BRAKE LOCKNUT ADJUSTMENT

NOTE

The following clearances are factory adjusted by Digitronics Corporation prior to delivery and should remain set. However, it is recommended that the clearances be checked at intervals suggested in Table 4-1.

(1) Locknut Check

a. Apply power to unit.

b. Using a spring tension scale, check that the force necessary to unseat an activate pinch roller solenoid is 3-4 lbs.

c. Perform the above steps for the other pinch roller if unit is B3500.

d. A similar force is necessary to unseat the brake bracket from an activated brake drum assembly.

(2) Locknut Adjust

If adjustment becomes necessary, perform the following procedures:

a. Remove the engraved coverplate by removing the two screws located on the underside of the coverplate.

b. Each solenoid to be adjusted must be in the activated condition. Apply a signal to the tape drive system to activate the solenoid to be adjusted.

c. Tighten locknut until solenoid toggles to de-activated position.

d. Backoff locknut until solenoid returns to activated position.

e. Backoff locknut one additional half turn.

f. Check that the force to unseat the solenoid is 3-4 lbs.

g. Perform this procedure for the other pinch roller and the other two brakes as required if unit is Model B3500.

4-16 REMOVAL & REPLACEMENT PROCEDURES

4-17 GENERAL

Refer to the exploded view illustrations in Section V to determine the relationship of the assemblies and attaching parts. These illustrations should be used in conjunction with the text when removal and replacement procedures are performed. Remove attaching parts of the assemblies in index number sequence only to the extent necessary to repair, replace, or clean the item. Whenever it becomes necessary to remove any solenoid block, un-screw the wiring at TB-2 and remove the wires.

4-18 MAJOR DIS-ASSEMBLY PROCEDURES

4-19 PAPER TAPE READER BRAKE ASSEMBLIES

4-20 LOW SPEED BRAKE & PINCH ROLLER ASSEMBLY

Dis-assemble the brake solenoid mount assembly and its parts (brake and solenoids) in accordance with Figure 5-6 for the B3500 and Figures 5-7 and 5-9 for the 3500 by following steps 1 through 3.

(1) Remove cover (not shown) enclosing brake solenoid by removing two screws, one located under each solenoid assembly.

(2) Remove the two socket-head screws (20) holding solenoid assembly to panel and remove the assembly (1).

(3) If the solenoid (2) needs to be replaced, it is necessary to remove the brake BRACKET (15), or pinch roller (5) before the solenoid mounting nuts (3) can be removed. Then refer to paragraphs 4-14 through 4-15 for adjustment procedures necessary to align the pinch roller or brake assembly.

4-21 PINCH ROLLER SOLENOID ASSEMBLY WITH HIGH SPEED BRAKE ASSEMBLY

Dis-assemble the pinch roller solenoid and its parts (roller and solenoid) in accordance with Figure 5-8 for the B3500 by following steps 1 through 3.

(1) Remove coverplate enclosing pinch roller and high-speed brake assemblies by removing two screws, one under each individual pinch roller and high-speed brake assembly.

(2) Remove two screws (27) holding pinch roller solenoid assembly to the base plate (27). Then refer to paragraphs 4-13 through 4-15 for adjustment procedures necessary to align the pinch roller/brake assembly.

(3) If the pinch roller solenoid (12) needs to be replaced, it is necessary to remove the roller bracket (17), before the solenoid mounting hardware (15 and 16) can be removed.

4-22 TAPE DRIVE CAPSTAN & PULLEY ASSEMBLIES

Figure 5-5 for 3500 and 5-5A for B3500

Dis-assemble the capstans by removing the capstan pulleys (13), (12, 3500 only), and attaching parts. In removing the drive belt (1), idler arm roller (8), (6, 3500 only) must be released by unhooking tension spring (10), (9, 3500 only).

4-23 TAPE DRIVE MOTOR & MOUNTING PLATE ASSEMBLY

Refer to Figure 5-4 in the Illustrated Parts Breakdown section and follow steps 1 through 5.

(1) Release belt roller idler arm (Figure 5-5, 6 or Figure 5-5A, 8) and remove belt (Figure 5-5, 1 or Figure 5-5A, 1) from capstan drive pulleys (Figure 5-5, 12 or Figure 5-5A, 13).

(2) Remove three motor mounting plate screws (12) from the tape reader panel.

(3) Remove the motor pulley (5) from the motor shaft.

(4) Remove three screws (3) holding motor to mounting plate and remove motor.

(5) If it becomes necessary to remove the phase shift capacitor (10), see Figure 5-4 and dis-assemble in accordance with the figure.

4-24 TAPE GUIDES

Remove the tape guide (figure 5-2) on either side of the photodiode read head by noting the index number order of dis-assembly. A tape guide (6) and its associated arm (5) are connected together by a rubber "O" ring (3).

4-25 BRAKE DRUM ASSEMBLY LOW SPEED
Figure 5-6 B3500 and Figure 5-9 3500

The brake drum assembly (Figure 5-6, 16 or 5-9, 19) is attached to the panel by a bolt extending through the panel.

4-26 READ HEAD ASSEMBLY
Figure 5-1

The read head assembly is mounted to the panel by four screws (25) inserted from the front side. To change the exciter lamp (4), remove the exciter lamp cover (1). When it is necessary to change any photodiode, return the entire unit (Figure 5-1, Read Head Assembly) to the manufacturer.

4-27 WIRING DIAGRAM

Refer to figure 4-6 chassis wiring (DK 400-65), figure 4-6A wire list (DK 400-66) for jumper location, and figure 4-6B (BK304) for optional wiring for the various units. Figure 4-6B (BK304) particularizes the standard chassis to enable it to conform to the Manufacturing Specification.

4-28 CONNECTOR P-3

This special connector determines the logic output by determining the bias on the photodiodes; it will determine whether the machine will have gated outputs or ungated outputs; and it will determine the direction of rotation for the capstan motor. For re-ordering of connector P-3, select the proper B-C 2313 dash number from figure 4-4.

TABLE 4-2 NOMINAL VOLTAGES

LOGICS OUTPUT SECTION			
DATA CHANNEL CARDS	TEST POINT	HOLE	NO HOLE
PGE-A	3	-15V	0.0V
PGF-A	3	-15V	0.0V±.5V
PGL-A	3	-15V	0.0V±.2V
PGH-A	3	0V	-15V
PGJ-A	3	+15V	0.0V
PGK-A	3	0V	+15V
SPROCKET CARDS	TEST POINT	HOLE	NO HOLE
PSE-A	3	-10V	0.0V
PSF-A	3	0.0V	-10V
PSG-H	3	+10V	0.0V
PSH-A	3	0.0V	+10V
AUXILIARY AMPLIFIER CARD	TEST POINT	HOLE	NO HOLE
AAA-1			
"-PSP"	2	0.0V	-10V
"PSP"	3	-15V	0.0V
AAA-2			
"-PSP"	2	-10V	0.0V
"PSP"	3	0.0V	-15V
BBB-1			
"-PSP"	2	+10V	0.0V
"PSP"	3	0.0V	+15V
BBB-2			
"-PSP"	2	+10V	0.0V
"PSP"	3	0.0V	+15V
AAA-SCM			
Diode Input		-10V	0.0V
ST Diode Input		RUN 0.0V	STOP -6V
"-PSP"	2	0.0V	-10V
"PSP"	3	-15V	0.0V

NOTE: For Data Channel Outputs and signal "PSP" the voltages are for the unloaded conditions.

TABLE 4-2 Cont'd. NOMINAL VOLTAGES

MOTION CONTROL SECTION

CARD LOCATION	CARD	TEST POINT	FWD RUN	REV RUN	FWD STOP	REV STOP
#11	SSA	1	—	—	—	—
		2	—	0	—	-6
#13	SSA	1	-6	—	0	—
		2	0	—	-6	—
#14	FRA	1	-6	-6	0	0
		2	0	0	-6	-6
#14	FRA-D	1	-6	-6	0	0
		2	0	0	-6	-6
#12	FRB	1	0	-6	0	-6
		2	-6	0	-6	0
		3	0	0	0	-6
#12	FRB-H	1	0	-6	0	-6
		2	-6	0	-6	0
		3	0	0	-6	-6
#15	SDC	1	-6	—	0	—
		3	0	—	-6	—
#15	SDA	1	-6	0	0	0
		2	0	-6	0	0
		3	0	0	-6	0
#15	SDA-H	1	-6	0	0	0
		2	0	-6	0	0
		3	0	0	-6	-6

DK 400-63-1

0V/NO HOLE, -10V/HOLE
GATED AMPLIFIERS
UNI - DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		1
YEL	4		2
	3		2
BRN	6		9
VIO	11		10

DK 400-63-2

0V/NO HOLE, -10V/HOLE
UN-GATED AMPS
UNI- DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		1
YEL	4		2
	3		2
BRN	6		8
VIO	11		10

DK 400-63-3

0V/NO HOLE, -10V/HOLE
GATED AMPS
BI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		1
YEL	4		2
	3		2
BRN	6		9
VIO	11		12

DK 400-63-4

0V/NO HOLE, -10V/HOLE
UN-GATED AMPS
BI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		1
YEL	4		2
	3		2
BRN	6		8
VIO	11		12

DK 400-63-5

0V/NO HOLE, +10V/HOLE
GATED AMPS
UNI - DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		2
YEL	4		1
	3		1
BRN	6		9
VIO	11		10

DK 400-63-6

0V/NO HOLE, +10V/HOLE
UN-GATED AMPS
UNI- DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		2
YEL	4		1
	3		1
BRN	6		8
VIO	11		10

DK 400-63-7

0V/NO HOLE, +10V/HOLE
GATED AMPS
BI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		2
YEL	4		1
	3		1
BRN	6		9
VIO	11		12

DK 400-63-8

0V/NO HOLE, +10V/HOLE
UN-GATED AMPS
BI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		2
YEL	4		1
	3		1
BRN	6		8
VIO	11		12

DK 400-63-9

-10V/NO HOLE, 0V/HOLE
GATED AMPS
UNI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		1
YEL	4		2
	3		1
BRN	6		9
VIO	11		10

DK 400-63-10

-10V/NO HOLE, 0V/HOLE
UN-GATED AMPS
UNI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		1
YEL	4		2
	3		1
BRN	6		2
VIO	11		10

DK 400-63-11

-10V/NO HOLE, 0V/HOLE
GATED AMPS
BI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		1
YEL	4		2
	3		1
BRN	6		9
VIO	11		12

DK 400-63-12

-10V/NO HOLE, 0V/HOLE
UN-GATED AMPS
BI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		1
YEL	4		2
	3		1
BRN	6		2
VIO	11		12

DK 400-63-13

+10V/NO HOLE, 0V/HOLE
GATED AMPS
UNI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		2
YEL	4		1
	3		2
BRN	6		9
VIO	11		10

DK 400-63-14

+10V/NO HOLE, 0V/HOLE
UN-GATED AMPS
UNI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		2
YEL	4		1
	3		2
BRN	6		1
VIO	11		10

DK 400-63-15

+10V/NO HOLE, 0V/HOLE
GATED AMPS
BI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		2
YEL	4		1
	3		2
BRN	6		9
VIO	11		12

DK 400-63-16

+10V/NO HOLE, 0V/HOLE
UN-GATED AMPS
BI-DIRECTIONAL

CLR	PIN	TO	PIN
RED	5		2
YEL	4		1
	3		2
BRN	6		1
VIO	11		12

NOTE:

1) ALL WIRES 22 GA. INSULATED AS INDICATED

2) USE SLEEVING ON DIODE LEADS

DIGITRONICS
ALBERTSON, NEW YORK

TITLE: 4-3
WIRING DIAGRAM
PARTICULARIZING
CONNECTOR P3

REF. DWG. NO.

DRAWING NO. D-K 400-63

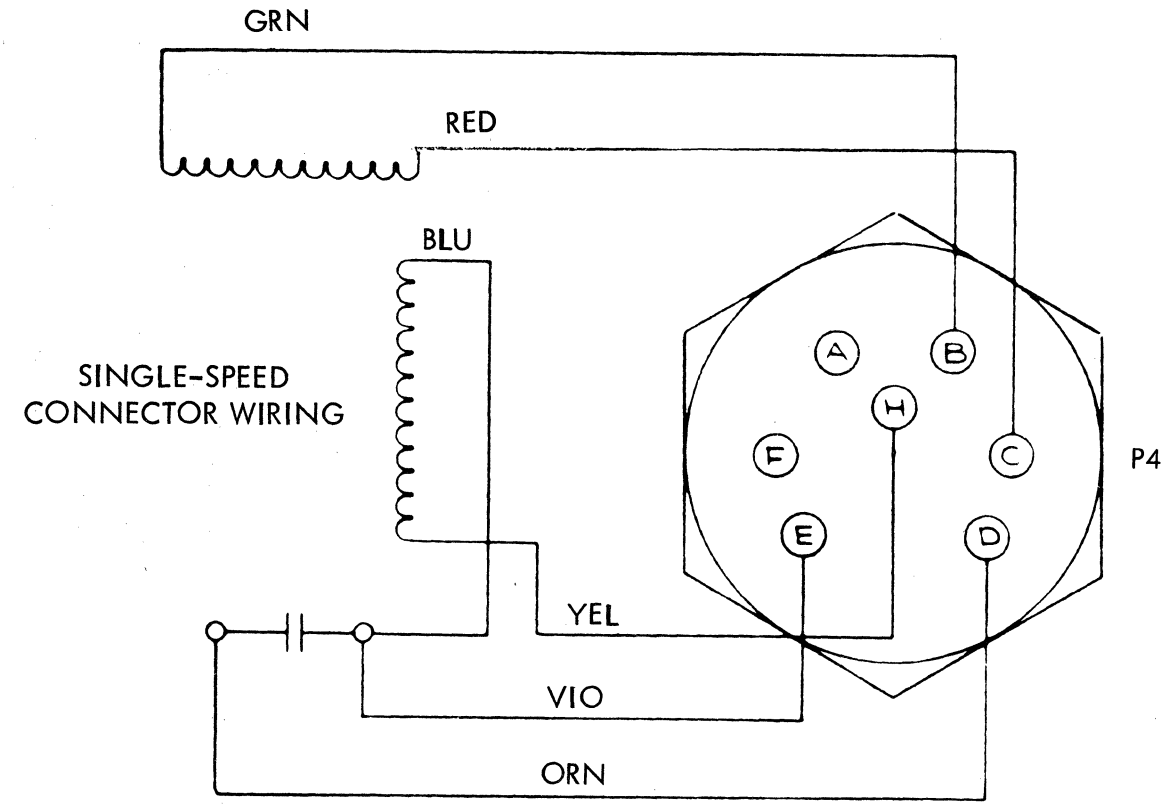
CONNECTOR NO.	PLUG DEFINITION									
	LOGIC OUTPUT SYSTEM						MOTION TYPE		GATING MODE	
	1A	1B	1C	1D	1E	1F	UNI-DIR	BI-DIR	GATED	UNGATED
B-C2313-1	✓						✓		✓	
B-C2313-1		✓					✓		✓	
B-C2313-5			✓				✓		✓	
B-C2313-9				✓			✓		✓	
B-C2313-13					✓		✓		✓	
B-C2313-1						✓	✓		✓	
B-C2313-3	✓							✓	✓	
B-C2313-3		✓						✓	✓	
B-C2313-7			✓					✓	✓	
B-C2313-11				✓				✓	✓	
B-C2313-15					✓			✓	✓	
B-C2313-3						✓		✓	✓	
B-C2313-2	✓						✓			✓
B-C2313-6			✓				✓			✓
B-C2313-10				✓			✓			✓
B-C2313-14					✓		✓			✓
B-C2313-2						✓	✓			✓
B-C2313-4	✓							✓		✓
B-C2313-8			✓					✓		✓
B-C2313-12				✓				✓		✓
B-C2313-16					✓			✓		✓
B-C2313-4						✓		✓		✓

DIGITRONICS
ALBERTSON, NEW YORK

TITLE:
4-4
WIRING DIAGRAM
PARTICULARIZING
CONNECTOR P3

USED ON: 10015

DRAWING NO. B-C2322



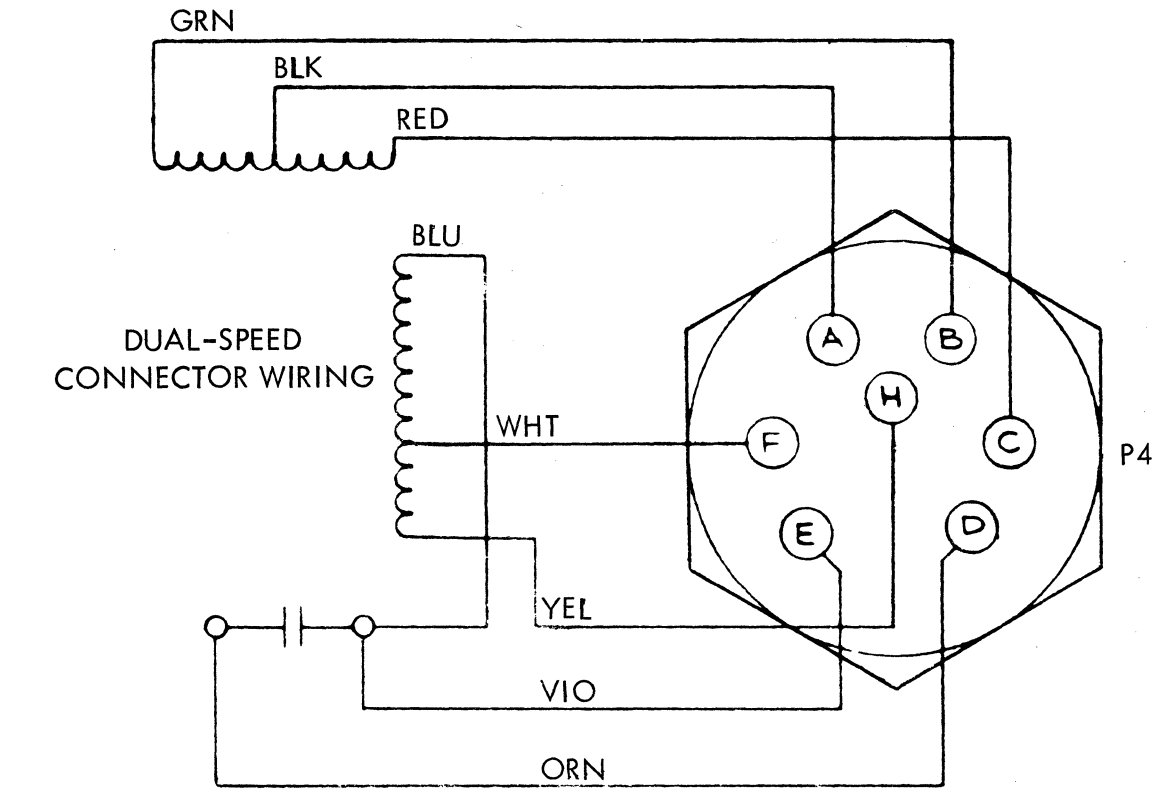


FIGURE 4-5 WIRING DIAGRAM - DRIVE MOTOR CONNECTOR, P4

ACTUAL VIEW

TERM 2

TERM 1

F2 (VIO) R4-3 CR1-1 (BLK) RED

F3 (BLK) R2-3 R5-1 (BLK) BLU CR2-1 (RED)

F4 WHT C5(-) R16-1 WHT CR3-1 (BLK) BRN

F1 (BRN) J1-D #20 J3-10 RED TB1-7 RED STD-2 RED #20

PC-1 connector rows L K J H F E D C B A; columns 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

J1-L J1-M J1-N J1-P J1-R J1-S J1-T J1-U J3-6 P2-15 J3-9 J1-Y J1-W J1-X J1-3 J1-b J1-Z J1-7 J1-H

SPA-J (W/BRN)
PC14-F (W/GRN)
PC12-K (W/GRN)
SPA-H (W/GRY)
SPA-N (W/ORN)
PC14-H (W/GRN)
PC12-E (W/GRN)
STD10 (VIO)

C4(+) YEL
C1(-) BLU

J6: SPA-C GRN, BUS, SPA-T W/YEL, SPA-A ORN

J1: STD-10 VIO; (BRN) F1-1 #20; STD-1 (BLK) #20; (W/GRY) PC6-J; (BLU) PC5-J; (W/RED) PC11-K; (GRN) PC4-J; (W/VIO) PC13-K; (W/BRN) PC11-L; PC13-L W/BLU; PC1-J (RED); PC2-J (ORN); PC3-J (YEL); PC7-J (GRY); PC8-J (WHT); PC13-D (W/ORN); PC13-F W/YEL; PC10-F (W/BLU) VIO; PC15-C VIO; J1-H VIO; J3-8; STD 10

R8; P2-13 GRY; J3-3 GRY; STD 9

F1-2 RED; SEE NOTE (2)

SPA-B YEL; PC1-A BRN; J4-D RED; 1 4 7 10 13

PC1-B ORN; SPA-D BLU; STD-9 GRY; 2 5 8 11 14

J3: 3 6 9 12 15; PC8-L W/BLK; PC10-H W/RED

STD10 (VIO) J4-C GRN; STD-1 BLK

TB1-1 BRN; TB1-2 ORN; TB1-4 BLU; TB1-5 VIO; TB1-3 YEL

J3-11 GRN; J3-10 RED

J4: A B C D E F H

R7-3; C6(-) WHT; P5-2 WHT; 3 1 2; CR4

R7; (RED) P5-1 #20; W/GRN; CR4-1; C6(+) BLU

SPA-A; R4-1 ORN; W/BLK C2(+); W/BLK C8(+); R9; T1-BRN; C7

SPA-Z; R10-1 GRY; W/BLK C9(+); W/BLK C7(-); C8

STD-3 W/BLK; C8(-) W/BLK; R11-2; SPA-W VIO; C9

STD-7 BLK; SPA-U W/GRN; STD 5

SPA-V W/BLU; STD-6 BRN; STD 4; C10; C11

C9(+) W/BLK; SPA-T W/YEL; STD 3

SPA

Z (GRY) C8(-)
Y (WHT) TB2-8
X (RED) TB2-3
W (VIO) C9(-)
V (W/BLU) STD-4
U (BLK) STD-5
T (W/YEL) J6-5 STD3 W/YEL
S (BLK) TB2-1
R (BRN) TB2-6
P
N (W/GRN) PC15-F
M (W/RED) PC13-J
L (W/BLK) PC1-C
K C4(-) (W/BLK)
J (W/GRN) PC15-L
H (W/GRN) PC15-H
F (W/VIO) PC12-F
E
D BLU C1(-)
C BLU J3-2 R10-1 GRN
B (GRN) TG-1
A (YEL) J3-1 C4(+) (YEL)
(GRN) TG-2 C7(-) ORN

C6: R7-3 BLU; R6-2 BLU; C5(-) WHT; CR9-3 WHT

J4-H YEL; J4-A ORN; J4B BRN; J4-F BLU; J4-E VIO; STD-1 #20 BLK; #20 F1-2 RED

TB1: 1 2 3 4 5 6 7

TB2-5 BLK; STD-5 BLK; STD 7

TB2-2 BRN; STD-4 BRN; STD 6

TB1-6 (BLK); T1-BLK; J3-12 (BLK) #20; J1-C (BLK) #20; STD 1

T1-WHT; W/BLK C3(-); W/BLK C1(+); W/BLK C7(+); R16-2 BRN; C2

R2-2 GRN; C3

YEL R3-1; YEL PC11-B; SPA-B YEL; C4

C3(-) W/BLK; SPA-L W/BLK; C4(+) W/BLK; C4(-) W/BLK

#20 F1-2 (RED) T1-BLK; STD 2

R5-3 ORN; F4-1 WHT; C6(-) WHT; C5

F2-1 VIO; R2-1 W/GRN; F3-1 BLK; W/GRN C2(-) BRN; GRN C3(+); F4-1 WHT; C7 ORN; C4(+) YEL; R4 R3 R2 R1 R16

C2(+) W/BLK; BLU R1-1; BLU PC11-A; BLU SPA-D; C1; GND

T1 (YEL); F2-2 RED; CR1-2 (BLK) W/GRN; CR1; T1 (YEL); CR1-1 (BLK) W/GRN

T1 (GRN); CR3-1 (YEL) W/GRN; F3-2 BLU; CR2-2 (RED) W/GRN; CR2; CR3-2 (YEL) W/GRN; T1 (GRN)

CR2-1 (YEL) W/GRN; F4-2 BRN; CR3-2 (BLK) W/GRN; CR3; CR2-1 (RED) W/GRN; CR3-1 (BLK) W/GRN; CR2-2 (YEL) W/GRN

PC4-D PC5-D PC3-D PC6-D PC2-D PC7-D PC1-D PC8-D BLK BLU RED GRN YEL GRY BLU VIO; STD-9 GRY; PC9-L WHT

P2

R7-1 (RED) #20; P5-1; TWISTED PAIRS; P5-2; CR9-3 WHT

TB2: SPA-Y WHT; R10-2 RED; SPA-R BRN; STD-7 BLK; R11-2 WHT; SPA-X RED; STD-6 BRN; SPA-S BLK; 8 7 6 5 4 3 2 1

R5 R6 W/GRN; C6(+) BLU; C5(+) ORN; F3-1 BLK

(WHT) TB2-4 C8(-) VIO; TB2-7 (RED) C8(-) GRY

R15 R14 R13 R12 R11 R10; SPA-C GRN; BUS

NOTES:
1) USE 22GA. WIRE UNLESS OTHERWISE SPECIFIED
2) FOR MATING CONNECTOR INFORMATION SEE DK400-63 (AS APPLICABLE)
3) FOR WIRING LIST REF. SEE DK 400-66
4) FOR CABLE PATH REF. SEE DK 400-64

10015

DIGITRONICS
ALBERTSON, NEW YORK

TITLE: 4-6 WIRING DIAGRAM CHASSIS (Reference)

REF. DWG. NO.

DRAWING NO. D-K400-65

CABLE WIRES

ITEM	GA.	CL.	FROM	TO	REMARKS
1	22	RED	PC1-J	J1-L	
2	↑	ORN	PC2-J	J1-M	
3		YEL	PC3-J	J1-N	
4		GRN	PC4-J	J1-P	
5		BLU	PC5-J	J1-R	
6		W/GRY	PC6-J	J1-S	
7		GRY	PC7-J	J1-T	
8		WHT	PC8-J	J1-U	
9		WHT	PC9-L	P2-15	
10		W/RED	PC10-H	J3-9	
11	↓	W/BLK	PC10-F	J1-V	
12		W/BRN	PC11-L	J1-W	
13		W/RED	PC11-K	J1-X	
14		W/VIO	PC12-F	SPA-F	
15		W/BLU	PC13-L	J1-a	
16		W/VIO	PC13-K	J1-b	
17		W/YEL	PC13-F	J1-Z	
18		W/ORN	PC13-D	J1-Y	
19		W/RED	PC14-J	SPA-M	
20		W/BLK	PC8-L	J3-6	
21		W/BRN	PC15-L	SPA-J	
22		W/GRY	PC15-H	SPA-H	
23		W/ORN	PC15-F	SPA-N	
24		BLK	PC1-D	P2-1	
25		W/BLK	PC1-C	SPA-L	
26		ORN	PC1-B	J3-5	
27		BRN	PC1-A	J3-4	
28		BRN	PC2-D	P2-2	
29		RED	PC3-D	P2-3	
30		ORN	PC4-D	P2-4	
31		YEL	PC5-D	P2-5	
32		GRN	PC6-D	P2-6	
33		BLU	PC7-D	P2-7	
34		VIO	PC8-D	P2-8	
35		YEL	PC11-B	C4(+)	
36	↓	BLU	PC11-A	C1(-)	
37	22	VIO	PC15-C	STD 10	
38	20	BLK	J1-C	STD-1	
39	20	BRN	J1-D	F1-1	
40	22	VIO	J1-H	STD-10	
41	22	BRN	TB1-1	J4-B	

CABLE WIRES

ITEM	GA.	CL.	FROM	TO	REMARKS
42	22	ORN	TB1-2	J4-A	
43	↑	YEL	TB1-3	J4-H	
44		BLU	TB1-4	J4-F	
45	22	VIO	TB1-5	J4-E	
46	20	RED	TB1-7	F1-2	
47	22	ORN	C5(+)	R5-3	
48	20	BLK	TB1-6	STD-1	
49	22	W/YEL	STD-3	SPA-T	
50	22	GRN	SPA-C	R10-1	
51	22	GRY	STD-9	P2-13	
52	22	YEL	SPA-B	C4(+)	
53	20	RED	F1-2	STD 2	
54	22	RED	J3-10	F1-2	
55	20	BLK	STD-1	J3-12	
56	20	RED	R7-1	P5-1	
57	22	WHT	CR4-3	P5-2	
58		GRN	J6-1	SPA-C	
59		ORN	J6-4	SPA-A	
60		W/YEL	J6-5	SPA-T	
61		BLK	TB2-1	SPA-S	
62		BRN	TB2-2	STD-6	
63		RED	TB2-3	SPA-X	
64		WHT	TB2-4	R11-2	
65		BLK	TB2-5	STD-7	
66		BRN	TB2-6	SPA-R	
67		RED	TB2-7	R10-2	
68		WHT	TB2-8	SPA-Y	
69		GRY	C8(-)	SPA-Z	
70		GRY	C8(-)	R10-2	
71		VIO	C9(-)	R11-2	
72		VIO	C9(-)	SPA-W	
73		W/BLU	STD-4	SPA-V	
74		BRN	STD-4	STD-6	
75		W/GRN	STD-5	SPA-U	
76		BLK	STD-5	STD-7	
77		WHT	CR4-3	C6(-)	
78		WHT	C6(-)	C5(-)	
79		BLU	C6(+)	R6-2	
80		BLU	C6(+)	R7-3	
81	↓	RED	CR1-1(BLK)	F2-2	
82	22	RED	J4-D	J3-10	

CABLE WIRES

ITEM	GA.	CL.	FROM	TO	REMARKS
83	22	W/BLK	C4(-)	SPA-L	
84	↑	BLU	CR1-1(RED)	F3-2	
85		W/BLK	C3(-)	C4(-)	
86		W/BLK	C2(+)	C3(-)	
87		BRN	CR3-1(BLK)	F4-2	
88		YEL	F3-1	SPA-B	
89		BLU	J3-11	SPA-D	
90		GRN	F2-1	J4-C	
91		VIO	F2-1	R4-3	
92		BLK	F3-1	R2-3	
93		BLK	F3-1	R5-1	
94		WHT	F4-1	R1-16	*
95		WHT	F4-1	C5(-)	
96		GRN	R2-2	C3(+)	
97		YEL	R3-1	C4(+)	
98		BRN	R6-2	C2(-)	*
99		W/BLK	C9(+)	STD-3	
100		W/BLK	C2(+)	C7(+)	
101		W/BLK	C2(+)	C1(+)	
102		W/BLK	C8(+)	C9(+)	
103		BLU	C1(-)	SPA-D	
104		BLU	R1-1	C1(-)	*
105		ORN	C7(-)	R4-1	
106	↓	ORN	C7(-)	SPA-A	
107	22	W/BLK	C7(+)	C8(+)	
108	22	GRY	J3-3	STD9	*
109	22	VIO	J3-8	STD10	*
110	22	BLU	CR4-1	R7-3	

COMPONENT CONNECTIONS

ITEM	GA.	CL.	FROM	TO	REMARKS
T1		BLK		STD1	SUPPLIED WIRE
		BLK		STD2	
		BRN		C7(+)	
		YEL		CR1-1(YEL)	
		YEL		CR1-2(YEL)	
		GRN		CR2-1(YEL)	
		GRN		CR2-2(YEL)	
↓		WHT		C2(+)	↓
R8			STD9	STD10	SLEEVE
R9			C7(+)	C7(-)	SLEEVE

JUMPERS

ITEM	GA.	CL.	FROM	TO	REMARKS
1	22	W/GRN	PC1-L	PC2-L	
2	↑		PC2-L	PC3-L	
3			PC3-L	PC4-L	
4			PC4-L	PC5-L	
5			PC5-L	PC6-L	
6			PC6-L	PC7-L	
7			PC7-L	PC8-L	
8			PC9-H	PC10-L	
9			PC10-H	PC10-E	
10			PC11-J	PC12-J	
11			PC12-L	PC14-F	
12			PC12-K	PC15-J	
13			PC12-J	PC14-E	
14			PC12-E	PC15-D	
15			PC17-D	PC13-E	
16			PC13-J	PC14-L	
17			PC13-E	PC14-D	
18			PC14-H	PC15-E	
19			PC14-F	PC15-K	
20			PC1-C	PC2-C	
21			PC2-C	PC3-C	
22			PC3-C	PC4-C	
23			PC4-C	PC5-C	
24			PC5-C	PC6-C	
25			PC6-C	PC7-C	
26			PC7-C	PC8-C	
27			PC9-C	PC10-C	
28			PC11-C	PC12-C	
29			PC12-C	PC13-C	
30			PC13-C	PC14-C	
31			PC14-C	PC15-C	
32			PC1-B	PC2-B	
33			PC2-B	PC3-B	
34			PC3-B	PC4-B	
35			PC4-B	PC5-B	
36			PC5-B	PC6-B	
37			PC6-B	PC7-B	
38			PC7-B	PC8-B	
39			PC8-B	PC9-B	
40	↓		PC9-B	PC10-B	
41	22	↓	PC11-B	PC12-B	

JUMPERS

ITEM	GA.	CL.	FROM	TO	REMARKS
42	22	W/GRN	PC13-B	PC13-B	
43	↑		PC13-B	PC14-B	
44			PC14-B	PC15-B	
45			PC1-A	PC2-A	
46			PC2-A	PC3-A	
47			PC3-A	PC4-A	
48			PC4-A	PC5-A	
49			PC6-A	PC7-A	
50			PC7-A	PC8-A	
51			PC8-A	PC9-A	
52			PC9-A	PC10-A	
53			PC11-A	PC12-A	
54			PC12-A	PC13-A	
55			PC13-A	PC14-A	
56		↓	PC14-A	PC15-A	
57		BUS	CR4-1	CR4-2	
58		BUS	J6-2	J6-3	
59		W/GRN	R6-2	R6-3	
60		W/GRN	P4-1	R4-2	
61		W/GRN	R1-2	R1-1	*
62		W/GRN	R3-1	R3-2	
63		W/GRN	R2-1	R2-2	
64		W/GRN	CR1-1(BLK)	CR1-2(BLK)	
65			CR2-1(RED)	CR2-2(RED)	
66			CR3-1(BLK)	CR3-2(BLK)	
67			CR2-1(YEL)	CR3-1(YEL)	
68			CR2-2(YEL)	CR3-2(YEL)	
69		↓	R2-1	R3-3	
70		BUS	R10-1	R11-1	
71		W/GRN	R5-2	R6-1	
72			PC8-C	PC9-C	
73			PC10-C	PC11-C	
74		↓	PC5-A	PC6-A	
75		BUS	R1-3	R16-2	*
76		W/GRN	R7-1	R7-2	
77		W/GRN	C1(+)	GND	
78		W/GRN	R1-3	R16-2	*
79	↓	W/GRN	PC10D	PC14H	

NOTES:
1) FOR CHASSIS REF. SEE DK 400-65
2) FOR CABLE PATH REF. SEE DK 400-64

DIGITRONICS
ALBERTSON, NEW YORK

TITLE: 4-6A
WIRING DIAGRAM
JUMPER LIST

MASTER DRAWING	MACHINE DRAWING
	DK 400-66

BK 304 -1- UNI-DIRECTIONAL STANDARD BRAKE	BK 304 -2- UNI-DIRECTIONAL HIGH SPEED BRAKE				BK 304 -3- BI-DIRECTIONAL STANDARD BRAKE				BK 304 -4- BI-DIRECTIONAL HIGH SPEED BRAKE				BK 304 -5- BI-DIRECTIONAL HIGH SPEED BRAKE (DOUBLED-UP)			
1. CONNECT TWO WHT/BLK WIRES TO POS. TERM OF C9 2. CONNECT TWO VIO. WIRES TO NEG. TERM. OF C9.	COLOR	FROM	TO	REMARKS	COLOR	FROM	TO	REMARKS	COLOR	FROM	TO	REMARKS	COLOR	FROM	TO	REMARKS
		R11-1	R12-1	#22 BUSSWIRE		R11-1	R12-1	#22 BUSSWIRE		R11-1	R12-1	#22 BUSSWIRE		R11-1	R12-1	#22 BUSSWIRE
		R11-2	R12-2	#22 BUSSWIRE		R12-1	R13-1	#22 BUSSWIRE		R12-1	R13-1	#22 BUSSWIRE		R12-1	R13-1	#22 BUSSWIRE
					BRN	R12-2	STD-6			R13-1	R14-1	#22 BUSSWIRE	BRN	R12-2	STD-6	
					BLK	R13-2	STD-7			R14-1	R15-1	#22 BUSSWIRE	BLK	R13-2	STD-7	
					WHT/BLK	C10(+)	STD-3		#22 BUS WIRE	R11-2	R12-2		WHT/BLK	C10(+)	STD-3	
					WHT/BLK	C11(+)	STD-3		#22 BUS WIRE	R14-2	R15-2		WHT/BLK	C11(+)	STD-3	
					BRN	C10(-)	STD-4		BRN	R13-2	STD-6		BRN	C10(-)	STD-4	
					BLK	C11(-)	STD-5		BLK	R14-2	STD-7		BLK	C11(-)	STD-5	
									WHT/BLK	C10(+)	STD-3					
									WHT/BLK	C11(+)	STD-3					
									BRN	C10(-)	STD-4					
									BLK	C11(-)	STD-5					

REF:
1. SEE SCHEMATIC DH718-1
2. SEE NOTE #2

REF:
1) SEE SCHEMATIC DH718-2
2) SEE NOTE #2

REF:
1) SEE SCHEMATIC DH718-3
2) SEE NOTE #1

REF:
1) SEE SCHEMATIC DH718-4
2) SEE NOTE #1

REF:
1) SEE SCHEMATIC DH718-5
2) SEE NOTE #1

NOTES
(1) TB1 JUMPER CONNECTIONS:
CONNECT 1 TO 7
3 TO 6
(2) TB1 JUMPER CONNECTIONS:
CONNECT 1 TO 6
3 TO 6

DIGITRONICS
ALBERTSON, NEW YORK

TITLE: 4-6B
WIRING DIAGRAM
OPTIONAL COMPONENT
WIRING AS PER MS

USED ON: 10015

DRAWING NO. BK 304

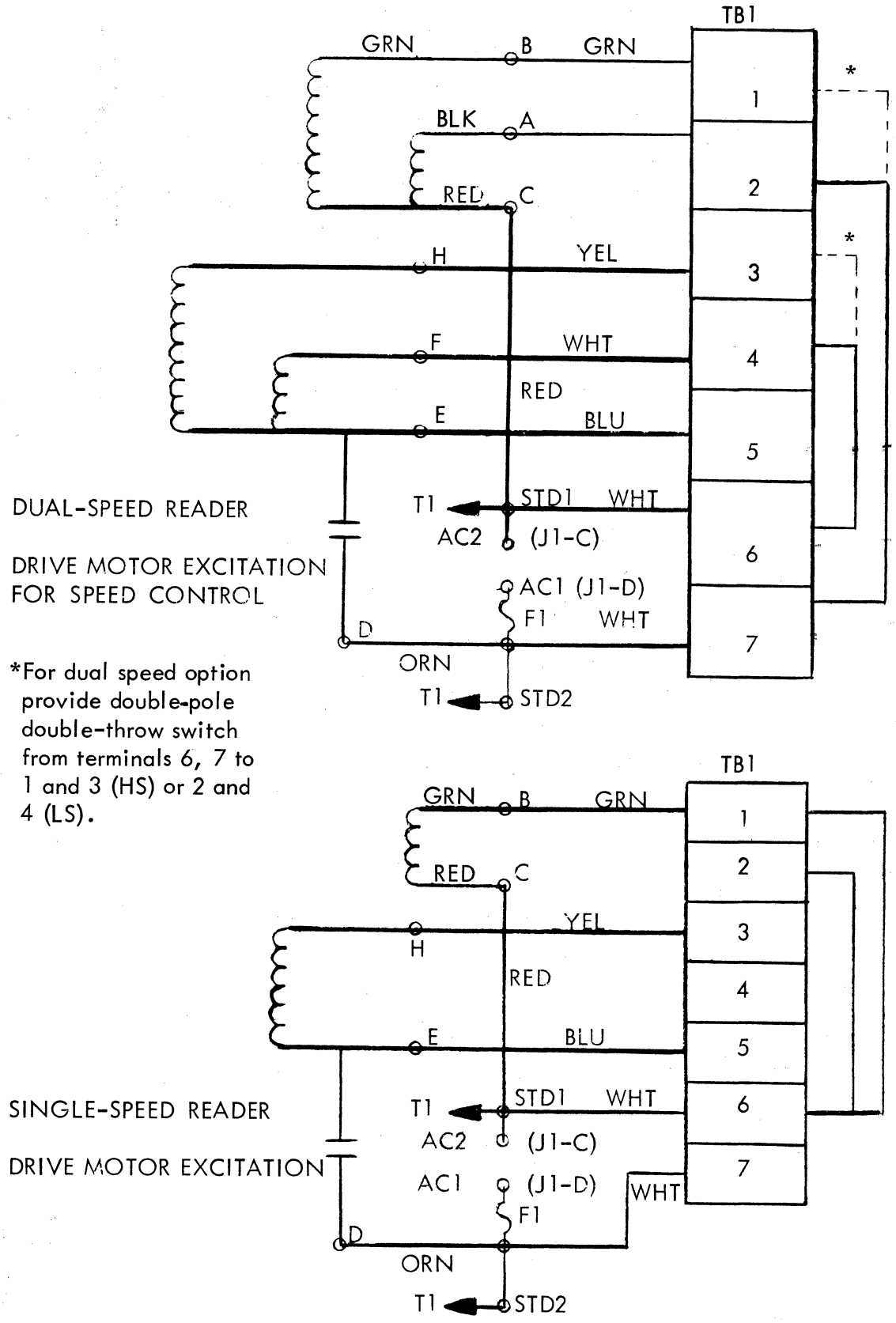


FIGURE 4-7 WIRING DIAGRAM - VARIABLE SPEED CONNECTIONS FOR TB1

SECTION V

ILLUSTRATED PARTS BREAKDOWN

5-1 GENERAL

This Illustrated Parts Breakdown lists, illustrates, and describes the various assemblies for the 3500 and B3500 perforated tape readers. It is intended to be used for identification, procurement of parts, assembly and dis-assembly procedures. Operation, maintenance, service, or repair should be performed by competent personnel using the applicable sections of this handbook. Also contained in this section is a replaceable electrical parts list. (Parts list for cards are on the card assembly drawings.)

5-2 GROUP ASSEMBLY PARTS LIST

The Group Assembly Parts List contains exploded view illustrations indexed to indicate the parts of the equipment, and the descriptive information for each part.

5-3 FIGURE & INDEX NUMBER COLUMN

This column lists the figure and index number which cross-references the description of the part to its illustration. The first number indicates the figure on which the illustration of the part may be found. The second number indicates the corresponding item number assigned to the illustration of the part. The figure number group is shown only at the first listing for an illustration. The item number is listed in numerical order for each part.

5-4 PART NUMBER COLUMN

This column contains the manufacturers part number. Commercial hardware, procurable from normal commercial sources require no part number. Descriptive information is sufficiently complete to make replacement procurements from commercial sources.

5-5 DESCRIPTION COLUMN

This column contains a description of each item in accordance with manufacturers' drawing, plus the modifiers necessary to establish the characteristics of the particular item. The descriptions are indented under the headings 1 through 3 to show the relationship of parts, sub-assemblies, and assemblies to one another. Attaching parts are listed immediately following the parts they attach in some cases, and have the same indentation.

5-6 UNITS PER ASSEMBLY COLUMN

The quantity listed in this column is the total quantity of a part used in a particular assembly. When an entire assembly is used more than once, only the assembly (5-1, 5-2, etc.) will carry the total number of parts used in the equipment.

5-7 LIST OF VARIATIONS

The list of variations table 5-1 has been replaced by drawings BC2414 and CC2227. The information contained on the drawings is the same as the information contained in the table, however the drawings contain speeds which were not called out on the table.

5-8 DIGITRONICS NINE DIGIT PART NUMBERS

Standard hardware and electrical components called out in the manual can be ordered directly from Digitronics Corporation. All hardware such as screws, nuts, bolts and standard electrical components such as transistors, diodes, capacitors, and resistors have been given nine digit part numbers. These nine digits describe the part. When ordering spares, please use the Digitronics part numbers whenever and wherever possible.

5-9 PRINTED CIRCUIT CARDS

When reordering printed circuit cards use the printed circuit (P.C.) assembly drawing number called out in Section III on the schematic representation for the card.

ILLUSTRATED PARTS BREAKDOWN

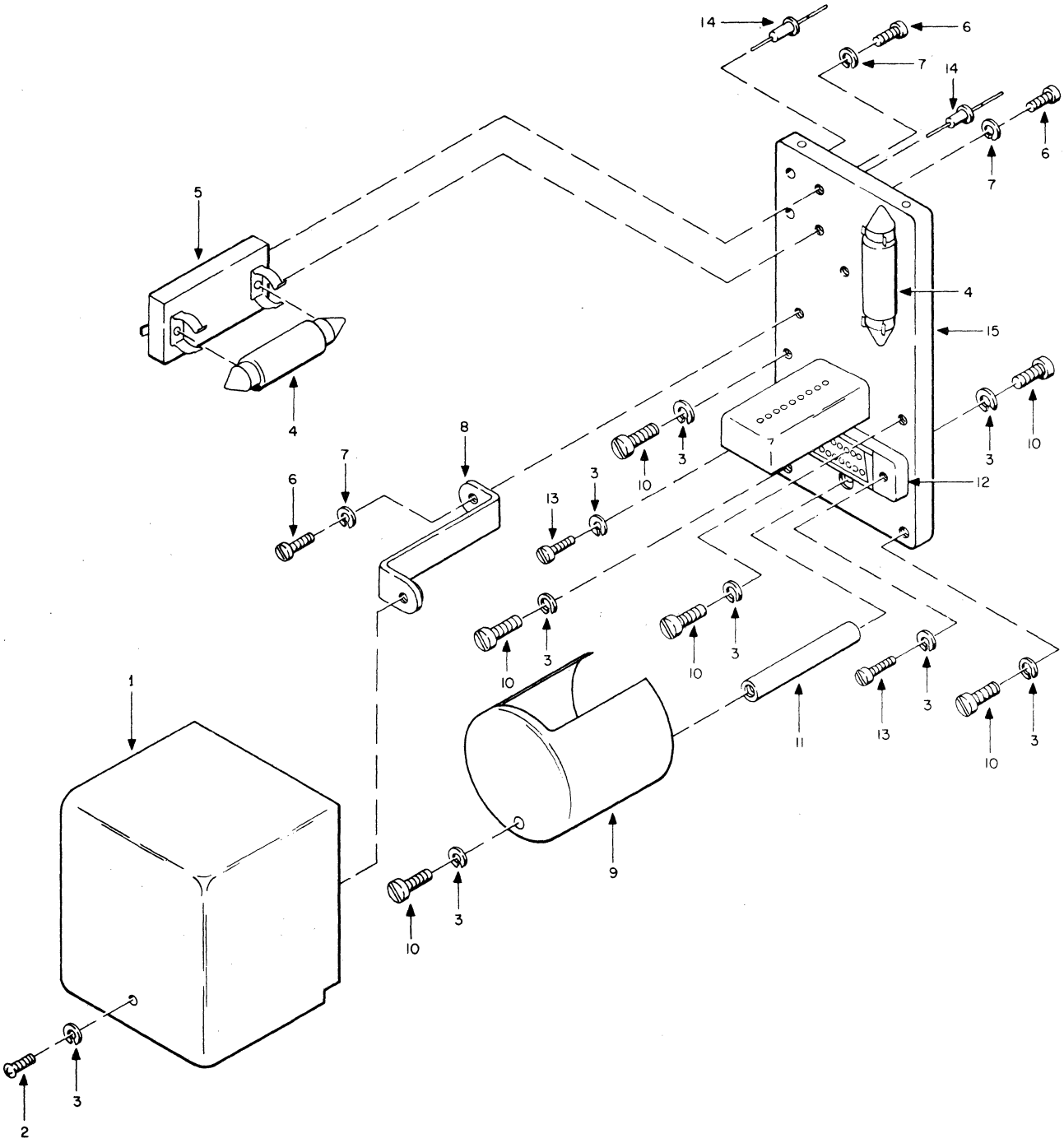


FIGURE 5-1 READ HEAD ASSEMBLY

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-1	B-C462	READ HEAD ASSEMBLY	1
-1	B-C999	. Cover, Exciter Lamp	1
-2	TH-SD0802	. Screw, #4-40 x 3/16 lg, PHM	1
-3	TH-WA0403	. Lockwasher, #4, Split	9
-4	TLNBE0004	. Lamp, Exciter, 12V, 10W, Osram #10-6411	1
-5	B-C461	. Holder Assembly, Lamp	1
-6	TH-SI1204	. Screw, #6-32 x 5/16 lg, BHM	3
-7	TH-WB0605	. Lockwasher, #6, Split	3
-8	B-B185	. Bracket Assembly	1
-9	B-A1321	. Cover, Head Block Assembly	1
-10	TH-SI0805	. Screw, #4-40 x 3/8 lg, BHM	6
-11	A-A1320	. Post	1
-12	TJMSO1548	. Connector, Cannon DA15P	1
-13	TH-SI0802	. Screw, #4-40 x 3/16 lg, BHM	2
-14	TJMS00162	. Plug, Sealtron FT-M-2	2
-15	B-A1436	. Base Plate	1

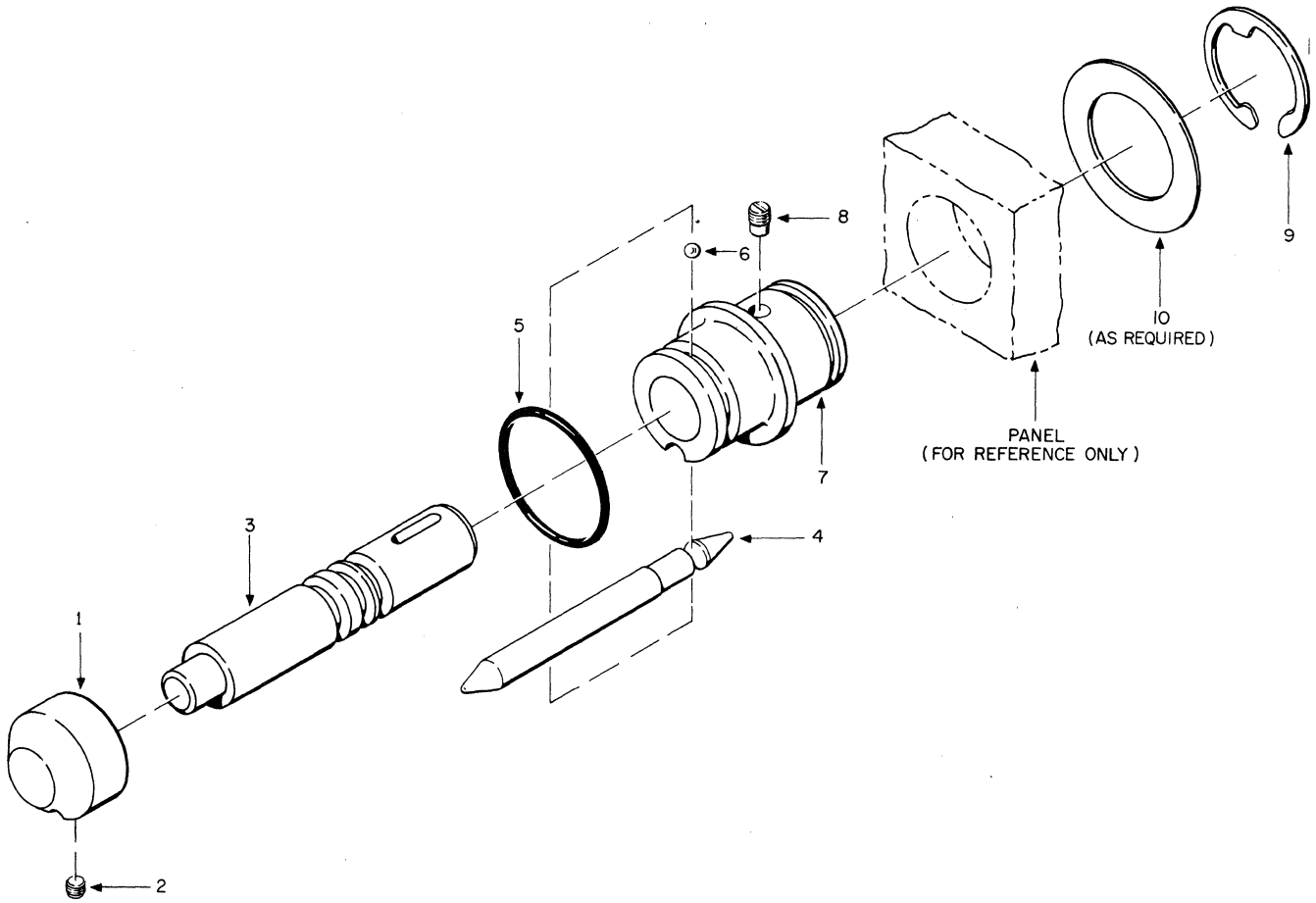


FIGURE 5-2 TAPE GUIDE ASSEMBLY

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-2	B-C726	TAPE GUIDE ASSEMBLY	2
-1	B-A1806	. Nose, Adjustable Guide	1
-2	TH-XC1201	. Screw, #6-32 x 1/8 lg, Sock Hd, Cup Pt.	1
-3	B-A1807	. Shaft, Adjustable Guide	1
-4	A-A699	. Arm, Guide Post	1
-5	S-22-1	. "O" Ring	1
-6	S-120-3	. Ball, Stainless Steel	1
-7	B-A1805	. Body, Adjustable Guide	1
-8	A-A1810	. Screw, #8-32 x 1/4 lg, Sock Hd, Set, Modified	1
-9	TTREA1215	. Ring, Retaining, Bowed, KOH-I-NOOR 5131-62W	1
-10	A-A1860	. Shim, (As Required)	1

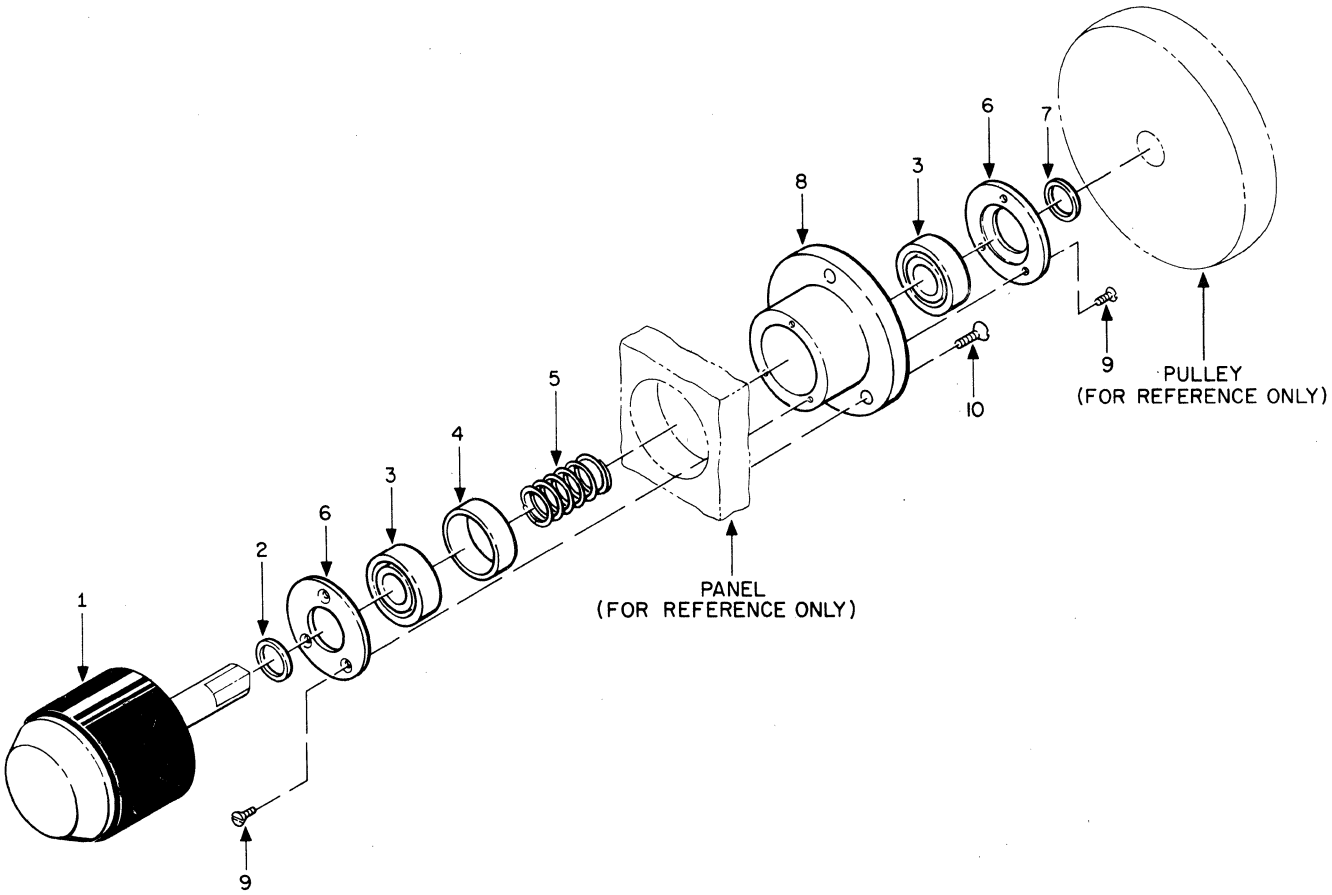


FIGURE 5-3 CAPSTAN ASSEMBLY

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-3	A-C78	CAPSTAN ASSEMBLY	2
-1	B-B127	. Capstan Sub-Assembly	1
-2	A-A2806-1	. Spacer	1
-3	S-119	. Bearing	2
-4	A-A2802	. Spacer, Bearing	1
-5	A-A2803	. Spring	1
-6	A-A2805	. Retainer	2
-7	A-A2806-2	. Spacer	1
-8	A-A2801	. Collar, Capstan Bearing	1
-9	TH-SG0303	. Screw, #2-56 x 1/4 lg, FHM	6
-10	TH-SG1214	. Screw, #6-32 x 1/2 lg, FHM	3

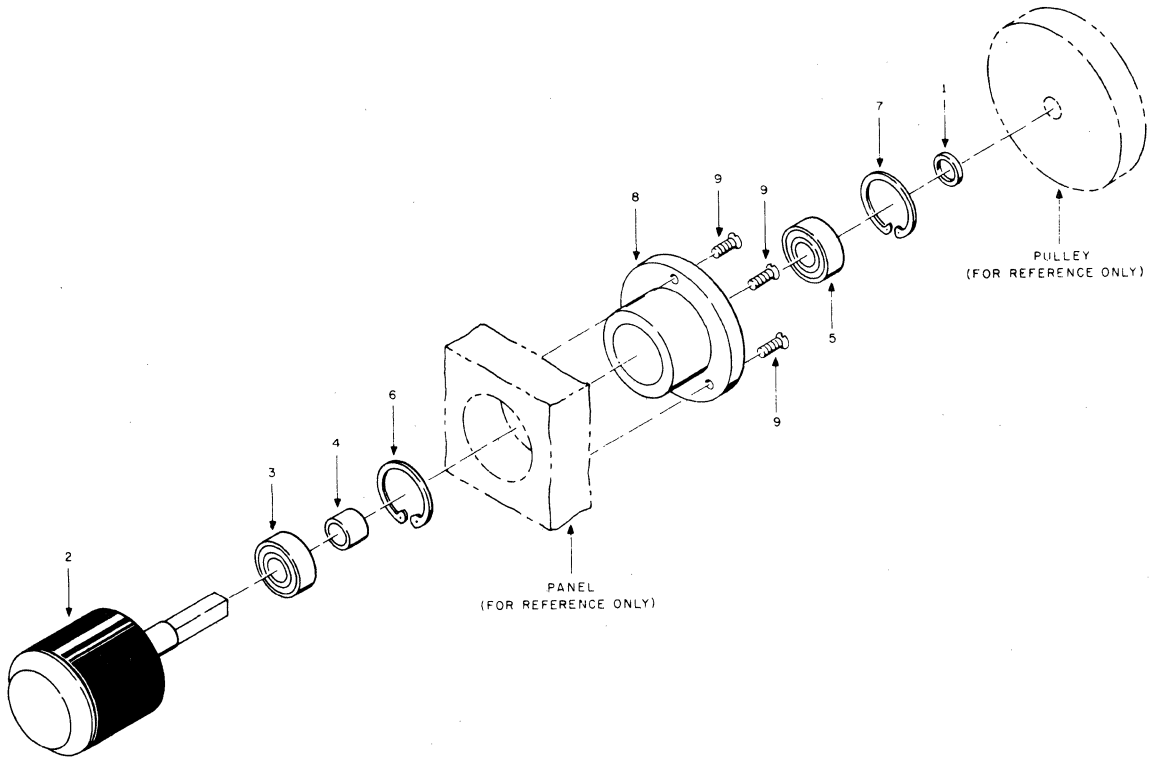


FIGURE 5-3A CAPSTAN ASSEMBLY

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-3A	*A-C78	CAPSTAN ASSEMBLY	2
-1	A-A1071-3	. Spacer, Pulley	1
-2	B-B127	. Capstan, Sub-Assembly	1
-3	A-1073-1	. Bearing, Inch Ball	1
-4	A-A1071-2	. Spacer, Bearing	1
-5	A-1073-1	. Bearing, Inch Ball	1
-6	A-1071-3	. Ring, Retaining, Internal (Flat)	1
-7	A-1071-4	. Ring, Retaining, Internal (Bowed)	1
-8	B-A1070	. Collar	1
-9	Coml	. Screw, #6-32 x 1/2 lg., FHM	3

*Alternate assembly used on some older models. New assembly (5-3) can be used as a direct replacement. Use this figure to re-order sub-assemblies.

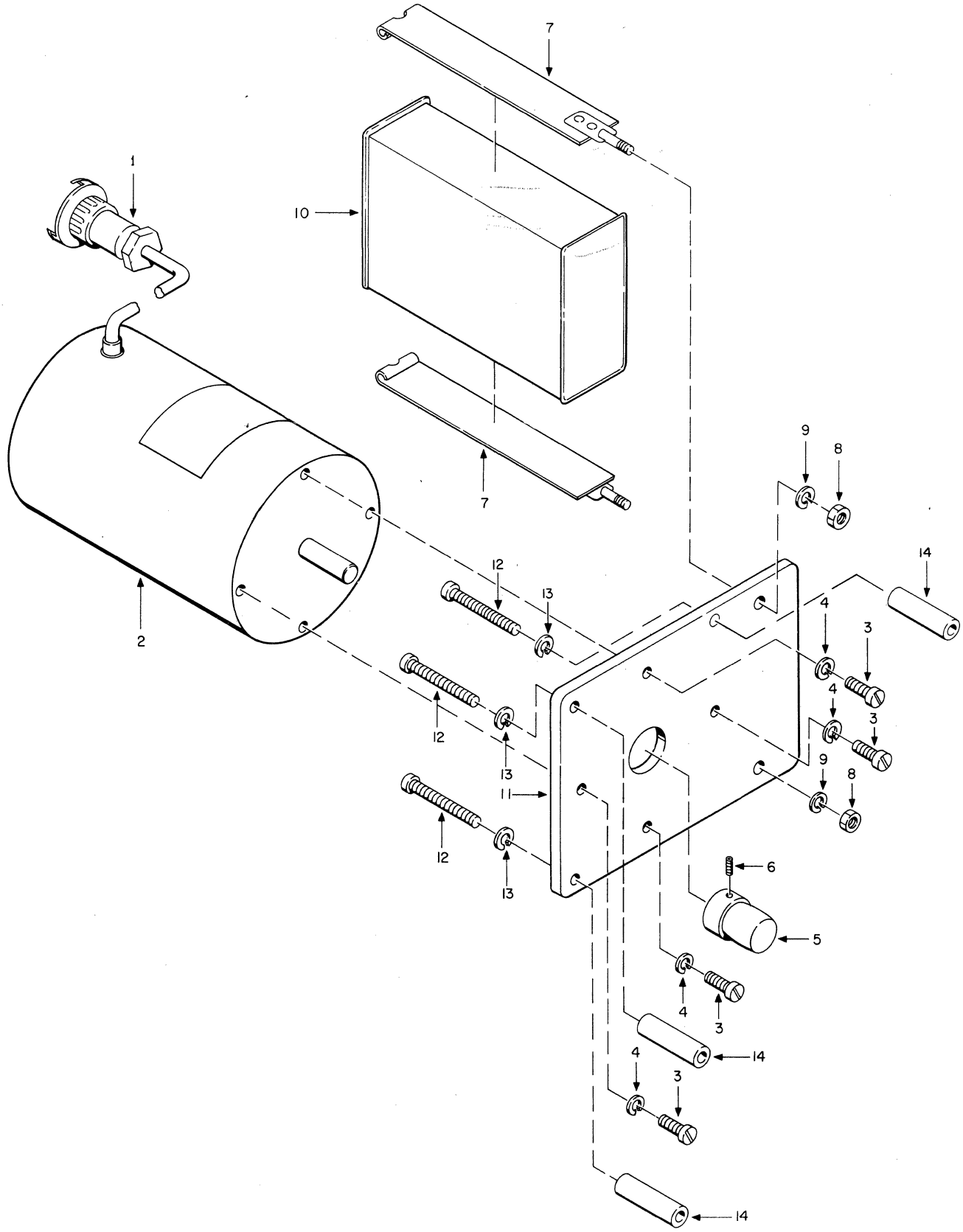


FIGURE 5-4 DRIVE MOTOR ASSEMBLY

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-4	See List of Variations	DRIVE MOTOR ASSEMBLY	1
-1	TPMS00722	Plug and Hood, Winchester M7P-LSH-19C	1
-2	See List of Variations	. Drive Motor	1
-3	TH-SI1710	. Screw, #10-32 x 7/8 lg., BHM	4
-4	TH-WB0810	. Lockwasher, #10, Split	4
-5	See List of Variations	. Pulley, Motor	1
-6	TH-XC1402	. Screw, #8-32 x 3/16 lg., Allen Hd., Cup Pt, Set	1
-7	A-1261-3	. Bracket, Capacitor	2
-8	TH-NB1608	. Nut, #10-32, Hex	2
-9	TH-WB0810	. Lockwasher, #10, Split	2
-10	See List of Variations	. Capacitor, Drive Motor	1
-11	A-A1381	. Plate, Motor Mounting	1
-12	TH-SI1716	. Screw, #10-32 x 1 7/8 lg., BHM	3
-13	TH-WB0810	. Lockwasher, #10, Split	3
-14	A-A1384	. Spacer, Motor Mount	3

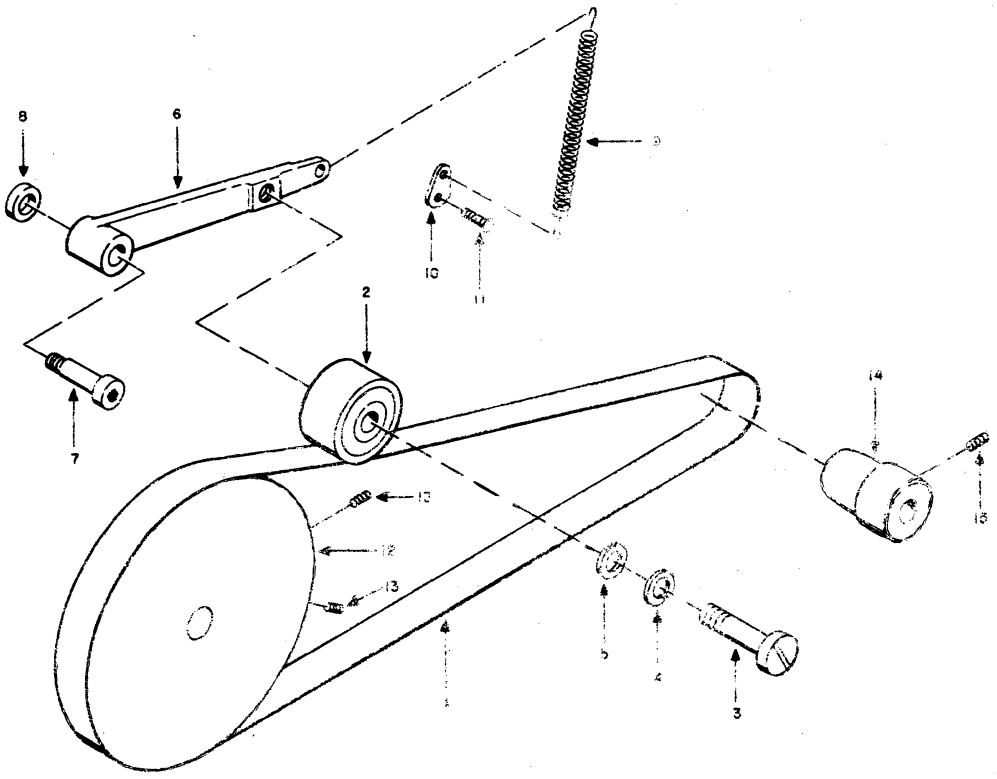


FIGURE 5-5 TAPE DRIVE SECTION (3500)

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-5	N/A	TAPE DRIVE SECTION (3500)	1
-1	See List of Variations	. Drive Belt	1
-2	A-A235-1	. Roller, Belt Tension Idler Arm	1
-3	Coml	. Screw, B.H., #10-32 x 7/8, S.S.	1
-4	Coml	. Washer, Lock Split, #10, S.S.	1
-5	Coml	. Spacer, #10, S.S.	1
-6	A-B32	. Idler Arm	1
-7	Coml	. Screw, Shoulder, Morton 9272	1
-8	Coml	. Spacer	1
-9	A-A188	. Spring, Belt Tension Idler Arm	1
-10	Coml	. Solder Lug, Internal Tooth, #6	1
-11	Coml	. Screw, B.H.D., #6-32 x 5/16, S.S.	1
-12	See List of Variations	. Capstan Pulley	1
-13	Coml	. Setscrew, Socket hd., Cup Pt., #8-32 x 3/8	2
-14	See List of Variations	. Motor Pulley	1
-15	Coml	. Setscrew, Socket hd., Knurled Pt., #8/32 x 3/16	1

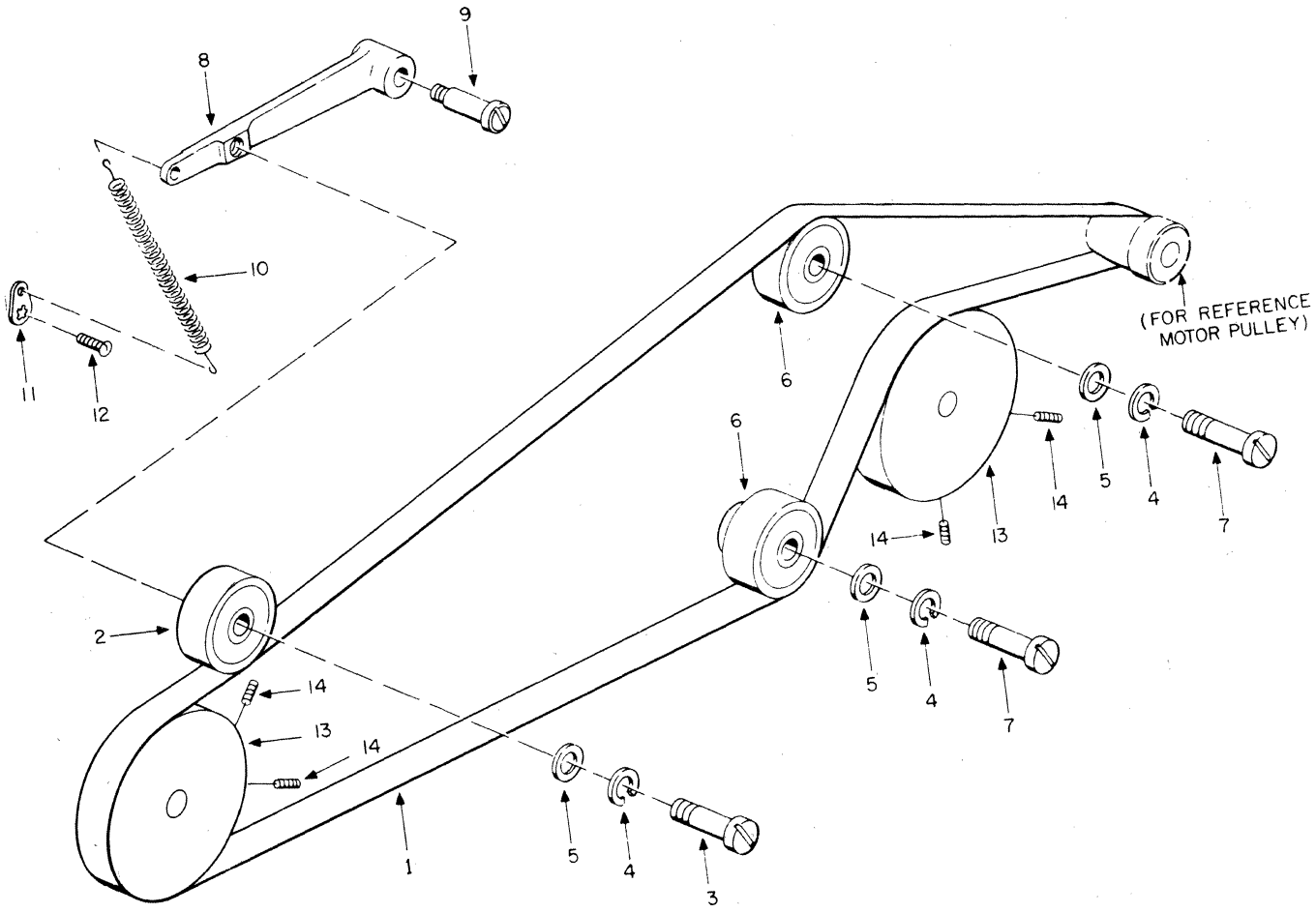


FIGURE 5-5A TAPE DRIVE SECTION (B3500)

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-5A	N/A	TAPE DRIVE SECTION (B3500)	1
-1	See List of Variations	. Belt, Drive	1
-2	A-A235-1	. Tension Roller, Idler, Belt	1
-3	TH-SI1710	. Screw, #10-32 x 7/8 lg., BHM	1
-4	TH-WB0815	. Lockwasher, #10, Split	3
-5	TH-WA0814	. Washer, #10, Light, Plain, Flat	4
-6	A-A235-2	. Roller, Idler, Belt	2
-7	TH-SI1712	. Screw, #10-32 x 1 1/8 lg., BHM	2
-8	A-B32	. Idler Arm, Belt	1
-9	TH-XE1705	. Screw, Shoulder, #10-32 x 1 1/16 lg., w/5/8" Shoulder, Morton 9272	1
-10	A-A188	. Spring, Tension Belt	1
-11	TH-WC0609	. Solder Lug, #6, Internal Tooth	1
-12	TH-SI1203	. Screw, #6-32 x 1/4 lg., BHM	1
-13	See List of Variations	. Pulley, Capstan	2
-14	TH-XC1405	. Screw, #8-32 x 3/8 lg., Allen Hd. Cup Pt., Set	4

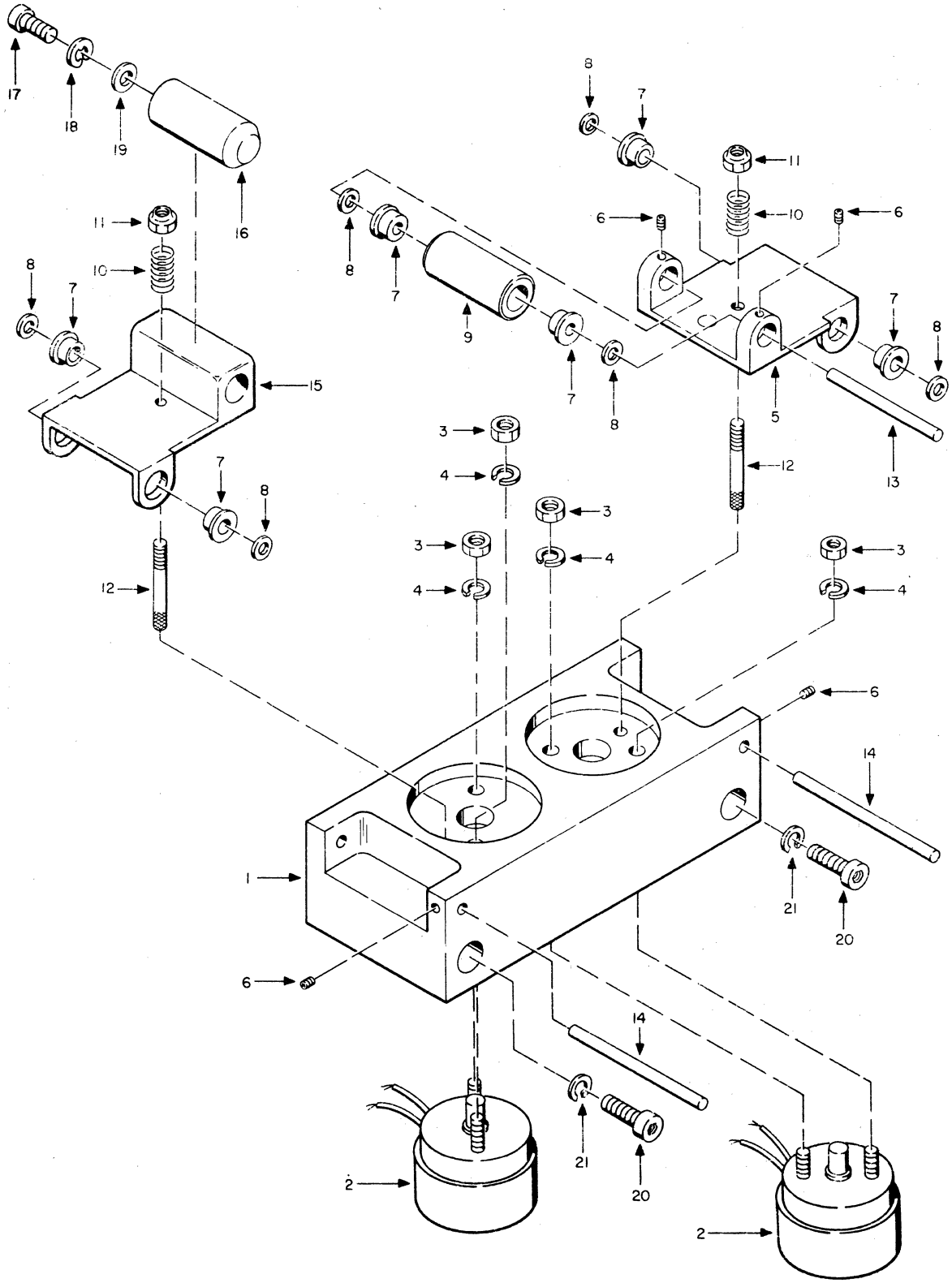


FIGURE 5-6 PINCH ROLLER AND LOW-SPEED BRAKE ASSEMBLY (B3500)

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-6	C-C86-4 (LH) C-C86-3 (RH)	PINCH ROLLER & LOW SPEED BRAKE ASSEMBLY (B3500)	1 of L Hand 1 of R Hand
-1	C-A472	. Mount, Solenoid	1
-2	A-B73-1	. Solenoid Assembly	1
-3	Coml	. Nut, #5-40, Hex.	4
-4	Coml	. Lockwasher, #6, Split	4
-5	B-A437	. Bracket, Roller	1
-6	Coml	. Screw, #4-40 x 1/8 lg., Allen Hd., Set, Cup Pt.	4
-7	A-1072-2	. Bearing, Miniature Ball	6
-8	A-1033	. Spacer	6
-9	A-A438-1	. Roller, Tape	1
-10	A-1160	. Spring, Compression	2
-11	Coml	. Nut, #5-40 NC 3B THD, Lock-ESNA	2
-12	A-1078-1	. Stud, Spring	2
-13	A-1014	. Shaft, Roller	1
-14	A-1199	. Shaft, Bracket	2
-15	B-A1100	. Brake, Bracket	1
-16	B-C428	. Brake Drum Assembly	1

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-6 Cont'd.	C-C86-4 (LH) C-C86-3 (RH)	PINCH ROLLER & LOW SPEED BRAKE ASSEMBLY (B3500)	
-17	Coml	. Screw, # 1/4-20 x 3/8 lg., Sock Hd. Cap	1
-18	Coml	. Lockwasher, #1/4, Split	1
-19	Coml	. Shim, (As Required)	
-20	Coml	. Screw, #10-32 x 1 lg., Sock Hd., Cap	2
-21	Coml	. Lockwasher, #10, Split	2

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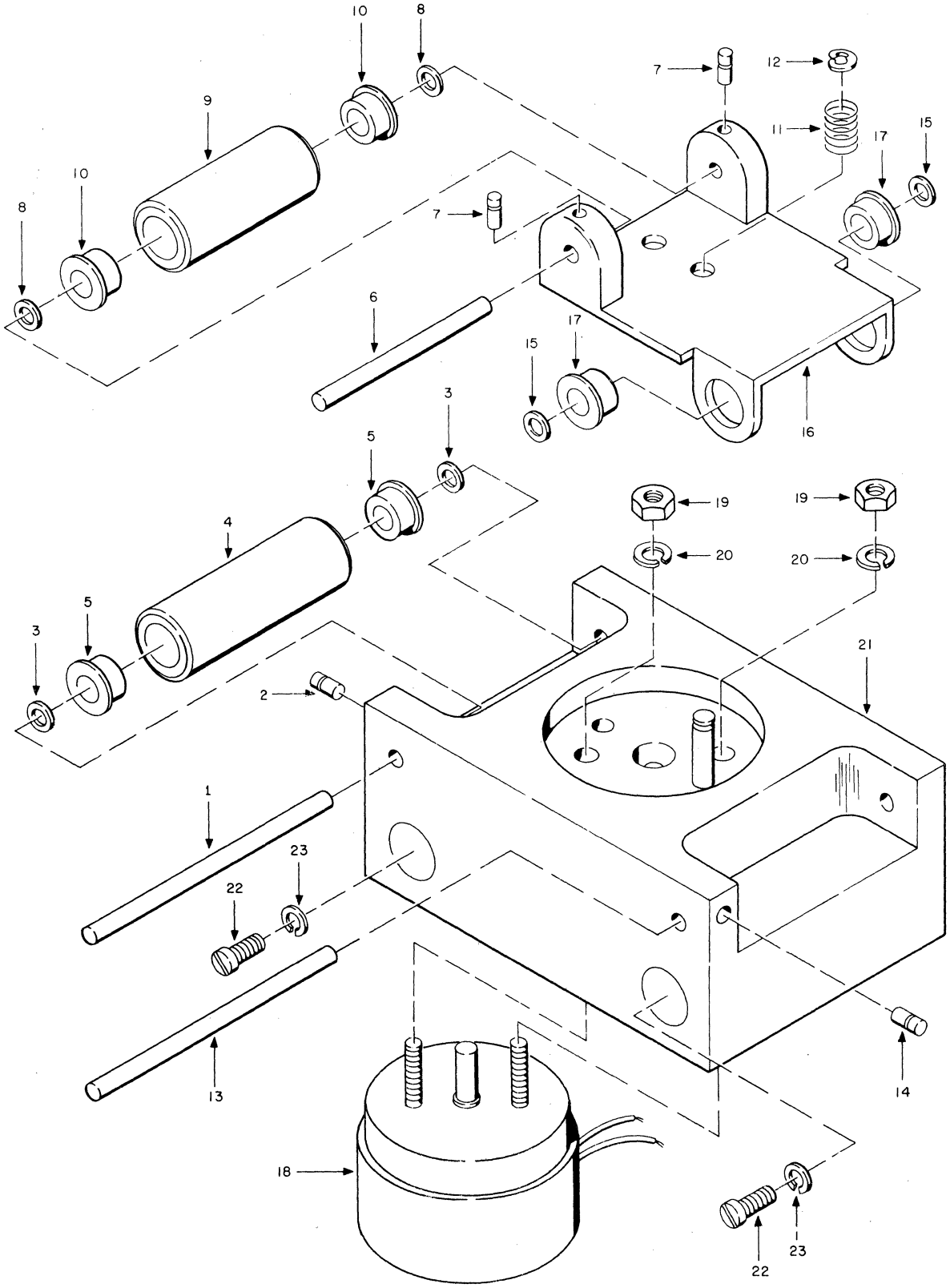

FIGURE 5-7 PINCH ROLLER ASSEMBLY (3500)

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-7	C-C81-5	PINCH ROLLER ASSEMBLY (3500)	1
-1	A-1199	. Shaft, Bracket	1
-2	Coml	. Setscrew, Socket hd., #4-40 x 1/8	1
-3	A-1033	. Spacer	2
-4	A-A438-2	. Roller, Tape	1
-5	A-1072-2	. Bearing, Miniature, Ball	2
-6	A-1014	. Shaft, Roller	1
-7	Coml	. Setscrew, Socket hd., #4-40 x 1/8	2
-8	A-1033	. Spacer	2
-9	A-A438-1	. Roller, Tape	1
-10	A-1072-2	. Bearing, Miniature, Ball	2
-11	A-1160	. Spring, Compression	1
-12	A-1070-4	. Retaining Ring, External	1
-13	A-1199	. Shaft, Bracket	1
-14	Coml	. Setscrew, Socket hd., #4-40 x 1/8	1
-15	A1033	. Spacer	2
-16	BA437	. Bracket, Roller	1
-17	A-1072-2	. Bearing, Miniature, Ball	2

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-7 Cont'd.	C-C81-5	PINCH ROLLER ASSEMBLY (3500)	
-18	A-B73-1	. Solenoid Assembly	1
-19	Coml	. Nut, Hexagonal #5-50, S.S.	2
-20	Coml	. Washer, Lock, Split, #6	2
-21	B-A435	. Mount, Solenoid	1
-22	Coml	. Screw, B.H., #4-40 x 3/8, S.S.	2
-23	Coml	. Washer, Lock, Split, #10, S.S.	2

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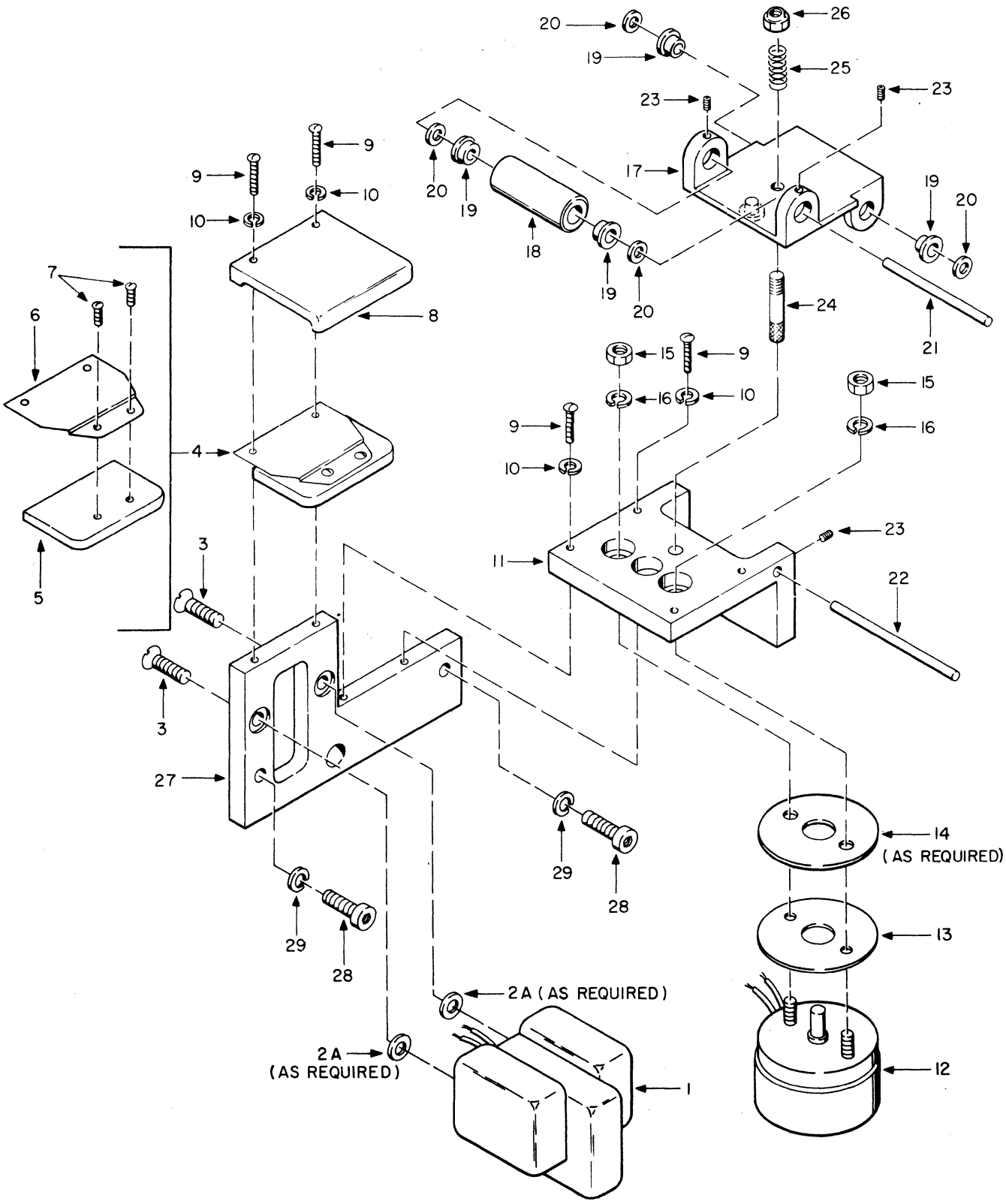

FIGURE 5-8 PINCH ROLLER AND HIGH-SPEED BRAKE ASSEMBLY (B3500)

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-6	C-C899 (LH) C-C888 (RH)	HIGH SPEED BRAKE & PINCH ROLLER MOUNT ASSEMBLY	1 of L Hand 1 of R Hand
-1	B-C890	. Coil Assembly	1
-2	A-A2200	. Spacer, (When Required)	2
-3	TH-SG1408	. Screw, #8-32 x 5/8 lg., FHM	2
-4	B-C889	. Armature Assembly	1
-5	A-A2058	. . Armature	1
-6	A-A2077	. . Spring	1
-7	TH-SI0801	. . Screw, #4-40 x 1/8 lg., BHM	2
-8	A-A2081	. Cover	1
-9	TH-SI0107	. Screw, #4-40 x 1/2 lg., BHM	2
-10	TH-WB0403	. Lockwasher, #4, Split	4
-11	B-A2076	. Solenoid Mount	1
-12	A-B73-1	. Solenoid Assembly	1
-13	A-A2080	. Spacer	1
-14	A-A2080	. Shim, (As Required)	
-15	TH-NB0905	. Nut, #5-40, Hex.	2
-16	TH-WB0605	. Lockwasher, #6, Split	2
-17	B-A437	. Roller (Bracket)	1
-18	A-A438-1	. Roller	1

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-8 Cont'd.	C-C899 (LH) C-C888 (RH)	HIGH SPEED BRAKE & PINCH ROLLER MOUNT ASSEMBLY (B3500)	
-19	A-1072-2	. Bearing, Miniature Ball	4
-20	A-1033	. Spacer	4
-21	A-1014	. Shaft, (Roller)	1
-22	A-1199	. Shaft (Bracket)	1
-23	Coml	. Screw, #4-40 x 1/8 lg., Allen Hd., Cup Pt., Set	3
-24	A-1078-2	. Spring, Stud	1
-25	A-1160	. Spring	1
-26	Coml	. Nut, #5-40, NC-3, Lock-ESNA	1
-27	B-A2074	. Base Plate	1
-28	Coml	. Screw, #10-32 x 1/2 lg., Sock Hd., Set	2
-29	Coml	. Lockwasher, #10, Split	2

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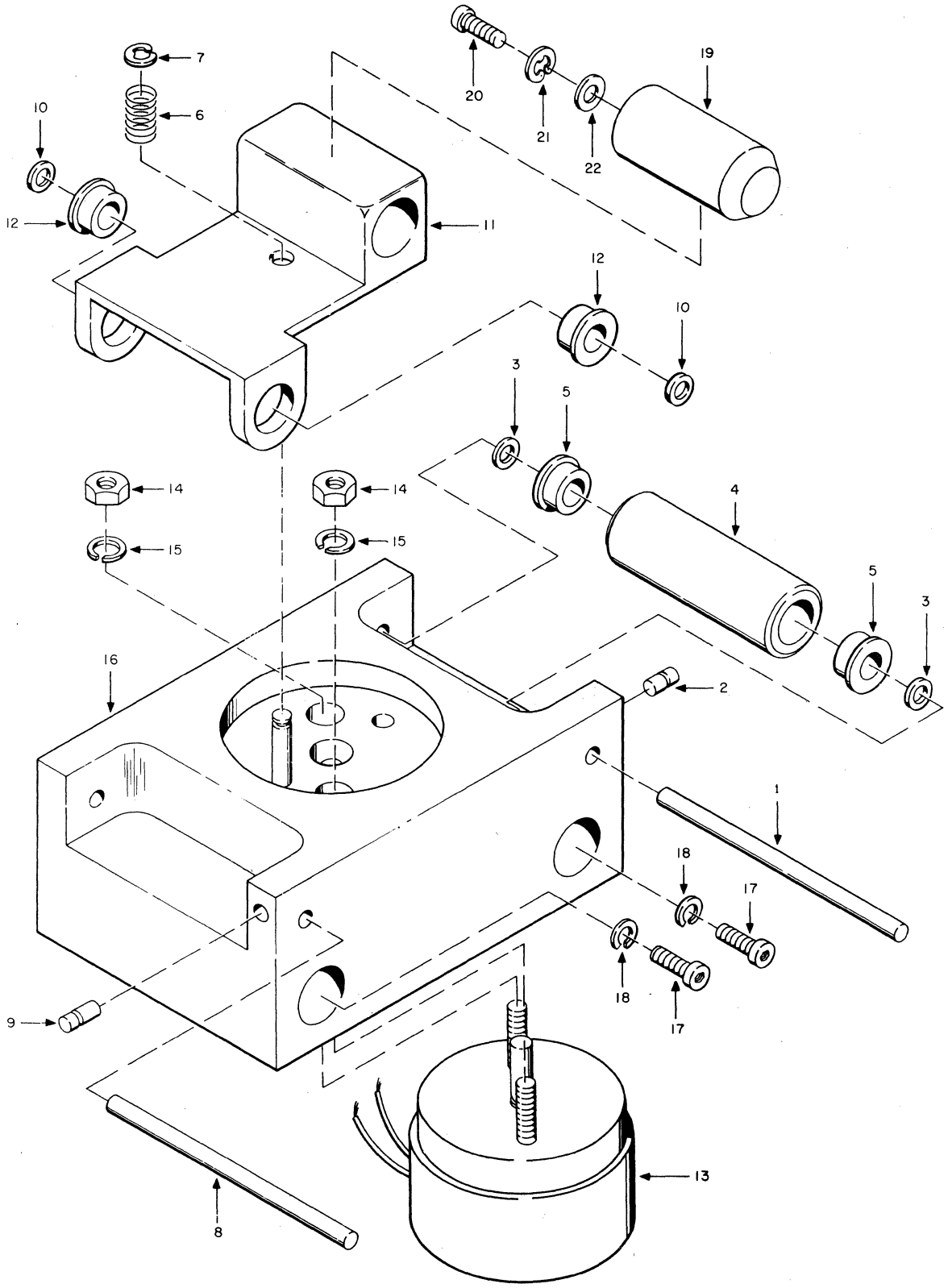

FIGURE 5-9 LOW-SPEED BRAKE ASSEMBLY (3500)

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-9	C-C79-5	BRAKE ASSEMBLY, LOW SPEED (3500)	1
-1	A-1199	. Shaft, Bracket	1
-2	Coml	. Setscrew, Socket hd., #4-40 x 1/8	1
-3	A-1033	. Spacer	2
-4	A-A438-2	. Roller, Tape	1
-5	A-1072-2	. Bearing, Miniature, Ball	2
-6	A-1160	. Spring, Compression	1
-7	A-1070-4	. Retaining Ring, External	1
-8	A-1199	. Shaft, Bracket	1
-9	Coml	. Setscrew, Socket hd., #4-40 x 1/8	1
-10	A-1033	. Spacer	2
-11	B-A1100	. Brake	1
-12	A-1072-2	. Bearing, Miniature, Ball	2
-13	A-B73-1	. Solenoid Assembly	1
-14	Coml	. Nut, Hexagonal, #5-40, S.S.	2
-15	Coml	. Washer, Lock, Split, #6	2
-16	B-A435	. Mount, Solenoid	1
-17	Coml	. Screw, Socket hd., #10-32 x 1, S.S.	2
-18	Coml	. Washer, Lock, Split, #10	2

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-9 Cont'd.	C-C79-5	BRAKE ASSEMBLY, LOW SPEED (3500)	
-19	B-C428	. Block, Brake	1
-20	Coml	. Screw, Socket hd., #1/4 20 x 3/4 lg.	1
-21	Coml	. Washer, Lock, Split, # 1/4	1
-22	Coml	. Spacer, Round #1/4, S.S.	1

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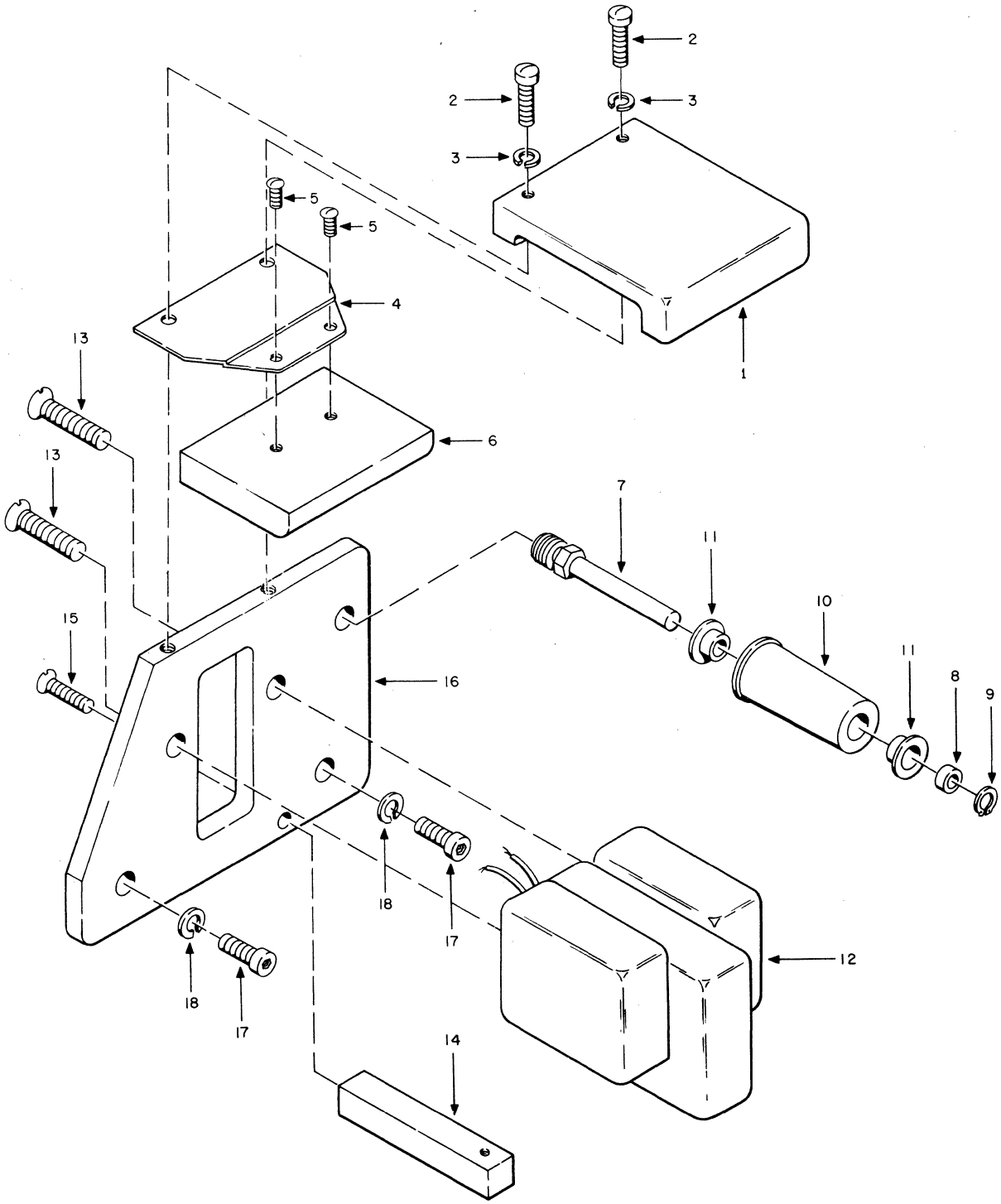


FIGURE 5-10 HIGH-SPEED BRAKE ASSEMBLY (3500)

FIG. & INDEX NO.	PART NUMBER	DESCRIPTION	UNITS PER ASSEMBLY
5-10	B-C894	BRAKE ASSEMBLY, HIGH SPEED (3500)	1
-1	A-A2081	. Cover	1
-2	Coml	. Screw, Phillips hd., #4-40 x 1/2, S.S.	2
-3	Coml	. Washer, Lock, Split, #4, S.S.	2
-4	A-A2077	. Armature Spring	1
-5	Coml	. Screw, #4-40 x 1/8, S.S., BHM	2
-6	A-A2058	. Armature	1
-7	A-B41	. Sub-Assembly, Shaft Stud	1
-8	A-A2200	. Spacer	1
-9	A-A2553	. Ring, Retainer, Grid	1
-10	A-1213	. Roller, Tapered	1
-11	Coml	. Bearing, Flanged, New Departure 77NM0820	1
-12	B-C890	. Coil Assembly	1
-13	Coml	. Screw, Flat hd., #8-32 x 5/8, S.S.	2
-14	A-A2128	. Spacer	1
-15	Coml	. Screw, Flat hd., #4-40 x 7/16, S.S.	1
-16	B-A2090	. Baseplate	1
-17	Coml	. Screw, Socket hd., #10-32 x 1/2, S.S.	2
-18	Coml	. Washer, Lock, Split, #10, S.S.	2

SPEED (CPS)	MOTOR ASSEMBLY	UNI-DIR. SPEED PKG	BI-DIR. SPEED PKG.
2000	C-C1371-6	B-C2227-5	B-C2227-13
1200	C-C1371-6	B-C2227-8	B-C2227-16
1000	C-C1371-6	B-C2227-4	B-C2227-12
900	C-C1371-6	B-C2227-7	B-C2227-15
800	C-C1371-6	B-C2227-6	B-C2227-14
600	C-C1371-6	B-C2227-3	B-C2227-11
500	C-C1371-2	B-C2227-4	B-C2227-12
450	C-C1371-2	B-C2227-7	B-C2227-15
400	C-C1371-2	B-C2227-6	B-C2227-14
333.3	C-C1371-10	B-C2227-5	B-C2227-13
300	C-C1371-2	B-C2227-3	B-C2227-11
250	C-C1371-4	B-C2227-4	B-C2227-12
225	C-C1371-4	B-C2227-7	B-C2227-15
200	C-C1371-4	B-C2227-6	B-C2227-14
166.6	C-C1371-10	B-C2227-4	B-C2227-12
150	C-C1371-4	B-C2227-3	B-C2227-11
133.3	C-C1371-10	B-C2227-6	B-C2227-14
100	C-C1371-10	B-C2227-3	B-C2227-11
75	C-C1371-4	B-C2227-1	B-C2227-9
66.6	C-C1371-10	B-C2227-2	B-C2227-10
50	C-C1371-10	B-C2227-1	B-C2227-9
2000/1000	C-C1371-1	B-C2227-5	B-C2227-13
2000/ 666.6	C-C1371-9	B-C2227-5	B-C2227-13
2000/ 500	C-C1371-3	B-C2227-5	B-C2227-13
1200/ 600	C-C1371-1	B-C2227-8	B-C2227-16
1200/ 400	C-C1371-9	B-C2227-8	B-C2227-16
1200/ 300	C-C1371-3	B-C2227-8	B-C2227-16
1000/ 500	C-C1371-1	B-C2227-4	B-C2227-12
1000/ 333.3	C-C1371-9	B-C2227-4	B-C2227-12
1000/ 250	C-C1371-3	B-C2227-4	B-C2227-12
900/ 450	C-C1371-1	B-C2227-7	B-C2227-15
900/300	C-C1371-9	B-C2227-7	B-C2227-15
900/ 225	C-C1371-3	B-C2227-7	B-C2227-15
800/ 400	C-C1371-1	B-C2227-6	B-C2227-14
800/ 266.6	C-C1371-9	B-C2227-6	B-C2227-14
800/ 200	C-C1371-3	B-C2227-6	B-C2227-14
666.6/333.3	C-C1371-11	B-C2227-5	B-C2227-13
600/ 300	C-C1371-1	B-C2227-3	B-C2227-11
600/ 200	C-C1371-9	B-C2227-3	B-C2227-11
600/ 150	C-C1371-3	B-C2227-3	B-C2227-11
500/ 333.3	C-C1371-7	B-C2227-5	B-C2227-13
500/ 250	C-C1371-5	B-C2227-4	B-C2227-12
500/ 166.6	C-C1371-8	B-C2227-4	B-C2227-12
450/ 225	C-C1371-5	B-C2227-7	B-C2227-15

SPEED (CPS)	MOTOR ASSEMBLY	UNI-DIR. SPEED PKG	BI-DIR. SPEED PKG.
450/ 150	C-C1371-8	B-C2227-7	B-C2227-15
400/ 200	C-C1371-5	B-C2227-6	B-C2227-14
400/ 133.3	C-C1371-8	B-C2227-6	B-C2227-14
400/ 100	C-C1371-3	B-C2227-2	B-C2227-10
333.3/166.6	C-C1371-11	B-C2227-4	B-C2227-12
300/ 200	C-C1371-7	B-C2227-8	B-C2227-16
300/ 150	C-C1371-5	B-C2227-3	B-C2227-11
300/ 100	C-C1371-8	B-C2227-3	B-C2227-11
300/ 75	C-C1371-3	B-C2227-1	B-C2227-9
266.6/133.3	C-C1371-11	B-C2227-6	B-C2227-14
250/ 166.6	C-C1371-7	B-C2227-4	B-C2227-12
225/ 150	C-C1371-7	B-C2227-7	B-C2227-15
200/ 133.3	C-C1371-7	B-C2227-6	B-C2227-14
200/ 100	C-C1371-11	B-C2227-3	B-C2227-11
200/ 66.6	C-C1371-8	B-C2227-2	B-C2227-10
150/ 100	C-C1371-7	B-C2227-3	B-C2227-11
150/ 75	C-C1371-5	B-C2227-1	B-C2227-9
150/ 50	C-C1371-8	B-C2227-1	B-C2227-9
133.3/66.6	C-C1371-11	B-C2227-2	B-C2227-10
100/ 66.6	C-C1371-7	B-C2227-2	B-C2227-10
100/ 50	C-C1371-11	B-C2227-1	B-C2227-9
75/ 50	C-C1371-7	B-C2227-1	B-C2227-9

DIGITRONICS
ALBERTSON, NEW YORK

TITLE:

READER SPEED REFERENCE CHART

USED ON: 10015

DRAWING NO. B-C2314

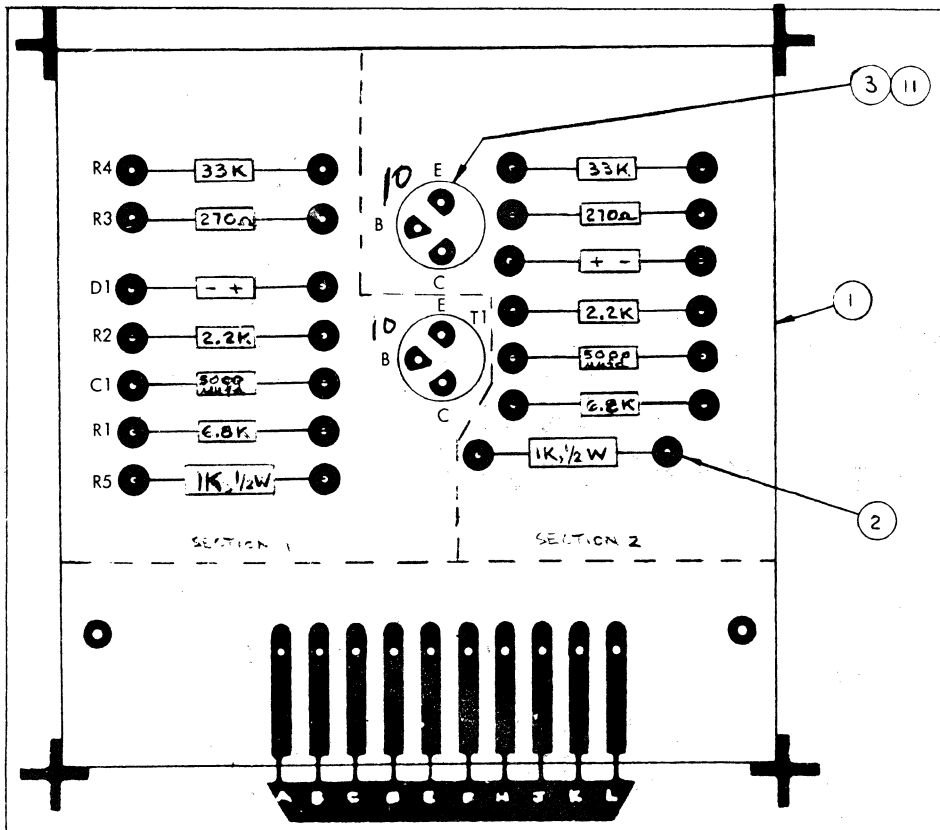
BI-DIRECTIONAL QUANTITY								UNI-DIRECTIONAL QUANTITY								DESCRIPTION	PART NO.	ITEM
—	-	-	-	-	-	-	1	-	-	-	-	-	-	-	1	MOTOR PULLEY (.259DIA.)	A-A3100-1	1
-	-	-	-	-	-	1	-	-	-	-	-	-	-	1	-	MOTOR PULLEY (.359DIA.)	A-A2418	2
-	-	-	-	-	1	-	-	-	-	-	-	-	1	-	-	MOTOR PULLEY (.538DIA.)	B-A2252-2	3
-	-	-	1	1	-	-	-	-	-	-	1	1	-	-	-	MOTOR PULLEY (.654DIA.)	B-A2252-1	4
-	-	1	-	-	-	-	-	-	-	1	-	-	-	-	-	MOTOR PULLEY (.670DIA.)	B-A2252-3	5
-	1	-	-	-	-	-	-	-	1	-	-	-	-	-	-	MOTOR PULLEY (.756DIA.)	B-A2252-6	6
1	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	MOTOR PULLEY (1.093DIA.)	B-A2252-8	7
																		8
																		9
																		10
2	-	-	-	-	2	2	2	1	-	-	-	-	1	1	1	CAPSTAN PULLEY (2.762DIA.)	A 1318	11
-	-	-	-	2	-	-	-	-	-	-	-	1	-	-	-	CAPSTAN PULLEY (2.000DIA.)	A-A1001	12
-	-	-	2	-	-	-	-	-	-	-	1	-	-	-	-	CAPSTAN PULLEY (.890DIA.)	A-A473-6	13
-	2	2	-	-	-	-	-	-	1	1	-	-	-	-	-	CAPSTAN PULLEY (2.564DIA.)	A-A473-1	14
																		15
																		16
																		17
-	-	-	-	-	-	-	-	-	1	1	-	-	1	1	1	BELT (13 ½ LG)	B-A2253-8	18
-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	BELT (12 ½ LG)	B-A2253-7	19
-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	BELT (10 3/4 LG)	B-A2253-10	20
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	BELT (11" LG)	B-A2253-17	21
-	-	-	-	-	-	1	1	-	-	-	-	-	-	-	-	BELT (30 ½ LG)	B-A2253-14	22
-	1	-	-	-	1	-	-	-	-	-	-	-	-	-	-	BELT (31" LG)	B-A2253-11	23
-	-	-	1	1	-	-	-	-	-	-	-	-	-	-	-	BELT (27" LG)	B-A2253-15	24
-	-	-	1	1	-	-	-	-	-	-	-	-	-	-	-	BELT (29 1/8 LG)	B-A2253-2	25
-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	BELT (30 3/4 LG)	B-A2253	26
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	BELT (31 ½ LG)	B-A2253-18	27
—	—	—	—	—	—	—	—	1	—	—	—	—	—	—	—	BELT (14 LG)	B-A2253-4	28
																		29
-	-	-	-	-	-	3	3	-	-	-	-	-	-	3	3	SPACER, MOTOR MOUNT	A-A2495-3	30
3	3	3	3	3	3	-	-	3	3	3	3	3	3	-	-	SPACER, MOTOR MOUNT	A-A1384	31
																		32
C-02227-16	C-02227-15	C-02227-14	C-02227-13	C-02227-12	C-02227-11	C-02227-10	C-02227-9	C-02227-8	C-02227-7	C-02227-6	C-02227-5	C-02227-4	C-02227-3	C-02227-2	C-02227-1			

DIGITRONICS
ALBERTSON, NEW YORK

TITLE: SPEED PACKAGE

USED ON:

DRAWING NO. CC2227



QUAN	DESCRIPTION	DWG NO.	ITEM
1	P.C. MASTER	P-C157	1
40	EYELET	S-179-1	2
8	EYELET	S-179-2	3
2	RESISTOR 2.2K, ¼W, 5%		4
2	" 6.8K, " "		5
2	" 270Ω, " "		6
2	" 33K, " "		7
2	" 68K, " "		8
2	" 1K, ½W, "		9
2	TRANSISTOR GT1170		10
	TRANSISTOR SPACER	S181	11
2	CAPACITOR 5000 mmfd CERAMIC 100 J ±30%		12
			13
2	DIODE GTDX3		14
			15
			16

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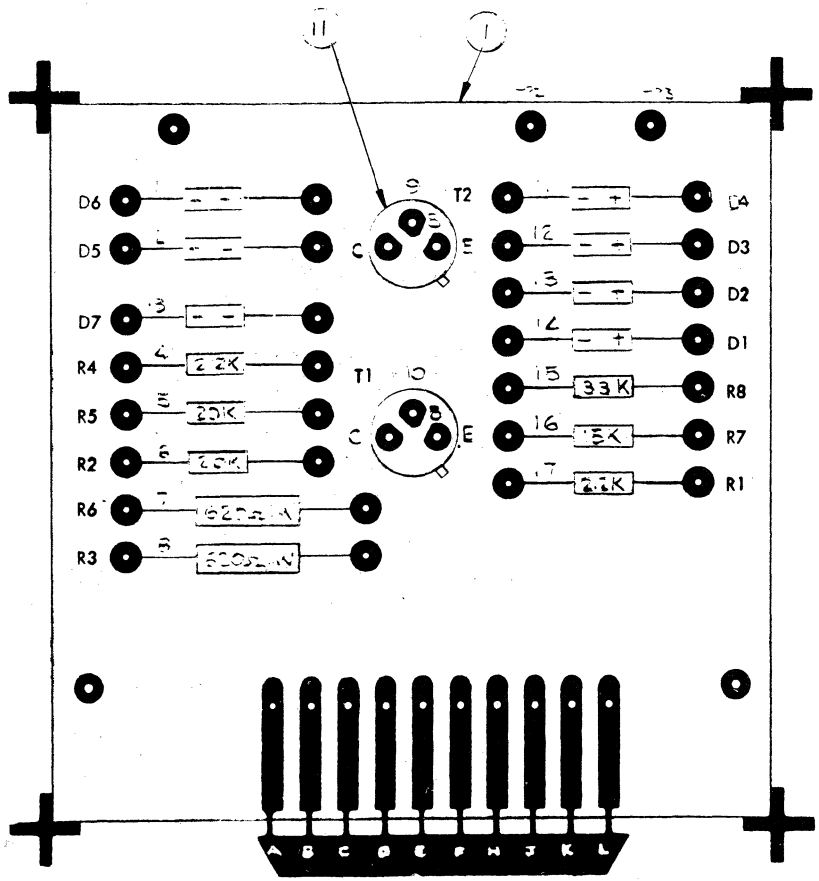
DIGITRONICS
ALBERTSON, NEW YORK

FIGURE 5-11

SSA ASSEMBLY DRAWING



LOCATION	QUAN	DESCRIPTION	DWG. NO.	ITEM
	1	PC MASTER	P-C 52A	1
5, 6	2	RESISTOR 20K 1/4W 5%		2
4, 17	2	RESISTOR 2.2K 1/4W 5%		3
15	1	RESISTOR 33K 1/4W 5%		4
7, 8	2	RESISTOR 620Ω 1W 5%		5
16	1	RESISTOR 15K 1/4W 5%		6
1, 2, 3, 11, 12, 13, 14	7	DIODE GTDX3		7
				8
9, 10	2	TRANSISTOR GT1170		9
				10
	2	TRANSISTOR SPACER	S-181	11

DIGITRONICS
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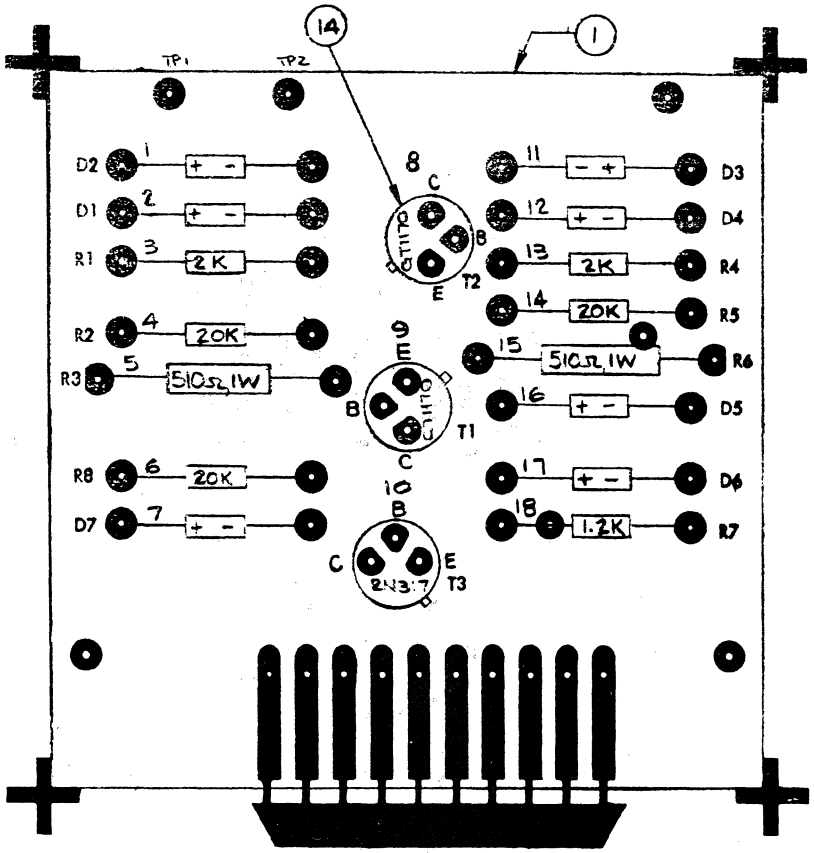
TITLE:

FIGURE 5-12

FRA ASSEMBLY DRAWING



LOCATION	QTY	DESCRIPTION	DWG. NO.	ITEM
	1	P.C. MASTER	P-C 1514	1
3, 13	2	RESISTOR 2K, 1/4W, 5%		2
				3
4,6, 14	3	" 20K, " "		4
18	1	" 1.2K, " "		5
5, 15	2	" 510Ω, 1W, "		6
				7
1,2,11,12,16, 17	6	DIODE GTDX3		8
7	1	" GT230		9
				10
8, 9	2	TRANSISTOR GT1170		11
10	1	" 2N317		12
				13
	3	TRANSISTOR SPACER	5181	14

SEE SCHEMATIC ~~FIGURE~~ 5-[illegible]0

DIGITRONICS
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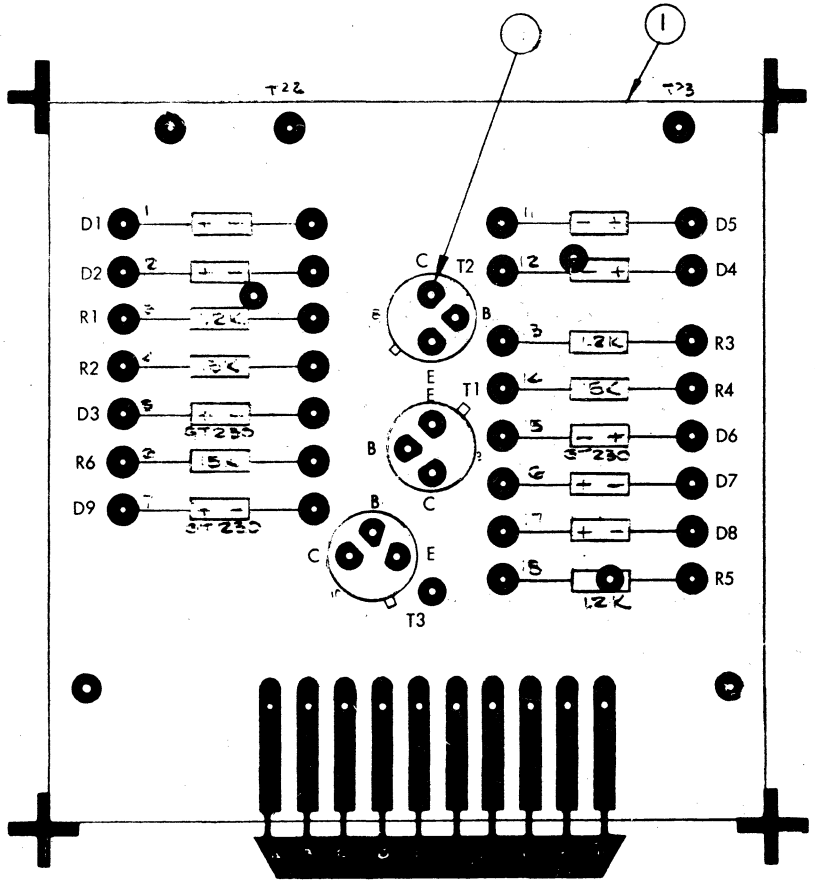
FIGURE 5-13
FRB ASSEMBLY DRAWING



LOCATION	QUAN.	DESCRIPTION	DWG NO.	ITEM
	1	P.C. MASTER "SDA"	P-C-53A	1
3, 13, 18	3	RESISTOR 12K 1/4W 5%		2
4, 6, 14	3	" 15K " "		3
				4
12, 16, 17	6	DIODE GTDX3		5
5, 7, 15	3	" GT230		6
				7
8, 9, 10	3	TRANSISTOR 2N317		8
	3	TRANSISTOR SPACER	S-181	11
				12

SEE SCHEMATIC FIGURE 5-2

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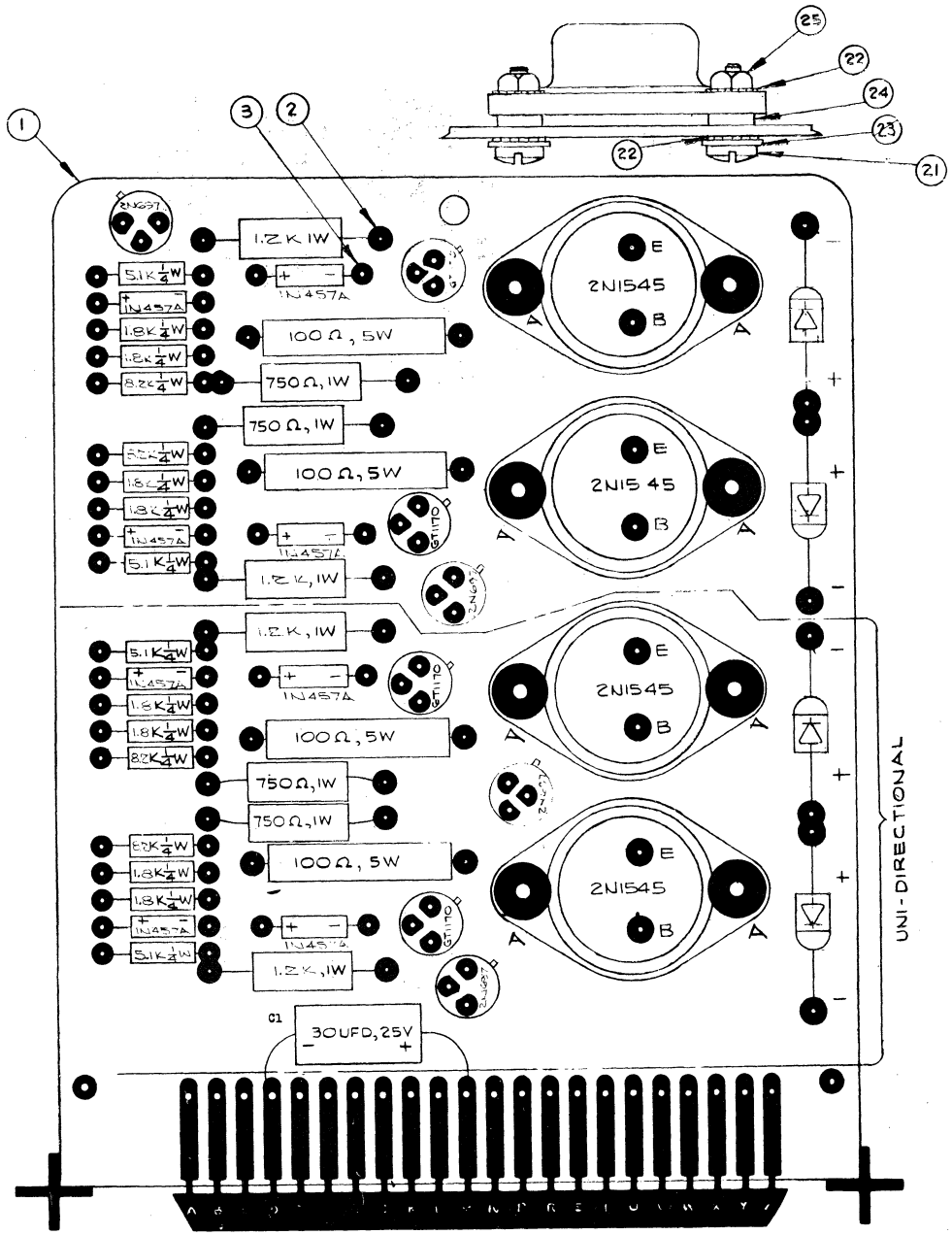
FIGURE 5-14
SDA ASSEMBLY DRAWING



QUAN	QUAN	DESCRIPTION	DWG. NO.	ITEM
1	1	P.C. BOARD MODIFIED (P-C231A)	C-A2413	1
62	62	EYELET TY-SA0001	S-179-1	2
75	75	" TY-SA0002	S-179-2	3
8	4	TRANSISTOR SPACER TQSA00001	S-181	4
4	2	" GT1170 TQ-SA1170		5
4	2	" ENG97 TQ-SD0697		6
4	2	" 2N1545 TQ-PA1545		7
1	1	CAPACITOR 30UFD 25V ILLINOIS*SMT-3025 TGHF306		8
8	4	DIODE IN457A TCRS5457A		9
4	2	" IN2069A TCRP2069A		10
				11
4	2	RESISTOR 100Ω, 5W, 5% SPRAGUE #243E1015 TR-WE10K		12
4	2	" 1.2K, 1W, "	TR-CC122C	13
4	2	" 750Ω, 1W, "	TR-CC751C	14
4	2	" 5.1K, 1/4W, "	TR-CA512C	15
8	4	" 1.8K, "	TR-CA182C	16
				17
4	2	" 8.2K, "	TR-CA823C	18
				19
				20
8	4	SCREW #4-40X7/16 LG BHM SS	TH-SI0806	21
16	8	LOCKWASHER # 4 EXT. TOOTH SS	TH-WC0407	22
8	4	WASHER # 4 PLAIN	TH-WA0409	23
8	4	" # 4 FLAT FIBRE H.H. SMITH #2161	TH-YA0406	24
8	4	NUT, HEX # 4-40 1/4 ACROSS FLATS S.S.	TH-NB0703	25
				26

BI-DIRECTIONAL (4 CIRCUITS) C-C1367-2

UNI-DIRECTIONAL (2 CIRCUITS) C-C1367-1

NOTE:
1. INSTALL ITEMS 2 & 3 FROM OPPOSITE SIDE.
2. DRILL 1/8 DIA FOR HOLES MARKED "A", 8 HOLES.

ASSEMBLY	SCHEMATIC
C-C1367-1	B-H542-1
C-C1367-2	B-H542-2

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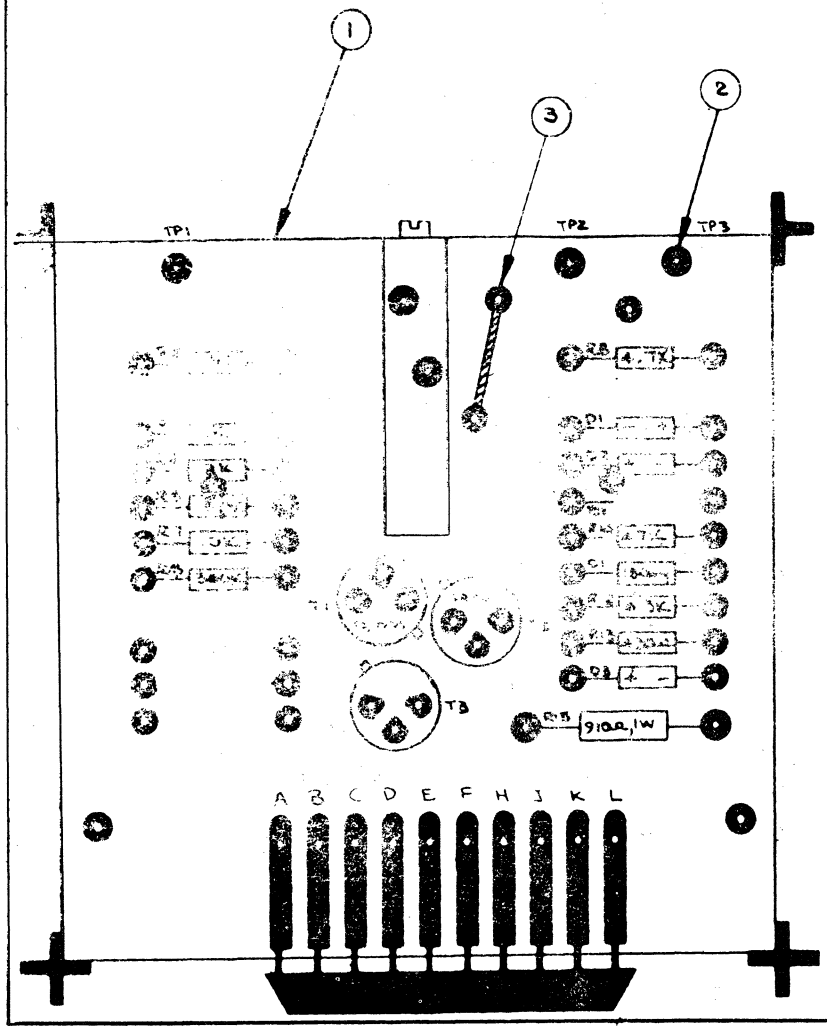
NEW YORK

FIGURE 5-15
SPA-A-UNI or SPA-A-BI
ASSEMBLY DRAWING

10015 | C-C1367



ITEM	DESCRIPTION	DWG. NO.	QUAN
1	P.C. MASTER	P-C 233	1
2	EYELET	S-179-1	18
3	"	S-179-2	54
4	TRANSISTOR SPACER	S-181	3
5	" 2A004 T1, T2		2
6	" GT1170 ① PHILCO 2N598 ② T3		1
7	RESISTOR 200K ADJ, ALLEN-BRADLEY TYPE RP	R1	1
8	" 910Ω, 1W, 5%	R15	1
9	" 18K, 1/4W, 5%	R2	1
10	" 1K, " "	R3	1
11	" 2K, " "	R4	1
12	" 150K, " "	R5	1
13	" 300K, " "	R6	1
14	" 10K, " "	R7	1
15	" 4.7K, " "	R8	1
16			
17			
18	" 4.3K " "	R12	1
19	" 430Ω " "	R13	1
20	" 47K " "	R14	1
21			
22	CAPACITOR 180 mmfd CM15	C1	1
23	DIODE GTDX3	D1,D2,D3	3
24			
25			
27	WIRE #20 SOLID .550 C/C		1

SEE SCHEMATIC FIGURE 5-14

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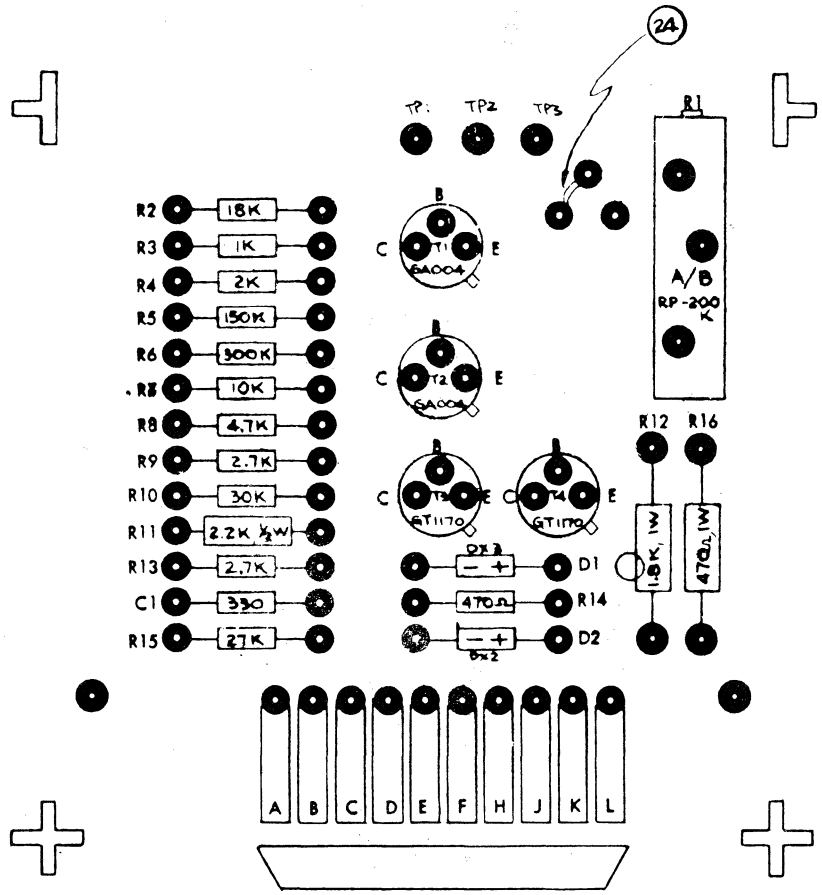
FIGURE 5-16
PGF-A, PGL-A ASSEMBLY DRAWINGS
① ②



ITEM	DESCRIPTION	DRWG. NO.	QUAN.
1	PRINTED CIRCUIT MASTER	P-C 232-B	1
2	EYELET	S-179-1	10
3	EYELET	S-179-2	58
4	RESISTOR 18K, ¼W, 5%		1
5	" 1K		1
6	" 2K		1
7	" 150K		1
8	" 300K		1
9	" 10K		1
10	" 4.7K		1
11	" 2.7K		2
12	" 30K		1
13	" 27K		1
14	" 470Ω		1
15	" 2.2K, ½W		1
16	" 1.8K, 1W		1
17	" 470Ω, 1W		1
18	DIODE GTDX2		1
19	" GTDX3		1
20	POT, ALLEN/BRADLEY TYPE RP 200K		1
21	TRANSISTOR GA004		2
22	" GT1170		2
23	" SPACER	S-181	4
24	WIRE JUMPER #20 SOLID		1
25	CAPACITOR 330 μf CM15		1

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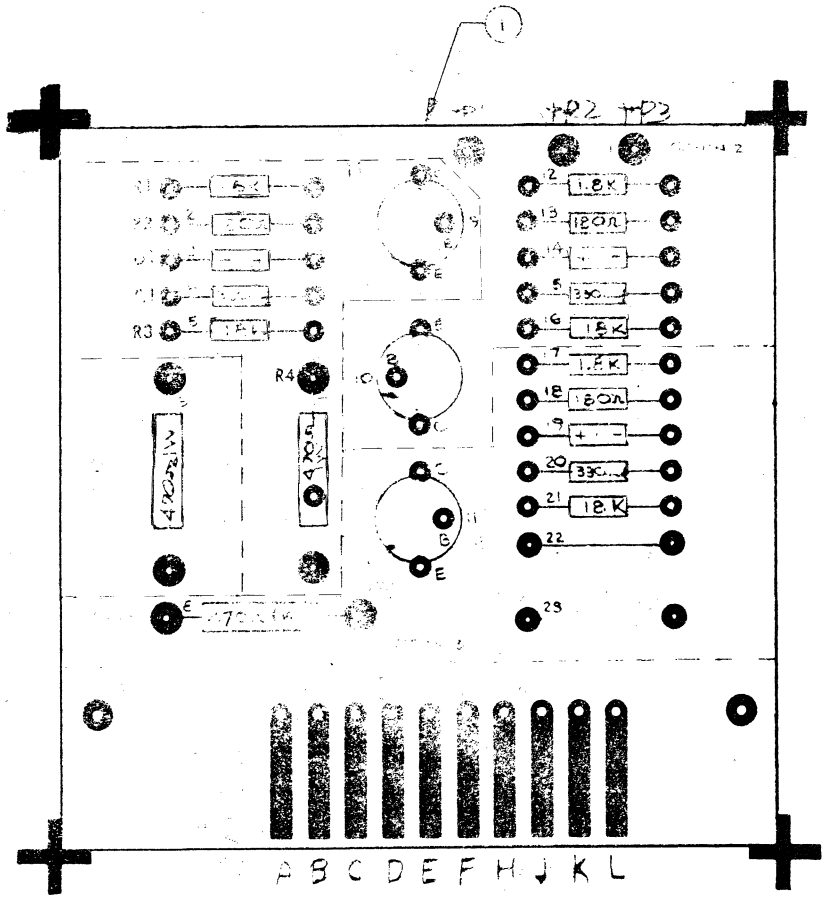
FIGURE 5-17
PSE-A ASSEMBLY DRAWING



LOCATION	QUAN	DESCRIPTION	DWG NO	ITEM
	1	P.C. MASTER	P-C186	1
1,12 & 17	3	RESISTOR 1.8K 1/4W 5%		2
5,16 & 21	3	" 18K " "		3
2,13 & 18	3	" 180Ω " "		4
6,7 & 8	3	" 470Ω 1W "		5
4,15 & 20	3	CAPACITOR 330 mmf 200V CM15		6
3,14 & 19	3	DIODE GTDX3		7
				8
9,10 & 11	3	TRANSISTOR GT1170① or PHILCO 2N598②		9
9,10,11	3	TRANSISTOR SPACER, EPSCO		10
22	1	SOLID WIRE #GA22		11
				12
				13

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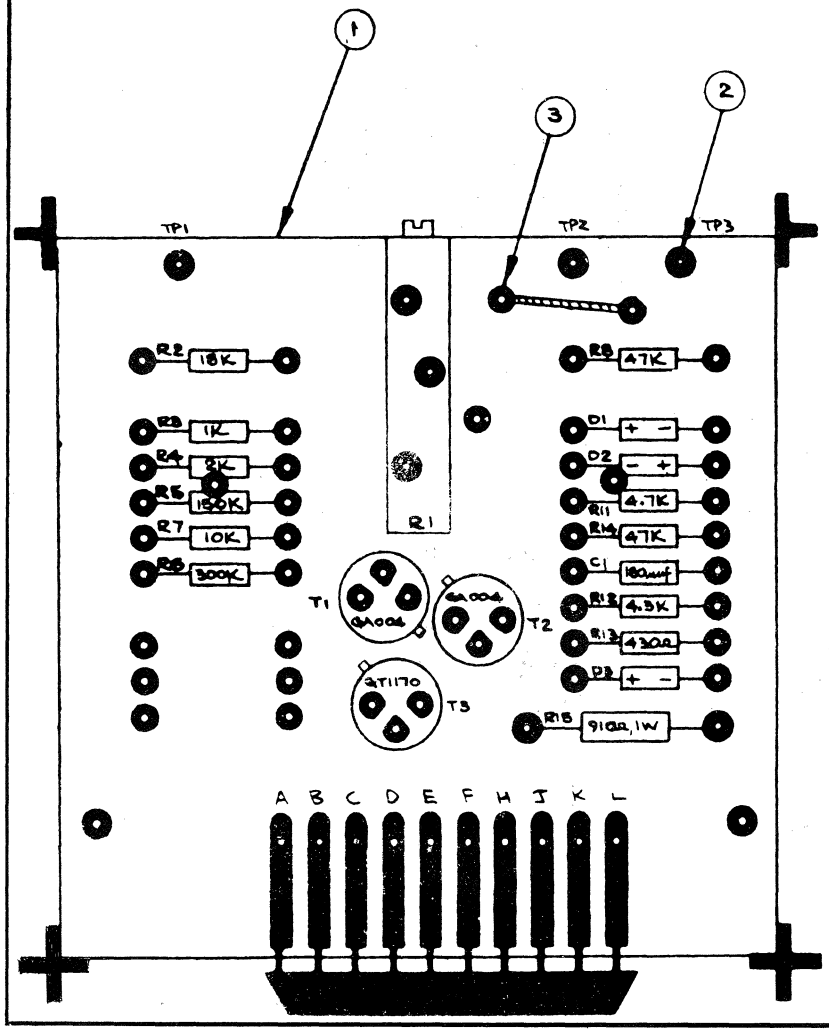
DIGITRONICS CORPORATION

FIGURE 5-18
AAA-1, AAA-3 ASSEMBLY DRAWINGS



ITEM	DESCRIPTION	DWG. NO.	QUAN
1	P.C. MASTER	P-C 233	1
2	EYELET	S-179-1	18
3	"	S-179-2	54
4	TRANSISTOR SPACER	S-181	3
5	" GA004 T1, T2		2
6	" GT1170 T3		1
7	RESISTOR 200K ADJ, ALLEN-BRADLEY TYPE RP	R1	1
8	" 910Ω, 1W, 5%	R15	1
9	" 18K, 1/4W, 5%	R2	1
10	" 1K, " "	R3	1
11	" 2K, " "	R4	1
12	" 150K, " "	R5	1
13	" 300K, " "	R6	1
14	" 10K, " "	R7	1
15	" 4.7K, " "	R11	1
16			
17			
18	" 4.3K, " "	R12	1
19	" 430Ω, " "	R13	1
20	" 47K, " "	R14, R8	2
21			
22	CAPACITOR 180 mmf CM15	C1	1
23	DIODE GTDX3	D1, D2, D3,	3
24			
26			
27	WIRE #20 SOLID .550 C/C		1

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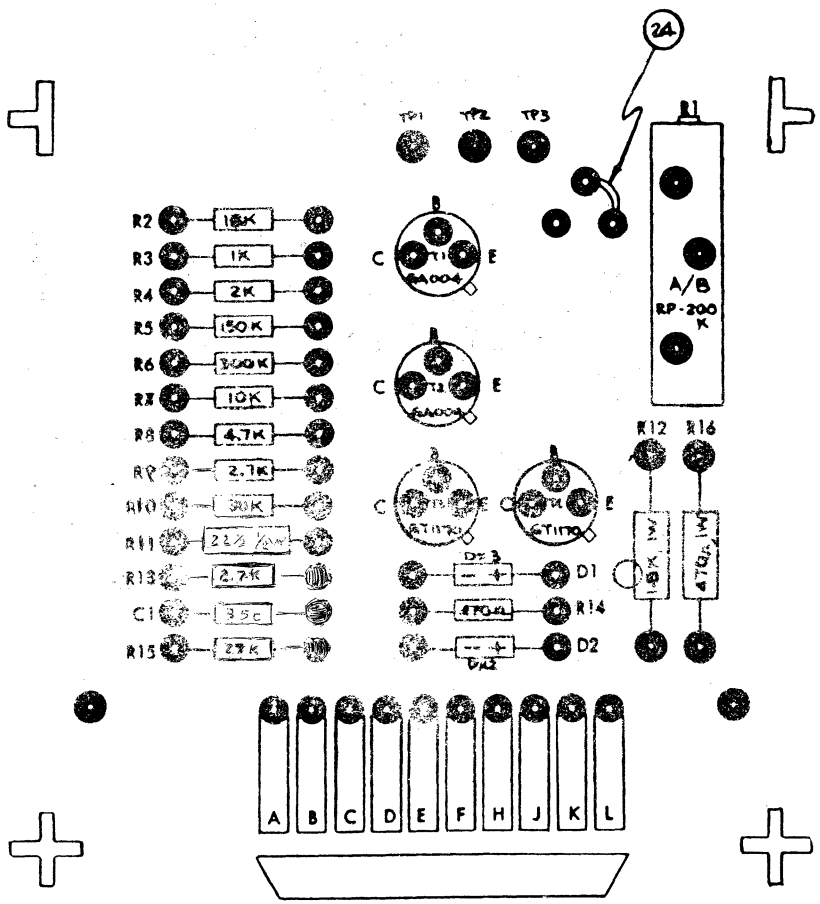
FIGURE 5-19
PGH-A ASSEMBLY DRAWING



ITEM	DESCRIPTION	DRWG. NO.	QUAN.
1	PRINTED CIRCUIT MASTER	P-C 232-B	1
2	EYELET	S-179-1	10
3	EYELET	S-179-2	58
4	RESISTOR 18K, ½W, 5%		1
5	" 1K		1
6	" 2K		1
7	" 150K		1
8	" 300K		1
9	" 10K		1
10	" 4.7K		1
11	" 2.7K		2
12	" 30K		1
13	" 27K		1
14	" 470Ω		1
15	" 2.2K, ½W		1
16	" 1.8K, 1W		1
17	" 470Ω, 1W		1
18	DIODE GTDX2		1
19	" GTDX3		1
20	POT ALLEN/BRADLEY TYPE RP 200K		1
21	TRANSISTOR GA004		2
22	" GT1170		2
23	" SPACER	S-181	4
24	WIRE JUMPER #20 SOLID		1
25	CAPACITOR 330 mmf CM15		1

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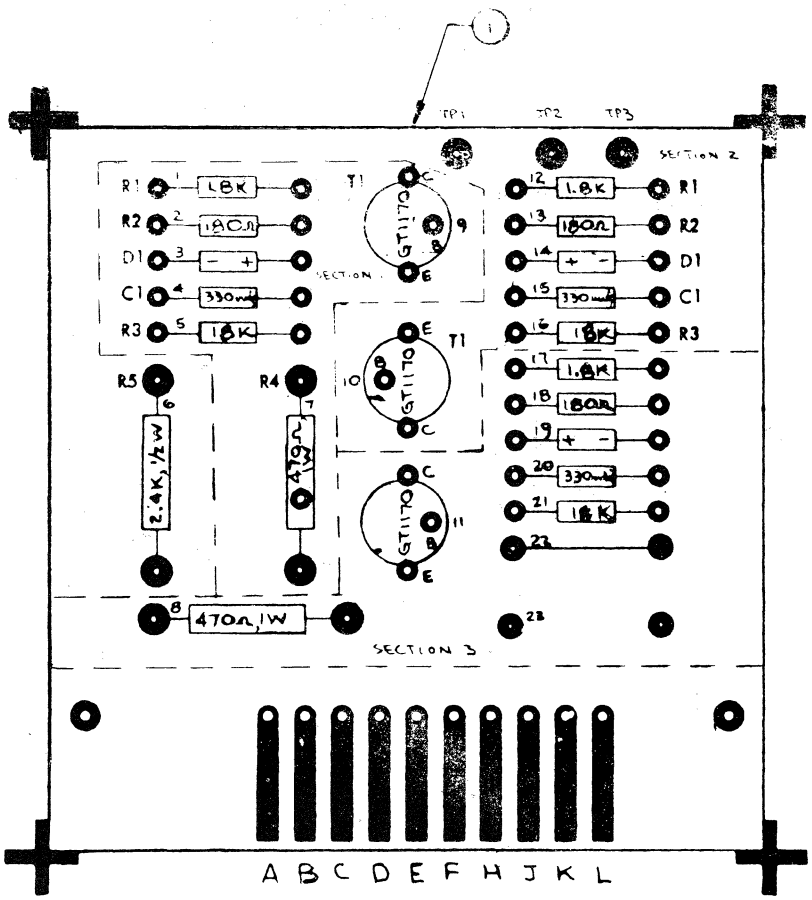
FIGURE 5-20
PSF-A ASSEMBLY DRAWING



LOCATION	QUAN	DESCRIPTION	DWG NO	ITEM
	1	P.C. MASTER	P-C186	1
1, 12, 17	3	RESISTOR 1.8K 1/4W 5%		2
5, 16, 21	3	" 18K " "		3
2, 13, 18	3	" 180Ω " "		4
7, 8	2	" 470Ω 1W "		5
4, 15, 20	3	CAPACITOR 330 mmf 200V CM15		6
3, 14, 19	3	DIODE GTDX3		7
6	1	RESISTOR 2.4K, 1/2W, 5%		8
9, 10, 11	3	TRANSISTOR GT1170		9
9, 10, 11	3	TRANSISTOR SPACER, EPSCO		10
22	1	SOLID WIRE #22 GA		11
				12
				13

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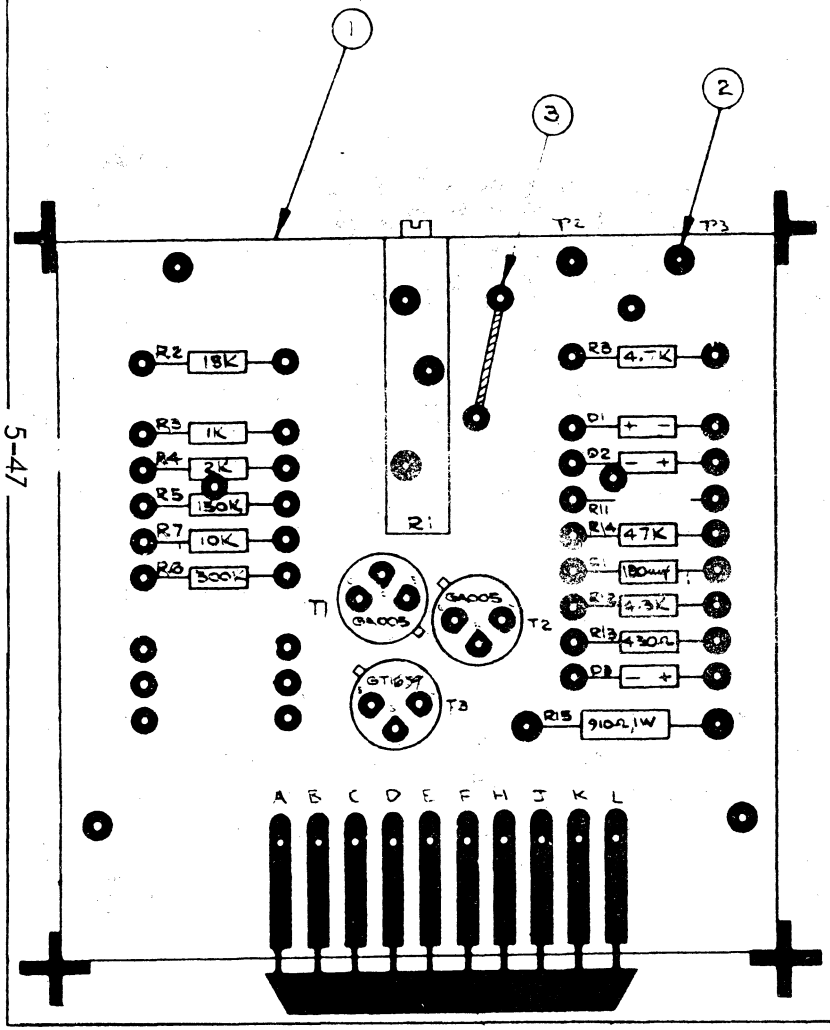
FIGURE 5-21
AAA-2 ASSEMBLY DRAWING



ITEM	DESCRIPTION	DWG. NO.	QUAN
1	P.C. MASTER	P-C 233	1
2	EYE-ET	5-179-	18
3		5-179-2	54
4	TRANSISTOR SPACER	5-18	3
5	GA005 T1, T2		2
6	GT1859 T3		1
7	RESISTOR 200K ADJ ALLEN-BRADLEY TYPE J R		1
8	" 910Ω 1W 5%	R15	1
9	" 18K 2W 5%	R2	1
10	" 1K " "	R3	1
11	" 2K " "	R4	1
12	" 150K " "	R5	1
13	" 300K " "	R8	1
14	" 10K " "	R7	1
15	" 4.7K " "	R8	1
16			1
17			1
18	" 4.3K " "	R12	1
19	" 430Ω " "	R13	1
20	" 47K " "	R14	1
21			
22	CAPACITOR 150 mmfd CM15	C1	1
23	DIODE GTDX3	D1, D2, D3,	3
24			
25			
27	WIRE #20 SOLID .550 C/L		

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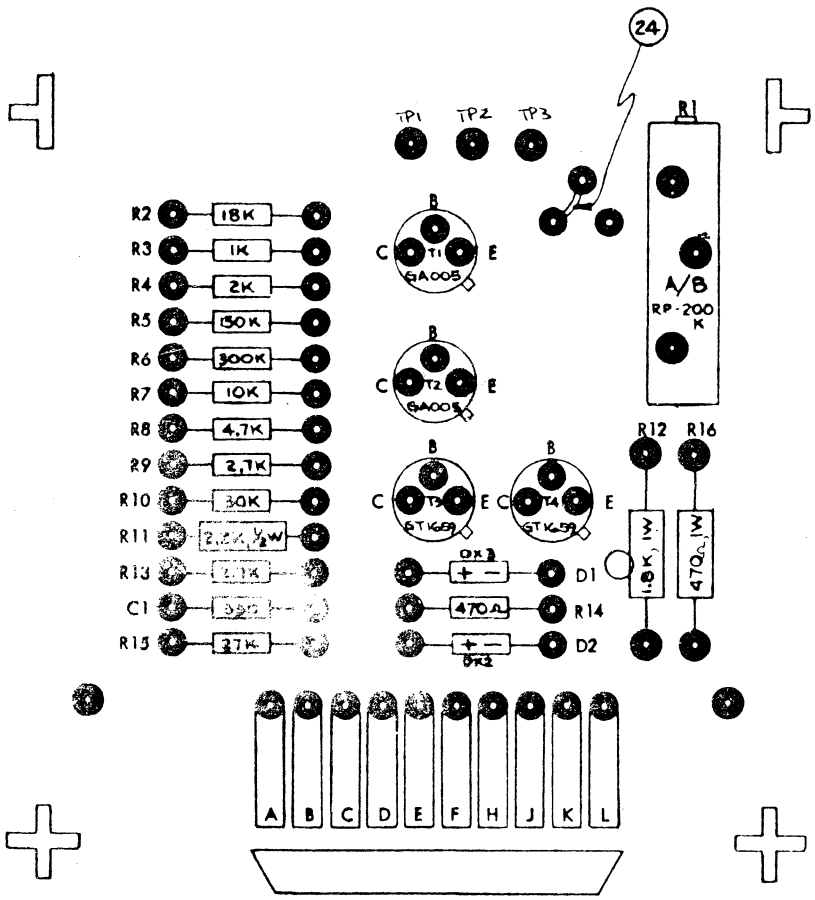
FIGURE 5-22
PGJ-A ASSEMBLY DRAWING



ITEM	DESCRIPTION	DRWG. NO.	QUAN
1	PRINTED CIRCUIT MASTER	P-C 232-B	1
2	EYELET	S-179-1	10
3	EYELET	S-179-2	58
4	RESISTOR 18K, ¼W, 5%		1
5	" 1K		1
6	" 2K		1
7	" 150K		1
8	" 300K		1
9	" 10K		1
10	" 4.7K		1
11	" 2.7K		2
12	" 30K		1
13	" 27K		1
14	" 470Ω		1
15	" 2.2K, ½W		1
16	" 1.8K, 1W		1
17	" 470Ω, 1W		1
18	DIODE GTDX2		1
19	" GTDX3		1
20	POT, ALLEN/BRADLEY TYPE RP 200K		1
21	TRANSISTOR GA005		2
22	" GT1659		2
23	" SPACER	S-181	4
24	WIRE JUMPER #20 SOLID		1
25	CAPACITOR 330 mmf CM15		1

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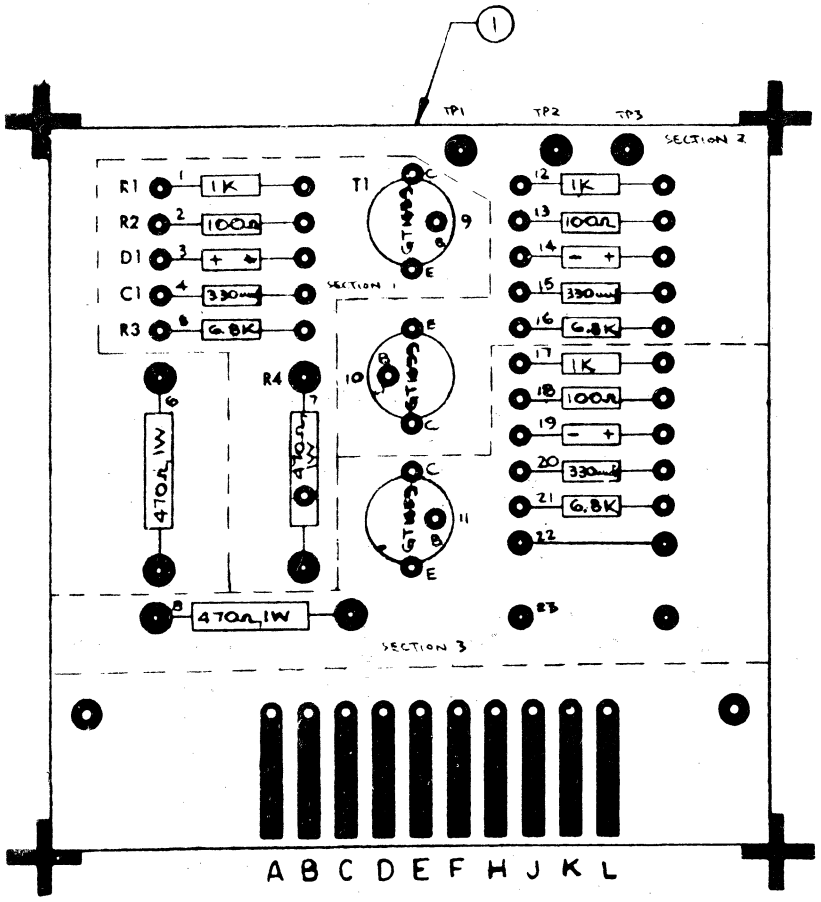
FIGURE 5-23
PSG-A ASSEMBLY DRAWING



LOCATION	QUAN	DESCRIPTION	DWG NO	ITEM
	1	P.C. MASTER	PC186	1
1, 12, 17	3	RESISTOR 1K, 1/4W, 5%		2
5, 16, 21	3	" 6.8K, " "		3
2, 13, 18	3	" 100Ω, " "		4
6, 7, 8	3	" 470Ω 1W, "		5
4, 15, 20	3	CAPACITOR 330 mmf		6
3, 14, 19	3	DIODE GTDX3		7
				8
9, 10, 11	3	TRANSISTOR GT1659		9
22	1	SOLID WIRE # 22GA		10
				11
				12
				13

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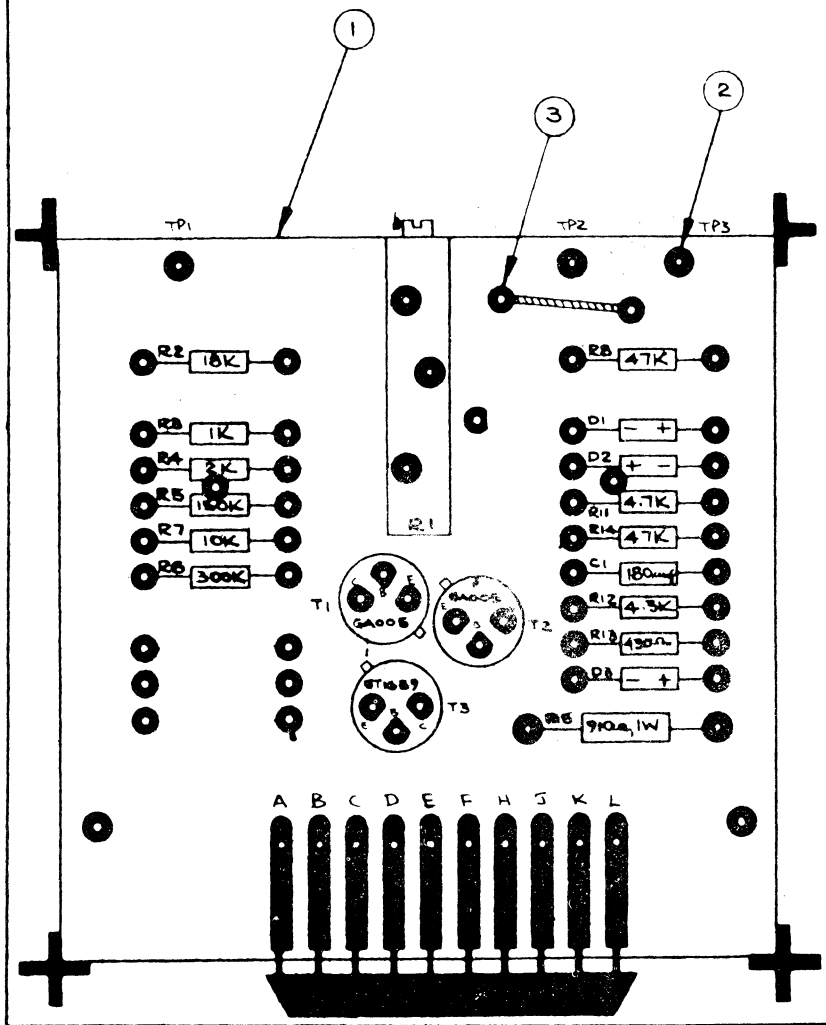
FIGURE 5-24
BBB-1 ASSEMBLY DRAWING



ITEM	DESCRIPTION	DWG. NO.	QUAN
1	P.C. MASTER	P-C 233	1
2	EYELET	S-179-1	18
3	"	S-179-2	54
4	TRANSISTOR SPACER	S-181	3
5	" GA005 T1, T2		2
6	" GTIG59 T3		1
7	RESISTOR 200K ADJ, ALLEN-BRADLEY TYPE RP	R1	1
8	" 910Ω, 1W, 5%	R15	1
9	" 18K, 1/4W, 5%	R2	1
10	" 1K, " "	R3	1
11	" 2K, " "	R4	1
12	" 150K, " "	R5	1
13	" 300K, " "	R6	1
14	" 10K, " "	R7	1
15	" 4.7K, " "	R11	1
16	" 120K, " "	R9	1
17	" 15K, " "	R10	1
18	" 4.3K, " "	R12	1
19	" 430Ω, " "	R13	1
20	" 47K, " "	R14 R8	2
21			
22	CAPACITOR 180 mmfd CM15	C1	1
23	DIODE GTDX3	D1, D2, D3, D4	4
24			
26			
27	WIRE #20 SOLID .550 C/C		1

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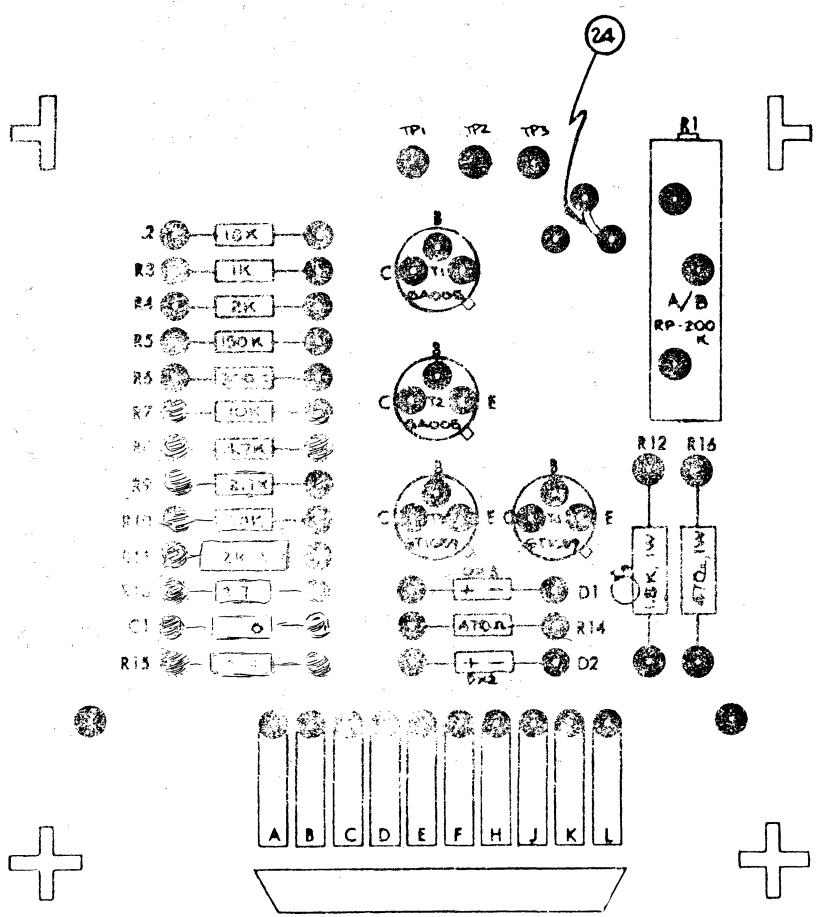
FIGURE 5-25
PGK-A ASSEMBLY DRAWING



ITEM	DESCRIPTION	DRWG. NO.	QUAN
1	PRINTED CIRCUIT MASTER	P-C 232-B	1
2	EYELET	S-179-1	10
3	EYELET	S-179-2	58
4	RESISTOR 18K, 1/4W, 5%		1
5	" 1K		1
6	" 2K		1
7	" 150K		1
8	" 300K		1
9	" 10K		1
10	" 4.7K		1
11	" 2.7K		2
12	" 30K		1
13	" 27K		1
14	" 470Ω		1
15	" 2.2K, 1/2W		1
16	" 1.8K, 1W		1
17	" 470Ω, 1W		1
18	DIODE GTDX2		1
19	" GTDX3		1
20	POT, ALLEN BRADLEY TYPE RP 200K		1
21	TRANSISTOR GA005		2
22	" GTI659		2
23	" SPACER	S-181	4
24	WIRE JUMPER #20 SOLID		1
25	CAPACITOR 330μμf CM15		1

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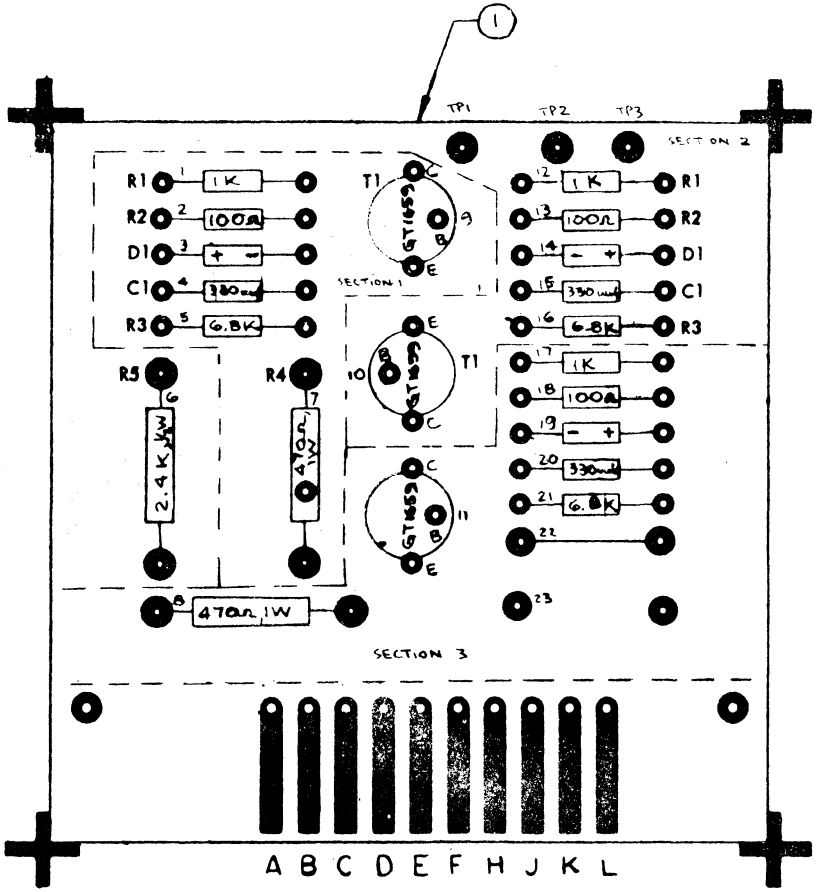
FIGURE 5-26
PSH-A ASSEMBLY DRAWING



LOCATION	QUAN	DESCRIPTION	DWG NO	ITEM
	1	P.C. MASTER	P-C186	1
1, 12, 17	3	RESISTOR 1K ¼W 5%		2
5, 16, 21	3	" 6.8K " "		3
2, 13, 18	3	" 100Ω " "		4
7, 8	2	" 470Ω 1W		5
4, 15, 20	3	CAPACITOR 330 μμf		6
3, 14, 19	3	DIODE GTDX3		7
6	1	RESISTOR 2.4K, ½W, 5%		8
9, 10, 11	3	TRANSISTOR GT1650		9
22	1	SOLID WIRE #22GA		10
				11
				12
				13

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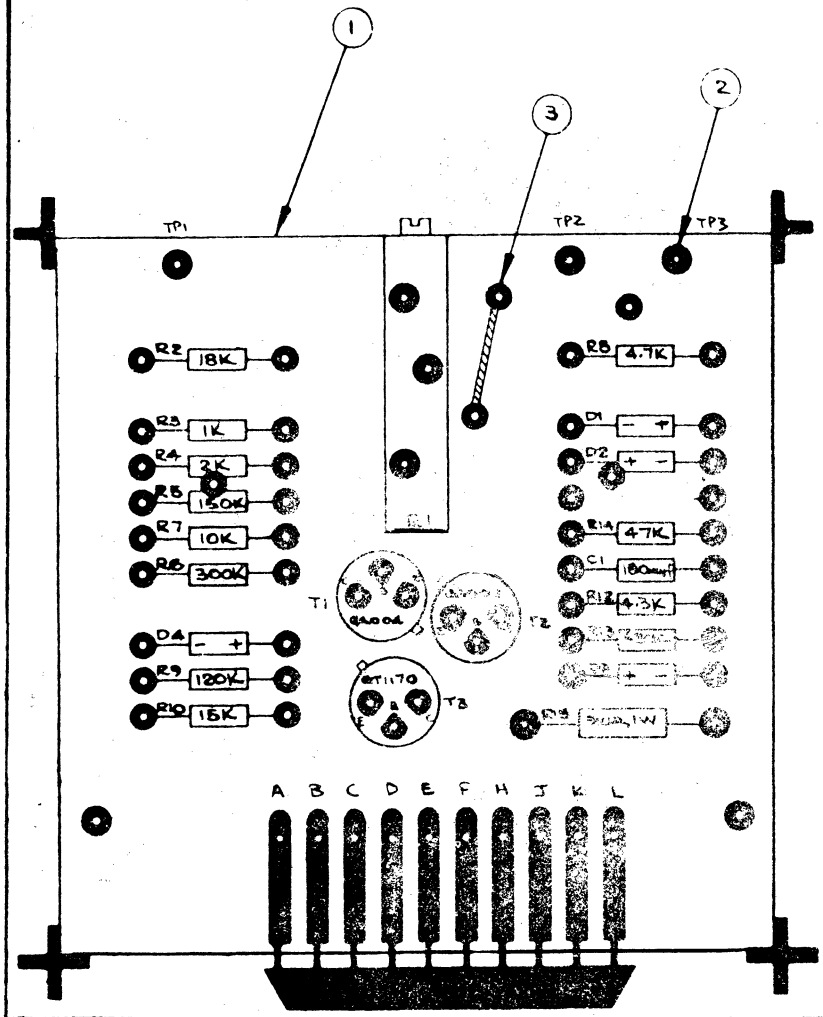
FIGURE 5-27
BBB-2 ASSEMBLY DRAWING



ITEM	DESCRIPTION	DWG. NO.	QUAN.
1	P.C. MASTER	P-C 233	1
2	EYELET	S-179-1	18
3	"	S-179-2	54
4	TRANSISTOR SPACER	S-181	3
5	" GA004 T1, 2		2
6	" GT1170 T3		1
7	RESISTOR 200Ω, 1/2W, ALLEN-BRADLEY TYPE RP	R1	1
8	910Ω, 1W, 5%	R15	1
9	18K, 1/2W, 5%	R2	1
10	1K	R3	1
11	2K	R4	1
12	150K	R5	1
13	300K	R6	1
14	10K	R7	1
15	4.7K	R8	1
16	120K	R9	1
17	15K	R10	1
18	4.3K	R12	1
19	430Ω	R13	1
20	4.7K	R14	1
21			
22	CAPACITOR 180mμf CM15	C1	1
23	DIODE 1N295	D1, D2, D3, D4	4
24			
25			
27	WIRE #20 SOLID .550 CIC		1

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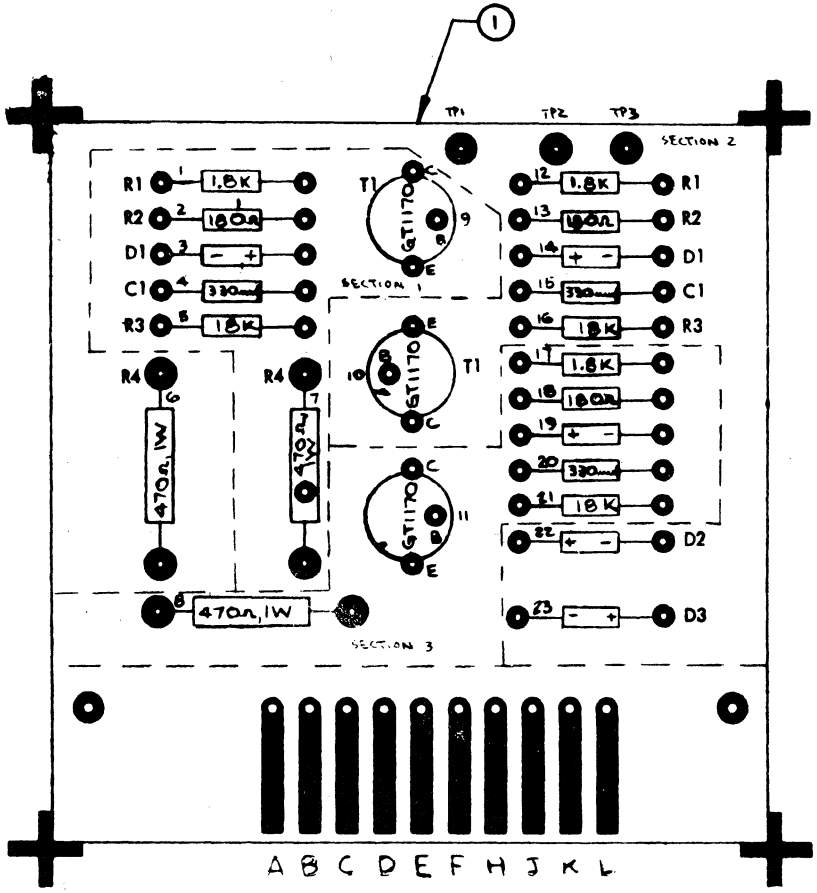
FIGURE 5-28
PGE-A ASSEMBLY DRAWING



LOCATION	QUAN	DESCRIPTION	DWG NO	ITEM
	1	P.C. MASTER	P-C186	1
1, 12, 17	3	RESISTOR 1.8K, 1/4W, 5%		2
5, 16, 21	3	" 18K, " "		3
2, 13, 18	3	" 180Ω, " "		4
6, 7, 8	3	" 470Ω, 1W, "		5
4, 15, 20	3	CAPACITOR 330 mμf 200V CM15		6
3, 14, 19	5	DIODE GTDX3		7
				8
9, 10, 11	3	TRANSISTOR GT1170		9
9, 10, 11	3	TRANSISTOR SPACER, EPS60		10
				11
				12
				13

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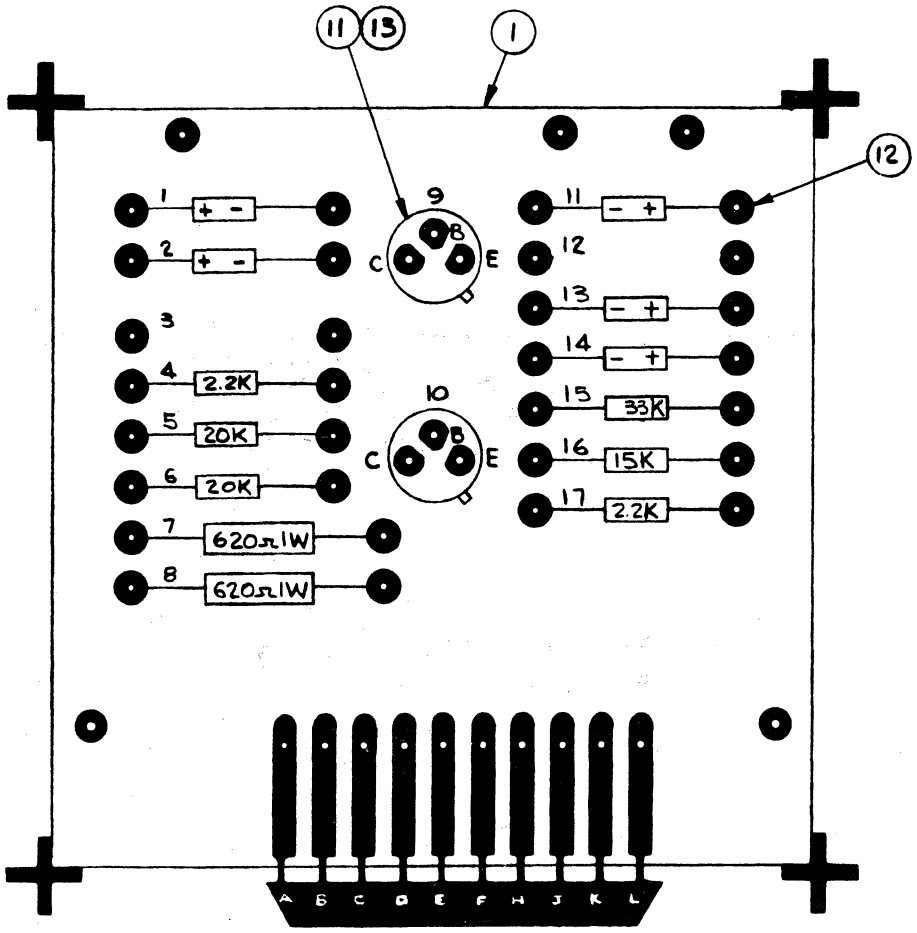
DIGITRONICS CORPORATION

FIGURE 5-29
AAA-SCM ASSEMBLY DRAWING



LOCATION	QUAN	DESCRIPTION	DWG. NO	ITEM
	1	P.C. MASTER	P-C152A	1
5, 6	2	RESISTOR 20K 1/4W 5%		2
4 & 17	2	RESISTOR 2.2K 1/4 W 5%		3
15	1	RESISTOR 33K 1/4W 5%		4
7 & 8	2	RESISTOR 620Ω 1W 5%		5
16	1	RESISTOR 15K 1/4W 5%		6
1, 2, 11, 13 & 14	5	DIODE GTDX3		7
				8
9 & 10	2	TRANSISTOR GT1170		9
				10
SEE NOTES 1 & 3	16	EYELET	S179-2	11
SEE NOTES 2 & 3	33	EYELET	S179-1	12
	2	TRANSISTOR SPACER	S-181	13

REF.-SCHEMATIC DWG. A-H483

NOTE:

1. DRILL #55 (.052), (SMALL LAND) FOR ITEM 11.
2. DRILL .067 (LARGE LANDS) FOR ITEM 12.
3. INSERT ITEMS 11 & 12 FROM OPPOSITE SIDE.

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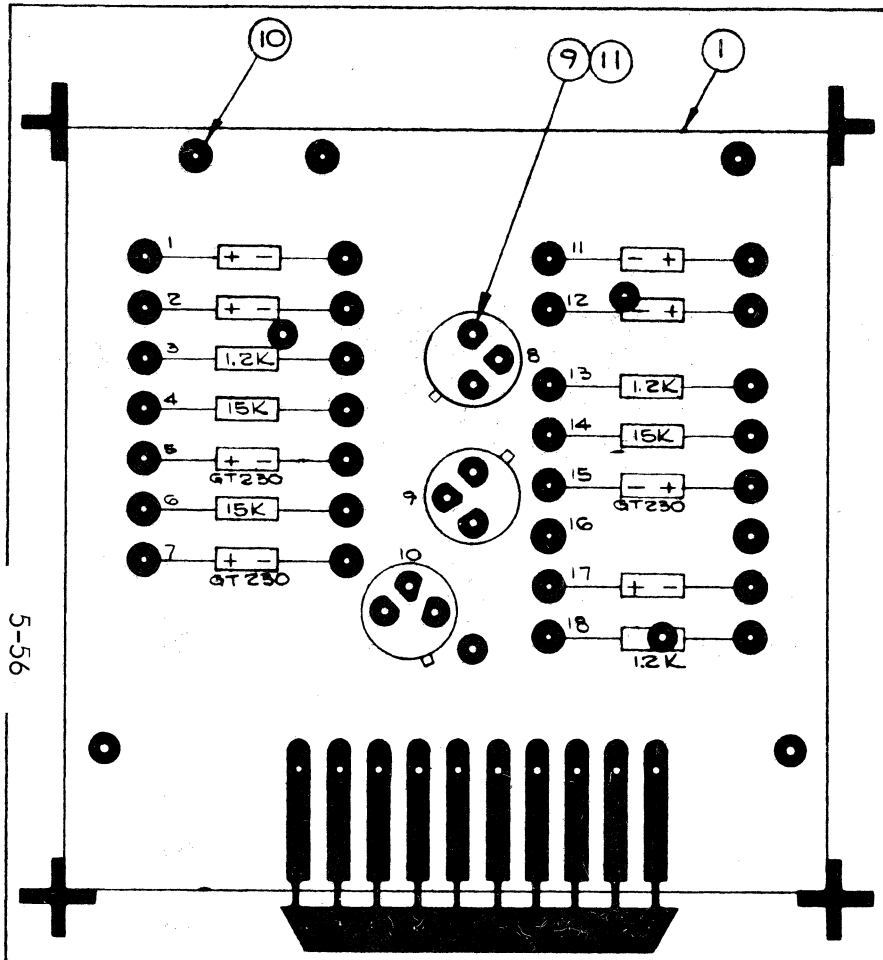
TITLE:

FIGURE 5-30
FRA-D ASSEMBLY DRAWING

USED ON: DAGE

DRAWING NO. B-C1093



LOCATION	QUAN.	DESCRIPTION	DWG. NO.	ITEM
	1	P.C. MASTER "SDA"	P-C153A	1
3,13 ¢18	3	RESISTOR 1.2K 1/4W 5%		2
4,6,14	3	" 15K " "		3
				4
1,2,11,12,16 ¢17	5	DIODE GTDX3		5
5,7 ¢15	3	" GT230		6
				7
8,9, ¢10	3	TRANSISTOR 2N598		8
SEE NOTE 2 ¢3	15	EYELET	S-179-2	9
SEE NOTE 1 ¢2	43	"	S-179-1	10
	3	TRANSISTOR SPACER	S-181	11
				12

REF- SCHEMATIC DWG. A-H 535

NOTE:
1. DRILL .067 FOR ITEM 10.
2. INSERT ITEM 9 ¢10 FROM OPPOSITE SIDE.
3. DRILL .052 FOR ITEM 9.

DIGITRONICS
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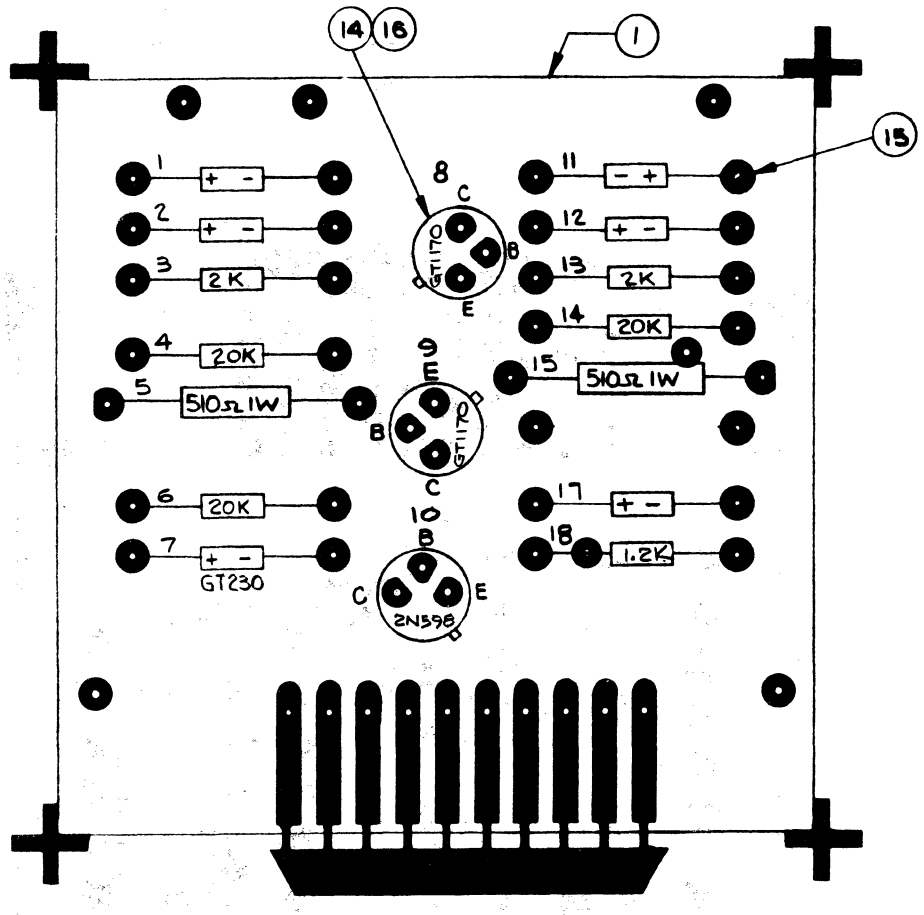
TITLE:
FIGURE 5-31
SDA-H ASSEMBLY DRAWING

USED ON: 10016

DRAWING NO. B-C1313



LOCATION	QTY	DESCRIPTION	DWG. NO	ITEM
	1	P.C. MASTER	P-C151A	1
3&13	2	RESISTOR 2K 1/4W 5%		2
				3
4,6&14	3	" 20K " "		4
18	1	" 1.2K " "		5
5&15	2	510Ω 1W "		6
				7
1,2,11,12&17	5	DIODE GTDX3		8
7	1	" GT230		9
				10
8&9	2	TRANSISTOR GT1170		11
10	1	" 2N598		12
				13
SEE NOTE 1&3	43	EYELET	S179-2	14
" " 2&3	10	"	S179-1	15
	3	TRANSISTOR SPACER	S181	16

REF.-SCHEMATIC DWG. NO. A-H534

NOTE:

1. DRILL #55 (.052) (SMALL LANDS) FOR ITEM 14.
2. " .067 (LARGE LANDS) " " 15.
3. INSERT ITEM 14&15 FROM OPPOSITE SIDE.

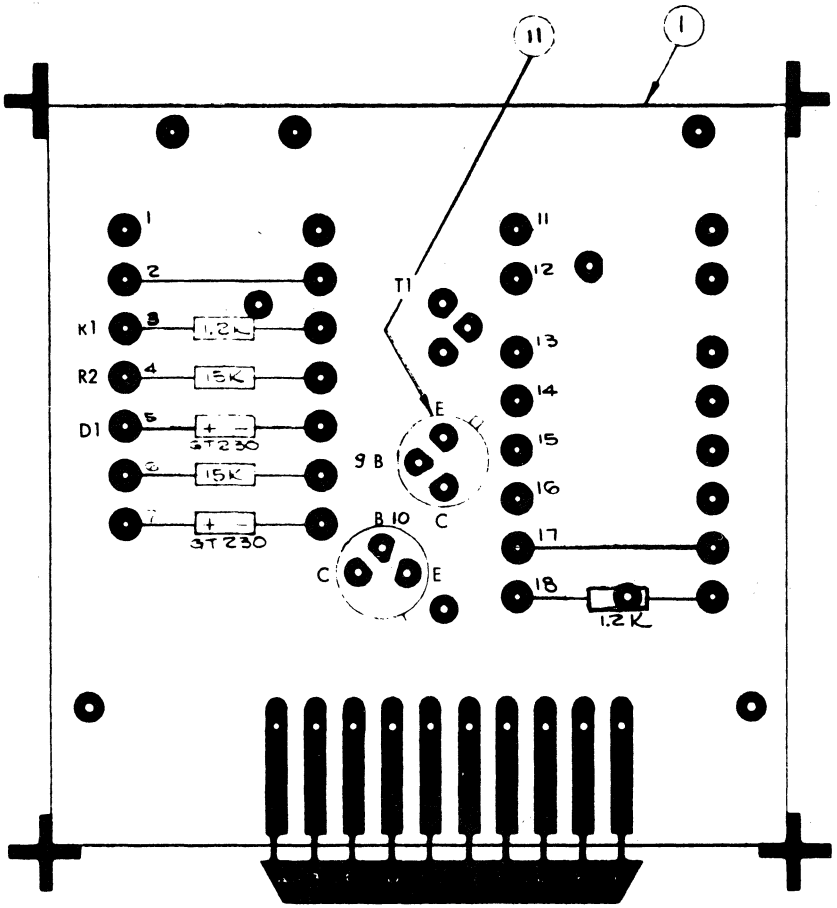
DIGITRONICS
ALBERTSON, NEW YORK

TITLE:

FIGURE 5-32
FRB-H ASSEMBLY DRAWING

USED ON: 6257

DRAWING NO. B-C1312



LOCATION	QUAN	DESCRIPTION	DWG NO	ITEM
	1	P.C MASTER "SDA	P-C153A	1
3 & 18	2	RESISTOR 1.2K 1/4W 5%		2
4, 6,	2	" 15K " "		3
				4
5, 7	2	DIODE GT230		5
				6
				7
9, & 10	2	TRANSISTOR 2N317		8
				9
				10
	2	TRANSISTOR SPACER	S-181	11
2, 17	2	WIRE JUMPER # 20 SOLID 5/10 %		12

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FIGURE 5-33
SDC ASSEMBLY DRAWING

REPLACEABLE ELECTRICAL PARTS

(Refer To Table 5-2 For Parts Options)

POWER SUPPLY

Reference Designation	Nomenclature	Digitronics Part Number*
C1	Capacitor, 1000 uf, 25 volts	TC-AH108F (TMS-11)
C2	Same as C1	
C3	Same as C1	
C4	Same as C1	
C5	Capacitor, 1000 uf, 50 volts	TC-AP108F (TMS-16)
C6	Same as C5	
C7	Same as C5	
C8	Capacitor, 100 uf, 150 volts	TC-AD107F (TMS-22)
C9	Capacitor, 50 uf, 150 volts (used on -1, -3)	TC-AD506F (TMS-20)
C9	Capacitor, 150 uf, 150 volts (used on -2, -4, -5)	TC-AK157F (TMS-25)
C10	Same as C8	
C11	Same as C9 (used on -3)	
CR1	Rectifier, Silicon	GE4JA411BC1BD1
CR2	Rectifier, Silicon	GE4JA411AC1AD1
CR3	Rectifier, Silicon	GE4JA411AC1BD1
CR4	Zener Diode	Motorola 50M10Z5

Reference Designation	Nomenclature	Digitronics Part Number*
F1	Fuse, 2A, FNA	TF-AJ0200
F2	Same as F1	
F3	Same as F1	
F4	Same as F1	
F5	Not Used	
J1	Receptable Connector	A-1134
J3	Receptable Connector	Jones S-315-DB
J6	Receptable Connector	SF-JAX54B
P1	Plug	A-1133
P2	Plug	Cannon DA 15 S
P3	Plug	See figure 4-4 (BC-2322) for proper connector number
P5	Plug	Sealectro SKT-1
R1	Resistor Adjustable, 15 ohms, 30 watts	TR-QK150C (Ohmite - F307)
R2	Resistor Adjustable, 20 ohms, 30 watts	TR-QK200C (Ohmite)
R3	Same as R2	
R4	Resistor Adjustable, 5 ohms, 30 watts	TR-QJ50UC (Ohmite)
R5	Resistor Adjustable, 25 ohms, 50 watts	TR-AL250D (Ohmite 0562)

Reference Designation	Nomenclature	Digitronics Part Number*
R6	Same as R5	
R7	Resistor Adjustable, 5 ohms, 10 watts	TR-AF50UD (Ohmite 1004)
R8	Resistor 270 ohms, 1 watt	TR-CC271C
R9	Resistor 10,000 ohms, 1/2 watt	TR-CB103C
R10	Resistor 50 ohms, 40 watts	TR-SK500C (Ward Leonard)
R11	Same as R10	
R12	Same as R10	
R13	Same as R10	
R14	Same as R10	
R15	Same as R10	
R16	Resistor 3 ohm, 30 watt	TR-SJ30UC
T1	Transformer	B-T53
TB1	Terminal Board	TTBAA0307 (Kulka)

*Vendors sources and part numbers are given when available.

TABLE 5-2 POWER SUPPLY PARTS OPTION

Reference Designation	POWER SUPPLY DRAWING D-H718				
	-1.	-2.	-3.	-4	-5.
C8	X	X	X	X	X
C9	X	X	X	X	X
C10			X	X	X
C11			X	X	X
R10	X	X	X	X	X
R11	X	X	X	X	X
R12		X	X	X	X
R13			X	X	X
R14				X	
R15				X	

DC 2296-1

ITEM	QUAN PER UNIT	PART NUMBER	REV	DESCRIPTION
1	1	CC81-5	F	ROLLER SOL.MT.ASS'Y
2	1	AC 78	D	CAPSTAN ASS'Y
3				
4	1	AA 1095	A	PLATE PHOTOETCHED
5				
6	1	AB 32	C	BELT IDLER ARM
7	1	AA235-1	B	BELT IDLER TEN.ROL.
8	1	TH-XE1708 92-76		SHLDR.SCREW MOTON
9	1	AA 188	A	BELT TENSION SPRING
10	2	BC 726	D	TP.GUIDE ASS'Y
11				
12	2	TTREA215 5131-62W		RET.RING,END,KOH.
13				
14				
15				
16				
17	4	TH-WA0409		FLATWASHER #4
18	1	TTBAA0308		BARR.STP.KULKA600A-B
19	1	TMSAA008		MARKER STRIP,KULKA 600-LEB
20	5	TMTPA0001		CABLE CLF.PAND.LSC-2
21	8	TH-SI0805		4-40x5/8LG.BHM ST.
22	3	TH-SI1204		6-32x5/16LG.BHM ST.
23	4	TH-SI1404		8-32x5/16LG.BHM ST.
24	3	TH-SI1715		10-32x1 7/8LG.BHM
25	4	TH-SL1711		10-32x1"LG.SOK.HD.CAP.
26	3	TH-SG1207		6-32x1/2LG.FL.HD.MACH.
27	1	TH-SI1710		10-32x7/8LG.BHM
28	2	TH-XC1405		8-32x3/8AL.HD. CPS
29	8	TH-WB0403		LKWSHR.#4 SPLIT
30	3	TH-WB0605		LKWSHR.#6 SPLIT
31	4	TH-WB0708		LKWSHR.#8 SPLIT
32	7	TH-WB0809		LKWSHR.#10 SPLIT
33	1	TH-WA0814		FL.WSHR.#10PL.LOT.
34	2	TH-SL1707		10-32x1/2LG.SK.HD.CAP.
35	1	TH-LA1006		SOLDER LUG#6 INT.TTH.
36	1	TH-SL2009		1/4-20x5/4SK.HD.CAP.
37	1	TH-WB1016		LKWSHR 1/4 SPLIT
38	1	TH-XC1402		8-32x5/16AL.HD.CPS
39	1	TH-SI1203		6-32X1/4 LG BHM
40				
41	1	SEE M.S.		BRAKE ASSEMBLY
42	1	SEE M.S.		MOTOR/SP. SS'Y
43	1	SEE M.S.		COVER
44	1	" " "		CHASSIS ASS'Y
45	1	" " "		CARD COMPLIMENT
46	1	" " "		HEAD ASSEMBLY
47	2	" " "		ROLLER ASSEMBLY
48	1	" " "		PANEL
49	2	" " "		PLUG BUTTON
50				

REF: SOLENOID WIRING AS PER AK1000

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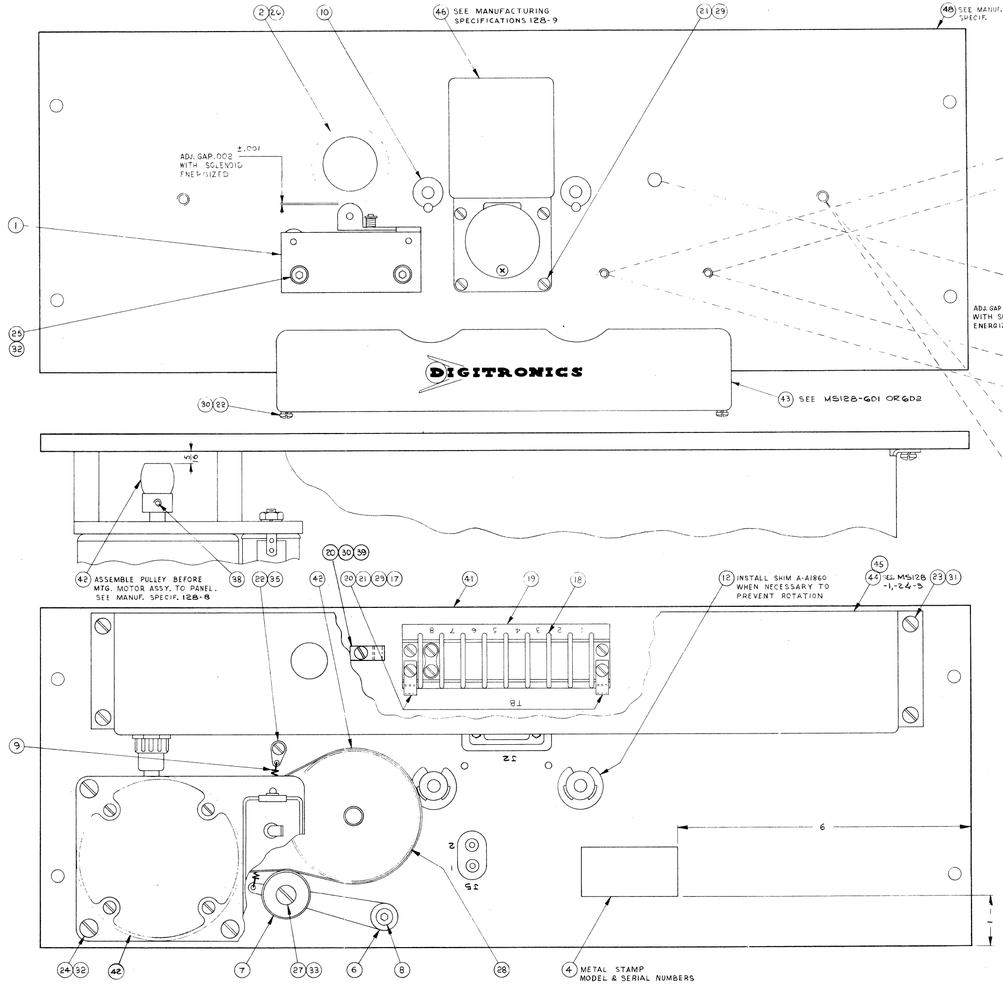
TITLE:
FIGURE 5-34
3500 ASSEMBLY DRAWING
SHEET 2 OF 2

FIRST USED ON: | SHEET 2 OF 2 | DRAWING NO. D-C2296

QUAN.	DESCRIPTION	REF. STD.	DRWG. NO.	ITEM



DIGITRONICS
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TITLE:
FIGURE 5-34
3500 ASSEMBLY DRAWING
SHEET 1 OF 2

FIRST USED ON: | SHEET 1 OF 2 | DRAWING NO. D-C2296

QUAN.	DESCRIPTION	REF. STD.	DRWG. NO.	ITEM

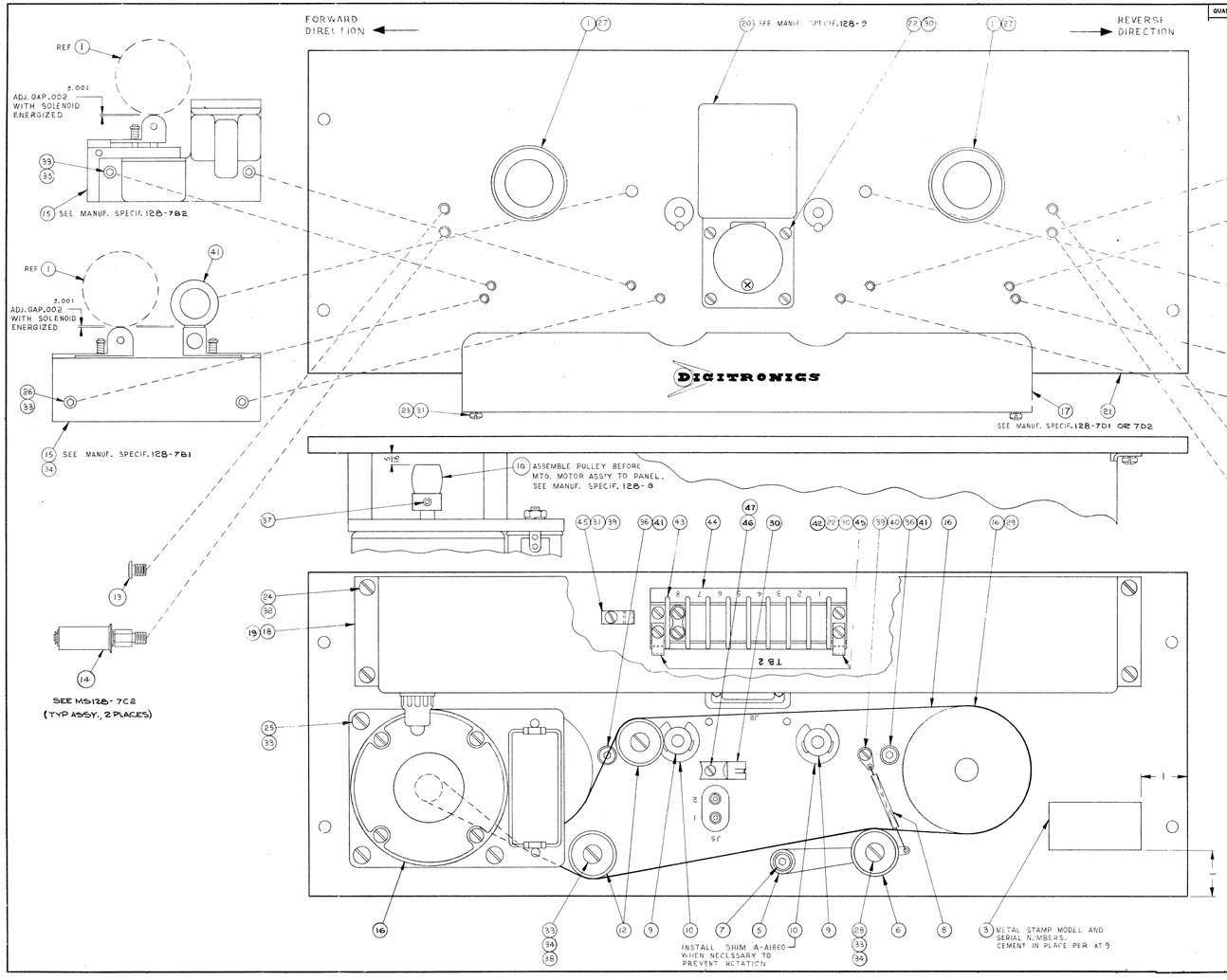
DC2297-1

ITEM	QUAN PER UNIT	PART NUMBER	REV	DESCRIPTION
1	2	AC 78	D	CAPSTAN ASSEMBLY
2				
3	1	AA 1095	A	PLATE PHOTOETCHED
4				
5	1	AB 32	C	BELT IDLER ARM
6	1	AA235-1	B	BELT IDLER TEN.ROLL.
7	1	TMXE1705		SHLDR. SCREW MORTON
8	1	AA 188	A	BELT TEN. SPRING .
9	2	BC 726	D	TP. GUIDE ASS'Y
10	2	TTPEA1215		RET.RING BOWD.KOH.
11				
12	2	AA 235-2	B	ROLLER BELT IDLER
13	2	AA 3179	-	PLUG BUTTON
14	2	AB 188	C	ROLLER ASSEMBLY
15	1	SEE M.S.		FINCH ROLLER BRAKE ASS'Y
16	1	" " "		MOTOR/SP. ASS'Y
17	1	" " "		COVER
18	1	" " "		CHASSIS ASS'Y
19	1	" " "		CARD COMPLIMENT
20	1	" " "		HEAD ASSEMBLY
21	1	" " "		PANEL
22	8	TH-SI0805		4-40x5/8LG.BHM
23	2	TH-SI1204		6-32x5/16LG.BHM
24	4	TH-SI1404		8-32x5/16LG.BHM
25	3	TH-SI1716		10-32x1 7/8LG.BHM
26	4	TH-SL1711		10-32x1"sk.HD.CAP.
27	6	TH-SE1207		6-32x1/2LG.FHM
28	1	TH-SI1710		10-32x7/8 LG.BHM
29	4	TH-XC1405		8-32x5/8AL.HD.CPS
30	9	TH-WB0403		LKWSHR.#4 SPLIT
31	3	TH-WB0605		LKWSHR.#6 SPLIT
32	4	TH-WB0708		LKWSHR.#8 SPLIT
33	10	TH-WB0815		LKWSHR.#10 SPLIT
34	7	TH-WA0814		FLTWSHR.#10 PL.LHT.
35	4	TH-SL1707		10-32x1/2LG.SK.HD.CAP.
36	2	TH-SL2005		1/4-20x5/8LG.SK.HD.CAP.
37	1	TH-XC1402		8-32x5/16AL.HD.CPS
38	2	TH-SI1712		10-32x1 1/8LG.BHM
39	2	TH-SI1203		6-32x1/4LG.BHM
40	1	TH-LA2007		SOLD.LUG#6INT.TTH.
41	2	TH-WB1016		LKWSHR.1/4 SPLIT
42	4	TH-WA0409		FL. WASHER#4
43	1	TTBAA0508		BARRIER STRIP,KULKA
44	1	TMSAA0108		MARKER STRIP,KULKA
45	3	TMRFB0001		CABLE CLAMP,PAND.
46	1	TMAA0402		CABLE CLIP,TINNRMN.
47	1	TH-SI0803		4-40x1/4LG.BHM
48				

REF: SOLENOID WIRING AS PER AK1001

TITLE: FIGURE 5-35 83500 ASSEMBLY DRAWING SHEET 2 OF 2

FIRST USED ON: | SHEET 2 OF 2 | DRAWING NO. D-C2297



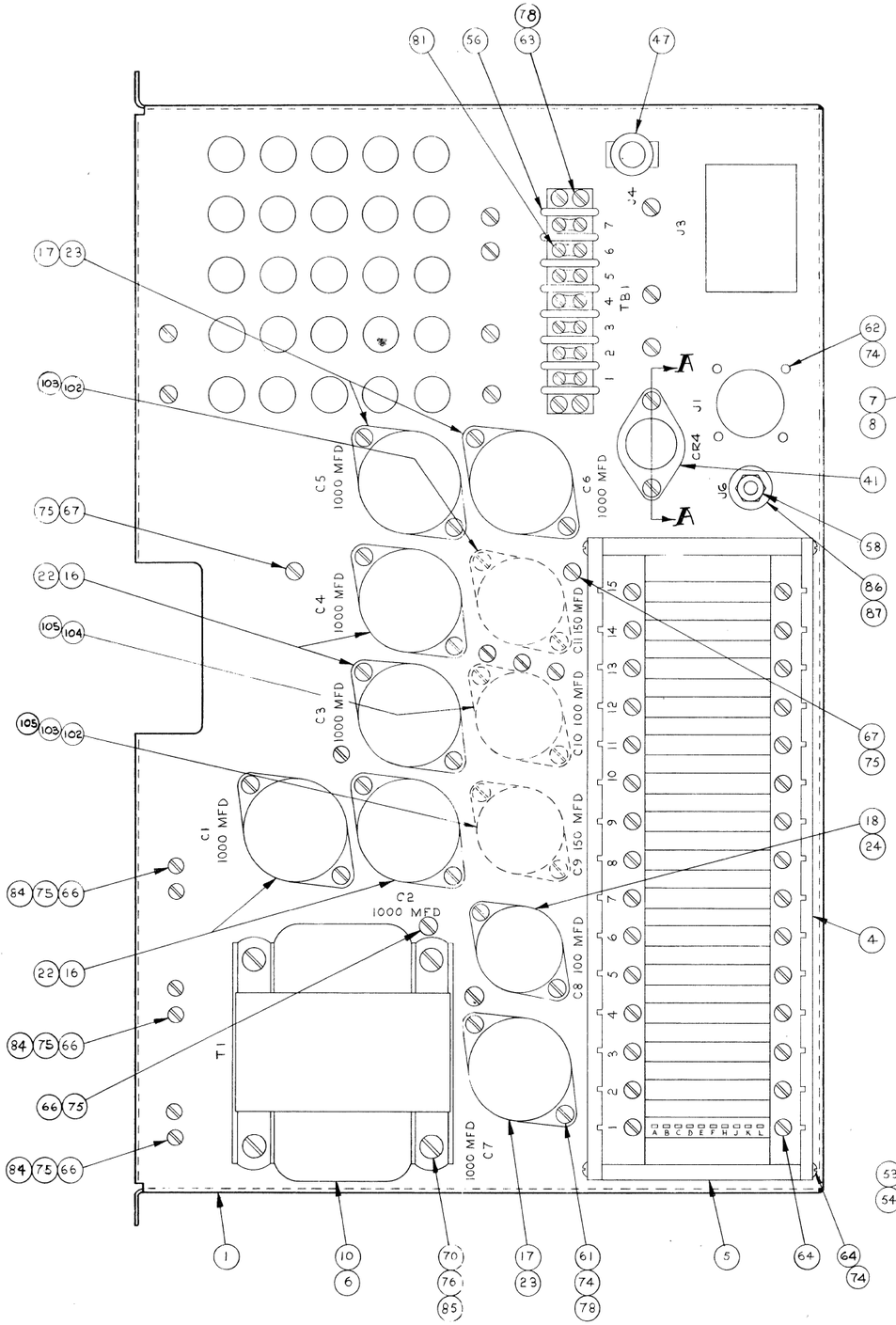
QUAN.	DESCRIPTION	REF. STD.	DRWG. NO.	ITEM

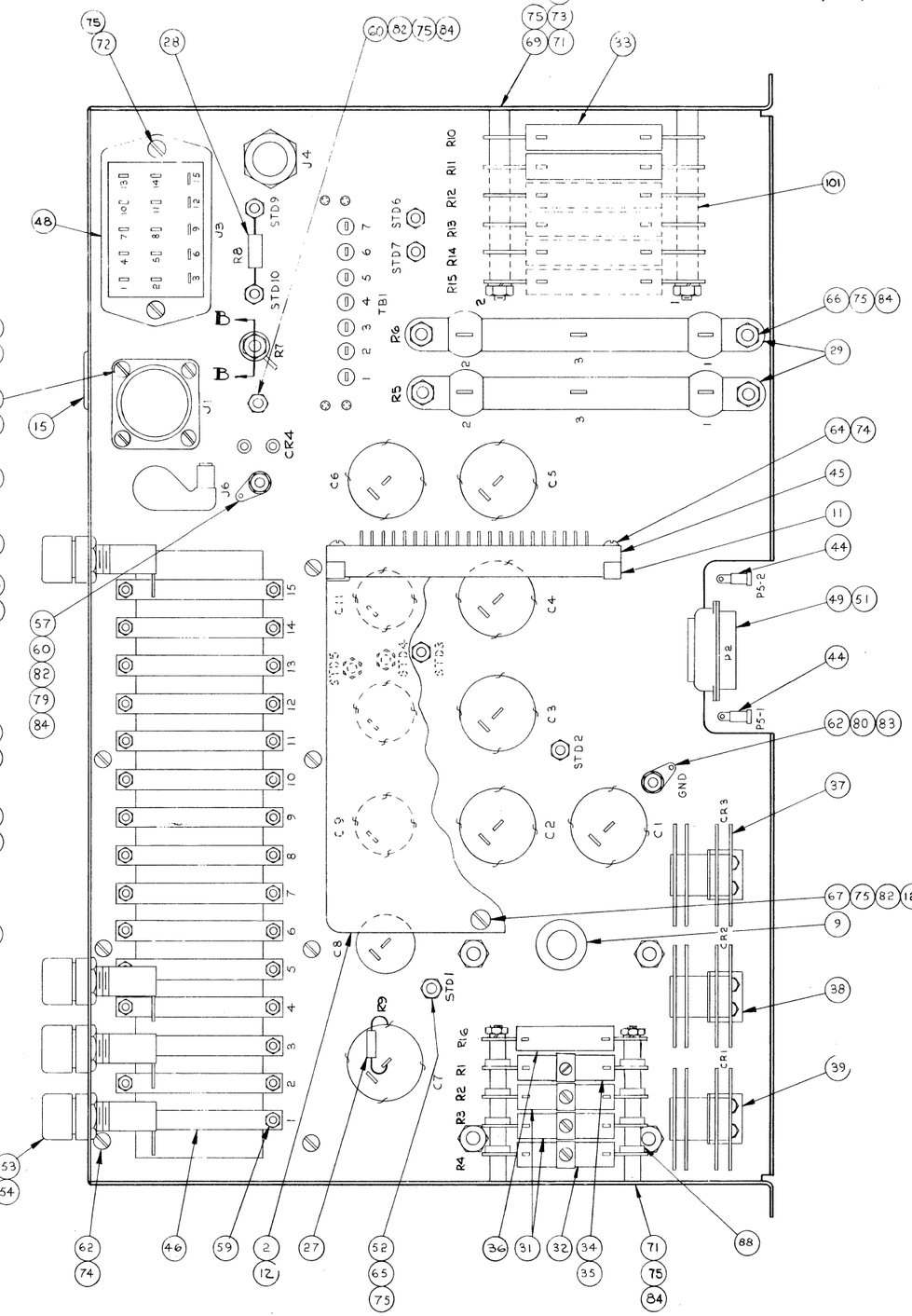
DIGITRONICS, ALBERTSON, NEW YORK

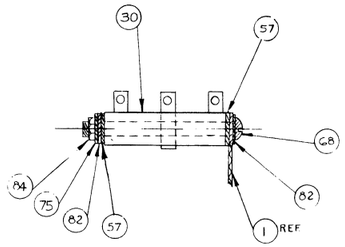
TITLE: FIGURE 5-35 83500 ASSEMBLY DRAWING SHEET 1 OF 2

FIRST USED ON: | SHEET 1 OF 2 | DRAWING NO. D-C2297

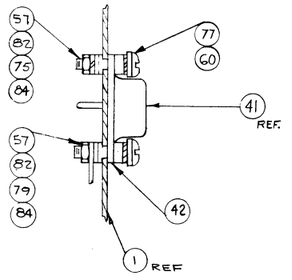
QUAN.	DESCRIPTION	REF. STD.	DRWG. NO.	ITEM







SECTION "B-B"



SECTION A-A

NOTES
1. COAT BOTH SIDES OF ITEM (42), WITH DC-33 (SILCON GREASE)
2. BEND CONNECTION LUGS ON CR1, CR2 & CR3, TO PREVENT CHASSIS FROM RESTING ON SAME

DIGITRONICS
ALBERTSON, NEW YORK

TITLE:
FIGURE 5-36
CHASSIS ASSEMBLY DRAWING
SHEET 1 OF 2

FIRST USED ON:	SHEET 1 OF 2	DRAWING NO.
10015		D-C2051

DC 2051-5

ITEM	QUAN PER UNIT	PART NUMBER	REV.	DESCRIPTION
100	1	DC2051-1	-	CHASSIS ASS'Y STOCK
101	4	TR-SK500C		RES.50ohm40W
102	2	TC-AC157F		CAP.150ufd150V FY.
103	2			INSUL.SLEEVE A283
104	1	TC-AD107F		CAP.100MFD150V FY.
105	1	A266		INSUL. SLEEVE

REF. W.A.P. BK304-4

DC 2051-6

ITEM	QUAN PER UNIT	PART NUMBER	REV.	DESCRIPTION
100	1	DC2051-1	-	CHASSIS ASS'Y STOCK
101	2	TR-SK500C		RES. 50ohm 40W
102	2	TC-AC157F		CAP.150uf,150V FY.
103	2	A283		INSUL. SLEEVE
104	1	TC-AD107F		CAP.100ufd,150V FY.
105	1	A266		INSUL. SLEEVE

REF. W.A.P. BK304-5

DC 2051-2

ITEM	QUAN PER UNIT	PART NUMBER	REV	DESCRIPTION
100	1	DC2051-1	-	CHASSIS ASS'Y STOCK
101				
102	1	TC-AD506F		CAP.50ufd150V FY.
103	1	A266		INSUL.SLEEVE FY.

REF. W.A.P. BK304-1

DC 2051-3

ITEM	QUAN PER UNIT	PART NUMBER	REV.	DESCRIPTION
100	1	DC2051-1	-	CHASSIS ASS'Y STOCK
101	1	TR-SK500C		RES.50ohm40W
102	1	TC-AC157F		CAP.150ufd150V FY.
103	1	A283		INSUL. SLEEVE FY.

REF. W.A.P. BK304-2

DC 2051-4

ITEM	QUAN PER UNIT	PART NUMBER	REV.	DESCRIPTION
100	1	DC2051-1		CHASSIS ASS'Y STOCK
101	2	TR-SK500C		RES.50ohm40W
102	2	TC-AD506F		CAP.50ufd150V FY.
103	2			INSUL. SLEEVE FY.
104	1	TC-AD107F		CAP.100MFD150V FY.
105	3	A266		INSUL. SLEEVE FY.

REF. W.A.P. BK304-3

DC 2051-1

ITEM	QUAN PER UNIT	PART NUMBER	REV.	DESCRIPTION
57	4	TH-YD0609		FIBRE WASHER,GEN.CEM.
58	1	TDF0Z8501		JACK,PHONO,SWITCHCRFT.
59	30	TH-ZA0704		NUT,HX.4-40MINI.ESNA
60	2	TH-SI1207		SCR.6-32x1/2LG BHM
61	12	TH-SI0803		SCREW,4-40x1/4LGBHM
62	23	TH-SI0804		SCREW,4-40x5/16LGBHM
63	4	TH-SI0805		SCR,4-40x3/8LG.BHM
64	36	TH-SI0807		SCR.4-40x1/2LG.BHM
65	8	TH-SI1202		SCR.6-32x3/16LG.BHM
66	7	TH-SI1204		SCR.6-32x5/16LG.BHM
67	10	TH-SI1206		SCR.6-32x7/16LG.BHM
68	1	TH-SI1218		SCR.6-32x2 1/4LG.BHM
69	2	TH-SG1221		SCR.6-32x2 7/8LG.F.H.M.
70	4	TH-SI1408		SCR.8-32x5/8LG.BHM
71	2	TH-SG1221		6-32x3 LG.FL.HD.M.
72	2	TH-SI1201		SCR.6-32x1/8 LG BHM
73	2	TH-SI1211		6-32x1 LG.BHM
74	64	TH-WB0403		LKWSHR.4 SPLIT TYP.
75	33	TH-WB0605		LKWSHR. 6SPLIT TYP.
76	4	TH-WB0708		LKWSHR.8 SPLIT TYP.
77	2	TH-WB0609		LKWSHR.6 EXT. TTH.
78	20	TH-WA0409		WASHER4 PLAIN
79	1	TH-LA2007		LUG,SOLDER 6INT.TTH.
80	1	TH-LA2003		LUG,SOLDER4 INT.TTH.
81	7	TH-IC1007		LUG,SOLDER KULKA
82	4	TH-WA0612		WASHER 6 PL.
83	7	TH-NA0704		NUT, HEX 4-40
84	18	TH-NA1106		NUT, HEX 6-32
85	4	TH-NA1307		NUT, HEX 8-32
86	1	TH-YA1226		SWEDGED FIBRE WASH. SWITCHCRAFT #51029
87	1	TH-YB1226		BAKELITE WASHER SWITCHCRAFT #51028
88	8	A-A1005-9		SPACER
		(REF)		WAP DK400-GA
				" DK400-65
				" DK400-66

ITEM	QUAN PER UNIT	PART NUMBER	REV.	DESCRIPTION
1	1	DE 336	-	CHASSIS MARKING
2				
3				
4	2	BA 1346	-	TRACK,PRT. CARD
5	2	BA 1347	A	SPACER, TRACK
6	2	AA 2792	-	SPACER, BAR
7	1	A-1133	-	CONNECTOR
8	1	A-1134	-	CONN. SOCKET
9	1	A196-3	A	GROMMET
10	1	BT 53	C	TRANSFORMER
11	2	AA 1344	-	POST,CONN.MOUNT.
12	1	AA1345		SPACER
13				
14				
15	1			PLUG BUT.CARR FASNRS.
16	4	TC-AH108F		CAP.1000ufd25VFY.TMS-11
17	3	TC-AP108F		CAP.1000ufd50VFY.TMS-16
18	1	TC-AD107F		CAP.100ufd150VFY.TMS-22
19				
20				
21				
22	4	TTWEPC003		SL.INSULAT.A269
23	3	TTWEPA001		SL.INSULAT.A258
24	1	TTWEPB002		SL.INSULAT.A266
25				
26				
27	1	TR-CB103C		RES.10K 1/2W5%FX.COMP.
28	1	TR-CC271C		RES.270ohm1W5%FX.COMP.
29	2	TR-AL250D		RES.ADJ.25ohm50W
30	1	TR-AF50UD		RES.ADJ.50hm10W
31	2	TR-QK200C		RES.ADJ.20ohm30W
32	1	TR-QJ50UC		RES.ADJ.5ohm30W
33	2	TR-SK500C		RES. .50ohm40W
34	1	TR-QK150C		RES.ADJ.15ohm30W
35	1			ADJST.BD.WD,LEONARD
36	1	TR-SJ30UC		RES. 3 OHM 30W
37	1	TCRPSF001		R.S.GE4JA411AC1BD1
38	1	TCRPSF002		R.S.GE4JA411AC1AD1
39	1	TCRPSF003		R.S.GE4JA411BC1BD1
40				
41	1	TCRZ28080		DIODE ,ZENER, MOTOROLA
42	1	TQSCA0001		INSUL.MON.MILLS
43				
44	2	TJFS00166		SEAL.CONN.SKT-1
45	1	TJFS02202		CONN.AMP.143-022-01
46	15	TJFS01054		CONN.AMP.143-010-01
47	1	TJFS00786		WINC. M7S-LRN
48	1	TJFS01596		JONES,S-315-DB
49	1	TJFS01598		CANNON,DA15S
50	1	TPWJS01523		JONES P-315-FHT
51	1	TPHSSUA06		HOOD,CONN.CANNON
52	8	TSFAA0602		STD.OFF,GARDE3449-14E
53	3	TXCBS0106		FUSE CART.,LITT.342004
54	4	TF-AJ0200		FUSE, 2 AMP FNA
55				
56	1	TTBAA0307		BARRIER STRIP,KULKA

QUAN.	DESCRIPTION	REF. STD.	DRWG. NO.	ITEM

DIGITRONICS
ALBERTSON, NEW YORK

TITLE:
FIGURE 5-36
CHASSIS ASSEMBLY DRAWING
SHEET 2 OF 2

FIRST USED ON:

SHEET 2 OF 2

DRAWING NO. D-C2051

APPENDIX A

CLAIM FOR DAMAGE IN SHIPMENT

The instrument should be tested as soon as it is received. If it fails to operate properly, or is damaged in any way, a claim should be filed with the carrier. A full report of the damage should be obtained by the claim agent, and this report should be forwarded to us. We will then advise you of the disposition to be made of the equipment and arrange for repair or replacement. Include model number, type number and serial number when referring to this instrument for any reason.

WARRANTY

Digitronics Corporation warrants each instrument manufactured by them to be free from defects in material and workmanship. Our liability under this warranty is limited to servicing or adjusting any instrument returned to the factory for that purpose and to replace any defective parts thereof (except tubes and fuses). This warranty is effective for one year after delivery to the original purchaser when the instrument is returned, transportation charges prepaid by the original purchaser, and which upon our examination is disclosed to our satisfaction to be defective. If the fault has been caused by misuse or abnormal conditions of operation, repairs will be billed at cost. In this case, an estimate will be submitted before the work is started.

If any fault develops, the following steps should be taken:

1. Notify us, giving full details of the difficulty, and include the model number, type number and serial number. On receipt of this information, we will give you service instructions or shipping data.

2. On receipt of shipping instructions, forward the instrument prepaid, and repairs will be made at the factory. If requested, an estimate will be made before work begins provided the instrument is not covered by the warranty.

SHIPPING

All shipments of Digitronics Corporation instruments should be made via Railway Express. The instruments should be packed in a wooden box and surrounded by two or three inches of excelsior or similar shock-absorbing material.

APPENDIX B

TRANSISTOR and DIODE LIST

Specified in this manual are certain transistors and diodes indicated with an asterisk (*) which are manufactured to our specifications and therefore not available commercially. Listed below are Digitronics part numbers for re-ordering information.

Transistor	Part Number
2N357A	TQ-SB357A
2N317	TQ-SA317A
2N1545	TQ-PA1545
GA004 *	TQ-SAA004
GA005 *	TQ-SB0005
GT1170*	TQ-SA1170
GT1659*	TQ-SB1659
2N598	TQ-SA0598

Diodes	
1N91	1N2069A (replaces 1N91)
DX2 *	TCRSU0125
DX3 *	TCRSU0125
GTD230 *	TCRSU0125
1N2069A	TCRP2069A

The following pages list the electrical and physical characteristics (and equivalents wherever possible) for these units to facilitate replacement or possible substitution.

I. DIODE	CLASS	MATERIAL	CATAGORY
125	SWITCHING	GERMANIUM	GOLD BONDED JUNCTION (UNIVERSAL TYPE)

II. PARAMETERS (at 25 degrees C unless otherwise noted)

POWER DISSIPATION 80 mw @ ϕ^{-1} = 1mw/°C

PIV 35 V (min) @ 100 ua

I reverse 10 V (min) @ 10 ua
50ua @ 55°C

V forward 0.45 @ 10 ma

I peak _____ @ _____

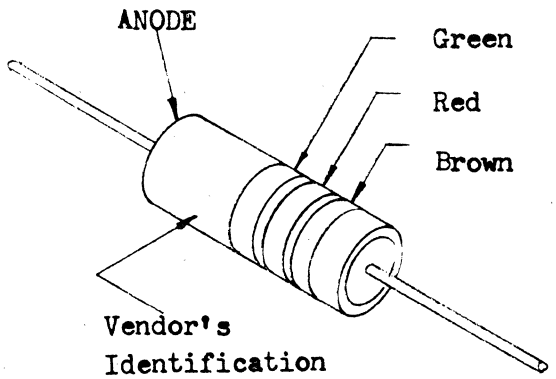
I average 70 ma @ 0.7 V (max)

I surge 300 ma @ $V_f \leq$ 1.5 V per 10 ms @ 5CPS (5% duty cycle)

NOTE: 1. Recovery as per ED-10
with tr $\leq$ 0.3 usec

2. Environmental as per ED-67.

3. Replaces DX2 (S-151)
, DX3 (S-152)
GTD230 (S-153)



DIGITRONICS
ALBERTSON, NEW YORK

TITLE: DIODE, 125

REV	E.C.O.	CHKD.	APP'D.	MO. DAY YR.
A				9/13/62

USED ON:

DRAWING NO TCR SU0125

I. TRANSISTOR	CLASS	MATERIAL	POLARITY
1170	SWITCH	Ge	PNP

II. PARAMETERS (at 25 degrees C unless otherwise noted)

POWER DISSIPATION 150 M. W. DERATING FACTOR 2.5 MW/°C

IC (max) 40 M.A.

BVCBO(min) 18 @ Ic = 100 ua *VCE (max) 0.5 V @ Ic = 40 MA Ib = 2ma

BVCES (min) ___ @ ___ *VCE (max) ___ @ ___

BVCEO (min) 12 @ Ic = 600 ua *VBE (max) 0.5 V @ Ic = 40ma Ib = 2ma

BVEBO(min) 10 @ Ie = 50 ua *VBE (max) ___ @ ___

ICBO (max) 8ua @ VCB = 10V

hFE (min) 25 @ Ic = 40 MA VC = 0.5V

hFE (min) ___ @ ___

* SATURATION

NOTE: 1. Time response as per

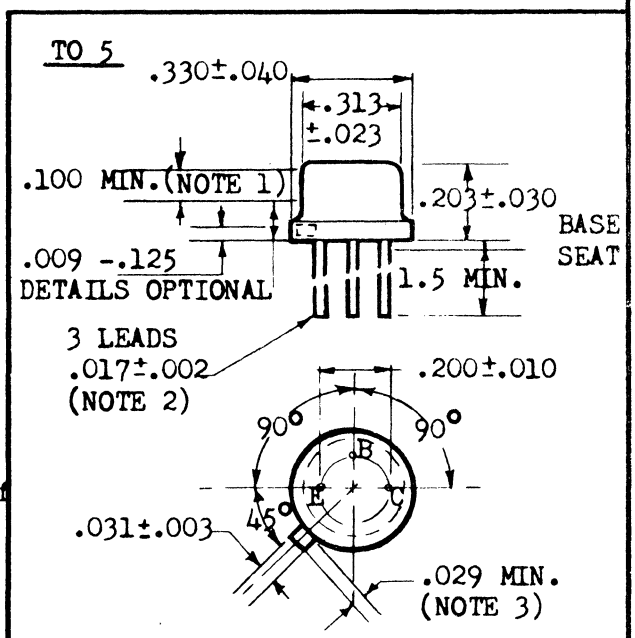
ED - 68 with

Tf = 0.7 us MAX To = 0.4 us MAX

2. Environmental as per

ED - 67

3. Replaceable by TQ-SA0222



NOTES FOR TO 5:

1. Controlled for automatic handling. Dia. not to exceed .010.
2. Lead dia. variation between .050 and .250 from base seat as specif Between .250 and 1.5 a max. of .021 dia. is held.
3. Measure from max. dia. of the actual device.

DIGITRONICS
ALBERTSON, NEW YORK

TITLE: TRANSISTOR

REV	E.C.O.	CHKD.	APP'D.	MO DAY YR.
A				7/13/62

USED ON:	DRAWING NO.
DIGITRONICS PART NUMBERS	TQ-SA1170

I. TRANSISTOR	CLASS	MATERIAL	POLARITY
TQS -GA004	SWITCH	Ge	PNP

II. PARAMETERS (at 25 degrees C unless otherwise noted)

POWER DISSIPATION 150 mw DERATING FACTOR 2 MW/° C

IC (max) 50 ma

BVCB (min) 25 V @ Ic = 25 ua *VCE (max) 0.5 V @ Ic = 5 MA, Ib = 1MA

BVCES (min) 20 V @ Ic = 25 ua *VCE (max) _____ @ _____

BVCEO (min) _____ @ _____ *VBE (max) 0,5V @ Ic = 5MA, Ib = 1MA

BVEB (min) 15 V @ Ie = 25 ua *VBE (max) _____ @ _____

ICBO (max) 3 ua @ Vcb = 10V

hFE (min) 80 @ Ic = 5 ma VCE = 0.5 V

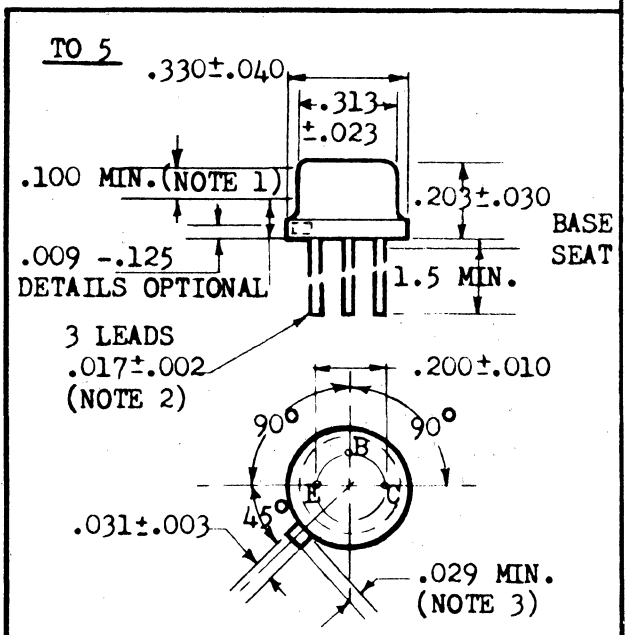
hFE (min) _____ @ _____

* SATURATION

NOTE: Time response as per ED-68 with

Tf = 1us MAX, To = 0.5us MAX

environmental as per ED-67.



NOTES FOR TO 5:

1. Controlled for automatic handling. Dia. not to exceed .010.
2. Lead dia. variation between .050 and .250 from base seat as specif. Between .250 and 1.5 a max. of .021 dia. is held.
3. Measure from max. dia. of the actual device.

DIGITRONICS
ALBERTSON NEW YORK

TITLE

TRANSISTOR

REV	E.C.O.	CHKD.	APP'D.	MO. DAY YR.	USED ON	DRAWING NO.
A				9/25/62	DIGITRONICS PART NUMBERS	TQ-SAA004

I. TRANSISTOR	CLASS	MATERIAL	POLARITY
2N 1545	POWER	Ge	PNP

II. PARAMETERS (at 25 degrees C unless otherwise noted)

POWER DISSIPATION 80 WATTS DERATING FACTOR 1.25 W/°C

IC (max) 5 AMP.

$B_{VCB}O$ (min) 60 V @ Ic = 20 MA MAX *VCE (max) 0.3 V @ Ic = 3AMPS Ib = 300MA

BVCES (min) 45 V @ Ic = .5A *VCE (max) _____ @ _____

BVCEO (min) 30 V @ Ic = .5A MAX, Ib = 0 *VBE (max) 0.5 V @ Ic = 3AMPS Ib = 300MA

BVEBO (min) 12 V @ Ie = 0.5 MA MAX *VBE (max) _____ @ _____

ICBO (max) 20 MA @ tb = +90°C, Vcb = 22 V

hFE (min) 75 @ Ic = 3.0 AMPS Vc = 2V

hFE (min) _____ @ _____

* SATURATION Switching time: Test Spec. See Note Below

NOTE: _____

Environmental as per ED-67

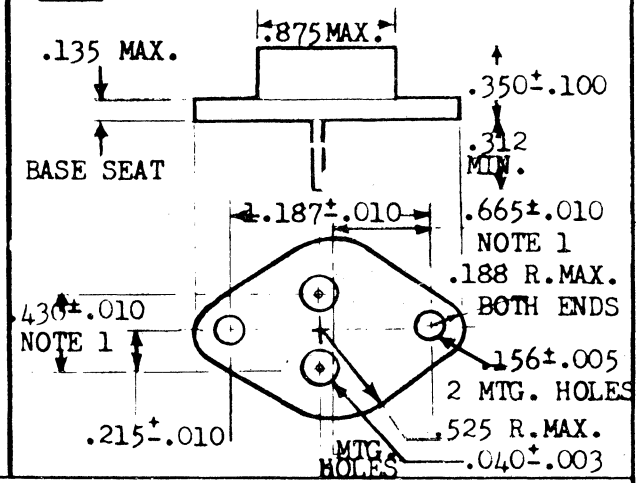
NOTE FOR TO 3:

1. These dimensions should be measured at points .050 to .005 below seating plane. When gage is not used, measurement will be made at base seat.

SWITCHING TIME:
TEST SPEC:
SEE (1) Motorola power Transistor Handbook, 1960 Edition, Page 181

(2) Clevite Transistor Bulletin TB 231-2 March 1, 1962

TO 3



DIGITRONICS
ALBERTSON NEW YORK

TITLE

TRANSISTOR

REV	E.C.O.	CHKD	APP'D	MO DAY YR
A		HH		7/26/62

ISSUED ON: DIGITRONICS PART NUMBERS

DRAWING NO. TQ-PA1545

I. TRANSISTOR	CLASS	MATERIAL	POLARITY
2N317A	SWITCH	Ge	PNP

II. PARAMETERS (at 25 degrees C unless otherwise noted)

POWER DISSIPATION 150 MW DERATING FACTOR 2 MW/°C

IC (max) 400 MA

BVCBO(min) 20 V @ Ic = 25 ua MAX *VCE (max) .2 V @ Ic = 400 MA, Ib = 20MA

BVCES (min) ____ @ _____ *VCE (max) ____ @ _____

BVCEO (min) 10 V @ Ic = 600 ua MAX *VBE (max) .95 V @ Ic = 400 MA, Ib=20MA

BVEBO(min) 20 V @ Ie = 25 ua MAX *VBE (max) .45 V @ Ib = 1 MA

ICBO (max) 2 ua @ VCB = 5 V

hFE (min) 20 @ Ic = 400 MA VCE = .25 V

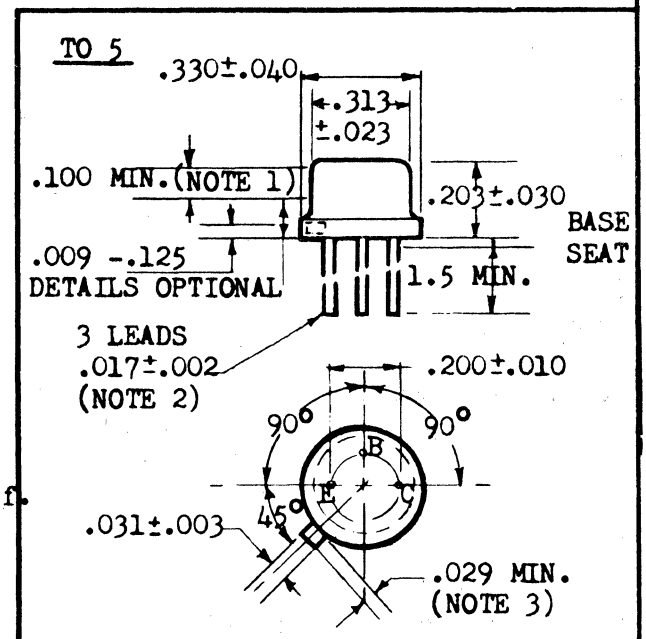
hFE (min) 65 @ Ib = 1 MA VCE = .25 V

* SATURATION

NOTE: Time Response as per ED-69 with

Tf =0.7us MAX, To =0.4us MAX

environmental as per ED-67.



NOTES FOR TO 5:

1. Controlled for automatic handling. Dia. not to exceed .010.
2. Lead dia. variation between .050 and .250 from base seat as specif. Between .250 and 1.5 a max. of .021 dia. is held.
3. Measure from max. dia. of the actual device.

DIGITRONICS
ALBERTSON, NEW YORK

TITLE: TRANSISTOR

REV	E.C.O.	CHKD.	APP'D.	MO. DAY YR.
A				9/13/62

USED ON: DIGITRONICS PART NUMBERS

DRAWING NO. TQ-SA317A

I. TRANSISTOR	CLASS	MATERIAL	POLARITY
2N 357A	SWITCH	Ge	NPN

II. PARAMETERS (at 25 degrees C unless otherwise noted)

POWER DISSIPATION 150 MW _____ DERATING FACTOR 2 MW/°C

IC (max) 400 MA

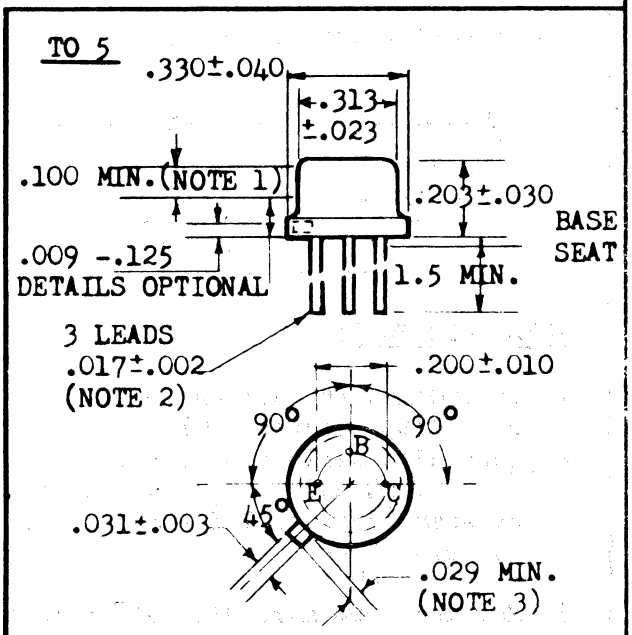
BVCBO (min)	30 V	@ Ic = 25 uA	*VCE (max)	0.5	@ Ic = 200 MA IB = 10 MA
BVCES (min)	25V	@ Ic = 100 ua	*VCE (max)		@
BVCEO (min)		@	*VBE (max)	o.5V	@ Ic = 200 MA IB = 10 MA
BVEBO (min)	6V	@ IE = 10 ua	*VBE (max)		@
ICBO (max)	25ua	@ VCB = 30 V			
hFE (min)	25	@ Ic = 200 MA Vc = 0.25 V			
hFE (min)		@			

* SATURATION

NOTE: Time Response as per ED-69 with

Tf =0.7us MAX, To =0.4us MAX

environmental as per ED-67.



NOTES FOR TO 5:

1. Controlled for automatic handling. Dia. not to exceed .010.
2. Lead dia. variation between .050 and .250 from base seat as specif Between .250 and 1.5 a max. of .021 dia. is held.
3. Measure from max. dia. of the actual device.

DIGITRONICS
ALBERTSON, NEW YORK

TITLE

TRANSISTOR

REV	E.C.O	CHKD APP'D	DATE
A			9/20/62

USED ON: DIGITRONICS PART NUMBERS

DRAWING NO: TX-55357A

I. TRANSISTOR	CLASS	MATERIAL	POLARITY
GA 005	SWITCH	Ge	NPN

II. PARAMETERS (at 25 degrees C unless otherwise noted)

POWER DISSIPATION 150 MW DERATING FACTOR 2 MW/° C

IC (max) 50 MA

BVCBO (min) 25V @ Ic = 25 ua *VCE (max) 0.5V @ Ic = 5Ma, Ib = 1MA

BVCES (min) 20 @ Ic = 25 ua *VCE (max) _____ @ _____

BVCEO (min) ____ @ _____ *VBE (max) 0.5V @ Ic = 5MA, Ib = 1MA

BVEBO (min) 15V @ Ie = 25 ua *VBE (max) _____ @ _____

ICBO (max) 3 ua @ Vcb = oV

hFE (min) 80 @ Ic = 5MA, Vce = 0.5V

hFE (min) _____ @ _____

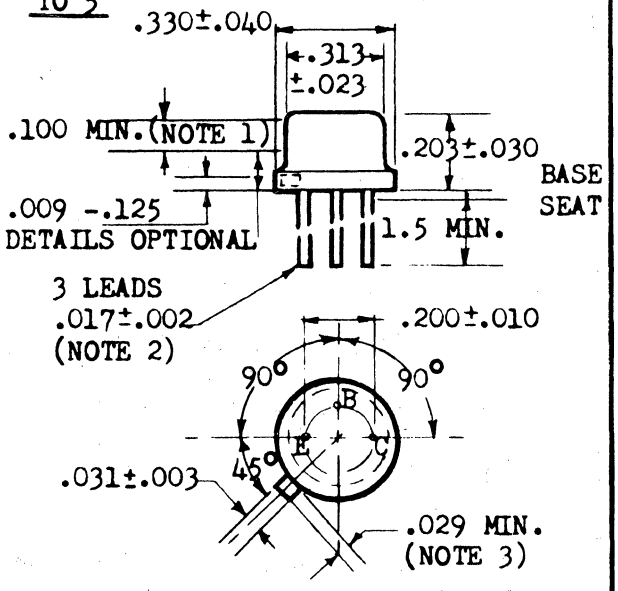
* SATURATION

NOTE: Time response as per ED-69

Tf = 1.0us MAX, To = 0.5us MAX

environmental as per ED-67.

TO 5



NOTES FOR TO 5:

1. Controlled for automatic handling. Dia. not to exceed .010.
2. Lead dia. variation between .050 and .250 from base seat as specif. Between .250 and 1.5 a max. of .021 dia. is held.
3. Measure from max. dia. of the actual device.

DIGITRONICS
ALBERTSON, NEW YORK

TITLE: TRANSISTOR

REV	E.C.O.	CHKD.	APP'D.	MO. DAY YR.
A				9/25/62

USED ON: DIGITRONICS PART NUMBERS

DRAWING NO. TQ_SB0005

I. TRANSISTOR	CLASS	MATERIAL	POLARITY
1659	SWITCH	Ge	NPN

II. PARAMETERS (at 25 degrees C unless otherwise noted)

POWER DISSIPATION 150 mw DERATING FACTOR 2 mw/°C

IC (max) 100 MA

BVCBO (min) 35V @ Ic = 25ua *VCE (max) .2V @ Ic = 20ma, Ib =0.5ma

BVCES (min) 30V @ Ic = 25ua *VCE (max) _____ @ _____

BVCEO (min) _____ @ _____ *VBE (max) .4V @ Ic = 20MA, Ib = 0.5 ma

BVEBO (min) 10V @ IE = 10 uA *VBE (max) _____ @ _____

ICBO (max) 10ua @ VCB = 12 V

hFE (min) 40 @ Ic = 20MA , Vc = 0.5V

hFE (min) 30 @ Ic = 100 MA Vc = 0.5V

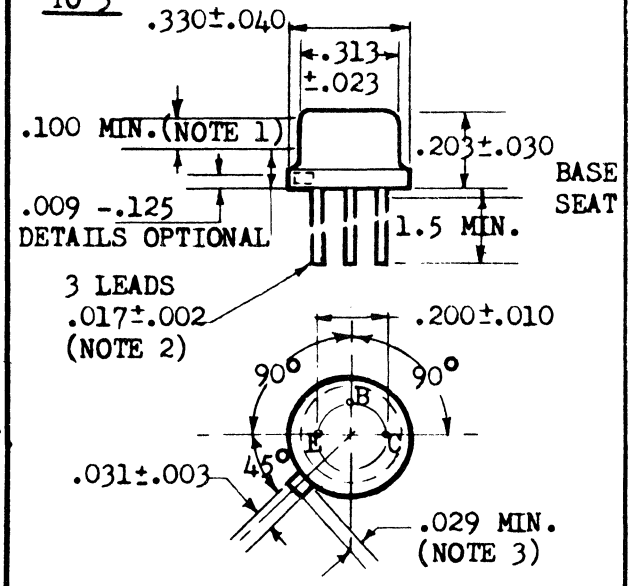
* SATURATION

NOTE: Time Response as per ED-69 with

Tf = 0.7us MAX, To = 0.4us MAX

Environmental as per ED-67.

TO 5



NOTES FOR TO 5:

1. Controlled for automatic handling. Dia. not to exceed .010.
2. Lead dia. variation between .050 and .250 from base seat as specif Between .250 and 1.5 a max. of .021 dia. is held.
3. Measure from max. dia. of the actual device.

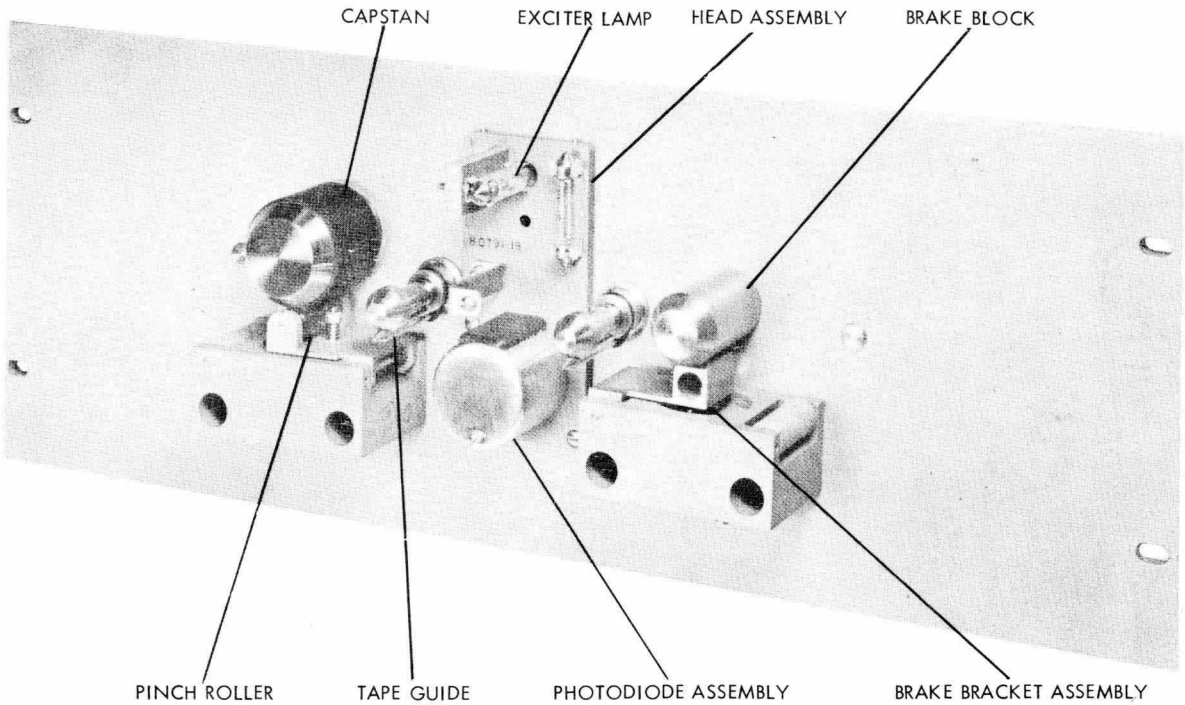
DIGITRONICS
ALBERTSON, NEW YORK

TITLE

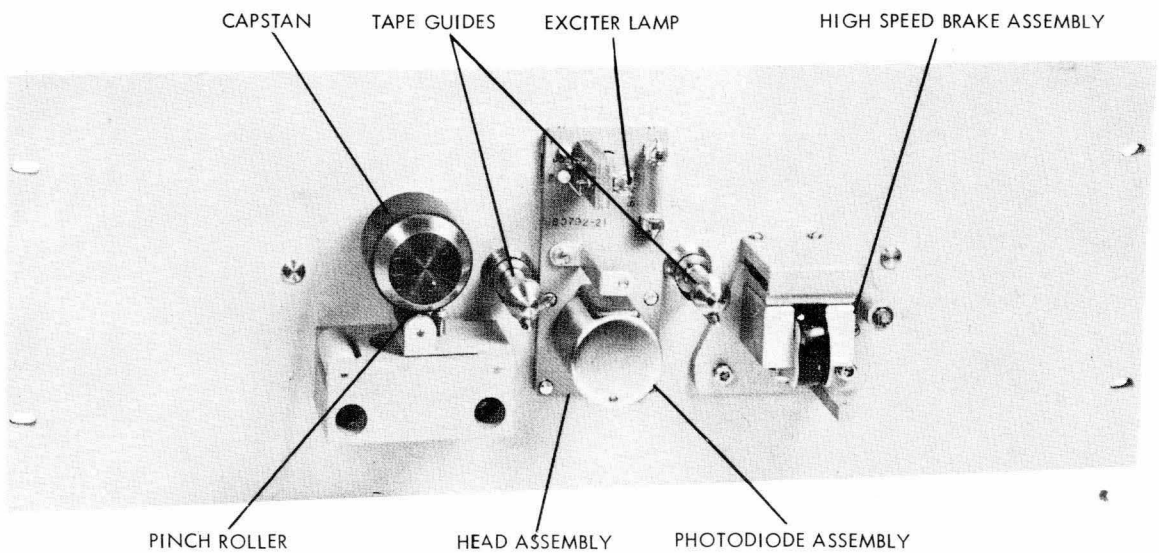
TRANSISTOR

REV	E.C.O.	CHKD.	APP'D.	MO DAY YR.	USED ON:	DRAWING NO.
A				9/20/62	DIGITRONICS PART NUMBERS	TQ- SB1659

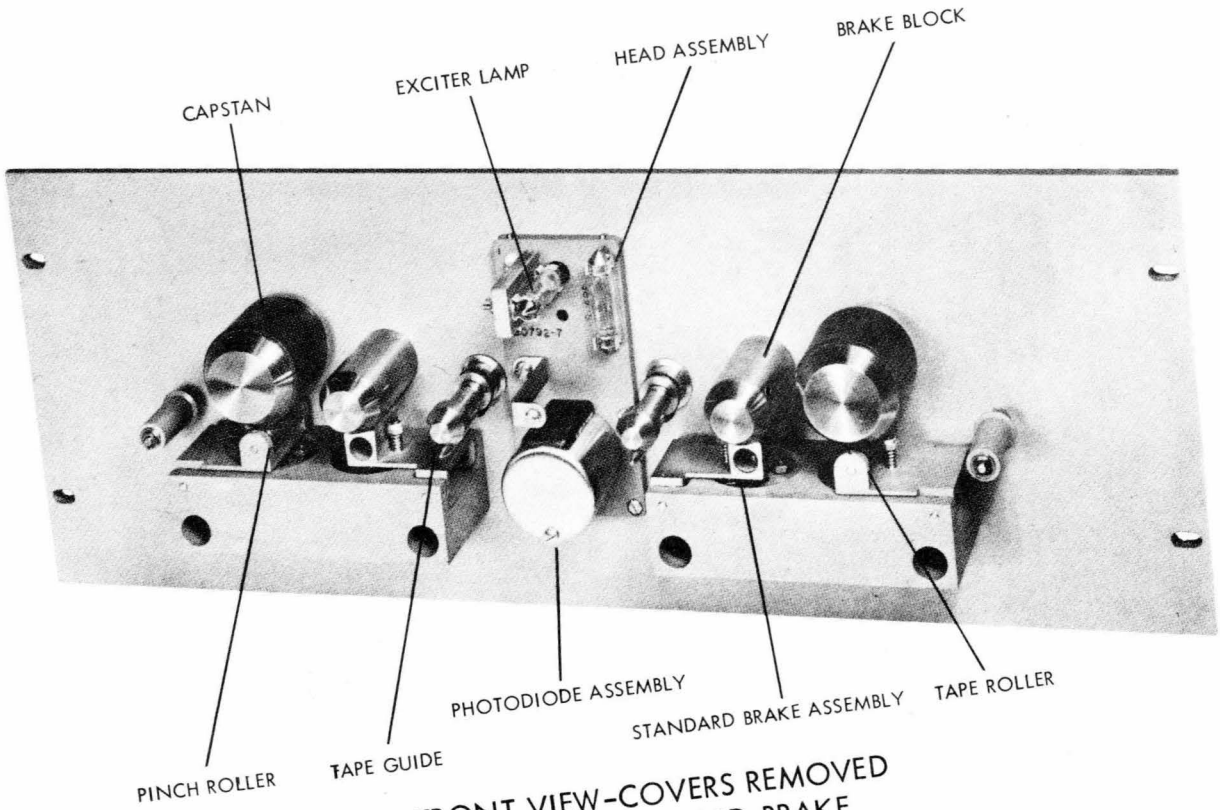
APPENDIX C



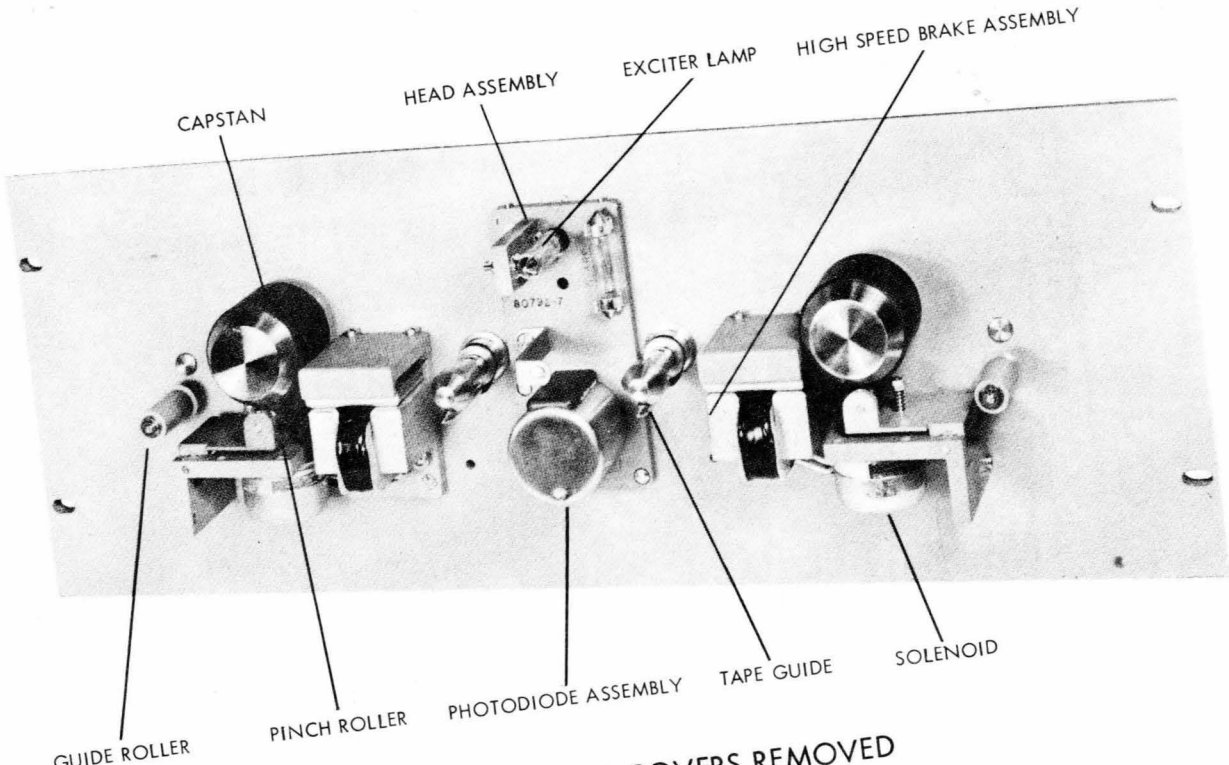
FRONT VIEW-COVERS REMOVED
3500 WITH STANDARD BRAKE



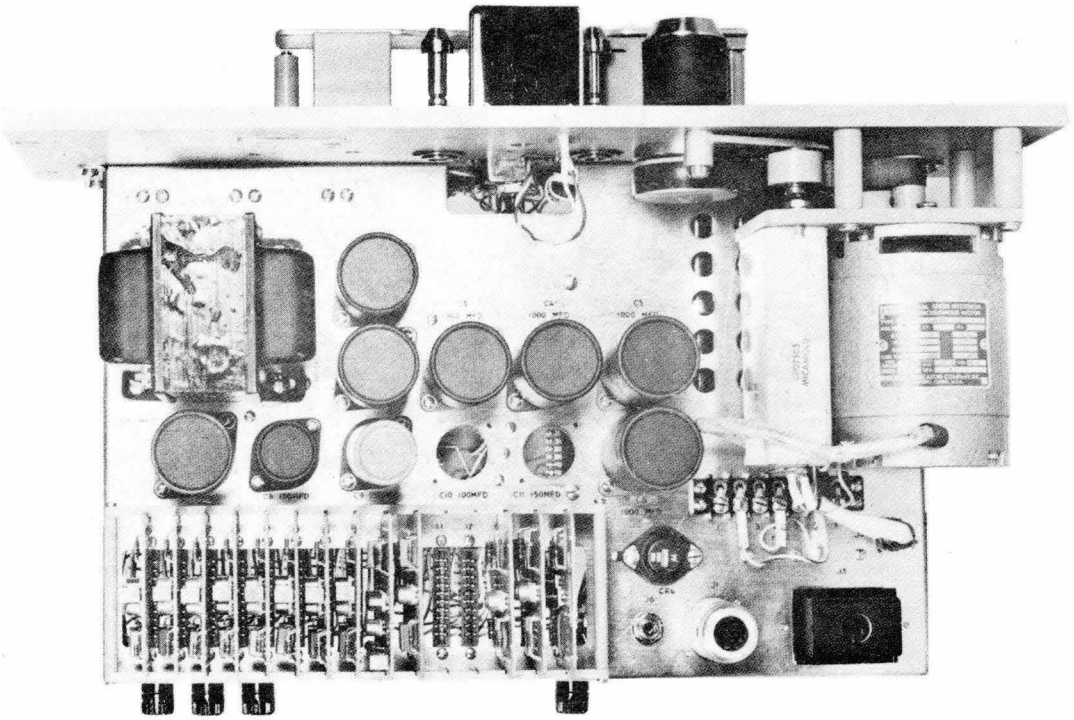
FRONT VIEW-COVERS REMOVED
3500 WITH HIGH SPEED BRAKE



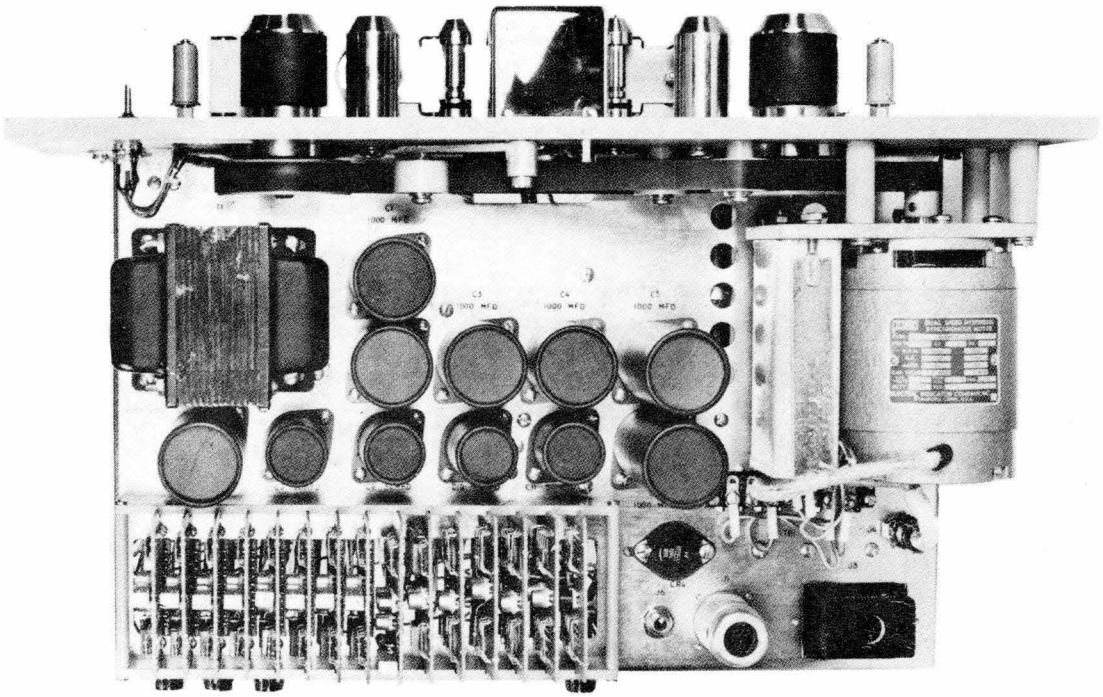
FRONT VIEW-COVERS REMOVED
B3500 WITH STANDARD BRAKE



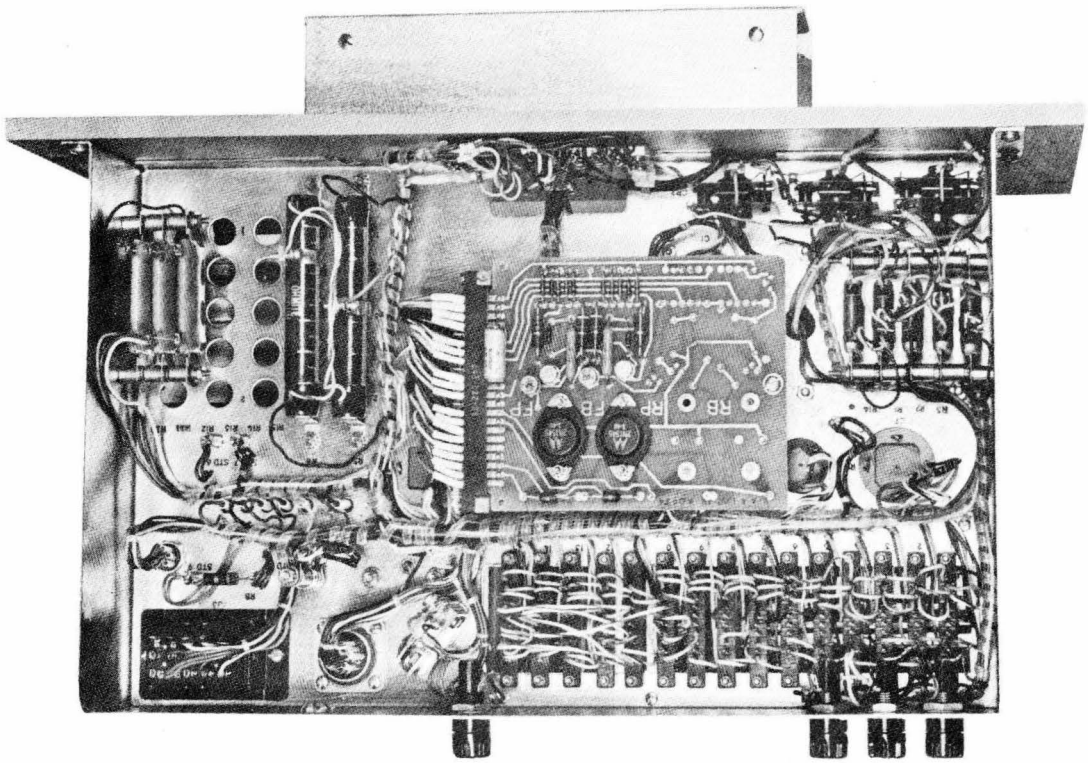
FRONT VIEW-COVERS REMOVED
B3500 WITH HIGH SPEED BRAKES



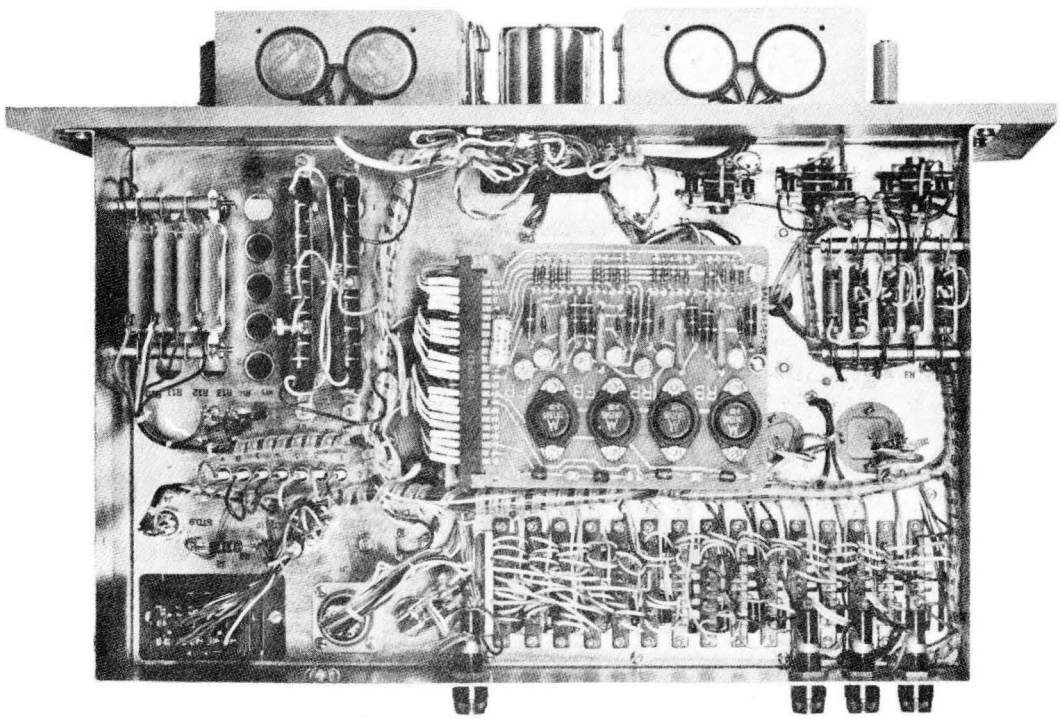
3500 UNI-DIRECTIONAL-TOP VIEW



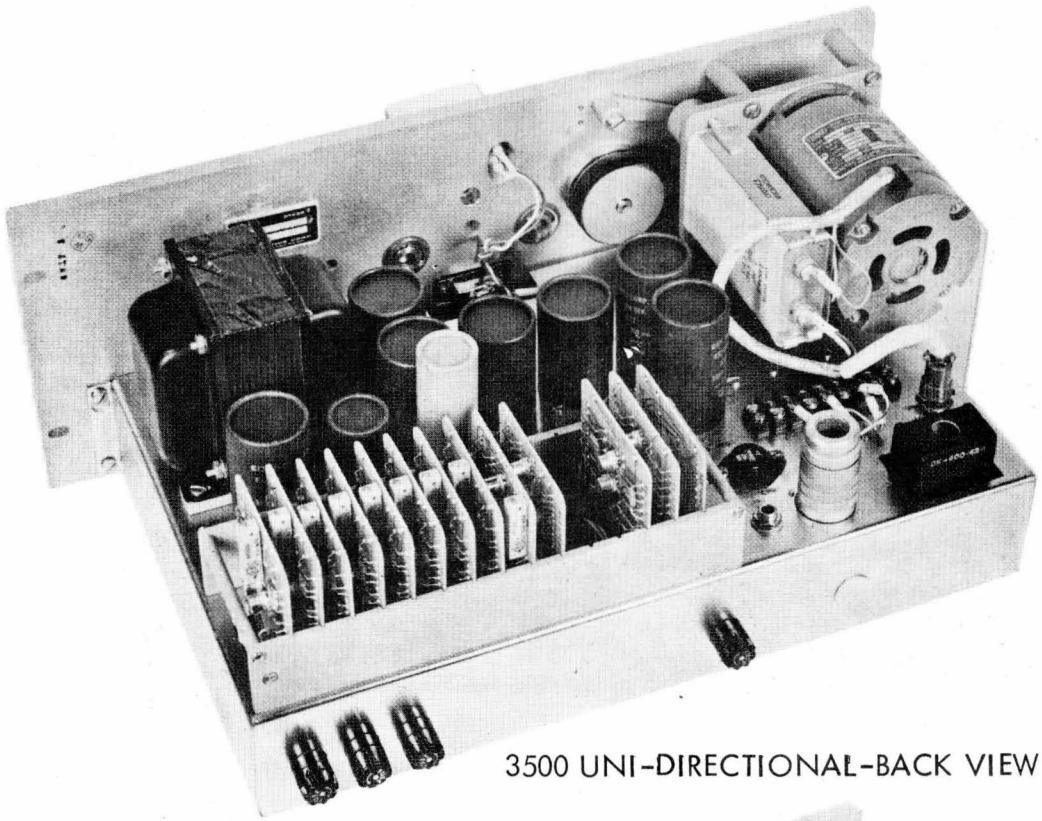
B3500 BI-DIRECTIONAL-TOP VIEW



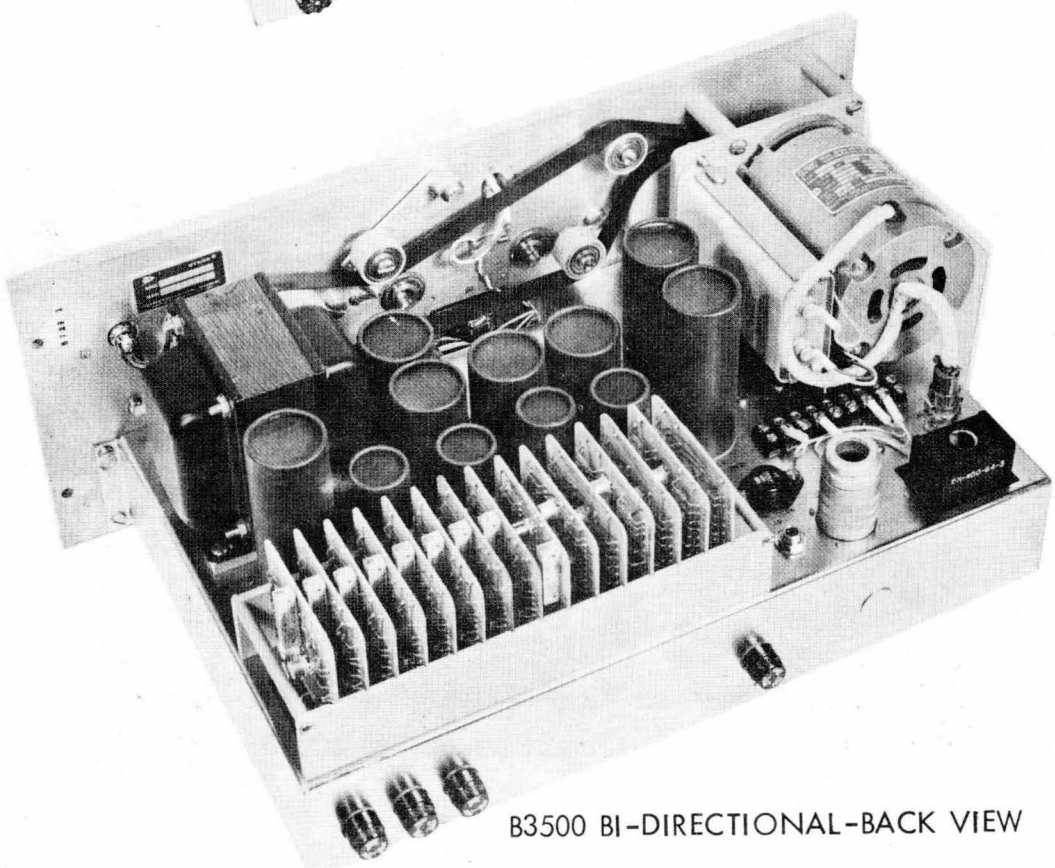
3500 UNI-DIRECTIONAL-BOTTOM VIEW



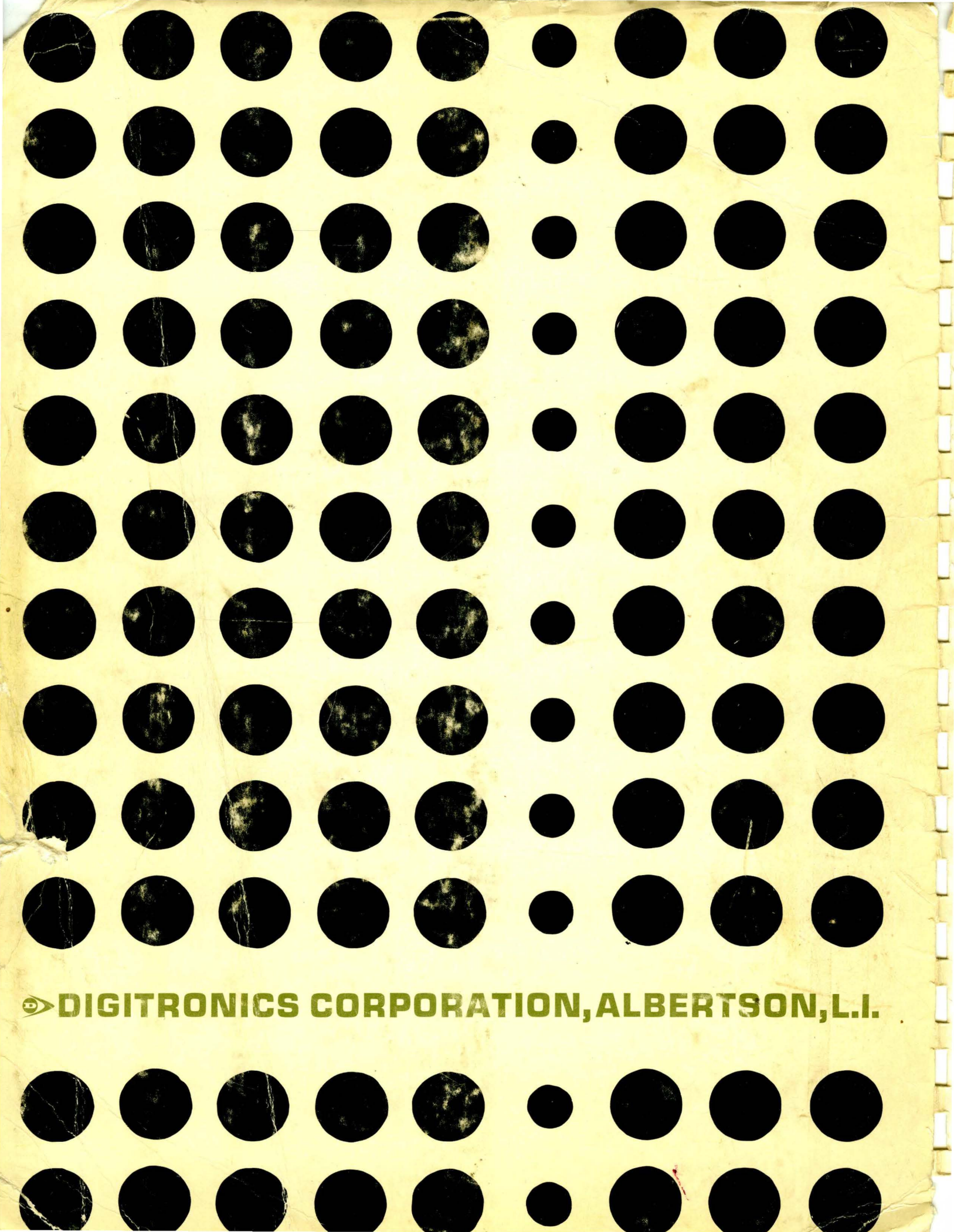
B3500 BI-DIRECTIONAL-BOTTOM VIEW



3500 UNI-DIRECTIONAL-BACK VIEW



B3500 BI-DIRECTIONAL-BACK VIEW



DIGITRONICS CORPORATION, ALBERTSON, L.I.