DSD 5215
Multibus Disk Controller
User Guide

Data Systems Part Number:
040040-01, Revision B

Printed in USA:
April 1984

PREFACE

This manual describes the features, specifications, and programming of the DSD 5215 Multibus Disk Controller. Instructions for equipment installation, operation, and elementary troubleshooting are included.

The material in this manual is subject to change without notice. The manufacturer assumes no responsibility for any errors which may appear.

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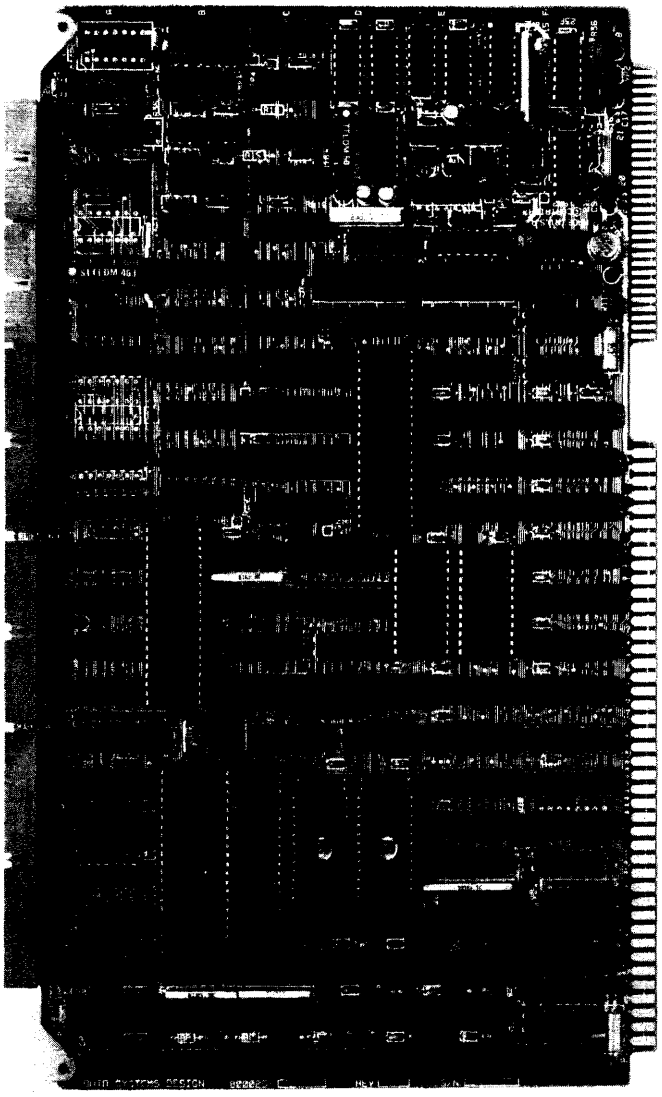


Figure 1-1. DSD 5215 Multibus Controller

1 GENERAL INFORMATION

1.1 Introduction

The DSD 5215 Multibus Disk Controller is a compact single-board controller for 5-1/4 inch Winchester, floppy, and any QIC-02 compatible streaming tape drive. The DSD 5215 emulates the Intel iSBC 215 and iSBX 218 controller combination. Operation is compatible with software and operating systems supporting that product.

This manual provides user information for the DSD 5215 controller. Coverage includes features, specifications, installation, operation, programming, block diagram and architecture, and user level maintenance.

1.2 Features

Features of the DSD 5215 Controller are:

- Standard interfaces for Winchester, floppy, and streaming tape drives.
- All drives are connected pin-for-pin by flat ribbon cables for easier installation.
- All interfaces plus data separation are on a single Multibus card for best system cost.
- Buffering provided for non-interleaved operation and off-line mirror image disk-to-tape backup operations.
- Built in high reliability and data integrity.
- Meets the requirements of the IEEE-P796 specifications for the Multibus standard, including 24-bit addressing.
- Emulates Intel's iSBC 215 and iSBX 218 controller combination.
- Compatible with operating systems supported by Intel, such as RMX-86.

1.3 Self-Test and Diagnostics

Two LEDs, labelled CR1 (ERR) and CR2 (RDY) are mounted on the controller card. These LEDs respond according to the option setting and error condition. LED CR2 (RDY) indicates whether the controller is ready to accept a new command (ON) or is busy (OFF). LED CR1 (ERR) is active when an error is detected. Use of these indicators during initial checkout and acceptance testing is detailed in Chapter 3.

Resident PROM diagnostics (jumper selectable by user) may be used for fault isolation to determine if a problem involves the controller hardware, disk drives, or bus. Refer to Chapter 6 for detailed fault isolation procedures.

1.4 Off-Line Backup Capability

Off-line backup for the Winchester drive can be provided by the quarter-inch streaming tape drive. Tape backup control is provided by an I/O port supporting the QIC-02 interface. This provides the user with high capacity backup at a low cost. Commands are provided for full image backup and restore at five megabytes per minute. The cartridge can store up to 45 megabytes of data.

1.5 Summary

Disk memory systems combining Winchester, floppy, and tape drives are opening new application possibilities for small computer systems. Their functional design and performance rival that of large disk systems costing several times as much. When considering a Winchester based disk memory system, the user should look beyond the usual considerations of capacity and backup and examine the function and capability of the entire system.

Data Systems Design has been an industry leader in the design and manufacture of disk storage systems since 1975. The DSD Multibus Controller is a powerful and effective design offering a combination of price, features, and performance unavailable from any other source. These features are summarized below:

Compatible:

- Multibus compatible board format
- Emulates the iSBC 215 and iSBX 218 combination
- Standard formats for disks (single- and double-density)
- Standard drive interfaces
- IEEE-P796 standard bus, including 24-bit addressing

Flexible:

- Supports floppy, tape, and Winchester
- Variety of standard drive selections
- Up to two disk drives of each type
- 8- or 16-bit I/O address for 8- or 16-bit systems
- Several bus arbitration choices
- Variable disk interleave
- Four sector sizes

Powerful:

- Non-interleaved disk transfer (floppy and Winchester)
- Byte or word transfers
- Burst mode transfer of any length (multiple sector transfers, up to entire disk)
- Overlapped seeks
- Five megabytes per minute disk backup without computer intervention
- Efficient bus arbitration
- Wide bandwidth design
- Memory based commands

Cost Effective:

- Three controllers in one
- No extra boards to buy
- Integrated data separator

Easy to Integrate:

- Single-board, occupies one slot
- One-to-one cable connection
- Easy jumper configuration
- Standard software interface
- Complete table top systems available
- Clear, complete, professional documentation

Reliable:

- Effective media flaw management
- Thorough test and burn-in
- Power up self-test
- Wide margin phase-locked-loop
- Full sector buffering eliminates data overrun and potential for lost data
- ECC for Winchester disk, 22-bit detect, 11-bit correct. Automatic error recovery and retry. Transparent data error correction
- Full disk backup
- Bus time-out eliminates hang-up states
- Conservative, no compromise design

Serviceable:

- Flashing error codes for easy problem identification
- On-board diagnostics for fault isolation
- HyperService with Rapid Module Exchange
- Customer Service hotline

2 SPECIFICATIONS

2.1 Introduction

This section contains specifications, environmental and power requirements, and dimensions for the DSD 5215 Controller/Interface.

Specifications listed in Table 2-1 include drive characteristics for Winchester, floppy, and tape drives. Requirements include those for interface cabling and connectors, and pin assignments for the controller connectors.

Table 2-1. Specifications

General:

Multibus Interface	IEEE P796, Master D16M24, Slave D8116VOEL
I/O Address	User selectable, 8 or 16 bit
Data Transfers	8 or 16 bits wide
Drive Capacity	Any capacity drive with supported interface
Memory Addressing	20 or 24 bit addressing
Bus Arbitration Modes	Jumper selectable: Single transfer Yield to any request Yield to higher priority Override
Interrupts	One interrupt, jumpered by user to any one of Multibus lines INT0/ to INT7/

Standard Interfaces:

Winchester	ST506
Floppy	SA460
Tape	QIC-02

DMA Bus Usage: (Single transfer mode)

Reading from bus	0.9 usec plus memory read access time/word
Writing to bus	0.5 usec plus memory write access time/word

Recording Formats:

FM	Single-density floppy
MFM	Winchester and floppy

Formatting:

Winchester:				
Sector Size (Bytes)	128,	256,	512,	1024
Sectors/Track	54,	31,	17,	9
Floppy:				
Sector Size (Bytes)	128,	256,	512,	1024,
Sectors/Track				
Single-density:	15,	8,	4,	2
Double-density:		15,	8,	4

Data Rates:

Winchester	5 Mbits/sec
Floppy	250 Kbits/sec
Tape	87 Kbytes/sec

Transfer Rates:

Winchester (Non-interleaved format)	
	1024 byte sectors
Within a sector	625 Kbytes/sec
Within a cylinder	529 Kbytes/sec
Across entire disk (8 tracks/cylinder)	410 Kbytes/sec
Floppy	256 byte sectors 31.25 Kbytes/sec

Error Detection/Correction:

Floppy and Tape	CRC checksum
Winchester	32-bit ECC polynomial 22-bit burst error detection 11-bit burst error correction
Activity Lights	Two LED indicators (also used by HyperDiagnostics)

Environmental Specifications:

Operating Temperature	41°F to 131°F (5°C to 55°C)
Humidity	Up to 90% non-condensing
Cooling	DSD 5215 dissipates 24W of heat (80 BTU/hr). Adequate air circulation must be maintained to prevent a temperature rise above 131°F (55°C).

Power Requirements:

+5 Vdc, ±5% @ 5.1 Amp typical
+12 Vdc, ±5% @ 0.1 Amp typical

Physical Specifications:

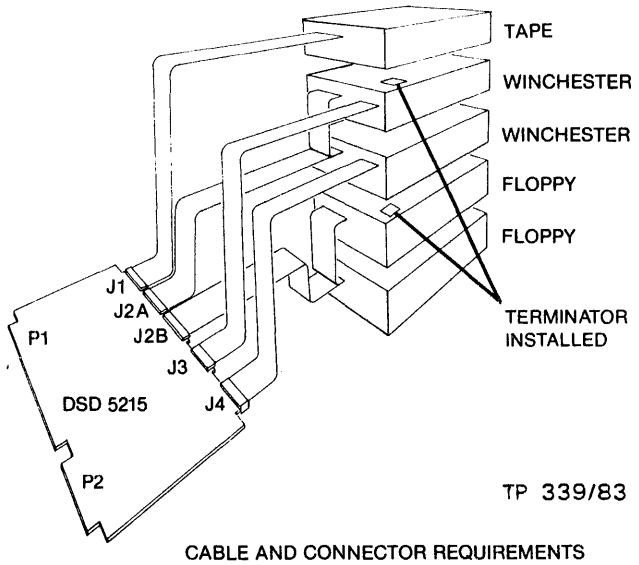
Mounting	Occupies one card slot in the Multibus backplane.
Dimensions	Width: 12.0 in. (30.5 cm.) Height: 7.1 in. (18 cm.) Thickness: 0.6 in. (1.5 cm.)

2.2 Cables and Connectors

Figure 2-1 shows all connector and cabling requirements. The connectors (wired pin-to-pin) used with J1 through J4 are female connectors with 1/10-inch pin spacing.

2.2.1 Multibus P1 and P2 Configurations

The controller communicates with the CPU via the Multibus interface. Table 2-2 and 2-3 list the Multibus connector pin assignments. Table 2-4 describes the controller/Multibus interface signals. Figure 2-2 is a diagram of the controller/Multibus interface timing signals with timing requirements. The controller is connected to the Multibus interface through connector P1, an 86-pin, double-sided, printed circuit edge connector. Connector P2 provides for optional Multibus signals, as listed in Figure 2-1.



CABLE AND CONNECTOR REQUIREMENTS

P1: 86 – PIN MULTIBUS CONNECTOR
P2: 60 – PIN OPTIONAL MULTIBUS SIGNALS
J1: 50 – PIN TAPE DRIVE CONNECTOR
CABLE IS 32 FEET (10 METERS) MAXIMUM.
J2A: 34 – PIN DRIVE CONTROL CONNECTOR
CABLE IS 20 FEET (6 METERS) MAXIMUM.
J2B: 34 – PIN DRIVE CONTROL CONNECTOR
CABLE IS 10 FEET (3 METERS) MAXIMUM.
J3: 20 – PIN WINCHESTER DATA CONNECTOR
CABLE IS 20 FEET (6 METERS) MAXIMUM.
J4: 20 – PIN WINCHESTER DATA CONNECTOR
CABLE IS 20 FEET (6 METERS) MAXIMUM.

J3 AND J4 ARE INTERCHANGEABLE.

Figure 2-1. Cable and Connector Configuration

Table 2-2. Multibus P1 Connector Pin Assignment

Component Side Pin	Signal Name	Circuit Side Pin	Signal Name
Power Supplies:			
1	GND	2	GND
3	+5Vdc	4	+5Vdc
5	+5Vdc	6	+5Vdc
7	+12Vdc	8	+12Vdc
9	-5Vdc (Not Used)	10	-5Vdc (Not Used)
11	GND	12	GND
Bus Controls:			
13	BCLK/	14	INIT/
15	BPRN/	16	BPRO/
17	BUSY/	18	BREQ/
19	MRDC/	20	MWTC/
21	IORC/	22	IOWC/
23	XACK/	24	INH1/
Bus Controls and Address Bus:			
25	Reserved	26	INH2/ (Not Used)
27	BHEN/	28	ADR10/
29	CBRQ/	30	ADR11/
31	CCLK/	32	ADR12/
		34	ADR13/
Interrupts:			
33	INTA/		
35	INT6/	36	INT7/
37	INT4/	38	INT5/
39	INT2/	40	INT3/
41	INT0/	42	INT1/
Address Bus:			
43	ADRE/	44	ADRF/
45	ADRC/	46	ADRD/
47	ADRA/	48	ADRB/
49	ADR8/	50	ADR9/
51	ADR6/	52	ADR7/
53	ADR4/	54	ADR5/
55	ADR2/	56	ADR3/
57	ADR0/	58	ADR1/
Data Bus:			
59	DATE/	60	DATF/
61	DATC/	62	DATD/
63	DATA/	64	DATB/
65	DAT8/	66	DAT9/
67	DAT6/	68	DAT7/
69	DAT4/	70	DAT5/
71	DAT2/	72	DAT3/
73	DAT0/	74	DAT1/
Power Supplies:			
75	GND	76	GND
77	Reserved	78	Reserved
79	-12Vdc (Not Used)	80	-12Vdc (Not Used)
81	+5Vdc	82	+5Vdc
83	+5Vdc	84	+5Vdc
85	GND	86	GND

"/" following the signal name indicates an active low.

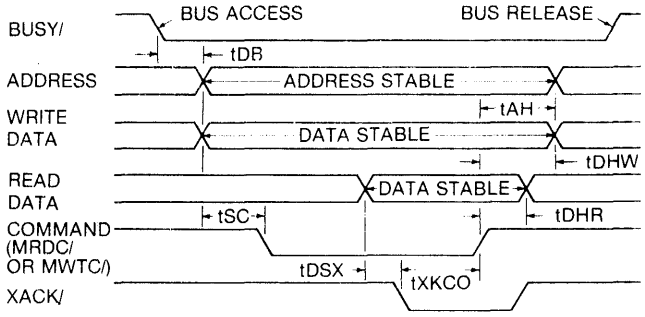
Table 2-3. Multibus P2 Connector Pin Assignment

Pin	Signal Name	Pin	Signal Name
55	ADR16/(Hex)	56	ADR17/(Hex)
57	ADR14/(Hex)	58	ADR15/(Hex)

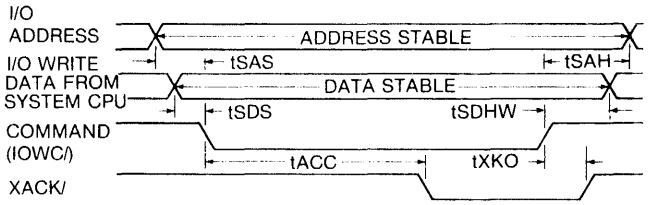
Table 2-4. Controller/Multibus Signals

Signal	Functional Description
ADR0/– ADRF/, ADR10/– ADR13/	**Address**: These 20 lines transmit the address of the memory location or I/O port to be accessed. For memory access, ADR0/(when active) enables the even byte bank DAT0/– DAT7/ on the Multibus connector; i.e., ADR0/ is active for all even addresses. ADR13/ is the most significant address bit.
BCLK/	**Bus Clock**: Used to synchronize the bus contention logic on all bus masters.
BHEN/	**Byte High Enable**: When active low, enables the odd byte bank (DAT8/– DATF/) onto the Multibus connector.
BPRN/	**Bus Priority In**: When low, indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	**Bus Priority Out**: In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	**Bus Request**: In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	**Bus Busy**: Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	**Common Bus Request**: Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller raises the CBRQ/ signal.
DAT0/– DATF/	**Data**: These 16 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF/ is the most significant bit. For data byte operations, DAT0/– DAT7/ is the even byte and DAT8/– DATF/ is the odd byte.
INIT/	**Initialize**: Reset the entire system to a known internal state.
INT0/– INT7/	**Interrupt Request**: These eight lines transmit interrupt requests to the appropriate interrupt handler. INT0/ has the highest priority.
IOWC/	**I/O Write Command**: Indicates that the address of an I/O port is on the Multibus connector address lines and that the contents on the Multibus connector data lines are to be accepted by the addressed port.
MRDC/	**Memory Read Command**: Indicates that the address of a memory location is on the Multibus connector address lines and that the contents of the location are to be read (placed) on the Multibus connector data lines.
MWTC/	**Memory Write Command**: Indicates that the address of a memory location is on the Multibus connector address lines and that the contents on the Multibus connector data lines are to be written into that location.
XACK/	**Transfer Acknowledge**: Indicates that the address memory location has completed the specified read or write operation. That is, data has been placed onto or accepted from the Multibus connector data lines.

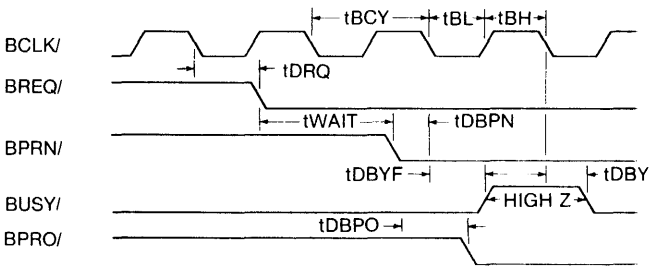
MASTER COMMAND ACCESS TIMING



SLAVE COMMAND TIMING



BUS EXCHANGE TIMING



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Parameter	Nanoseconds Min	Max	Description
tDB		61	Busy–to–address/data delay
tSC	60		Address/ data set–up to CMD
tXKCO		500	XACK/ to CMD turn off
tAH	50		Address hold time
tDHW	50		Data hold time
tDHR	0		Read data hold time
tDSX	0		Data set–up time before XACK/
tSAS	23		Address set–up time to I/O CMD
tSDS	32		Data set–up time to I/O CMD
tSAH	36		Address hold time from I/O CMD
tSDHW	50		Data hold time from I/O CMD
tACC		77	I/O access time
tXKO	10	63	XACK/ hold time from I/O CMD
tBCY	100		Bus clock cycle time
tBL	35	65	Bus clock low
tBH	35	65	Bus clock high
tDRQ		32	Bus request delay
tDBY		48	Bus busy turn on delay
tDBYF		65	Bus busy turn off delay
tDBPN	0		Priority input set–up time
tDBPO		7	BPRO/ serial delay from BPRN/
tWAIT		∞	Requesting master bus access time

Figure 2-2. Master Command Access Timing

2.2.2 Connector Configuration, J1 Through J4

Tables 2-5 through 2-8 show the pin assignments for controller drive connectors J1, J2A, J2B, J3, and J4. These connectors are mounted on the component side of the board with an embossed arrow to indicate pin 1. The odd numbered pins of these connectors are the upper row of pins.

Table 2-5. Tape Drive Control Connector J1

Pin	Signal	Description
2,4,6,8,10		**Reserved.**
12	HB7/	**Host Bus Bit 7.** MSB of eight-bit bidirectional data bus.
14	HB6/	**Bit 6**
16	HB5/	**Bit 5**
18	HB4/	**Bit 4**
20	HB3/	**Bit 3**
22	HB2/	**Bit 2**
24	HB1/	**Bit 1**
26	HB0/	**Bit 0.** LSB of eight-bit bidirectional data bus.
28	ONL/	**On-Line.** Control signal to terminate a read/write operation. On-line going false terminates the command and returns tape to beginning of tape (BOT).
30	REQ/	**Request.** User by host to inform controller that a command is on data bus. Also to handshake status information from controller to host.
32	RES/	**Reset.** Used after power up to initialize drive and controller and to recalibrate drive head position.
34	XFER/	**Transfer.** Host handshake signal to transfer data to and from drive. During read operation, XFER going true means host has received data. During write, XFER going true means host has put data on bus.
36	ACK/	**Acknowledge.** Controller handshake signal to transfer data to and from drive. During read, ACK going true means data is available on bus for host. During write, ACK going true means data has been received by the controller.
38	RDY/	**Ready.** Used by controller for following functions: 1. Ready in true state indicates controller can accept new command. 2. During command transfer, RDY going true means command has been read. 3. Used to signal asynchronous transfer of status information from controller to host. 4. Used to indicate that a block of data is ready to be transferred.
40	EXC/	**Exception.** Used by controller to inform host of a condition which has terminated an operation. When EXC goes true, host must respond with a Read Status Command.
42	DIR/	**Direction.** Used by controller to indicate the direction of data flow on data lines. When true, flow of data is from controller to host.
44,46,48,50		**Reserved**

All odd numbered pins, 1-49, are at signal ground.

Table 2-6. Winchester Drive Control Connector J2A

Pin	Signal	Description
2	RWC/	**Reduce Write Current.** When true, the lower value of write current is selected.
	OR HS2^3/	**Head Select Line (2^3bit)** For class 5, or higher, drives not requiring reduced write current.
4	HS2^2/	**Head Select Line (2^2 bit)**
14	HS2^0/	**Head Select Line (2^0 bit)**
18	HS2^1/	**Head Select Line (2^1 bit)**
6	WG/	**Write Gate.** When true, enables write data to be written to disk. When false, enables transfer of data from drive and enables step pulses to reposition head arm.
8	SKCOMP/	**Seek Complete.** True when heads settled on final track at completion of a seek.
10	TRK000/	**Track 000.** True only when heads are at track zero.
12	WTFLT/	**Write Fault.** Indicates drive condition exists that could cause improper writing on disk. Occurs when write current in the head without write gate active or multiple heads are selected.
16		**Reserved.**
20	INDEX/	**Index.** Drive provides this signal once each revolution to indicate beginning of track.
22	RDY/	**Ready.** When true, together with seek complete, indicates drive is ready to read, write, or seek, and that the signals are valid.
24	STEP/	**Step.** Causes heads to move in the direction defined by direction in line.
26	DS1/	**Drive Select 1-2.** When true, connects
28	DS2/	the selected drive to the control lines. Only one drive select line may be active at a time.
30,32		**Reserved.**
34	DIRC/	**Direction In.** Defines the direction of motion of the heads when step line is pulsed. Direction in true and step line is pulsed, the heads will move toward center of disk.

All odd numbered pins, 1-33, are at signal ground.

Table 2-7. Floppy Drive Control Connector J2B

Pin	Signal	Description
2,4,14,34		**Reserved**
6	RDY/	**Ready.** When true, indicates drive is ready for read/write operations.
8	INDEX/	**Index.** Signal provided by drive each time an index hole is sensed by photo detector.
10	DS1/	**Drive Select 1-2.** When true, connects the selected drive to control lines. Only one drive select line may be active at a time.
12	DS2/	
16	MTR ON/	**Motor On.** When true, will turn on drive motor allowing read/write operations.
18	DIRC IN/	**Direction In.** Defines direction of motion of heads when step line is pulsed.
20	STEP/	**Step.** Causes heads to move in direction defined by direction in line.
22	WR DATA/	**Write Data.** This line provides the data to be written on disk.
24	WG/	**Write Gate.** When true, allows write data to be written on disk.
26	TRK 00/	**Track 00.** When true, indicates heads are at track zero.
28	WR PROT/	**Write Protect.** Signal provided by drive to indicate write protected disk installed.
30	RD DATA/	**Read Data.** This line provides raw data (clock and data together) as detected by the drive electronics.
32	S SEL/	**Side Select.** This signal defines which side of a two-sided disk is to be written to or read from. True means side 0 of head.

All odd numbered pins, 1-33, are at signal ground.

Table 2-8. Winchester Data Connectors J3 and J4

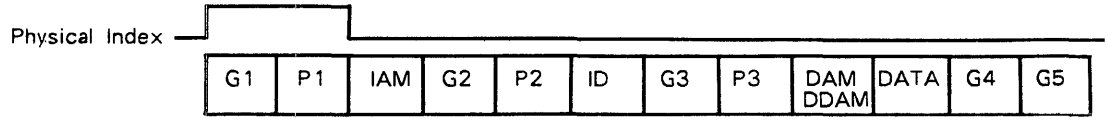
Pin	Signal	Description
1	DS/	**Drive Select.** When true, drive is connected to I/O lines.
13	+WR DATA/	**+Write Data.** Defines bits written to disk.
14	-WR DATA/	**-Write Data.** Defines bits written to disk.
17	+RD DATA/	**+Read Data.** Data recovered by reading disk.
18	-RD DATA/	**-Read Data.** Data recovered by reading disk.

J3 and J4 have identical pinouts and are interchangeable. Pins 2,4,6,8,11, 12,15,16,19, and 20 are at signal ground. Pins 3,5,7,9, and 10 are spares.

2.3 Disk Drive Formats

The Winchester and floppy disk drives operate with all standard iSBC 215 sector sizes. These include the 128, 256, 512, and 1024 bytes per sector formats. The floppy disks handle standard formats, single-density (128 to 1024 bytes per sector) and double-density (256 to 1024 bytes per sector), including double-sided. See Table 2-9. This flexibility enables the user to copy programs from one format to another using the Winchester as intermediate storage.

Table 2-9. Disk Formats



	Sectors/ Track	Bytes/ Sector	G1	P1	IAM	G2	P2	ID	G3	P3	DAM DDAM	DATA	G4	G5
Single-Density			FF	00	FC/DC	FF	00		FF	00	FB/C7 F8/C7		FF	FF
IAM=FC/D7	15	128	40	6	1	26	6	7	11	6	1	130	27	232
IDAM=FE/C7	8	256	40	6	1	26	6	7	11	6	1	258	42	404
DAM=FB/C7	4	512	40	6	1	26	6	7	11	6	1	514	58	640
DDAM=F8/C7	2	1024	40	6	1	26	6	7	11	6	1	1026	170	598
										Repeat				Total 3125
Double-Density			4E	00		4E	00		4E	00			4E	4E
IAM=3(C2/14),FC	15	256	80	12	4	50	12	10	22	12	4	258	54	524
IDAM=3(A1/0A),FE	8*	512	80	12	4	50	12	10	22	12	4	514	80	872
DAM=3(A1/0A),FB	4	1024	80	12	4	50	12	10	22	12	4	1026	116	1296
DDAM=3(A1/0A),F8														
										Repeat				Total 6250
Winchester						4E	00		4E	00			4E	4E
IDAM=A1/0A,FE	54	128				4	12	10	3	6	2	132	21	368
DAM=A1/0A,FB	31	256				4	12	10	3	6	2	260	30	399
DDAM=A1/0A,F8	17	512				4	12	10	3	6	2	516	44	331
	9	1024				4	12	10	3	6	2	1028	61	314
										Repeat				Total 10416

*IBM Personal Computer Format

Write to read recovery time left in addition to a six percent drive speed tolerance gap:
128: 20 μs; 256: 22 μs; 512: 20 μs; 1024: 0 μs.

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2.4 Drive Characteristics

One method of classifying Winchester and floppy drives is according to control timing sequence, precompensation requirements, and for Winchester drives only, requirements for reduced write current.

Tables 2-10 and 2-11 show characteristics of Winchester and floppy drives respectively with some drives grouped according to the indicated characteristics. Not all drives are listed, only a representative selection to show examples of drives matched to chosen characteristics. Contact the factory for correct jumper configuration for higher performance Winchester drives not listed.

These tables will be referred to again in Chapter 3, to show required board jumper settings for drive groups listed.

WINCHESTER CONTROL TIMING/PRECOMP/READ WRITE CURRENT

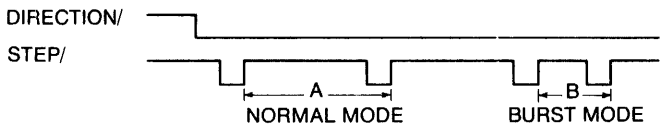

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Table 2-10. Winchester Drive Characteristics

Drive Class	STEP/ Normal A	STEP/ Burst B	Precomp 12 ns Cylinders	Reduced Write Current Cylinders
0	3 ms	25 µs	≥128	≥128
1	3 ms	25 µs	≥77	≥77
2	2 ms	25 µs	≥0	≥132
3	3 ms	25 µs	≥0	≥96
4	3 ms	3 ms	≥128	≥128
5	3 ms	10.8 µs	none	none
6	3 ms	10.8 µs	≥320	none
7	3 ms	10.8 µs	≥256	none

Drive Class	Typical Drive Types
0	ST412; SA602, 604, 606; Tandon 602, 603; CDC 9415-21-5 CMI CM5206, 5412
1	RMS 503, 506, 512
2	PYXIS 7, 13, 20, 27 (Rodine)
3	PYXIS 4, 8, 12, 16 (Ampex)
4	ST506
5	Et 5510, 5520, 5530, 5540; XT-1065, 1105, 1140; V130, V150, V170
6	3020, 3033, 3046 (Atasi)
7	Q-500 (Quantum)

FLOPPY CONTROL TIMING/PRECOMP

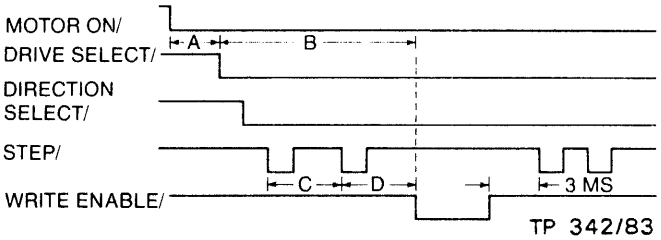

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Table 2-11. Floppy Drive Characteristics

Drive Class	Motor On A	Head Load B	Step Settle C	Seek Settle D	Precomp 160 ns
0	250 ms	50 ms	3 ms	15 ms	None
1	500 ms	50 ms	6 ms	15 ms	*
2	1500 ms	75 ms	30 ms	50 ms	*
3	Reserved				

Drive Class	Typical Drive Types
0	Mitsubishi M4853; Tandon TM100-3, -4
1	CDC 9409-T; Tandon TM100-1, -2; Shugart SA410, SA460; MPI 51, 52
2	Pertec FD200, 250; Shugart SA400, 450; BASF 6106, 6108; Micropolis 1015 I, II, III, IV, V, VI; Qumetrak 592; TEAC 50A, 50C, 50F
3	Reserved

*If cylinder ≥ 1/2 (total) +4

3 INSTALLATION

3.1 Introduction

This chapter contains information on unpacking, inspection, configuration, and initial checkout of the DSD Multibus Disk Controller.

3.2 Unpacking and Inspection

When the DSD Controller arrives, inspect the shipping container immediately for evidence of mishandling during transit. If the container is damaged, request that the carrier's agent be present when the package is opened. Compare the packing list attached to the shipping container against your purchase order to verify the shipment is correct.

Unpack the shipping container and inspect each item for external damage such as broken controls and connectors, or scratches and loose components. If damage is evident, notify DSD Customer Service immediately.

Retain the shipping container and packing materials for examination in the settlement of claims, or for future use.

3.3 Installation

The controller board may be installed in any Multibus-compatible backplane that meets the power and cooling requirements specified in Chapter 2. Note that power **MUST** be **OFF** when installing or removing controller board.

Up to two floppies and two Winchesters may be connected to the controller (see Figure 2-1).

Note

Terminators must be installed in last floppy drive and last Winchester drive.

3.4 Jumper Options

Jumper options allow the user to tailor the installation to the requirements of his particular system. Figure 3-1 shows jumper locations and pin configuration of each jumper on the controller board.

Normally, jumper options are exercised by placing a Berg mini-jumper on the indicated pins. The exception to this is jumper W10. It is wire-wrapped at the factory because the physical layout of the pins precludes the use of the mini-jumpers.

3.4.1 Jumper Configurations

Tables 3-1 and 3-2 summarize the DSD Controller jumper configuration installed at the factory. Table 3-1 covers all board jumpers except W6, W7, and W9. These jumpers are of slightly different configuration and are described in Tables 3-2, 3-3, and 3-4. Jumpers W2, W4, and W13 are for factory use only, and should not be changed in the field. User should note that there are no jumpers labelled W1, W11, or W12 on the board.

Jumper groups W7 and W9 (Table 3-2) select the 8-or 16-bit I/O port address. This address is logically related to the memory address of the wake up block. Refer to paragraphs 4.5.4 and 4.5.5 for details on address selection. W-9 contains the low order bits (0 to 7) and W7 the high order bits (8 to 15) of the WUA jumper setting. These bits are set at the factory to 0F70 hex.

Jumper W6 provides options for selection of types of drives supported by the controller (See Table 3-3 and 3-4). It is also used to select off-line diagnostic testing. Refer to Chapter 6 for using W6 Jumper group with off-line HyperDiagnostics.

Table 3-1. Jumper Configurations

Jumper	Function	Factory Setting Pins	IN	OUT	Options	Remarks
W2	Factory Use Only	1-2	X		None.	Leave as set.
W3	Byte- or Word-Size Data Transfers	1-2		X	Byte-size data bus selected. IN selects 16-bit data bus.	User option.
W4	Factory Use Only	1-2 3-4	X X		None.	Leave as set.
W5	Bus Arbitration Mode Select	1-2 2-3 2-4 5-6	X	 X X X	Yield to higher priority mode. IN= yield to any request mode. IN= single-transfer mode. 1-2 and 5-6 IN = override mode.	User option. Except for override mode, only one jumper at a time is IN. See Paragraph 3.4.3.
W8	Serial or Parallel Bus Priority Continuity	1-2	X		Serial bus priority scheme selected. OUT= parallel bus priority scheme.	User option.
W10	Interrupt Priority Level Select	C-0 C-1 C-2 C-3 C-4 C-5 C-6 C-7	 X 	X X X X X X X	Priority level 0 (Highest) Priority level 1 Priority level 2 Priority level 3 Priority level 4 Priority level 5 (Factory Set) Priority level 6 Priority level 7 (Lowest)	User option. Factory set at level 5. Factory wire-wrapped. User may change as required.
W13	Factory Use Only	1-2	X		None.	Leave as set.
W14	8- or 16-Bit I/O Address Select	1-2 2-3	 X	X	8-bit I/O addressing selected. Reverse selects 16-bit.	User option. Jumpers 1-2 IN, 2-3 OUT selects 16-bit addr.
W15	Factory Set	A B	X	 X	None.	Leave as set.
W16	Factory Set		 X	X	5215-01/03 Version (ECC) 5215-02 Version only (CRC)	Leave as set.

For jumper groups W6, W7, and W9 see page 3-3.
Jumpers W1, W11, W12 are not physically present on the 5215 board.

Table 3-2. W7 and W9 WUA Jumper Configurations

Jumper	Factory Setting Pins	1	0	Hex Setting
W9 sets least significant eight bits to be converted to wake-up address.	0		X	LSB
	1		X	0
	2		X	
	3		X	
	4	X		7
	5	X		
	6	X		
	7		X	
W7 sets most significant eight bits to be converted to wake-up address.	8	X		F
	9	X		
	10	X		
	11	X		
	12		X	MSB
	13		X	0
	14		X	
	15		X	

Address Example: The 16-bit WUA jumper setting (W7 and W9) = 0F70H multiplied by 16 gives the 20-bit Multibus address of WUB = 0F700H.
The 8-bit I/O port address = 70H.
Optionally, the 16-bit I/O port address = 0F70H.

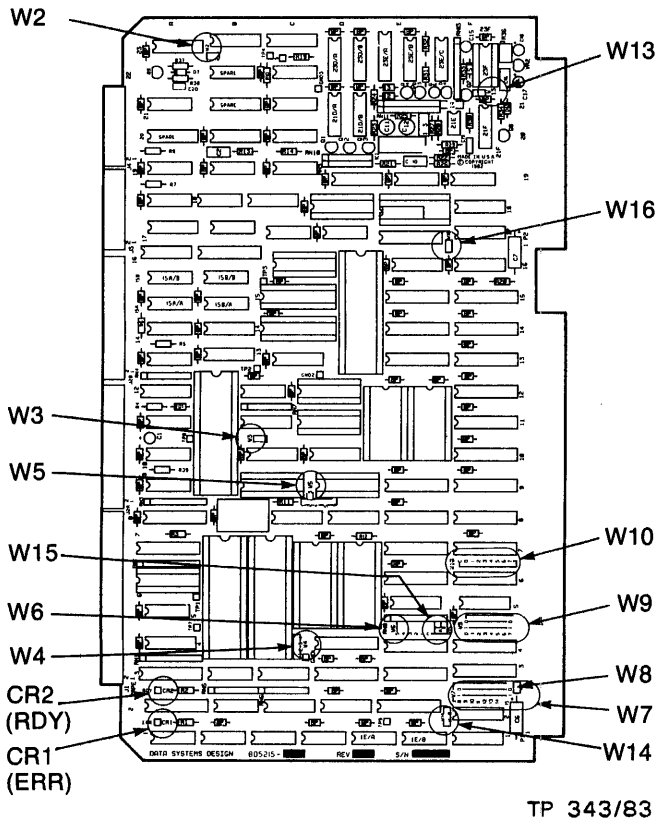

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Figure 3-1. Jumper Locations

3.4.2 Jumper Group W6 Configuration

In Chapter 2, Table 2-10, Winchester drives were classified according to timing control characteristics. Here, these same classifications will be related to jumper group W6 for drive type selection.

The DSD 5215 Controller will handle up to two Winchester drives that are compatible with an ST506 interface. See Table 2-10. If your drive is listed, set jumper W6 as follows in Table 3-3. If your drive is not listed, attempt to match it with classes shown in the table, or call Customer Service for assistance.

Table 3-3. W6 Jumper Configurations, Winchester

Winchester Drive Class	Jumper Group W6 W6-4	W6-3	W6-2
0	IN	IN	IN
1	IN	IN	OUT
2	IN	OUT	IN
3	IN	OUT	OUT
4	OUT	IN	IN
5	OUT	IN	OUT
6	OUT	OUT	IN
7 Reserved	OUT	OUT	OUT

W6-5, normally installed, selects HyperDiagnostics when removed.

Table 2-11, Chapter 2, classifies 5-1/4 inch floppy drives according to control timing characteristics. These classifications are related to jumper group W6 for proper drive type selection in Table 3-4.

The DSD 5215 Controller can handle up to two floppy disk drives compatible with an SA460 interface. See Table 2-11. If your drive is listed, set jumper group W6 as follows. If your drive type is not listed, attempt to match it with classes shown in the table, or call Customer Service for assistance.

Table 3-4. W6 Jumper Configurations, Floppy

Floppy Drive Class	Jumper Group W6 W6-1	W6-0
0	IN	IN
1	IN	OUT
2	OUT	IN
3 Reserved	OUT	OUT

3.4.3 Bus Arbitration Modes

The following bus arbitration mode options are placed in order of increasing throughput and decreasing bus availability. The bus, acquired on the basis of availability, is always released at the end of burst transfer. Maximum burst length is one full sector per bus grant.

- **Single-Transfer:** Control of the Multibus is acquired before each data transfer and released immediately after. This minimizes controller time on the bus, but compromises maximum throughput capability.
- **Yield to Any Request:** The bus is released for any request, regardless of priority, through use of the CBRQ signal, or when the transfer of a block of data is completed. This allows maximum throughput capability only when other bus masters do not want to use the bus.
- **Yield to Higher Priority:** The bus is released only for higher priority requests, or when the transfer of a block of data is completed. This allows maximum throughput capability only when higher priority bus masters do not want to use the bus.
- **Override:** Higher priority bus master requests are overridden. The bus is released only at the end of data transfer. This guarantees maximum throughput performance.

3.4.4 Drive Jumpering

Information concerning jumper operations on the disk or tape drive controller cards is contained in Appendix A. All drives must be jumpered to ensure proper operation, and terminators **MUST** be installed in the last Winchester and last floppy disk drive connected to the DSD Controller. Drive mapping tables are provided for the following type drives:

- Winchester: ST412
- Floppy: SA460

3.5 Initial Checkout and Acceptance Tests

Two LEDs, at board positions A1 and A3 (upper left corner), respond according to board option settings and error condition. LED CR2 (RDY) indicates whether the board is ready to accept a new command (ON), or is busy (OFF). LED CR1 (ERR) is active when an error is detected. These indicators, after a reset condition, indicate if the board is performing properly. Normal indicator sequence is shown in Table 3-5.

Table 3-5. Indicator Sequence

Sequence	Power	CR1 (ERR)	CR2 (RDY)	Remarks
During a Reset, Multibus INIT/ or Power Up:	ON	ON X	ON X	Good Bad Board
After Reset: (During Self-Test)	ON	OFF ON	ON ON	Good Self-Test Failure
While Running:	ON	OFF OFF ON Blinking	ON OFF OFF OFF	Ready Busy Not Valid Error Code

When self-test is complete, CR2 (RDY) will be ON. If CR1 (ERR) is OFF, self-test was successful and the board is ready to receive a new command. If CR1 (ERR) is blinking on and off, a recognized error is indicated. Refer to Chapter 6 for fault analysis procedures.

3.5.1 Test and Verification

Up to this point, no other Multibus cards have been required, only power. The user may further verify system operation using off-line diagnostics to check that all peripherals are operational. These tests are selected using jumper W6, refer to Section 6 for information on tests and jumper reconfiguration.

4 PROGRAMMING

4.1 Introduction

This chapter describes the programming conventions that must be followed to initiate and monitor the transfer of data between the host memory and a disk drive. Included are discussions of disk organization and track formats, host/controller communications, command descriptions, and error processing.

4.2 Winchester Disk Organization

In the following discussion, a head is assumed to be associated with a single disk surface. Each surface can have up to 4096 tracks (circular data paths numbered 0 through 4095). The set of tracks on multiple recording surfaces at a given head position is referred to as a cylinder (See Figure 4-1). A drive that has 4096 tracks per surface also has 4096 cylinders.

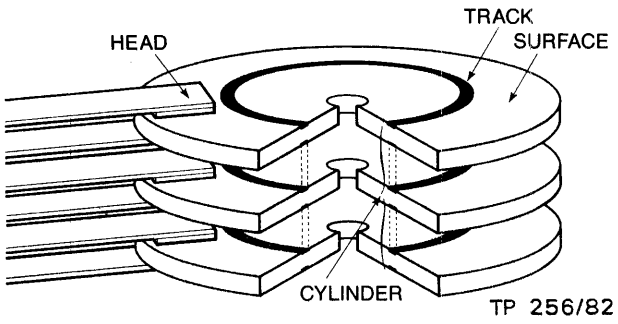


Figure 4-1. Winchester Disk Organization

Each track is divided into equal sized sectors. Each sector includes a sector identification block with error checking information and a data block with error checking information. The controller allows the user to select the size of the data block. The size of the data block determines the maximum number of sectors permitted per track (Refer to Chapter 2).

The controller generates the format of the sector identification block and the error checking fields of each sector of the disk, one track at a time.

4.3 Floppy Disk Organization

The floppy disk drives use standard IBM single- or double-sided media. The formats supported are single-density (128 to 1024 byte sectors), and double-density (256 to 1024 byte sectors).

4.4 Streaming Tape Organization

Data are recorded on this drive in 512 byte blocks. The track selection is transparent to the host, and is accomplished by the internal controller unit.

4.5 Issuing Commands and Receiving Status

The main channel of communication is the memory-based tables. The protocol for issuing commands and receiving status is simple, straight-forward, and essentially constant for all commands. Put controller into reset condition, set up the WUB, CCB, and CIB as required, issue clear and start commands, and wait for not busy. For any subsequent command: set up the CCB, CIB, and IOPB for command, issue start command and wait for interrupt or poll status semaphore. These steps are detailed as follows:

A **Put Controller Into Reset Condition:** Issuing a programmed I/O reset command clears pending interrrupts and applies a hardware reset to the controller hardware. All drives are deselected. Disk writes in process are terminated. Floppy heads are unloaded.

B **Set WUB, CCB, and CIB as Required:** The wake-up block is set up, pointing to the CCB. The channel control block is set up, pointing to the CIB and finally, the controller invocation block is set up. The status semaphore byte in the CIB is cleared by the host to 00H. The busy flag in the CCB is set by the host to FFH.

C **Issue Clear and Start Commands:** Issuing a programmed I/O clear removes the hardware reset and allows the controller to recognize the start command. The first programmed I/O start command is treated in a special way when the controller has been reset. Instead of attempting to fetch an IOPB and execute a command, the controller examines the jumper settings to determine the multibus memory address of the WUB. It chains from the WUB to the CCB and CIB internally, saving the addresses of the latter blocks. It then clears the busy flag in the CCB without issuing status.

D **Wait for Not Busy:** While the controller is collecting its table addresses, the host CPU must refrain from issuing further commands. When the busy flag in the CCB has been cleared, the controller is ready to receive commands. The first commands issued must be to initialize the various disk drives in the system.

E **Set Up IOPB for Initialize Command:** The first commands issued must be to initialize disk drives in the system. Refer to paragraph 4.7.1 for setting up the IOPB for Initialize Command. Each system disk drive requires a separate command and Winchester drives are to be initialized first with floppy drives afterward.

F **Issue Start Command:** A programmed I/O start command is issued once the proper table entries have been set. This causes the controller to fetch the table contents and begin executing the command.

G **Wait for Interrupt, or Poll Status Semaphore:** Status will be posted when the controller has finished execution of a command, when a seek completes, or when a disk drive becomes ready. The host CPU then examines the status to determine if an error has occurred and to decide what command to issue next.

When the controller has status information to pass to the host, it examines the status semaphore byte in the CIB. If it is zero, the controller assumes that previous status information has been accepted by the host. It writes the new status to the operation status byte in the CIB and sets the semaphore to non-zero. An interrupt is generated, if enabled.

The host follows the reverse protocol. When the status semaphore is non-zero the host assumes the operation status byte contains new information. It fetches that information, as required, and clears the status semaphore telling the controller the status has been received. Any interrupt must be cleared by a programmed I/O clear command. Bits in the operation status byte may be decoded to determine the status type and whether an error has occurred.

H **Set Up IOPB for Read Data Command:** Refer to paragraph 4.7.5 and set up IOPB for Read Data Command. Set the requested transfer count for one or two sectors. Successful completion of this command will confirm proper operation of the controller. Poll status semaphore as outlined in Step G.

I **Set Up CCB, CIB, and IOPB for Command:** An IOPB is set up for command to be executed next. The CIB must point to the IOPB. Busy is set (FFH) in the CCB by the host.

4.6 Host/Controller Communications

The controller provides a sensible, straightforward means of communication with the host computer. The host initiates controller activity through a single I/O port addressed via the Multibus interface. Once initiated, the controller handles all communication with the host CPU and between host memory and disk drives. Controller activity is divided into three areas for discussion: I/O commands, controller generated interrupts, and memory-based disk operations.

4.6.1 Input/Output Commands

Communication with the controller is based upon Multibus memory-based tables. The programmed I/O interface is limited to that required for overall control functions. The controller responds to a single I/O address, jumper selectable by the user. This address may be 8- or 16-bits, as applicable for the CPU and application. Only I/O write operations are recognized. When an I/O write is detected by the controller, the two least significant bits determine which of three possible hardware functions will be performed.

Command	Function
00H	Clear Interrupt/Remove Reset
01H	Start Operation
02H	Reset Controller

- **Clear (00H):** Causes controller-to-host interrupts to be reset. Clears the controller reset condition following reset controller command, assertion of the Multibus INIT/ signal, or application of power. **Note that after reset is removed by a clear function, a drive initialization command is required before further disk access.**
- **Start (01H):** Causes the controller to fetch the address of its memory-based control tables. On completion, no status information is returned, but the busy flag is cleared. Any subsequent start command causes the controller to fetch the I/O parameter block (IOPB) and begin executing the specified function command. Commands and content of the IOPB are described in this section.
- **Reset (02H):** Causes the controller hardware to reset immediately. Current disk operations are terminated, buffer transfers in progress are halted, and no status information is returned.

NOTE: The programmed I/O start command is used in two separate and distinct ways. First, after a controller reset, the I/O start command causes controller to fetch the address of WUB, CCB, and CIB to initiate host to controller communication. Once the communication path is established, and until controller is again reset, subsequent I/O start commands begin execution of functions set up by user in the IOPB.

4.6.2 Interrupts

The controller modules generate interrupts to alert the host of significant changes in disk system status by assertion of one of eight Multibus interrupt lines (INT0/ through INT7/). These lines are user selectable by a wire-wrapped jumper (W10) on the controller board. Once an interrupt is asserted, it can be removed by a clear I/O command from the host to the controller, by a power-on reset, or by assertion of the Multibus INIT/ signal.

Three events that cause the controller to assert an interrupt are completion of a command, completion of a seek, or a media change.

Note

Command completion interrupt may be disabled by controlling the appropriate bit in the modifier word of the I/O parameter block (Refer to paragraph 4.5.8). Interrupts generated at completion of seek or media change may NOT be disabled.

4.6.3 Memory-Based Control Paths

The command and status path between the controller and the host consists of four tables stored in Multibus memory. These tables are used to pass required command information for disk access, as well as status information returned by the controller.

- WUB: Wake-Up Block
- CCB: Channel Control Block
- CIB: Controller Invocation Block
- IOPB: Input/Output Parameter Block

Figure 4-3 shows a fifth block, the data buffer, associated with most controller operations where data is read, written, or used for functions such as disk formatting. The data buffer block is linked into the chain of control blocks.

4.6.4 Address Representation

Prior to a discussion of the individual control blocks shown in Figure 4-3, we will review the details of the addressing scheme used in these blocks. Addresses may be represented in two ways. Segmented address representation is compatible with iSBC operation, but is limited to 20 bits. To achieve full 24-bit address compatibility with processors such as the MC 68000, a linear addressing scheme can be specified by the wake-up block when the controller is reset. A comparison of the two schemes is shown in Table 4-1.

Table 4-1. Addressing

Segmented		Linear	
Offset	=3456H	First Word	=3456H
Segment	=0012H	Second Word	=0012H
Segment X16 (Shift Left)	=00120H	Multibus Addr	=00123456H
Plus Offset	=+3456H		
Multibus Addr	=03576H		

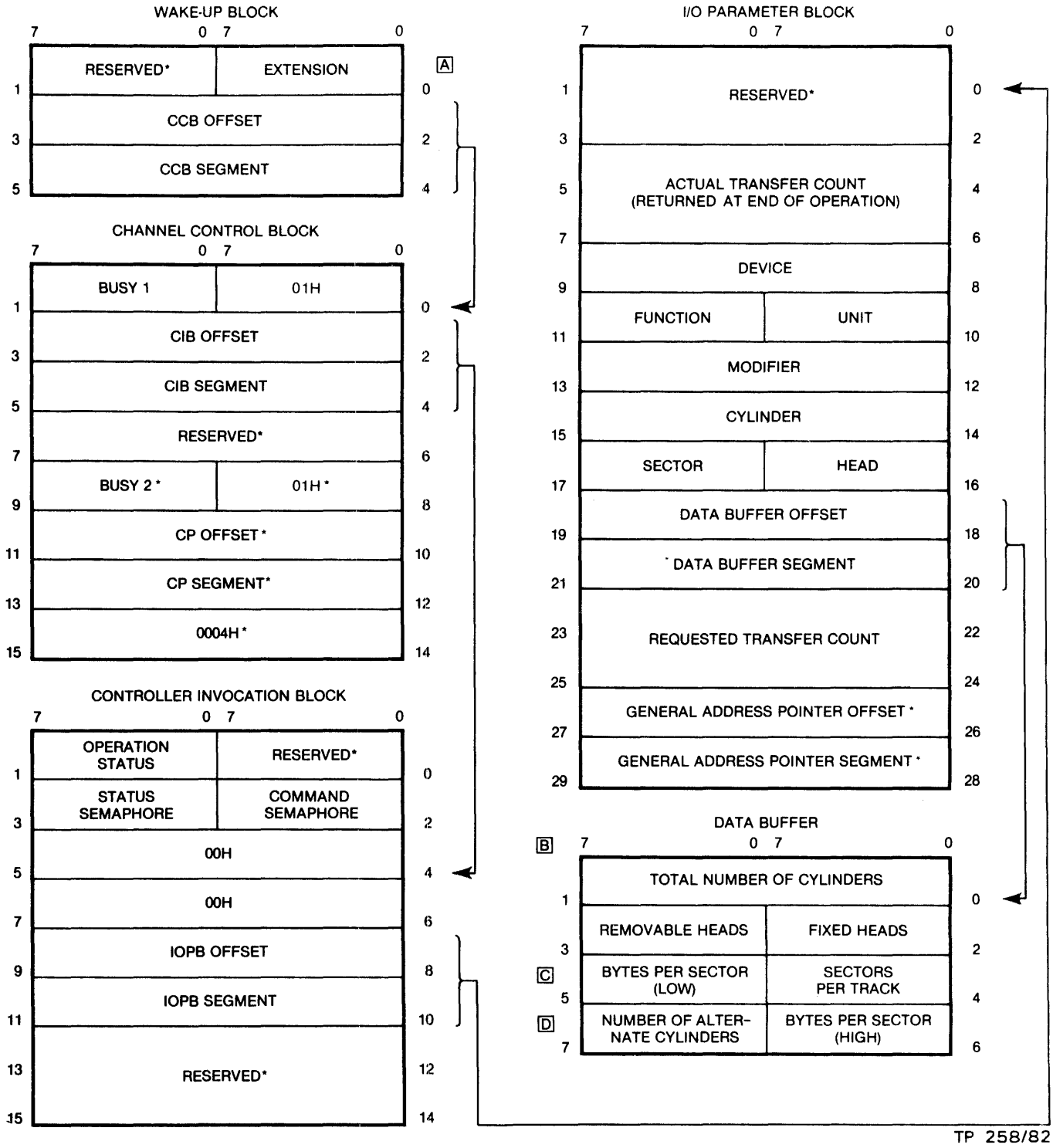
Segmented addressing is the representation selected by most users. It is the scheme shown in tables throughout the remainder of this manual. Those selecting 24-bit linear addressing have to interpret the tables accordingly.

Segmented addressing permits specifying any Multibus address as a truncated representation of the address of a block of memory, called a segment, and a relative address within that block called an offset. Segment addresses consist of two 16-bit numbers, the segment and the offset (See Figure 4-3). In all cases where segmented addressing is used, these two numbers are stored in memory in the same format. To arrive at the 20-bit Multibus address that corresponds to a particular segmented address, the controller multiplies the 16-bit segment by 16 (shifts it left four bits), and adds the 16-bit offset to the result. This is shown in Table 4-1.

Any Multibus address may be represented in a variety of ways. For example, 44444H may be the result of a segment of 4440H and an offset of 0044H, or a segment of 4000H and an offset of 4444H.

4.6.5 Wake-Up Block

The wake-up block (WUB), the first block in the chain, is used to link the controller to the rest of the chain. It consists of six bytes as



* Set to all zeros.

A. Wake-up address switches must point to this byte.

B. Example shows data buffer for format command.

C. Bytes 5 and 6 are a word, 5 is the low byte and 6 is the high byte.

D. This byte defines the bit encoding scheme when initializing a floppy drive (00H for FM, single density, and 01H for MFM, double density).

NOTE

The MC68000 looks at the bytes in reverse. That is:

1	High Byte	Low Byte	0 (Multibus)
0	Low Byte	High Byte	1 (MC68000)

Figure 4-3. Chain of Communication Blocks

shown in Figure 4-4. The address of the WUB is defined by the same controller board jumpers that define the programmed I/O address (Refer to paragraph 3.4.1). The value represented by these jumpers is multiplied by 16 to obtain the 20-bit Multibus address of the WUB. On recognition of the first I/O start command from the host, the controller goes to this address, fetches the WUB, and internally saves the CCB address. This action is taken only after a reset; the WUB need not be preserved.

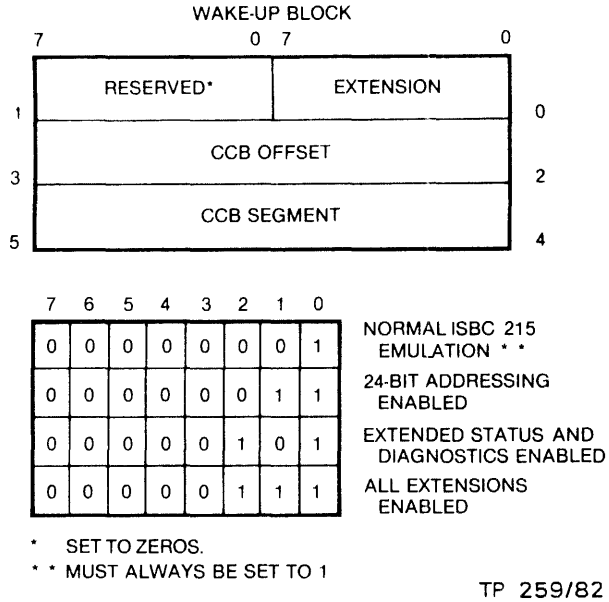


Figure 4-4. Wake-Up Block

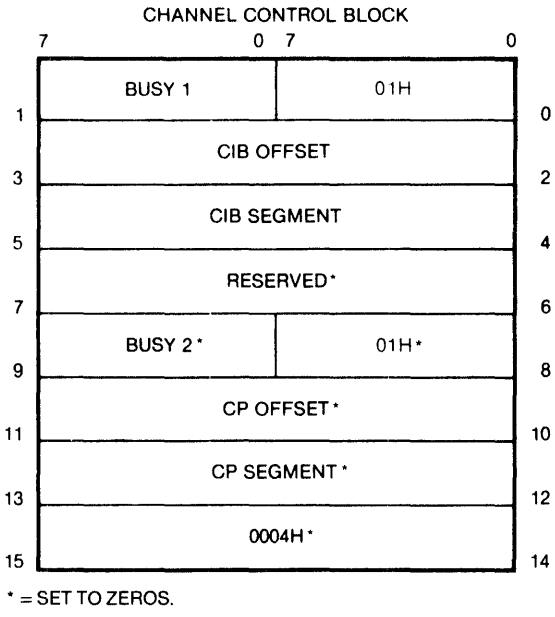
The first byte in the WUB (extension byte) indicates if any command extensions are to be recognized. Figure 4-4 shows the values of this byte for various extensions beyond normal iSBC 215 operation. When this byte is 01H (normal iSBC 215 emulation), no extensions are enabled. When the value of this byte is is 07H, all extensions are enabled. Refer to paragraph 4.6.4 for discussion of 24-bit addressing and all of paragraph 4.7.2 for discussion of extended status and on-line diagnostics.

The second byte of the WUB is reserved. The remaining four bytes contain the address of the CCB, the next block in the chain.

4.6.6 Channel Control Block

The channel control block (CCB), the next block in the control chain, requires 16 bytes as shown in Figure 4-5. The last ten bytes in this block are not read or written. They are shown for compatibility with iSBC operation only. Of the first six bytes, the first byte must contain a value of 01H. If this byte does not contain a value of 01H when checked by the controller, processing ceases with no status returned, and an error is indicated by LED CR1 (ERR).

The second byte is the busy flag. It informs the host whether the controller is busy (FFH), or idle (00H). The busy flag is posted when the controller is busy processing a command, and cleared after the command is completed. This information is used in handshaking and status commands between the host and the controller. The next four bytes contain the offset and segment (address) of the CIB, the next block in the chain.



Byte(s)	Function
0	01H Always
1	Busy 1 Flag. 00H =Idle, FFH =Busy
2-5	CIB address
6-15	Not read or written by DSD Controller

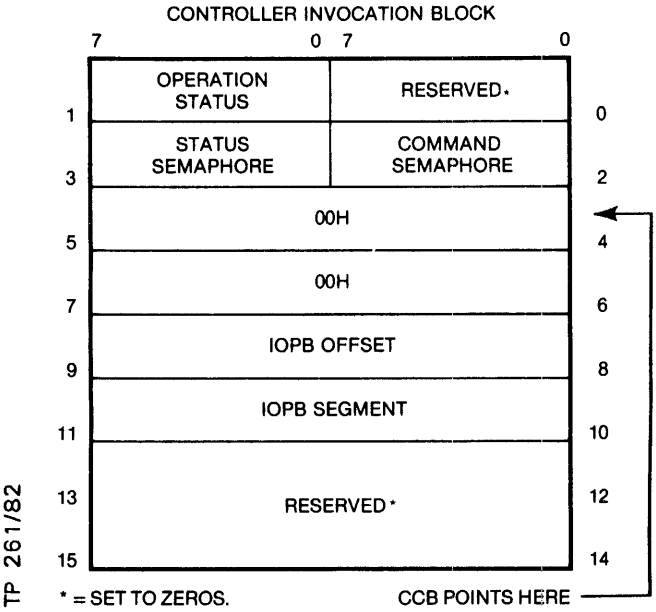
Figure 4-5. Channel Control Block

Note

The addresses of the CCB and CIB are stored within the controller while processing the first I/O start command after a reset. These locations MUST NOT be changed without a controller reset and initialization sequence.

4.6.7 Controller Invocation Block

The DSD Controller uses the controller invocation block (CIB) to post status to the host. The functions of each byte are shown in Figure 4-6.



Byte(s)	Function
0	**Reserved.** Set to zeros.
1	**Operation Status.** This byte contains the latest controller status, interlocked by byte 3. The status is encoded on a bit-by-bit basis as shown:

7	6	5	4	3	2	1	0
E	H	U		D	M	S	O

E =Summary Error
H =Hard Error
U =Unit ID
D =Drive Type (0 =Winchester, 1 =Floppy)
M =Media Change Detected
S =Seek Complete
O =Operation Complete

2	**Command Semaphore.** Controller does not use this block. Provided as a multiprocessor interlock.
3	**Status Semaphore.** Controller posts status only when this byte is 00H; when new status has been posted, controller sets byte to FFH. When host has read status, it sets this byte to 00H.
4-7	**Set to All Zeros.**
8-11	**Segmented Address for IOPB.**
12-15	**Reserved.** Set to zeros.

Figure 4-6. Controller Invocation Block

4.6.8 Input/Output Parameter Block

The Input/Output Parameter Block (IOPB) is the main channel for communication between the controller and the host CPU. Information required by the controller for each command is stored in this block. The IOPB and its content is shown in Figure 4-7.

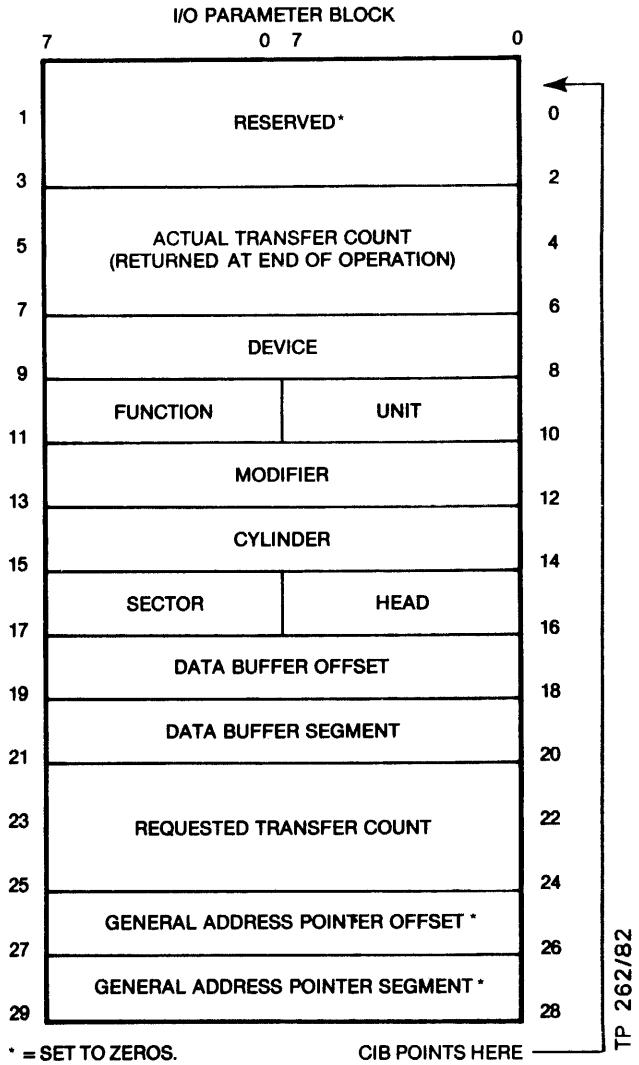


Figure 4-7. Input/Output Parameter Block

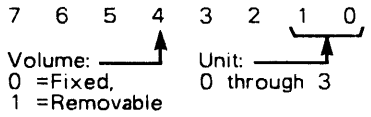
The first four bytes in Figure 4-7 are reserved for future expansion. These fields should always be set to zero by the host driver to insure continued compatibility. This is true for all reserved fields in the commands that follow.

- **Actual Transfer Count:** This four-byte field specifies the number of bytes transferred in the process of executing a command. It is treated as a 32-bit positive number. Byte four of the IOPB contains the least significant byte, byte seven contains the most significant. For normal disk data transfers without error, the actual transfer count will equal the requested transfer count. A count of six is indicated following a track formatting function and a count of 12 after a status transfer function.

- **Device:** This word specifies the device type to be accessed:

  0000H =Winchester Drive (iSBC 215 equivalent)
  0001H =Floppy Disk Drive (iSBX 218 equivalent)
  0010H =Streaming Tape Drive

- **Function:** This single-byte field specifies the operation to be performed; read, write, format, etc. The byte value determines how some other fields in the IOPB are interpreted. These are described in detail in paragraph 4.7.
- **Unit:** This field specifies which disk drive, of the drive types selected by the device field, is to be accessed. Bits 2, 3, 5, 6, and 7 are reserved.



- **Modifier:** This word is treated by the controller as a field of single-bit control flags. The bits, independent of each other, are assigned the following functions:

Bit(s)	Function (Enabled when set to 1)
8-15	Specifies the diagnostic test to be executed when the operation specified in the function byte is the diagnostic command (Function =0FH). For all other commands, this byte must be set to zero.
3-7	Reserved.
2	Allows read data, read to buffer and verify, write data, and write buffer data functions to be modified to read or write deleted data. 0 =normal data; 1 =deleted data.
1	Inhibits automatic retries for error recovery when set to 1.
0	Suppresses interrupt on command completion when set to 1.

- **Cylinder:** This word specifies the starting cylinder (track) number where a read, write, or format command begins. The range of acceptable values depends upon the drive type and drive parameters specified at initialization. The smallest cylinder number is always 0. An illegal value causes the selected drive head to go to cylinder 0, and an error will be returned.
- **Sector:** This byte is functionally similar to the cylinder word. It specifies the starting sector number for disk read or write operations. The range of legal values depends on the drive type and format (number of sectors per track). The smallest sector number for a floppy disk is always 1, not 0 as for cylinder and head numbers. The smallest sector number for a Winchester drive is 0.
- **Head:** This byte is also similar to the cylinder word in function. It specifies the starting head number for disk read or write operations. The range of legal values depends upon drive type. Like cylinder numbers, head numbers start at zero. For single-sided floppy disks the head number is always 0. For double-sided disks the only values allowed are 0 and 1.
- **Data Buffer Address:** This four-byte field contains the segmented address of the data buffer. For normal read or write operations, this is the address of the multibus memory buffer where data are stored or fetched. For some commands, this is the address of additional control information.
- **Requested Transfer Count:** This four-byte field, set by the host CPU, specifies the number of bytes to be transferred in the process of executing a command. This field has the same format as the actual transfer count and is treated as a 32-bit positive number.
- **General Address Pointer Address:** This four-byte field is not used by the controller.

4.7 Controller Commands

The controller presents the programmer with a set of commands designed to take full advantage of the capabilities of the supported disk drives. These include normal read and write commands, commands to tailor the disk system for different applications, and a complete set of diagnostics. These commands are invoked by setting up the described functions and executing a programmed I/O start command to the controller.

The following paragraphs detail the IOPB and data buffer requirements for each command executed by the controller. The command to be executed is determined by the function field in the IOPB.

Hex Value	Function
00H	Initialize
01H	Transfer Status
02H	Format
03H	Read Sector ID
04H	Read Data
05H	Read Buffer and Verify
06H	Write Data
07H	Write Buffer Data
08H	Initiate Track Seek
09H-0DH	Reserved
0EH	Buffer I/O
0FH	Diagnostic
80H	Reset Tape Drive
81H	Disk Image Backup
82H	Disk Image Restore
83H	Read Tape Status
84H	Retension Tape Cartridge

The following description of each function includes a diagram of the IOPB showing those fields (shaded blocks) that must be set by the host CPU before the command is executed.

4.7.1 Initialize (00H)

The initialize function (See Figure 4-8) is used to transfer drive related parameters to the controller and to seek drive heads to cylinder zero to synchronize position. These parameters include the number of cylinders, heads, bytes per sector, etc.

The information passed to the controller is contained in an extension to the IOPB. This eight-byte extension is addressed by the data buffer offset and segment stored in the IOPB.

Information in the IOPB extension is used by the controller for all disk related commands. The initialize function command should be issued for each drive in the system following any hardware reset caused by power-on, Multibus INIT/, or a programmed I/O reset command. Commands issued for drives not initialized will not be executed and an error will be returned. The fields in the IOPB extension block have the following meaning:

- **Number of Cylinders:** This word specifies the number of cylinders available on a disk drive. Refer to the appropriate drive manual for the proper word value for drives being used. If this word is set to zero, the initialize function command removes the specified drive from use as if an initialize command had not been issued since the last reset.
- **Fixed Heads:** This byte specifies the number of fixed heads on the drive. For example, an ST412 Winchester drive has four.
- **Removable Heads:** This byte specifies the number of heads on a floppy disk drive. For example, a single-sided floppy drive has one. A double-sided drive has two.
- **Sectors per Track:** This byte specifies the number of sectors per track for the drive specified. Refer to Section 2 of this manual for the proper byte value.
- **Bytes per Sector:** These two bytes form a word specifying the number of data bytes in a disk sector. This sector length must match the format for the disk, and must be 128, 256, 512, or 1024.
- **Number of Alternate Cylinders or Encoding:** For a Winchester drive, this byte specifies the number of cylinders reserved as alternates for defective tracks. For a floppy drive, this byte specifies the data encoding scheme to be used; 00H for FM, single-density and 01H for MFM, double-density.

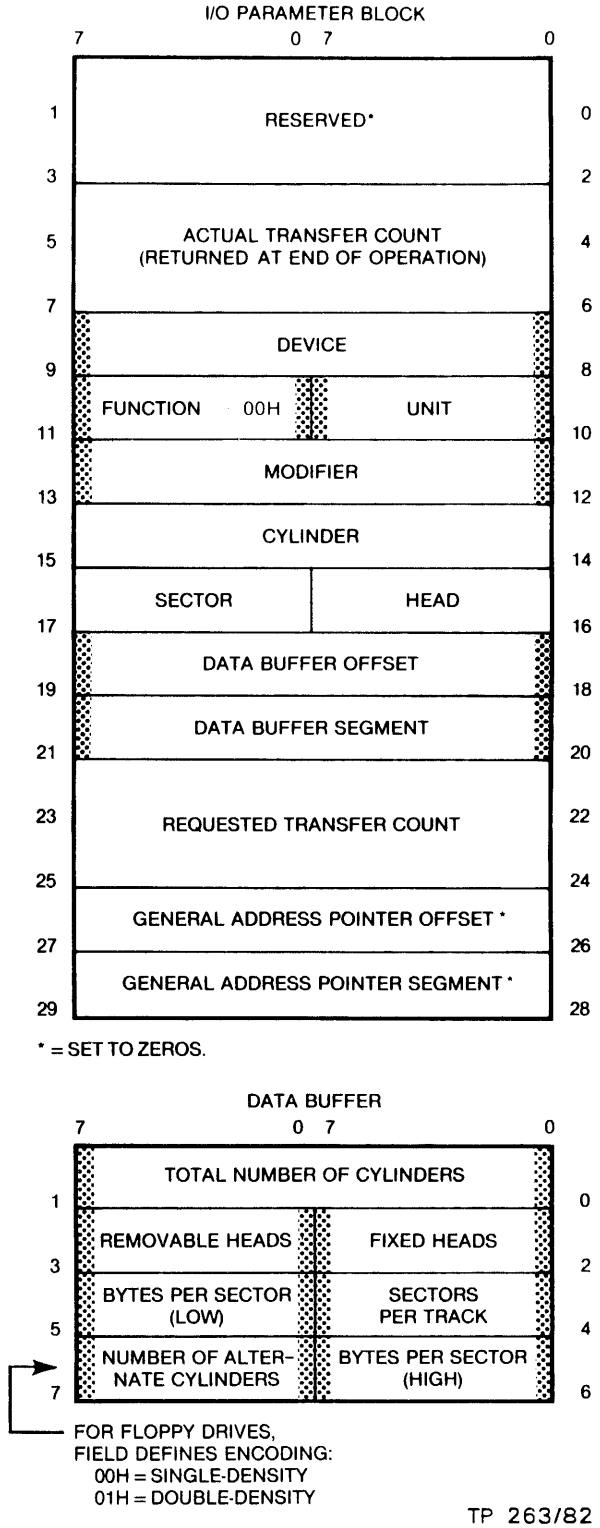


Figure 4-8. Initialize Function

Figure 4-9 illustrates the IOPB set up for initialization of an ST412-type Winchester and an SA460-type floppy drive. The addresses used in the figure are for illustrative purposes only and not intended for actual use. Table 4-2 defines the values of each byte or word in the IOPB and data buffer extension shown in Figure 4-9.

The shaded blocks indicate required, significant values (Hex) for the type of drive. The information contained in unshaded blocks reflects suggested values only.

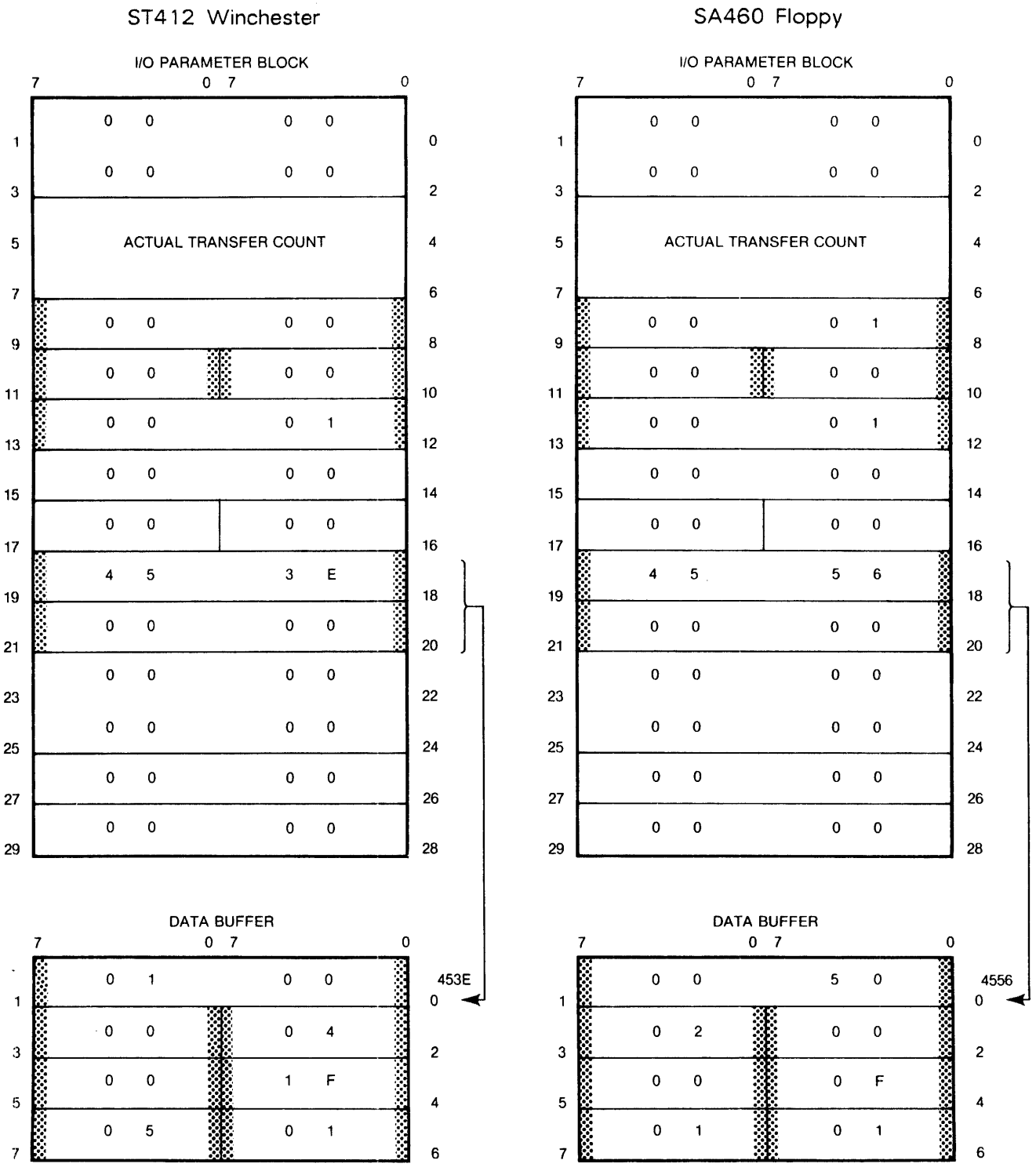


Figure 4-9. Initialization Examples

TP 264/82

Table 4-2. Byte Values Example (IOPB)

Byte(s)	Meaning	Enter Value (Hex)
Winchester IOPB Block:		
0-3	Reserved	All Zeros
4-7	Actual Transfer Count	N/A
8,9	Device Code	0000H= Winchester
10	Unit Number	00H= Drive 0
11	Function	00H= Initialize
12,13	Modifier	0001H= CMD Complete Interrupt Suppressed
14,15	Cylinder	0000H= Not Used
16	Head	00H= Not Used
17	Sector	00H= Not Used
18,19	Data Buffer Offset	453EH= Example Only
20,21	Data Buffer Segment	0000H= Example Only
22-25	Requested Transfer Count	0000H= None
26,27	General Address Pointer Offset	0000H= None
28,29	General Address Pointer Segment	0000H= None
Winchester Data Buffer Block:		
0,1	Number of Cylinders	0100H= 256
2	Fixed Heads	04H= Four Heads
3	Removable Heads	00H= None
4	Sectors per Track	1FH= 31
5,6	Bytes per Sector	0100H= 256
7	Number of Alternate Cylinders	05H= Five Assigned (2 percent of total)
Floppy IOPB Block:		
8,9	Device Code	0001H= Floppy
10	Unit Number	00H= Drive 0
11	Function	00H= Initialize
18,19	Data Buffer Offset	4556H= Example Only
20,21	Data Buffer Segment	0000H= Example Only
Floppy Data Buffer Block:		
0,1	Number of Cylinders	0050H= 80 Tracks
2	Fixed Heads	00H= None
3	Removable Heads	02H= Two Heads
4	Sectors per Track	0FH= 15
5,6	Bytes per Sector	0100H= 256
7	Encoding Scheme	01H= MFM Double-Density

For the SA460 floppy drive, only the shaded blocks need be described. Unshaded blocks are the same as for a Winchester drive.

4.7.2 Transfer Status (01H)

This function command reads the content of the error status buffer from the controller's internal memory. See Figure 4-10 for set up of the IOPB for this function. The command is used to access information about an error reported via the summary error bit in the operation status byte of the CIB.

Executing the command causes the current content of the error status buffer to be written to the data buffer specified in the data buffer offset and segment fields of the IOPB. The contents of the error status buffer are cleared during the execution of each new command, except transfer status. Therefore, if error information is required, the transfer status command should be issued immediately following the erroneous command execution.

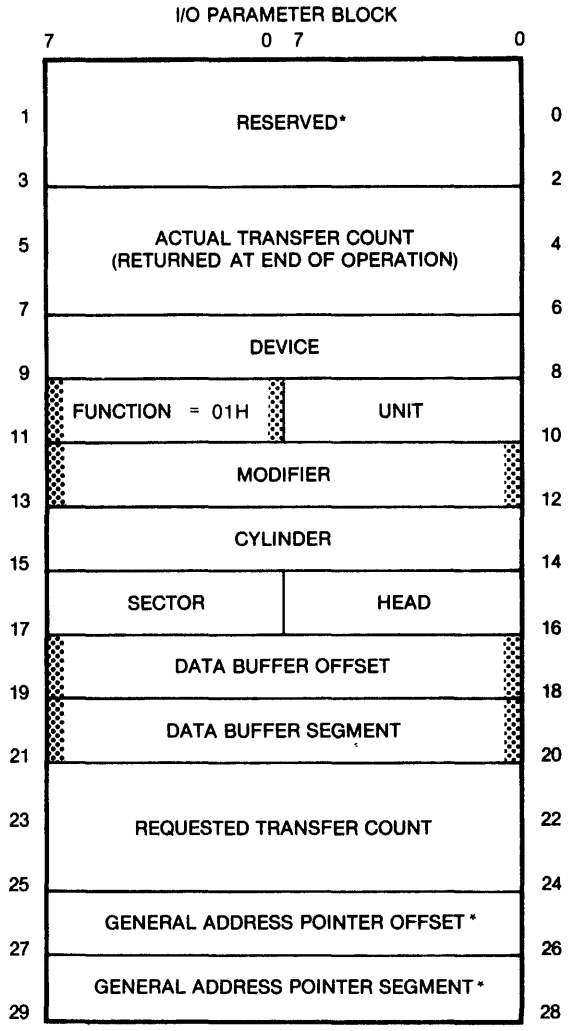


Figure 4-10. Transfer Status Function

4.7.2.1 Error Status Buffer

The data returned by the error status buffer consists of 13 bytes, if bit 2 (read extended status enabled) in the extension byte of the WUB is set, and 12 bytes otherwise. Table 4-3 defines the content of the error status buffer. Bytes 0, 1, and 2 of the status buffer contain the hard and soft error bits that reflect error status during normal iSBC 215 operation. These error bits are defined in Table 4-4.

Table 4-3. Error Status Buffer

Byte(s)	Function
0,1	Hard Error Status (See Table 4-4)
2	Soft Error Status (See Table 4-4)
3,4	Desired Cylinder
5	Desired Head and Volume
6	Desired Sector
7,8	Actual Cylinder and Flags (Byte 8, Bits 4-7)
9	Actual Head and Volume
10	Actual Sector
11	Number of Retries Attempted
12	Extended Error Status, if Enabled (See Table 4-5)

Table 4-4. Error Status Bit Definition

Bit(s)	Definition
Byte 0:	
0-2	**Reserved** for future use.
3	**RAM Error**: Controller RAM error detected.
4	**ROM Error**: Controller ROM error detected.
5	**Seek in Progress**: Indicates a seek was already in progress when another disk operation was requested.
6	**Illegal Format Type**: Both alternate track and defective alternate tracks set indicating, an illegal attempt to create an alternate track for a defective alternate track or, an attempt to access an unassigned alternate track.
7	**End of Media**: End of media encountered before requested transfer count expired.
Byte 1:	
8	**Illegal Sector Size**: Sector size read from the sector ID field conflicts with sector size specified during initialization.
9	**Diagnostic Fault**: Micro-diagnostic fault indicated.
A	**No Index**: Controller did not detect index pulse.
B	**Invalid Command**: Invalid function code detected.
C	**Sector Not Found**: Desired sector could not be found on selected track.
D	**Invalid Address**: Invalid address requested.
E	**Selected Unit Not Ready**: Selected unit is not ready, or not responding to unit connect request.
F	**Write Protection Fault**: Attempt made to write to a write protected unit.
Byte 2:	
0-2	**Reserved** for future use.
3	**Data Field ECC Error**: Error detected in data field of a sector. If bit 6 in CIB status byte (byte 1) is set, error is hard and uncorrectable. If bit 6 is not set, error is soft and correctable.
4	**ID Field ECC Error**: Error detected in ID field of a sector. If bit 6 of CIB status byte is set, error is soft and correctable.
5	**Drive Fault**: Hardware fault detected in selected drive unit. Fault characterized by read/write, positioner, power, or speed faults.
6	**Cylinder Address Miscompare**: ID field contains a cylinder address different from that expected.
7	**Seek Error**: Hardware seek error detected.

4.7.2.2 Extended Error Status

The extended error status is enabled by setting bit 2 in the extension byte of the wake-up block. When enabled, the transfer status command will write, in byte 12 of the error status buffer, a hexadecimal value that reflects the extended error status. Table 4-5 defines the error codes reported via the extended error status byte. These codes are also reported by the blinking patterns of CR1 (ERR) indicator.

A comparison of Tables 4-4 and 4-5 shows that all the error codes in Table 4-4 are also reported by the extended error status byte. Only one error at a time can be posted in either bytes 0, 1, and 2 or byte 12 of the error status buffer. Complete error code information is accessed only when read extended status is enabled (bit 2 in extension byte of the WUB).

Table 4-5. Extended Error Status Codes

Hex Code	Definition
11-13	Reserved
14	RAM error
15	ROM error
16	Seek in progress
17	Illegal format type
18	End of media
21	Illegal sector size
22	Diagnostic fault
23	No index
24	Invalid command
25	Sector not found
26	Invalid address
27	Selected unit not ready
28	Write protect
31-33	Reserved
34	Data ECC (or CRC) error
35	ID ECC (or CRC) error
36	Drive fault
37	Cylinder address miscompare
38	Seek error
41	Data field not found
42	Wrong type of data field
43	Index too early (Drive spinning too fast)
44	Index too late (Drive spinning too slow)
45	Read/write controller error
46	Bus time out error
47	No drive exists
51	Tape cartridge not in place
52	Tape cartridge write protected
53	Tape drive not on line
54	Tape unrecoverable data error
55	No data on tape
56	Data miscompare during diagnostic
57	Miscellaneous tape error

4.7.3 Format (02H)

The format function (Figure 4-11) writes sector header information onto a single track (one track per command) of a specified disk drive. These sector ID fields segment the track and allocate space for the data sectors. They contain information, used in subsequent write or read operations, to locate the correct sector data area, to verify the correct cylinder and head have been reached, and that the sector data area allocated matches the sector size to be written or read.

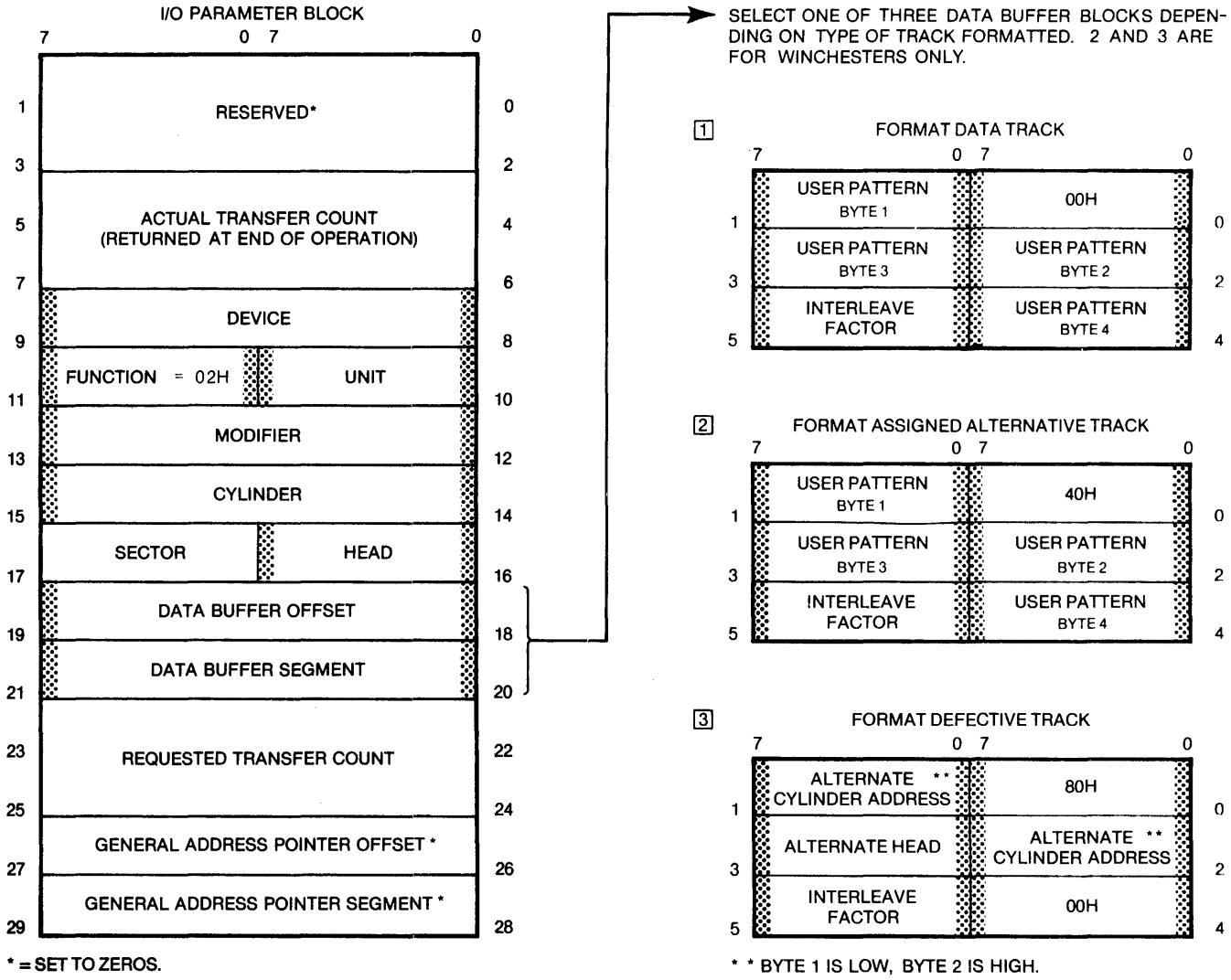


Figure 4-11. Format Function

Information required by the controller to format the track is passed by the host CPU via the data buffer. The data buffer, consisting of six bytes, is addressed by the data buffer offset and segment words in the IOPB.

As shown in Figure 4-11, a track can be designated as a normal data-type track (00H), an assigned alternate track (40H), or as a defective track (80H). Refer to paragraph 4.8.1 for bad track handling. When formatting a floppy disk drive, the first byte in the data buffer **MUST** be 00H.

The user pattern is a four-byte sequence repeated throughout the data field of each sector of the track. The pattern is written to the drive in the order it appears. User pattern one is written first and user pattern four last.

When the track is to be formatted as a defective Winchester track, information in the data buffer is used on subsequent accesses to locate the assigned alternate track where data are to be written. A defective alternate track cannot point to another alternate track.

The interleave factor controls the order in which the sectors appear on a track. An interleave factor of one specifies that sectors are to be written in sequence around the track; Index, Sector 1, Sector 2, etc.

Other values may be used to increase the disk rotational time between sequential sector numbers so the data from each sector may be processed before the next sector on the track comes under the drive read/write head.

The extra disk rotational time may be necessary if the bus is not readily available, or if slow Multibus memories are used.

The interleave factor is the minimum number of sector intervals between the start of one sector and the start of the next sequential sector. Sector 1 is always written immediately after the physical track index.

The following examples assume eight sectors per track; 1024 bytes per sector on a floppy, single-density disk. Refer to paragraph 4.8.1 for alternate and defective track handling.

Factor	Order from Index
1	1 2 3 4 5 6 7 8
2	1 5 2 6 3 7 4 8
3	1 4 7 2 5 8 3 6
4	1 3 5 7 2 4 6 8

4.7.4 Read Sector ID (03H)

The read sector ID function transfers the contents of the next available sector ID field into the data buffer addressed by the data buffer offset and segment in the IOPB (See Figure 4-12). This information may then be used for a number of purposes; verification of cylinder and head selection, sector length determination, rotational access optimization, etc.

Since the command may be used to verify disk position, no implied seek or head selection is performed. The sector ID is read from the last referenced disk track on the drive. The data buffer to be used is addressed by the data buffer offset and segment in the IOPB. The data written to this buffer consists of five bytes.

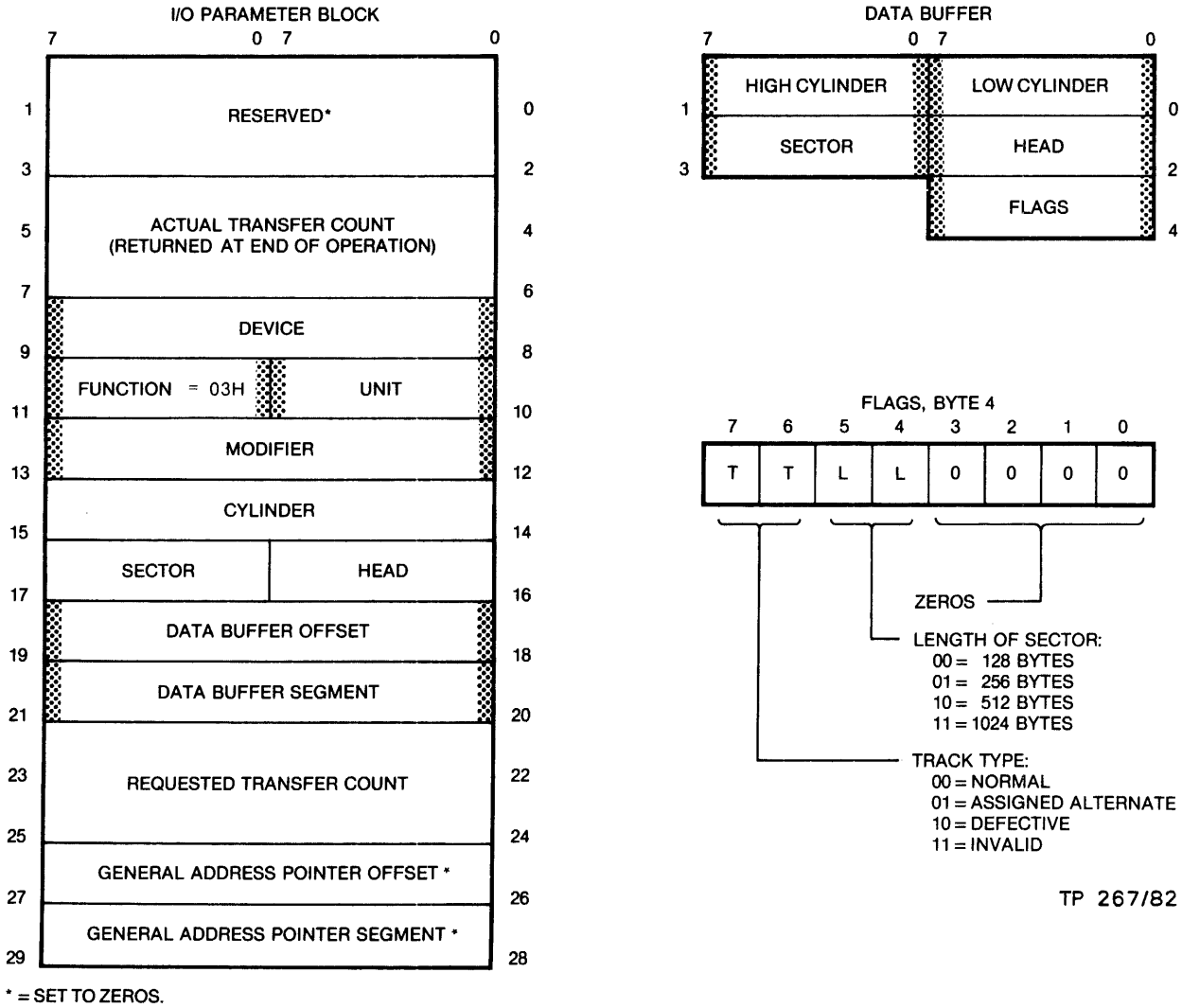


Figure 4-12. Read Sector ID Function

4.7.5 Read Data (04H)

The read data command is one of the two most used commands, write data command is the other. The read data command transfers data from a disk drive into a Multibus memory buffer. The IOPB device and unit fields specify the drive to be accessed. The cylinder, head, and sector fields determine the starting location on the disk (See Figure 4-13). An implied seek is invoked if the current head position is different from that specified.

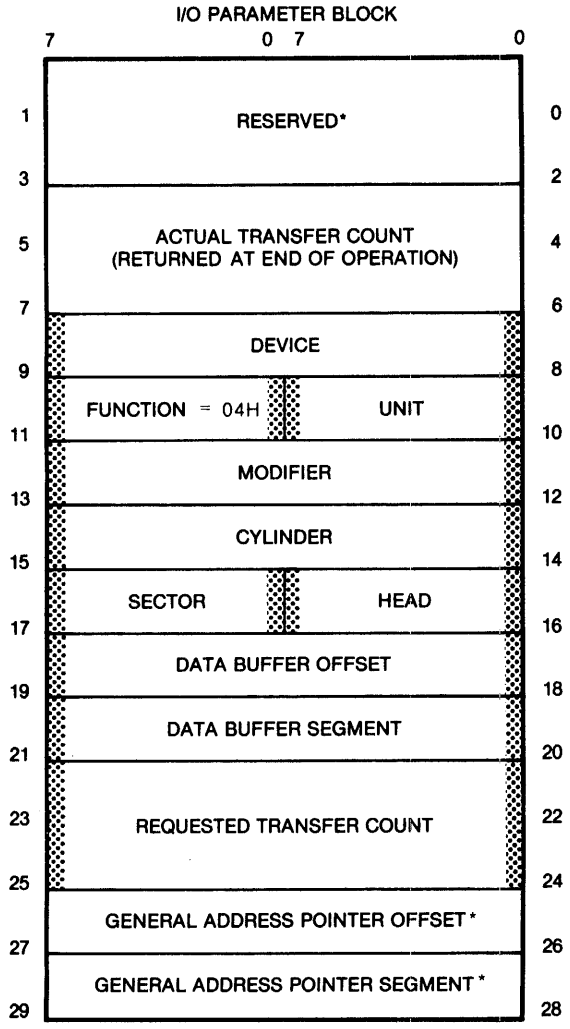


Figure 4-13. Read Data Function

Data are read into the controller buffer one sector at a time and then transferred into the Multibus memory location addressed by the data buffer offset and segment fields of the IOPB. Subsequent bytes are transferred to sequential locations in the buffer until the number of transferred bytes is equal to the requested transfer count field in the IOPB, end of media is reached, or an error occurs.

The last valid sector, head, and track address (not including alternates) from the initialization table defines the end of media. At this point, the actual transfer count field in the IOPB is updated with the number of bytes written to the memory buffer and status is returned.

If the requested transfer count is not exhausted when the last sector on a track has been transferred, the controller automatically continues reading data from sector 1 on the next track by incrementing the head number. If the count is not exhausted when the last sector or the last track of the cylinder has been transferred, the controller automatically seeks the drive to the next sequential cylinder and continues reading at head 0, and the first sector. If the requested transfer count does not specify an integral number of sectors the last sector containing part of the data is read into the on-board buffer in full. Only enough data to exhaust the count is moved to the Multibus buffer.

4.7.6 Read Buffer and Verify (05H)

This command is similar to the read data command except no data are transferred to the Multibus buffer. Typically, this command verifies that certain disk sectors may be read with proper ECC/CRC checks, or to fill the controller on-board buffer for access by subsequent commands such as write buffer data, or buffer I/O.

For data transfer, the 'write-data from controller buffer (07H)' function is required. Read (05H) and then write (07H) must be used alternately because of the 4K limit imposed by the size of the on-board buffer.

Requested transfer counts that are not a multiple of full sectors are rounded up to the nearest full sector count. The requested transfer count should not exceed 4K bytes, or data will be lost, since full sectors are always read into the on-board buffer. If the requested transfer count does exceed 4K bytes, the bytes in exceed of 4K overwrite the data already in the buffer, starting with the first address.

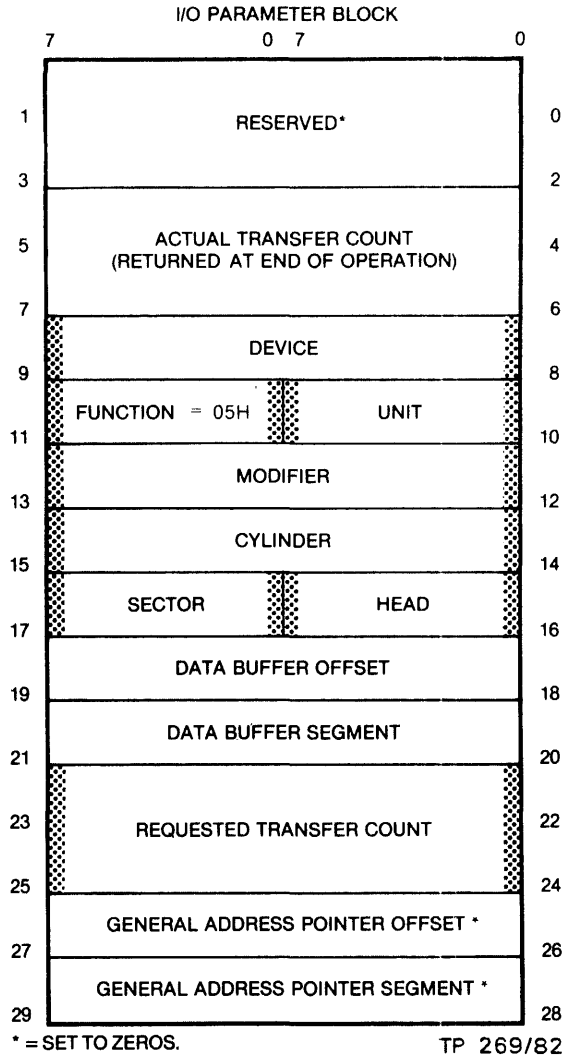


Figure 4-14. Read Buffer and Verify Function

4.7.7 Write Data (06H)

This command, except for direction of data transfer, is functionally similar to the read data command. The write data command transfers data from a Multibus memory buffer to a disk drive (See Figure 4-15). The IOPB device and unit fields specify the drive to be accessed. The cylinder, head, and sector fields determine the starting location.

An implied seek is invoked if the current head position is different from specified. Data are transferred, starting with the first byte in the Multibus memory buffer specified by the data buffer offset and segment fields of the IOPB, into the controller on-board buffer. The first sector is written into the data areas.

Consecutive bytes are transferred from sequential locations in the buffer and are written one sector at a time until the number of bytes transferred equals the requested transfer count, end of media is reached, or an error occurs. The actual transfer count is updated with the number of bytes written on the disk. Each full sector of data is first transferred from the Multibus buffer into the controller on-board buffer. The data are then written onto the disk.

If the requested transfer count is not exhausted when the last sector on a track has been transferred, the controller automatically continues writing data to the first sector on the next track of the cylinder by switching head selection in sequence.

If the count is not exhausted by the time the last sector on the last track of the cylinder has been transferred, the controller automatically seeks the drive to the next sequential cylinder and begins writing at head 0, and the first sector. If the requested transfer count does not specify an integral number of sectors, the last sector written will contain the

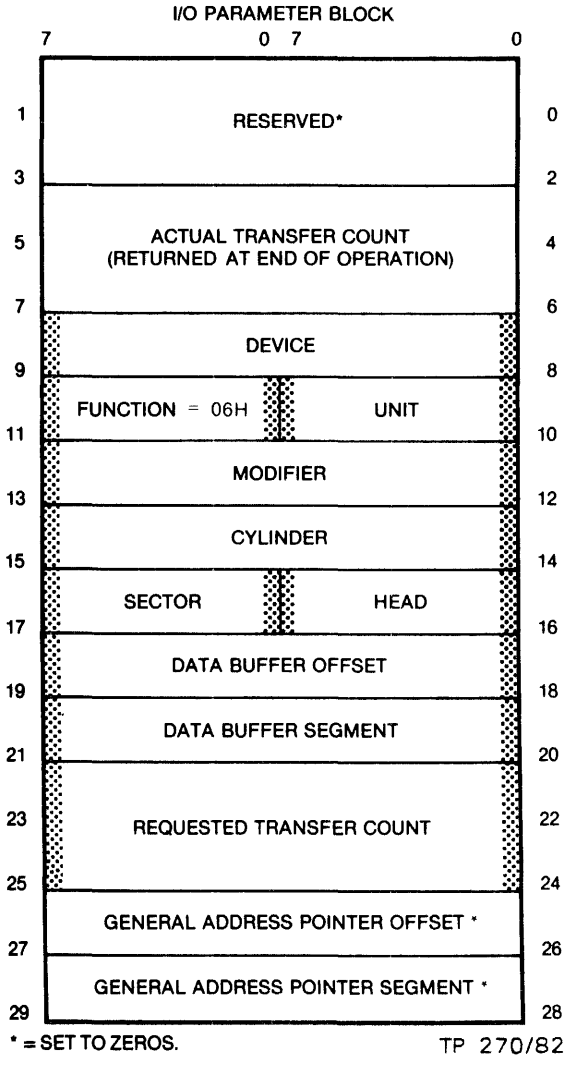


Figure 4-15. Write Data Function

last sector's partial data. The balance of the sector is written with zeros.

4.7.8 Write Buffer Data (07H)

This command is similar to the write data command except no data are transferred from the Multibus buffer. Typically, this command writes the same data pattern to multiple sectors on a disk. If the requested transfer count specified in the IOPB is more than the number of bytes in the first sector specified, the sequential sectors will be written with the same data starting at the first byte in the controller's on-board buffer. If the requested transfer count is not a multiple of the number of bytes in a sector, the last sector written will be written with partial buffer data. The balance of the sector will be written with zeros. For details concerning the IOPB parameters required for this command, refer to the write data command description (See Figure 4-15).

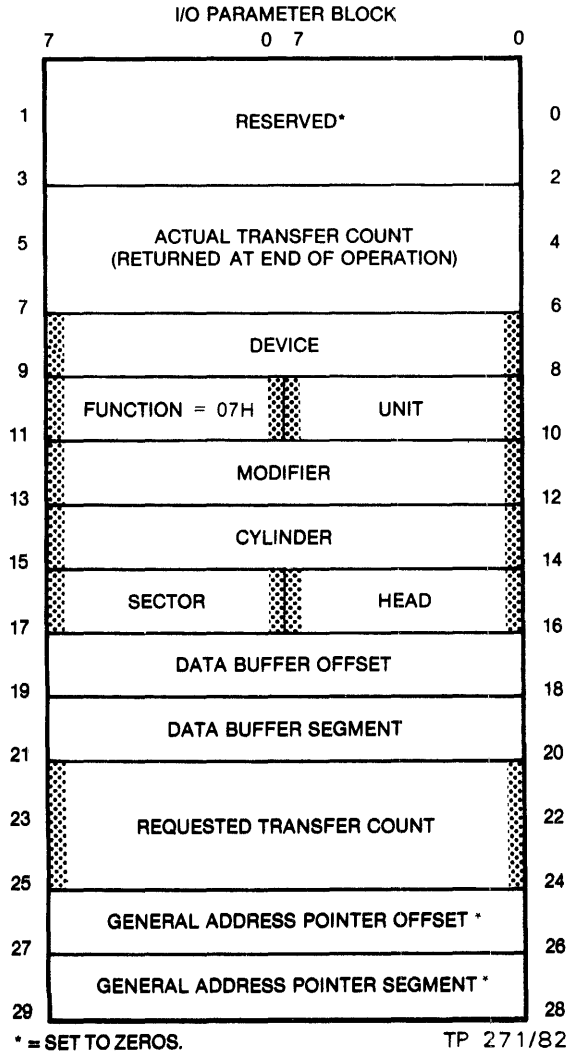


Figure 4-16. Write Buffer Data Function

There are two kinds of controller functions: short-term and long-term. On the 5215 and the 7215, all controller functions are short-term except initiate track seek (08H).

Short-term functions assert one interrupt when complete. This interrupt can be disabled by setting bit 0 of the IOPB modifier field to zero (see IOPB, in section 4).

When a short-term function is complete, the controller clears the busy 1 field and asserts an interrupt (if enabled). The status available must be processed before any other functions can be issued.

Initiate Track Seek (08H) is the only long-term function on the 5215 or 7215. It asserts two interrupts in the course of execution. The first interrupt can be disabled by setting bit 0 of the IOPB modifier field to zero. The second interrupt cannot be disabled.

A seek, up to the point of the first interrupt, is essentially the same as a short-term function:

- Up to the point of the first interrupt, the seek is the only function being executed.
- The status available at the point of the first interrupt must be processed before any other functions can be issued.

Any error detected at that point will be reflected in the status available when the controller clears the status semaphore and asserts the first interrupt (if enabled). If no error condition was detected, the status information will reflect this.

The program must process the status available when the controller clears the status semaphore and/or asserts the first interrupt before any other controller activity can take place. If the status shows an error, the seek is over: no second interrupt will be asserted.

Errors are detected and reported at the time of the first interrupt. There are no errors reported at the time of the second interrupt.

If the status at the time of the first interrupt shows no errors, then the seek continues. However, the status semaphore has been cleared, and the controller can process other functions. Any other function requested must be for a different drive.

After the status from the point of the first interrupt has been processed, if the program requests a short-term function the controller will execute it completely before asserting the second interrupt of the pending seek. If the new function is another seek, the controller will process it to the point of the first interrupt, just like a short-term function, before asserting the second interrupt of the pending seek.

Since any short-term function requested after the first interrupt of a seek must be completely executed including status processing by the program, before the controller will assert the second interrupt of the pending seek, there is no possibility of status from one function disrupting the other.

A second seek requested after the first interrupt of a previous seek will be handled up to the point of its first interrupt as if it was a short-term function; thereafter, both seeks are pending.

4.7.9 Initiate Track Seek (08H)

The initiate track seek command positions the read/write heads on the specified drive without transferring data (See Figure 4-17).

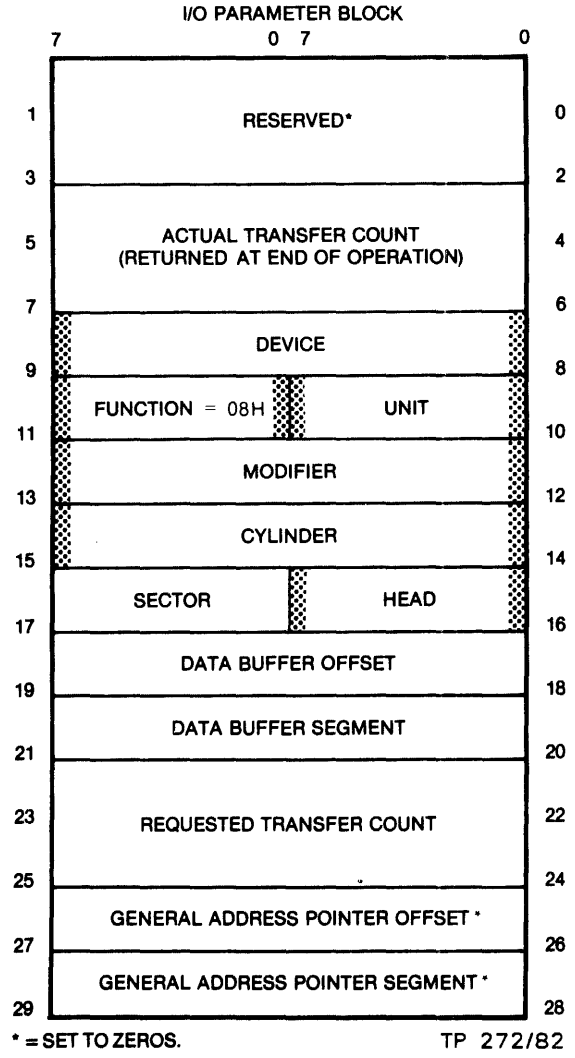


Figure 4-17. Initiate Track Seek Function

Each data transfer command includes an implied seek. The primary use of this command is to allow the controller to perform other activities on other drives in the system while the heads are being positioned. Unlike other commands, initiate track seek does not wait until the heads have reached the requested track before allowing the controller to accept a new command.

Once the controller determines that the drive is ready, a seek is initiated and status returned. When the heads on the drive have reached the specified track, seek complete status is posted and a seek complete interrupt is generated. Because the command is finished when the seek is initiated, several seeks may be in process on different drives at the same time (overlapped seek). This allows the host CPU to start seeks on multiple drives and read or write data from the first of them to reach the specified track.

One command, not a seek, may be executed while seeks are in progress. If a seek operation is requested before completion of a previous seek command for that same drive, an error is reported. If a seek to a cylinder beyond the end of media, including alternates, is initiated, the drive automatically performs a re-zero operation and posts an invalid address error.

4.7.10 Buffer I/O (0EH)

The buffer I/O function allows the host CPU to transfer data between the controller's on-board buffer and a Multibus memory buffer (See Figure 4-18). It is used primarily for diagnostic purposes and for filling the buffer for subsequent write buffer commands. No disk access is involved. The Multibus buffer is addressed by the data buffer offset and segment fields.

The on-board buffer starting address is specified in the cylinder field of the IOPB. For iSBC 215 compatibility, all addresses in the on-board buffer **MUST** be between 4000H and 45FFH. The head field in the IOPB specifies the direction of data transfer; 00H for on-board to Multibus (read the buffer), and FFH for Multibus to on-board (write the buffer) transfers. The requested transfer count specifies the number of bytes transferred the same way as for data transfers.

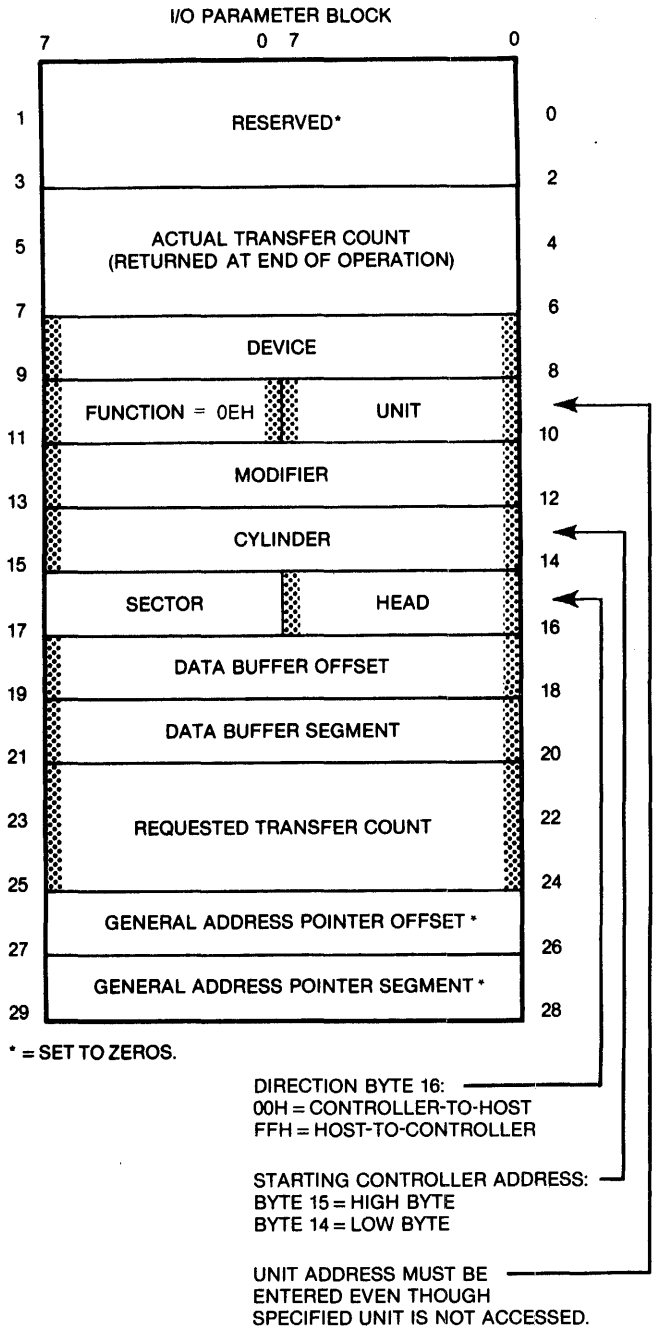


Figure 4-18. Buffer I/O Function

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4.7.11 Diagnostics (0FH)

The diagnostic function (0FH) exercises the controller and disk drive system to verify proper operation or to help isolate a malfunction to a subsystem. With 0FH set into the function field of the IOPB (See Figure 4-19), the diagnostic to be performed is determined by the Hex value in the upper byte (byte 13) of the modifier word. Table 4-6 lists the diagnostic tests and the hex codes used to select the individual tests. The number of diagnostic tests available to the user is dependent upon the setting of bit 2 (extended status) in

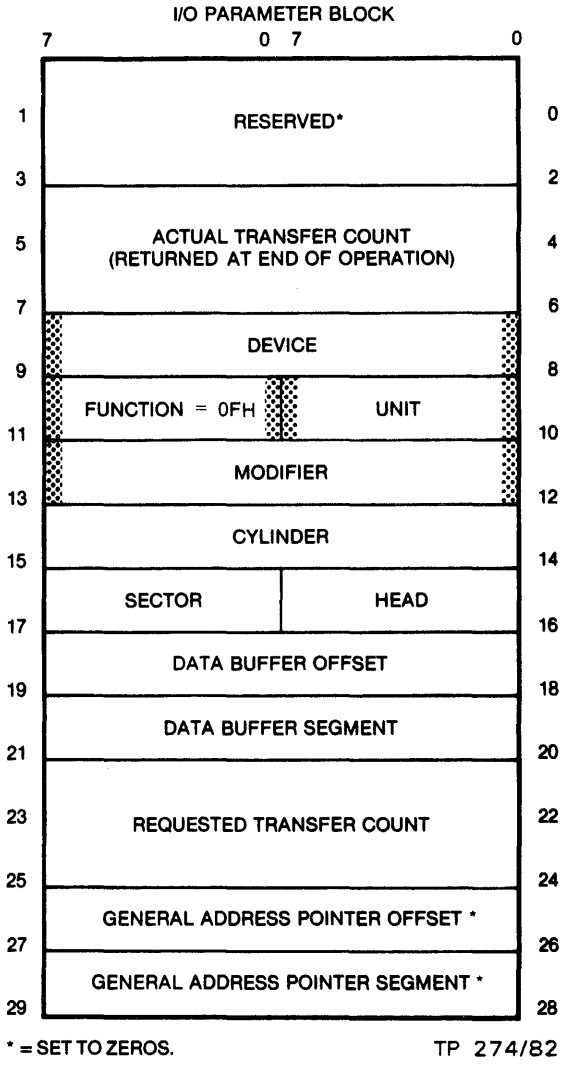

Figure 4-19. Diagnostic Function

the extension byte of the WUB. If read extended status is enabled, all the tests listed in Table 4-6 can be selected. If not enabled, only normal iSBC 215 tests can be selected. These tests are similar to off-line Hyper Diagnostics except, on-line diagnostics require the device and unit number be specified in IOPB. Each command issued will initiate one pass of selected diagnostic test.

The diagnostic track is located on a drive unit's last (highest number) track of head 0. When allocating memory space for the disk unit, this track **MUST** be dedicated to the diagnostic program. When beginning a diagnostic program, the head and cylinder are selected automatically; the user selects the drive unit.

Table 4-6. On-Line Diagnostics

Byte 13	Description
Normal Diagnostics:	
00H	A seek is executed to the last cylinder on the drive. Head 0 is selected and a read ID is performed to verify head position. The first sector is written with a 55AAH pattern and the same sector is read to verify the data and ECC/CRC.
01H	Controller self-test is executed once.
02H	Drive heads are positioned to cylinder 0.
Extended Diagnostics:	
1FH	**8085 Self-Test**: Tests the 8085 PROM, RAM, two-port buffer, and DMAC independent of components in read/write controller section.
1BH	**Read/Write Controller Self-Test**: Tests read/write controller without exercising drives. Test 1F must have been successfully completed prior to this test.
19H	**Drive Test**: Tests operation of the drive selected by the device and unit fields of the IOPB. ▪ **Floppy Drive Test**: Test only if drive is physically present, media is installed, and write enabled. Note that previous data on disk are destroyed during this test. Test first homes to track zero, then seeks out 35 tracks and returns to track zero. It then performs a Read ID command, and writes 16 double-density (256 bytes per sector) sectors with a double incrementing pattern of 0, 1 through 255, for sector 1. Each successive sector adds one to the content of each byte. Therefore, sector 2 is written as 1, 2 through 255, 0; sector 16 as 15, 16 through 255, 0 through 14. The test then reads and verifies the patterns. Test 1BH must first have been completed without error prior to initiating this test. ▪ **Winchester Drive Test**: This test will fail if Winchester has not been formatted. Test first lowers the heads to track zero, then seeks out 128 tracks and returns to track zero. It then performs a Read ID command to determine sector size, and reads sectors 0 through 3 on head 0 for three cylinders, checking for ECC errors. Test 1BH must first have been completed without error prior to initiating this test.
15H	**Tape Drive Test**: Test only if drive 0 is physically present, cartridge is installed and write enabled. Note that any previous data stored on tape are destroyed during this test. Test first retensions the tape cartridge (approximately two minutes), then writes two tracks with a double incrementing pattern from the buffer (another two minutes) and then reads and verifies the two tracks (final two minutes of test). Test one 1FH must first have been completed without error prior to initiating this test.

4.7.12 Reset Tape Drive (80H)

The reset tape drive command is accomplished by setting the device and function fields in the IOPB. The byte value for the device field is 10H, selecting the streaming tape drive. The function field contains a value of 80H as shown in Figure 4-20. This command resets the tape drive and brings it to a known initial state. Execution of this command aborts earlier tape operations that may have been in progress, and must be issued prior to other tape operations.

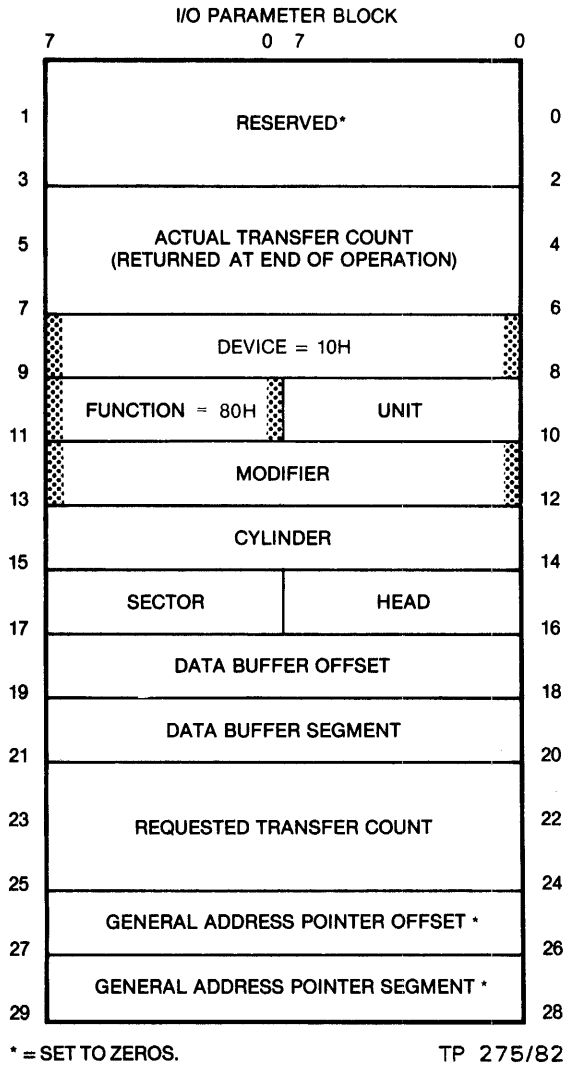

Figure 4-20. Reset Tape Drive Function

4.7.13 Disk Image Backup (81H)

The disk image backup command provides backup for data stored in Winchester drives. Figure 4-21 shows the IOPB for this function. The device field contains 00H selecting the Winchester drive. The unit field contains the Winchester unit number to be backed up. The function field contains 81H. The tape drive **MUST** be reset and the disk drive initialized prior to issuing this command.

If the size of the Winchester exceeds the capacity of the tape cartridge, the backup can be continued onto another cartridge. At the end of tape, the controller posts the status and generates an interrupt if enabled. The operation status byte contains the following information; operation not complete, media change not detected, seek not complete, Winchester drive type, no error, and Winchester

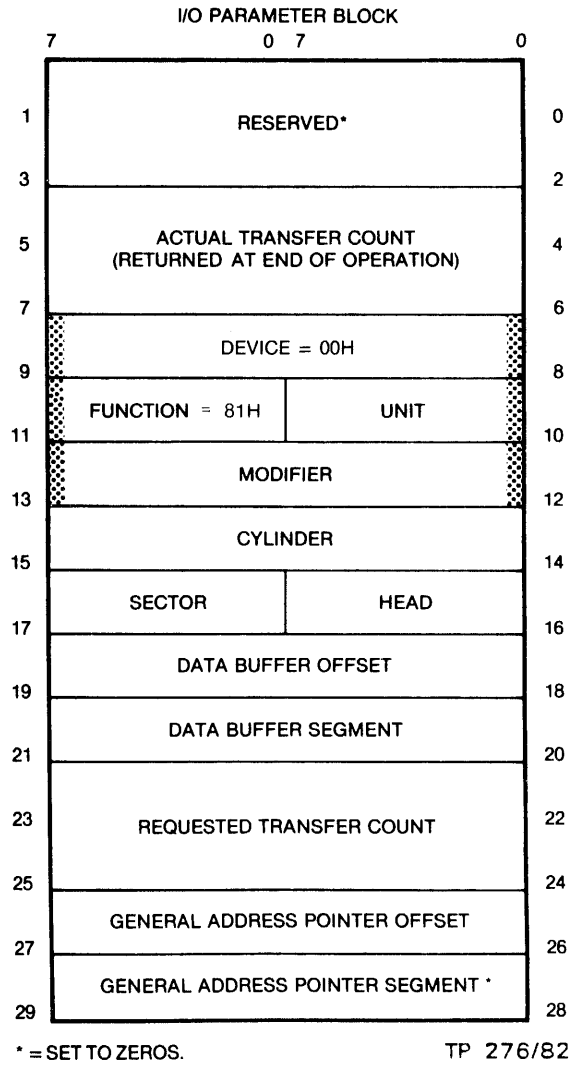

Figure 4-21. Disk Image Backup Function

unit number. When a new tape cartridge is inserted, the controller again posts status showing media change detected.

4.7.14 Disk Image Restore (82H)

The disk image restore function restores a previously backed up disk image from one or more tape cartridges. Figure 4-22 shows the IOPB for this command. The device field contains 00H for the Winchester drive. The unit field contains the Winchester unit number to be restored. The tape drive **MUST** be reset and the disk drive initialized prior to issuing this command.

If end of tape is reached before the restore is completed, the restore continues from the next tape cartridge in the order in which it was backed up. The change of tape procedure is identical to the disk image backup function command.

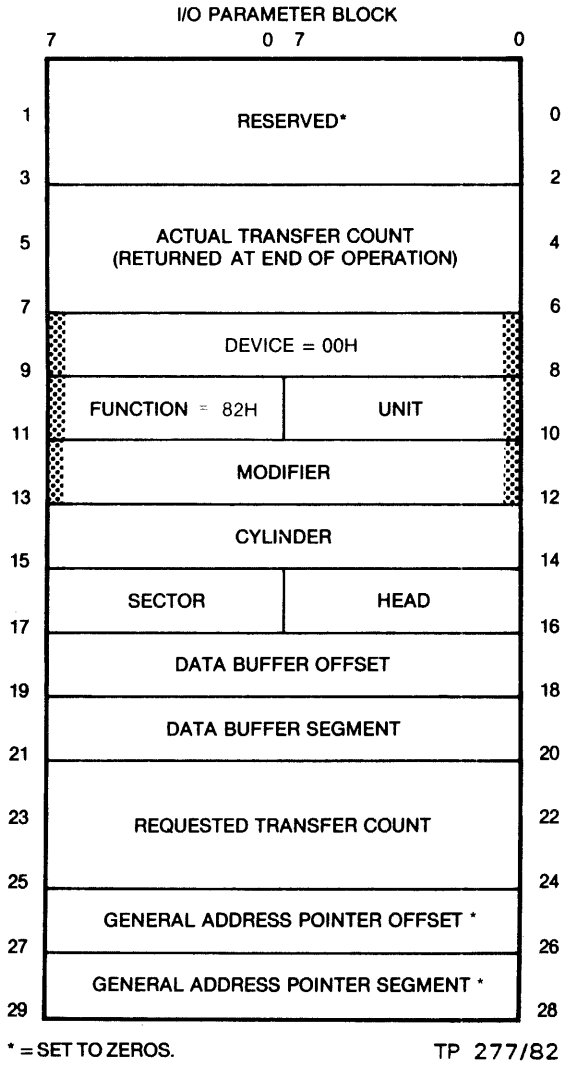

Figure 4-22. Disk Image Restore Function

Note

If the previous backup cartridge has been in storage, or additional data has been written to the Winchester since the last backup, a new backup image of the disk should be accomplished prior to attempting a disk image restore function. This insures against a complete loss of data if the previous backup cartridge is faulty.

To preform a disk image backup from one Winchester with disk image restore to another Winchester, the user MUST ensure that formatting of data area, number of heads, and sector size is the SAME for BOTH drives.

4.7.15 Read Tape Status (83H)

The read tape status function causes six status bytes, provided by the streaming tape drive, to be transferred to the host. Status byte 0 is transferred to the host memory location specified by the data buffer offset and segment fields. The remaining bytes follow in order.

The device field contains 10H, selecting the tape drive. The function field contains 83H (See Figure 4-23).

The six status bytes are defined as follows:

- **Status Bytes 0 and 1:** Bit 7 will be set true if any other bit has been set true. If bit 7 of either of the bytes is not set, no other bit will be set.

Bit	Description
Byte 0:	
7	Byte 0 has some other bit set.
6	Tape cartridge not inserted, or was removed while drive select light was on.
5	Selected drive was not present when command was issued.
4	Write command was given to a drive containing a write protected cartridge.
3	End of the last track was reached during a read or write operation.
2	Unrecoverable data error.
1	Unrecoverable error. The block in error may have been transferred.
0	File mark detected. (End of image reached during disk image restore.)
Byte 1:	
7	Byte 1 has some other bit set.
6	Illegal command sent to tape controller.
5	Drive controller was unable to find data on tape.
4	Eight or more read retries were required to recover a data block (indicative of a cartridge nearing end of life).
3	Tape is at beginning of tape, track 0.
2	Reserved.
1	Reserved.
0	Power-on reset has occurred since the last operation.

- **Status Bytes 2 and 3:** The third and fourth bytes contain a 16-bit binary number that is the count of the number of rewrites that occurred during a write operation, or the number of read retries that occurred during a read operation. Byte 2 contains the high byte, and byte 3 the low.
- **Status Bytes 4 and 5:** The fifth and sixth bytes contain a 16-bit binary number that is the count of the number of underruns that occurred during a read or write operation. Byte 4 contains the high byte, and byte 5 the low.

A read status command resets bits 0 through 3 in byte 0, and bits 0 through 7 in byte 1. It clears the count in bytes 2 through 5. To inform the user of data errors on tape, bits 0 through 2 of byte 0, and bits 4 and 5 of byte 1 will be set (if they were set on the last read status command).

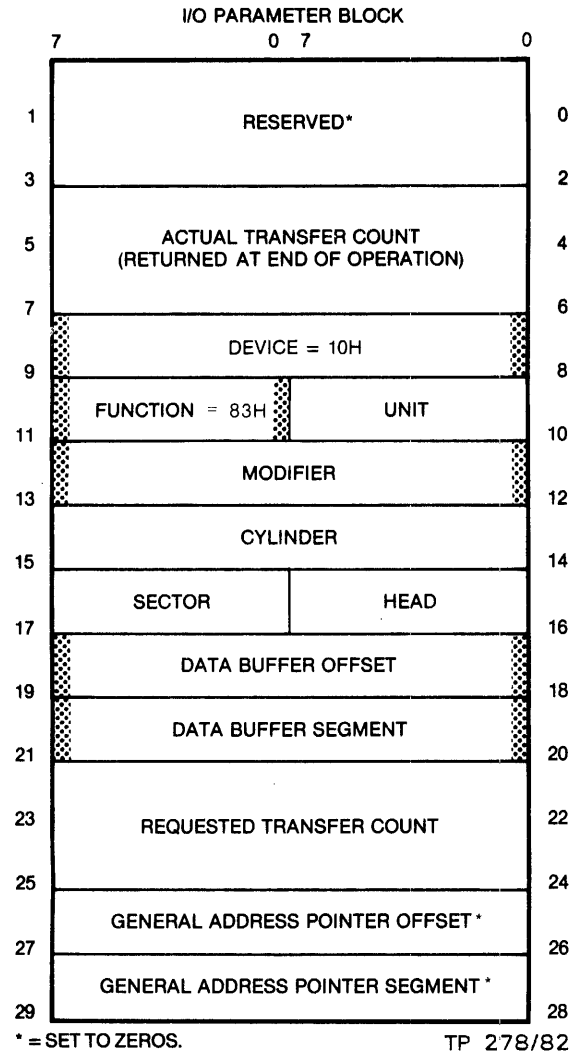

Figure 4-23. Read Tape Status Function

4.7.16 Tape Retension Cycle (84H)

The tape retension cycle function allows the user to retension the tape cartridge. For this function, the IOPB contains 10H in the device field. The function field contains 84H (See Figure 4-24).

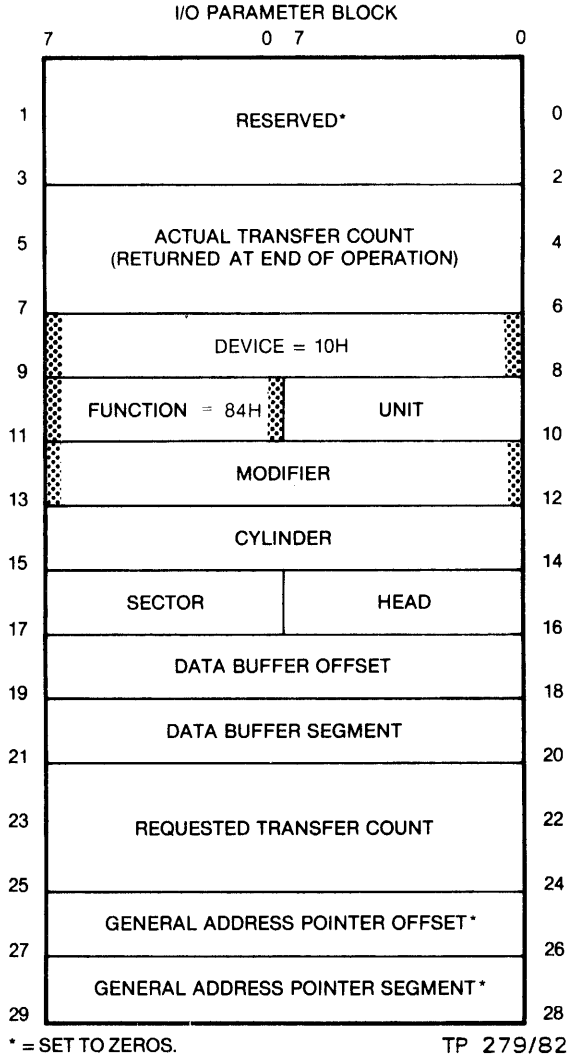

Figure 4-24. Tape Retension Cycle Function

This function command returns an operation completed status when the retension cycle starts. Except for a reset tape drive command that aborts any other command, commands issued before the retension cycle is completed wait for the command to complete before proceeding. Recommended for new cartridges or when tape drive has excessive amount of read retries or rewrites.

4.8 Error Processing

Under normal operation, commands issued to the controller are processed without error. The operation status byte for these commands reflects this by having the summary error bit (bit 7) equal to zero when status is reported. The host CPU takes appropriate action based upon whether the status is for the end of operation, a seek completion, or a new drive ready. If an error occurs, the level of host action is determined by the application and type of error. The transfer status command is often used to determine details of an error. Error status information is cleared at the beginning of each new command, except transfer status.

Errors generally fall into one of two catagories. The first are operational errors caused by software or operator and include illegal sector, wrong sector length, write protect errors, etc. The controller reports these errors so the host CPU, or operator may take corrective action. The second category is disk media errors. These occur because of flaws in the media itself (hard errors), or because of an occassional error on media read operations by the disk system (soft errors). The controller is pre-programmed to handle the majority of these errors directly, without host intervention. If automatic retries are not disabled by setting inhibit bit 1 in the modifier field of the IOPB, the controller attempts to recover from errors using a retry policy dependent upon the type of error encountered.

For errors caused by media read errors, the read operation is repeated up to five times before an error is considered hard. The number of retries is available at the end of the command by executing the transfer status command. Errors handled in this way are ECC for Winchester and CRC for floppy.

In addition to error recovery procedures, the controller supports error correction on data fields of the Winchester drives. When an ECC error is detected, the sector is re-read until it is read correctly, or the same error code is read twice. In the latter case, a correction is performed if the length of the error burst is less than 11 bits. When a CRC error occurs, an attempt is made to recover the data and continue.

When the transfer status command is issued with the extended error bit in the WUB extension byte set (bit 2), the last byte returned is an internal controller code for the precise error detected. For a hard error, this code is identical to that indicated by the flashing error LED (CR1). The operation status byte of the CIB indicates whether the error was hard or soft (Refer to Tables 4-3, 4-4, and 4-5). A soft error is one which was recovered with ECC or controller retry.

4.8.1 Bad Track Handling

The current state-of-the-art in the production of Winchester recording media makes it impossible to guarantee a flawless recording surface. A certain number of disk defects are expected. If a track has a defect, it is formatted as a defective track which points to an assigned alternate track. Refer to paragraph 4.7.3 for format function. The controller automatically switches to the assigned alternate track for subsequent operations. This automatic referral is transparent to the host.

Each disk surface should be divided into a data track and an alternate track area. The user may follow recommendations of the drive manufacturer, or can assign the number of tracks in the alternate track area, typically one to two percent of the total number tracks on the surface. Alternate tracks should be assigned to the inner tracks of the drive surface, and the last track of head 0 **MUST** be reserved for the diagnostic program. The assignment of alternate tracks must be reaccomplished each time the disk is reformatted.

When a track is formatted as a defective track, the controller writes the address of the alternate cylinder and head on every sector of the defective track. When the defective track is accessed, the controller automatically recognizes the track as defective and begins reading sectors until it reads one successfully. The controller then picks up the alternate track information from the data buffer and accesses the alternate track.

It may become necessary to determine which alternate tracks are already being used, in order to map a new defective track to an unused alternate. This can be done by issuing a read command to each track on the disk, followed by a read ID command. The flags reported by read ID will indicate whether an alternate track was encountered, and if so, which alternate track was addressed.

5 CONTROLLER ARCHITECTURE

5.1 Introduction

This chapter contains a basic block diagram description of the DSD Controller. The controller consists of a high speed internal bus and data path (pipeline), internal bus masters, and slave interfaces (See Figure 5-1). The MPU (microprocessor unit) and DMAC (direct memory access controller) control the bus as masters. The Multibus, streaming tape drive, and disk drive interfaces are slaves on the internal bus.

5.2 DSD Controller Description

The MPU, which provides all the intelligent controller functions, consists of a five MHz 8085 microprocessor, a pair of 2764 EPROMs, and a combination RAM-I/O counter peripheral chip. The 256-byte RAM is a local stack and scratch area that buffers disk commands received from the Multibus interface.

The I/O ports provide control lines for the slave interfaces and the Read/Write Controller (R/WC). The 8085 controls low speed operations such as buffering commands from the host system, housekeeping chores, executing on-board confidence tests, and initiating off-line backup and restore operations. It supports the iSBC 215 and iSBX 218 emulations.

The DMAC, a five MHz 8237 chip, transfers data at high speeds between one port of the dual-port memory and either of two slave interfaces. During backup and restore operations, data are transferred to and from the streaming tape interface. During disk operations, data are transferred to and from the Multibus interface.

Disk operations that are too fast for the MPU are performed by the R/WC. Its basic functions are to format the disk tracks, recognize header fields for disk sectors, and to read or write data on the drive, track, and sector specified by the MPU and the disk drive slave interface.

The R/WC is a 2910 sequencer clocked at the disk data rate, and is part of the data transfer pipeline. The sequencer uses 1K words of PROM which act as instructions to control other functions including the dual-port buffer and ECC/CRC gate array. The sequencer instructions are decoded by one of seven PALs (programmable array logic devices), to reduce chip count. The 2910 permits generation of data streams for direct writing in Winchester drives via the pipeline.

The dual-port buffer consists of a buffer controller with arbitration provided by two PALs. The dual-port buffer anticipates successive transfers to guarantee both the R/WC and the internal bus master always have the next byte of data available when requested.

The Multibus interface requests bus access and directs all data transfer operations once bus master control is achieved. Two PAL chips, tailored to the controller architecture, achieve efficient operation and maintain strict Multibus compatibility. The Multibus interface transfers data as bytes or words, depending upon the system environment. This is an important feature, as word transfer results in twice the data being handled per Multibus access.

Data integrity is a foremost concern of systems integrators. The controller incorporates a proprietary error correction chip which handles both Winchester ECC and floppy CRC. A unique computer-generated polynomial for ECC offers improvements in correction accuracy compared with conventional polynomials over a variety of sector sizes.

When data are read, the chip detects errors including error bursts up to 22-bits in length. If an error is detected, the controller automatically tries to re-read the sector. If a correct read ensues, the controller passes the data (via a DMA operation) and reports a soft error (via status registers) to the operating

system. If retries cannot correct the error and the error pattern is repeatable, the ECC chip allows up to 11 bits to be corrected.

The MPU writes the corrected bits directly into the dual-port buffer. The DMA controller transfers the corrected data to the Multibus main memory. Selection of automatic correction is software controlled.

A high performance PLL (phase-locked-loop) performs data separation for both Winchester and floppy disks. The PLL locks the controller onto the serial bit stream so data can be correctly interpreted. The PLL has been optimized for the best possible reading margins over a wide range of temperature and voltage variations.

The disk controller uses a PAL to encode and decode the data before writing or during reading. The serializer/deserializer (SERDES) provides parallel-to-serial conversion of data during write operations and vice versa during read operations. Drivers and receivers are installed as needed to interface with the disk drive control and data signal lines.

The quarter-inch streaming tape drive uses an eight-bit parallel data bus to transfer data and commands. Handshake and status lines control the direction and type of information transmitted over the eight-bit data path. A PAL is programmed to handle transfer protocol while the DMA chip moves data between the tape interface and dual-port buffer during disk backup/restore. The controller is active during this time in handling data transfers between the disk and dual-port buffer.

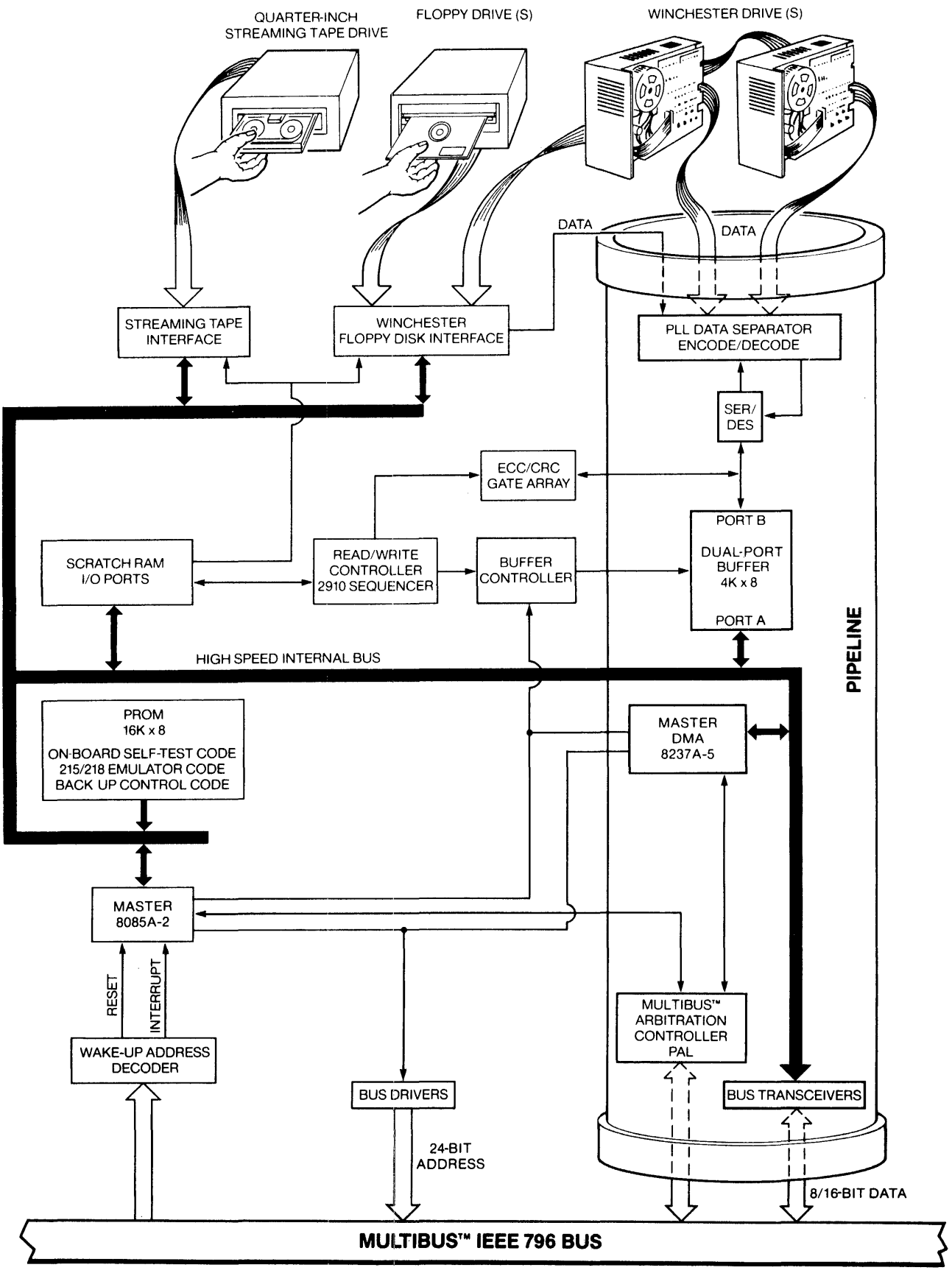

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Figure 5-1. DSD 5215 Multibus Controller Block Diagram

6 USER LEVEL MAINTENANCE

6.1 Introduction

This chapter provides information on user level maintenance of the DSD Multibus Disk Controller. Coverage includes troubleshooting and fault analysis, HyperDiagnostic routines, error codes, and customer service assistance.

The DSD Controller requires no adjustment in the field. User level maintenance is limited to the use of HyperDiagnostics to isolate any problem to the subsystem and then swapping the module at fault for a known good one. All subsystem modules can be readily removed and replaced without the need of special tools. Information on returning a product to the factory for repair is covered paragraph 6.4.

6.2 Troubleshooting and Fault Analysis

The following list of diagnostic tools is furnished to assist in the isolation of faults that may occur.

- Built-In Self-Tests
- Activity Indicators on the Controller Module
- On-Line or Extended Diagnostic Routines
- Off-Line HyperDiagnostics
- DSD Customer Service Hotline

The built-in self-tests, and the use of activity indicators CR1 (ERR), and CR2 (RDY), were described under Initial Checkout and Acceptance Tests, contained in Chapter 3. On-line or extended diagnostics are described under the diagnostic function command (0FH), contained in Chapter 4.

The following paragraphs describe the use of off-line HyperDiagnostics and interpretation of error codes.

6.3 Off-Line HyperDiagnostics

Jumper group W6, located at coordinate E5, enables and selects the off-line HyperDiagnostic test to be performed. This is a secondary function of W6. The jumper group must be restored to its standard configuration upon completion of testing.

Jumper W6-5 is removed to enable the off-line diagnostics. The specific test to be performed is selected by jumpers W6-4 through W6-0. These jumpers represent a hexadecimal value with the least significant bit provided by W6-0 and the most significant bit by W6-4. An inserted jumper represents a value of 1 and an open jumper a value of 0.

When testing has been enabled and selected by jumper group W6, a power-up, Multibus INIT/ signal, or a programmed reset and clear command through the wake-up I/O port causes the selected diagnostic to begin execution.

LEDs CR1 (ERR) and CR2 (RDY), mounted in the upper left hand corner on the component side of the controller board, indicate the status of the diagnostic test being performed. After the selected diagnostic begins, CR1 (ERR) and CR2 (RDY) turn OFF. When the test is completed with no errors, CR 2 (RDY) turns ON, and the test begins again. Upon successful completion of the second pass, CR2 (RDY) turns OFF. If no error is detected, the test continues indefinitely, with each successful pass of the diagnostic indicated by CR2 (RDY) changing state; OFF to ON, or ON to OFF.

If an error is detected during the execution of a diagnostic, the test halts and CR1 (ERR) blinks the appropriate error code. Refer to paragraph 6.3.1 for detailed information on blinking error codes and their interpretation.

A complete set of tests are provided for use in the off-line HyperDiagnostic mode. A detailed description of the individual test is

provided after the table and includes the approximate time required to complete one pass of selected test.

Table 6-1. Off-Line HyperDiagnostics and Jumper W6 Configurations

Test (Hex)	Description	Jumper Group W6 MSB 5	4	3	2	1	LSB 0
1F	8085 Environment Self-Test	OUT	IN	IN	IN	IN	IN
1E	Factory Use Only	OUT	IN	IN	IN	IN	OUT
1D	Factory Use Only	OUT	IN	IN	IN	OUT	IN
1C	Factory Use Only	OUT	IN	IN	IN	OUT	OUT
1B	R/WC Self-Test	OUT	IN	IN	OUT	IN	IN
1A	CR1, CR2 Blinking Wakeup Address	OUT	IN	IN	OUT	IN	OUT
19	Floppy Drive 0	OUT	IN	IN	OUT	OUT	IN
18	Floppy Drive 1	OUT	IN	IN	OUT	OUT	OUT
17	Winchester Drive 0	OUT	IN	OUT	IN	IN	IN
16	Winchester Drive 1	OUT	IN	OUT	IN	IN	OUT
15	Tape Drive	OUT	IN	OUT	IN	OUT	IN
14	Stand Alone System	OUT	IN	OUT	IN	OUT	OUT
13	Multibus Read/Write	OUT	IN	OUT	OUT	IN	IN

HyperDiagnostic routines in detail:

1F **8085 Environment Self-Test:** Tests 8085, PROM, RAM, two-port buffer and DMAC independent of components in the read/write controller section of the board. Test takes approximately 45 seconds to complete one pass. CR2 (RDY) light toggles ON to OFF or OFF to ON to indicate completion of one pass.

1E **Winchester PLL Alignment:** Factory use only.

1D **Floppy Double-Density PLL** Alignment: Factory use only.

1C **Floppy Single-Density PLL** Alignment: Factory use only.

1B **Read/Write Controller Self-Test:** Tests the Read/Write Controller hardware without exercising the disk drive. Test 1F must be successfully completed prior to implementing this test. Test takes approximately one millisecond to complete one pass.

1A **CR1, CR2, Blinking Wakeup Address Test:** CR1 is the clock and CR2 represents the bits set by each of the 16 wakeup address jumper settings. The test flashes through an eight-bit cycle, most significant bits first, waits two seconds and then flashes the remaining eight bits, waits two seconds and then loops to repeat the test. See timing diagram, Figure 6-1.

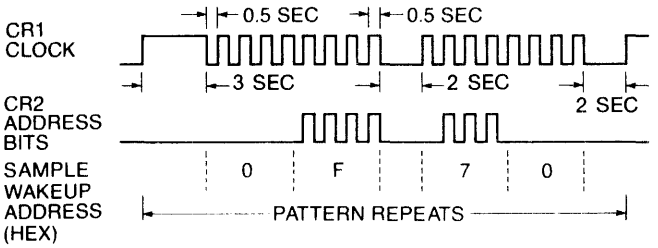

Figure 6-1. Timing for CR1, CR2 Blinking Wakeup Address Test

As shown in Figure 6-1, CR1 (clock) is on for three seconds before beginning the first series of eight clock pulses. The value of CR2 is valid only when the clock (CR1) is high (ON). That is, if CR1 (clock) is ON and CR2 is OFF, the bit value is zero. Conversely, if CR1 and CR2 are both on, the bit value is one. Figure 6-1 shows the timing of a sample wakeup address of 0F70 Hex. The test takes approximately 23 seconds to complete one pass.

19 **Floppy Drive 0 Test:** Test only if drive is physically present and media is installed and write enabled . Operator should note that previous data stored on disk are destroyed during this test. Test first homes the head to track zero, then seeks out 35 tracks, and returns to track zero. The test then performs a Read ID command, and writes 16 double-density (256 bytes per sector) sectors with a double incrementing pattern. Sector 1 is written in pattern 0, 1 thru 255. Each successive sector adds one to content of each byte. Therefore, sector two is written as 1, 2 thru 255, 0; sector 16 as 15, 16 thru 255, 1 thru 14. The test then reads and verifies the patterns. The test takes approximately nine seconds to complete one pass. Tests 1F and 1B must first have been completed successfully prior to implementing this test.

18 **Floppy Drive 1 Test:** Exactly the same as test 19, if drive 1 is physically present.

17 **Winchester Drive 0 Test:** This test will fail if the Winchester has not been formatted. Test first homes the heads to track zero, then seeks out 128 tracks and returns to track zero. The test then performs a Read ID command to determine sector size, and then reads sectors 0 through 3 on head 0 for 3 cylinders and checks for ECC errors.

Test takes approximately four seconds to complete one pass. Tests 1F and 1B must first have been successfully completed prior to implementing this test.

16 **Winchester Drive 1 Test:** Exactly the same as test 17, if second drive is physically present.

15 **Tape Drive Test:** Test only if drive is physically present and cartridge is installed and write enabled.

Note:

Any previous data stored on tape are destroyed during this test.

Test first retensions the tape cartridge (appoximately two minutes), then writes two tracks with a double incrementing pattern from the buffer (another two minutes) and then reads and verifies the two tracks written (final two minutes of test). Test 1F must first have been successfully completed prior to implementing this test. Test takes approximately six to eight minutes.

14 **Standalone System Test:** Note that this test will destroy any data previously stored on floppy disks or tape cartridges. Test runs diagnostics 1F, 1B, 19, 18, 17, 16, and 15 sequentially, if all drives are physically present.

Note:

Details of each test are given previously, and operator should familiarize himself with these tests.

Error 47 indicates that the controller recognizes no drives as present, and either the drives are malfunctioning or the cabling between drives and controller is not correct. Time for one complete pass of standalone system test depends upon the number of drives present in system.

13 **Multibus Read/Write Test:** Test writes and reads Multibus memory 000000 Hex to 000FFF Hex using DMA. Memory must exist from 000000 Hex to 000FFF Hex, and BPRN/ (Multibus pin P1-15) must be low giving the controller bus priority. BCLK/ must be present. First pass of this test has a three second ready time and then two second run time. Each successive pass of this test takes two seconds. Test 1F must first have been completed successfully prior to implementing this test.

6.3.1 HyperDiagnostics and Error Code Interpretation

To initiate the off-line HyperDiagnostics proceed as follows:

1. With the power OFF, remove the DSD controller board from the host backplane.
2. Reconfigure jumper group W6 as shown in Table 6-1.
3. Reinstall the controller card in the host backplane and apply power in the host computer.
4. Selected diagnostic begins with application of power with each successful pass of the test indicated by CR2 (RDY) changing state (OFF to ON, or ON to OFF). The test continues until halted by the user.

To halt the continuous repeating sequence of the successful diagnostic, remove power from host computer, reconfigure jumper W6 to select drive types used in system (Refer to Section 3 for drive type select information), and reinstall controller in backplane.

If an error is encountered during any HyperDiagnostic test, the test will halt, CR2 (RDY) will be OFF, and CR1 (ERR) will begin blinking the error code. Figure 6-2 illustrates the sequence of CR1 (ERR) while blinking an error code.

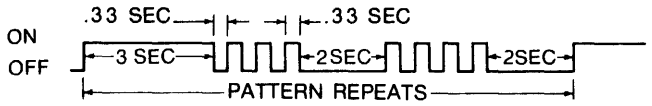

Figure 6-2. CR1 Blinking Error Code TP 281/82

Figure 6-2 shows the on/off sequence of CR1 (ERR) blinking error code 34 Hex. The sequence start is indicated by CR1 (ERR) being on for three seconds. CR1 then begins a series of short pulses (three in this example) to indicate the first digit of the error code.

A two-second off time signals completion of first digit. Then CR1 (ERR) begins a second series of short pulses to indicate the remaining digit and another two-second off time. The pattern then repeats. The sequence can be

halted by removing power, or by initiating another diagnostic test. The blinking error codes of CR1 (ERR) are the same error codes reported by the extended status byte in the error status buffer (Refer to Chapter 4).

6.4 Maintenance Assistance

Data Systems Design maintains a fully staffed Customer Service Department. If at any time during inspection, installation, or operation of the equipment you encounter a problem, contact one of these offices. Our trained staff can help you diagnose the cause of failure, and if necessary, speed replacement parts to you. Any time you need to return a product to the factory, please contact Customer Service for a Material Return Authorization Number.

Data Systems Design
Customer Service:

Western Region
2241 Lundy Avenue
San Jose, CA 95131
(408) 946-5800
TWX: 910-338-0249

Central Region
5050 Quorum Drive
Suite 339
Dallas, TX 75240
(214) 980-4884

Eastern Region
51 Morgan Drive
Norwood, MA 02062
(617) 769-7620
TWX: 710-336-0120

North Central Region
2311 West 22nd Street
Suite 110
Oakbrook, IL 60521
(312) 920-0444

For products sold outside the United States, contact your local DSD distributor for parts and customer service assistance.

APPENDIX A: DSD 5215 MULTIBUS DISK CONTROLLER DRIVE CONFIGURATIONS

This Appendix provides drive jumpering for selected drives supported by the DSD 5215 Controller. Each drive type has a table that shows each jumper, its description, and the required configuration for proper disk system operation. Tables included are:

- Table A-1: SA460 Floppy Drives (Double-Sided)
- Table A-2: ST412 Winchester Drives
- Table A-3: One and Two Drive System Configurations

Note that there are no drive jumper options for the streaming tape drive. Jumpers are factory set for the tape drive and the user **MUST** leave as set for proper operation.

Table A-1. SA460 Floppy Drive Jumper Configuration

Trace Designator	Description	Required Setting IN	OUT
U3	Termination for Standard Inputs	Table A-3	
DS1,2,3,4	Drive Select 1 Through 4	Table A-3	
MX	Drive Select Enabled Single Drive System		X
MS	Motor On from Drive Select		X
SS	Standard Side Select	X	
SD	Side Select Using Direction Select		X
DD	Door Disturb	X	
DO	Door Open		X
RI	Ready Index	X	
RD	Ready Door		X
DA	Door Lock from Drive Select		X

Table A-2. ST412, Winchester Drive Jumper Configuration

Trace Designator	Description	Required Setting IN	OUT
R	Radial Option		X
DS1,2,3,4	Drive Select	Table A-3	
6F Dip	Terminator for Standard Inputs	Table A-3	

An Option Shunt Block is provided at IC position 6E on the ST412 (terminator block is adjacent at location 6F). The 14-pin shunt block (16-pin socket) is plugged in pins 2 through 15, leaving pins 1 and 16 open.

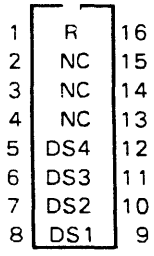

Table A-3. One and Two Drive System Configurations

	Drive Select 1	2	3	4	Terminator
One Drive Systems:					
	IN	OUT	OUT	OUT	IN
Two Drive Systems:					
Drive 1	IN	OUT	OUT	OUT	OUT
Drive 2	OUT	IN	OUT	OUT	IN

APPENDIX B: CROSS REFERENCE INDEX

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DATA SYSTEMS DESIGN

Data Systems Part Number:
040040-01, Revision B