system reliability/system integrity
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EPROM-32/64K
EPROM/ROM BOARD WITH
8 AND 16 BIT DATA PATHS
FOR THE IEEE 696/S-100 BUS

USER'S MANUAL

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SECTION 1 INTRODUCTION AND GENERAL INFORMATION

1.1 Introduction

The Dual Systems EPROM-32/64 EPROM/ROM board has sockets for up to sixteen industry-standard EPROM or ROM integrated circuits. The board is useful in applications which require non-volatile storage of programs and data. The board may also be used as a RAM board, if suitable RAM integrated circuits are installed in place of EPROMS. RAM's may be intermixed with type 2716 EPROMS.

The EPROM-32/64 is normally shipped configured for use with type 2716 EPROMS. In this configuration, the board has a capacity for storing up to 32,768 (32K) bytes of data.

The EPROM-32/64 may be altered for use with type 2732 EPROMS. In this alternate configuration, the board will hold up to 64K bytes of data. Section 2.2.1 describes the procedure for modifying the board to accept 2732 EPROMS.

The EPROM board has been designed to make use of the advanced features contained in the proposed IEEE-696 standard for the S-100 bus. Data path widths of either 8 or 16 bits may be selected by the computer. Extended addressing may be done either through 24-bit direct addressing, or through the bank select feature used with most pre-standard S-100 computers. Hence, the EPROM board meets the IEEE proposed specifications for new computers while remaining compatible with most existing systems.

1.2 FEATURES

* Up to 64K bytes of nonvolatile read-only memory on one IEEE-696/S100 board.

* 8 or 16 bit wide data paths.

* Specifically designed to be compatible with the new 16 bit CPU boards, including the Dual Systems CPU/68000 and CPU/68000M

* On board wait state generator allows operation in up to 6 MHz systems.

* Full compliance with I.E.E.E. 696 Proposed Standard for the S-100 bus, while remaining compatible with almost all pre-standard S-100 computers (eg. Cromemco SCC, Systems 2 and 3, Northstar Horizon, etc.)

* Extended 24-bit addressing.

* Bank Select, with automatic enable or disable on system reset.

* Starting address may be set on any 4K byte boundary in the address space when unit is configured as a 32K byte board.

* Any 4K byte block of memory may be disabled or enabled by means of a DIP switch with unit configured as 32K board. 8K blocks may be disabled with unit configured as 64K board.

* Allows operation with 2K byte static RAM integrated circuits, in place of EPROMS, when board is set for factory configuration. RAMS may be intermixed with type 2716 EPROMS.

1.3 SPECIFICATIONS

Memory Capacity: 32,768 Bytes (factory configuration)
65,536 Bytes (alternate configuration)

Bus Compatibility: S-100 as defined in IEEE-696 proposed standard. Also compatible with most earlier non-standard S-100 systems.

I.E.E.E.-696 Compliance level:

Slave D8/D16 LO/LE M24 I8 F6 T_{epr}+50nS W1

where T_{epr} is the address access time of the EPROMS installed in the board. Refer to the IEEE-696 proposed standard for an explanation of the above notation.

Memory Type:
Factory Configuration:
2716 EPROMS
2316 ROMS
6116 RAMS

EPROMS must be "single supply" (+5 volt) and must not consume more than 30 milliamperes in standby mode, and 150 milliamperes in operating (read) mode.

Recommended vendor: NEC (for EPROMS)
HITACHI (for RAM's)

Alternate Configuration:
2732 EPROMS
Also: Other EPROMS or ROMS with same pinout as 2732 EPROM.

EPROMS must be "single supply" (+5 volt) and must not consume more than 30 milliamperes in standby mode, and 150 milliamperes in operating (read) mode

Recommended vendor: NEC

Access Time: Board access time is equal to access time of added EPROM or ROM chips plus 50 nS. For example: Board access time is 400 nS when loaded with 350 nS EPROMS or RAM chips.

Wait States: 0 or 1 wait state (switch selectable)

Address Selection:

Factory Configuration:

-Board arranged as single 32K byte block.
-Any 4K byte block of EPROM/ROM space may be enabled or disabled by means of dip switches.
-Starting address may be set for any 4K byte boundary within 64K byte address space

Alternate Configuration:
(board modified for 2732 EPROMS).

-Board arranged as single 64K byte block. Any 8K byte block of EPROM/ROM space may be enabled or disabled by means of dip switches.
-Starting address of board automatically is XX0000 Hex. In other words, board spans entire 64K Global address space. However, board may be made to begin on other 8K byte boundary by installing EPROMS at the desired address blocks.

Global Addressing Mode: (16-bit) — Board addressed as specified above.

Extended Addresssing: (24-bit) — When enabled, uses address lines A16 through A23 to determine which 64K byte page the EPROM board will reside on, in a 16 megabyte address space.

Bank Select: — An I/O-mapped output port is used to enable or disable the board. The EPROM 32/64's bank select is compatible with most current bank-select schemes. The output port address is switch-selectable on any even address in the I/O address space.

Phantom: — When the phantom line is asserted, the EPROM 32/64 can be set to disable itself, regardless of the state of the address lines.

Data Transfers: — 8 or 16-bit. High order (M.S.) byte (during 16-bit transfers) can be jumper selected to have either odd or even address (during 8-bit transfers). Operates with 8-bit systems if successivebytes are stored in alternate EPROM chips.

Operating Power:

Voltage:	Operates on +8 volts (nominal) as supplied on S-100 bus. Minimum voltage 7.5 volts, maximum 12 volts.
Current:	650 milliamperes typical, 1200 mA maximumwhen board is fully loaded with NEC 2732 EPROMS.

Environmental Requirements:

Operating Temperature: 0 to 55 degrees Celsius
Relative Humidity: 90% maximum, without condensation.

SECTION 2. BOARD SETUP AND INSTALLATION

2.1 BEFORE YOU USE THE BOARD.

All EPROM 32/64K memory boards are burned-in at the factory for 168 hours, and then thoroughly tested before being shipped. Therefore, these boards should work when you receive them.

When unpacking the boards, a brief visual inspection should be made. If there is any obvious physical damage to the units, or to the packaging materials, a claim should be filed with the carrier.

Before plugging the EPROM board into your S-100 system, it will be necessary to configure the board for the system, by setting the on board DIP switches and jumpers as described in the following sections.

2.2 SETTING UP YOUR BOARD

Five groups of switches and two jumpers control the selection of all options on the board. Figure 1 shows the function of all switches and jumpers for the FACTORY-configured board.

This section of the manual gives a brief explanation of the switch settings which is sufficient for most applications. The following three examples of typical configurations are given:

1. A "NO OPTIONS" mode, in which the EPROM-32/64K is used in its factory configured 32K mode, in 8-BIT computers, without the need for multiple memory banks or extended addressing. THIS SIMPLE CONFIGURATION IS ALL THAT IS REQUIRED IN MOST APPLICATIONS. SEE FIGURE 4.

2. An example using the new 24-BIT EXTENDED ADDRESSING scheme found in new systems which make use of the features specified in the IEEE proposed S-100 standard. SEE FIGURE 5.

3. An example using the BANK SELECT option, which allows the computer to access multiple memory banks. This feature is used mostly in "pre-IEEE standard" systems where more than 64K bytes of memory are needed, or in certain multi-user systems. SEE FIGURE 6.

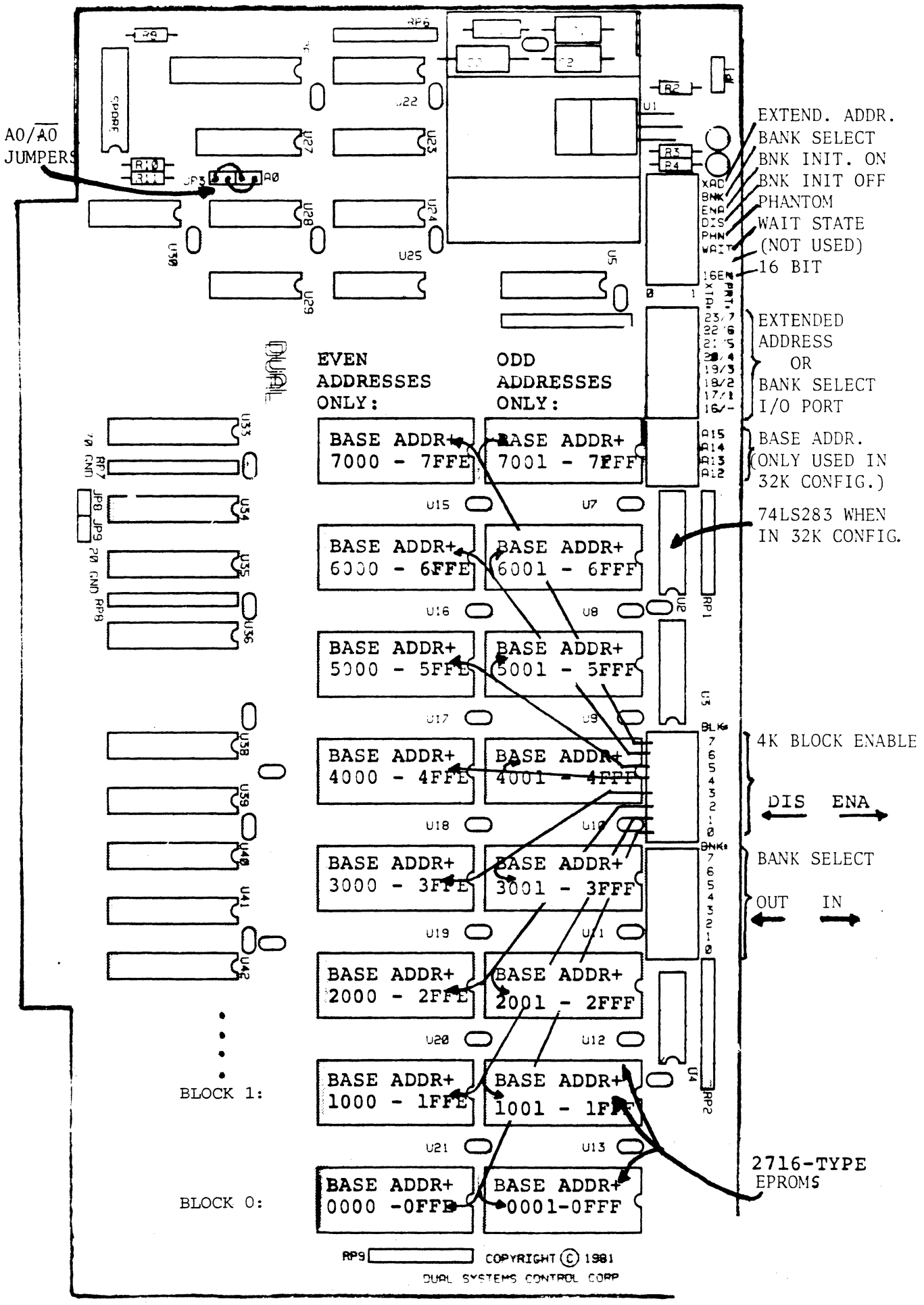


Figure 1. Switch and Jumper Overview for FACTORY CONFIGURATION ONLY.

2.2.1 CONFIGURING THE EPROM-32/64K BOARD FOR 64K OPERATION USING 2732's.

Your EPROM board may be altered so that 2732's may be used instead of 2716 type EPROMs. In this configuration, only 2732 type EPROMs may be used. 2716's or 6116 RAM IC's may not be mixed with them. Of course, PROMS with equivalent pinout and electrical specifications to the 2732 may be used.

To make this change, do the following:

Step 1

Remove integrated circuit U2, a 74LS283, as shown in figure 2. To avoid hurting yourself, use a tool - not your fingers.

Step 2

Remove I.C. U28, a 74LS32. Keep U2 and U28, if you intend to convert the board back at some later date.

Step 3

Remove integrated circuit U29, a 74LS08, and bend out pin 2 on it. Refer to figure 2 to locate the IC's and pin 2 on U29. Replace U29 back into its socket, being sure that pin 2 does not accidently make any contact with the socket.

Step 4

Find your jumper assembly and insert the 16-pin header in the socket for U2 exactly as shown in figure 2.

Step 5

Install the 14-pin header in the socket for U28 exactly as shown in figure 2.

Figure 1 should now be IGNORED. Figure 3 should instead be used to determine all switch, jumper and EPROM socket functions on your modified board.

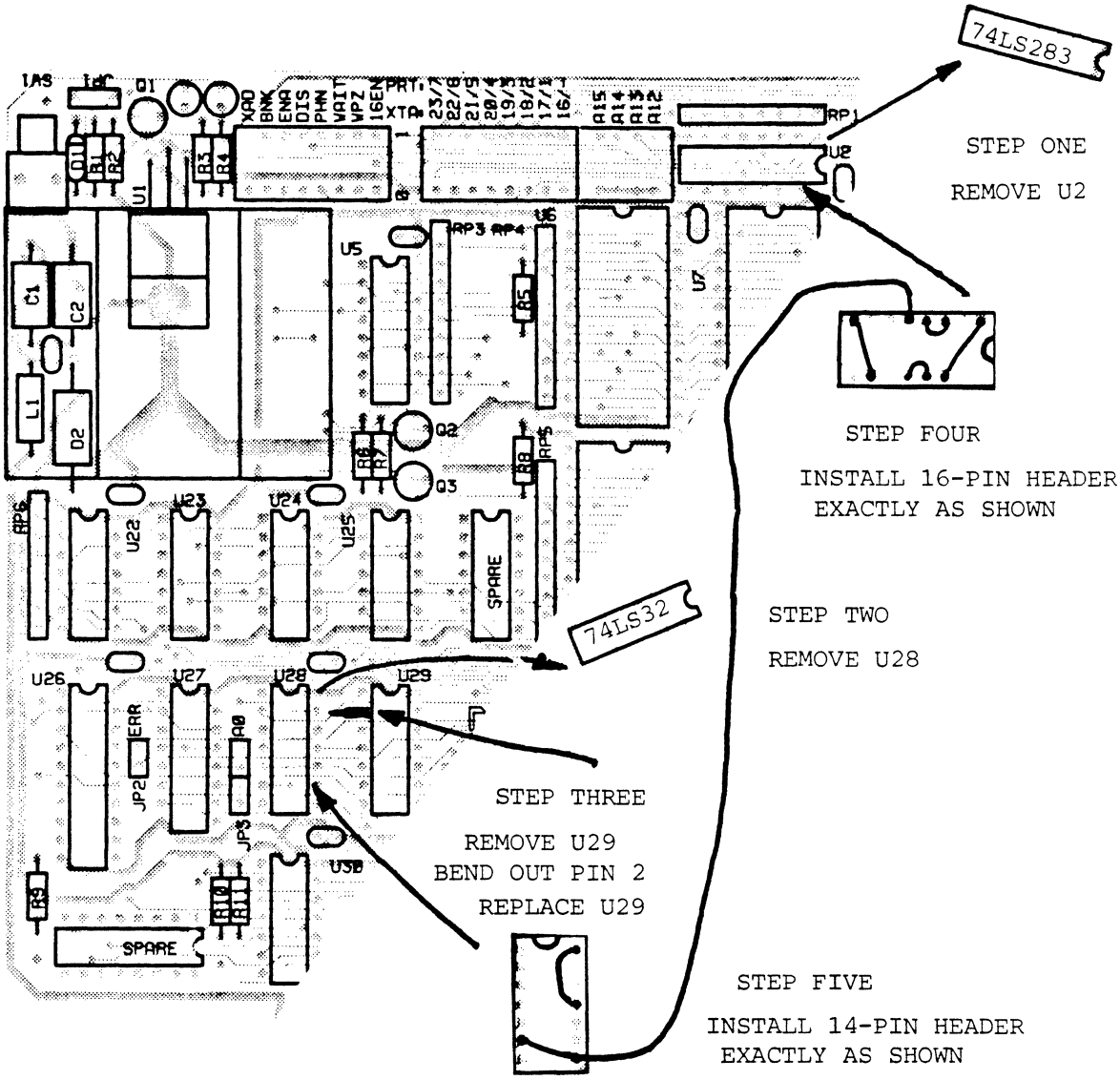


Figure 2. Steps for converting the EPROM board for operation with type 2732 EPROMS.

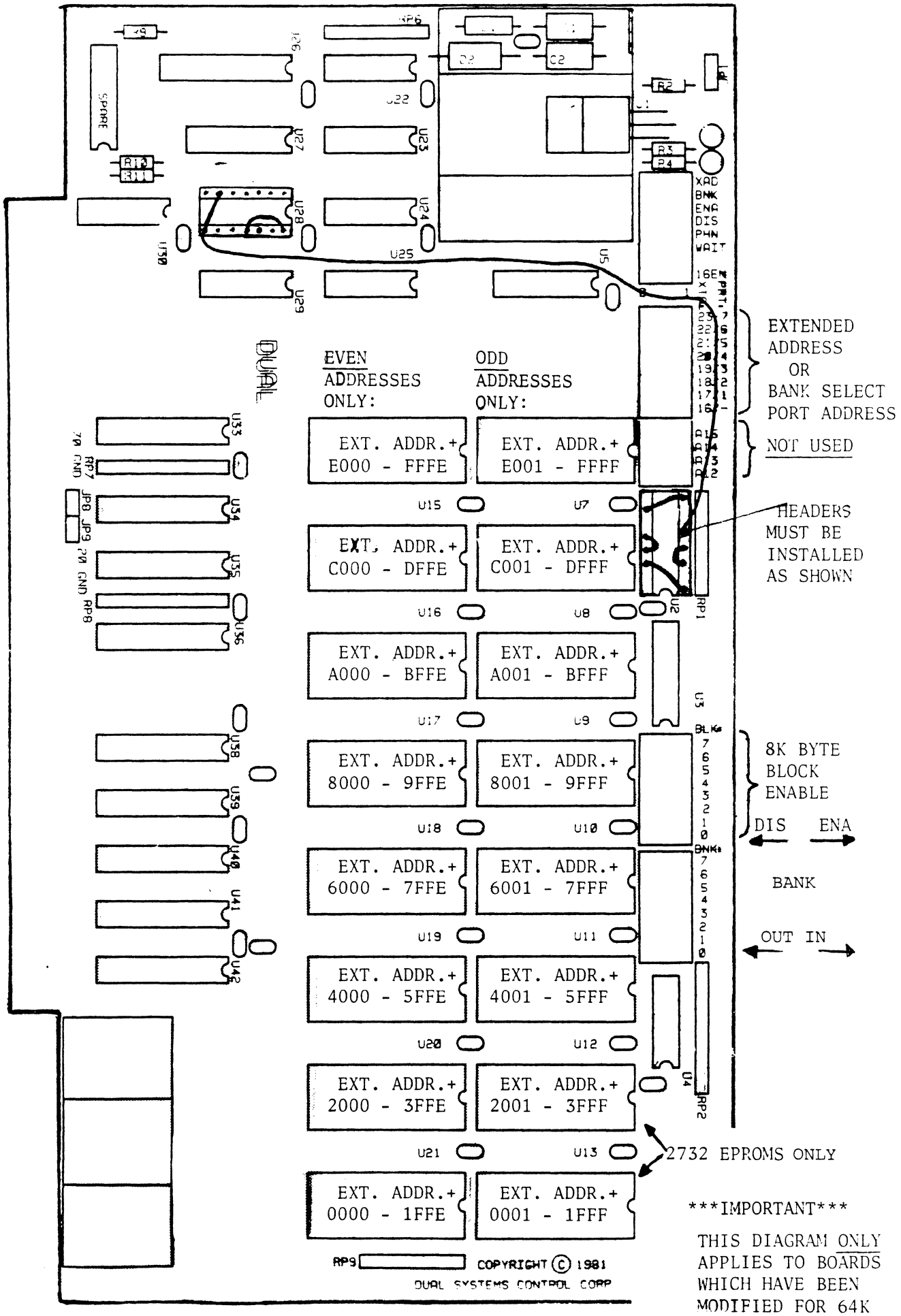


FIG. 3. Switch, Jumper and EPROM socket functions for MODIFIED (2732) BOARDS ONLY.

2.2.2 SETTING THE BASE ADDRESS (STARTING ADDRESS) (SWITCH S3, POSITIONS 1 THROUGH 4)

2.2.2.1 FOR FACTORY-CONFIGURED BOARDS (USING 2716's)

In the factory configuration (32K), positions 1 through 4 of switch SP3 are used to select the starting address of the board. This address may be set for any 4K byte boundary within the 64K byte "global" address space (eg. 0, 4096, 8192, ..., 61440). The settings of these switches are independent of any extended addressing scheme (ie. bank select, phantom, 24-bit extended addressing, or no extended addressing at all). Positions 1 through 4 of SP3 merely specify the starting address of the board WITHIN THE 64K BYTE ADDRESS SPACE CURRENTLY BEING ACCESSED BY THE COMPUTER.

The following are the possible switch settings and the resulting starting address for each:

	SP3 SWITCH POSITION:				STARTING ADDRESS:	
	1	2	3	4		
ADDRESS BIT:	A15	A14	A13	A12	DECIMAL	HEXIDECIMAL
	0	0	0	0	0	0000H
	0	0	0	1	4096 (4K)	1000H
	0	0	1	0	8192 (8K)	2000H
	0	0	1	1	12288 (12K)	3000H
0=OFF	0	1	0	0	16384 (16K)	4000H
	0	1	0	1	20480 (20K)	5000H
1=ON	0	1	1	0	24576 (24K)	6000H
	0	1	1	1	28672 (28K)	7000H
	1	0	0	0	32768 (32K)	8000H
	1	0	0	1	36864 (36K)	9000H
	1	0	1	0	40960 (40K)	A000H
	1	0	1	1	45056 (44K)	B000H
	1	1	0	0	49152 (48K)	C000H
	1	1	0	1	53248 (52K)	D000H
	1	1	1	0	57344 (56K)	E000H
	1	1	1	1	61440 (60K)	F000H

**********IMPORTANT**********

MOST "PROBLEMS" WITH MEMORY BOARDS RESULT FROM THE ADDRESS SWITCHES BEING SET INCORRECTLY. CHECK THESE SWITCHES CAREFULLY TO BE SURE THAT THE ADDRESS SPAN OF THE EPROM 32/64K DOES NOT OVERLAP WITH THE ADDRESS SPAN OF ANY OTHER BOARDS IN THE SYSTEM.

****

ALSO: If the starting address of the EPROM-32/64K is set to a sufficiently high value (eg. 9000H or higher for a fully updated board, the memory may extend over the 64K upper boundary of the global address space (ie. above FFFFH). This will cause the extra memory beyond FFFFH to wrap around and begin at 0000H.

2.2.2.2 SETTING THE BASE ADDRESS FOR EPROM-32/64K's THAT HAVE BEEN ALTERED FOR 64K OPERATION (USING 2732's).

If the board has been modified to use 2732's, the global address may **not** be set. In this case, the board's memory space begins automatically at the beginning of the 64K global address space. Switch SP3 has **no effect.** However, before you become furious and decide to return the board, please read further:

The board **may** be made to have memory starting on any 8K boundary by installing EPROMS only where you need them, and setting switch SP4 accordingly (see section 2.2.7), to disable the 8K blocks of address space where EPROMS are not used.

Furthermore, extended addressing or bank select may be used to enable or disable the EPROM board. Hence, the modified EPROM board can still be made to occupy only the address desired, and **not** the entire address space.

Finally, the modified board will no longer be usable with RAM chips, as a read/write memory, since the write line which would have been used by these chips is now occupied as the address line A11.

2.2.3 WAIT STATE (OPTIONAL, SP1 POSITION 6) "WAIT"

The WAIT switch is used to add an optional wait state, which is required when using 300nS or slower EPROMS in 4MHz systems. The memories will run in virtually all systems with 1 wait state. THEREFORE, THE WAIT SWITCH SHOULD BE SET TO ON IN MOST CASES. When this switch is turned to ON, it will cause the read or write cycle generated by the computer to be lengthened by one clock cycle.

2.2.4 PHANTOM DESELECT (SWITCH SP1 POSITION 5) "PHN"

This switch, when turned ON will cause the EPROM 32/64K to be deselected when the PHANTOM line on the S-100 bus is activated. If your system requires that the read/write memory be deselected in response to PHANTOM, this switch should be turned ON. OTHERWISE, PHN SHOULD BE SET TO OFF.

2.2.5 SETTING FOR 8-BIT OR 8/16-BIT OPERATION (SP1, POS 8) "16EN"

This switch, when ON allows the EPROM-32/64K to transfer data to the new 16-bit CPU's in either 8-bit or 16-bit chunks. When SXTRQ is asserted while the board is addressed, and the 16EN switch is ON, the board will assert SIXTN (sixteen acknowledge) on the bus, and will transfer data in one 16-bit word. Generally speaking:

IF YOU HAVE AN 8-BIT SYSTEM (EG. z-80), SWITCH "16EN" SHOULD ALWAYS BE TURNED OFF.
IF YOU HAVE A 16-BIT SYSTEM (EG. 8086, z-8000 or 68000) "16EN" SHOULD BE TURNED ON.

2.2.6 ENABLING AND DISABLING BLOCKS OF MEMORY. (SWITCH SP4 POSITIONS 1 THROUGH 8) "BLK"

2.2.6.1. Factory configured board (using 2716's)

In a factory configured (32K) board, switch SP4 is used to enable or disable 4K byte blocks of memory. Switch positions 1 through 8 correspond to memory blocks 7 through 0, respectively. When a switch is ON, its corresponding block is enabled. When OFF, its block is disabled. Block 0 is the lowest 4096 bytes of memory on the board. Block 1 is the next, and so on. In a board populated with only 1 pair of EPROMS (1 column filled), only 1 block would be enabled. In a board populated with all 8 pairs, all 8 blocks (blocks 1 - 8) would be enabled.

The most common reason for disabling a block of memory is to create a "hole" in the memory address space to make room for a memory-mapped I/O device (eg. a disk controller).

2.2.6.2. Board modified for 2732's

In a modified board, switch SP4 is used, as before, to enable or disable blocks of memory, except in this case, the switch inherently enables or disables 8K byte blocks, instead of 4K byte blocks. Otherwise the operation of SP4 is the same as for the factory configuration.

2.2.7 SETTING THE FACTORY-CONFIGURED BOARD (32K) FOR STANDARD "GLOBAL" 16-BIT ADDRESSING (NON-EXTENDED ADDRESSING)

In the majority of S-100 systems, the computer only needs to address a maximum of 64K bytes of memory. For these cases, extended addressing and bank select need not, AND SHOULD NOT, be used. To be sure that they are not invoked, the following switches should be turned off:

BANK SELECT ENABLE (SP1 POS. 2-"BNK") = OFF
EXTENDED ADDR. ENABLE (SP1 POS. 1 - "XAD") = OFF

In this mode, there is no need to set switch SP5 as well as "ENA" or "DIS" of SP1, since their positions are not important.

An example of the switch settings for a system that is set up for simple 16 bit addressing is shown in figure 4. In this case, the user is configuring an EPROM board as follows:

STARTING ADDRESS AT 32768 (8000 IN HEXADECIMAL)
ONE WAIT STATE
NO PHANTOM
8-BIT MACHINE
EPROMS INSTALLED AT BLOCKS 0, 1, AND 3.

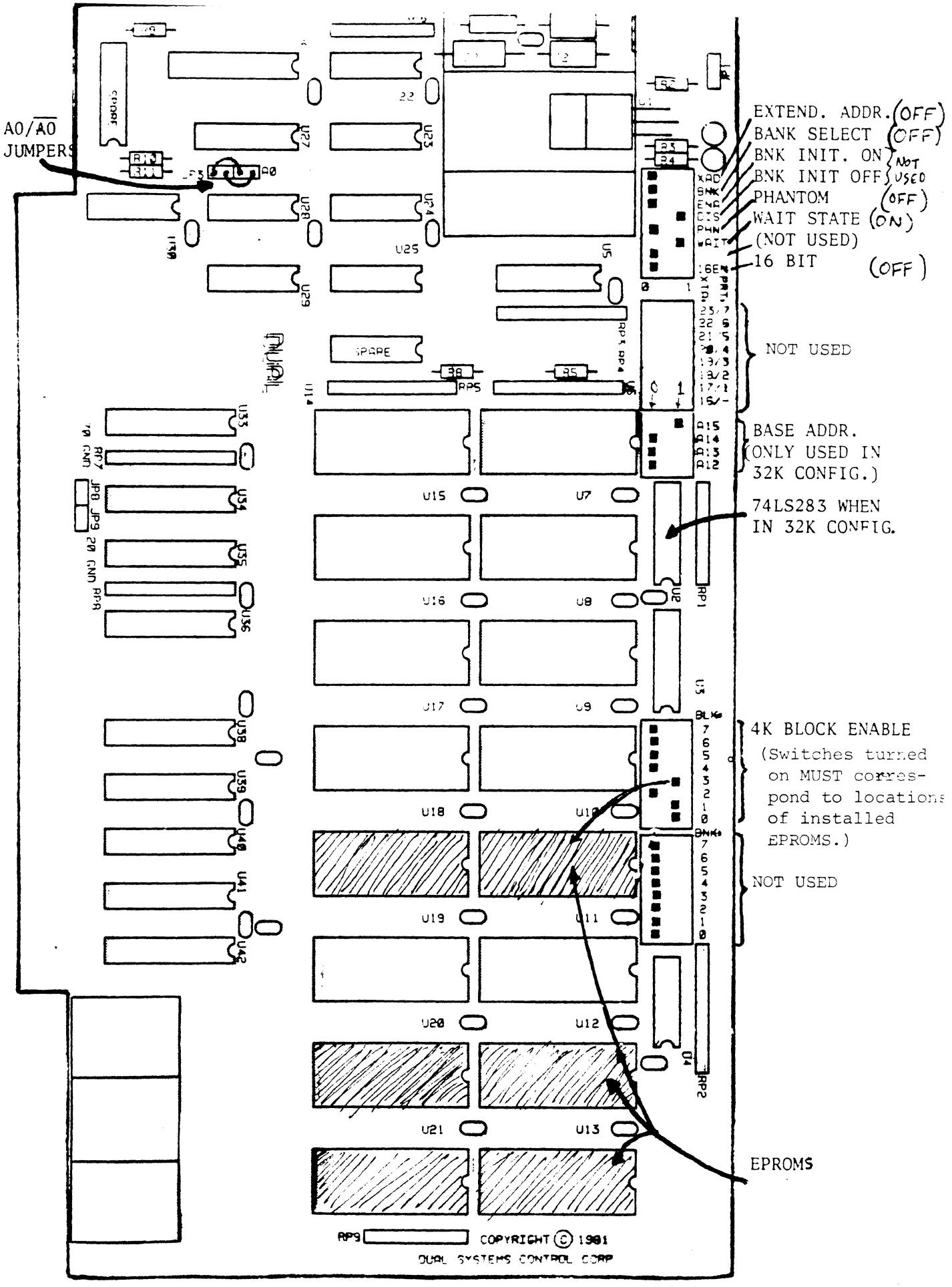


Figure 4. Example of simplest configuration of EPROM-32/64K

2.2.8 SETTING FOR 24-BIT EXTENDED ADDRESSING

If your computer system allows 24-bit extended addressing (as specified in the IEEE proposed S-100 standard), the EPROM 32/64K may be located in any 64K byte section in the 16 megabyte address space. To use EXTENDED ADDRESSING, SET SWITCH SP1 POS. 1 (XAD) to ON, and set SP1 POS. 2 (BNK) to OFF. Then, the extended address bits A16 through A23 may be set on switch SP2 (Positions 1 through 8 respectively). The board will then be selected in use any time the address bits A16 through A23 match the switch settings of SP2 positions 1 through 8, respectively (assuming, of course, that the global address bits also match, and the correct 4K (or 8K) blocks are enabled.)

As an example, if you would like a EPROM 32/64K to be accessed in the address range of:

260000 through 267FFF (Hexadecimal)

then switch SP 2 should be set to 26 (Hex.) which is 00100110 in binary. Also, A12 through A15 should be set to 0000 (binary) for this example, using switch SP 3 positions 1 through 4. THE SWITCH SETTINGS FOR THIS EXACT EXAMPLE ARE ILLUSTRATED IN FIGURE 5. THIS FIGURE DEPICTS THE FOLLOWING HYPOTHETICAL CONFIGURATION OF AN EPROM-32/64K SET UP FOR EXTENDED ADDRESSING:

16 BIT COMPUTER
ONE WAIT STATES
NO PHANTOM DISABLE
EXTENDED STARTING ADDRESS OF 260000 (Hex.)
FACTORY CONFIGURATION OF EPROM BOARD (For 2716's)

Note that switch SP2 sets the address of the BANK SELECT PORT or the EXTENDED ADDRESS, whichever mode was chosen via "BNK" or "XAD".

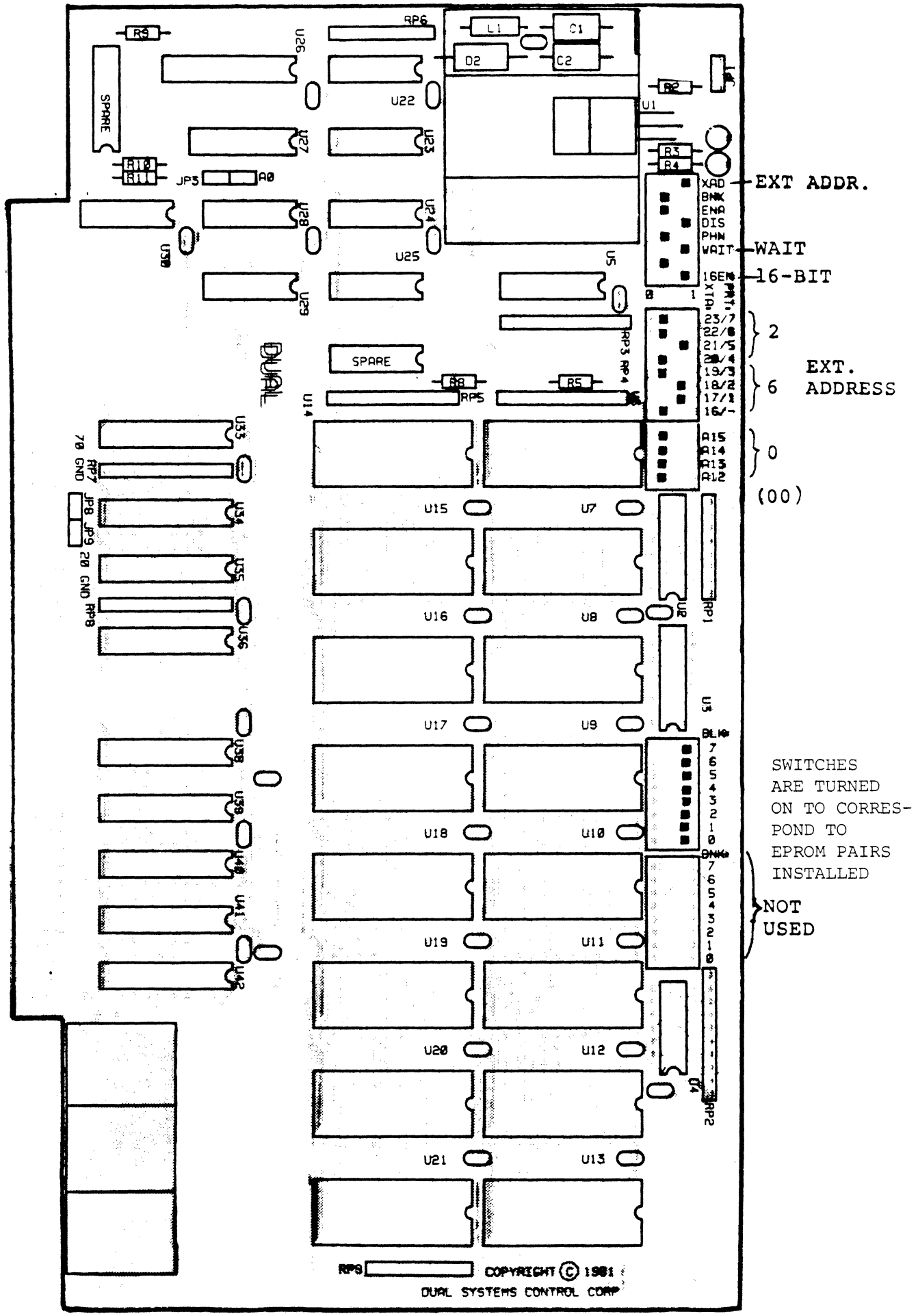


Figure 5. Example of board set up for 24-bit extended addressing in a 16-bit computer system

2.2.9 SETTING FOR BANK SELECT

Bank select is used in many large "pre-IEEE standard" S-100 systems. In this scheme, memory is organized in up to eight 64K byte memory BANKS (Bank 0 through Bank 7). This allows up to 512K bytes (8 x 64K) to be addressed by the CPU.

One or more EPROM 32/64K cards can be set to appear in a given bank (as long as the total memory in the bank does not exceed 64K bytes). Also, a EPROM 32/64K can be set to appear in more than one bank. Memory banks are activated and deactivated under software control via the bank select output port. Switch SP5 determines which bank(s) the board appears in. Switch SP2 is used to specify the I/O address of the bank select output port. THIS ADDRESS MUST BE EVEN and is often set to 40 (Hex.)

Setting SP5 so that a given bank is in the ON position places the board in that bank. In operation, when the computer outputs a byte to the bank select output port, the board is either activated or disabled, depending on whether this byte has a 1 or 0 at the bit corresponding to the switch that is in the ON position. For example, suppose the address of the bank select output port is set to 40 (hex) via switch SP2, and the EPRM 32/64K is set, via SP5, to reside in banks 0 and 4, as shown in figure 6. Then, any time the computer outputs a byte to port 40, shich has a 1 in either bits D0 or D4, the bank containing the board is enabled, and it may now be addressed as if it were in a global (64K byte) address space. Later, if a new byte is sent to port 40, which has binary zeroes in both bits D0 and D4, the bank becomes deactivated and the board will not be enabled, regardless of the state of the "global" address bits A0 to A15.

BANK SELECT IS INVOKED BY SETTING SP 1 POS 2 (BNK) TO ON
AND SETTING SP L1 POS 1 (XAD) TO OFF

The EPROM-32/64K board may be set to AUTOMATICALLY COME UP ENABLED when the computer is turned on (or a system reset occurs) by turning SP 1 POS 3 (ENA) to ON and POS. 4 (DIS) to OFF.

The board will come up DISABLED if DIS is set to ON, and ENA to OFF. DO NOT set BOTH DIS and ENA to ON at the same time.

Figure 6 shows an example of switch settings for a EPROM-32/64K set up for BANK SELECT, with the board set to appear in banks 0 and 4, and the BANK SELECT I/O PORT set for an address of 40(Hex.). The board is set to come up ENABLED in this example. For this example the following bytes are typical of data that could be outputted to I/O addr. 40 to ENABLE or DISABLE the board:

BINARY DATA:	D7	6	5	4	3	2	1	0	
TO ENABLE THE BOARD:	x	x	x	1	x	x	x	x	
	x	x	x	x	x	x	x	1	
	x	x	x	1	x	x	x	1	x=DON'T CARE
TO DISABLE THE BOARD:	x	x	x	0	x	x	x	0	

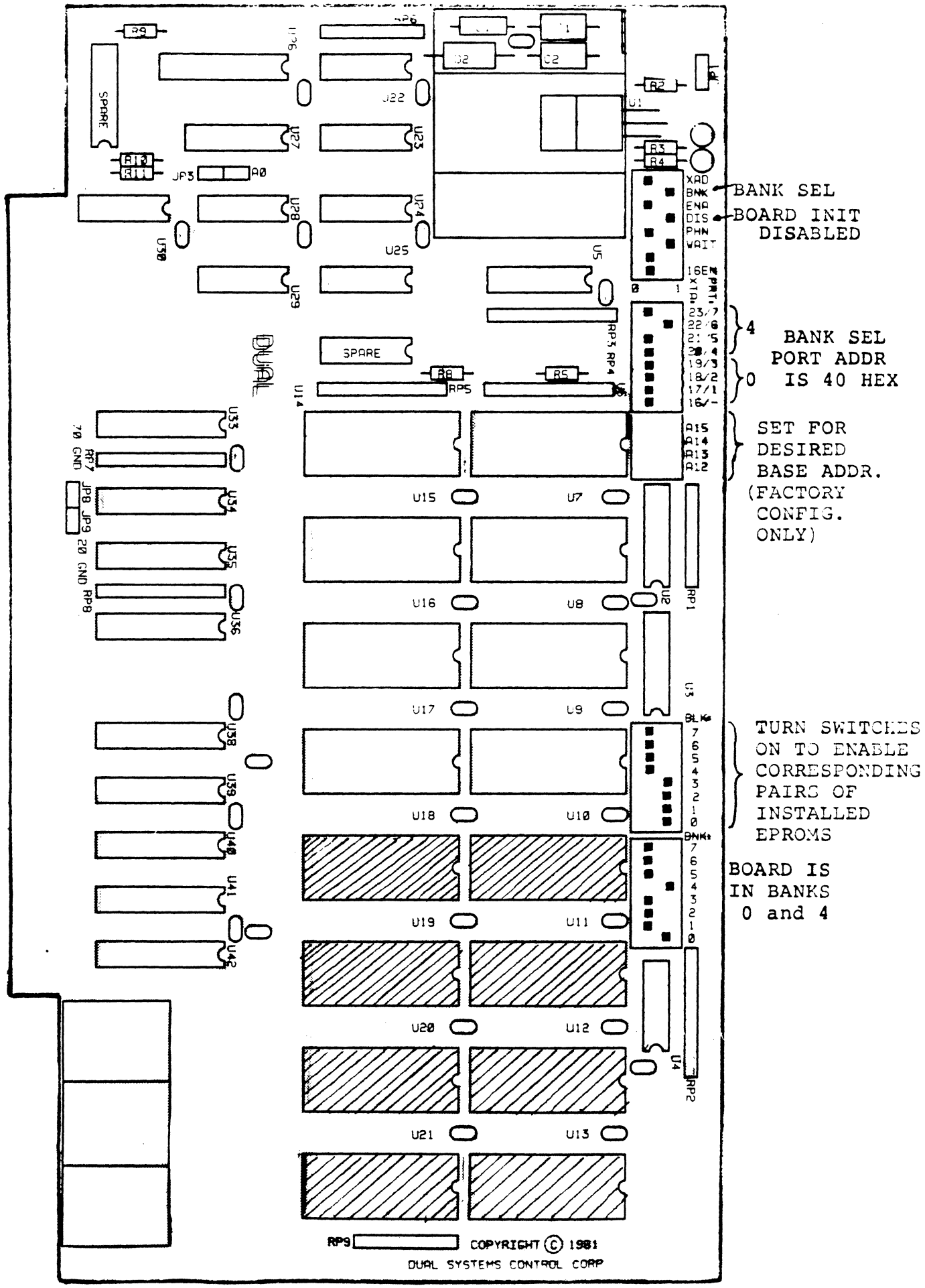


Figure 6. Example of board set up for bank select

2.2.10 A0 JUMPERS

The jumpers described in this section are ones which will rarely need to be changed from the factory settings. They are used as follows:

A0 CUTTABLE TRACES

The A0 jumpers (JP3) are only important in 16 bit computer systems which mix 8 and 16 bit data transfers. The traces are connected in such a way that the EPROM 32/64K meets the IEEE-696 proposed S-100 standard, which requires the following relationship between BYTE and 16-bit WORD addressing:

DURING 16-BIT TRANSFERS, THE BYTE GATED TO THE "DO" BUS SHOULD HAVE AN EVEN ADDRESS (A0=0)

DURING 16-BIT TRANSFERS, THE BYTE GATED TO THE "DI" BUS SHOULD HAVE AN ODD ADDRESS (A0=1)

The proposed standard was changed during its development. Prior to this change, the standard was just the opposite of the above. If the EPROM-32/64K is used with a CPU board which follows the obsolete convention, jumpers JP3 may be changed so that the byte gated to the DO bus will be at an ODD address (instead of even), and the byte gated to the DI bus will have an EVEN address. In this unlikely case, the A0 jumpers may be changed as shown below.

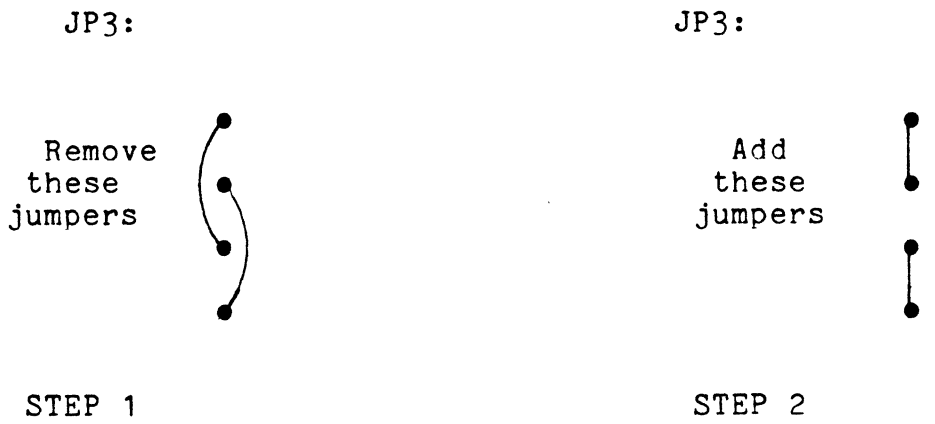


Figure 7. Reversing the order of the EVEN and ODD bytes.

2.3 Installing the EPROMS

After being sure that all of the switches and jumpers have been correctly set, the (suitably programmed) EPROMS may be installed. The EPROMS must be installed in pairs (one in the top row, and one in the bottom).

In 16-bit systems, the EPROM in the bottom row normally contains the MOST significant 8 bits of the word, and the EPROM in the top row contains the LEAST significant 8 bits. NOTE: with some CPU's this order is reversed.

In 8-bit systems, the EPROM in the bottom row normally contains the EVEN addressed bytes (addresses 0, 2, 4, 6, ... etc) while the top row EPROM contains the ODD bytes.

The addresses which correspond to the various EPROM socket locations are shown in figure 1 (Factory configuration) and figure 3 (Alternate configuration, using 2732's.

Install the EPROM pairs (or RAM pairs) in the desired sockets, as illustrated in figure 1 or 3, whichever is applicable. For each pair of installed chips, the corresponding switch location should be turned on. See figure . All other switches (corresponding to vacant pairs of sockets) should be turned OFF.

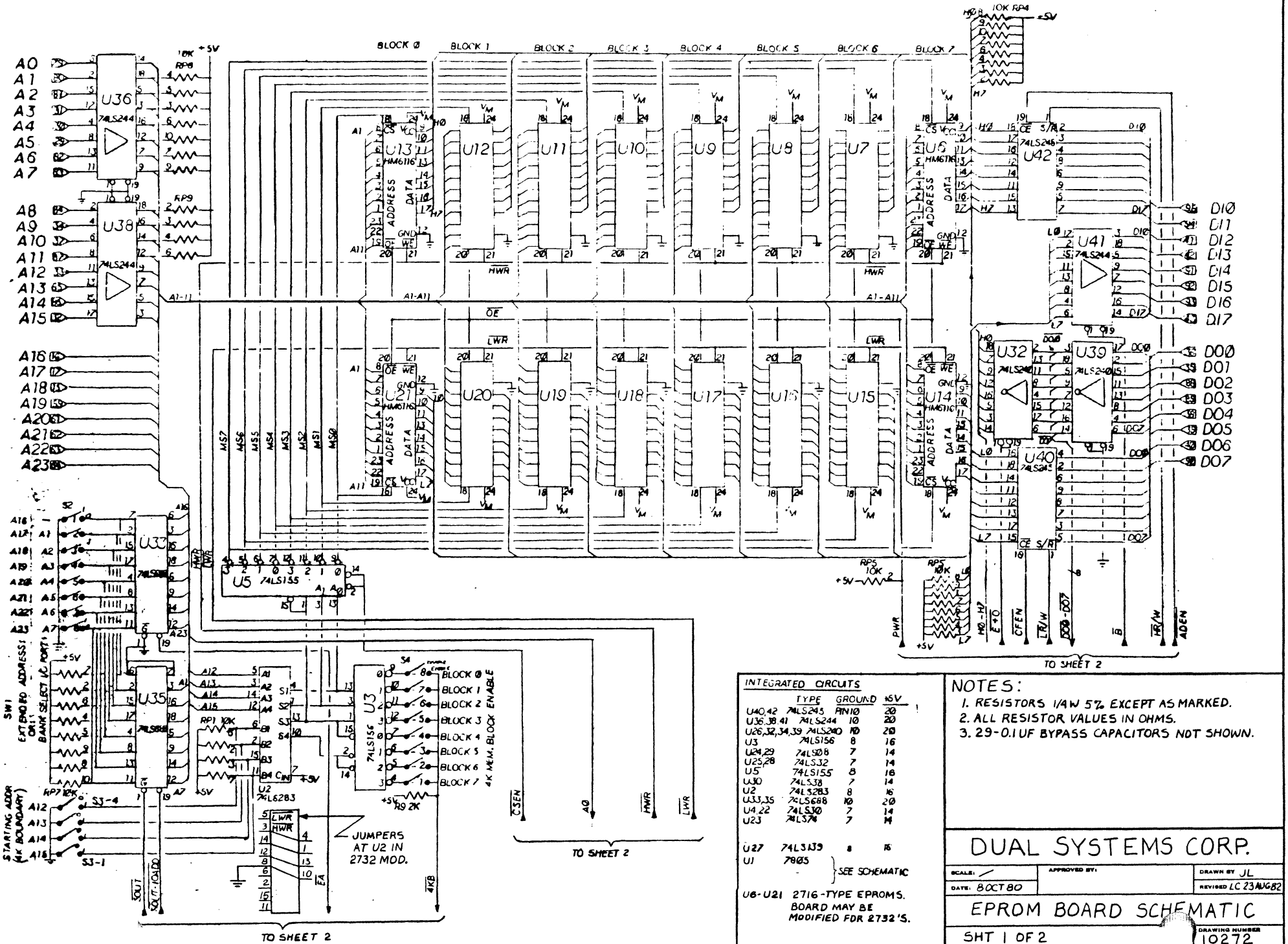
Before installing the board into the computer system, check the following.

1.) Are the EPROMS installed with pin 1 facing the right way?

2.) Are the switches on the board set correctly so that the base address does not conflict with the address range of other boards in the system?

3.) Is the system power OFF? NO BOARD SHOULD EVER BE REMOVED OR INSERTED INTO THE CARD SLOTS WITH THE POWER ON.

The board may now be installed into the system.



INTEGRATED CIRCUITS	TYPE	GROUND	+5V
U40,42	74LS245	PIN 10	20
U36,38,41	74LS244	10	20
U26,32,34,39	74LS240	10	20
U3	74LS156	8	16
U24,29	74LS08	7	14
U25,28	74LS32	7	14
U5	74LS155	8	16
U30	74LS38	7	14
U2	74LS283	8	16
U33,35	74LS688	10	20
U4,22	74LS30	7	14
U23	74LS74	7	14
U27	74LS139	8	16
U1	7805		SEE SCHEMATIC

U6-U21 2716-TYPE EPROMS. BOARD MAY BE MODIFIED FOR 2732'S.

NOTES:
1. RESISTORS 1/4W 5% EXCEPT AS MARKED.
2. ALL RESISTOR VALUES IN OHMS.
3. 29-0.1 UF BYPASS CAPACITORS NOT SHOWN.

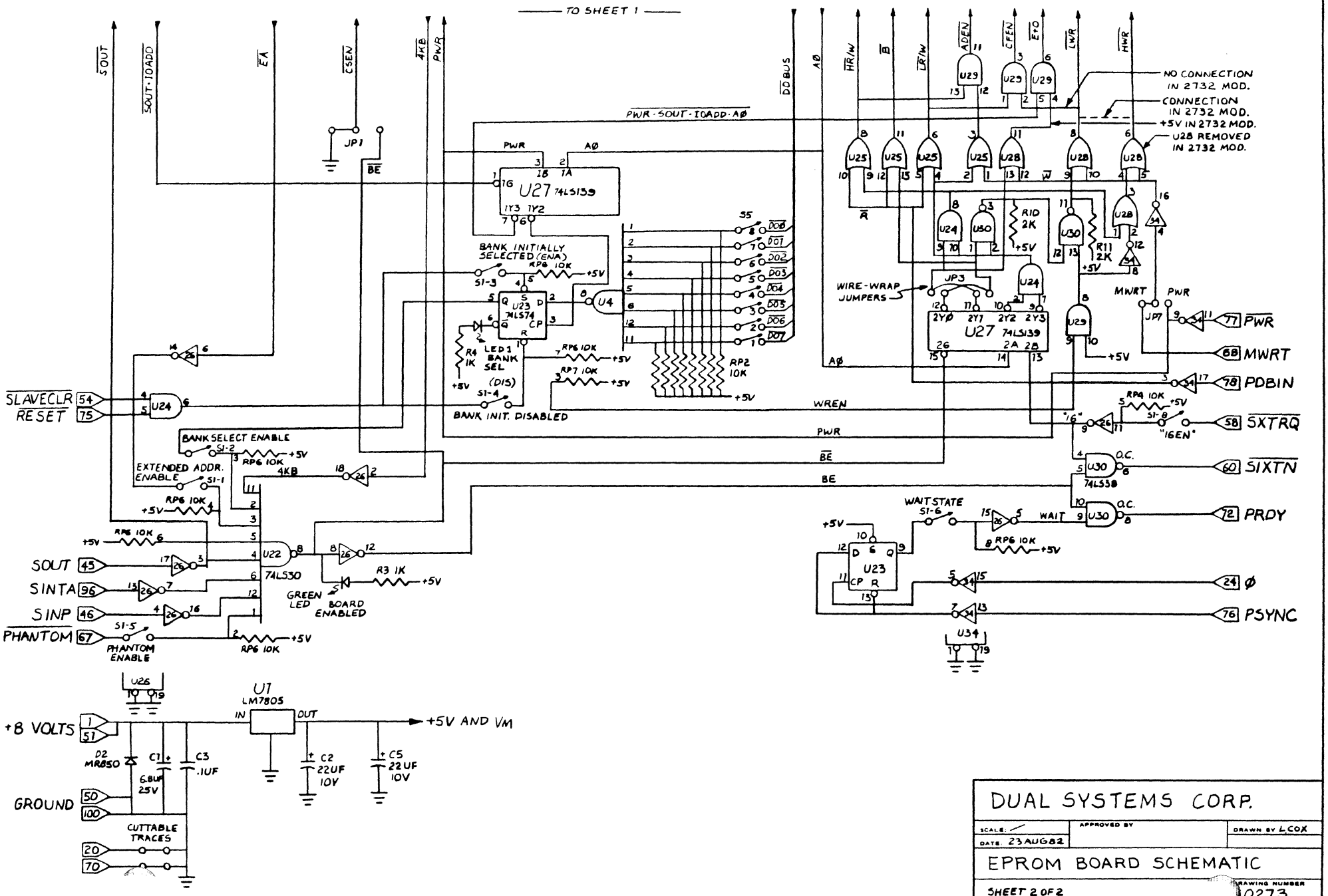
DUAL SYSTEMS CORP.

SCALE:	APPROVED BY:	DRAWN BY JL
DATE: 8 OCT 80		REVISED LC 23 AUG 82

EPROM BOARD SCHEMATIC

SHT 1 OF 2

DRAWING NUMBER 10272



DUAL SYSTEMS CORP.		
SCALE:	APPROVED BY	DRAWN BY L.COX
DATE: 23AUG82		
EPROM BOARD SCHEMATIC		
SHEET 2 OF 2		DRAWING NUMBER 0273

Warranty and Service

Dual Systems Control Corporation guarantees its products, under normal use and service as described in the manufacturer's product literature, free from defects in material and workmanship, for a period of one year from date of shipment. This warranty is limited to the repair or replacement of the product, or any part of the product found to be defective at the manufacturer's factory, when returned to Dual Systems Control Corporation, transportation charges prepaid by customer. This warranty does not apply to any equipment that has been repaired or altered, except by Dual Systems Control Corporation, or which has been misused or damaged by accident. In no case shall the manufacturer's liability exceed the original cost of the product.