ECMA

EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION

STANDARD ECMA-39

FOR

TRACK FORMAT CHARACTERISTICS
OF INTERCHANGEABLE
SINGLE DISK CARTRIDGES
(TOP LOADED)

Free copies of this **ECMA** standard are available from ECMA European Computer Manufacturers Association 114 Rue du Rhône - 1204 Geneva (Switzerland)

ECMA EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION

STANDARD ECMA-39

FOR

TRACK FORMAT CHARACTERISTICS OF INTERCHANGEABLE SINGLE DISK CARTRIDGES (TOP LOADED)

BRIEF HISTORY

On April 30, 1965, ECMA adopted their Standard ECMA-6 for a 7-Bit Coded Character Set for Input and Output purposes. In the form adopted, it included no proposals for implementation in media which were deliberately left as the subject for specific standards.

Standard ECMA-38 defines the mechanical, physical and magnetic characteristics for interchange of Single Disk Cartridges. This Standard ECMA-39, prepared by ECMA TC16, is directed to the Track Format Characteristics for data interchange on such disk cartridges.

It has been adopted by the General Assembly of ECMA on June 15, 1973.

TABLE OF CONTENTS

	TRACK FORMAT CHARACTERISTICS	Page
1.	General Requirements	1
	1.1 Rotation Speed and Clock Frequency 1.2 Mode of Recording 1.3 Index 1.4 Track Capacity 1.5 Track Layout	1 1 1 1
2.	Definition of Terms	1
	<pre>2.1 Sector 2.2 Sector ZERO 2.3 Data Sectors 2.4 Identifier 2.5 Data Block 2.6 Gap 2.7 Byte 2.8 Hexadecimal Notation 2.9 Error Detection Characters (EDC)</pre>	1 1 2 2 2 2 2 2 2
3.	Detailed Description of Track Layout	2
	3.1 Sector ZERO 3.2 Data Sector	2 4
	Drawings: Fig. 1 - 4	7
	APPENDICES	9
App	endix A - Rotational Speed and Clock Frequency Tolerance	11
App	endix B - Minimum Data Capacity	13
App	endix C - Index Slot Detection Tolerance	15
App	endix D - Factors Affecting Data Interchange	19
App	endix E - EDC Implementation	21

1. GENERAL REQUIREMENTS

1.1 Rotation Speed and Clock Frequency

The total tolerance on rotation speed + clock frequency shall not exceed \pm 3% (see Appendix A).

1.2 Mode of Recording

The mode of recording shall be double frequency where the start of every bit cell is a clock transition. A ONE is represented by a transition between two clock transitions.

At the nominal rotational speed of 2400 rpm the all ZERO pattern consists of 2,50 . 10^6 transitions per second nominally and the all ONES pattern consists of 5,0 . 10^6 transitions per second nominally.

$1.3 \quad \underline{\text{Inde x}}$

The index is the point which determines the beginning and the end of the track. Its nominal location is specified in Sec. III, 1.2.5 of Standard ECMA-38. A tolerance of \pm 12,5 bytes is applied to this position (see Appendix C).

1.4 Track Capacity

The capacity of a track is 62500 + 1933 bits (see also Appendix B).

1.5 Track Layout

Figure 1 shows the general track layout.

2. DEFINITION OF TERMS

2.1 Sector

A track is divided into sectors. A sector may be further subdivided.

2.2 Sector ZERO

The Sector ZERO contains information which defines the physical location and characteristics of a track.

2.3 Data Sectors

Each data sector is composed of an Identifier and a Data Block.

2.4 Identifier

The Identifier contains information which defines the physical location and characteristics of a sector.

2.5 Data Block

Part of a sector in which data is recorded.

2.6 Gap

A gap is the space between the various divisions of a track.

2.7 Byte

A byte is a group of eight bit-positions, identified B8 to B1 with B8 most significant and recorded first. The bit in each bit-position is a ZERO or a ONE.

2.8 Hexadecimal Notation

Hexadecimal notation is used hereafter to denote a number of typical bytes:

- (00) for (B8 to B1) = 00000000
- (01) for (B8 to B1) = 00000001
- (FF) for (B8 to B1) = 111111111
- (CC) for (B8 to B1) = 11001100
- (09) for (B8 to B1) = 00001001
- (14) for (B8 to B1) = 00010100
- (OB) for (B8 to B1) = 00001011
- (OF) for (B8 to B1) = 00001111
- (F2) * for (B8 to B1) = 11110010

2.9 Error Detection Characters (EDC)

The two EDC bytes consist of the remainder formed by dividing the relevant bytes defined later in this specification by the polynomial:

$$x^{16} + x^{15} + x^{2} + 1$$

(see also Appendix E: EDC implementation).

3. DETAILED DESCRIPTION OF TRACK LAYOUT

3.1 Sector ZERO

The first sector following Index is unique in that it contains a Track Identifier and will therefore be described separately. Fig. 2 shows the Sector ZERO layout.

 $[^]st$ where the clock transitions of B6 and B5 are missing.

3.1.1 Index Gap

he

er

on-

This is a gap preceding the track identifier and must be written so that the start of the track identifier is located within (65 ± 12,5) bytes from Index. It is also a requirement that when this gap is initially written, 65 bytes of (FF) shall precede the track identifier. The first 25 bytes of (FF) may, as a result of interchange, be unreadable (see Appendix C).

3.1.2 Track Identifier

The Track Identifier consists of 16 bytes as follows:

- 3.1.2.1 Synchronization (8 bytes) as follows:
 - (00) (00) (00) (00) (FF) (F2)* (F2)* (09)

The first two bits in (B8 and B7) are always ZERO. B6 to B3 are reserved for future standardization and contain all a ZERO.

- B2 B1 = ZERO ZERO indicates good original track
- B2 B1 = ZERO ONE indicates good alternative track
- B2 B1 = ONE ZERO indicates defective track, alternative has been allocated.
- B2 B1 = ONE ONE indicates defective track, no alternative has been allocated.
- 3.1.2.3 C Cylinder (2 bytes) These specify in binary the address of the cylinder.
- 3.1.2.4 H Head (1 byte) This specifies in binary the address of a track within a cylinder. The byte can be either a (00) or a (01) byte.
- 3.1.2.5 NS Number of Sectors (1 byte) This specifies in binary the number of data sectors in a track. For interchange purposes this byte is a (14) byte.
- 3.1.2.6 Error Detection Characters (2 bytes). The bytes defined in 3.1.2.2 to 3.1.2.5 are divided by the polynomial specified in 2.9.
- 3.1.2.7 The track identifier ends with one byte (CC).

3.1.3 Track Identifier Gap

A 36 bytes gap of (FF) is initially recorded between the end of the track identifier and the start of sector ONE. The contents of this gap may subsequently become undefined because of repeated writing operations.

3.2 Data Sector

3.2.1 Identifier

The Identifier is composed of 18 bytes. Fig. 3 shows the Identifier layout. The Identifier is as follows:

3.2.1.1 Synchronization (8 bytes) as follows:

(00) (00) (00) (FF) (F2)* (F2)* (OB)

3.2.1.2 F - Flag (1 byte) - This is used in each identifier for certain control and checking operations and can be used to indicate defective and alternative tracks. The significance of the bits in this byte is as follows:

B8 = ONE for the first sector following the track identifier sector and alternative sectors thereafter, and

B8 = ZERO for the other sectors.

B7 to B3 are reserved for future standardization and contain all a ZERO.

Bl to B2 see 3.1.2.2.

- 3.2.1.3 C and H Cylinder and Head (3 bytes) These bytes are identical to those in sector ZERO except when appearing on defective or alternative tracks. On a defective track cylinder and head bytes C and H contain the cylinder and head number of the alternative track if the flag bits Bl and B2 are ONE and ZERO respectively. On an alternative track C and H contain cylinder and head number of the defective track which it replaces.
- 3.2.1.4 S Sector (1 byte) It is used to identify sectors on the track. For the first sector after sector ZER this byte is a (01) byte, and the subsequent sectors will be numbered consecutively.
- 3.2.1.5 DL Data Length (2 bytes) These specify in binary the number of information bytes in the data sector.

For interchange purposes the data length will be 256 bytes.

- 3.2.1.6 Error Detection Characters (2 bytes). The bytes defined in 3.2.1.2 to 3.2.1.5 are divided by the polynomial specified in 2.9.
- 3.2.1.7 The identifier ends with one byte of (CC).

3.2.2 Identifier Gap

A 34-byte gap of (FF) is initially recorded between the end of the identifier block and the start of the data block. The contents of this gap may subsequently become undefined because of repeated writing operations.

3.2.3 Data Block

)

S

ck ors

n

erna[.] mber

ctors

ctors

inar; tor.

e

е

ZER(

The data block consists of (DL + 12) bytes, where DL is the number of information bytes (see 3.2.1.5). Fig. 4 shows the data block layout.

The data block is as follows:

3.2.3.1 Synchronization (8 bytes) as follows:

(00) (00) (00) (FF) (F2)* (F2)* (OF)

- 3.2.3.2 <u>Information</u> A number of information bytes as specified in the DL portion of the preceding identifier.
 - i) The characters are represented by means of the 7-bit coded character set (Standard ECMA-6) and, where required, by its 7-bit or 8-bit extensions (Standard ECMA-35);
 - ii) Each 7-bit coded character is recorded in bit position Bl to B7 of a byte; bit position B8 is recorded with value ZERO.

 The relationship is as follows:

Bits of the 7-bit combination	0	b 7	b6	b ₅	b ₄	b 3	b ₂	b ₁
Bit position in the byte	В8	В7	В6	B5	В4	В3	B2	В1

iii) Each 8-bit coded character is recorded in bit positions Bl to B8 of a byte.

The relationship is as follows:

Bits of the 8-bit combination	b ₈	b 7	b ₆	b ₅	b 4	b ₃	b	b	
Bit position in the byte	В8	В7	В6	B5	В4	B3	B2	B1	

3.2.3.3 DF - Data Flag byte - This is used in each data field and B8 = ONE indicates that the information in this data field is continued in the following sector.

 $\ensuremath{\mathsf{B7}}$ to $\ensuremath{\mathsf{B1}}$ are reserved for future standardization and are all ZERO.

3.2.3.4 Error Detection Characters. The bytes defined in

3.2.3.2 and 3.2.3.3 are divided by the polynomial specified in 2.9.

3.2.3.5 The data block ends with one byte (CC).

3.2.4 Data Block Gap

The gap between the end of the data block and the start of the next sector is initially recorded with (FF). Its initial length is:

$$36 + \frac{1}{-} DL$$

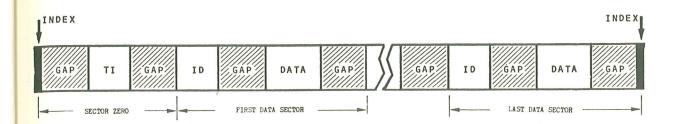
any fraction is truncated.

DL is the number of information bytes in the data block. The contents of this gap may subsequently become undefined because of repeated writing operations. The length of the gap may vary due to repeated writing operations, however, a minimum of 36 bytes shall always be present.

Note: For interchange purpose the length of this gap is initially 52 bytes.

3.2.5 Last Data Block Gap

The gap following the last sector will be recorded as (FF) until Index slot detection point. Under worst case conditions of disk speed and clock frequency and with maximum data capacity at least 11 bytes of (FF) shall be present (see Appendix C).



TI - TRACK IDENTIFIER

ID - IDENTIFIER

h

oe-

atytes

gap

d orst

of

DATA - DATA BLOCK

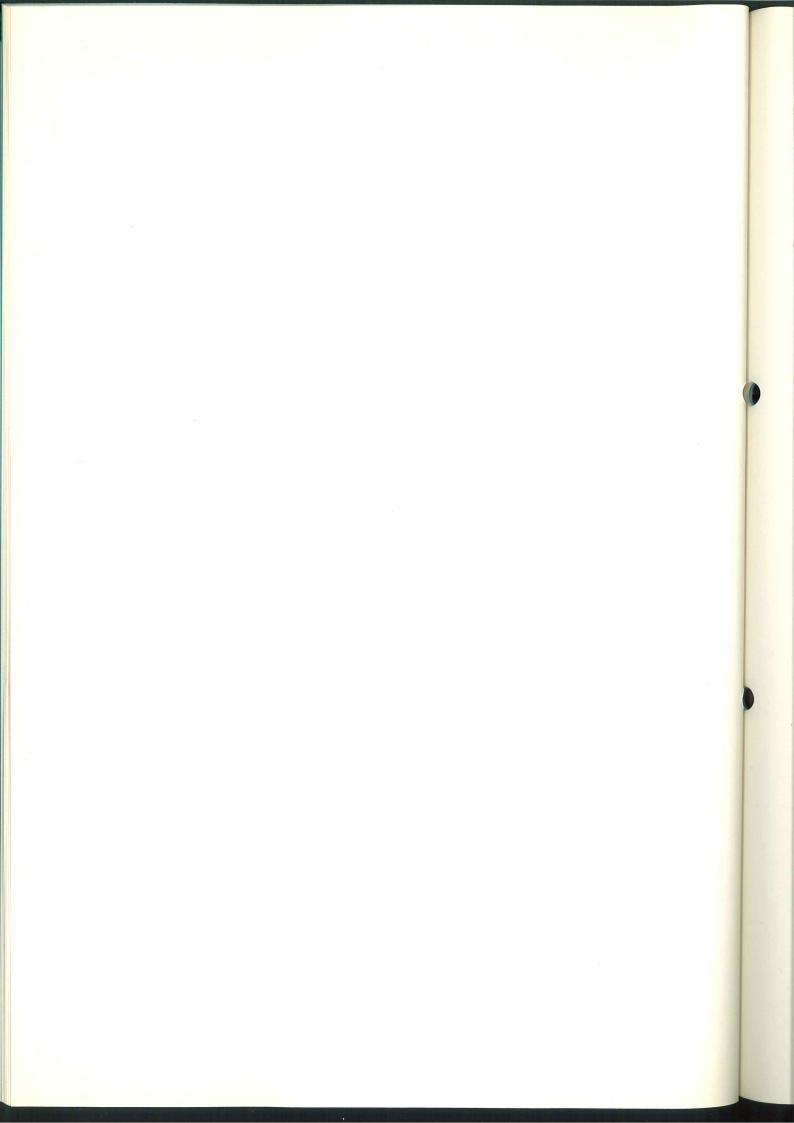
Fig. 1 GENERAL TRACK LAYOUT

INDEX 4 bytes | 1 byte | 2 bytes | 1 byte | F C C H NS 1 byte 36 bytes gap 2 bytes 65 bytes (09) (F2)* EDC (CC) (FF) (00) (FF) (FF) TRACK IDENTIFIER -Fig. 2 SECTOR ZERO LAYOUT

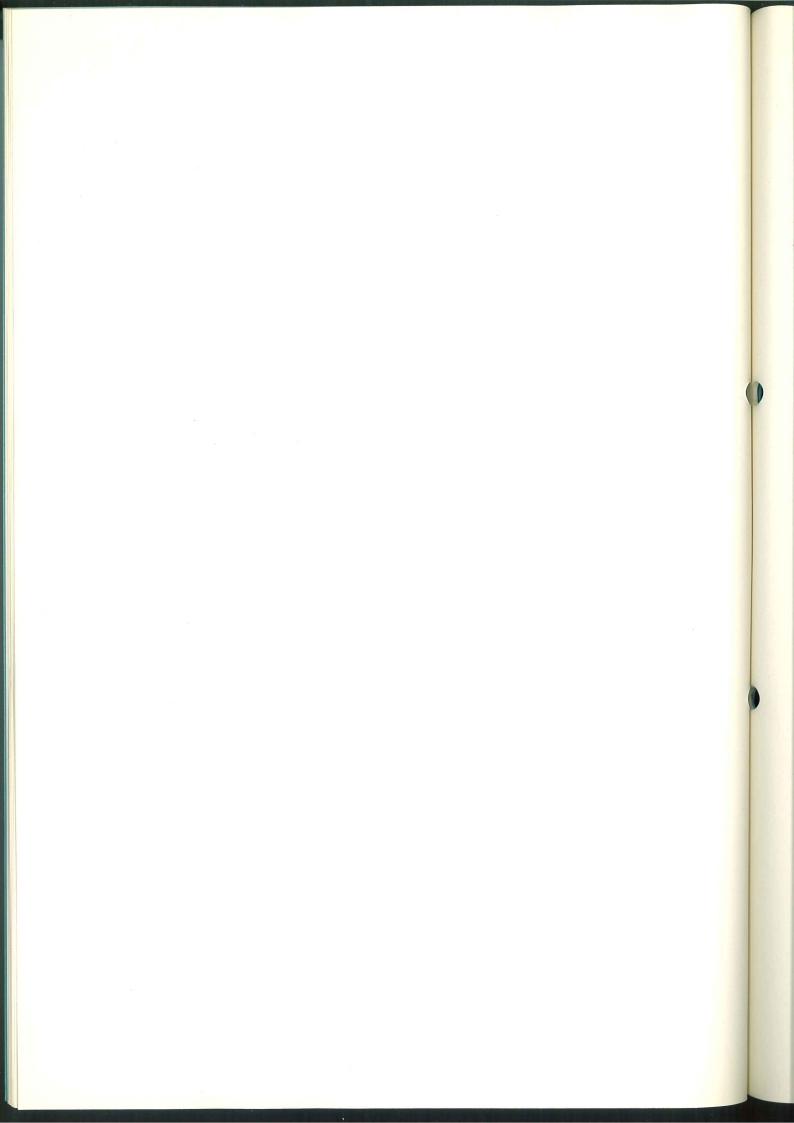
> 1 byte 34 bytes gap FCCHS 2 bytes 2 bytes Z bytes 1 byte 4 bytes 1 byte EDC (CC) (FF) (F2)* (OB) DL (00) (FF) - IDENTIFIER -Fig. 3 IDENTIFIER LAYOUT

4 bytes (00)	1 byte (FF)	2 bytes (F2)*	DL bytes informations	1 byte DF	2 bytes EDC	1 byte (CC)	36 bytes c minim (FF)	ap um
◀			 DATA BLOCK				- BLOCK	Fig.

DATA BLOCK LAYOUT



APPENDICES



APPENDIX A

ROTATIONAL SPEED AND CLOCK FREQUENCY TOLERANCE

If the nominal record length is L, the minimum record length is L1, the maximum record length is L2 and the tolerance is \mathbf{x} :

From 3.2.4 :

$$\frac{L2}{L1} = 1 + \frac{1}{16}$$

$$L1 = L - x$$

$$L2 = L + x$$

therefore

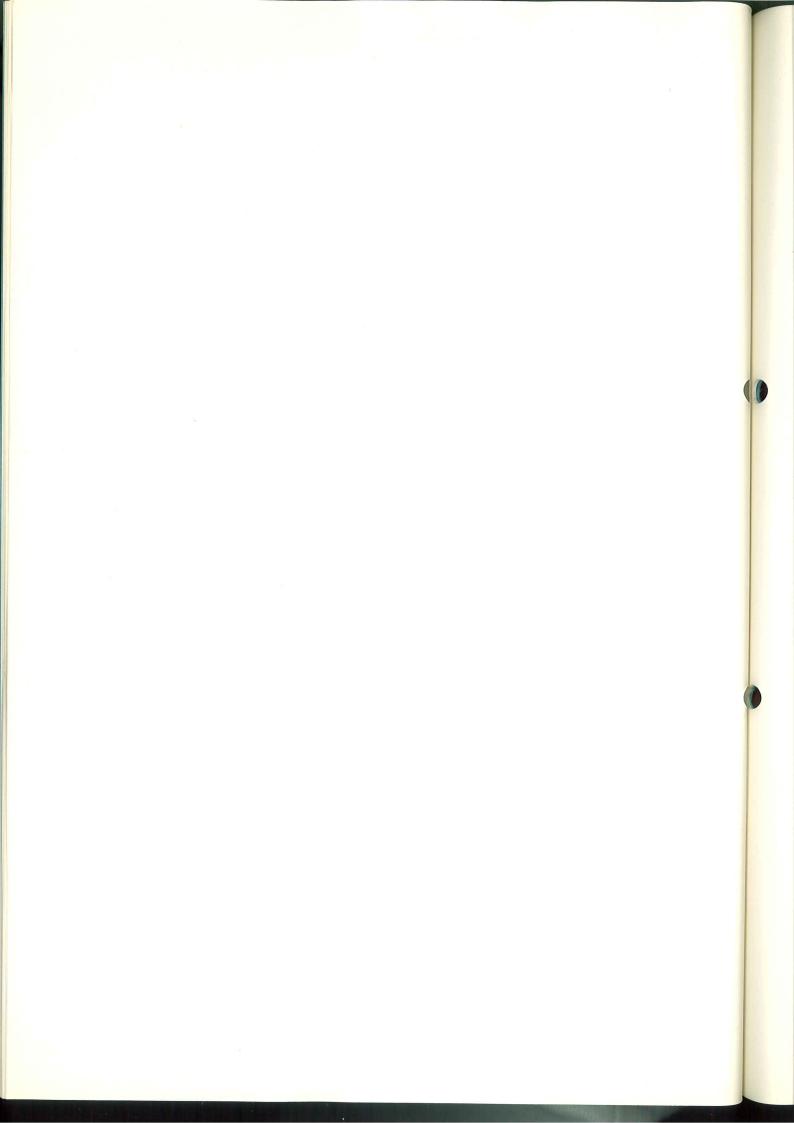
$$\frac{L + x}{L - x} = \frac{17}{16}$$

$$16L + 16x = 17L - 17x$$

$$33x = 1L$$

$$\frac{x}{L} = \frac{1}{33} = 3,03\%$$

Hence, 3,0% is used.



APPENDIX B

The minimum data capacity of a track may be calculated as follows:

- a) The minimum number of bytes in the track is 7585 bytes. This is derived from the following figures:
 - maximum rotational speed: 2472 rpm
 - bit cell frequency: $2,5 \cdot 10^6$.
- b) This capacity is allocated as follows:

Index gap 65 bytes Track Identifier 16 bytes Track Identifier gap 36 bytes

Identifier 18 bytes
Identifier gap 34 bytes
Data block 12 + DL bytes
Data block gap $36 + \frac{1}{16}$ DL bytes

$$n(100 + \frac{17}{16} DL)$$

where n is the number of data sectors in the track.

The following formula gives the maximum number of equal length sectors that can be accommodated on a track.

$$n(100 + \frac{17}{16} DL) - \frac{1}{16} DL \leqslant 7468$$

where the term $\frac{1}{16}$ DL compensates for the last data block gap.

Any fraction is truncated.

For data interchange purposes where DL = 256 the formula gives n = 20



APPENDIX C

INDEX SLOT DETECTION TOLERANCE

A tolerance is given for the location of the start of the Track Identifier with respect to Index to allow for equipment adjustment of the Index slot detection system.

The diagrams below show the effect, on the Index gap and the gap after the last sector, of the tolerance on Index slot detection under worst case conditions of disk speed and clock frequency with maximum data capacity.

The following cases are covered:

- A. This shows the location of the start of the Track Identifier and the end of the last sector with respect to Index when the Index slot is detected at its nominal position.
- B. As case A but with the Index slot detected early.
- C. As case A but with the Index slot detected late.
- D. This shows a track which was formatted as in case B being read by equipment which detects the Index slot late. For this equipment the Index gap is shortened to 40 bytes while the gap after the last sector is increased to 61 bytes.
- E. This shows a track which was formatted as in case C being read by equipment which detects the Index slot early. For this equipment the Index gap is lengthened to 90 bytes. The gap after the last sector is shortened to 11 bytes.

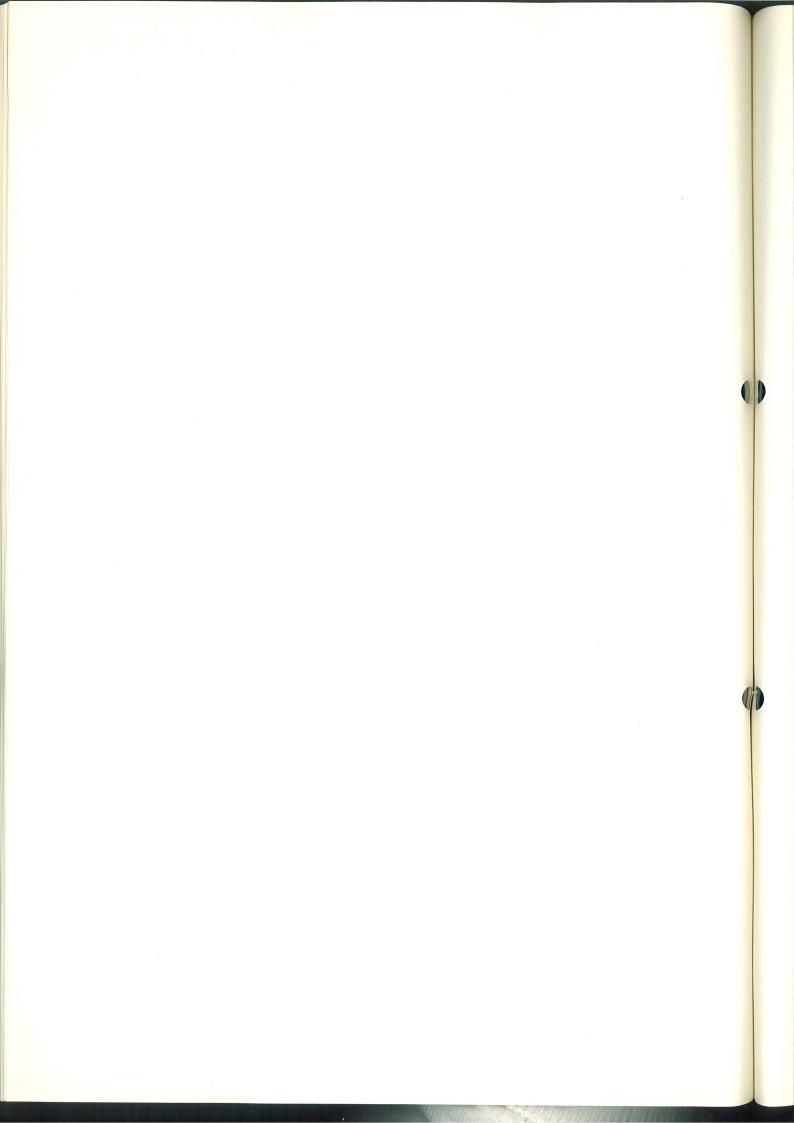
In the above only the extreme cases are shown; intermediate values of the tolerance on Index slot detection result in a situation where the first 25 bytes, read after the Index slot has been detected, cannot be guaranteed. It is therefore recommended that these 25 bytes should be treated as undefined.

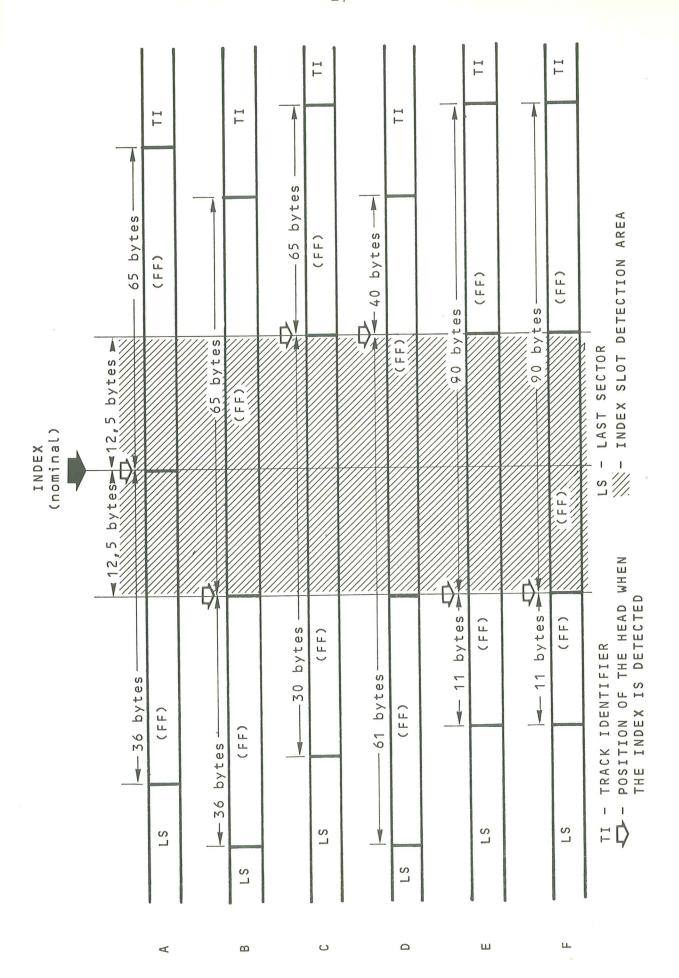
A further case is included which shows the conditions under which a minimum length gap after the last sector is written.

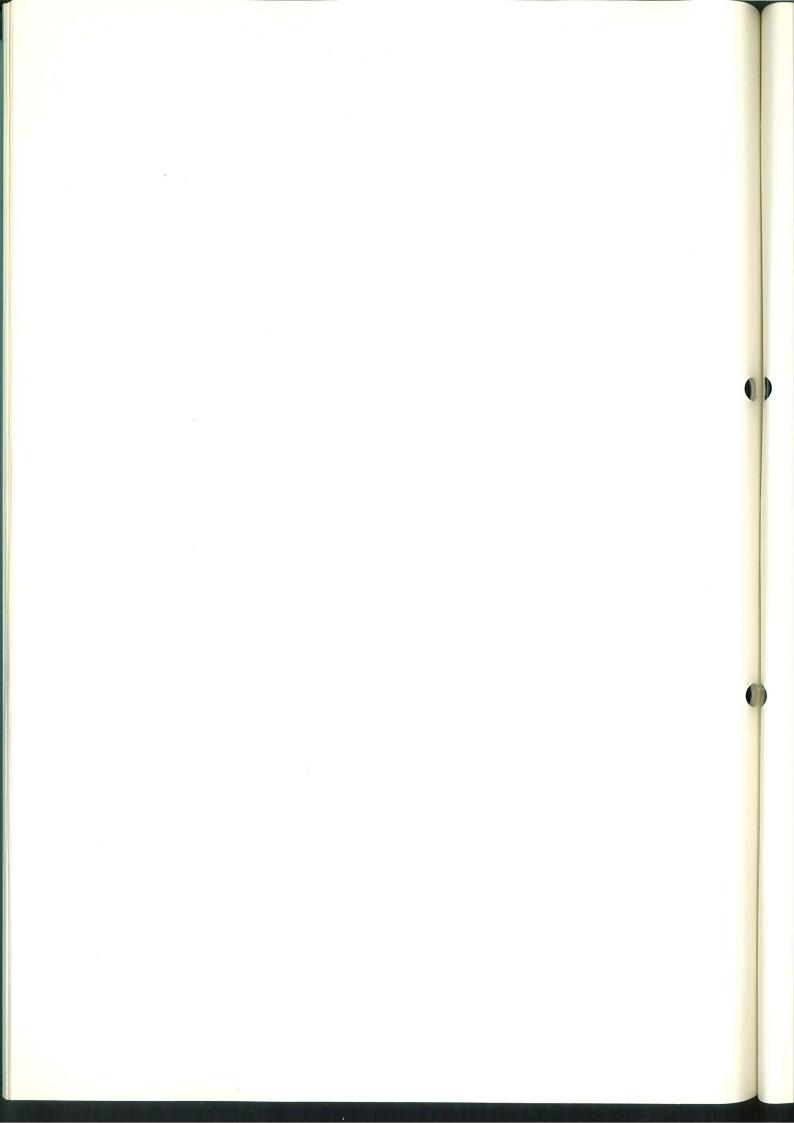
F. This shows a track which was partially formatted as in case C having the format completed, under worst case conditions of disk speed and clock frequency with maximum data capacity, by equipment which detects the Index slot early. The Index gap is lengthened to 90 bytes leaving only 11 bytes after the last sector before the Index slot is detected.

It should be noted that in all the above cases the minimum gap between the end of the last sector and the start of the track Identifier is 101 bytes.

NOTE: For the interchange standard of 256 bytes the gap after the last sector is increased by 44 bytes in all of the above cases.







APPENDIX D

FACTORS AFFECTING DATA INTERCHANGE

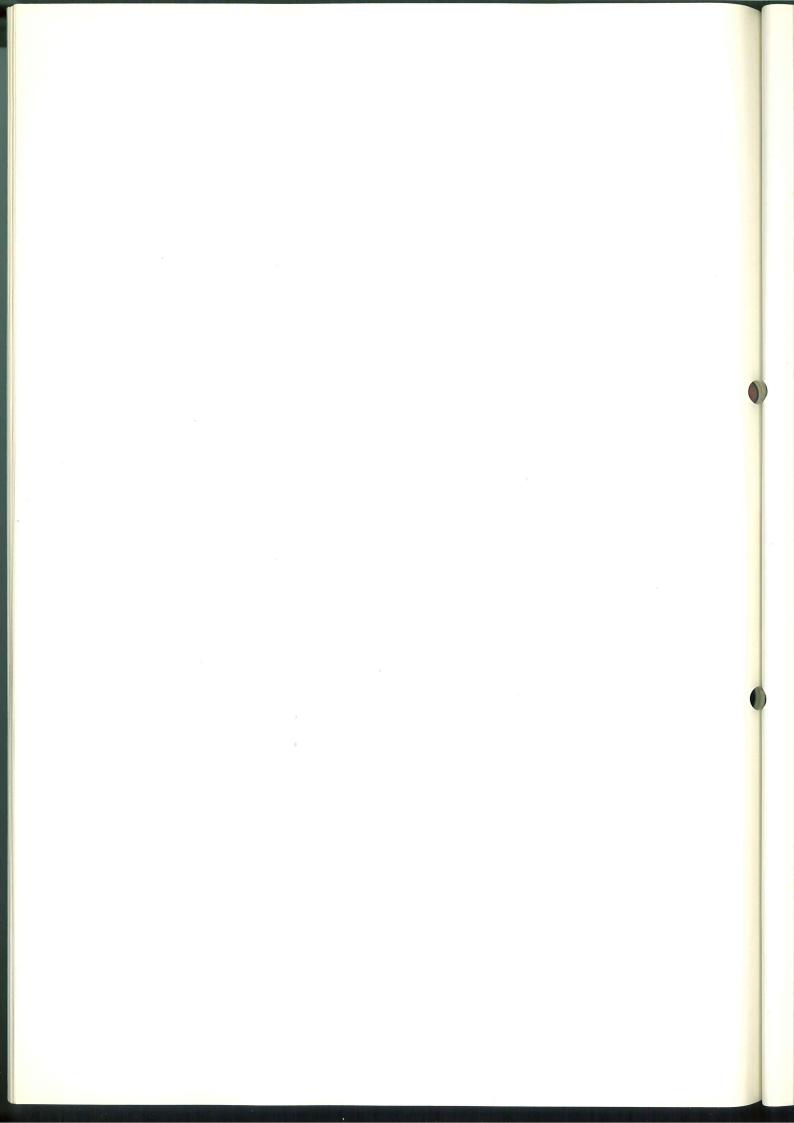
This appendix provides some guidelines on the use of the format for data interchange.

1. Synchronization Bytes

These are bytes at the start of the Track Identifier, Identifiers and Data Blocks; their purpose is to enable equipment reading the information on the track to identify the start of the above areas. The synchronization bytes are special in that they contain a unique pattern of flux reversals which would not normally be encountered elsewhere on the track. This enables equipment reading the information on the track to locate the synchronization bytes without reference to Index.

2. Undefined Gap Contents

If information that lies within a track is updated, then at the point at which writing is started and terminated the information may be corrupted. Writing must be started and terminated such that the Track Identifier, Identifiers and Data Blocks remain as defined in the body of this document. To allow for flexibility in equipment design and to allow for disk speed tolerances, the point of switching from reading to writing and vice-versa has not been precisely defined. This means that after a number of update operations a number of bytes in the gap may be corrupted and for example an (F2)*6 pattern may be generated. However, the gaps are initially defined in such a way that the chance of a complete set of synchronization bytes being generated is negligible.



APPENDIX E

EDC IMPLEMENTATION

Fig. El shows the feedback connections of a shift register which may be used to generate the EDC bytes.

Prior to the operation the shift register is set to ZERO. Input data is added (exclusive OR) to the contents of bit 15 of the register to form a feedback.

This feedback is in its turn added (exclusive OR) to the contents of bit 1 and bit 14.

On shifting the outputs of the exclusive OR gates are entered respectively into positions CO, C2 and C15.

After the last data bit has been added the register is shifted once more as specified above.

The register then contains the EDC bytes.

If further shifting is to take place during the writing of the EDC bytes the control signal inhibits exclusive OR operations. To check for errors when reading, the data bits are entered into the shift register in exactly the same manner as they were during writing. After the data the EDC bytes are also entered into the shift register as if they were data. After this operation the shift register contents will be all ZERO if the record does not contain errors.

The error detection characteristics of this method are as follows:

- Burst of 16 bits or less
- 99,9970% of the bursts of length 17
- 99,9985% of the longer bursts

will be detected for data lengths of 4096 bytes or less.

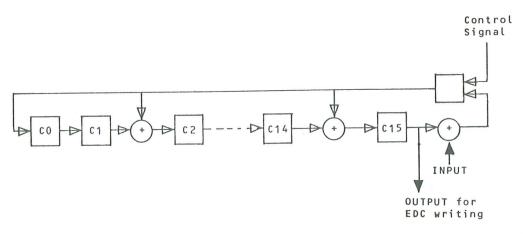


Fig. E.1 EDC SHIFT REGISTER

