

## MAINTENANCE MANUAL

7370/148 MEMORY

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## TABLE OF CONTENTS

<u>PARA.</u>	<u>DESCRIPTION</u>	<u>PAGE</u>
Sect. I	General Description	
1-1	Introduction	1-1
1-2	System Architecture	1-2
1-3	Basic Storage Module PWBA (BSM PWBA) Part No. 942945-001	1-3
1-4	148 Interface PWBA Part No. 942930-001	1-7
1-5	Storage Protect	1-8
1-6	Buffered Controlled Address (BCA) PWBA Part No. 942940-001	1-9
1-7	Universal Buffer PWBA	1-10
1-8	I Cycle M Reg EXP PWBA Part No. 941599-001	1-11
1-9	BSM Select PWBA Part No. 942905-001	1-12
Sect. II	Console Operation and Diagnostic Guide	
2-1	Introduction	2-1
2-2	Alter/Display	2-2
2-3	Diagnostic/Console File Control Switch	2-4
2-4	IBM Microdiagnostics	2-7
2-5	IBM Macrodiagnostics	2-10
2-6	EMM Macrodiagnostics	2-11
2-7	Diagnostic Tie Ups	2-16
2-8	Error Display	2-17
2-9	Address Display	2-18
2-10	Four Word Micro-Loop	2-19
2-11	RC Mode	2-21
Sect. III	Troubleshooting	
3-1	Introduction	3-1
3-2	General Guidelines	3-2
3-3	Troubleshooting Guide	3-4
Sect. IV		
4-1	Parts Replacement and Adjustments	4-1
4-2	Line Power Options	4-12
4-3	DC Voltage Checks/Adjustments	4-13
4-4	Memory Board/Chip Replacements	4-14

Table of Contents (Cont.)

<u>PARA.</u>	<u>DESCRIPTION</u>	<u>PAGE</u>
Sect. V	Preventive Maintenance	
5-1	Introduction	5-1
5-2	PM Frequency	5-2
5-3	Visual Inspection/Housekeeping	5-3
5-4	Electrical Checks	5-4
5-5	Diagnostics	5-5
5-6	System Error Logs	5-6
5-7	Customer Briefing	5-7

FIGURE

1-1	BSM DATA BIT ASSIGNMENT	1-4
1-2	BSM DATA BIT ASSIGNMENT	1-5
1-3		1-6
4-1	EMM CPU Upgrade Cards	4-3
4-2	EMM CPU Upgrade Cards	4-3

CHART

#1	ADDRESS/SAR BIT TESTED CHART	3-7
----	------------------------------	-----

TABLE

4-1	148 Interface Board	4-5
4-2	BSM Select PWBA Timing Specifications and Jumper Positions	4-7
4-3	BCA PWBA Switch Settings	4-10

SECTION I  
GENERAL DESCRIPTION

1-1      INTRODUCTION

The 7370/148 MAINTENANCE Manual was written to facilitate the troubleshooting and on-going maintenance of the EMM 7370/148 Main Memory System. The information enclosed is not intended to be a "course outline" or "student theory guide", but rather to provide reference information peculiar to the EMM 7370/148 Memory Unit and the attachment (Upgrade) to the IBM System 370/148 Central Processing Unit.

Therefore, this manual will not supercede the requirement of the Customer Engineer to have:

- a) working understanding of IBM System 370 architecture;
- b) good technical/mechanical skills;
- c) common sense/rationality.

This manual is divided into sections as follows:

- A. SECTION I - GENERAL DESCRIPTION
- B. SECTION II - CONSOLE OPERATION AND DIAGNOSTIC GUIDE(S)
- C. SECTION III - TROUBLESHOOTING
- D. SECTION IV - REPLACEABLE SUB-ASSEMBLIES
- E. SECTION V - PREVENTIVE MAINTENANCE

SYSTEM ARCHITECTURE

The 7370/148 Memory System is designed to enhance any IBM 370/148 CPU to a total Main Storage Capacity of 4.0 Megabytes (4096K Bytes). The enhancement consists of a Main Memory unit containing up to 4.0 Megabytes in 1.0 Meg increments, and the CPU upgrade hardware required for expanding Main Storage addressing and Storage Protect.

The 7370/148 cabinet contains up to (4) four Basic Storage Modules, each containing 1024K Bytes of memory cards (18 BSM PWBA's) and (1) one Interface card. The 7370/148 cabinet also contains forced-air cooling arrays for the BSM's, an AC power controller, and DC power sources for all EMM 7370/148 Logic.

The 7370/148 Memory System provides for Storage Protect memory, which is located in the 01B-A4 array of the IBM 3148 CPU.

BASIC STORAGE MODULE PWBA (BSM PWBA) Part No. 942945-001

Each Megabyte of 7370/148 is contained within its own memory baseplate, with (18) eighteen BSM PWBA's required per megabyte. The BSM PWBA is a 4 bit x 128K module. On any main storage access to an EMM 7370/148 BSM, all (18) eighteen BSM PWBA's are accessed at once, giving 64 data bits and 8 ECC check bits.

The arrangement of the BSM PWBA's within each of the (4) EMM Megabyte locations, and the respective bit positions are represented in Figures 1-1, and 1-2. Note: Figure 1-1 is for either a 1.0 Meg or 2.0 Meg System, while Figure 1-2 is for 3.0 Meg or 4.0 Meg versions.

The BSM PWBA has a bi-directional data buss, using MST-2 driver/receiver pairs. These devices are replaceable, located on 16-pin dip sockets. See Figure 1-3 for BSM PWBA, and MST driver/receiver locations.

The BSM PWBA receives and sends data via the bi-directional buss directly to and from the CPU via the interconnecting tri-lead cable assembly. Terminations for this data is provided by EMM at the end of the last (highest addressable) BSM installed.

Address and write/read controls are provided by the 148 Interface PWBA.

BSM DATA BIT ASSIGNMENT

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
EMM BITE/BIT	C32	03	07	13	17	23	27	33	37	1 4 8 I N T E R F A C E B D.	CØ8	43	47	53	57	63	67	73	77	51*
IBM BIT	C32	3	7	11	15	19	23	27	31		CØ8	35	39	43	47	51	55	59	63	
	C16	02	06	12	16	22	26	32	36		CØ2	42	46	52	56	62	66	72	76	53
	C16	2	6	10	14	18	22	26	30		CØ2	34	38	42	46	50	54	58	62	
	CT	01	05	11	15	21	25	31	35		CØ1	41	45	51	55	61	65	71	75	
	CT	1	5	9	13	17	21	25	29		CØ1	33	37	41	45	49	53	57	61	
	CØ4	00	04	10	14	20	24	30	34		CØØ	40	44	50	54	60	64	70	74	
CØ4	0	4	8	12	16	20	24	28	CØØ	32	36	40	44	48	52	56	60			

\* DATA I/O PIN

NOTES: This is for either a 1 or 2 Meg (single baseplate) system. Use above chart for BSM's 1 and/or 2.  
For 3 or 4 Meg EMM units, see Figure 1-2.

Figure 1-1

BSM DATA BIT ASSIGNMENT

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
EMM BYTE/BIT	C32	03	07	13	17	23	27	33	37	I N T E R F A C E B D.	C08	43	47	53	57	63	67	73	77	51*
IBM BIT	C32	3	7	11	15	19	23	27	31		C08	35	39	43	47	51	55	59	63	
	C16	02	06	12	16	22	26	32	36		C02	42	46	52	56	62	66	72	76	53
	C16	2	6	10	14	18	22	26	30		C02	34	38	42	46	50	54	58	62	
	CT	01	05	11	15	21	25	31	35		C01	41	45	51	55	61	65	71	75	55
	CT	1	5	9	13	17	21	25	29		C01	33	37	41	45	49	53	57	61	
	C04	00	04	10	14	20	24	30	34	C00	40	44	50	54	60	64	70	74	57	
	C04	0	4	8	12	16	20	24	28	C00	32	36	40	44	48	52	56	60		

BSM's 1 & 4 (on 3 or 4 Meg EMM Units)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
	77	73	67	63	57	53	47	43	C08	I N T E R F A C E B D.	37	33	27	23	17	13	07	03	C32	51
	63	59	55	51	47	43	39	35	C08		31	27	23	19	15	11	7	3	C32	
	76	72	66	62	56	52	46	42	C02		36	32	26	22	16	12	06	02	C16	53
	62	58	54	50	46	42	38	34	C02		30	26	22	18	14	10	6	2	C16	
	75	71	65	61	55	51	45	41	C01		35	31	25	21	15	11	05	01	CT	55
	61	57	53	49	45	41	37	33	C01		29	25	21	17	13	9	5	1	CT	
	74	70	64	60	54	50	44	40	C00	34	30	24	20	14	10	04	00	C04	57	
	60	56	52	48	44	40	36	32	C00	28	24	20	16	12	8	4	0	C04		

BSM's 2 & 3 (on 3 or 4 Meg EMM Units)

\*Data I/O Pin

Figure 1-2

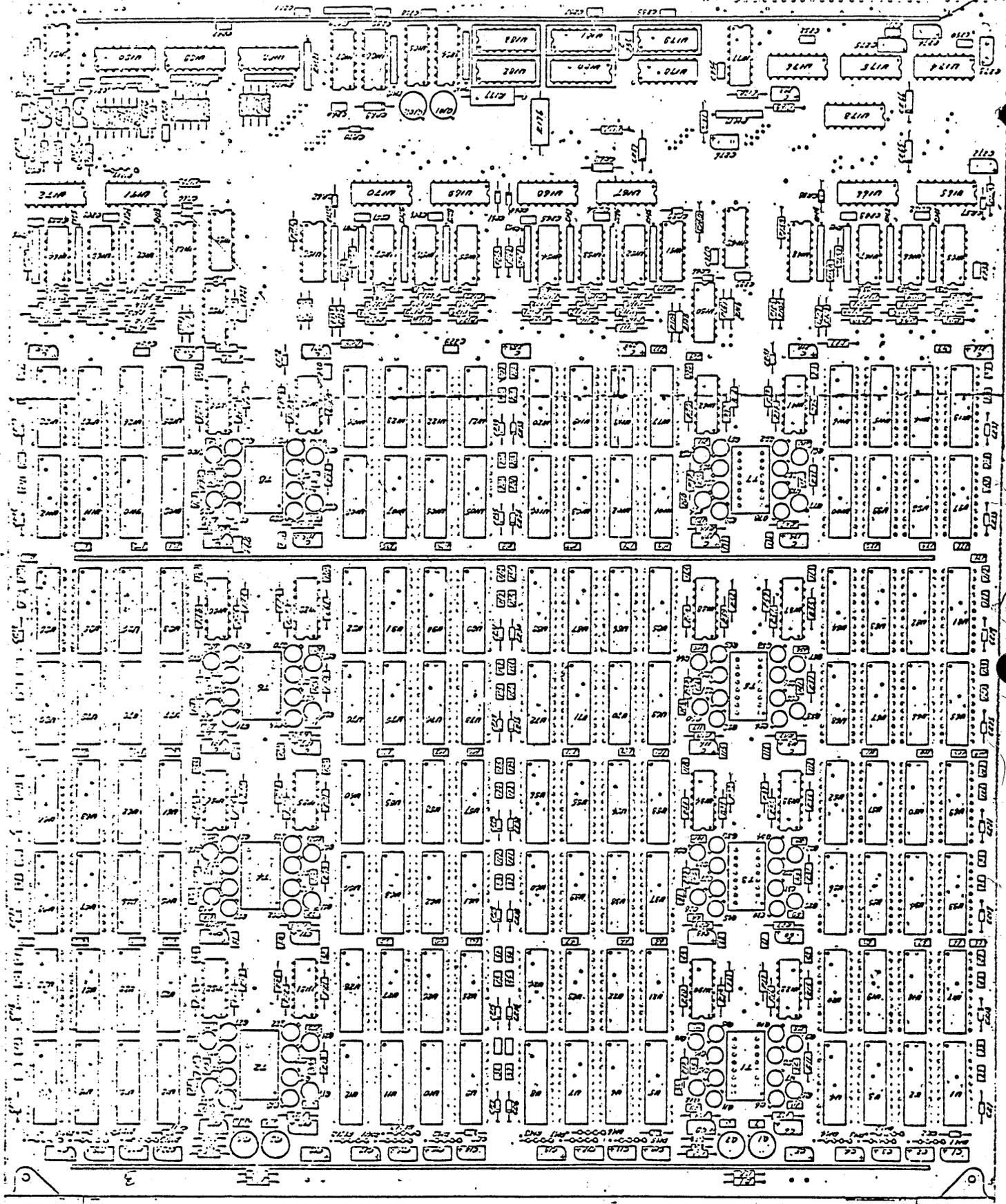


FIGURE 1-3

148 INTERFACE PWBA Part No. 942930-001

Within each Megabyte location (BSM), there is one (1) 148 Interface PWBA, located in Slot 10 (center slot). The 148 Interface PWBA provides signal translation from MST to ECL, chip select generation, 4K addresses for chip addressing, and write controls/write timings. The 148 Interface PWBA also supplies +1.25 VDC to the (18) eighteen BSM PWBA's within the respective BSM, from a small regulator located at the "card-ejector" end of the PWBA.

STORAGE PROTECT

EMM replaces all of IBM Storage Protect with EMM 7370/148 STORAGE PROTECT. The EMM STORAGE PROTECT UPGRADE FOR ALL 3148 ENHANCEMENTS CONSISTS of (2) PWBA's: the 148 SP DATA/ADDRESS PWBA, and the 148 SP Array PWBA. Both PWBA's require both the IBM +1.25 VDC and the EMM -4.0 VDC up-grade supply be active.

## 1-5.1 148 SP Array PWBA Part No. 942915-001

The 148 SP ARRAY PWBA is the actual storage array for all SP keys. The PWBA is an 8 bit x 2K Array. Bits are: Parity bits, data bits 0 - 3, and "fetch, reference and change" bits. The array card will protect both IBM and EMM main memory to a System maximum of 4.0 Megs.

The EMM 7370/148 SP ARRAY is located in slot 01BA4-F2, and is a "4 x 3" card.

## 1-5.2 148 SP Data/Address PWBA Part No. 942910-001

The SP DATA/ADDRESS PWBA interfaces and controls the 148 SP ARRAY PWBA to the IBM 3148 CPU. Both write data and read data is controlled by the SP Data/Address PWBA. Write timings, X & Y Drives, and card select lines are generated by the 148 SP DATA/ADDRESS PWBA, and sent to the SP ARRAY PWBA.

The EMM 7370/148 SP DATA/ADDRESS PWBA is located in slot 01BA4C2, and is a "4 x 3" card.

BUFFERED CONTROLLED ADDRESS (BCA) PWBA Part No. 942940-001

Addition of the EMM 7370/148 Main Memory System includes expansion of CPU main storage addressing capability, diagnostic memory rotation, and "off-line" capability for the EMM 7370/148. The heart of these features is the BUFFERED CONTROLLED ADDRESS (BCA) PWBA. This board generates high-order addresses (M Register 1:1, 1:2, 1:3) by sampling the B Register or Address Buss, according to active Gate B Reg or Gate Addr Bus to M Reg lines. Also, included within the pre-address assembly logic are paths to the M Reg from the I-Cycle Address Buss for DAT (Dynamic Address Translation) facilities.

SAR's 20, 19 & 18 are generated by the BCA, for use in memory selects to the EMM 7370/148. SAR is also gated to the IBM Main Storage, replacing the IBM generated SAR 18 or "M Reg 1:3 to ECC."

The BCA also controls "M Reg less than ACB" (output of Address Check Boundary Comparitor Circuitry) that gives a machine check when a software-generated main storage address is greater than the actual high limit of real storage. EMM adjusts the "boundary" when the EMM 7370/148 is "on-line", by holding off the address check circuitry until the new Address Check Boundary (ACB) is reached.

The BCA PWBA is located in slot 01AB1-T2. The BCA PWBA is a 4 wide x 2 card.

UNIVERSAL BUFFER PWBA

The BCA is fed by signals from IBM panels 01AA1, 01AB3, and 01AC1. Because of signal transmission characteristics due to termination requirements, EMM buffers all critical signals at their source, using two (2) types of UNIVERSAL BUFFER PWBA's. The locations of the Type-001 Buffers are:

01AA1-G2 and 01AB3-G3 Part No. 942935-001

The location of the Type-002 Buffer is:

01AA1-G3. Part No. 942935-002

Both types of buffers are "1 wide" PWBA's.

I CYCLE M REG EXP PWBA Part No. 941599-001

The I CYCLE M REG EXP PWBA is installed in slot 01BC3-P2. The function of this board is to expand the M Register by 2 bits during I CYCLE PREFETCH operations. M Reg Byte 1, Bits 2 and 3 are developed from the I CYCLE Address, corresponding to SAR's 19 & 18. The I CYCLE M REG EXP PWBA is installed on any 3148 processors with a total system size greater than 2 Megs (IBM & EMM).

The BSM SELECT PWBA is a replacement for its IBM counterpart, and is located on all System 370/148 CPU's, with attached EMM Main Memory, in slot 01BA3-V3. The primary functions of the board are to generate the IBM memory controls, select signals and the selects to each 1.0 Meg EMM BSM. The signal Store (and Store) to each EMM Megabyte is also generated by this PWBA.

During diagnostic testing of the EMM Memory Unit, relocating EMM Memory allows complete testing by the IBM Microdiagnostics, even though these diagnostics are capable of only testing a maximum of 2 Megabytes of main storage at a time. By effectively electronically substituting the EMM Memory in 1.0 Meg or 2 Meg segments, it is possible to test all main memory with the standard IBM floppy disks. If all microdiagnostics run normally, then the system can be further tested using macro-diagnostics which can be run with all main memory "on-line". This function is performed by the BSM SELECT PWBA, in conjunction with the EMM DIAGNOSTIC PANEL. By forcing SAR 18 and/or SAR 19 active to the BSM SELECT generator, the appropriate EMM BSM will be selected, instead of the BSM (either IBM's or EMM's) that would normally be selected according to the state(s) of M Reg Byte 1 Bits 19 and 18. It should be noted that the actual SAR (M Reg) is unchanged during this operation, therefore the indicator for SAR 18 (or 19) will not be lit when the "EMM SAR 19" is enabled. For further information, see "EMM DIAGNOSTIC PANEL",

NOTE: There are (2) two types of BSM SELECT PWBA's: Part No. 942905-001 is for a 1 Meg IBM System, while 942905-002 is for a 2 Meg IBM System. A single jumper determines which part goes with which system. See 4-1.5 (BSM Select PWBA - Replacement), for instructions on how to convert -001 to -002, and vice versa.

SIGNAL LEVELS

EMM uses two types of IC components. Each component type, with their respective voltage levels, are listed below:

MST (Voltage - compensated ECL)

High (1) +0.3V to +0.5V

Low (0) -0.3V to -0.5V

ECL (Non-voltage compensated ECL)

High (1) -0.81V to -0.96V

Low (0) -1.65V to -1.85V

SECTION II  
CONSOLE OPERATION AND DIAGNOSTIC GUIDE

2-1

INTRODUCTION

This section is to be used as a reference guide for utilization of both the IBM supplied 3148 microdiagnostics, and EMM supplied macrodiagnostics. In addition, the necessary console operations required to properly diagnose system problems concerning the EMM 7370/148 Main Memory are detailed within this section. This section used in conjunction with Section III, TROUBLESHOOTING, should prove to be a valuable tool for the Customer Engineer.

ALTER/DISPLAY

To use the ALTER/DISPLAY functions, the IBM CPU must be IMPL'd using the 370 IMPL DISK 1. TO IMPL the System 370/148 CPU, the IOC must be loaded first, then the IMPL can be performed. Note: both IOC load and IMPL are automatic when the IMPL disk is in the 33FD on powering up the CPU. Otherwise, with all CPU switches in their normal positions, and the IMPL DISK 1 in the floppy reader, press the IOC LOAD button and wait for CRT to indicate 'IOC LOADED AND READY', before pressing the "START CONSOLE FILE" key. After this, the CRT will request an operator entry in response to "ENTER IMPL OPTION" message on CRT display. Correct response for a 370 Coreload IMPL is 'N', then the "ENTER" key. If a good IMPL is performed, the message: 'IPL CS PATCH ROUTINE THEN CAUSE INTERRUPT FROM CONSOLE (REQUEST KEY)' will be displayed on the CRT, and the "EXEC CPLT" indicator will be on, on the CPU console. For further IMPL information, see EMM 7370/148 OPS Manual.

## 2-2.1

## Alter/Display Procedure

1. Press the "CPU STOP" push button on CPU console.
2. Press "MODE SELECT" key on console keyboard.
3. Wait for 'ALT/DISPLAY' and 'PROCEED' to appear on CRT.
4. Type the appropriate two-character mnemonic and address of the storage or register to be altered or displayed, from the following table:

MNEMONIC AND ADDRESS

STORAGE AREA	MNEMONIC		ADDRESS RANGE
	ALTER	DISPLAY	
Main Storage	AM	DM	000000 - FFFFFFF*
CONTROL STORAGE	AS (NOTE 1)	DS	00000 - 1FFFF
GENERAL-PURPOSE	AG	DG	0-F
FLOATING POINT REG.	AF	DF	0, 2, 4, 6
CURRENT PSW	AP	DP	NONE REQUIRED
LOCAL STORAGE	AL (NOTE 1)	DL	00 - 7F
CONTROL REG.	AC	DC	0 - F
STORE PROTECT KEYS	AK	DK	000000 - FFFFFFF*

NOTES: IBM CE KEY REQUIRED: TO SIMULATE CE KEY, JUMPER 01AA4-Q4B03  
to 01AA4-Q4B08.

\*HIGH BOUNDARY IS MOVEABLE, DEPENDING ON AMOUNT OF MAIN STORAGE  
ON-LINE.

DIAGNOSTIC/CONSOLE FILE CONTROL SWITCH

This rotary switch allows STORE RIPPLE and Read or SCAN RIPPLE operations, without having to build machine-language instructions. To utilize this feature, the CPU must be IMPL'd with the IBM IMPL disk 1.

## 2-3.1 To Store Data Throughout Main Storage:

1. CE/OP Toggle switch to CE.
2. Set desired data into rotary switches A - H.
3. Set DIAG/CNSL FILE CNTRL Sw. to "LOAD SW's A - H."
4. All other switches to normal, depress "START". Data in rotary switches A - H will be loaded into all double word locations throughout main storage, until an ACB check is obtained. Data to memory is displayed in A Reg, lower roller, position 1.

## 2-3.2 To Scan Storage:

1. Step 1 as above.
2. Set DIAG/CNSL FILE CNTRL Sw. to "SCAN".
3. All other switches to normal, depress "START".

If either the CPU or RETRY ERROR indicators comes on, place the ERROR CONTROL rotary switch to HARD STORP, and repeat operation above. Failing address is displayed in B Reg, upper roller, position 5. Data from memory (SDEO) is displayed in lower roller, position 2.

## 2-3.3 To Cycle a Single Control Word:

The DIAGNOSTIC/CONSOLE FILE CONTROL SW. also provides for micro-instruction repeat. This allows performing store and read operations to a single main storage, control storage, or STOR/PROTECT location.

- A. Zero out S P T L REGS
  - a) Set Roller 2 to Position 3.
  - b) Set "STORE SELECT" sw. to ANY LEFT POSITION (EXT REG).
  - c) Set sw. H to BYTE DESIRED S P T L

0 1 2 3

- d) Set sw's A & B to 00.
- e) Depress "STORE" PB.

B. ALTER G P R O & 1.

- a) "STORE SELECT" sw. to LOCAL STORAGE POSITION.
- b) Sw. F & G to 00 (GPR 0).
- c) Sw. A & B = DATA TO BE STORED.
- d) Sw. H to DESIRED BYTE WITHIN WORD (0, 1, 2 & 3).
- e) Depress "STORE" PB ONCE FOR EACH BYTE.
- f) Sw. F & G to 01 (GPR 1)
- g) Sw. A & B to DESIRED STARTING ADDRESS (4 BYTES REQ.).
- h) Sw. H to BYTE WITHIN THE WORD (0, 1, 2 & 3).
- i) Press "STORE" PB ONCE FOR EACH BYTE.

NOTE: See Charts 1 & 2 for data & address patterns.

C. Set "ACB" VALUE FOR YOUR SYSTEM SIZE (2 BYTES)  
(SEE NOTE 1)

- a) Set Roller 2 to POSITION 1 (EXT REG OR A REG).
- b) STORE SELECT sw. to ANY LEFT POSITION.
- c) Sw. F & G to 0A.
- d) Sw. A & B to DESIRED VALUE as follows:
  - 1. 1024K = 10 03
  - 2. 2048K and above = 20 03

BYTE BYTE  
"0" "1"
- e) Set sw. H to DESIRED BYTE (0 or 1).
- f) Press "STORE" PB ONCE FOR EACH BYTE.
- g) "STORAGE SELECT" sw. to MAIN STORAGE.

D. Set "DIAGNOSTIC CONSOLE FILE" sw. to "EXE CTRL WORD SWS  
A → H".

E. Set "RATE" sw. in SINGLE CYCLE

F. Set sw's A thru H to the following:

NOTE: VIEW ADR. ROLLER 1 POS 5 (B REG)  
VIEW DATA ROLLER 2 POS 1 (A REG)

- 4 8 0 8 1 4 0 3 STORE RIPPLE
- 4 0 5 8 1 4 0 3 READ RIPPLE
- 4 8 0 4 1 4 0 3 STORE ONE ADDRESS
- 4 0 5 4 1 4 0 3 READ ONE ADDRESS

6 9 0 4 1 F 0 3      STORE KEY  
 6 0 5 4 1 F 0 3      READ KEY

STORAGE WORD FORMAT

C0			C1		
01	0 0 0	0 0 0	0 0 0 0	1 0	0 0
STORAGE	FETCH	BRANCH	DATA	RIPPLE INC.	STAT.
WORD	0 0 1		INPUT	1 1	
	STORE		(GPR 0)	RIPPLE DEC.	
				0 1	
				NO ADR. UPDATE	

C2			C3		
0 0 0 0 1	0 1	0 0	0 0 0 0		0 0 1 1
ADR.	MODE	STAT.	NEXT		DISABLE
SOURCE	01=M.S.		ADR.		ECC
(GPR 1)	10=C.S.				(VAL MODE)
					0 0 0 0
					NORMAL

G. Set ERROR CONTROL TO DISABLE.

H. Set RATE SW to PROCESS & press START.

NOTES: If System has been successfully IMPL's and "patched",  
 Step C is not necessary.

IBM MICRODIAGNOSTICS

IBM provides a microdiagnostic floppy disk with the 3148, which provides test routines for functional testing of the 3148 CPU and associated hardware. It should be stressed here that these diagnostics are not reliability tests, but rather are strictly tests for function. Intermittant failures will usually not be flagged with the microdiagnostics. The floppy disk labeled IMPL DISK 2 BAS/EXO contains the following diagnostics:

BASICS		(BAS)	BASIC CPU DIAGNOSTICS
EXTENDED	0	(EX-0)	
EXTENDED	1	(EX-1)	
EXTENDED	2	(EX-2)	
EXTENDED	3	(EX-3)	
EXTENDED	4	(EX-4)	Manual Tests (not used)

BASIC provides the initial checkout of basic CPU hardware only. The successful completion of BAS is a prerequisite to running the EXTENDED diagnostics, as the facilities tested by the BAS routines are required to function to operate the DIAGNOSTIC MONITOR loaded from EX-0.

The EXTENDED diagnostic routines provide increasingly complex test routines, encompassing more and more CPU hardware as the tests progress. If the EX-0 test section is passed successfully, it is not necessary to proceed in sequence with the EX-1 thru EX-4 diagnostics; if desired, skipping to any particular diagnostic is generally possible. Note however, that all microdiagnostics must be tested before a system can be assumed "clean" or free of error, previous to further testing by macrodiagnostics, with the sole exception of EX-4, which is not required.

## 2-4.1 Microdiagnostic Run Procedure

To run all micro's, sequentially:

1. Place IMPL DISK 2 in 33FD.
2. Turn "INTERVAL TIMER" Sw. to "DISABLE".

3. All other CPU controls to normal positions, press "START CONSOLE FILE" PB.
4. Enter "D", when CRT displays 'IMPL OPTIONS'; depress "ENTER" key.
5. All micro's are run to completion.

To select a specific microdiagnostic:

Note: only EXTENDED micro's can be selected.

1. Place IMPL DISK 2 in 33FD.
2. Turn "INTERVAL TIMER" Sw. to "DISABLE".
3. All other CPU controls to normal positions, depress "START CONSOLE FILE".
4. Enter "E", then "ENTER" key.
5. Place "CPU RATE" Sw. to "INSTRUCTION STEP".
6. When CRT display's following message:  
                   ' CYCLE EACH TEST: Y. N.'  
 Enter "N", then place "RATE" sw. to "PROCESS".
7. CRT then displays:  
                   ' ENTER TEST NAME:'  
 Type in desired 4 alpha-numeric character name.
8. Diagnostic called in will be automatically initiated. When CPU reaches desired diagnostic location, following message is displayed on CRT:

```
' TEST NUMBER
40 - TEST LOOP           04 - QUIET MODE
20 - SECT LOOP          10 - TEST 1D
06 - ERRORS             01 - INSTR
Enter Sense SW'
```

To execute the test, with failure printouts if occurred, enter "40", then "ENTER" key.

To execute the test, with no failure printout, enter "44", the "ENTER" key.

In both cases, the selected test routine is cycled continuously.

To bypass the selected test, and continue with following tests (sequentially to completion), enter "00" then "ENTER" Key. Diagnostics will proceed, stopping only at incidence

of failure. If no test failures occur, floppy disk will continue thru last test routine, then stop.

#### 2-4.2 Loading MBO (Memory Analyzation)

- Step 1. Place IBM IMPL DISK 2 in 33FD.
2. All CPU Switches to normal, press "START CONSOLE FILE " key.
  3. Enter IMPL OPTION "E", press "END" key.
  4. Place "RATE" sw. to "INSTRUCTION STEP".
  5. Respond to 'CYCLE EACH TEST - Y - N' by entering "N", then place RATE sw to PROCESS.
  6. Respond to 'ENTER TEST NAME' by entering "MBAØ".
  7. Test will load and display TITLE and LOOP instructions, and size of memory to be tested. Set rotary switch "H" to "Ø" for no looping, or "1" for continuous looping.
  8. Depress "START" key.

MBO test will analyze CONTROL STORAGE, then each megabyte of MAIN STORAGE. Note: the sole determination of the testing range of main memory by MBO is the result of analyzing the FEATURE REG, Byte 2, Bits 0 - 3.

#### 2-4.3 MBO Error Printouts

a) 'EXCHANGE S 01B-XX YY'

Where XX = IBM Backpanel Location  
YY = IBM Board/Slot Location

A DBE was detected in the address range covered by the storage board displayed. Two EXCHANGE S messages on the same card indicates 2 bits on that card are failing at the same address.

b) REPLACE S

A solid single bit failure has been detected. The threshold for a solid bit is 256.

c) REPLACE I SSCF I

An intermittant single bit failure has been detected. The threshold for intermittent bits is 128.

IBM MACRODIAGNOSTICS

The T148 (IMPL DISK 2) Macrodiagnostic contains tests for CPU hardware, Channels, timers, Address Translation (DAT) Facilities, and STORAGE PROTECT. To operate these tests, following prerequisites apply:

1. System must have passed BAS - EX-3 normally.
2. System must be IMPL'd with DISK 1.
3. System must be "patched" if EMM Main Memory is to be included.
4. IOC must be reconfigured as a '148' with "CP/KB" (console printer/keyboard). See "RC MODE", para. 2-11.

## 2-5.1 Procedure for Loading T148

1. Place IMPL DISK 2 (IOC/T48) in 33FD.
2. Set CE/OP sw. to CE.
3. Place ERROR CONTROL sw. to "HARDSTOP".
4. Perform "SYSTEM CLEAR".
5. Press "START CONSOLE FILE" PB.
6. Select IMPL OPTION "T" on CRT/KB.
7. Floppy will load, "WAIT" lite will come on.
8. Press PA-1 Key on Keyboard.
9. Hold down "TOD CLK SECURE/ENABLE SET" sw, while first pressing "SYSTEM RESET" PB then "SYSTEM RESTART" PB; release "TOD CLK" sw.
10. Repeat above Step 9, except DO NOT hold down the "TOD CLK" sw.
11. Press "PA-1" key on keyboard.
12. Display will activate with T148 test listings. Diagnostics are self-starting.

EMM MACRODIAGNOSTICS

These diagnostics require that the System 370/148 be IMPL'd with IMPL DISK 1, and if the EMM 7370/148 is to be included, the system must be "patched".

The following diagnostics may be used on the System 370/148 Central Processor, and attached hardware:

DME (E330)	paragraph	2-6.1
ST370 (OLTSEP)		2-6.2
T145/T48 (STAND ALONE)		2-6.3
MDP (MEMORY DIAGNOSTIC PROGRAM)		2-6.4
HDM		2-6.5

The above diagnostics are stored on magnetic tape, then loaded into Main Memory for use. Rather than explain the operation of these diagnostics, this section will give selected "aids" for use, and interpretation of these diagnostics. Therefore, it is assumed that the customer engineering is familiar with the IPL stage and operating procedures of the above diagnostics.

## 2-6.1 DME (E330)

DME is a CPU utility diagnostic, with a diagnostic monitor providing error logging, interpretation and trace routines.

## 2-6.1.1 Full Error Recording/Printing

1. IPL DME
2. When "WAIT" indicator comes on, type the following:  
I/L330/S.4.5.6.8 (ENTER)
3. When 'WAIT DME' appears on CRT, type the following:  
E7101.7. X X X X X X 0 0 X X X X X X (ENTER)  
STARTING ADDR. ENDING ADDR.
4. Type "B" (ENTER)

Routines will loop with full printout of errors.

2-6.1.2 Stop on ECC ERROR (NO Printout of Errors)

1. IPL DME
2. When "WAIT" lite comes on, type:  
I/L 330/S.4.5.6.8.13 (ENTER)
3. When "WAIT DME" appears on CRT, type the following:  
E7101.7. X X X X X X 0 0 X X X X X X (ENTER)  
STARTING ADDR. ENDING ADDR.
4. Type "B" (ENTER)  
  
Routines will loop with no printout of errors.
5. Place CPU "ERROR" sw. to HARDSTOP. All machines will stop on error - with Single ECC being exception.
6. Press "STOP" key.
7. Install "STOP ON SINGLE ECC" JUMPER (See Para. 2-7).
8. Press "START" key.
9. If ECC errors occur, CPU will HARDSTOP. See Para. 2-8 for ERROR DISPLAY, Para. 2-9 for ADDRESS DISPLAY.

2-6.2 ST370 (OLTSEP)

ST370 is basically a reliability diagnostic for the System 370 product line. It can be IPL'd on any IBM System 370 CPU.

The main benefit of the ST370 operating system is its ability to fully exercise:

CPU Hardware, Timers,  
Channels, DAT facilities,  
Control and Main Storages,  
and Storage Protect.

The best use for this diagnostic is after all other diagnostics have been run successfully. Then, this program can be used as a reliability test, or to enable the "STOP ON SINGLE ECC" procedure to be used with the system closely resembling actual customer applied useages.

2-6.3 T145/T48 (STAND ALONE)

T145 exists on both the IBM supplied floppy disk (IMPL DISK 2 T48/IOC) and on tape. If T145 is loaded from tape, the

System 370/148 must be configured as a 145 with Console Printer/Keyboard. See RC MODE, para. 2-11.

#### 2-6.4 MDP

MDP (Memory Diagnostic Program) is contained on the MT1 Diagnostic Utility Tape. This program is a main storage diagnostic routine, allowing full printout/recording of both solid and intermittent single bit errors, and mapping of errors to the device level.

To utilize MDP, the System 370/148 must be IMPL'd with IMPL DISK 1, and if the EMM 7370 is to be tested, must be "patched".

Also, this diagnostic will load only if the IOC is configured as a 370/145 with console printer/keyboard (See RC MODE, para. 2-11).

#### 2-6.4.1 MDP Operating Procedures

- Step 1. Mount MT1 tape and make ready.
2. Enter load unit into sw's F, G and H (console)
3. IPL ("LOAD" PB)
4. At "WAIT" state press PA-1 key. Following message is displayed on CRT:  

'HARD COPY?'
5. a) If printout is desired, and 370/148 does not have an attached console line printer, type 'YES' then press ENTER key. If console line printer is attached, go to Step 6.  
b) Program will then request output device address (printer). Type '00X' (X = device address), then enter.  
c) Press "Restart" key on console. Go to Step 7.
6. Press "ENTER" key as "default" option. Printout will be via console line printer.
7. The following is displayed on CRT:

'370/145 SER. NO X X X X X X MEM SIZE: X X X X X'

'\* \* \* \* M.T.I. PROGRAM LOCATOR \* \* \* \*

VERSION NUMBER: 03.5 \* \* \* \* \*' (where XXX =  
(where XXX = IPL DEVICE ID)

'ENTER PROGRAM NAME (AS 'PROG X X X X X X') OR  
'LIST'\*

8. Enter 'PROG \_\_ MDP' ( \_\_ = space bar)
9. MDP is loaded thru autoloader utility. CRT will display:

'PROG MDP LOADED'

'START OF THE M9 MT1 MEMORY TEST'

'\* A ENTER LOW/HIGH MEMORY LIMITS'

Respond with correct hex boundaries for desired testing range, then press "ENTER" key.

10. Failures are printed in following format:

(EXAMPLE)

TEST 4 EXECUTING

\*MCK INT \*MCIC 20004FDF, R/C 00004E32, F/A 051C90, BOX 00, SYND 4E, BD 05(L), ROW 8, BIT 7 \*\*

DATA BIT (0 - 7) OR C-BIT (CØØ → CØT)

1K CHIP SELECT ADDRESS (NOT USED)

(NOT USED)

DECODED SYNDROME BITS (S32 S16 S8/S4 S2 S1 S0)

(NOT USED)

FAILING ADDRESS

REGION CODE

MACHINE CHECK INTERRUPT CODE

2-7

DIAGNOSTIC TIE UPS

STOP ON SINGLE ECC:

01AB2-N2D07 to 01AB2-M2B08

ENABLE CS WRITE (CE KEY):

01AA4-Q4B03 to B08

NO CF DELAY:

01F-J2B07 to ANY D08 pin.

BLOCK PREFETCH:

01BC3-G4B07 to 01BC3-J2B07.

DIAGNOSTIC PARITY MODE:

01BA3-K2B03 to 01BB3-V3B08.

(DISENGAGES ECC).

2-8

ERROR DISPLAY

The following assumes CPU has come to HARDSTOP after incurring a machine check.

2-8.1

To Display MCKB

1. RATE sw. to SINGLE CYCLE
2. Observe STOR 1 CYC indicator. If on, press "START" once.
3. STOR SELECT sw. to MPX OR EXT REGS)
4. Rotary sw's. F & G to "06".
5. Upper roller, position 1 = MCKB

2-8.2

To Display MCKA

1. RATE sw. to SINGLE CYCLE
2. Observe STOR 1 CYC indicator. If on, press "START" once.
3. "STOR SELECT" sw. to "MAIN".
4. MCKA is displayed on lower roller, position 8.

ADDRESS DISPLAY

The following assumes CPU has come to HARDSTOP either after a machine check, or due to operator intervention.

## 2-9.1 If System has Stopped in Stor 1 Cycle:

M REG should contain valid MS (or CS) address. If not:

1. Display B Reg (lower CPU roller, position 5)  
Bytes 1 - 3 contain MS address, if source is B Reg.
2. Press "START" once, while "RATE" switch is in "single cycle" position. M Reg should be loaded with B Reg data if B Reg was sourced. M Reg = lower roller, position 1.

## 2-9.2 If System has Stopped while not in Stor 1 Cycle:

1. Display M Reg. If no valid MS Address,
2. Press "START" once while in single cycle mode.
3. Display EXT Reg 1B.
  - a) If Byte 1 Bit 5 = 1, failing microword was a storage word.
  - b) If Byte 1 Bit 5 = 1, and Byte 1 Bit 0 = 0, EXT 18 contains the storage data address.

FOUR WORD MICRO-LOOP

This loop allows store and read operations to two memory locations. This loop will run at normal CPU speeds unlike some loops in the IBM Microdiagnostics which run in LOCAL STOR/CONTROL STOR mode. Those loops have a "dummy" cycle between each control word execution.

Options include storing data in validate mode, which prevents ECC corrections and allows writing into Storage locations containing double or multibit errors.

<u>CONTROL WORD ADDRESS</u>	<u>CONTROL WORD</u>	<u>STATEMENT</u>
FFF4	490424F3	STW LS00, LS02 VAL
FFF8	481434F3	STW LS01, LS03 VAL
FFF0	414424F1	RDW LS04, LS02
FFFC	405434F1	RWW LS05, LS03

- LS00 = source data, 1st address (STORE)
- LS01 = source data, 2nd address (STORE)
- LS02 = source address, 1st address
- LS03 = source address, 2nd address
- LS04 = data dest, 1st address (READ)
- LS05 = data dest, 2nd address (READ)

2-10.1 Procedure to Run 4-Word Micro-loop

1. Install CE jumper (ALLOW CS WRITE) 01AA4-Q4B03 to Q4B08
2. IMPL DISK 1 ("patch" if EMM 7370 is to be addressed).
3. Depress "SYSTEM RESET" on CPU.
4. Depress "MODE SEL" key on keyboard.
5. Type 'AS FFF0' (ENTER)
6. Type: '414424F1 490424F3 481434F3 405434F1'  
(Depress 'ENTER')
7. Depress "MODE SEL".
8. Type: 'AG 0'
9. Type: W W W W W W W W X X X X X X X X Y Y Y Y Y Y Y Y  
Z Z Z Z Z Z Z Z

NOTE:

- W's = data pattern for first address (write)
- X's = data pattern for second address (write)
- Y's = address (right-hand justify) for first address

Z's = address (right-hand justify) for second address.

10. Depress 'ENTER' key.
11. Set RATE = single cycle, CHECK CONTROL = disable
12. Set P Reg (EXT 04:1) = "00"
13. Set rotary switches E → H = "FFF4"
14. ADDRESS COMP CNTRL = SYNC/NORM, ADDR COMP = control word address.
15. Depress CHECK RESET, CONTROL ADDRESS SET.
16. Press START button while verifying proper operation of loop, then
17. Set RATE = Process, depress START

Loop should run continuously. By using the IBM scope sync hub (on top edge of 01AAl panel), any sync point within the loop may be used. Set switches E → H to desired control word address of desired control word. A +M level will be sent whenever the micro-loop reaches the desired control word, via the IBM "GATED MATCH" hardware.

RC MODE

The 370/148 utilizes a CRT display (125 DISPLAY) and a console KEYBOARD. Optional features include a line printer. These I/O devices are generally assigned as (1) one unit, emulating the console printer/keyboard (3215) used on the 370/145. Alternate assignment may make the console CRT/Keyboard one device address, and the optional line printer another (if attached).

To reconfigure the I/O devices present on a particular 370/148 CPU, the IMPL disk 1 must be loaded. At completion, follow the operations described below:

1. IMPL with Disk 1 successfully.
2. "PATCH" system, if desired.
3. On CRT, press MODE SELECT key.
4. Type "RC", then "enter" key.
5. 33FD reader will locate configuration data. CRT display will show present configuration data.
6. Follow directions on CRT for altering data.
7. To terminate configuration, press PA-3 key.

Note: Pressing PA-4 or PA-6 keys will cause configuration data, present on screen at time, to be permanently written on the IMPL disk.  
DO NOT PRESS PA-4 or PA-6 keys.

SECTION III  
TROUBLESHOOTING

3-1      INTRODUCTION

This section is intended to be a guide for the qualified Customer Engineer to troubleshoot and correct system failures associated with the EMM 7370/148 memory system, and the CPU upgrade hardware. Contained in this section is all the necessary information to successfully maintain the EMM memory system.

It must be made clear that this manual will not replace the need for pre-requisite training on the 7370/148 memory system, or the necessary familiarity with the IBM 370/148 Central Processing Unit.

3-1.1      Contents

- |    |                       |     |
|----|-----------------------|-----|
| A. | GENERAL GUIDELINES    | 3-2 |
| B. | TROUBLESHOOTING GUIDE | 3-3 |

GENERAL GUIDELINES

The following steps should be verified as being performed prior to determining any specific failing area or assembly:

1. Normal PM has been performed on the unit, insuring all power supplies are properly adjusted, and an adequate airflow is passing through the baseplate(s).
2. All cables, tri-leads, and harnesses are checked for good routing and seating.
3. A.C. line voltage is  $\pm 10\%$  of nominal.

The following rules should apply whenever a problem situation arises:

1. When replacing any CPU upgrade card, both the IBM, CPU, and the EMM 7370/148 should be powered down. Note: by placing the CPU power control panel switch CE5 to "I/O HOLD", the I/O gear connected to the CPU will remain powered up. Also, it may be desired to leave the 7370/148 memory unit powered up, and only power-off the CPU/UPGRADE supply when replacing upgrade cards. Use the CPU/UPGRADE ON/OFF switch on the EMM A.C. Control Assembly.
2. When swapping cards, be very careful to recognize changing symptoms. If symptoms do not change, ALWAYS put back the original card(s) to original locations. Also, when trying spare boards, place only 1 spare in the unit at a time. DO NOT "SHOTGUN" SPARES, in an attempt to repair problems. Generally, this only results in "digging a deeper hole".
3. Whenever a problem appears to be IBM's, but it is in an area related to the 7370/148 upgrade, ensure that all signals related to the failure are scoped and verified before calling in IBM. Remember that the upgrade on 2 Meg. IBM systems, "daisy-chains" the data and address lines from IBM's 2nd Meg. to the EMM 7370/148. Therefore, it is best to be sure that those cables are intact, whenever a 2nd IBM Meg. problem appears, before notifying the customer.

4. Always attempt to stay away from areas not involved with the problem. Nothing creates more dissatisfaction or loss of credibility than to have a minor problem escalate, or major problems multiply. When handling CPU cards or trileads, be most careful not to disturb any other cables or assemblies.

## 3-3.1 Problem/Source Determination

Assuming that a red-lite error has occurred, the initial decision to be made is whether the problem is in the EMM supplied hardware, or the resident IBM CPU. BASIC's generally will detect memory or CPU errors, other than single bit errors. It will locate a solid failing data-bit line by testing "address as data" patterns. Therefore, BASIC's is probably the best diagnostic for starting the determination process.

On most problems, it is advisable to first test the IBM CPU without the EMM 7370/148 active. This may be easily accomplished by switching the EMM ON/OFF switch, on the EMM Diagnostic Panel, to OFF. Another method is to power down the EMM 7370/148. (Remember that the upgrade supply must remain on).

With the EMM unit "off-line", follow the steps below for determining EMM vs. IBM failure source.

## 3-3.1.1 Determine Failing Unit (IBM vs. EMM) EMM OFF-LINE

## I. RUN BASIC's

- A. If no error, next step (II)
- B. If error:
  - 1. For SAR check, step IVA.
  - 2. For DBE, step IVB.
  - 3. For SBE, step IVC.
  - 4. For STOR/PROTECT, step IVD.
  - 5. For ALL OTHER FAILURES, notify customer, problem is IBM's.

## II. RUN EXTENDED's (EX-0 thru EX-3)

- A. If no error, next step (III)
- B. If error:
  - 1. For SAR check, step IVA.
  - 2. For DBE check, step IVB.
  - 3. For STOR/PROTECT check, step IVD.
  - 4. For ALL OTHER FAILURES, problem is most likely IBM.

### III. RUN T148 (IMPL FIRST!)

- A. If no errors, problem is most likely EMM's-Go to Paragraph 3-3.2.
- B. If error:
  - 1. For SAR check, step IVA.
  - 2. For DBE check, step IVB.
  - 3. For STOR/PROTECT check, step IVD.
  - 4. For ALL OTHER FAILURES, problem is most likely IBM.

### IV. TROUBLESHOOTING FAILURES

#### A. SAR CHECK

- 1. EMM BCA Supplies SAR's 20, 19, & 18 and SAR P1.
  - a) Replace BCA location 01AB1-T2, return to step IA.
  - b) Check tri-leads at 01AB1-T2 thru T5, return to step IA.
  - c) Check tri-lead at 01BA3-V3J05 (+ MS ADDR 18) return to step IA.
- 2. Determine Failing SAR Line
  - a) Use Single Control Wd. Loop 2-3.3  
Use chart #1 for address bit location.
  - b) If SAR's 20, 19, 18 or SAR P1 cause SAR RTY CK.
    - (1) Scope affected line for valid levels.
    - (2) Check affected line for correct source/destination.
    - (3) Replace (one at a time) the EMM UNIVERSAL BUFFERS.
      - LOC 01AA1-G3
      - LOC 01AA1-G2
      - LOC 01AB3-G3
  - c) If failing SAR line is not SAR 20, 19, 18 or P1:  
Problem is IBM's - notify appropriate person(s).

B. DBE (Double or Multibit Error)

1. On 1.0 Meg. IBM Systems

- a) EMM plugs into 2nd Meg. Port (unoccupied by IBM). Therefore, DBE's while running IBM only cannot be caused by EMM's data and address cables.
- b) Check BCA for a stuck SAR 18, 19, or 20.
- c) Check +MS Addr. 18 to ECC for proper connections.
- d) Check BSM select card for proper operation, 01BA3-V3.

IBM's BSM select card can be put back into the system to verify function. No wire changes are necessary.

2. On 2.0 Meg. IBM Systems

- a) EMM extends (daisy-chains) the address and data lines from IBM's 2nd (HI) Meg. Also, the terminations for these nets are removed from IBM (Loc. 01BC4-V2) and suitable terminators are placed at end of net (last EMM Meg BSM).
- b) Check all EMM tri-leads at 01BC4-V2 thru V5.
- c) Check all EMM tri-leads at 01BC4-A6 and B6.
- d) Check for proper seating:
  - (1) Paddle boards at EMM 1st Meg.
  - (2) Terminator boards at EMM last Meg.
  - (3) Any and all jumper cables from one EMM Meg to another.
- e) Check CPU/UPGRADE P.S. for proper voltage.
- f) NOTE: failures in IBM 1st (LO) Meg cannot be caused by 2nd Meg (HI) cable or terminator problems. If problems is in 1st (LO) IBM Meg, refer to step IVB1.
- g) Check both BCA and BSM select boards for proper operation.

CHART #1

ADDRESS (Source Register Content)

SAR BIT TESTED

00000000	--
00000004	U/L
00000008	1
00000010	2
00000020	3
00000040	4
00000080	5
00000100	6
00000200	7
00000400	8
00000800	9
00001000	10
00002000	11
00004000	12
00008000	13
00010000	14
00020000	15
00040000	16
00080000	17
00100000	18
00200000	19
00400000	20
00800000	21

C. SBE (Single Bit Error)

1. If a solid single bit error occurs in IBM main memory:
    - a) On 1 Meg IBM systems, EMM has no affect to IBM data I/O for the 1 IBM Meg.
    - b) On 2 Meg IBM systems, EMM does not connect in any way to IBM's 1st (LO) Meg. Therefore, SBE in IBM's LO Meg. are not EMM caused. Only the 2nd IBM Meg. can be affected by EMM as far as SBE are concerned. Note: If the SBE is at all addresses, (solid data-line failure) scope affected data-line from IBM 01BC4-V2 board, to the EMM replacement terminator board. If the net is not contiguous, there would be a lack of termination at the IBM 2nd Meg., and no path for EMM's data I/O line to the IBM HI port. Check affected I/O cable for correct placement.
  2. If the SBE is segment-selective, (run MBO-if only 1 slot location per bit is listed as failed, SBE is card sensitive) verify by moving affected storage board in IBM 2nd Meg. Re-run diagnostic-check for changed symptom. Problem is probably dead storage chip in IBM memory, if error moves with IBM storage card.
- D. STORAGE PROTECT
1. All storage protect is replaced by EMM.
    - a) If failure is a solid bit-line failure, at all addresses, replace EMM SP Data and Address BD., Loc. 01BA4-C2.
    - b) If failure is a solid bit-failure at selective addresses, replace EMM SPS Array Bd., Loc. 01BA4-F2.
    - c) If replacing both 01BA4-C2 and F2 does not fix problem, check the EMM supplied address bits (SAR's 18, 19, 20). Tri-lead locations at 01BA4

are C2P02 (SAR 20), C2P04 (SAR 19), and C2P05 (SAR 18). If these tri-leads are loose, the corresponding address to the EMM Data & Address Board will be active, skewing the card and segment selects.

- d) If above does not correct problem, replace BCA Bd. Loc. 01AB1-T2. The EMM supplied BCA Bd. supplies the hi-order memory and storage key addresses (SAR's 20, 19, 18).

Remember, the EMM upgrade supply must be active to operate the storage protect and BCA logic.

Never remove or replace either EMM supplied or original IBM supplied logic or storage cards with IBM or EMM power on. Always power off the CPU and attached EMM 7370/148 main memory, before changing cards. NOTE: you may power off the EMM upgrade supply by switching the upgrade ON/OFF toggle switch to the OFF.

### 3-3.2 Troubleshooting EMM Failures

In the previous outline, many modes of failures were examined, most of which could be caused by the EMM 7370/148 memory unit, and the CPU upgrade hardware. Remember that most any failure, caused by EMM, involving the UPGRADE will probably show up in both IBM only and EMM on-line modes. Therefore, troubleshooting should always initiate with verifying proper operation of the upgrade and attachment hardware in IBM only modes. Generally, if the IBM CPU runs clean without the 7370/148 main storage unit logically "active", the only hardware left untested will be the EMM 7370/148 storage unit (ie: BSM boards and 148 Interface Bd.), and the increased storage address range (ie: the BCA hi-order address generator). Note that the BCA, and the BSM SELECT PWBA's are at least 60% tested under "IBM only" mode. In the case of the BCA, in most configurations, the only remaining unchecked logic would be in increased address

bit generation, and the corresponding adjustment in the ACB (+M Reg > ACB) hold-off. In the case of the BSM SELECT, all IBM selects, generated by the card, have been checked. The only remaining logic left unchecked is the blocking of IBM 1 and 2 Meg selects and controls, and the gating of EMM select(s) and write controls.

Follow the outline below for troubleshooting EMM failures. The following assumes that the IBM CPU is error free with EMM "off-line", but attached.

Note: When running EQB7 on EX-3, with EMM memory "on-line", at a total system size of 3 Megs or greater, EQB7 will fail. If the EMM ON/OFF switch on the diagnostic panel is set to "OFF", the EQB7 failures should disappear.

The reason for the failure is that EQB7 attempts to force an address exception (MS SAR > ACB) to check for correct trap routine. If the diagnostic is run at 2 Megs, with the actual main storage at 3 or more Megs, EMM raises the ACB to the appropriate level. However, because the micro's will only test to 2 Megs, no ACB check occurs at a 2 Meg + 1 address.

### 3-3.2.1 Locating EMM Failures EMM ON-LINE

- I. Place EMM 7370/148 memory "on-line".
- II. RUN BASIC diagnostic.
  - A. If no error, next step (III).
  - B. If error:
    1. SAR check, step VI.
    2. DBE check, step VII.
    3. SBE check, step IX.
    4. ALL OTHER FAILURES, return to previous section, test IBM only.
- III. RUN EXTENDED Diagnostics
  - A. If no error, next step IV.
  - B. If error:
    1. SAR check, step VI.
    2. DBE check, step VII.

3. SBE check, step IX.
  4. STOR/PROTECT check, step VIII.
- IV. IMPL, then RUN T148
- A. If no error, next step (V).
  - B. If error:
    1. SAR check, step VI.
    2. DBE check, step VII.
    3. STOR/PROTECT check, step VIII.
- V. RUN RELIABILITY (MACRO DIAGNOSTICS) TESTS  
(OLTSEP, ST370, E330, etc.)
- A. Remove all SBE (chip failures) in 7370/148 unit.
  - B. Operate under margins.
    1. If no further failures are found, unit should be fully operational.
    2. If failures are still encountered, return to step I.
- VI. SAR CHECK
- A. Replace BCA PWBA.  
If no fix, next step. (replace original BCA).
  - B. Replace Universal Buffer, Loc. 01AA1-G2.  
If no fix, replace original Buffer, then next step.
  - C. Replace Universal Buffer, Loc. 01AA1-G3.  
If no fix, replace original Buffer, then next step.
  - D. Check all EMM tri-leads at:
    - 01AA1-G2
    - 01AB1-T2 thru T5
    - 01AC1-V5B02
    - 01BA3-V3
  - E. LOCATE FAILING SAR LINE
    1. Use Single Control Wd. Loop, Para. 2-3.3.
    2. Use Chart #1 for SAR LINES/GPRL CONTENT.
    3. If failing, SAR is 20, 19, 18 or SAR P1, scope affected net back to BCA board.
- VII. DBE
- A. Verify proper address function to EMM 7370/148  
Use Single Control Wd. Loop, Para 2-3.3.

Verify that all SAR's function both on and off.

B. Verify proper data-line path function.

Use Single Control Wd. Loop, Para. 2-3.3.

Vary Data to Memory-Check for Bit Cross or Bit Malfunction.

C. Verify failing address (address range).

IF FAILURE is in 1 EMM Meg only, and another EMM Meg is functional, problem is not I/O cables or addresses 17 → 1.

- a) Verify function of BSM selects to EMM (at EMM backplane).
- b) Verify function of block signals to IBM 1 and 2 Megs. (at BSM SELECT PWBA).
- c) Verify function of STORE signal at affected EMM Meg.
- d) Replace 148 INTERFACE BD. in affected EMM Meg.
- e) Replace affected BSM Bd. (use MBO).

VIII. STOR/PROTECT

If STOR/PROTECT fails only when EMM 7370/148 is ON-LINE, but runs O.K. when IBM only, the only difference is the amount (address range) of keys required or used in the particular configuration. Therefore, if the STOR/PROTECT works at 1.0 Meg, the problem is either a bad key in the 1 to 2 Meg address range, or SAR 18 to the Storage Protect DATA & ADDRESS card is not functioning. Refer to Section 3-3.1.1, step IVD.

IX. SBE

A. If a SBE occurs:

Verify address range:

- a) If all addresses, check affected BSM Board, or Data I/O Cable(s).
- b) If Chip Location-Sensitive, replace failing chip(s).

## SECTION IV

### 4-1 PARTS REPLACEMENT & ADJUSTMENTS

#### 4-1.1 Replaceable Sub-Assemblies

FIGURE 4-2 shows positions of various EMM CPU upgrade cards. FIGURE 4-1 shows positions of EMM power supplies and logic cards within the 7370/148 mainframe. NOTE: both figures represent the maximum board and assembly configurations. Therefore, a particular configuration may not require some assemblies or PWBA's.

#### 4-1.2 Tri-Lead Spares

The interconnecting tri-lead harness for data and addresses to the 7370/148 unit contains:

64 data I/O lines

8 ECC C-BIT I/O lines

17 address bits (17 thru 1)

The harness is made up from individual tri-leads. Each tri-lead is a standard tri-lead (pin & rail) connector at the IBM end, but a solder-joint at the EMM 7370/148 end, to one of (4) four "paddle boards". Spare tri-leads are laced into the harness with a "worst-case" length, however, the EMM end of the tri-lead must be soldered to the paddle board by the CE if replacement is desired. Because of the high-level of manual dexterity required, be absolutely certain that: a) the particular tri-lead is definitely faulty, and b) the correct tri-lead is isolated. An error by the CE in locating and repairing the affected net could be most costly! Therefore, BE CAREFUL!

#### 4-1.3 BSM PWBA

Whenever replacing chips or the entire BSM board, BE SURE THAT EMM POWER IS OFF. There is no such thing as being overly careful. Just because it "worked the last time..." If re-seating an assembly becomes difficult, arcing or otherwise intermittantly applying power to the card will most certainly damage the logic, either on that card, or another

one. Remember that data lines from each BSM board are the same ones that IBM uses (ie: data is "daisy-chained" from IBM to EMM, not "buffered") for the HI (2nd) megabyte of main memory.

When removing or replacing BSM boards, if warpage is encountered, try the following procedure:

- 1) Locate assembly in card-guides. Be sure both top and bottom edges are within guides.
- 2) Slowly slide board in and out, from connector face to about 6" from connector. Ascertain whether card is staying within guides, or is edging out of either guide.
- 3) Slide assembly out about 6" from connector face, then firmly and smoothly snap the board into the backplane connector, using your fingertips. Do not miscontrue the above: this is not an attempt to smash the board into the connector! Therefore, picture the relative locations of both the edge connector, and the backplane, and then apply just enough force to make the connection.

EMM CPU UPGRADE CARDS LOCATIONS AND PART NUMBERS

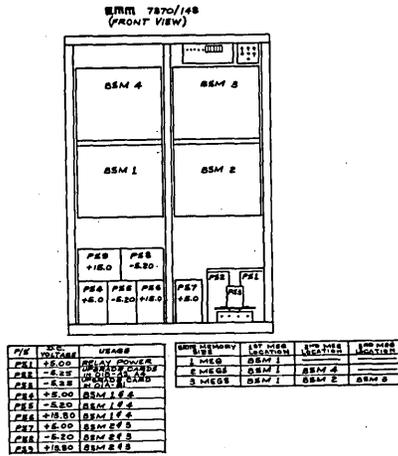


FIGURE 4-1

EMM UNIT

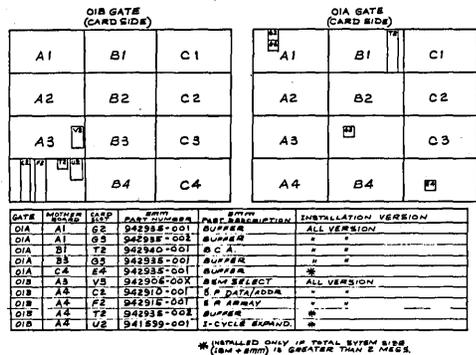
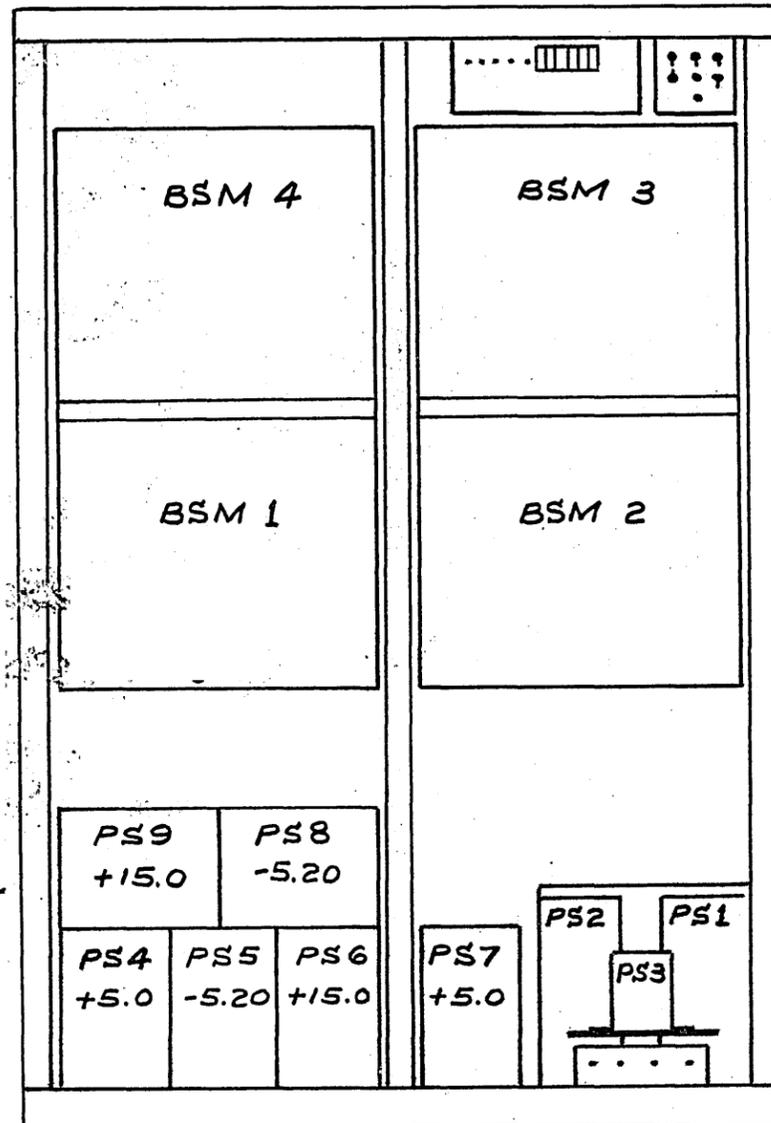
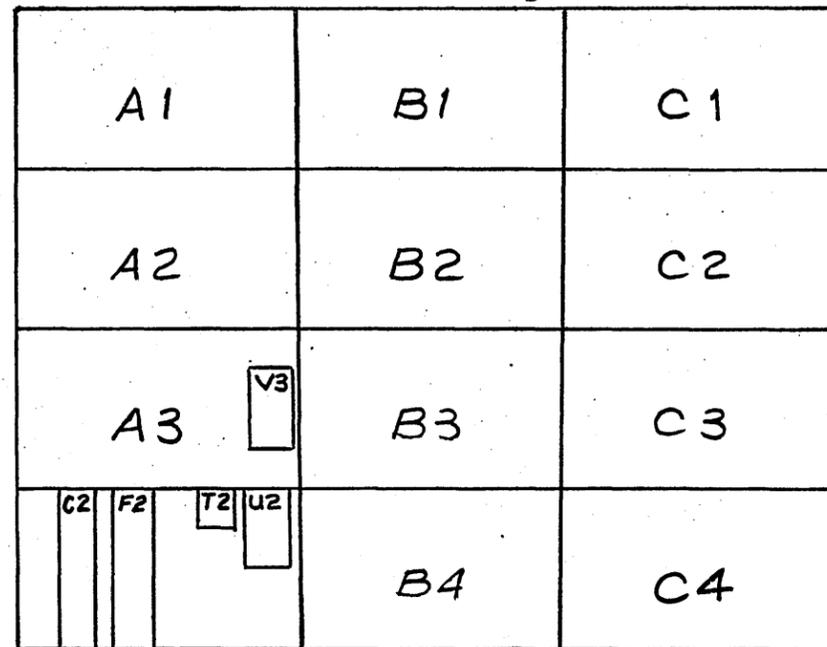


FIGURE 4-2

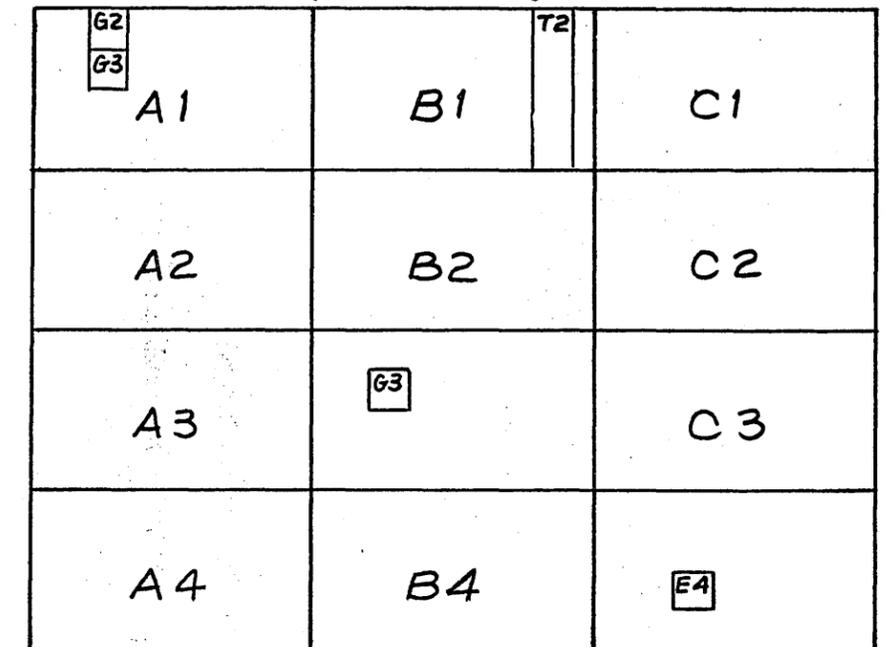
**EMM 7370/148  
(FRONT VIEW)**



**OIB GATE  
(CARD SIDE)**



**OIA GATE  
(CARD SIDE)**



GATE	MOTHER BOARD	CARD SLOT	EMM PART NUMBER	EMM PART DESCRIPTION	INSTALLATION VERSION
OIA	A1	G2	942935-001	BUFFER	ALL VERSION
OIA	A1	G3	942935-002	BUFFER	" "
OIA	B1	T2	942940-001	B.C.A.	" "
OIA	B3	G3	942935-001	BUFFER	" "
OIA	C4	E4	942935-001	BUFFER	*
OIB	A3	V3	942905-00X	BSM SELECT	ALL VERSION
OIB	A4	C2	942910-001	S.P. DATA/ADDR	" "
OIB	A4	F2	942915-001	S.P. ARRAY	" "
OIB	A4	T2	942935-002	BUFFER	*
OIB	A4	U2	941599-001	I-CYCLE EXPAND.	*

P/S	D.C. VOLTAGE	USAGE
PS1	+5.00	RELAY POWER
PS2	-5.25	UPGRADE CARDS IN OIB-A3, A4
PS3	-5.25	UPGRADE CARD IN OIA-B1
PS4	+5.00	BSM 1 & 4
PS5	-5.20	BSM 1 & 4
PS6	+13.80	BSM 1 & 4
PS7	+5.00	BSM 2 & 3
PS8	-5.20	BSM 2 & 3
PS9	+13.80	BSM 2 & 3

EMM MEMORY SIZE	1ST MEG LOCATION	2ND MEG LOCATION	3RD MEG LOCATION
1 MEG	BSM 1	---	---
2 MEGS	BSM 1	BSM 4	---
3 MEGS	BSM 1	BSM 2	BSM 3

\* INSTALLED ONLY IF TOTAL SYTEM SIZE (IBM + EMM) IS GREATER THAN 2 MEGS.

FIGURE 4-1

FIGURE 4-2

TABLE 4-1  
148 INTERFACE BOARD

TIMING SPECIFICATIONS  
AND  
JUMPER LOCATIONS

#### 4-1.5

#### BSM Select PWBA

The EMM BSM SELECT BOARD is a replacement for the IBM BSM SELECT, LOC. 01BA3-V3. The enhanced logic supplied by EMM provides 1 Meg. memory selects and controls to both EMM and IBM main memories.

When replacing the EMM BSM SELECT PWBA, certain jumpers for timing generation must be checked. The timings on the BSM SELECT BOARD are ultra-critical, therefore, even if a board passes diagnostics, all timings should be checked and adjusted when necessary.

Table 4-2 has all specified timing settings and jumper positions as set by the factory.

NOTE: for -001 type, jumper from E27 to E28.

for -002 type, jumper from E27 to E30.

Type -001 is for 1 Meg IBM Systems.

Type -002 is for 2 Meg IBM Systems.

TABLE 4-2  
BSM SELECT FWBA

TIMING SPECIFICATIONS

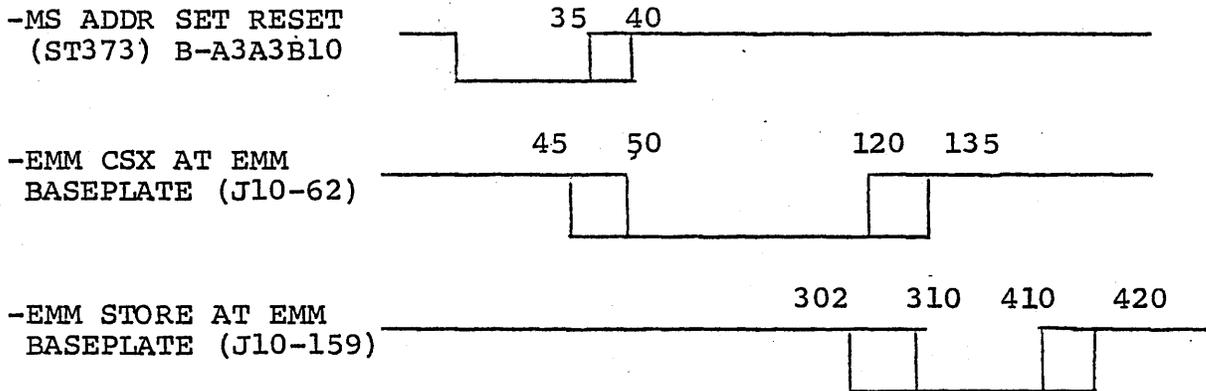
&

RECOMMENDED JUMPER POSITIONS

Refer to Assembly drawing 942905 for EMM BSM SELECT TIMING JUMPER Chart. The timing tabs are factory set and should not require Field Timing Changes.

Refer to IBM ALD ST006 for IBM Timing Reference, and EMM Schematic 942907, Sheet 2 for -CSX, -DOG, -SAG and -STORE Timing option should re-timing be required.

The -EMM X CSX and - EMM X STORE should be approximately as shown.



#### 4-1.6 BCA (Buffered Controlled Address) PWBA

The EMM BCA PWBA generates the high-order address bits necessary to address (up to) 8 Megabytes of main memory. Also provided are "gated address match" (to 8 Megs) "ACB (+ M Reg Less Than ACB) Override" hardware, and an "address remap/force" feature allowing full diagnostic capability.

When replacing the BCA PWBA, LOC. 01AB1-T2, jumper or switch settings, defining main memory sized, must be checked for validity.

Table 4-3 shows jumper or switch setting for the BCA PWBA.

4-3 BCA PWBA SWITCH SETTINGS.

#### 4-1.7 Storage Protect Array PWBA

The EMM STOR/PROTECT ARRAY PWBA provides all key storage for the system 370/148. One array card provides protect key storage for up to 4 Megs of main memory. The location for the first array card is 01BA4-F2. There are no jumpers or timing settings required on the STOR/PROTECT Array Card.

#### 4-1.8 Storage Protect Data & Address PWBA

The EMM STOR/PROTECT DATA & ADDRESS board is used on all 370/148 CPU's with attached EMM 7370/148 main memory. The functions of this board are to interface the EMM STOR/PROTECT ARRAY PWBA to the host processor. Addresses and data in and out are steered by the Data & Address board.

There are no timing taps to be set on the EMM Data & Address board, LOCATION 01BA4-C2.

NOTE: ALWAYS POWER DOWN BOTH THE IBM 370/148, AND THE EMM UPGRADE SUPPLY, WHEN CHANGING EMM UPGRADE CARDS.

#### 4-1.9 Power Supply Replacement

This section describes the procedure for removal and replacement of power supplies in the EMM 7370/148 Memory Unit.

CAUTION:

Extreme care must be exercised during portions of this procedure to avoid damage to the equipment. Also, whenever working on 208 VAC, common sense dictates being extremely aware of where you and your tools are.

4-1.9.1 Power Supply Removal (941601 & 941602)

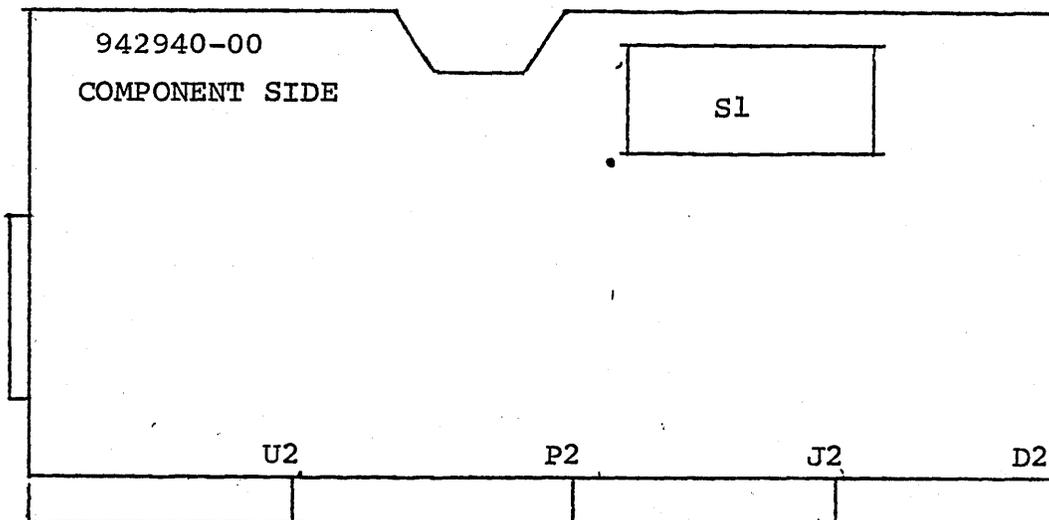
- A) Turn off CBL. Note: if the IBM CPU is to be operated during this removal/replacement operation, leave main circuit breaker on, place LOCAL/REMOTE switch to LOCAL position, and place the UPGRADE ON/OFF switch to on. Now, by placing the EMM ON/OFF switch to OFF, the CPU UPGRADE power supply will remain active.
- B) Disconnect power supply AC lines from terminal strip, DC cables, and DC power sense lines. It is advisable to tag and identify all cables associated with the supply being serviced.
- C) Release (2) two quarter-turn fasteners and slide power supply out of chassis.

TABLE 4-3

BCA PWBA SWITCH SETTINGS

SWITCH (S1)	S1-1	S1-2	S1-3	S1-4	S1-5	S1-6	S1-7	S1-8
ADDRESS	SAR 19	SAR 17	SAR 18	SAR 20	SAR 21	NC	NC	NC
B-INPUT	B2	B0	B1	B3	B4	NC	NC	NC
TOTAL SYSTEM SIZE ON-LINE								
1 MEG	0	1	0	0	0	X	X	X
2 MEGS	0	1	1	0	0	X	X	X
3 MEGS	1	1	0	0	0	X	X	X
4 MEGS	1	1	1	0	0	X	X	X

KEY: 1 = CLOSED 0 = OPEN X = DON'T CARE NC = NOT CONNECTED



NOTE: Set switch S1 according to total main storage on-line (i.e.: EMM + IBM = X Megs).

4-1.9.2 Power Supply Installation (Replacement) (941601 & 941602)

Reverse the procedure called out in paragraph 4-1.9.1 and adjust power supply per paragraph 4-3, Table 4-4.

4-1.9.3 + 5VDC 10A Removal/Replacement (926538-A04)

PS1 and PS2 are located within the AC Power Control Unit. To allow access to PS1 and PS2, remove grill cover.

## Line Power Options

There are two (2) types of power supplies used in the EMM 7370/148 Memory System. The Pioneer power supplies (P/N's 941601 and 941602), which are designed to operate on line voltages of either 208VAC or 230VAC without changing transformer taps, and the +/-5V power supplies (CPU UPGRADE supply, and AC box relay and sequencer supply), which are factory preset for 208VAC operation, and must be adjusted to accommodate 230 VAC.

The input transformer has (3) three primary coil terminals, identified by numbers 1, 2, and 3. The appropriate connections should be made as listed below.

208 V AC - Terminals 1 and 2

230 V AC - Terminals 1 and 3

DC VOLTAGE CHECKS/ADJUSTMENTS

The specified voltages for the BSM supplies, AC controller/ Sequencer-Relay Supply, and the CPU UPGRADE supply are listed in Table 4-4. Measure power supply voltages, (with all margin switches in their nominal (normal) positions. A 250 MV. maximum drop is allowed between DC voltage lugs on power supplies and voltage pins per TABLE 4-4. If a greater drop is found, check for faulty connections on both DC and AC connectors, buss bar connections, etc. When a measured voltage cannot be correctly adjusted within tolerance, it is necessary to replace the supply.

## POWER SUPPLY SETTINGS AND TEST POINTS

Description	Type	From (V)	To (V)	Nominal
+15VDC 50A P/N 941602-001	BSM	(Voltage	GND	+13.8V+50MV
+5VDC 120A P/N 941601-001	BSM	Buss Bar	GND	+50V+50MV
-5.2VDC 120A P/N 941601-001	BSM	Lower)	GND	-5.2V+50MV
+5VDC 10A P/N 926538-A04	REG BOX	PS1(+)*	PS1(-)	+5.0V+250MV
-5.2VDC 10A P/N 926538-A04	UPGRADE	01BA4F2B08	01BA4F2D08	-4.0V+50MV
+1.25VDC PCBA 942930-001	INTERFACE	J10B J10-645	GND J10-043	+1.25V+20MV

\* AC Power Distribution/Control Box.

should be 1.33

## 4-4 MEMORY BOARD/CHIP REPLACEMENT

### 4-4.1 Introduction

The EMM 7370/148 is designed using 4K NMOS static RAM's located on pluggable sockets. Because of the easy ability to locate single bit failures, it is standard procedure to replace failing devices, rather than replacing the board. This reduces the logistics and costs in maintaining large inventories of memory boards, and also maximizes burn-in time on a given module.

### 4-4.2 Methods for Determining Failures

- 1) MBO- STORAGE ANALYSIS TEST - Refer to Maint. 2-4.2
- 2) EMM DIAGNOSTICS - Refer to Maint. 2-6.
- 3) IBM DIAGNOSTICS - Refer to Maint. 2-5.
- 4) ANY MICRODIAGNOSTIC/CUSTOMER SOFTWARE, USING STOP ON SINGLE ECC ERROR JUMPER - Refer to Maint. 2-6.1.2.
- 5) EREP/SEREP

### 4-4.3 Criteria for Replacing Storage Chips

- 1) A 'REPLACE S' message is displayed on MBO.
- 2) More than 64 errors within any one chip.
- 3) If there have been recurring system problems, all single bit errors should be corrected.

### 4-4.4 Criteria for Replacing Storage Boards

- 1) If replacing a chip more than once does not correct a problem at that chip address.
- 2) When the failing board will only indicate Double Bit Errors.
- 3) Multiple Chip Failures within same Bit Line.
- 4) As emergency maintenance - defer correcting chip problem until time is allowed.

### 4-4.5 Chip Replacement Procedure

Using the detailed diagnostics previously mentioned, location and replacement of failing chips should be relatively easy.

The information necessary for location of failing chips are - failing bit, and address of failure.

- 1) Using Table 4-5, locate failing megabyte, decoding SAR's 19 and 18 from failing address.
- 2) Using Figures 1-1, (Maint. Section 1) and 1-2, locate board location of failing bit.
- 3) Using Figure 1-1, locate bit location on failing board.
- 4) Using Figure 4-3, locate failing chip by decoding SAR's 17, 16 and 15 for CS and SAR's 14 and 13 for R/W selects.

EXAMPLE 1: FAILING BIT = 4:0    EMM = 2.0M    IBM = 1.0M  
                    FAILING ADDRESS = 17BF00

TABLE 4-5 shows that the failing board is within EMM's first meg.

FIGURE 1-1 shows that the failing bit is located in slot 8 of the lower baseplate.

EDGE CONNECTOR SIDE

	CS 0	CS 1	CS 2	CS 3	CS 4	CS 5	CS 6	CS 7
R/W 0	U113	U97	U81	U65	U49	U33	U17	U1
R/W 1	U114	U98	U82	U66	U50	U34	U18	U2
R/W 2	U115	U99	U83	U67	U51	U35	U19	U3
R/W 3	U116	U100	U84	U68	U52	U36	U20	U4
R/W 0	U117	U101	U85	U69	U53	U37	U21	U5
R/W 1	U118	U102	U86	U70	U54	U38	U22	U6
R/W 2	U119	U103	U87	U71	U55	U39	U23	U7
R/W 3	U120	U104	U88	U72	U56	U40	U24	U8
R/W 0	U121	U105	U89	U73	U57	U41	U25	U9
R/W 1	U122	U106	U90	U74	U58	U42	U26	U10
R/W 2	U123	U107	U91	U75	U59	U43	U27	U11
R/W 3	U124	U108	U92	U76	U60	U44	U28	U12
R/W 0	U125	U109	U93	U77	U61	U45	U29	U13
R/W 1	U126	U110	U94	U78	U62	U46	U30	U14
R/W 2	U127	U111	U95	U79	U63	U47	U31	U15
R/W 3	U128	U112	U96	U80	U64	U48	U32	U16

BIT 3/7  
51\*

BIT 2/6  
53

BIT 1/5  
55

BIT 0/4  
57

SAR BUS																			
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	U/L X X

CS 0 CS 1 CS 2 CS 3 CS 4 CS 5 CS 6 CS 7

\*I/O Pin on BSM PWBA

NOTE: When using the Chip Decoder at right, use the real SAR's from the CPU. (Look at the indicators on CPU.)

	CS	0	1	2	3	4	5	6	7
SAR 17		0	0	0	0	1	1	1	1
SAR 16		0	0	1	1	0	0	1	1
SAR 15		1	0	1	0	1	0	1	0

	B/W	0	1	2	3
SAR 14		1	1	0	0
SAR 13		1	0	1	0

By overlaying the failing address (in hex) across the SAR Bus (Figure 4-1), values for SAR 17 thru 13 can be obtained.

SAR	<u>19</u>	<u>18</u>	<u>17</u>	<u>16</u>	<u>15</u>	<u>14</u>	<u>13</u>
VALUE	0	1	0	1	1	1	1

To obtain the correct chip select scheme used in the EMM 7370/148, SAR's 15, 14 & 13 must then be inverted.

Therefore, the CS SAR for example 1 is shown below:

SAR	<u>19</u>	<u>18</u>	<u>17</u>	<u>16</u>	<u>15</u>	<u>14</u>	<u>13</u>
REAL SAR	0	1	0	1	1	1	1
ACTUAL CS SAR	0	1	0	1	0	0	0
		MEG		CS		R/W	

The Meg location would then be Meg 1 (IBM Meg = 0). The Chip Select then would equal CS 2. The R/W Select would then equal R/W 0. Location of Chip is = EMM Meg 1, SLOT 8, CHIP U93.

Figure 4-1 performs the adjustment to the SAR in the CS Chart at bottom. Note that by inverting the SAR's 15, 14, & 13 shown in the chart, the binary CS result is true. Therefore, by applying the real system SAR values for SAR 17, 16 and 15 will result in the actual Chip Select location in the 7370/148. No inversion is necessary when using the chip locator. Use the real system SAR's as indicated in either the MREG (when in Stor 1 cycle, CS indicator off) or the BREG (roller position 5, lower).

## SECTION V

### PREVENTIVE MAINTENANCE

5-1

#### INTRODUCTION

This section provides preventive maintenance (PM) procedures for the EMM 7370/148 Main Memory System. Correctly performed, PM can be the most effective method of minimizing remedial maintenance (RM) incidents.

The following points are discussed in this section:

- |                                   |     |
|-----------------------------------|-----|
| A. PM Frequency                   | 5-2 |
| B. Visual Inspection/Housekeeping | 5-3 |
| C. Electrical Checks              | 5-4 |
| D. Diagnostics                    | 5-5 |
| E. System Error Logs              | 5-6 |
| F. Customer Briefing              | 5-7 |

PM Frequency

Normal preventive maintenance should be performed on a quarterly basis as a minimum. Frequency should be increased due to any one of the following conditions:

- A. Excessive dirt or dust found on system filters.
- B. Extreme temperature changes.
- C. Low humidity/High static levels.
- D. Excessive single bit (correctable) errors at last PM period.
- E. Continual or excessive power supply drift.

Visual Inspection/Housekeeping

The careful visual inspection can often correct a problem looking for a chance to happen. A critical inspection can be carried out while running a reliability or macro-diagnostic.

- A. Check all fans and filters for cleanliness and correct operation. Vacuum if necessary.
- B. Check all cables, connectors and harnesses for breaks or frayed insulation. Pay close attention to harnesses near pivot points of assemblies or hinged frames.
- C. Check baseplates for proper seating of cable connectors, terminator paddle boards, power cables, etc.
- D. Check boards (without removing) within baseplates for warping or shorting against each other. Correct if necessary.

Electrical Checks

The only electrical checks necessary on the EMM 7370/148 system are checking the power supply voltages and correcting any discrepancies.

All power supplies should be checked for correct margin operations, as well as for correct nominal output. Also, power supplies should be checked for excessive or frequent drift, by recording the outputs of all supplies each PM. By noting the system log each PM, drifting supplies should be found easily.

Diagnostics

Each PM, a full run of all available diagnostics should be run, with a copy of the console printout attached to the system log. If a diagnostic error does appear during PM, it will be readily determined whether it is a new, or existing failure. This information may often be useful, if not necessary, to repair a problem.

All IBM micro-diagnostics should be run, both on the IBM resident memory, and with either the EMM memory "on-line" in addition to IBM or, by using the EMM Diagnostic Panel, by logically substituting EMM memory for IBM.

T145 or T148 should be run to check Storage Protect function. ST370 and E330 should also be run.

All single bit errors should be removed. Use procedure in Section IV, troubleshooting.

System Error Logs

Obtain copies of recent EREP's or LOGREC's from the customer. Determine if there have been any memory errors logged. In the event that there are logged memory errors, check the failing address for range of failures. If there are errors within EMM main memory locations, corrective action should be taken at this time. (Refer to Section III TROUBLESHOOTING).

Remember that most error logs, as applied to main memory, are the result of double or multi-bit errors. Therefore, if the error indication on LOGREC or EREP is DBE, the failing bit register (syndromes) will not be useful in determining failing bits. The only useful information will be the failing address register.

3-2-78  
JL



# ENGINEERING CHANGE ORDER

PROJECT <b>148</b>	SHEET <b>1</b> OF <b>2</b>	ECO No <b>80022</b>
REFERENCE ECR <b>---</b>	DISTRIBUTION NUMBER <b>1910</b>	PREPARED BY <b>B.ADA 2-27-8</b>

DOCUMENT NUMBER <b>942930</b>	CURRENT REV <b>A</b>	NEW REV <b>A1</b>	TITLE <b>ASSEMBLY - INTERFACE CARD</b>				CHECK
PART NUMBER	CURRENT REV	NEW REV	CLASS OF CHANGE	DISPOSITION OF EXISTING PARTS	EFFECTIVITY	S/N or EFFECTIVITY DATE	RESPECTABLE ENGINEER <i>J. Adams 2/27/8</i>
OTHER DOCUMENTS AFFECTED	ECO NUMBER		<input type="checkbox"/> 2 WAY INTERCHANGEABLE	<input type="checkbox"/> USE	<input type="checkbox"/> NEXT ORDER		ENGINEER/EC
PARTS LIST			<input type="checkbox"/> 1 WAY INTERCHANGEABLE	<input type="checkbox"/> REMARK	<input type="checkbox"/> PRIME INSPECTION		MANUFACTURING
WIRE LIST			<input type="checkbox"/> NON-INTERCHANGEABLE	<input type="checkbox"/> REFURBISH	<input type="checkbox"/> MANDATORY		PRODUCT SUPPORT
SCHEMATIC			<input checked="" type="checkbox"/> RECORD	<input type="checkbox"/> SCRAP	<input type="checkbox"/> MANDATORY WITH RETROFIT		OTHER
ARTWORK			<input checked="" type="checkbox"/> ACCEPT	REASON FOR REJECTION		FSI REQD	OTHER
OTHER			<input type="checkbox"/> REJECT			<input type="checkbox"/> YES <input checked="" type="checkbox"/> NO	<i>Special 3/1/8</i>

REASON FOR CHANGE: TO CLARIFY **(13)**, **(14)** AND RELOCATE TIMING JUMPER TO MEET TIMING SPEC, THEREFORE, ALLOWING MINIMAL CHANGE PER NOTE **(14)**

DESCRIPTION OF CHANGE

IS

WAS

**(14)** ON FINAL ASSEMBLY, TIMING TAPS MAY NOT BE AS SHOWN. TIMING TAPS MAY BE ALTERED BY TEST (LAB-SET) TO MEET TIMING SPEC (TS 942850)

**(13)** INSTALL WIRE WRAP POST, ITEM 36 OF P/L ON E1 THRU E38, AND ON EYELETS PROVIDED FOR PINS 3 THRU 7 and 9 THRU 13 OF U37, U38, U47, U48, U49, U50, U51, U52.

**(14)** ON FINAL ASSEMBLY, TIMING TAPS MAY NOT BE AS SHOWN. THESE ARE SUBJECT TO CHANGE IN TEST.

**(13)** INSTALL WIRE WRAP POST ITEM 36 OF P/L ON E1 THRU E38, U37-PINS 3-7 & 9-13, U38-PINS 3-7 & 9-13, U52-PINS 3-7 & 9-13, U47-PINS 3-7 & 9-13, U48-PINS 3-7 & 9-13, U49-PINS 3-7 & 9-13, U50-PINS 3-7 & 9-13, U51-PINS 3-7 & 9-13.

IS

TIMING WIRE WRAP LIST	
FROM :	TO
E17(U33-10)	U47-13
E18(U33-7)	U37-7
E19(U33-11)	<del>U38-7</del>
E20(U33-6)	U49-4
E21(U33-12)	U47-4
E22(U33-5)	U52-4
E23(U33-13)	U52-4
E24(U33-4)	<del>U38-10</del>
E28(U35-6)	<del>U38-4</del>
E29(U35-7)	U38-7
E30(U19-6)	U38-4
E31(U19-4)	U49-3
E32(U19-10)	U47-3
E33(U35-13)	<del>U37-4</del>
E34(U35-12)	U50-13
E35(U35-11)	U37-6
E36(U35-10)	<del>U49-13</del>

U38-9

U38-6

U38-11

U37-3

U49-12

WAS

TIMING WIRE WRAP LIST	
FROM :	TO
E17(U33-10)	U47-13
E18(U33-7)	U37-7
E19(U33-11)	U38-7
E20(U33-6)	U49-4
E21(U33-12)	U47-4
E22(U33-5)	U52-4
E23(U33-13)	U52-4
E24(U33-4)	U38-10
E28(U35-6)	U38-4
E29(U35-7)	U38-7
E30(U19-6)	U38-4
E31(U19-4)	U49-3
E32(U19-10)	U47-3
E33(U35-13)	U37-4
E34(U35-12)	U50-13
E35(U35-11)	U37-6
E36(U35-10)	U49-13