CS01/H2 (DH11/DM11 COMPATIBLE) COMMUNICATIONS MULTIPLEXER TECHNICAL MANUAL



FCC NON-CERTIFIED COMPUTER EQUIPMENT

This equipment has not been tested to show compliance with new FCC Rules (47 CFR Part 15) designed to limit interference to radio and TV reception. Operation of this equipment in a residential area is likely to cause unacceptable interference to radio communication requiring the operator to take whatever steps are necessary to correct the interference.

Copyright (C) 1984 Emulex Corporation

The information in this manual is for informational purposes and is subject to change without notice.

Emulex Corporation assumes no responsibility for any errors which may appear in the manual.

Printed in U.S.A.

TABLE OF CONTENTS

Section	1	INTRODUCTION	
	1.1 1.2	SCOPE OVERVIEW	1-1 1-1
	1.2.1	General Description	1-1
	1.3	FEATURES	1-1
	1.3.1	Microprocessor Design	1-1
	1.3.2	Packaging	1-2
	1.3.3	Configuration Flexibility	1-2
	1.3.4	Self-Test	1-2
	1.4	FUNCTIONAL COMPATIBILITY	1-2
	1.4.1 1.4.2	Diagnostics	1-2 1-3
	1.4.2	Operating Systems	1-3
Section	2	GENERAL DESCRIPTION	
	2.1	ORGANIZATION	2-1
	2.1.1	Controller	2-1
	2.1.2	Distribution Panel	2-1
	2.2	PHYSICAL DESCRIPTION	2-3
	2.2.1	Controller	2-3
	2.2.1.1	Connectors	2-3
	2.2.1.2	Indicators	2-3
	2.2.1.3 2.2.1.4	Switches PROM's	2-3 2-3
	2.2.1.5	RAM Buffer	2-3
	2.2.2	Distribution Panel	2-5
	2.2.2.1	Line Adapter Boards	2-5
	2.2.2.2	Interface Board	2-5
	2.3	INTERFACES	2-5
	2.3.1	Q-Bus	2-5
	2.3.1.1	Q-Bus Starting Addresses	2-7
	2.3.1.2	Interrupt Vector Addresses	2-7
	2.3.1.3	BR (Interrupt) Priority Level	2-7
	2.3.1.4	DCLO and INIT Signals	2-8
	2.3.1.5	DMA Transfers	2-8
	2.3.2	CAll/H Line Adapter	2-8
	2.3.2.1	CAll/H Line Adapter Options	2-8
	2.3.3	CAll/C Line Adapter	2-9
	2.3.3.1	CAll/C Line Adapter Options	2-9
	2.4	FUNCTIONAL DESCRIPTION	2-9
	2.4.1	Receiver Operation	2-9
	2.4.1.1	UART	2-9
	2.4.1.2	Receiver Scanner	2-10
	2.4.1.3	Silo Operation	2-10 2-10
	2.4.1.4	Half-Duplex Operation Received Character Distortion	2-11
	2.4.1.5 2.4.2	Transmitter Operation	2-11
	2.4.2.1	UART	2-11
	2.4.2.2	DMA Transmission	2-11
	2.4.2.2	Auto-Echo Operation	2-12

2.5.1 2.5.2 2.5.3	22-Bit Memory Addressing Interrupts	2-13 2-13 2-13 2-13
3.2 3.2.1 3.2.2 3.2.3 3.2.4 3.2.5 3.2.6 3.2.7 3.2.8 3.3 3.3.1 3.3.2	DH11 REGISTERS SYSTEM CONTROL REGISTER (SCR) RECEIVED CHARACTER REGISTER (RCR) LINE PARAMETER REGISTER (LPR) CURRENT ADDRESS REGISTER (CAR) BYTE COUNT REGISTER (BCR) BUFFER ACTIVE REGISTER (BAR) BREAK CONTROL REGISTER (BRCR) SILO STATUS REGISTER (SSR) DM11 (MODEM CONTROL) REGISTERS CONTROL AND STATUS REGISTER (CSR) LINE STATUS REGISTER (LSR) DH11/DM11 GENERAL PROGRAMMING	3-7 3-10 3-11 3-11 3-12 3-13 3-13 3-16 3-18
3.4.1 3.4.2 3.4.4 3.4.4.1 3.4.4.2 3.4.4.3 3.4.5.1 3.4.5.2 3.5 3.5.1	INFORMATION INITIALIZE INTERRUPTS 22-BIT ADDRESS PROGRAMMING PROCEDURE RECEIVER OPERATION Receiver Scanner Silo Operation Half-Duplex Operation TRANSMITTER OPERATION DMA Transmission Modem Control CC01 CONTROLLER ARCHITECTURE	3-18 3-19 3-20 3-20 3-21 3-21 3-21 3-21 3-22 3-22 3-22
4	INSTALLATION	
4.1 4.2 4.3 4.3.1 4.3.2 4.3.2.1 4.3.3 4.3.3.1 4.3.3.2 4.3.3.3	INSPECTION PREPARE THE CPU CONTROLLER BOARD SETUP Number of DH11 Emulations Q-Bus Starting Address Alternate Unibus Addresses Interrupt Vector Address DH11 Vector DM11 Vector Interleaving DH11 and DM11 Vector Addresses Option Selection Option Switches Extened Silo Option	4-1 4-2 4-2 4-2 4-4 4-6 4-6 4-6 4-7 4-7 4-7
	2.5.2 2.5.3 3 3.1 3.2.1 3.2.2 3.2.5 3.2.6 3.2.6 3.2.6 3.2.7 3.3.2.6 3.3.2.6 3.3.3.1 3.4.4.3 3.4.4.3 3.4.4.3 3.4.4.3 3.4.4.5 3.4.5.1 3.4.5.2 3.5.2 4.1 4.2 4.3 4.3.3.1 4.3.3.3.1	2.5.2 22-Bit Memory Addressing Interrupts DEVICE REGISTERS AND PROGRAMMING 1. OVERVIEW 3.2 DH11 REGISTERS 3.2.1 SYSTEM CONTROL REGISTER (SCR) 3.2.2 RECEIVED CHARACTER REGISTER (RCR) LINE PARAMETER REGISTER (LPR) CURRENT ADDRESS REGISTER (CAR) 3.2.4 CURRENT ADDRESS REGISTER (BAR) 3.2.5 BYTE COUNT REGISTER (BAR) 3.2.6 BUFFER ACTIVE REGISTER (BAR) 3.2.7 BREAK CONTROL REGISTER (BRCR) 3.2.8 SILO STATUS REGISTER (SRR) 3.3.1 CONTROL AND STATUS REGISTER (CSR) LINE STATUS REGISTER (LSR) DH11/DM11 GENERAL PROGRAMMING INFORMATION 3.4.1 INTERRUPTS 3.4.2 INTERRUPTS 3.4.4 RECEIVER OPERATION 4.4.3 S1LO Operation 3.4.5 TRANSMITTER OPERATION 3.4.5.1 DMA Transmission Modem Control CCO1 CONTROLLER ARCHITECTURE RECEIVER OPERATION 4.5.1 NAME OF TRANSMITTER OPERATION 4.5.2 RECEIVER OPERATION 4.5.3 CONTROLLER ARCHITECTURE RECEIVER OPERATION 4.1 INSPECTION 4.2 PREPARE THE CPU 4.3 CONTROLLER BOARD SETUP 4.4

	4.4	CP11 DISTRIBUTION PANEL CONFIGURATION	4-7
	4.4.1	Panel Numbering	4-7
	4.4.2	International Power Supply	4-8
		Conversion Instructions	
	4.5	LINE ADAPTER CONFIGURATION/INSTALLATION	
	4.5.1	CAll/H Option Selection	4-9
	4.5.1.1	Flow Control Option	4-9
	4.5.1.2	Pinning Assignment Options	4-11
	4.5.2	CAll/C Option Selection	4-13
	4.6	CP11 DISTRIBUTION PANEL INSTALLATION	4-13
	4.7	CC01 CONTROLLER INSTALLATION	4-13
	4.7.1	SPC Slot Selection	4-13
	4.7.2	Controller Mounting	4-14
	4.8	CABLING	4-15
	4.8.1	Controller to Distribution Panel	4-14
	4.8.2	CAll/H Line Adapter to External Device	4-14
	4.8.2.1	Cable Types	4-14
	4.8.2.2	Cable Lengths	4-16
	4.8.3	CAll/C Line Adapter to External	4-17
		Cable Type	4-17
	4.8.3.1	Cable Type Cable Length	4-18
	4.8.3.2	VERIFICATION	4-18
	4.9	Self-Test	4-18
	4.9.1	Register Examination	4-19
	4.9.2		4-19
	4.9.3	Line Adapter Wrap-Around Test	4-19
	4.9.3.1	CAll/H Tests	4-20
	4.9.3.2	CAll/C Tests	4-22
	4.9.4	Mini-Test	4-23
	4.9.5	Diagnostics	4-23
	4.9.6	Test Connector	4-23
Appendix	A	CONTROLLER OPTION SWITCHES	
	A.1	CC01 CONTROLLER PCBA	A-1
	A.2	CAll/H LINE ADAPTER	A-2
Appendix	В	ZDHM DIAGNOSTIC	
Appendix	С	EXPANDED SILO OPTION	
Appendix	D	ZDHK DIAGNOSTIC PATCHES	

LIST OF TABLES

Table No.	<u>Title</u>	
Table 1-1 Table 2-1 Table 2-2 Table 2-3 Table 3-1 Table 4-1 Table 4-2	CS01/H2 Subsystem Specifications Q-Bus Connections DH11 and DM11 Q-Bus Starting Addresses CA11/H Interface Connector Tx and Rx Speed Table Number of DH11 Emualtions (CP11 Distribution Panels) Q-Bus Starting Address Selection	1-3 2-6 2-7 2-8 3-4 4-2
Table 4-3 Table 4-4 Table 4-5 Table 4-6 Table A-1 Table A-2 Table A-3 Table A-4 Table A-5 Table A-5 Table A-6	DH11 Vector Address Selection DM11 Vector Address Selection RS-232-C Cable Lengths 20 mA Current Loop Cable Lengths Distribution Panel Select DH11 Interrupt Vector Select DM11 Interrupt Vector Select Controller Starting Address Line Test Switch Option Switch	4-3 4-4 4-17 4-18 A-1 A-1 A-2 A-2 A-2 A-3
	LIST OF FIGURES	
Figure No.	<u>Title</u>	
Figure 2-1 Figure 2-2 Figure 3-1 Figure 4-1 Figure 4-2 Figure 4-3	CP11 Distribution Panel DH11/DM11 Registers CC01 Controller Assembly CA11/H Line Adapter CA11/C Line Adapter	2-3 2-4 3-2 4-5 4-10 4-10
Figure 4-3 Figure 4-4	CP11 Distribution Panel Physical	4-10

Dimensions

Figure 4-5 Figure 4-6 Figure 4-7

Terminal Cable Schematic

Null-Modem Cable Schematic

Modem Cable Schematic

4-15 4-15

4-16

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the CS01/H2 communications multiplexer. In addition, this manual provides diagnostics and application information.

1.2 OVERVIEW

1.2.1 General Description

The CS01/H2 Communications Multiplexer connects up to 64 asynchronous serial communications lines with individually programmable parameters to the LSI-ll computers manufactured by Digital Equipment Corporation.

The CS01/H2 emulates 1, 2, 3 or 4 DEC DH11 Asynchronous 16-Line Multiplexers and their associated DM11 Modem Control units. The subsytem consists of a CC01/H controller board and 1 to 4 CP11 Distribution Panels each containing one or two CA11 line adapter boards. The CC01 is a single quad-size board which plugs directly into the LSI-11. The line adapter boards contain the line connection and the line circuitry which interface the serial communication line with the parallel data cable to the communications controller.

The CS01/H2 includes the functions of the DM11 Modem Control unit as part of its emulation. As such the CS01/H2 serves as an interface between the modem and the processor. The modem control signals are available as a standard feature with the RS-232-C line adaptor (CA11/H); however, the current loop line adaptor (CA11/C) does not support modem control.

1.3 FEATURES

1.3.1 Microprocessor Design

The CS01/H2 design incorporates an 8-bit high performance bi-polar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to perform an emulation of the equivelant DEC controller. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up and line-loop test.

1.3.2 Packaging

The CC01/H controller is constructed on a single quad-size PC board which plugs directly into the LSI-11 chassis. A single 34-quad flat cable daisy-chains to a maximum of four CP11 distribution panels which contain the line adapter circuitry. The CA11 line adapter boards are plugable modules in eight line groups.

1.3.3 Configuration Flexibility

Each communications controller emulates up to four 16 line DHlls and four DMlls for a maximum of 64 lines. Various types of line adapters may be mixed in eight line groups.

1.3.4 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, the on-board memory, and the individual line adapters. Although this test does not completely test all circuitry, successful execution indicates a very high probability that the controller and the line adapters are operational. If the controller fails the self-test, it leaves the fault LED ON and the controller cannot be addressed from the CPU.

The power-up self-test also does a loop test on each of the line adapter UART circuits. In addition it is possible to perform either an internal or external loop-back test on groups of eight circuits while the CS01/H2 is on-line.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Diagnostics

The CS01/H2 executes the following standard DEC DH11 and DM11 diagnostics (*16 lines only; patch required, see Appendix D):

ZDHK DHll Modem Control Multiplexer Diagnostic*

ZDHM DHll Comprehensive Diagnostic ZDHN DHll Data Reliability Test

1.4.2 Operating Systems

The CS01/H2 communications multiplexer is compatible with all DEC LSI-ll operating systems that support DHlls without modification.

Table 1-1 CS01/H2 Subsystem Specifications

Characteristic	Specification
CC01/H CONTROLLER	
Design	High-speed bipolar microprocessor implementation of all CS01 functional operations.
Function	Provides complete functional emulation of four DH11 multiplexers and DM11 modem controls.
Software Compatibility	Diagnostics: ZJ179 (DH11) and ZJ118 (DM11) kits Operating Systems: RSX11M, RSX11M+, RSTS/E
No. of Distribution Panels	1 to 4
No. of Lines	8 to 64
Throughput	50,000 characters per second total
Distribution Panel Interface	Eight-bit bidirectional data bus with necessary addressing and control in a single 34-conductor flat cable.
Receive Silo	64-character FIFO for each functional 16-channel DH11; Interrupt programmable for any FIFO full level.
Expanded Receive Silo	Optional 128-character FIFO for each functional 16-channel DH11.
CPU Interface	Standard Q-Bus interface. One bus load for both DHll and DMll.
DMA Address Range	0 - 2097K words
DMA Transfer	16-bit word with parity check

Table 1-1 (Cont.) CS01/H2 Subsystem Specifications

Device Address	Selectable with switches and PROM's to cover all DEC-defined DHll assignments.
Vector Address	Switch selectable for DMll and DHll
Priority Level	BR5
Indicator	Controller self-test fault
Option Switches	DIP switches for selection of controller options.
Packaging	Single quad-size two layer printed circuit board
Power	5v +/- 5%, 4 amps.
CP11 DISTRIBUTION PANEL	
Configuration	Seven inch high panel for two 8-channel line adapters, including power supply and cable interface.
Dimensions	7" high x 19" wide x 7" deep
Weight	16 1bs.
Power	Self-contained supply, 50-60 Hz. 115/230 vac, 35 watts
CAll/H LINE ADAPTER	
Configuration	Two-sided PCB measuring 6-1/2" x 8" which plugs into CPll Distribution Panel.
Interface	RS-232-C, with DMll-compatible modem control
Connectors	Standard EIA RS-232-C, 25-pin male connector.

Table 1-1 (Cont.) CS01/H2 Subsystem Specifications

Indicators	Fault LED per line.
Transmission Modes	Half-duplex, full-duplex, echo-plex
Line Formats	Character lengths: 5-8 bits Stop bits: 1, 1-1/2, 2 Parity: odd, even, none
Data Rates	50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200 baud and ext. 1X clock
Distortion	Transmitter: less than 2% intersymbol Receiver: up to 43% intersymbol distortion and speed variation
Modem Control Signals	To: RTS, DTR, Secondary Tx From: CTS, CD, RI (or DSR), Secondary Rx
CAll/C LINE ADAPTER	*.
Configuration	Same as CAll/H.
Interface	20 mA current loop.
Connections	Four screw posts
Transmission Modes	Half-dulpex, full-duplex, echo-plex
Line Formats	Same as CPll/A.
Data Rates	Same as CPll/A.
Distortion	Same as CP11/A.

BLANK

2.1 ORGANIZATION

The CS01/H2 communications multiplexer consists of two units: the CC01/H Communications Controller and one to four CP11 Distribution Panels which are connected to the controller by a single 34-conductor flat cable.

2.1.1 Controller

A block diagram showing the major functional elements of the CC01 controller is shown in Figure 2-1. The controller is organized around an 8-bit high-speed bipolar microprocessor which performs all controller functions. The ALU and register file portion of the microprocessor are implemented with two 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with 12 2K X 4 PROM's.

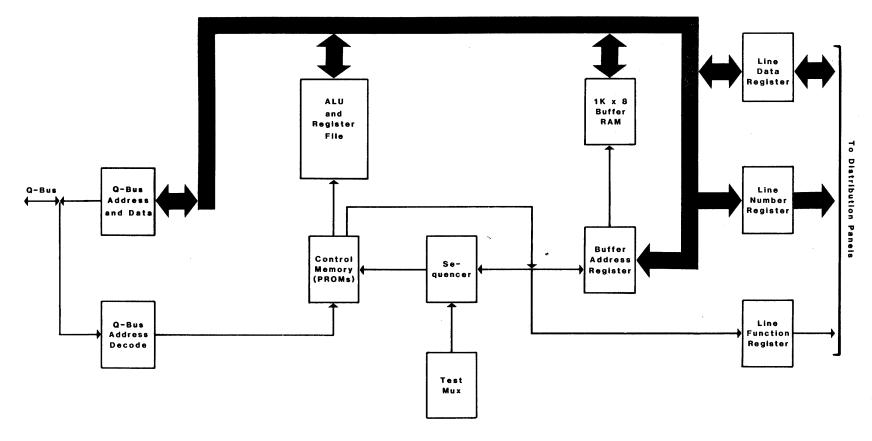
A 4K \times 8 high-speed RAM holds device registers, silo buffer and working storage for the microprocessor. The RAM is both a source and destination to the internal data bus and is addressed directly and indirectly by the microprocessor.

The Q-Bus interface consists of 42 bidirectional and two unidirectional signal lines. The Q-Bus interface is used for programmed I/O, CPU interrupts, and data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA operations and transfers data between the Q-Bus data lines and each line buffer.

The line adapter boards with their UART circuits are interfaced to the controller by a 34-conductor cable. This cable contains an 8-bit bidirectional data path, seven address signals and control signals. The Output Data Register holds data going to the line adapters. The Line Address Register holds the address of the line and the distribution panel.

2.1.2 Distribution Panel

Each distribution panel contains one or two eight-line CAll Line Adapters and an intergal power supply. Two types of line adaptors are available. The CAll/H provides a RS-232-C interface with modem control. The CAll/C has a 20 mA current loop interface and does not support modem control. The line adapters provide the data and modem interface circuitry plus the UARTs circuits which provide the serial to parallel and parallel to serial conversions normally found in these type devices. The UART also contain the baud rate generator for each line. Data control and status transfers between the line adapters and communication controller are on a parallel byte basis.



CS0101-0282

Figure 2-1 CS01 Block Diagram

2.2 PHYSICAL DESCRIPTION

2.2.1 Controller

The CC01 controller board is designated Part Number CU0110401. The board is shown in Figure 2-2. The board dimensions correspond to the DEC quad-size board. The board is two-sided.

2.2.1.1 Connectors

The distribution panels interface to the controller by means of the 34 pin connector J1 located in the upper right hand corner of the board. Connectors J2 and J3 are used for connecting special test equipment for factory test and repair operations and are not intended for use in normal controller operations.

A quad-sized PCBA, the board interfaces to connector rows A, B, C and D. The 18 pins of each connector row are designated A through V - excluding the letters G, I, O, and Q - from right to left; the top side pins are designated "1" and the bottom side pins are designated "2".

2.2.1.2 Indicators

There are two LED indicators on the located on the top of the CC01 PCBA. LED1 is a fault indicator which will remain ON after powering-up the controller if a fault is detected during the self-test. LED2 is a DMA activity indiactor that flashes during NPR activity.

2.2.1.3 Switches

There are three DIP switches on the board. In addition there is a eight pole switch (SWI) located along the top edge of the board. The switches in these packs are used to select the controller Q-Bus and vector addresses, the number of emulations to be performed and other user selectable options.

2.2.1.4 PROM's

The 12 firmware PROM's are located along the top edge of the board. The PROM locations are designated 0 through 11. The number written on top of the PROM IC is the Emulex part number which identifies the unique pattern of the PROM. These numbers are in the same numerical order as that of the PROM numbers.

The controller makes use of two special PROM's to perform Q-Bus address decoding.

2.2.1.5 RAM Buffer

The two 2168 RAM ICs located on the PCBA are used for configurations of up to 64 lines.

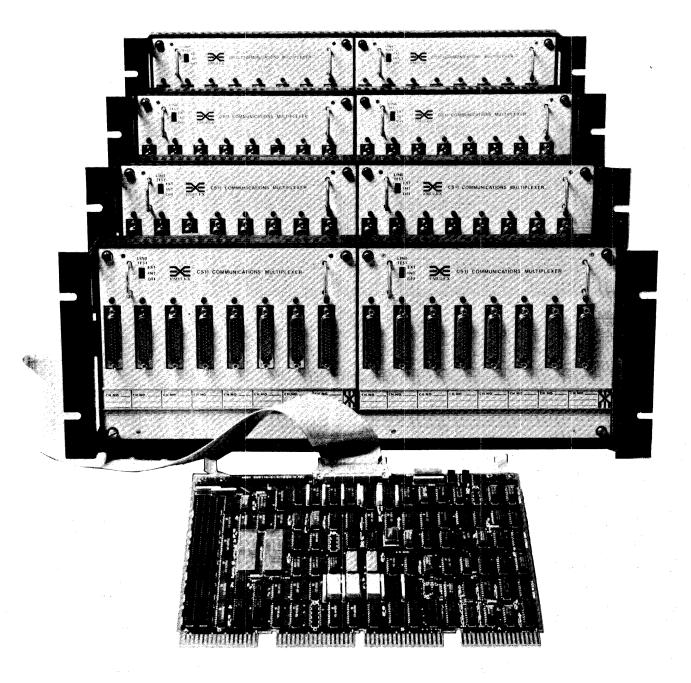


Figure 2-2 CC01 Controller Board and Distribution Panel

2.2.2 Distribution Panel

The distribution panels consist of a mechanical assembly, a power supply, an interface board, and one or two line adapter boards with their cover plates. The distribution panel is shown in Figure 2-2.

2.2.2.1 Line Adapter Boards

Both the CAll/H and CAll/C line adapter boards measure 6-1/2" x 8" and connect to the Interface Board, located in the back of the panel, through a set of 38 AMP MOD l pins. The CAll/H board contains eight 25-pin male connectors for interfacing to RS-232-C terminals, modems, or like devices. The CAll/C also provides eight lines, but it uses a four-screw terminal strip for interface to 20 mA current loop devices. Both contain UART and level conversion circuitry for each line.

Each line has a small LED indicator mounted directly above the connector which is used to indicate that the internal self-test of the controller has detected a fault for that line adapter. A three position slide switch in the upper left hand corner of the line adapter board is used to enable an internal, external wrap-around or terminal echo test for the eight line group.

2.2.2.2 Interface Board

The interface board interfaces the daisy-chain cable and the power supply to the two line adapter boards. It is mounted by a set of screws to the Distribution Panel. Each of the line adapter boards plugs into the AMP pins connected to the interface board and inturn is fastened to the panel by four screws. Two daisy-chain cable connectors protrude through the back of the panel so that the cable may be continued or terminated if the panel is the last one on the cable. The power supply cable plugs into a connector on the back of the interface board which also protrudes through the panel.

2.3 INTERFACES

2.3.1 Q-Bus

The LSI-11 Bus consists of 42 bidirectional and 2 unidirectional signal lines. These form the lines along which the processor, memory and I/O devices communicate with each other.

Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The lines are divided as follows:

- 1. Twenty-two data/address lines <BDAL21:BDAL00>
- Six data transfer control lines BBS7, BDIN, BDOUT, BRPLY, BSYNC, BWTBT

Table 2-1 Q-Bus Connections

	A		В	
	1	2	1	2
Α	BIRQ5	+5V	BDCOK	+5V
В	BIRQ6		BPOK	
С	BDAL16	GND	BDAL18	GND
D	BDAL17		BDAL19	
E		BDOUT	BDAL20	BDAL02
F		BRPLY	BDAL21	BDAL03
H		BDIN		BDAL04
J	GND	BSYNC	GND	BDAL05
K		BWTBT		BDAL06
L		BIRQ4		BDAL07
M	GND	BIAKI	GND	BDAL08
N	BDMR	BIAKO	BSACK	BDAL09
P	BHALT	BBS7	BIRQ7	BDAL10
R	BREF	BDMGI	BEVNT	BDALll
S		BDMGO		BDAL12
T	GND	BINIT	GND	BDAL13
U		BDAL00		BDAL14
V		BDAL01		BDAL15

- Three direct memory access control lines BDMG, BDMR, BSACK
- Six interrupt control lines BEVNT, BIAK, BIRQ4, BIRQ5, BIRQ6, BIRQ7
- 5. Five system control lines BDCOK, BHALT, BINIT, BPOK, BREF.

The MS four data/address lines (BDAL <21:18>) are used only for addressing and do not carry data. BDAL <17:16> reflect the parity status of the 16-bit data word during the data transfer portion of the bus cycle.

2.3.1.1 Q-Bus Starting Addresses

The Q-Bus starting address for the first DHll and DMll is selected by SWl. The available addresses are listed in Table 2-2, below. Instructions for setting SWl are given in paragraph 4.3.2.

Table 2-2
DHll and DMll Q-Bus Starting Addresses

DHll	DMll
17760020	17770500
17760040	17770510
17760060	17770520
17760100	17770530
17760120	17770540
17760140	17770550
17760160	17770560
17760200	17770570
17760220	17770600
17760240	17770610
17760260	17770620
17760300	17770630

2.3.1.2 Interrupt Vector Addresses

The DMll and DHll interrupt vector addresses are progammed by SW2. Data for setting these switches is given in Table 4-3 and Table 4-4.

2.3.1.3 BR (Interrupt) Priority Level

Both the DH11 and the DM11 interrupt the CPU on BR5.

2.3.1.4 DCOK and INIT Signals

The DCOK and INIT signals both perform a controller clear. The self-test is performed only when DC power is initially applied.

2.3.1.5 DMA Transfers

The controller performs word DMA transfer read operations, so as to halve Q-Bus loading. The controller checks for memory parity errors (if the system has a memory parity controller) which is posted as a NXM error when a parity error is detected.

2.3.2 CAll/H Line Adapter

The CAll/H Line Adapter has eight channel interfaces. Interface pinning assignments are the same as the DEC DHll with DMll modem control. As such, the pinning assignments are those specified for Bell 202C Data Sets (modems). Electrical signal levels are per EIA RS-232-C specifications. The receiver circuits are implemented with 1489 devices; the transmitter circuits are implemented with 1488 devices. Stock Emulex interface pinning assignments are defined in Table 2-3.

Table 2-3 CAll/H Interface Connector

Pin #		Function
Pin l		Chassis Ground
Pin 2	_	Transmit Data
Pin 3	_	Receive Data
Pin 4	_	Request To Send
Pin 5	-	Clear To Send
Pin 7	-	Logic Ground
Pin 8	-	Carrier Detector
Pin ll	-	Secondary Transmit Data
Pin 12	_	Secondary Receive Data
Pin 18	_	Make Busy
Pin 20	_	Data Terminal Ready
Pin 22	-	Ring Indicator

2.3.2.1 CAll/H Line Adapter Options

The CAll/A interface can be reconfigured to allow use of a number of other modems. The following is a list of the modem options and their pinning assignments. The changes are effected using wire wrap jumpers. Instructions for implementing the options are in the chapter on installation, paragraph 4.5.1. Note that the additional modems may not be supported by DEC software and that custom drivers may have to be written for their implementation.

Option	Pinning Assignments
Standard RS-232-C	Secondary Receive, Pin 16. Secondary Transmit, Pin 14.
103 E,G,H,J Modems	Make Busy, Pin 25 = Ready to Send, Pin 4.
212 A Modem	Make Busy, Pin 18 = Ready to Send, Pin 4.
811 B	Receive Signal Element Timing, Pin 17 = Secondary Receive, Pin 12.
DSR for Ring	Data Set Ready, Pin 6 = Ring, Pin 22.

2.3.3 CAll/C Line Adapter

The CAll/C Line Adapter provides a 20 mA current loop interface for each of its eight lines. Modem control is not supported. Both the transmit and receive circuits are optically coupled. This provides common noise rejection that is much greater than RS-232C and 20 ma interfaces that are not optically coupled. LEDs above each channel's interface connector are used to indicate faulty channels.

2.3.3.1 CAll/C Line Adapter Options

There are several options that can be selected using jumpers on the CAll/C. The CAll/C comes from the factory configured with active transmitters and receivers. The transmitters and receivers can be independently reconfigured for passive operation if required. The CAll/C also comes configured from the factory with an open circuit voltage of 12VDC. A Long Line (L.L.) option with an open circuit voltage of 24VDC can be selected if longer line lengths and/or increased imunity to noise are required. To further increase noise rejection, additional filtering may be strapped to the receiver loop. Implementation of these options is described in the Installation Section, paragraph 4.5.2.

2.4 FUNCTIONAL DESCRIPTION

2.4.1 Receiver Operation

2.4.1.1 UART

Reception on each line is by means of universal asynchronous receiver/transmitters (UARTs). These MOS/LSI devices perform all the function of double buffered asynchronous character assembly. The receiver section of the UART samples the line at 16 times the bit rate of the signals to be received on the line. Upon detection of a mark to space transition, the UART counts eight clock pulses and checks the state of the line again. This sampling occurs in the center of the normal start bit. If the sample is a mark, the receiver return to its idling state, ready to detect another mark to space transition. If the sample is a space, the receiver enters

the data entry condition and samples the state of the line at subsequent sample points spaced at multiples of 16 clocks from the center of the start bit. The number of samples taken is determined by the character length information and parity enable programmed in the Line Parameter Register. If parity checking is enabled for the line, the receiver computes the parity of the character received and compares it with the parity sense specified for the reception on the line. If the parity does not check, the parity error bit is set.

The character length, parity, and number of stop bits that are used by the UART to perform the above operations are stored in each UART from information received from the Line Parameter Register for the associated UART.

2.4.1.2 Receiver Scanner

The receiver section of the UARTs are serviced by a receiver scanner which polls the UARTs for a line which has assembled a received character. The received character and its associated status bits are transferred to the silo, if it is not full. The receiver scanner has priority over the transmitter scanner since the transmitting output is by means of DMA and can be deferred if necessary during conditions of peak activity. In this manner, characters will not be lost or overrun conditions generated because of the operation of the controller itself.

2.4.1.3 Silo Operation

The silo for each DHll is contained in the RAM memory. A 16-bit wide by 64 word (optional 128 word) deep first-in-first-out (FIFO) storage is maintained by the controller's microprogram. In effect, a 16-bit word entered at the top of the silo is automatically shifted down to the lowest location that does not already contain an entry. The bottom of the silo is the received character register.

There are two registers associated with the silo. The received character register is a read-once register that is the bottom location of the silo. Reading it extracts the character, and its associated status, from the silo and causes all other entries to shift down one word position.

The other register is the Silo Status Register. The high byte of this register is read-only and contains the status of the number of words which fill the silo. The low byte is read-write and contains the number of characters which must be loaded into the silo before a received interrupt request will be generated.

2.4.1.4 Half-Duplex Operation

When the line is programmed for half-duplex operation, the receiver is enabled at all times except when the BAR bit for the line is set indicating that transmission is underway. The receiver is blinded from receiving the characters being transmitted, since the transmitting is done on the same circuit as the receiving. No transmit characters are sent to the silo. The line may not be in auto-echo mode when operating half-duplex, since transmitting and receiving can not be done at the same time.

2.4.1.5 Received Character Distortion

Received characters may contain up to 43.75 percent distortion on any bit due the sampling rate employed in the UART. However, the overall bit rate must be accurate. Specifically, errors in bit rate are cumulative such that when the receiver samples the first stop bit to see if it is a mark, the error accumulated by that time must not exceed 43.75 percent of the bit time. The accumulated error (called "gross start-stop distortion") is calculated as clock error times number of bits plus one, plus the bias distortion of the final character. Assuming the reception of eight data bits, or seven data bits plus parity, 4.8 percent speed distortion would be permissible. Speed distortion (clock error and bit rate error) of any amount causes severe problems to an echo situation. If a terminal sends at a slightly fast rate and the controller sends the exact same characters back to the terminal at the correct rate, the silo will eventually fill with unechoed characters.

2.4.2 Transmitter Operation

2.4.2.1 <u>UART</u>

Transmission on each line is also performed by UARTs. These MOS/LSI devices perform all the necessary functions for double buffered asynchronous character transmission. The transmitter section of the UART holds the serial output at a marking state when idle. When a character has been loaded into the transmitter holding buffer, the UART will generate a start bit within 1/16 of the bit time. The start space is followed by five, six, seven, or eight data bits and the parity bit if parity is selected. Control of the UART is performed by the Line Parameter Register. Data bits are presented to the line least significant bit first.

The minimal number of stop bits depends upon the setting in the Line Parameter Register. If transmission is in five-bit code, either one or one and half stop bits is transmitted.

If the transmitter's holding register has been loaded while a character is being transmitted, the second character will have its start bit transmitted immediately at the end of the preceding character's stop bits.

2.4.2.2 DMA Transmission

Unlike the receiver operation where the controller transfers received characters from the UART to the silo for programmed input by the CLU, the CS01/H2 performs automatic direct memory access (DMA) of characters to be transmitted. Data is accessed a word at

a time from the LSI-ll memory except for odd bytes at the beginning or end of the buffer. The low-order byte is transferred to the UART's transmitter holding buffer and the high-order byte is held in the controllers memory. The DMA accessing is controlled by the 16-bit Byte Count Register (BCR) and the 22-bit Current Address Register (CAR). The CAR is incremented by two for every word accessed from memory. The BCR is incremented by one for each byte transferred to the UART's transmitter holding buffer. The transmitting operation for a line is active only as long as the bit corresponding to the line is set in the Buffer Active Register (BAR). This bit is set under programmed control to initiate the transmitting of a buffer and is reset after the last character of the buffer has been shifted from the UART.

2.4.2.3 Auto-Echo Operation

There are provisions for the controller to echo (transmit) received characters without software intervention. This feature is enabled for each line by setting the AEE (bit 15) in the Line Parameter Register.

The auto-echo is performed by the receiver scanner. When the receiver scanner finds a received character for a line on which the auto-echo is enabled and which does not have a framing error or overrun error, it transfers the character to the transmitter holding register for the line as well as to the silo. If the transmitter holding register is not empty at the time the received character is found, the character remains in the receiver holding register until the next time the receiver scanner finds the character.

It is not advisable to simultaneously transmit messages on a line and auto-echo characters received on that line. The auto-echo feature of the controller will interlock these functions to some degree, but if more than two characters are received on a line while the scanner is waiting for the transmitter holding buffer to become available, data overrun occurs and characters are lost. Auto-echo and software driven transmission should not be attempted on the same line simultaneously if input from the line is expected.

2.4.3 Modem Control

The line interface board provides level conversion for all modem control lines. The output control functions are: Terminal Ready, Request To Send, and Secondary Transmit. The received control functions are: Clear To Send, Carrier, Secondary Receive and Ring.

The controller has a modem control scanner which scans the four modem control inputs line-by-line. When a transition is detected, the scanner is stopped with appropriate status displayed in the control status register (CSR), and an interrupt is generated. The scanner can be programmed to "free run" or can be sequentially stepped through line-by-line. The scanner may be cleared under program control to reset the scanner, its enable, and all memory associated with the transition detectors.

3.1 OVERVIEW

This section contains a detailed description of the device registers which are accessible to the Q-Bus that are used to monitor and control the CS01/H2 Communications Subsystem. The registers are functionally compatible with those of a DEC DH11 communications multiplexer with DM11 modem control.

This section also includes some general programming notes designed to aid the programmer who writes software to operate the CS01/H2, and a brief architectural description of the CC01 Controller Module.

The following table outlines the contents of this section.

Subsection	Title
3.1 3.2 3.3 3.4 3.5	Overview DHll Registers DMll Registers General Programming Notes Architecture

For quick reference, Figure 3-1 illustrates the entire DH11- and DM11-type register set. The bit mnemonics are the same as those used in the more complete descriptions that follow. The subsection numbers in Figure 3-1 reference the appropriate descriptions.

The register address is given in terms of an offset from the device's base address. Simply add the offset to the base address to obtain the correct address for a specific register (base addresses and offsets are in octal notation). Note that the base addresses for the DH11 and DM11 register sets are different.

3.2 DHll REGISTERS

There are eight 16-bit registers for the DH11. Three of these registers (LPR, CAR and BCR) are replicated for each of the 16 channels. Selection of the particular register set is made by the line number in SCR.

```
SYSTEM CONTROL REGISTER (SCR) +0
     15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
     TI SI TIE SIE MC NXM MM CNI RI RIE Al7 Al6 | Line No.
RECEIVED CHARACTER REGISTER (RCR) +2
     15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
                               Received Character
     VDP DO FE PE Line No.
LINE PARAMETER REGISTER (LPR) +4
     15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
              Tx Speed
                         Rx Speed
      0 HD
                                       OP PE 0 TSB Char.
                                                    Length
CURRENT ADDRESS REGISTER (CAR) +6
     15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
                       Current Address
BYTE COUNT REGISTER (BCR) +10
     15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
                Two's Complement of Number of Bytes
BUFFER ACTIVE REGISTER (BAR) +12
     15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
                     Transmit Enable Bits
BREAK CONTROL REGISTER (BRCR) +14
     15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
                      Break Bits
SILO STATUS REGISTER (SSR) +16
     15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
             Silo Fill Level
                               A17 A16
                                         Silo Alarm Level
CONTROL AND STATUS REGISTER (CSR) +0
     15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
     RF CF CTS 0 CS CM MM STP DONE IE SE BUSY
                                                Line No.
LINE STATUS REGISTER (LSR) +2
     15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
      0 0 A21 A20 A19 A18 A17 A16 RNG CAR CTS 0 0 RTS DTR LE
       Figure 3-1. DHll/DMll Registers CS0101-0092
```

3.2.1 SYSTEM CONTROL REGISTER (SCR) +0

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

TI	ST	TTE	STE	MC	NXM	MM	CNT	RT	RIE	A17	A16	Line No.
1	<i>D</i> T				14441		V1.1					

Read/Write, Byte Addressable

Transmitter Interrupt (TI) - Bit 15

Read/Write

Cleared by Master Clear

This bit is set when the controller increments the byte count to zero, indicating that the last character of a DMA transfer has been loaded into a UART transmitter holding register. Setting TI also causes an interrupt to be generated if TIE (bit 13) is set.

The line that caused TI to set can be determined by reading the BAR. The bit(s) that is reset and had been previously set to enable transmission identifies the line(s) that caused the interrupt. An exclusive-or comparison of the current contents of BAR and the pervious image will identify the interrupting line(s). TI must be reset before reading the BAR to allow the controller to post another interrupt.

Storage Interrupt (SI) - Bit 14

Read-Only

Cleared by Master Clear

This bit is set when the receiver scanner has found a receiver-holding register with a character in it and desires to store that character in the receiver silo, but cannot because the receiver silo is full. Setting this bit causes an interrupt to be generated if SIE (bit 12) is set.

Transmitter Interrupt Enable (TIE) - Bit 13

Read/Write

Cleared by Master Clear

Setting this bit allows the setting of TI or NXM (bit 15 or 10, respectively) to generate a transmitter interrupt request or non-existent memory interrupt request.

Storage Interrupt Enable (SIE) - Bit 12

Read/Write

Cleared by Master Clear

Setting this bit allows the setting of SI (bit 14) to generate an interrupt request.

Master Clear (MC) - Bit ll

Read/Write

Cleared by Master Clear

Setting this bit initializes the controller, clearing the silo, the UARTs and the registers. The controller resets this bit when the initialization operation is complete.

Non-Existent Memory (NXM) - Bit 10

Read-Only

Cleared by Master Clear

This bit is set when the controller is bus master during NPR transfer and does not receive a SSYN from the memory within 20 microseconds NXM is also set if a parity error is detected during a DMA (memory read) operation.

Maintenance Mode (MM) - Bit 09

Read/Write

Cleared by Master Clear

Setting this bit places the controller in the Maintenance mode. When in Maintenance mode, it is possible to write bits 07, 10 and 14 of the SCR, which are normally read-only. Also, the transmitted data signal is internally looped to the received data input.

<u>Clear Non-Existent Memory Interrupt (CNI) - Bit 08</u>

Read/Write

Cleared by Master Clear

Setting this bit clears the non-existent memory interrupt (bit 10) and clears itself.

Receiver Interrupt (RI) - Bit 07

Read-Only

Cleared by Master Clear

Setting this bit indicates that the number of characters stored in the silo exceeds the "alarm level" specified by the low byte of the SSR. Setting this bit generates an interrupt request if RIE (bit 06) is also set.

Receiver Interrupt Enable (RIE) - Bit 06

Read/Write

Cleared by Master Clear

Setting this bit allows the setting of RI (bit 07) to generate an interrupt request.

Extended Address Bits (Al7, Al6) - Bits <05:04>

Read/Write

Cleared by Master Clear

These bits are bus address bits Al7 and Al6 for the line specified in bits <03:00>. The contents of these bits are copied into the 18-bit CAR for the line when the low-order 16 bits are loaded in the CAR. When these bits are read, they do not represent the actual status of the address bits for the selected line.

NOTE

If the 22-bit addressing mode option has been selected, these bits are not used. The upper six bits of the current address are written through the high byte of the LSR.

Line Number - Bits <03:00>

Read/Write

Cleared by Master Clear

Each of the 16 channels served by the controller has its own storage for channel parameter information, current address, and byte count. These storage locations are loaded by the program via the LPR, CAR, and BCR, which are indexed by the line number in the SCR.

3.2.2 RECEIVED CHARACTER REGISTER (RCR) +2

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

ſ						
١	VDP 1	DO	FE	PE	Line No.	Received Character
•						

Read-Once, Word Addressable

This register is the bottom of the 64-word silo. Valid silo data is displayed if bit 15 is set. When this register is read the bottom word of the silo is removed, the Silo Fill Level in SSR is decremented by one, and SI in the SCR is reset.

Valid Data Present (VDP) - Bit 15

Read-Once

Cleared by Master Clear

When set, this bit indicates that the data present in bits <14:00> of this register are valid. When this register is read and bit 15 is set, the character in the low byte is valid and should be processed. The program should continue reading this register and processing characters until bit 15 is found to be reset, indicating the the receive silo is empty. An entry is lost after being read.

Data Overrun (DO) - Bit 14

Read-Once

Cleared by Master Clear

When set, this bit indicates that the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding-register or because the silo is full.

Framing Error (FE) - Bit 13

Read-Once

Cleared by Master Clear

When set, this bit indicates that the receiver has sampled a line for the first stop bit, and found the line in a spacing condition (logical zero). This condition usually indicates the reception of a Break.

Parity Error (PE) - Bit 12

Read-Once

Cleared by Master Clear

When set, this bit indicates that the parity of the received character does not agree with that designated for the channel.

Line Number - Bits <11:08>

Read-Once

Cleared by Master Clear

The state of these bits indicate the line number on which the received character was received. Bit 08 is the least significant bit.

Received Character - Bits <07:00>

Read-Once

Cleared by Master Clear

These bits contain the received character, right justified, if the valid bit (bit 15) is set. The least significant bit is bit 00.

3.2.3 LINE PARAMETER REGISTER (LPR) +4

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

0 HD Tx Speed	Rx Speed	OP	PE	0	TSB	Char. Length
---------------	----------	----	----	---	-----	-----------------

Read/Write, Byte Addressable

The LPR for all channels is cleared by Initialize and Master Clear.

Half-Duplex (HD) - Bit 14

Cleared by Master Clear

Setting this bit causes the channel to operate in half-duplex mode. If HD is reset, this channel will operate in full-duplex mode. In half-duplex operation, the receiver is blinded during transmission of a character.

Transmitter Speed - Bits <13:10>

Cleared by Master Clear

The state of these bits determines the operating speed for this channel's transmitter. See Table 3-1.

Table 3-1. Tx and Rx Speed Table

Tx Rx	13 09	12 08	Bits 11 07	10 06	Baud Rate
	0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1 0 0	0 0 1 1 0 0 1 1 0 0	0 1 0 1 0 1 0 1	Disable 50 75 110 134.5 150 200 300 600 1200 1800 2400
	1 1 1	1 1 1 1	0 0 1 1	0 1 0 1	4800 9600 19200 or 100 ¹ , ² , ³ Not Supported

When a CP34 Distribution Panel is used with the CC01 Controller Module, the rate selected by this code is determined by 2SW1-7 on the CP34.

Receiver Speed - Bits <09:06>

Cleared by Master Clear

The state of these bits determines the operating speed for this channel's receiver. See Table 3-1.

When a CP32 Distribution Panel is used with the CC01 Controller Module, the rate selected by this code is determined by 3SW2-3 on the CP32.

When a CPll or a CPl2 Distribution Panel is used the rate selected by this code is 19200.

Odd Parity (OP) - Bit 05

· Cleared by Master Clear

If this bit and PE (bit 04) are set, characters of odd parity are generated on this channel and incoming characters will be expected to have odd parity. If this bit is not set, but bit 04 is set, characters of even parity are generated on this channel and incoming characters are expected to have even parity. If bit 04 is not set, the setting of this bit has no meaning or affect.

Parity Enabled (PE) - Bit 04

Cleared by Master Clear

If this bit is set, characters transmitted on this channel have an appropriate parity bit affixed, and characters received on this channel have their parity checked.

NOTE

Switch SW1-7 on the CC01 Controller Module can override the code specified here. When SW1-7 is closed (ON) all channels will transmit two stop bits with every character.

Two Stop Bits (TSB) - Bit 02

Cleared by Master Clear

Setting this bit conditions a channel that is transmitting with six-, seven-, or eight-bit code to transmit characters that have two stop bits. If the channel is transmitting five-bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop bits. If this bit is not asserted, one stop bit is sent.

Character Length - Bits <01:00>

Cleared by Master Clear

To receive and transmit characters of the lengths (excluding parity bit) shown, these bits should be set as listed in the following table.

Bi	.t	Bits/				
01	00	Character				
0	0	5 bit				
0	1	6 bit				
1	0	7 bit				
1	1	8 bit				

3.2.4 CURRENT ADDRESS REGISTER (CAR) +6

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Current Address

Read/Write, Word-Addressable

This register contains 16 of the 18 or 22 memory address bits for the channel specified in the SCR. This register must be loaded only after the SCR has been loaded with the desired channel number and the Al7 and Al6 address bits. (If the 22-bit addressing mode option has been selected, the upper six bits of the address are loaded through the upper byte of the LSR. See subsection 4.3.4.3 for details on this option.) When this register is loaded, address bits <15:00> of this register and Al7 and Al6 from the SCR are transferred into an 18-bit CAR for the channel.

3.2.5 BYTE COUNT REGISTER (BCR) +10

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Two's Complement of Number of Bytes

Read/Write, Word Addressable

This register is loaded with the two's complement of the number of bytes to be transferred.

In the same fashion as LPR and CAR, this register must not be loaded or read without first selecting the channel number in SCR.

3.2.6 BUFFER ACTIVE REGISTER (BAR) +12

15 14 13 12 11 10 09 8 0 07 06 0.5 04 03 02 01 00

Transmit Enable Bits

Read-Modify-Write Ones-Only, Byte Addressable

Cleared by Initialize and Master Clear

This register contains one bit for each channel. The bits are set individually using BIS instructions. Setting a bit initiates transmission on the associated channel. The bit is cleared by the controller when the last character to be transmitted on that channel is loaded in the the transmitter-holding buffer of the UART. Although the clearing of a BAR bit does indicate that a new message may be sent, it does not indicate that the last characters from the preceding message have been completely sent. Specifically, two more characters are sent after the BAR bit clears. These are the last two characters of the message; one of them is starting when the BAR is cleared, and one is the final character that is loaded into the holding register at time the BAR is cleared. This effect is a normal consequence of double-buffered transmission and is mentioned here for the benefit of programmers who want to write programs that control such modem leads as Request To Send.

The software driver should maintain an image of BAR. After setting a BAR bit to initiate transission, the software image of BAR should be updated. Upon receipt of a transmit interrupt (indicating transmission is completed), bit 15 of SCR should be reset. Then, the driver should read BAR and perform an exclusive-or comparison between BAR and the software image. This action will identify the line that completed the transmission. When the line finishes transmission, the software image of BAR should once again be updated. Note that although it is possible for multiple lines to finish transmission on a single interrupt, the driver need only read BAR once for each entry into the transmit service routine. (It is possible to find that no lines have finished transmission even though an interrupt was generated. In this case, the line that caused the interrupt was detected in BAR on the previous interrupt.)

3.2.7 BREAK CONTROL REGISTER (BRCR) +14

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Break Bits

Read-Modify-Write, Byte Addressable

Cleared by Initialize and Master Clear

This register contains one bit for each channel. Setting a bit in this register immediately generates a break condition on the channel

corresponding to that bit number; clearing the bit terminates the break condition. For the break condition to occur, bits <13:10> in LPR must contain a nonzero value. A zero value in these bits disables the transmitter and inhibits a break operation. The duration of the break must be controlled by a software timer. Do not use the transmission of characters during a break interval to time the interval. Cleared by Initialize and Master Clear.

3.2.8 SILO STATUS REGISTER (SSR) +16

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

SM 0 Silo Fill Level A17 A16 Silo Alarm Level

SM 0 | Silo Fill Level | Al7 Al6 | Silo Alarm Level

Read/Write, Byte Addressable

Silo Maintenance (SM) - Bit 15

Read/Write

Cleared by Initialize and Master Clear

Each time this bit is set, a fixed binary pattern (125252_8) is sent to the silo for checking during maintenance. Clearing and setting SM loads another copy of the pattern.

Silo Fill Level - Bits <13:08>

Read-Only

Cleared by Initialize and Master Clear

These bits are an up-down counter that indicates the actual number of characters in the silo. A full silo has a count of 77_8 and an empty silo has a count of 00_8 .

NOTE

When the Expanded Silo option is activated, the entire upper byte (bits <15:08>) is used to indicate the number of characters in the silo. There is no Silo Maintenance function. A full expanded silo has a count of 3778.

Extended Memory Address (Al7, Al6) - Bits <07:06>

Read-Only

These bits contain the Al7 and Al6 bits of the current address for the channel which is selected in the SCR.

NOTE

If the 22-bit addressing mode option has been selected, these bits are not used. The upper six bits of the current address are read through the high byte of the LSR.

Silo Alarm Level - Bits <05:00>

Read/Write

Cleared by Initialize and Master Clear

The program writes a number between zero and 63 into this location. This number is the desired silo alarm level. When the number of characters stored in the silo exceeds that number, the RI (bit 07 in SCR) is set and the interrupt request is generated if enabled by RIE (SCR bit 06).

3.3 DM11 (MODEM CONTROL) REGISTERS

The controller has two registers that are associated with modem control for a 16-channel group.

3.3.1 CONTROL AND STATUS REGISTER (CSR) +0

15 14 13 12 11 10 09 0.8 07 06 05 04 03 02 01 00 RF CF CTS 0 CS MM STP DONE IE SE BUSY CM Line No.

Read/Write, Byte Addressable

This register contains modem control transition information found by the scanner. It also contains maintenance controls.

Ring Flag (RF) - Bit 15

Read-Only

Cleared by Initialize and Clear Scanner

When DONE is set, a Ring OFF to ON transition on the channel specified by bits <03:00> is indicated by setting this flag.

Carrier Flag (CF) - Bit 14

Read-Only

Cleared by Initialize and Clear Scanner

When DONE is set, a Carrier transition on the channel specified by bits <03:00> is indicated by setting this flag.

Clear To Send (CTS) - Bit 13

Read Only

Cleared by Initialize and Clear Scanner

When DONE is set, a Clear To Send transition on the channel specified by bits <03:00> is indicated by setting this flag.

Clear Scanner (CS) - Bit 11

Write-Only

Setting this bit clears all logic associated with the modem control scanner, including the stored values of Carrier and Ring for all 16 channels. This function is especially useful if the programmer requires knowledge of the ON states of Carrier and Ring. When the scanner is enabled (or a step is performed) following a Clear Scanner, an interrupt occurs for all ON states as they appear as OFF-to-ON transitions. The Clear Scanner function is not completed until BUSY is reset by the controller.

Clear Multiplexer (CM) - Bit 10

Write-Only

Setting this bit clears the Request To Send, Terminal Ready, Secondary Transmit, and Line Enable flip flops for all channels.

Maintenance Mode (MM) - Bit 09

Read/Write

Cleared By Initialize and by Clear Scanner

Setting this bit forces the scanner inputs (Ring and Carrier) to a set condition.

Step (STP) - Bit 08

Write-Only

Setting this bit causes the scanner to increment the Line Number and to test that channel for interrupt-causing transitions. Step may be used in place of Scanner Enable, but care should be exercised that the scan rate is great enough (milliseconds) such that double carrier transitions are detected. If DONE is set, the program can still increment the scanner using STP. This function is not completed until BUSY is reset by the controller.

Done (DONE) - Bit 07

Read-Only

Cleared by Initialize and by Clear Scanner

When set, the DONE flag indicates that the scanner has detected a transition which requires an interrupt to the program. An interrupt occurs if Interrupt Enable is set. When DONE is set, it inhibits the scanner from advancing and makes available:

- o The Line Number that caused the interrupt
- o The status of the flags (four bits)

The scanner is released when DONE is reset.

Interrupt Enable (IE) - Bit 06

Read/Write

Cleared by Initialize and by Clear Scanner

Setting this bit allows interrupts to be generated.

Scanner Enable (SE) - Bit 05

Read/Write

Cleared by Initialize and by Clear Scanner

Setting this bit allows the scanner to "free run," testing all channels sequentially, if DONE is reset. BUSY is set as long as the scanner is enabled.

Busy (BUSY) - Bit 04

Read-Only

This bit is set when scanner is cycling. It is reset after clearing or stopping the scanner, or after a step function is completed.

Line Number - Bits <03:00>

Read/Write

Cleared by Initialize and by Clear Scanner

This three-bit field contains the binary address of the modem scanner's position. When loading this field under program control be sure that the scanner is disabled or not busy.

3.3.2 LINE STATUS REGISTER (LSR) +2

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

0 0 A21 A20 A19 A18 A17 A16 RNG CAR CTS 0 0 RTS DTR LE

Read/Write, Byte Addressable

The LSR is replicated for all 16 channels. The LSR being addressed is determined by the channel number in the CSR for the lower byte, and by the channel number in the SCR for the upper byte.

Extended Address Bits 21:16 (A21:A16) - Bits <13:08>

Read/Write

These bits are used to specify the most significant six bits of the 22-bit buffer address in the CAR for the line specified by the SCR. When read, these bits indicate the status of (A21:A16) of the 22-bit Current Address for the line specified by the SCR. Subsection 3.4.3 provides the programming procedure for 22-bit addressing.

NOTE

When writing to the high byte, you must use a byte write.

NOTE

These bits will be used as the high-order bits of the CAR only if the 22-bit addressing mode option is selected by switch SW1-8 on the CC02 Controller Module. See subsection 4.3.4.3 for details.

NOTE

(A21:A16) must be set to their desired state **before** writing to the CAR. Also, the correct status of these bits cannot be read until **after** writing to the CAR.

Ring (RNG) - Bit 07

Read-Only

This bit reflects the status of the modem Ring (or Data Set Ready) lead.

Carrier (CAR) - Bit 06

Read-Only

This bit reflects the status of the modem Carrier Detect lead.

Clear To Send (CTS) - Bit 05

Read-Only

This bit reflects the status of the modem Clear to Send lead.

Request To Send (RTS) - Bit 02

Read/Write

Cleared by Initialize and by Clear Multiplexer

Setting this bit conditions the modem to transmit if all other conditions are met.

<u>Data Terminal Ready (DTR) - Bit 01</u>

Read/Write

Cleared by Initialize and by Clear Multiplexer

Setting this bit causes the DTR pin of the specified port's interface to become asserted (ON).

Line Enable (LE) - Bit 00

Read/Write

Cleared by Initialize and by Clear Multiplexer

Setting this bit allows the Ring and Carrier inputs to be sampled by the program and to be tested for transitions.

3.4 DH11/DM11 GENERAL PROGRAMMING INFORMATION

Specific controller functions of interest to programmers are summarized in this subsection.

3.4.1 INITIALIZE

A Q-Bus INIT signal clears the silo, the UARTs and all registers except CAR and BCR. All scanners are forced to channel zero and all memory associated with transition detectors is cleared.

MC (SCR bit 11) performs an initialization of the DH11 portion of the controller. CS (CSR bit 11) clears the scanner and transition detector logic of the DM11 portion of the controller.

The type of clear for each bit is described in the definition of each bit in the register sections.

3.4.2 INTERRUPTS

The controller generates five kinds of interrupts:

Receiver Interrupt (SCR bit 07) - This interrupt, when enabled by RIE (SCR bit 06), occurs whenever the number of entries in the silo exceeds the silo alarm level that the program has stored in low-byte of the SSR.

Storage Overflow Interrupt (SCR bit 14) - This interrupt, when enabled by SIE (SCR bit 12), occurs when the receiver scanner attempts to put a character into the silo which already contains 64 entries (full). Should this occur, data is not necessarily lost since the character which was to have been moved to the silo is still in the UART's receiverholding register.

Transmitter Interrupt (SCR bit 15) - This interrupt, if enabled by TIE (SCR bit 13), occurs whenever a channel has finished transmitting a complete string of characters. Specifically, it occurs when the corresponding BAR bit is reset at the time the last character has left the shift register of the UART.

Non-Existent Memory Interrupt (SCR bit 10) - This interrupt, when enabled by TIE (SCR bit 13), occurs when the controller detects no response from the addressed memory or when a parity error is detected in the accessed word.

Modem Transition Interrupt (CSR bit 07) - This interrupt, if enabled by IE (CSR bit 06), occurs whenever the modem control scanner detects a transition on an enabled modem control input.

3.4.3 <u>22-BIT ADDRESS PROGRAMMING PROCEDURE</u>

This subsection provides the programming procedure for 22-bit DMA addressing on the CS01/H2 Communications Subsystem for the DH11/DM11 emulation. The following steps provide the programming procedure.

- 1. To set up the CS01/H2 DH11/DM11 emulation with a 22-bit DMA address:
 - a. Lockout interrupts.
 - b. Load the desired channel number in the DH11 SCR, bits <03:00>.
 - c. Load bits <21:16> of the desired 22-bit DMA address in the DMll LSR, bits <13:08>. Use a 'MOVB' (high byte) instruction only.
 - d. Load bits <15:00> of the desired 22-bit DMA address in the DH11 CAR.
 - e. Enable interrupts.

2. To read the 22-bit DMA address:

- a. Lockout interrupts.
- b. Load the desired channel number in the DH11 SCR, bits <03:00>.
- c. Read the DH11 CAR to obtain 22-bit DMA address bits <15:00>.
- d. Read the high byte of the DM11 LSR (bits <13:08>) to obtain 22-bit DMA address bits <21:16>.
- e. Enable interrupts.

- 3. It is important to understand the following information concerning read/write accesses to the DMll LSR.
 - a. The line pointer for the high byte (DMA address bits of <21:16>) of the DM11 LSR is bits <03:00> of the DH11 SCR.
 - b. The line pointer for the low byte of the DM11 LSR is bits <03:00> of the DM11 CSR.
 - C. A write word to the DMll LSR will be treated as a write low byte.
 - d. When accessing the high byte of the DM11 LSR, use a 'MOVB' instruction only. DO NOT use BIS(B) or BIC(B) instructions.

3.4.4 RECEIVER OPERATION

3.4.4.1 Receiver Scanner

The receiver section of each UART is serviced by a receiver scanner which polls the UARTs for a channel which has assembled a received character. Each of the two channels in the UART has a receive character first-in-first-out (FIFO) buffer which is four deep. The received character and its associated status bits are transferred to the silo, if it is not full. The receiver scanner has priority over the transmitter scanner because the Transmit operation is by means of DMA and can be deferred if necessary during conditions of peak activity. In this manner, characters are not lost and no overrun conditions are generated because of the operation of the controller itself.

3.4.4.2 Silo Operation

The silo for the DHll is contained in the RAM memory. A 16-bit wide by 64-character deep FIFO storage is maintained by the controller's microprogram. In effect, a 16-bit word entered at the top of the silo is automatically shifted down to the lowest location that does not already contain an entry. The bottom of the silo is the received character register.

There are two registers associated with the silo. RCR (see subsection 3.2.2) is a read-once register that is the bottom location of the silo. Reading RCR extracts the character and its associated status from the silo and causes all other entries to shift down one word position.

The other register is SSR. Bits <13:08> of this register are readonly; that six-bit binary number represents the number of characters in the silo. The low byte is read/write and sets/indicates the number of characters which must be loaded into the silo before a received interrupt request will be generated.

3.4.4.3 <u>Half-Duplex Operation</u>

When a channel is programmed for half-duplex operation, the receiver is enabled at all times, except when the BAR bit for the channel is set, which indicates that transmission is underway. The receiver is blinded from receiving the characters being transmitted, because the transmitting is done on the same circuit as the receiving. No transmit characters are sent to the silo.

3.4.5 TRANSMITTER OPERATION

3.4.5.1 DMA Transmission

Unlike the receiver operation where the controller transfers received characters from the UART to the silo for programmed input by the CPU, the CS01/H2 performs automatic direct memory access (DMA) of characters to be transmitted. Data is accessed a word at a time from the memory, except for odd bytes at the beginning or end of the The low-order byte is transferred to the UART's transmitterholding buffer, and the high-order byte is held in the controller's The DMA accessing is controlled by the contents of 16-bit BCR and the 18-bit CAR. The CAR content is incremented by two for every word accessed from memory. The BCR content is incremented by one for each byte transferred to the UART's transmitter holding buffer. A channel transmits only as long as the bit corresponding to the channel is set in BAR. This bit is set under program control to initiate the transmission of a buffer's contents, and it is reset after the last character of the buffer has been shifted from the UART.

3.4.5.2 Modem Control

The controller PCBA provides level conversion for modem control channels. The output control function is: Data Terminal Ready. The input control functions are: Carrier and Ring.

The controller has a modem control scanner which scans the two modem control inputs channel-by-channel. When a transition is detected, the scanner is stopped with the appropriate status entered in CSR, and an interrupt is generated if the appropriate interrupt enable bit is set. The scanner can be programmed to "free run" or can be sequentially stepped through channel-by-channel. The scanner may be cleared under program control. The Clear resets the scanner, its enable, and all memory associated with the transition detectors.

3.5 CC01 CONTROLLER ARCHITECTURE

The controller is organized around an eight-bit high-speed bipolar microprocessor which performs all controller functions. The ALU and register file portion of the microprocessor are implemented with two 2901 bit-slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with 12 2K X 4-bit PROMs.

A 4K x 8-bit high-speed random access memory (RAM) holds the contents of device registers, silo buffer and working storage for the microprocessor. The RAM is both a source and destination to the internal data bus and is addressed directly and indirectly by the microprocessor.

The Q-Bus interface consists of 42-bit bi-directional and two unidirectional signal channels. The Q-Bus interface is used for programmed I/O, CPU interrupts and DMA Data Transfer operations. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA Read operations.

3.5.1 RECEIVER OPERATION

Reception on each channel is by means of Universal Asynchronous Receiver/Transmitters (UARTs). These MOS/LSI devices perform all the functions of double buffered asynchronous character assembly. receiver section of the UART samples the channel at 16 times the bit rate of the signals to be received on the channel. Upon detection of a mark-to-space transition, the UART counts eight clock pulses and checks the state of the channel again. This sampling occurs in the center of the normal start bit. If the sample is a mark, the receiver returns to its idling state, ready to detect another markto-space transition. If the sample is a space, the receiver enters the data entry condition and samples the state of the channel at subsequent sample points spaced at multiples of 16 clock pulses from the center of the start bit. The number of samples taken is determined by the character length information and parity enable programmed in the device registers. If parity checking is enabled for the channel, the receiver computes the parity of the character received and compares it with the parity sense specified for reception on that channel. If the parity does not check, the parity error bit is set.

The character length, parity, and number of stop bits that are used by the UART to perform the above operations are stored in each UART from information received from the device register controlling the line parameters for the associated channel in the UART.

3.5.2 TRANSMITTER OPERATION

Transmission on each channel is also performed by UARTs. These MOS/LSI devices perform all the necessary functions for double buffered asynchronous character transmission. The transmitter section of the UART holds the serial output at a marking state when idle. When a character has been loaded into the transmitter- holding buffer, the UART generates a start bit within 1/16 of the bit time. The start space is followed by five, six, seven, or eight data bits and the parity bit if parity is selected. Control of the UART is performed by the device register controlling the line parameters. Data bits are presented to the channel with the least significant bit first.

If the transmitter's holding register has been loaded while a character is being transmitted, the the start bit of the second character is transmitted immediately at the end of the preceding character's stop bits.

BLANK

This section describes the step-by-step procedure for the installation of the CS01/H2 communication controller in a Q-Bus environment. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the CS01, is covered in paragraph 4.1).

Emulex recommends that Section 4 be read in its entirety before installation is begun.

- 1. Inspect the CS01.
- 2. Prepare the CPU.
- Configure the CC01 controller.
- 4. Configure the CPll distribution panel.
- 5. Configure the CAll line adapters.
- 6. Install the distribution panels with the line adaptors.
- 7. Install the CCOl controller.
- 8. Cable the subsystem.
- 9. Test the subystem.

4.1 INSPECTION

Before unpacking the CS01, examine the packaging for any signs of damage. Notify the carrier if any damage is noted.

Make a visual inspection of the CC01 controller board and CP11 distribution panel after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROM's should be examined carefully to insure that they are firmly and completely seated in their sockets.

Be sure that you have received all the components that you ordered.

4.2 PREPARE THE CPU

Power down the system and switch OFF the main AC breakers. If the CPU is mounted in a rack, slide the CPU out to gain access to the card cage. Remove the rear cabinet door to expose the RETMA rails. If the LSI is a stand-alone model, remove the cover.

4.3 CONTROLLER BOARD SETUP

Reference Figure 4-1 for the location of all controller PCBA switches referred to in the paragraphs below.

4.3.1 Number of DHll Emulations

The number of DH11 emulations is selected by SW1 in accordance with Table 4-1. Each 16 line CP11 distribution panel (even if only eight lines are installed) represents one DH11; consequently, the number of emulations equals the number of panels.

Table 4-1 Number of DHll Emualtions

No.	SV	V 1-
Panels	3	2
1	0	0
2 3	0	С
3	C	0
4	С	С

4.3.2 Q-Bus Starting Address

The DHll and DMll Q-Bus addresses are set in accordance with Table 4-2. The DHll uses the floating address space that begins at 17760010 and it is located after any DJlls. Each CS01/H2 requires a set of eight word addresses starting with an address which is a multiple of 20_8 . All CS01s should have consecutive addresses. Each DJll in the system, plus one for the gap to indicate there are no more, requires a starting address which is a multiple of 10_8 starting at 17760010. Therefore, the first CS01/H2 will have a starting address of 17760020 if there are no DJlls, and a starting address of 17760040 if there are one or two DJlls.

If more than one DH11 is being emulated, select an initial starting address with enough starting addresses above it for each emulation. The starting addresses will be contiguous. That is, if three CP11 distribution panels are installed (three DH11 emulations, essentially) and the starting address selected is 17760060, then the CC01 controller will also respond to accesses in the address ranges starting at 17760100 and 17760120. The second and third starting addresses represent the second and third DH11 devices that are being emulated.

The starting address for the DMll is selected by the same switches that select the DHll address (see Table 4-2). There is a DMll for each DHll. The DMll addresses are a multiple of 10_8 .

Table 4-2 Q-Bus Starting Address Selection

Address	Range 1*	Address	Range 2	Address	Range 3	SWl			SW4		
DH11	DMĺl	DHll	DMĬl	DHll	DM11	4	1	2	3	4	5
760020	770500	760220	770600	761020	770500	С	0	0	0	0	С
760040	770510	760240	770610	761040	770510	Ç	.C	0	_0	0	С
760060	770520	760260	770620	761060	770520	Č	0	C.	0	0	C
760100	770530	760300	770630	761100	770530	. C	С	C.	0	0	C -
760120	770540	760320	770640	761120	770540	С	0	Ö	С	0	С
760140	770550	760340	770650	761140	770550	С	С	0	С	0	С
760160	770560	760360	770660	761160	770560	C	0	С	С	0	C
760200	770570	760400	770670	761200	770570	С	С	С	С	0	С
760220	770600	760420	770700	761220	770600	С	0	0	0	С	С
760240	770610	760440	770710	761240	770610	С	С	0	0	С	С
760260	770620	760460	770720	761260	770620	С	0	С	0	С	С
760300	770630	760500	770730	761300	770630	Ċ	С	C	0	С	С
*	. 3 . 3										
Standai	d Addres	s kange									

Table 4-3
DHll Vector Address Selection

				SW2-						SW2-	-	
	Addr	5	4	3	2	1	Addr	5	4	3	2	1
	300	0	0	0	0	0	 500	С	0	0	0	0
	310	0	0	0	0	C	510	С	0	0	0	С
	320	0	0	0	C	0	520	С	0	0	C	0
•	330	0	0	0	C	C	530	С	0	0	С	С
_ \	340	0	0	С	0	0	540	С	0	C	0	0
>	[∆] 350	0	0	С	0	С	550	С	0	C	0	С
54.	360	0	0	<u>C</u> ·	C	0	560	С	0	С	C	0
	370	0	0	C	С	С	570	С	0	С	С	С
	400	0	C	0	0	0	600	С	С	0	0	0
	410	0	C	0	0	С	610	С	С	0	0	С
	420	0	С	0	С	0	620	C	С	0	С	0
	430	0	С	0	С	С	630	С	С	0	С	С
	440	0	C	С	0	0	640	С	С	С	0	0
	450	0	C	C	0	C	650	C	C	C	0	C
	460	0	C	C	C	0	660	C	C	С	C	0
	470	0	С	С	С	С	670	С	С	С	С	С

Table 4-4
DMll Vector Address Selection

Addr	6	5		73- 3	2	1	Addr	6	5		۷3 – 3	2	1
Addr 300 304 310 314 320 324 330 344 350 364 370 374 400 404 410 414 420		5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	2 0 0 C C 0 0 C C 0 0 C C 0 0 C C 0	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr 500 510 514 520 534 554 554 554 560 610 614 620	6 0000000000000000000000000000000000000	5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0000000000000000000000000000000000000
404 410	0 0	С С С	0	0 0	0 C	C 0	604 610	0000000	С	0 0	0	0 C	0000000
440 444 450 454 460 464 470	0000000	00000000000	00000000	00000000	00000000	00000000	640 644 650 654 660 664 670	00000000	00000000	00000000	00000000	00000000	00000000

4.3.2.1 Alternate Unibus Starting Addresses

Two alternate Unibus address ranges are available on the CSO1/H2. The alternate ranges require different address decode PROMs, which may be ordered from Emulex. The table below describes the address ranges and the option kits which provide the alternate PROMs.

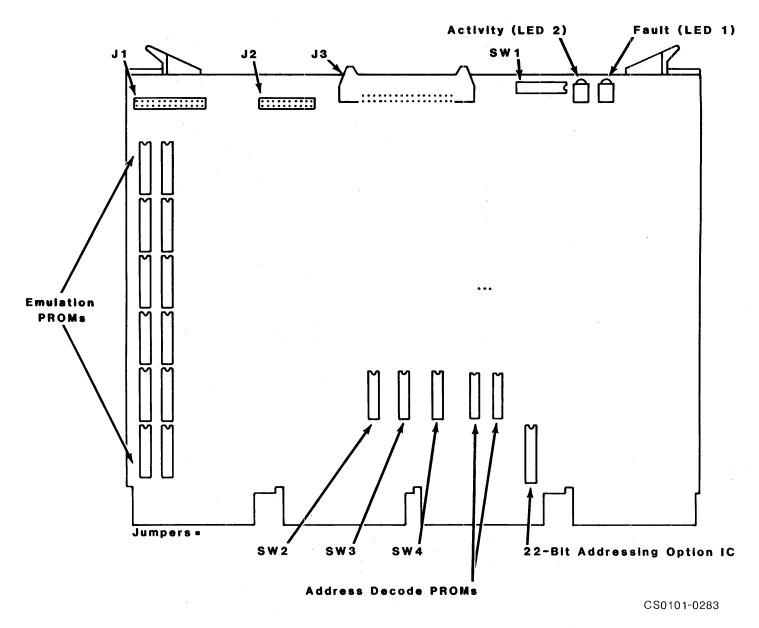


Figure 4-1 CC01 PCBA

Address Range	PROM Numbers	PCBA Locations	Option Kit Number
1*	018A 019A	U81 U82	Standard
2	018A 797A	U81 U82	CC1111727
3	018A D00A	U81 U82	CC0111702

4.3.3 <u>Interrupt Vector Address</u>

4.3.3.1 DHll Vector

The DHll interrupt vector address is set by the switches in SW2 in accordance with Table 4-3. Each DHll requires two interrupt vectors. The receiver vector is XX0; the transmitter vector is XX4. The DHll falls in behind the DCll, KLll, DPll, DNll, DMll, DRll, PA6ll, DXll, DLll and DJll. Remember to count the vectors of the associated DMlls and any other DMlls or DHlls with lower Q-Bus addresses.

4.3.3.2 DMll Vector

The DMll interrupt vector address is set by the switches in SW3 in accordance with Table 4-4. Each DMll requires one interrupt vector. The vector addresses are assigned starting at 300. The DMll falls in behind the DCll, KLll, DPll and DNll. Remember to count other DMlls on the bus which have lower Q-Bus addresses.

4.3.3.3 Interleaving DHIL and DMIL Vector Addresses

In order to interleave the DH1l and DM1l interrupt vector address option switch SW1-5 must be closed. When enabling this option, it is important to set the addresses so that they do not overlap. This can be accomplished by setting the first DH1l vector 10° higher than the first DM1l vector. Thus, if the first DM1l vector is set at 300, the first DH1l vector must be set at 310, and the second DH1l vector will occupy 314. The next open address is 320, so the DM1l vector will be assigned to that and so on. The chart

below provides a sampling of typical interleaved interrupt vector assignments.

DMll	DHll
300	310
320	314 330
340	334 350
	354
360	370 374

4.3.4 Option Selection

4.3.4.1 Option Switches

Reference Appendix A for the selection of options not discussed in the paragraphs below.

4.3.4.2 Extended Silo Option

Setting option switch SW2-7 ON will enable the Extended Silo Option.

4.3.4.3 <u>22-Bit Memory Addressing</u>

Twenty-two bit addressing capability is available as an option for the CS01. The Emulex part number for the option kit is CS0113001. The kit consists of a single AMD2908 IC which is placed in socket U101 on the CS01 PCBA. See paragraph 2.5.2 for programming instructions.

WARNING

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing a CSO1 with the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. A CSO1 without the addressing option will not be damaged if power is present on those lines.

4.4 CP11 DISTRIBUTION PANEL CONFIGURATION

4.4.1 Panel Numbering

There is no address selection to be done on the CPll Distribution Panel. Each panel takes on a number corresponding to its position

on the daisy-chain cable. The number of CPll panels is selected by switches SWl-2 and SWl-3 on the CC0l controller PCBA. See Table 4-1 for switch setting information. The switches on the CPll are not used and should be ignored.

4.4.2 International Power Supply Conversion Instructions

The power supply accompanying your order is wired for 115 v AC. To convert the power supply to 220 v proceed as follows;

- 1) Make sure the power supply is not plugged in.
- 2) Replace the existing lA slow/blow fuse with the enclosed l/2A slow/blow fuse. The fuse plug is on the left hand side when viewed from the front.
- 3) Move the slide switch to the 230 v position. The switch is next to the fuse holder.
- 4) Remove the existing AC plug and replace it with the type desired for your application. The wire coloring code is: green--safety ground; white--neutral; black--AC power.

4.5 LINE ADAPTOR CONFIGURATION

The CAll/H (RS-232-C) has several user selectable options that are effected using a switch and several wirewrap jumpers. The switch is used to select the compatiblity mode of the entire unit (see 4.5.1.1). All of the other available options can be selected for each channel individually by rearranging the jumpers. See Figure 4-2 for the locations of the switches and jumpers on the CAll/H.

The CAll/C (20 mA current loop) Line Adaptor Panels has several user selectable options. All of the options are selected for each channel individually by rearranging the jumpers. See Figure 4-3 for the locations of the switch and jumpers on the CAll/C.

The following procedure is a general one to be used when reconfiguring either type adaptor. Refer to the appropriate paragraph (below) for specific jumper connections when you reach step 7. When configuring the adaptors for initial installation, only steps 2 through 11 will apply as the distribution panel will not yet have been installed.

- 1) Unplug the 34-wire ribbon cable from the CPll Distribution Panel.
- 2) Turn off the AC power to the Distribution Panel by unplugging the AC line cord.
- 3) Unscrew the knurled screw at each corner of the adaptor. They need not be completely removed.

- 4) Grasp the handles in the upper left and right hand corners of the adapter and pull the adapter from the AMP MOD 1 pins on the Distribution Panel.
- 5) Remove the four screws that hold the two panel handles in place and remove the handles.
- 6) Unscrew the four counterset screws that hold the face plate on the adaptor PCBA and remove the face plate.
- 7) Make the wire wrap changes as required.
- 8) Replace the face plate on the adapter PCBA.
- 9) Replace the two panel handles.
- 10) Fit the adapter panel to the AMP pins and press the panel home.
- 11) Tighten the four knurled screws.
- 12) Plug in the Distribution Panel's AC line cord.
- 13) Plug in the 34-wire cable.
- 14) All of the Adapter Panel LEDs will be lit. Move the LINE TEST slide switch from the OFF to the INT position and back again. This will cause the controller to test each channel. All of the LEDs should go out.

4.5.1 CAll/H Option Selection

4.5.1.1 Flow Control Option

If desired, the CAll/H may be configured to use Clear to Send (CTS pin 5) and Carrier Detect (CD pin 8) for flow control as required by some peripheral devices. This is done by opening SW2-2. SW2 is the piano type switch mounted under the face plate on the left edge of the CAll PCBA. If necessary, use a screwdriver to set SW2-2 to the up (open) position.

When in this mode, the UART's transmitter is controlled by the CTS line. When CTS is active (high) the transmitter is enabled. When it is inactive (low) the transmitter is disabled. (The UART will finish transmitting any character it had started before CTS became inactive.)

When this option is enabled, the UARTs receiver is controlled by Carrier Detect (CD). Therefore, if the peripheral can be expected to transmit anything back to the CAll, CD will have to be biased active (high) in order to enable the receiver. Generally, one of the signals generated by the peripheral such as Data Set Ready (DSR

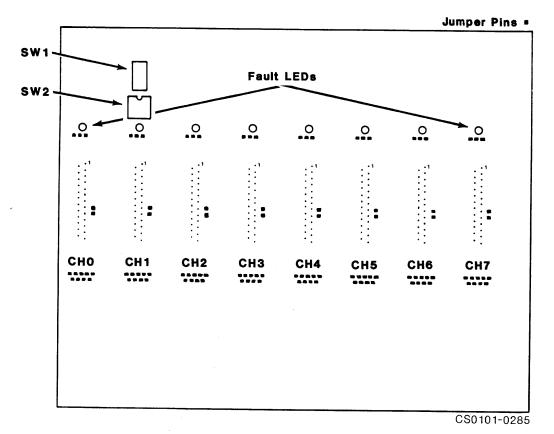


Figure 4-2 CAll/H Line Adapters

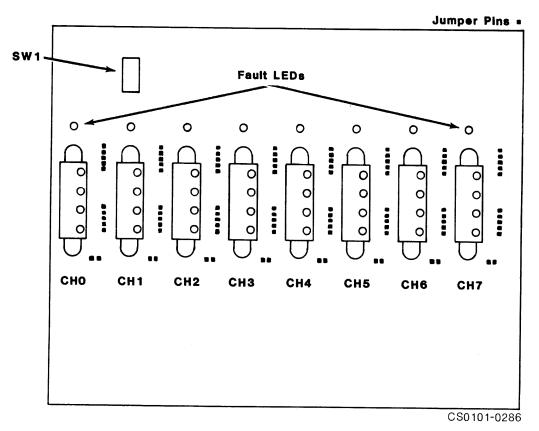


Figure 4-3 CAll/C Line Adapters

pin 6) or Data Terminal Ready (DTR pin 20) is always active and can be connected to CD to accomplish this. Also, some devices have +v on pin 9 of the interface. In all cases, the bias should be in the range +15 to +3 v DC with respect to pin 7 (signal gound).

NOTE: SW2-2 selects the flow control option for all eight lines on the adaptor panel. Consequently, if flow control is required on only one port (for a printer, for example), the rest of the lines must have both CTS and CD biased high in order to function.

4.5.1.2 Pinning Assignment Options

The CAll/H is shipped from the factory with the following jumper connections:

Connection	Function
A to B	Connects RING (pin 22) to DSR input on UART.
R to P	Connects RTS output on UART to pin 4.
S to T	Connects Sec TX output to pin 11.

To effect one of the following options, reconfigure the wirewrap jumpers as indicated for that option. Each channel is reconfigured separately.

- 1) RS-232 Secondary Receive and Secondary Transmit (pins 16 and 14, respectively) rather than Bell 202C pinning assignments: Remove S T; Jumper S J; Jumper U G on back of board (cut etch H G if necessary to isolate pin 12).
- Substitute Data Set Ready for Ring: Remove B A; Jumper C A.
- 3) For 103 E,G,H,J modems, connect Busy (pin 25) with RTS (pin 4): Jumper R L.
- 4) For 212 A modems, connect Make Busy (pin 18) with RTS (pin 4): Jumper R N.



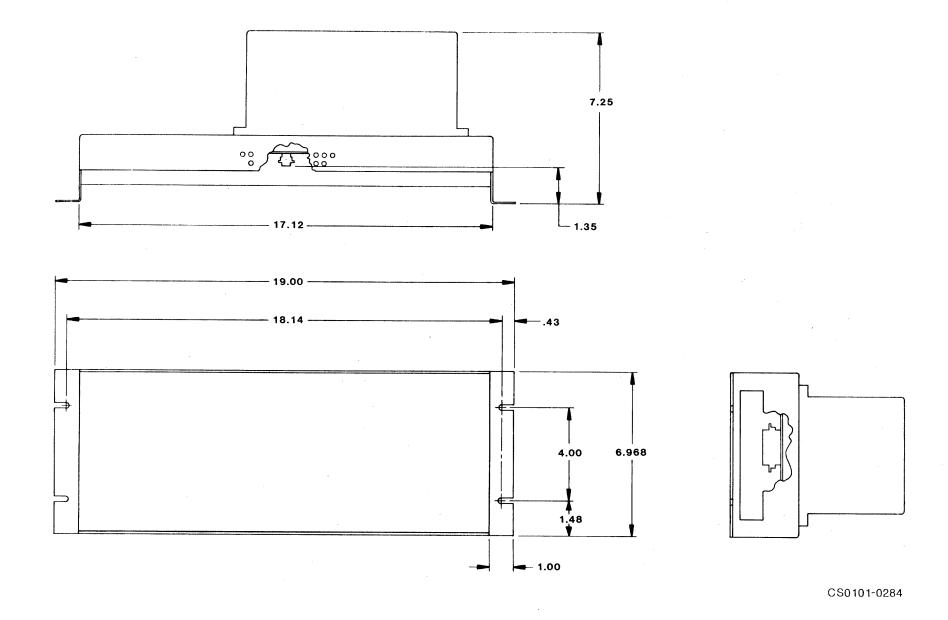


Figure 4-4 Distribution Panel Physical Dimensions

4.5.2 CAll/C Option Selection

The standard jumper connections are:

Connection	Function
A-B, C-D	Active transmitter, active receiver, 12 vDC

To effect one of the following options, reconfigure the wirewrap jumpers as indicated for that option. Each channel is reconfigured separately.

- Long Line (L.L.) transmit option (active, 24 vDC): Remove C
 D; Jumper D E.
- 2) Long Line (L.L.) receive option (active, 24 vDC): Remove H
 J; Jumper J K.
- 3) Passive transmit option (passive operation reverses indicated terminal polarity): Remove A - B, C - D (or D -E); Jumper A - D.
- 4) Passive receive option (passive operation reverses indicated terminal polarity): Remove F G, H J (or J K); Jumper F J.
- 5) Install Receive Filter: Jumper L M.

4.6 CP11 DISTRIBUTION PANEL INSTALLATION

The distribution panels can be installed with the line adapters in place. See Figure 4-4 for panel dimensions pertinent to mounting.

The distribution panels are usually mounted to the RETMA rails of a rack or cabinet. The panel is recessed so that the connectors and their cables do not get in the way of the door or side panel of the cabinet.

NOTE: If a panel is not to be mounted in the cabinet with the controller, then the panel case must be connected to the CPU cabinet by a ground strap.

4.7 CC01 CONTROLLER INSTALLATION

4.7.1 Slot Selection

The controller board may be placed in any slot in the LSI-11. The controller should be placed fairly close to the CPU so as to give it higher interrupt priority than other devices even though it does not need a high NPR priority. In all cases, Emulex disk controllers should be after the CCOl since they have a large amount of buffering.

4.7.2 Controller Mounting

The controller board should be plugged into the Q-Bus backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the board with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly in the throat of the connector before attempting to seat the board by means of the extractor handles.

4.8 CABLING

4.8.1 Controller to Distribution Panel

A 34-conductor flat cable daisy-chains between the CC01 controller and the distribution panels. The cable plugs into Jl on the controller with pin 1 on the top (front) of the board. The pin 1 of the cable connector has a notch on the body to identify it. Also, the pin 1 edge of the cable has a black stripe.

The cable from the controller plugs into the top connector (J1) on the back of the distribution panel. If only one panel is to be used with the controller, the terminator plug is inserted into the bottom connector (J2). If more than one panel is to be used, a cable is plugged into J2 and connected to J1 of the next panel. The terminator card must be plugged into J2 of the last panel.

The panels are assigned addresses based on their order on the cable. The first panel will be the DHll with the lowest Q-Bus address, the next panel will have the next higher Q-Bus address, etc.

4.8.2 CAll/H Line Adaptor to External Device

The CS01 communications multiplexer is used to provide communications between the host CPU and up to 64 external devices through individual ports. The external devices can be of various sorts, but they can be roughly grouped into two classes: local (no modem control signals required) and remote (modem control signals required).

4.8.2.1 Cable Types

Devices that are in the local class (terminals, printers) can be connected to a port using a simple four wire-cable called a terminal cable. A schematic of the standard DEC cable for local devices is shown in Figure 4-5.

Devices that are in the remote class (modems, other computers) require cables that can carry the modem control signals. Figure 4-6 is a schematic of a modem cable.

The CS01 hardware is unable to make the distinction between local and remote devices. The host operating system is told whether to use the remote or local mode for each line. If this is impractical

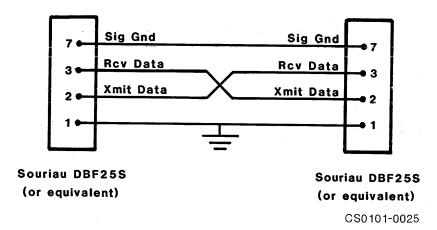


Figure 4-5 Terminal Cable Schematic

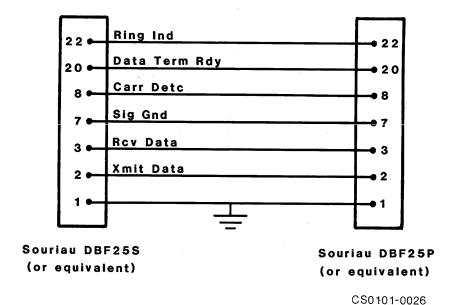
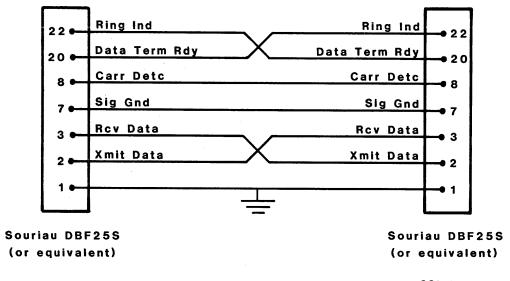


Figure 4-6 Modem Cable Schematic



CS0101-0027

Figure 4-7 Null-Modem Cable Schematic

because modems are constantly being moved from one line to another, then the remote mode is often specified for all of the communications ports. In such cases, the four-wire cable described for local devices will not work because the software will generate modem control signals and expect to receive the correct responses in return. Thus, devices that would normally be in the local class are connected to their ports using null-modem cables. These cables interconnect the modem control signals to give the software the illusion that it is talking to a modem. The standard DEC null-modem cable is shown schematically in Figure 4-7.

The standard CAll/H interface pinning assignments are the same as DEC's DHll with DMll modem control. As such, the pinning assignments are those for Bell 202C Data Sets (modems). The CS01/H2 may be used as delivered with DEC equipment and software. If a different modem is required, the CAll/H's pinning assignments may be changed as needed. See CAll/H Option Configuration, paragraph 4.5.1, for instructions. Note, however, that DEC software drivers may not support the optional modem configurations.

If any alternate pinning assignments described in paragraph 4.5.1 are used, the cables described above may not work.

4.8.2.2 Cable Lengths

The EIA RS-232-C interface standard to which the CS01 conforms guaranties error free transmission over cables of no longer than fifty feet. EMULEX DOES NOT WARRANTY OPERATION OVER CABLE LENGTHS

GREATER THAN 50 FEET IN ANY CIRCUMSTANCES. However, satisfactory performance over cables of several thousand feet in length can be obtained depending on the speed of data transmission required and the environment in which the cable is placed. Emulex offers the following table as a guide for the pratical application of the CS01.

NOTE: The ground potential difference between the CS01 and terminal must not exceed 2 v. This requirement will generally limit operation without modems to within a single building served by one AC power service. In other cases, or in noisy electrical environments, 20 mA operation should be considered.

Table 4-5 RS-232-C Cable Lengths

Baud	Shielded, (in feet)	Unshielded ₂ (in feet)
110 300 1200 2400 4800 9600	5000 5000 3000 1000 1000	3000 3000 3000 500 250 250

Cable is two, 22 AWG twisted pairs shielded in Belden 8777 (three pair). Shields tied to ground.
Cable is 22 AWG 4-conductor (quad) inside station wire.

4.8.3 CAll/C Line Adaptor to External Device

The CAll/C provides 20 mA current loop interface for use with older teletype-style equipment or in environments with a great deal of electrical noise.

4.8.3.1 Cable Type

The CAll/C comes configured with active transmitters and receivers. As such, each device with which the CAll/C interfaces must have a passive transmitter and receiver. Determine whether or not individual devices have active or passive interfaces by consulting the manual for that device. If a device has an active transmitter and/or receiver, the CAll/C may be reconfigured for passive operation as described in paragraph 4.5.2.

NOTE: When passive operation is selected for a CAll/C channel, THE TERMINAL POLARITY IS REVERSED from that which is printed on the CAll/C's face.

When connecting a device to an adaptor channel, these rules must be followed. Remember, if a channel receiver and/or transmitter has

been reconfigured for passive operation, the polarity of the terminals will be reversed.

- The T+ terminal of the CAll/C is connected to the R+ terminal of the slave device.
- 2) The T- terminal of the CAll/C is connected to the Rterminal of the slave device.
- 3) The R+ terminal of the CAll/C is connected to the T+ terminal of the slave device.
- 4) The R- terminal of the CAll/C is connected to the T-terminal of the slave device.

4.8.3.2 Cable Length

No definitive 20 mA current loop specification exists. The length of cable that may be used is a function of electrical noise, loop resistance, cable type and speed of operation. The following table is given as a practical guide to the cable lengths that can be used with the CAll/C adaptor panel; however, there is no guarantee of error free operation under all circumstances.

Table 4-6 20 mA Current Loop Cable Lengths

Baud	Shielded (in feet)	Unshielded ₂ (in feet)
9600	500	1000
4800	1000	1800
2400	2000	3000
1200	4000	5000

Belden 8777, 22 AWG, shielded, twisted pairs (sheild floating). 22 AWG, 4 conductor inside station wire.

4.9 VERIFICATION

4.9.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. The test is not executed with every bus INIT but only on powering-up. If the self-test has been executed successfully, the Fault LED on the top edge of the board will be off. If the LED is ON, the controller did not pass its self-test and the controller cannot be addressed from the CPU.

In addition to the controller self-tests executed when powering-up, the electronics associated with each line on the distribution panel and each line adaptor are tested. If any failures occur, the LED above the faulty line or lines will remain ON. LEDI on the CCOl will also be ON in the event of a line failure. If the overide switch (SWI-6) is OFF and a fault is detected with one of the lines, the controller will hang. If the override switch is ON, the Fault light above the bad channel will still come ON, but the controller will not hang. In this mode LEDI will not come ON.

NOTE: If any distribution panel has only one line adaptor (eight lines), then the controller will detect a line adaptor fault. If such a configuration is used, the override switch must be on to prevent the controller from hanging.

The override switch has nothing to do with the controller's own self-test. That is, if the controller detects a fault in itself, it will hang regardless of the override switch's position.

4.9.2 Register Examination

After powering-up the CPU and noting that the FAULT indicator is not ON, a quick check should be made to insure that the controller registers can be read from the computer console. This can be done by depositing 177777 in location SCR + 10 (BCR) and then examining the location for 177777.

4.9.3 Line Adaptor Wrap-Around Test

The CC01 controller is capable of running both internal and external wrap-around tests for each channel that is connected to it. For both the CA11/H and the CA11/C Line Adaptors, the internal wrap-around tests are performed during the controller power-up self-test. If desired, both the internal and external wrap around tests may be initiated on a adaptor-by-adaptor basis by the slide switch located on each adaptor panel. The internal test should be run during verification. The external test need only be run if a fault is suspected. The following paragraphs describe the test procedure for both Line Adaptors.

4.9.3.1 <u>CAll/H Tests</u>

Internal Wrap-Around Test: The internal wrap-around test is run by simply placing the slide switch in the INT position for each adaptor panel that is to be tested. The controller will then select a loop-back data path, transmit a character, and then read the receive buffer to verify that the data has been received correctly. If an error is detected, the LED above the faulty channel will be illuminated. The controller will do this continuously, one character at a time. If the error is intermittent, the LED will flicker on and off. If a hard error occurs, the LED will remain illuminated after the slide switch is returned to the OFF position.

This test may be run without affecting the operation of any other adaptor. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

2) External Wrap-Around Test: The line receivers and drivers are not tested by the internal loopback test. If such a fault is suspected, the external wrap-around test will detect it.

There are two kinds of external tests, both executed with the slide switch in the EXT position. When the microcode detects the presence of a wrap-around connector, it will run the second of the two tests on that particular line.

The first test causes the line adaptor to echo characters received from a terminal at 9600 baud back to that terminal. A fault within the terminal, the connecting cable or the Line Adaptor will cause the character to be echoed incorrectly or not at all.

Once the identity of the faulty line has been determined, the second external test can be executed to further isolate the fault. Unplug the line from the adaptor panel that is to be tested. The controller will then transmit a character out each line driver, and it will expect to see a character looped back through the respective line receiver. Because no loop back path has been provided, the fault LED will be illuminated. Plug the H315 wrap-around connector (see 4.9.6) that is provided with the CS01 into the channel. While the connector is in place, the LED above that channel should go out. If it does not, there is a problem with that channel.

If one of the channels has failed the external test yet passes the internal test, then the problem is either the line driver or receiver for that channel. This test may be run without affecting the operation of any other adaptor. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

4.9.3.2 <u>CAll/C Tests</u>

1) Internal Wrap-Around Test: The internal wrap-around test is run by simply placing the slide switch in the INT position for each panel that is to be tested. The controller will then select a loop-back data path, transmit a character, and then read the receive buffer to verify that the data has been received correctly. If an error is detected, the LED above the faulty channel will be illuminated. The controller will do this continuously, one character at a time. If the error is intermittent, the LED will flicker on

and off. If a hard error occurs, the LED will remain illuminated after the slide switch is returned to the OFF position.

This test may be run without affecting the operation of any other adaptor panel. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

2) External Wrap-Around Test: The line receivers and drivers are not tested by the internal loopback test. If such a fault is suspected, the external wrap-around test will detect it.

There are two kinds of external tests, both executed with the slide switch in the EXT position. When the microcode detects the presence of a loop-back data path, it will run the second of the two tests on that particular line.

The first test causes the line adaptor to echo characters received from a terminal at 9600 baud back to that terminal. A fault within the terminal, the connecting cable or the Line Adaptor will cause the character to be echoed incorrectly or not at all.

The second test uses a loop-back data path from the transmit to the receive terminals of a given channel to test that channels line drivers and receivers. However, to perform the test, either the line driver or receiver must be configured for passive operation while the other is configured for active operation. Reconfiguring a driver or receiver is somewhat involved. Consequently, it is recommended that the character echo test be performed a second time on a channel that is suspected of being faulty using a different terminal and line. If the channel still fails the character echo test with the new terminal and line, then the problem is probably in the Line Adaptor. If performance of the loop-back test is convenient, the procedure is outlined below.

Before running the external test, either the receiver or transmitter for each channel to be tested must be in the passive configuration. Follow the procedure in paragraph 4.5.2 to reconfigure one of the drivers. Also, the receiver filter must not be connected for external loop back testing.

After either the transmitters or receivers have been reconfigured for passive operation, the transmit and receive line for each channel must be connected together. Regardless of which half of the channel is active or passive, connect the two outermost terminals one another and the two innermost terminals to one another. Do this for each channel to be tested. Place the slide switch in the EXT position. The controller will then continually transmit

characters out the line drivers, and it will expect to see the characters looped back through the line receivers. All of the LEDs should remain unlit. If one does not, there is a problem with that channel.

After the test has been completed, return the channels to their original configurations. Place the slide switch in the INT position to reset the LEDs. If one of the channels has failed the external test yet passes the internal test, then the problem is either the line driver or receiver for that channel.

This test may be run without affecting the operation of any other adaptor. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

4.9.4 Mini-Test

If diagnostics are not available or it is decided not to run them, it is possible to prove out the NPR function which is not checked by the self-test, by running the following simple procedure from the CPU console:

- Deposit 000400 into memory location 0; deposit 000377 into location 2.
- 2) Deposit 004000 into SCR location to clear controller.
- Deposit 001000 into SCR location to set Maintenance Mode to achieve wrap-around. Could use different line number here.
- 4) Deposit 033503 into SCR + 4 location (LPR).
- 5) Deposit 000000 into SCR + 6 location (CAR).
- 6) Deposit 177775 into SCR + 10 location (BCR).
- 7) Deposit 000001 into SCR + 12 location (BAR) to enable line 0 transmitter.
- 8) Examine location SCR + 2 (RCR) four times and check the following:

100000 100001 100377 000377

9) Examine SCR and the following seven locations and check for the following:

101000 000377 033503 000003 000000 000000 000000 000000

The above procedure performs a transmission of three characters in wrap-around mode on line 0. Another line could be used. The silo is read out by examining RCR to see that the characters were transmitted and received properly.

4.9.5 <u>Diagnostics</u>

The ZDHM diagnostic should be run to insure that the controller and all the lines are operational. This program is a very comprehensive diagnostic and includes most of the functions of the other diagnostics. Instructions for running this program can be found in Appendix B. Patches for running this program with the Expanded Silo option can be found in Appendix C.

4.9.6 Test Connector

The diagnostics and the online "Line Test" activated by the Line Adapter Board slide switch require an H315 type wrap-around connector. One connector is supplied with each panel and a full set of 16 can be ordered from Emulex. The standard DEC H315 must have a jumper added from pin 4 to pin 6 if Data Set Ready is being used rather than Ring. The H315 connector has the following connections:

2 - 3	Tx Data - Rx Data
11 - 12	Sec. Tx Data - Sec. Rx Data
20 - 5 - 8	DTR - CTS - Carrier
4 - 22 - 6	RTS - Ring - DSR

BLANK

Appendix A

CONTROLLER OPTION SWITCHES

A.1 CC01 CONTROLLER PCBA

TABLE A-1 DISTRIBUTION PANEL

Option Sw	Open	Closed	Function
SW1-1 SW1-2 SW1-3 SW1-4	Run	Halt-Reset	Controller Run/Halt-Reset Number of CPll Panels2 Number of CPll Panels2 DHll/DMll Starting Address4
SW1-5	Disable	Enable	Interleave DH and DM vector locations
SW1-6	Halt	Override	Override power-up line test failures (if this switch is open, the controller will hang with the FAULT LED ON if any line fails) 3
SW1-7 SW1-8	Disable 18 BIT	Enable 22 BIT	Force two Stop Bits on all lines ADDRESSING MODE

All unused switches MUST BE OFF.

See Table 4-1.

See paragraph 4.9.1.

See Table 4-2.

TABLE A-2 INTERRUPT VECTOR SELECTION

Switch	Open	Closed	Function
SW2-1 SW2-2 SW2-3 SW2-4 SW2-5 SW2-6 SW2-7 SW2-8	2K Disable	lK Enable	DH11 Vector Address ² PROM Address Range ³ Expanded Silo Not used ¹

²All unused switches MUST BE OFF. 2See Table 4-3 for settings. Must be open (OFF).

TABLE A-3
DISTRIBUTION PANELS

Switch	Open	Closed	Function
SW3-1 SW3-2 SW3-3 SW3-4 SW3-5 SW3-6 SW3-7 SW3-8			DM11 Vector Addresses2 Not used1 Not used1

All unused switches MUST BE OFF. See Table 4-4 for settings.

TABLE A-4
CONTROLLER STARTING ADDRESS

Switches	Open	Closed	Function
SW4-1 SW4-2 SW4-3 SW4-4 SW4-5 SW4-6 SW4-7 SW4-8			DH11/DM11 Starting Address2 Not used1 Not used1 Not used1

All unused switches MUST BE OFF. See Table 4-2 for settings.

A.2 CAll/H LINE ADAPTER

TABLE A-5 LINE TEST SWITCH

Switches	Open	Closed	Function
SWl			Online Self-Test2
See paragi	ranh 1 9 3		

TABLE A-6 OPTION SWITCHES

Switches	Open	Closed	Function
SW2-1 SW2-2 SW2-3 SW2-4	Enabled	Disabled	Not used ¹ CTS/CD Flow Control Not used ¹ Not used ¹
T			

All unused switches MUST BE OFF.

BLANK

Appendix B

ZDHM DIAGNOSTIC

B.1 GENERAL DESCRIPTION

ZDHM is a comprehensive diagnostic test program designed to aid in the acceptance testing, installation checkout, and corrective maintenance of the DH11 16 line asynchronous serial line multiplexer. It consists of 48 logically sequenced diagnostic tests designed to test and verify that the DH11 is operating in accordance with its design specifications.

The program is configurable by the autosizer or by console dialogue to enable it to automatically test and verify all 16 lines on up to 16 contiguous DHlls (with non-contiguous/contiguous vector assignments). Individual units and individual lines within a unit may be selected or deselected to facilitate fault isolation to a particular DHll or a functional area of logic affecting a particular line within a unit. Whenever an error is detected, a comprehensive error report is typed that allows the user to isolate the fault to a functional area of logic. Extensive documentation is provided to permit the user to proceed from the error report to additional logic checks in order to isolate the problem to a replaceable unit.

In order to facilitate installation checkout, tests 101 and 105 through 107 (test group 1) of the modem control diagnostic, ZDHK, have been included in this program. In this way, all the level converters and cables can be checked with just one program using the H315 turnaround connector.

NOTE 1: The H315 turnaround connector must be installed on any line under test when running ZDHM. As described in Section B.3.1, lines may be selected and tested on an individual basis.

NOTE 2: The ZDHM diagnostic will not consistantly run error free if a distribution panel contains only one of the eight-line adaptor panels. The procedure for testing a distribution panel with this configuration is to temporarily place another eight-line adaptor in the panel. This problem is caused by the diagnostic's assumption that each DEC DHll is equiped with 16 lines. The diagnostic expects certain modem status information from every line even though all of the lines might not be selected for testing.

B.2 <u>DIAGNOSTIC PATCHES</u>

The following patches must be installed before running the ZDHM diagnostic on the CS01/H2.

Patch				
Number	Location	From	То	Description
1	011700 011702	012737 011730	000137 012204	Skip subtest 40
2	012206 012210	012737 012236	000137 012512	Skip subtest 41
3	015306 015310	012737 015362	000137 015754	Skip subtest 50
4	017266 017270	012737 017302	000137 017526	Skip subtest 54
5	020102 020104 020174	005077 010202 105227	004737 037720 005227	Patch subtest 56: Add modem signal delay
6	020272 020274 020364	005077 010012 105227	004737 037720 005227	Patch subtest 57: Add modem signal delay
7	020462 020464 020554	005077 007622 105227	004737 037720 005227	Patch subtest 60: Add modem signal delay
8	020410 020412	005077 007676	000137 020576	Skip subtest 60
9	025322 026424	170670 160420	171370 161370	Extend autosize address range
10	037720 037722 037724 037726 037730 037732 037734 037736 037740	vacant vacant vacant vacant vacant vacant vacant vacant vacant	010546 013705 030310 005015 005005 005205 001376 012605 000207	Software delay for patches 5 and 6

Patches 1 through 4 cause subtests 40, 41, 50, and 54 to be bypassed. These patches are required when running with the CP32 or CP34 distribution panels. These patches are not required when

running with CPll or CPl2 distribution panels. The CP32 and CP34 distribution panels use DUARTs which are not compatible in all cases with the operation of the ZDHM diagnostic.

Patches 5 through 7 insert software delays before Line Status Register reads in subtests 56, 57, and 60. These patches are required because the CS01/H2 updates the modem signal status every 5 milliseconds instead of every few microseconds as in the DM11.

Patch 8 causes subtest 60 to be bypassed. Subtest 60 attempts to test the Secondary Transmit and Secondary Receive signals on pins 11 and 12 of the 25-pin EIA connector. These signals are not supported on the CP32 or CP34 distribution panel.

Patch 9 extends the address range the diagnoostic uses to autosize. The range is increased for the DH11 from <760020:760420> to <760020:761370> and for the DM11 from <770500:770670> to <770500:771370>. This patch is not necessary for the standard address PROMs provided with the CS01/H2 (see section 4.3.2.1 for Address PROM identification).

Patch 10 is the software delay loop for patches 5, 6, and 7.

B.3 LOADING PROCEDURES

There are several different methods for loading the DH11 diagnostics under the control of the XXDP diagnostic monitor. The following procedure is common to many DEC systems and similar to others.

- 1) Mount the appropriate medium (Dectape, disk, etc.) containing the XXDP monitor and ZDHM.
- 2) Boot the system to load the monitor.
- Once loaded the XXDP monitor prints an introductory message and displays a period (.) to indicate that it is ready to accept commands.
- 4) Type "L ZDHMDO." This will cause the diagnostic to be loaded, but it will not be started.

B.4 STARTING PROCEDURES

The console switch register is used to select between DHll diagnostic program options. The program can also be started at different locations to allow it to be rerun without having to reenter the DHll parameters.

B.4.1 Program Options

The CPU switch register (SR) is used to allow the user to select between several program options. The 16 bits of the register

represent different options during program start than they do during testing (SR = switch register).

_15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CD.	CD	CD	C D	CD	CD.	CD	CD	CD	CD	CD	CD	C D	C.D.	CD	SR
L SK	SK.	DK.	AG	3K	DK	3K	3K	DK	SK	SK	SK.	SK.	SR	SR	SK
								2.5	,			· · · · · · · · · · · · · · · · · · ·			
				L			<u> </u>			L			1		

Switch Reg.	Start	Testing
Bit 15 = 1	No function.	Halt on error (after typing message).
Bit 14 = 1	No function.	Loop continuously on current test.
Bit 13 = 1	No function.	Inhibit error typouts.
Bit 11 = 1	No function.	Inhibit sub-test iterations (quick pass).
Bit 10 = 1	No function.	Inhibit modem control on abbreviated test.
Bit 09 = 1	No function.	Lock on hard errors.
Bit 08 = 1	Halts after configuration to permit dumping pre- configured copies of the program.	Search for and lock on test selected by the contents of SR <07:00>.
<07:00>	See below for <01:00>	Contains test number to search for when SR 08 = 1.
Bit 01 = 1	Types device map generated by the auto-sizer.	
Bit 00 = 1	Allows the user to input DH parameters manually. (inhibits the autosizer).	

B.4.2 Normal Program Start At 200

After loading diagnostic, start execution at 200^8 . Set SR bit 0 OFF if autosizer is to be used and set it ON if the operator is to enter the parameters. The operator should respond as indicated to the following questons asked by the program:

- o Number of addresses between vectors Enter 10⁸ for standard DH11's with contiguous vectors; enter 20⁸ if the DM11 vectors are interleaved with the DH11 vectors. The default value is 20⁸.
- o Device address Enter the octal address of the first DHll in the system.
- o Vector address Enter the octal receiver vector address for the first DHll in system.
- o DH11 device selection Type in a six digit octal number encoded as follows (setting bit 15 to one causes device 15 to be tested, setting bit 13 to one causes device 13 to be tested, setting bit 10 to zero causes device 10 to be ignored, etc.):

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
				,			l		DH	1			1		

A value of 177777^8 will test all DH11's. The default is 177777^8 . (DH = Device)

o Line selection - Type in a six digit octal number encoded as follows (setting bit 15 to one causes line 15 of all selected devices to be tested, setting bit 13 to one causes line 13 of all selected devices to be tested, setting bit 10 to zero causes line 10 to be ignored, etc.):

_15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN
							<u> </u>						<u> </u>		

A value of 177777^8 will test all lines. The default is 177777^8 . (LN = Line)

B.4.3 Default Parameter Start At 204

When starting at 204⁸, the program will default to the parameters used in the previous execution. It should not be used for the first execution. The SR should be set for testing at the time the program is started.

B.4.4 Line and Device Parameter Change Start At 210

When the program is started at 210^8 , it will ask the last two (parameter setting) questions of the input dialogue described above. Set the SR for testing.

B.4.5 <u>Switchless CPU</u>

If the diagnostic is run on a CPU without a Switch Register, then a software switch register (location 176) is used which allows the user the same switch options.

When SR values are needed the program types out the current value of the SR and asks for new values by typing NEW=. A control G will allow the user to change the contents of the software switch register.

Note: After typing control G, it may be necessary to wait up to 30 sec for the diagnostic to respond. This is because the diagnostic allows SR changes only after completion of each of the 48 subtests.

B.5 TEST SUMMARY

```
Check SSYN response from all DHll registers.
 1
     Test that Master Clr can clear the SCR, LPR, BKR, SSR regs
 2
     Test SCR register R/W bits can set CLR (normal mode)
 3
     Test SCR register read-only bits (normal mode)
 4
     Test SCR register bits that can be Set/Clr in maint. mode
 5
     Test that all R/W bits in LPR can be set/clr
 6
     Test that all R/W bits in BKR can be set/clr
7
     Test that all R/W bits in SSR can be set/clr
10
     Test that Clr/Set bit N in LPR doesn't clear any other bits
11
     Test that Clr/Set bit N in BKR doesn't clear any other bits
12
     Test that Clr/Set bit N in SSR doesn't clear any other bits
13
     CAR memory addressing test
14
     BCR memory addressing test
15
     CAR register test - all l's / all 0's - all lines
16
     BCR register test - all l's / all 0's - all lines
17
     CAR memory patterns test / 0's disturb
20
     BCR memory patterns test / 0's disturb
21
     CAR memory patterns test / l's disturb
22
     BCR memory patterns test / l's disturb
23
     Test that CAR memory ext bits Set/Clr properly
24
     Test intr. enable bits - intr. condition disabled
25
     Test char. available i.e., with intr. condition active
26
     Test silo overflow i.e., with intr. condition active
27
     Test NXM i.e., with intr. condition active
30
     Test XMITTR done i.e., with intr. condition active
31
     Transmitter NPR logic test 1
32
33
     Transmitter NPR logic test 2
     Test that character available can cause RCVR interrupt
34
     Test that the silo status register counts up correctly
35
     Test that silo status register down counts correctly
36
     Test silo alarm level for counts 0,1,2,4,8,16, and 32
37
     Transmitter timing test - all selected lines - all speeds
40
     Receiver timing test - all selected lines - all speeds
41
     Verify storage overflow-non maint mode-all selected lines
42
     Basic data test - all selected lines/all character lengths
43
     Single line data test - all selected lines
44
     Basic parity logic test - all selected lines - odd parity
45
     Multi-line parity data test - all selected lines
46
     Auto-echo test 1 - all selected lines
47
     Auto-echo test 2 - all selected lines
50
     Auto-echo test 3 - all selected lines
51
     Break bit test - all selected lines
52
     Half-duplex test - all selected lines
53
     Verify that overrun can set properly - all selected lines
54
     Abbreviated modem control diagnostic (ZDHK T101)
55
     Modem control diagnostic continued (ZDHK T105)
56
     Modem control diagnostic continued (ZDHK T106)
57
     Modem control diagnostic continued (ZDHK T107)
60
```

B.6 ERROR HEADER MNEMONIC DEFINITIONS

All numbers printed as error data are in octal

(PC) Address of the error call (error PC)

(PS) Contents of the PSW at the time of the error

(SP) Contents of the stack pointer at the time of the error

TEST Test number

DEVADR Device address - 1st address in the selected DH11

REGADR Address of the DHll register being tested

WAS What the actual data read was (DH11 register or memory location)

S/B What the data read should have been

SPEED Speed code in the LPR register at the time of error

TIMEB Contents of software counter used in timing tests

TIMEC contents of software counter used in timing tests.

CHRLNG Character length code in the LPR at the time of the error 00=5 bits, 01=6 bits, 02=7 bits, 03=8 bits

TRPPC Contents of the PC (R7) at the time of a bus error or RSVD instruction trap

TRPPS Contents of the PSW at the time of a bus error or RSVD instruction trap

(LPRG) Contents of the LPR register at the time of the error

LINACT Flags used by multi-line tests to indicate active lines

WASADR Memory address of the WAS data (actual data read)

SBADR Memory address of the S/B data (good data)

SCRWAS Contents of the SCR register

SCRS/B What the contents of the SCR register should have been

LINCHK Line no. being checked during CAR and BCR memory tests

LINEWR Line no. being written into during CAR and BCR tests

PATTRN Test pattern being written into CAR or BCR memories

Appendix C

EXPANDED SILO OPTION

C.1 GENERAL DESCRIPTION

As described in Section 2.4.1.3, each DHll contains a 16-bit wide by 64 word deep silo. The amount of storage in this silo may be doubled to 128 words by closing the Expanded Silo option switch SW2-7 (see Appendix A). Using this option has the advantage of doubling the latency time available before a receiver interrupt must be serviced.

The ZDHM diagnostic test program may be run with the Expanded Silo option selected if the program is patched as described below. All subtests which use the Silo Maintenance function to fill the silo are skipped, since there is no Silo Maintenance function for the expanded silo. Other tests are modified as appropriate to handle the increased depth of the silo.

C.2 ZDHM DIAGNOSTIC PATCHES

Location	From	TO	Comment
10734	12737	4	Skip Tests 34, 35, 36, 37
10736	10756	4	
10740	1110	4	
10742	13703	137	
10744	27304	11676	
12550	177677	177577	Patch Test 42
12754	77	177	
17322	177674	177574	Patch Test 54
17434	101	201	
17450	101	201	
27672	100077	77	Modify SSR Mask for Read/Write Bits

BLANK

Appendix D

ZDHK PATCHES

The Modem Control Multiplexer Diagnostic requires a minor patch to allow it to run without error. The patch is shown below:

Is	Should	Ве
5077 12332	137 3266	
	 5077	5077 137

Shipping Kit List -- C801/H2 Part Number: SKLC801H2 Edit Date: 19-Nov-84

Revision : E

	Part	
aty.	Number	Description
********	and and the did one pas	good give nive does vive dole gong good nivel bank
1	C30151001	CSO1/H2 Technical manual
1	BEOODIA	Publication Addendum
1	ADOOOGB	Publication Addendum



	NO.	DATE:	
İ	AD0006B	09 Oct 84	
-	PAGE:	OF	
	1	25	

PUBLICATION NUMBER	PUBLICATION TITLE	REV	EFFECTIVE DATE
CS1151004	CS11/H2 Technical	All	13 Aug 1984
CS1151005	CS11/U2 Technical Manual	All	13 Aug 1984
CS0151001	CS01/H2 Technical Manual	All	09 Oct 84

REASON

CP12 DISTRIBUTION PANEL ADDENDUM

WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Comminsion (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

ORIGINATOR
M. Johnson

SE0804 107801

ENGINEERING SERVICE

ENGINEERAN

PUBLICATIONS



C5 (950F) (10783)

PUBLICATION ADDENDUM

NO. AD0006 DATE: 1984
PAGE: 2 OF 25

TABLE OF CONTENTS

Section	Title	Page
1.1 1.1.1 1.1.2	OVERVIEW	4 4 4
2.1	THE POWER SUPPLY	5
3.1	ACCESSING THE INTERFACE BOARD	5
4.1 4.1.1 4.1.1.1 4.1.1.2 4.1.1.3	INTERFACE BOARD SETUP OPTION SWITCH FUNCTIONS CTS Flow Control Force DTR/RTS Active Sampling Rate (External Clock) For CA12/V Line Adapter	6 8 8 9
5.1 5.1.1 5.1.1.2 5.1.1.2 5.1.2.5 5.1.2.1 5.1.2.2 5.1.2.3 5.1.3 5.1.3.1 5.1.3.2 5.1.3.3		9 11 11 11 12 16 16 16 18 18 18
6.1	MAINTAINING FCC CLASS A COMPLIANCE	20
7.1 7.1.1 7.1.2 7.1.3 7.1.3.1 7.1.3.2	CP12 DISTRIBUTION PANEL INSTALLATION	20 21 21 21 22 22



NO. DATE:
AD0006 06 Apr 1984
PAGE: 3 OF 25

LIST OF TABLES

HIST OF TABLES				
Table No.	Title	Page		
Table 1-1 Table 1-2 Table 4-1	CP12 Distribution Panel Part Numbers	4 5 7		
Table 5-1 Table 5-2 Table 5-3 Table 7-1	20 mA Current Loop Cable Lengths	12 16 18 23		
LIST OF FIGURES				
Figure No.	Title	Page		
Figure 4-1 Figure 5-1 Figure 5-2	Interface Board Switch Locations	6 10 10		
Figure 5-3	CA12/V Line Adapter Panel Switch and Jumper	11		
Figure 5-4 Figure 5-5	CA12/C Current Loop Interface Schematic	13 14		
Figure 5-6	CAl2/C Transmit and Receive Passive Current Source Configuration	15		
Figure 5-7 Figure 5-8 Figure 7-1	CAl2/H Line Adapter Panel Channel Schematic CAl2/V Line Adapter Panel Channel Schematic Shielded Cable Installation	17 19 25		



NO.		DATE	:	ŧ .	
	AD0006	06	Apr	1984	
PAGE:	4	OF	25		

1.0 OVERVIEW

This is an addendum to the technical manual you received with your Emulex CSl1/H2 or CSl1/U2 Communications Subsystem. This addendum contains installation and application data for the Emulex CPl2 Distribution Panel. The CPl2 Distribution Panel replaces the CPl1 Distribution Panel described in the technical manual.

This addendum is divided into sections. The table below lists those sections.

1.0 2.0 3.0 4.0 5.0	OVERVIEW THE POWER SUPPLY ACCESSING THE INTERFACE BOARD INTERFACE BOARD SETUP LINE ADAPTER PANELS
6.0 7.0	MAINTAINING FCC CLASS A COMPLIANCE CP12 DISTRIBUTION PANEL INSTALLATION

1.1 CP12 EMULEX PART NUMBERS

There are six different types of CP12 Distribution Panels available. Each type is briefly described in Table 1-1.

Table 1-1. CP12 Distribution Panel Part Numbers

Part Number	Number of Channels	Adapter Panel Type (Model)	Interface
CP1220001	8	Asynchronous (CA12/H) Asynchronous (CA12/H) Synchronous/Async. (CA12/V) Synchronous/Async. (CA12/V) Current Loop (CA12/C) Current Loop (CA12/C)	RS-232-C
CP1220002	16		RS-232-C
CP1220003	8		RS-232-C
CP1220004	16		RS-232-C
CP1220005	8		20 mA
CP1220006	16		20 mA

Async. = Asynchronous

1.2 CP12 DISTRIBUTION PANEL KIT

Table 1-2 lists the contents of the CP12 Distribution Panel Kit.

[F 059BU10783]



NO. DATE:				
	AD0006	06	Apr	1984
PAGE:	5	OF	25	

Table 1-2. CP12 Distribution Panel Kit Contents

	Contents	Comments
2 3	CP12 Distribution Panel 8 foot Cable Terminator Wrap-Around Connector	See Table 1-1 for part number From CC11 to CP12

2.0 THE POWER SUPPLY

The CP12 Distribution Panel power supply can be configured to operate with either a 115 Vac or 230 Vac voltage supply. The supply is wired for 115 Vac when shipped from the factory. To convert the power supply to 230 Vac, use the following procedure:

- 1. Make sure the power supply is not plugged in.
- Replace the existing lA slow/blow fuse with the enclosed 1/2A slow/blow fuse. The fuse plug is on the left hand side when viewed from the front.
- 3. Move the slide switch to the 230 v position. The switch is next to the fuse plug.
- 4. Remove the existing ac plug and replace it with the type desired for your application. The wire coloring is: green--safety ground, white--neutral, black--ac power.

3.0 ACCESSING THE INTERFACE BOARD

It is necessary to access the interface board of the CP12 Distribution Panel to set certain switches. The switch locations on the interface board are shown in Figure 4-1. Use the following procedure to access the interface board, which is located underneath the line adapters:

- 1. Turn OFF the ac power to the distribution panel by unplugging the ac line cord.
- Unscrew the knurled screw at each corner of line adapter panel. The captive screws will dangle loosely when free.
- 3. Grasp the handles in the upper left and right hand corners of one of adapter panel and pull the adapter from the AMP MOD 1 pins on the distribution panel. Repeat for the remaining adapter.



NO. D		DATE	:	•	
	AD0006	06	Apr	1984	
PAGE:	6	OF	25		

4.0 INTERFACE BOARD SETUP

The interface board has five dual-inline package (DIP) switches that are used to select different options. The five DIP switches are labeled SW1(L), SW1(R), SW1(L), SW1(R), and SW3. Switch SWX(L) configures the left-hand Line Adapter Panel; SWX(R) configures the right-hand Line Adapter Panel. See Figure 4-1 for switch locations. Table 4-1 defines the switch settings and factory settings.

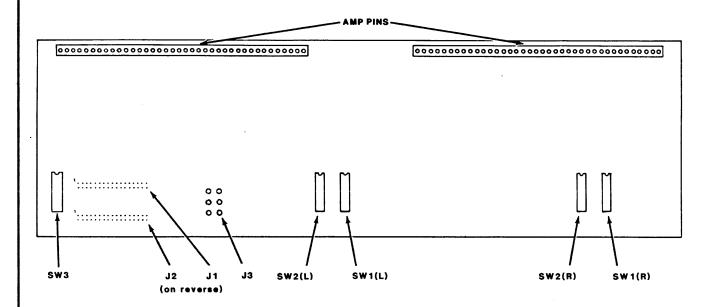


Figure 4-1. Interface Board Switch Locations

F059B(10783)



NO.		DATE	:	
	AD0006	06	Apr	1984
PAGE:	7	OF	25	

Table 4-1. CP12 Interface Board Switch Definitions/Factory Configuration

CUITMOU	000 (0)	017/11			
SWITCH	OFF(0)	ON(1)	Fact	Function	Section
	Disable			Channel 0 CTS Flow Control	4.1.1
	Disable	Enable	OFF(0)	Channel 1 CTS Flow Control	4.1.1
	Disable	Enable	OFF(0)	Channel 2 CTS Flow Control	4.1.1
	Disable	Enable	OFF(0)	Channel 3 CTS Flow Control	4.1.1
SW1-5(L)	Disable	Enable		Channel 4 CTS Flow Control	
	Disable	Enable		Channel 5 CTS Flow Control	
	Disable			Channel 6 Cmg Blow Control	4.1.1
	Disable			Channel 6 CTS Flow Control	4.1.1
		DIIGDIE	Off (U)	Channel 7 CTS Flow Control	4.1.1
SW2-1(L)	Disable	Enable	OFF(0)	Force DTR/RTS Active	4.1.2
SW2-2(L)	lX	16X	OFF(0)	Sampling Rate for CA12/V	4.1.3
SW2-3(L)	_	-		Not Used	4.1.3
SW2-4(L)	_	-	OFF(0)*	Not Used	j
SW2-5(L)	-		OFF(0)*	Not Used	ł
SW2-6(L)	_		OFF(0)*	Not Used	
SW2-7(L)	_	_	OFF (0) *	Not Used	
SW2-8(L)	_	_	OFF(0)*	Not Used	1
			OFF (O)	Not used	ŀ
SW1-1(R)		Enable	OFF(0)	Channel 8 CTS Flow Control	4 7 7
SW1-2(R)	Disable	Enable	OFF(0)	Channel 9 CTS Flow Control	4.1.1
SW1-3(R)	Disable	Enable	OFF(0)	Channel 10 Cmg Blow Control	4.1.1
SW1-4(R)		Enable	OFF(0)	Channel 10 CTS Flow Control	4.1.1
SW1-5(R)		Enable	off(0)	Channel 11 CTS Flow Control	4.1.1
SW1-6(R)				Channel 12 CTS Flow Control	4.1.1
SW1-7(R)	Disable	Enable	OFF(0)	Channel 13 CTS Flow Control	4.1.1
		Enable	OFF(0)	Channel 14 CTS Flow Control	4.1.1
SW1-8(R)	Disable	Enable	OFF(0)	Channel 15 CTS Flow Control	4.1.1
SW2-1(R)	Disable	Enable	OFF(0)	Force DTR/RTS Active	4 7 2
SW2-2(R)	lx	16X	OFF (0)	Sampling Rate for CA12/V	4.1.2
SW2-3(R)	_	_		Not Used	4.1.3
SW2-4(R)	-	_	OFF(0)*	Not Used	
SW2-5(R)	_	_	OFF(0)*	Not Used	Į
SW2-6(R)	_	-	OFF (0) *	Not Used	
SW2-7(R)		_	OFF (0) *	Not Used	
SW2-8(R)	_	_	OFF (0) *	Not used	
DNZ O(R)		_	OFF (0) *	Not Used	
SW3-1	_	-	OFF(0)*	Not Used	-
SW3-2	•••	-		Not Used - Must be ON	
SW3-3	-	_	OFF(0)*	Not Used	1
SW3-4	-	-		Not Used	
SW3-5	_	_		Not Used - Must be ON	
SW3-6	_	_	OFF(0)*	Not Used - Must be ON	
				not obcu	
OFF(0)	= Open				
ON(1)	= Closed]
*	= Switch	n must be	e in fact	ory setting	
Fact	= Switch must be in factory setting t = Factory switch setting				
CTS	= Clear	to Send	- 5		
DTR	= Data 1		Readv		İ
RTS	= Reques				1
					



-	NO.		DATE	:	3
		AD0006	06	Apr	1984
	PAGE:	8	OF	25	

4.1 OPTION SWITCH FUNCTIONS

4.1.1 CTS Flow Control

The Clear to Send (CTS) flow control option allows devices to use CTS for their receive data flow control instead of the XON/XOFF flow control typically used by DEC equipment. When this option is selected, dropping CTS at a channel causes the CS11 to halt transmission on a character boundary. Because this action is transparent to the host software, it is not necessary to specify modem control for the lines involved. The state of the CTS line is reflected in the Line Status Register whether or not this option is selected.

This option is enabled for individual channels on a line adapter using switch SWl-X(L) and switch SWl-X(R) on the interface board. SWl-X(L) affects the left-hand adapter on the distribution panel and SWl-1(R) affects the right-hand adapter.

Switch	OFF	ON	Factory
SW1-X(X)	Disable	Enable	OFF

4.1.2 Force DTR/RTS Active

This option causes the Data Terminal Ready (DTR) and Request to Send (RTS) modem control signals for the eight RS-232-C connectors on the adapter to be forced active when the host computer writes to the Line Parameter Register associated with a particular channel. The signals remain active until the controller is reset or until the host computer writes into the Line Status Register to change these signals.

This option is enabled for all channels on a line adapter using switch SW2-1(L) and switch SW2-1(R) on the interface board. SW2-1(L) affects the left-hand adapter on the distribution panel and SW2-1(R) affects the right-hand adapter. See the Registers and Programming section of the technical manual for a description of programming controller register functions.

Switch	OFF	ON	Factory
SW2-1(X)	Disable	Enable	OFF

EF059B(10/83)



NO.	DATE:				
	AD0006	06	Apr	1984	
PAGE:	9	OF	25		

4.1.3 Sampling Rate (External Clock) For CA12/V Line Adapter

On the CAl2/V Line Adapter, there are external clock inputs for transmit and receive clocks. These are used by the USARTs on the CAl2/V for sampling the incoming data, and for clocking the outgoing data. The data may be sampled once per bit period (lx), or 16 times per bit period (l6X). The position of this switch determines how the external clocks will be used by the USARTs.

The sampling rate for all channels on a line adapter is selected using switch SW2-2(L) and switch SW2-2(R) on the interface board. SW2-2(L) affects the left-hand adaptor on the distribution panel and SW2-2(R) affects the right-hand adaptor.

NOTE

Bits <06:13> in the Line Parameter Register must be set to ones. Bits <06:09> set the reception sampling rate and bits <10:13> set the transmission sampling rate.

Switch	OFF	ON	Factory
SW2-2(X)	lx	16X	OFF

NOTE

This option applies only to the CAl2/V Line Adapter. The CAl2/H and CAl2/C Line Adapters are unaffected by the position of this switch.

5.0 LINE ADAPTER PANELS

Each CPl2 Distribution Panel contains one or two Line Adapter Panels. Each Line Adapter Panel has eight channel interfaces. If the CPl2 Distribution Panel has only one Line Adapter Panel, the right side of the chassis contains a blank panel.

One of three types of adapter panels may be used with the CS11/H2 and CS11/U2 emulations. The three types are the CA12/C, the CA12/H and the CA12/V. Figures 5-1, 5-2 and 5-3 depict the switch and jumper locations for the CA12/C, the CA12/H and the CA12/V, respectively. The necessary setup procedures for the three types of Line Adapter Panels are described in the following subsections.



NO. DATE:
AD0006 06 Apr 1984

PAGE: 10 OF 25

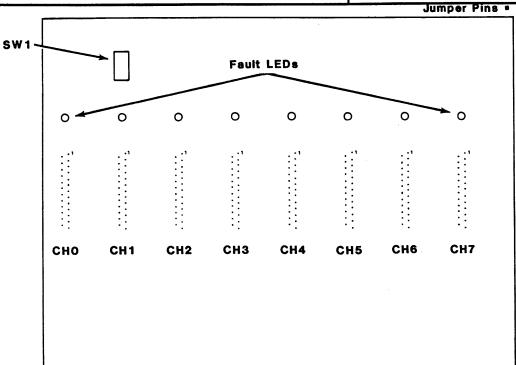


Figure 5-1. CA12/C Line Adapter Panel Switch Locations
Jumper Pins •

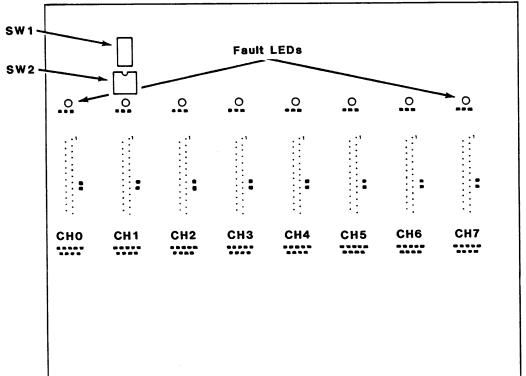


Figure 5-2. CAl2/H Line Adapter Panel Switch and Jumper Locations

[F 059Ft 10783]



NO.		DATE	:	
	AD0006	06	Apr	1984
PAGE:	11	OF	25	

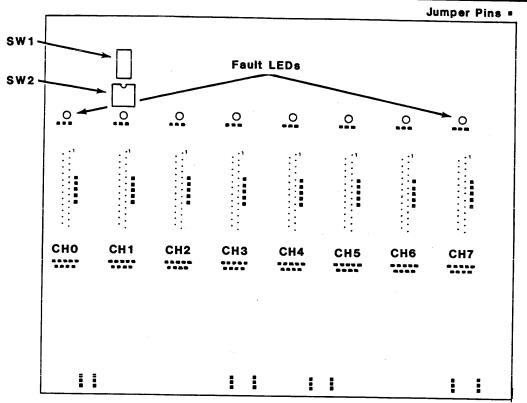


Figure 5-3. CAl2/V Line Adapter Panel Switch and Jumper Locations

5.1 CA12/C LINE ADAPTER PANEL SETUP

5.1.1 Line Test Switch

The Line Test Switch, SWI, should be OFF for normal operation. For a description of this switch's use, see paragraph 4.9.3 in the CS11/H2 Technical Manual, and paragraph 4.9.2 in the CS11/U2 Technical Manual.

5.1.2 Cabling

<u>5.1.2.1</u> Configuration for Active or Passive Current loop printers and terminals must use current loop wiring. Figure 5-4 provides a simplified schematic of the CAl2/C current loop interface.

Both the transmission and reception on the CAl2/C channels may be configured independently for active or passive current sources. If the CP12 channel is configured as the current source (active) in the loop, the terminal device must be configured for passive operation. If the terminal device is configured to provide the current source, the CP12 channel must be configured for passive operation. Figure 5-5 shows the CP12 transmitter and receiver configured for active current source operation. Figure 5-6 shows the CP12 transmitter and receiver configured for passive current source operation.



NO.		DATE	:	,
	AD0006	06	Apr	1984
PAGE:	12	OF	25	

5.1.2.2 Current Loop Cable Lengths No definitive 20 mA current loop specification exists. The length of cable that may be used is a function of electrical noise, loop resistance, cable type and speed of operation. Table 5-1 is given as a practical guide to the cable lengths that can be used with the CPl2 Distribution Panel; however, there is no guarantee of error free operation under all circumstances.

Table 5-1. 20 mA Current Loop Cable Lengths

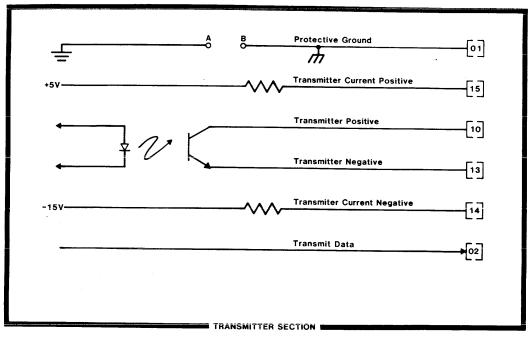
Baud	Shielded Un (in feet)	nshielded (in feet)
9600	500	1000
4800	1000	1800
2400	2000	3000
1200	4000	5000

Shielded cable is Belden 8777, 22 AWG, twisted pairs (shield floating). Unshielded cable is 22 AWG, 4 conductor inside station wire.

[F059B(10783)



NO.	DATE:				
L	AD0006	06	Apr	1984	
PAGE:	13	OF	25		



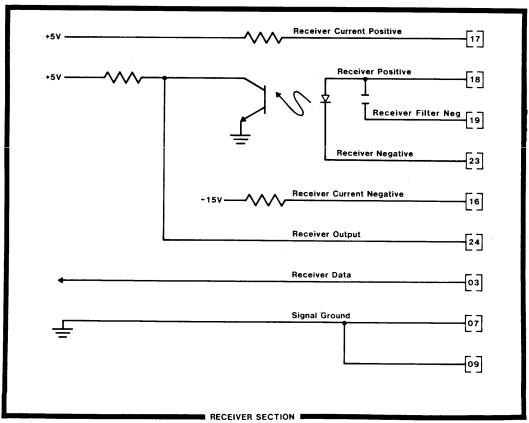
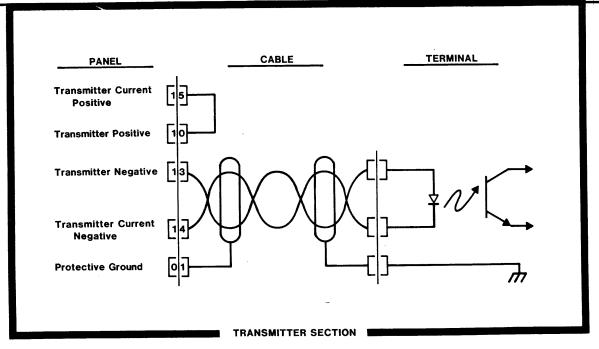


Figure 5-4. CAl2/C Current Loop Interface Schematic





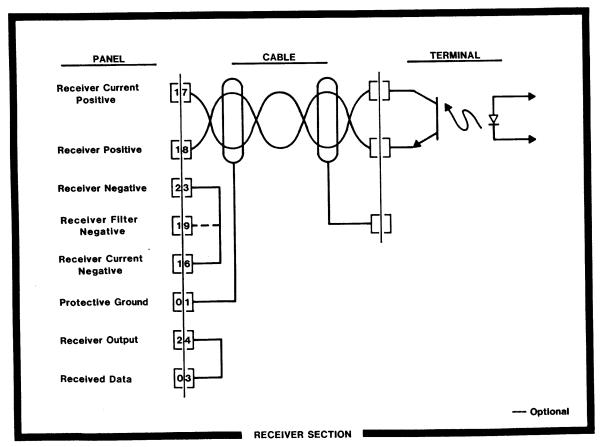
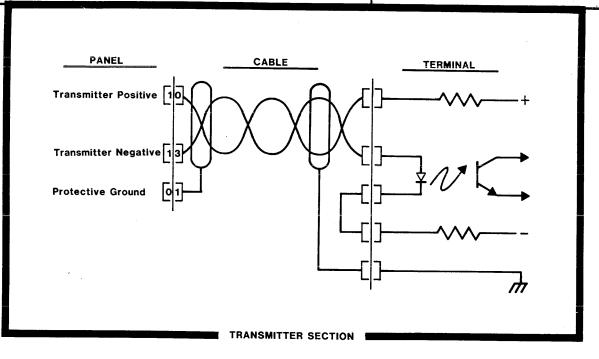


Figure 5-5. CAl2/C Transmit and Receive Active Current Source Configuration

FF059B(10/83)



NO. DATE:
AD0006 06 Apr 1984
PAGE: 15 OF 25



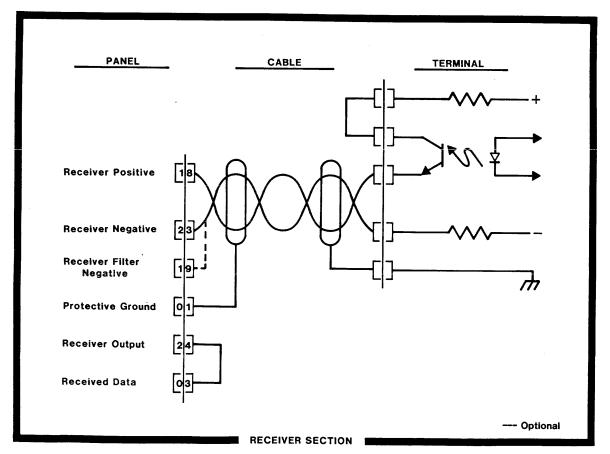


Figure 5-6. CA12/C Transmit and Receive Passive Current Source Configuration



_	NO.		DATE	•	
		AD0006	06	Apr	1984
	PAGE:	16	OF	25	

5.2 CA12/H LINE ADAPTER PANEL SETUP

5.2.1 Adapter Type Code Switches

Switch SW2 MUST be set to the factory setting shown in Table 5-2.

Table 5-2. CAl2/H Type Code Switch Settings

Adapter Type	1	SV 2	72 3	4
CA12/H	0	1	0	1

0 = off/open

1 = on/closed

5.2.2 Modem Control Pin Assignment Options

Pin assignment options are effected using the group of jumpers associated with each physical connector on the adapter. The jumpers are located underneath the dress panel of each adapter which must be removed to change jumper options. The jumpers are clearly marked on the printed circuit board. A simplified schematic of a typical channel's circuitry is shown in Figure 5-7. That schematic depicts the factory-installed jumpers and the other possible jumper connections on the CA12/H.

NOTE

If the CS11/H2 is to be used in a normal DH11/DM11 application, the jumper options should be left in the factory installed configuration. No special setup is necessary.

5.2.3 Line Test Switch

The Line Test Switch, SWl, should be OFF for normal operation. For a description of this switch's use, see paragraph 4.9.3 in the CSll/H2 Technical Manual, and paragraph 4.9.2 in the CSll/U2 Technical Manual.

EF059B(10783)



NO.	DATE:				
	AD0006	06	Apr	1984	
PAGE:	17	OF	25		

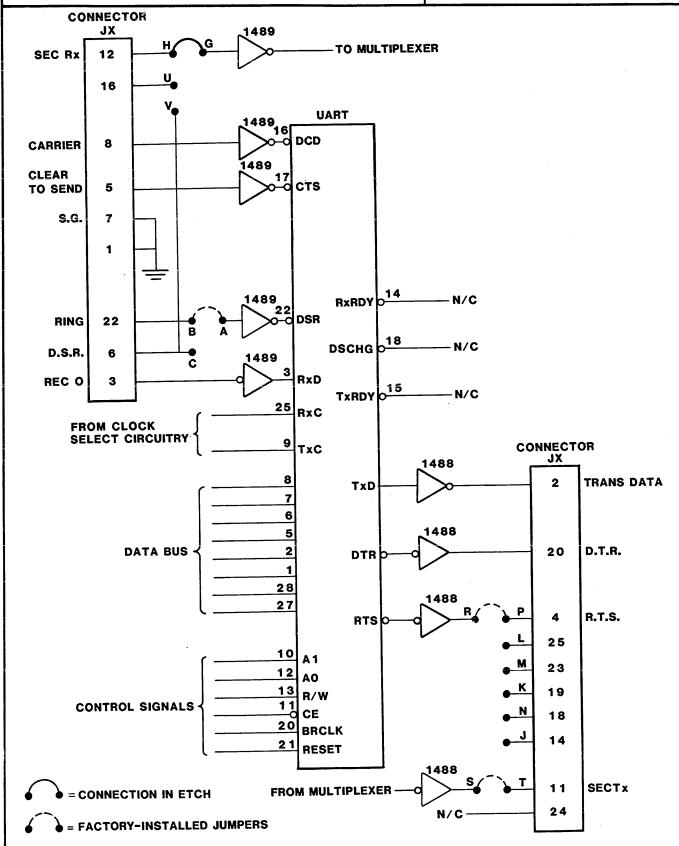


Figure 5-7. CAl2/H Line Adapter Panel Channel Schematic



NO.		DATE	DATE:		
	AD0006	06	Apr	1984	
PAGE:	18	OF	25		

5.3 CA12/V LINE ADAPTER PANEL SETUP

5.3.1 Adapter Type Code Switches

Switch SW2 MUST be set to the factory setting shown in Table 5-3.

Table 5-3. CAl2/V Type Code Switch Settings

Adapter Type	 1	SW 2	2	4
CAl 2/V	0	0	1	0

0 = off/open

1 = on/closed

5.3.2 Modem Control Pin Assignment Options

Pin assignment options are effected using the group of jumpers associated with each physical connector on the adapter. The jumpers are located underneath the dress panel of each adapter which must be removed to change jumper options. The jumpers are clearly marked on the printed circuit board. A simplified schematic of a typical channel's circuitry is shown in Figure 5-8. That schematic depicts the factory-installed jumpers and the other possible jumper connections on the CA12/V.

5.3.3 Line Test Switch

The Line Test Switch, SWl, should be OFF for normal operation. description of this switch's use, see paragraph 4.9.3 in the CS11/H2 Technical Manual, and paragraph 4.9.2 in the CS11/U2 Technical Manual.

E 0598 (10783)



NO.	DATE:				
<u> </u>	AD0006	06	Apr	1984	
PAGE:	19	OF	25		

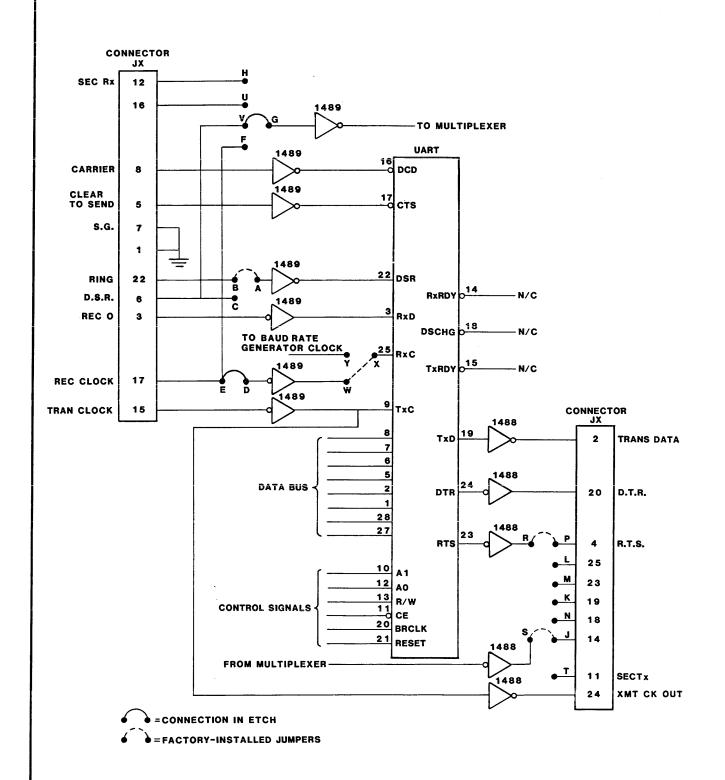


Figure 5-8. CAl2/V Line Adapter Panel Channel Schematic



NO.		DATE	>	
	AD0006	06	Apr	1984
PAGE:	20	OF	25	

6.0 MAINTAINING FCC CLASS A COMPLIANCE

Emulex has tested the CSll Communications Subsystem with DEC computers that comply with FCC Class A limits for radiated and conducted interference.

The CCll and CPl2 are designed to be imbedded in the CPU cabinet. When properly installed, those two components do not cause compliant computers to exceed Class A limits.

There are two possible configurations in which the CCll and CPl2 can be installed:

- 1. With the CCll Controller Module and the CP12 Distribution Panel both mounted in the same CPU cabinet, and
- 2. With the CCll mounted in the CPU cabinet and the CP12 mounted in a separate expansion cabinet.

To limit radiated interference, DEC completely encloses the components of their computers that generate or could conduct radio frequency interference (RFI) with a grounded metal shield (earth ground). When installing these two imbedded components, nothing must be done that would reduce this shield's effectiveness. That is, when the CCll and CPl2 installation is complete, no gap in the shield that would allow RFI to escape can be allowed.

Conducted interference is generally prevented by installing a filter in the ac line between the computer and the ac outlet. Most power distribution panels that are of current manufacture contain suitable filters.

The steps which must be taken to maintain the integrity of the shield and to limit conducted interference are explained fully in section 7 (CP12 Distribution Panel Installation).

7.0 CP12 DISTRIBUTION PANEL INSTALLATION

The CP12 Distribution Panel is designed for rack mounting within the DEC CPU cabinet or in a separate expansion cabinet. As noted in section 6, the proper installation of the CP12 is critical with respect to radiated and conducted interference. Subsections 7.1.1 and 7.1.2 detail techniques for installing the CP12 in the same cabinet as the CC11 Controller Module or in a separate expansion cabinet, respectively. The installations described are designed to limit interference to acceptable levels.

Mount the CP12 on the cabinet rack with its RS-232-C connectors facing out. The required mounting hardware is included.

F F 059B (10783)



NO.		DATE	DATE:	
	AD0006	06	Apr	1984
PAGE:	21	OF	25	

7.1 SAME CABINET

If the CCll Controller and CPl2 Distribution Panel are mounted in the same cabinet, the main concern is installing the Panel in such a way that no gaps are left in the shield. The CPl2 Distribution Panel is designed to be rack mounted on the rear RETMA rails of the CPU cabinet. This area is typically shielded with a bulkhead from the top to the bottom of the cabinet. The bulkhead is segmented to allow different options to be installed. The general procedure is to remove one of the bulkhead segments and replace it with the CPl2 Panel. To maintain the integrity of the RFI shield, no gap must remain above or below the Panel after it is installed. If the integrity of the shield is maintained, no other steps need be taken to ensure compliance.

Conducted interference should be prevented by the line filters that are installed by DEC in the CPU cabinets power distribution panel.

7.2 SEPARATE CABINETS

If the CP12 Panel is mounted in a separate cabinet from the CC11 Controller, then the expansion cabinet must be shielded against RFI radiation in much the same way that the DEC CPU is shielded. Also, the cable that connects the CC11 Controller to the CP12 Panel must be shielded since it runs outside of the shielded cabinet environment.

Emulex recommends using a hardened cabinet such as the Everest Electronic Equipment model EH9642 with the FCC option. The Everest, like the DEC CPU cabinets, has a full length, segmented bulkhead in the rear. One of the segments should be removed and replaced with the CP12 Panel. In addition, it will be necessary to install a CP22 rack mount chassis with a blank and a personality panel (these components are needed to allow the shielded cable from the CC11 to be terminated). As in the DEC cabinet, there must be no gap above or below the two rack mounted panels when the installation is complete.

To prevent the introduction of conducted interference on the ac line that feeds the CP12 Panel's power supply, a power distribution panel with a line filter must be installed in the expansion cabinet.

Marway Products Incorporated's model MDP110 contains a Filter Concepts 1020 EMI Filter, which is adequate.

7.3 CABLING THE CC11 CONTROLLER TO THE CP12 DISTRIBUTION PANEL

A single 34-conductor flat cable connects the CCll Controller to the first CPl2 Distribution Panel. Additional panels are daisy-chained from the first (additional cables are provided with the additional panels). An un-shielded, eight-foot cable is provided with the CSll, which is adequate for installations that have the CCll Controller and CPl2 Panel mounted in the same cabinet. If the two componets are mounted in separate cabinets, the 34-wire cable that runs between (and thus outside of the shield provided by the cabinet) must be shielded to prevent excessive levels of radiated interference.



NO.		DATE			
		AD0006	0,6	Apr	1984
	PAGE:	22	OF	25	

The installation of the 34-wire cable between CCll and CPl2 components in the same cabinet is described in subsection 7.1.1. Installation of shielded cables between components in separate cabinets is discussed in subsection 7.1.2.

7.3.1 Non-Shielded Cable Installations

An un-shielded, eight-foot cable is provided with the CS11; cables 15 feet or longer can be ordered (Emulex part number CS1111201-04=15 ft, -05=35 ft, -06=50 ft).

The flat cable is connected as follows:

- 1. Find the arrow that is molded into the header at either end of the cable. The arrow identifies pin 1 of the cable header.
- 2. Find the corresponding arrow on CCll connector Jl.
- 3. Align the arrow on the cable header with the arrow on connector Jl and plug the cable connector into Jl.
- 4. With one end of the cable plugged into connector Jl of the CCll, find the arrow on the cable header at the other end of the cable. Align this arrow with the corresponding arrow on connector Jl of the distribution panel and plug the connectors together.
- 5. For additional panels, connect the cable between J2 of the first panel and to J1 of the next (observe the alignment instructions of steps 3 and 4).
- 6. Terminate the daisy chain with the terminator board by placing it in J2 of the last panel.

7.3.2 Shielded Cable Installations

When it is necessary to run the 34-wire cable that connects the CCll and the CPl2 Panel between two cabinets, the cable must be shielded to prevent excessive RFI. In such cases, the 34-wire cable is broken up into three segments, one external and shielded, and two internal and un-shielded. The external cable's shield is grounded to the cabinet at each end of the cable using a clamping bracket. The clamping brackets are called personality panels and mount in a special holder that allows them to be rack mounted. The part numbers for the cables, personality panels, and rack mount chassis are given in Table 7-1.

F059F(10783)



NO.		DATE:		
	AD0006	06	Apr	1984
PAGE:	23	OF	25	

Table 7-1. Shielded Cables and Installation Hardware

Item	Part Number	Description	Quantity Required
1.	CU3211202-02 CU3211202-03 CU3211202-04 CU3211202-04	Shielded Cable, 8 ft Shielded Cable, 15 ft Shielded Cable, 25 ft Shielded Cable, 35 ft	1
2.	CU3211201-01 CU3211201-02 CU3211201-03 CU3211201-04	Extension Cable, 2 ft Extension Cable, 4 ft Extension Cable, 6 ft Extension Cable, 8 ft	2
3.	CU3210202	CP12 Personality Panel	2
4.	CU2213102	Rack Mount Chassis Kit	2

Un-shielded

The items listed in Table 7-1 can be ordered from your Emulex sales representative or directly from the factory. Contact:

Emulex Customer Service 3545 Harbor Boulevard Costa Mesa, CA 92626 (714) 662-5600 TWX 910-595-2521

To install the 34-wire cable between the CCll Controller and CPl2 Distribution Panel use the following procedure:

- Select an extension cable long enough to run from the CCll Controller Module to the proposed location of the personality panel in the CPU cabinet.
- Find the arrow that is molded into the female header of the cable. The arrow identifies pin 1 of the cable header.
- 3. Find the corresponding arrow on CCll connector J2.
- 4. Align the arrow on the cable header with the arrow on connector J2 and plug the cable connector into J2.
- 5. Select an extension cable long enough to run from the first CP12 Distribution Panel to the proposed location of the personality panel in the expansion cabinet.



NO.		DATE:		Aug.	
	AD0006	06	Apr	1984	
PAGE:	24	OF	25		

NOTE

To allow the 34-wire cable to be properly daisy chained between several CPl2s, begin the daisy chain with the uppermost CPl2. Take this into consideration when selecting an extension cable. If the personality panel is located at the bottom of the rack and there are several CPl2s, the extension cable will have to run from the bottom of the cabinet to the uppermost CPl2 Panel.

- 6. Find the arrow that is molded into the female header of the cable. The arrow identifies pin 1 of the cable header.
- 7. Find the corresponding arrow on CP12 connector J1.
- 8. Align the arrow on the cable header with the arrow on connector Jl and plug the cable connector into Jl.
- 9. For additional panels, connect the cable between J2 of the first panel and to J1 of the next (observe the alignment instructions of steps 7 and 8).
- 10. Terminate the daisy chain with the terminator board by placing it in J2 of the last panel.
- 11. Install the rack mount chassis kits in the CPU and expansion cabinet racks. Make sure that no gap is left between the rack mount chassis and the bulk head above it or below it. Pull the extension cables from both the CCll Controller and the CPl2 Panel through the empty mounting cut outs in the two rack mount chassis.
- 12. Select a shielded cable of appropriate length and route the cable between the two cabinets.
- 13. Strip about one inch of shield insulation from one end of the cable to expose the shield. Cut the shield at each edge to allow the shield to be folded back over the insulation. Route the cable through the personality panel and clamp the exposed shielding securely in the personality panel. See detail, Figure 7-1. Repeat this process at the other end of the cable.
- 14. Find the arrow that is molded into the female header of the shielded cable at the CPU end.
- 15. Find the corresponding arrow on the loose end of the extension cable. Align the arrows and plug the cables together. Repeat this process at the expanion cabinet end of the cable.

EF059B(10783)



NO. DATE:					
		AD0006	06	Apr	1984
	PAGE:	25	OF	25	

16. At the CPU cabinet, insert the personality panel into the rack mount chassis and finger tighten the eight captive screws. Repeat at the expansion cabinet.

The letter callouts in Figure 7-1 denote the following equipment:

- A the cabinet with the CPU
- B the external cable
- C the expansion cabinet
- G & H the rack mount chassis and the CP12 personality panel

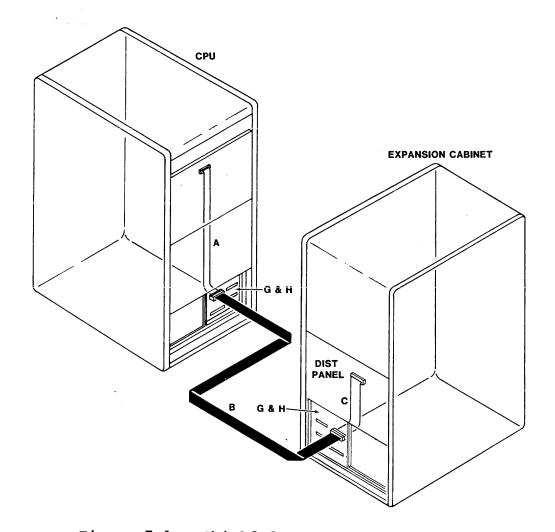


Figure 7-1. Shielded Cable Installation



Reader's Comments

State/Country _____

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publication. Manual Part Number _____ Rev. ____ What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? What features are most useful? What faults or errors have you found in the manual? Does this manual satisfy the need you think it was intended to satisfy? Does it satisfy *your* needs? ______ Why? _____ ☐ Please send me the current copy of the *Controller Handbook*, which contains the information on the remainder of EMULEX's controller products.

Additional copies of this document are available from:

Company _____

Department _____

Emulex Corporation 3545 Harbor Boulevard P.O. Box 6725 Costa Mesa, CA 92626 Attention: Customer Services Fold Here and Staple

Do Not Tear — Fold Here



NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 202 COSTA MESA, CA

POSTAGE WILL BE PAID BY ADDRESSEE
EMULEX CORPORATION
3545 HARBOR BOULEVARD
P.O. BOX 6725
COSTA MESA, CALIFORNIA 92626
ATTN: TECHNICAL PUBLICATIONS