SC02/L

(RL01/RL02 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL

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INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC02/L Disk Controller. In addition, this manual provides diagnostics and application information.

1.2 OVERVIEW

1.2.1 General Description

The SC02/L Disk Controller is a one board, imbedded controller for LSI-11 computers manufactured by Digital Equipment Corporation. This controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC02/L controller emulates the RLV11/RLV12 disk controller manufactured by Digital Equipment Corporation for use with RL01 and RL02 disk drives.

1.2.2 SC02/L Emulation of RL01 and RL02

The RLV11/RLV12 provides a convenient controller architecture for a wide variety of modern technology type disks. It is supported by all DEC operating systems and is easy to program.

The SC02/L controller can handle two disk drives. The drives need not be of the same type or manufacture. The controller configures each drive from the information in a configuration PROM. This technique permits up to 64 different switch selectable combinations of disk drive arrangements.

1.3 FEATURES

1.3.1 Microprocessor Design

The SC02/L design incorporates a unique 8-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various sizes.

1.3.2 Packaging

The SC02/L is constructed on a single, quad-size, multi-layer PC board which plugs directly into the LSI-11 chassis. No cabling is required between the computer and the disk controller. The controller obtains its power from the chassis in which it is mounted.

1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the LED ON and the controller cannot be addressed from the CPU.

1.3.4 Buffering

The controller contains a 1K x 8 high-speed RAM buffer. It is used to store the device registers of the controller plus a full 512 byte data sector. This buffering permits multiple sector reads with a 3-to-1 sector interlace format. Buffer operations eliminate the possibility of a data late condition and permits the controller to be operated at low bus priorities.

1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits in length and detecting bursts of longer length. The controller determines the location of the error and the pattern so that the software may correct the data after it is transferred to memory. A 32-bit CRC is employed with the header of every sector.

1.3.6 Option and Configuration Switches

Sockets provide for insertion of optional 512 word boot strap PROMS and Q-Bus termination resistor packs. Provisions are also made to enable an optional software-controlled line time clock (LTC) which is BDV11 compatible.

DIP switches are used to configure the controller for various disk sizes, Q-Bus addresses and options. It is possible to select one of 64 possible combinations of disk characteristics for the two drives which can be handled by the controller, inculuding mixtures of disk sizes and drive type codes.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Media Compatibility

In all cases, the headers written on the drives are not standard RL01/RL02 headers. In addition, a three-to-one or two-to-one sector interleave is generated by the hardware formatter. Packs may be formatted by utilizing the hardware formatting capability of the extended command set. Disk packs formatted with an SC02/L controller are not media compatible with other Emulex controllers or with RL01/RL02 packs.

1.4.2 Disk Mapping

Depending upon the type and size of the disk drive, one to four logical units may be mapped on it. Various mapping organizations are used; most of which do not leave direct 1:1 correlation between the logical and physical addresses.

1.4.3 Diagnostics

The SC02/L will run the following DEC diagnostics on LSI-11 computers. No modification of the diagnostic is required.

- ZRLKB1 Performance Exerciser
- ZRLMB0 Bad Sector File Tool

1.4.4 Operating Systems

The SC02/L is compatable with all DEC operating systems running on LSI-11 computers that support DEC RL01 or RL02 disk subsystems. No operating system modifications are required.

Table 1-1
RLV11/RLV12/RL01/RL02 Disk Subsystem Characteristics

Characteristics	Specifications RL01	RL02
Surfaces/Drive	2	2
MBytes/Logical Unit	10.24	20.48
Blocks/Drive	10,240	20,480
Tracks/Cylinder	2	2
Cylinders/Drive	256	512
Sectors/Track	40	40
Data Bytes/Sector	256	256
Sectors/Block	2	2
Drives/Controller, Max	4	4

Table 1-2
General Specification

Functional	
Emulation	DEC RL01 and RL02
Media Format	3-to-1 or 2-to-1 sector interlace
Drive Interface	Storage Module Drive (SMD)
Number of Drives	2 maximum
Error Control	32-bit ECC for data and 32-bit CRC for headers. Correction of single data error burst of up to 11 bits.
Sector Size	256 words (512 bytes)
Sectors/Track	Selectable for each physical drive
Tracks/Cylinder	Selectable for each physical drive
Cylinders/Drive	Selectable for each physical drive
Drive Type Code	Selectable RL01 or RL02 for each physical drive
Computer Interface	LSI-11 Q-Bus
Vector Address	214 Standard, 140 Optional
Priority Level	Level 5
Data Bufferring	1 Sector (256 words)
Data Transfer	High speed DMA operation
Self-Test	Extensive internal self-test on powering up

Table 1-2 (Cont.)
General Specification

Functional	
Indicator	Activity/Error/Status LED
Options	512 word bootstrap/Q-Bus terminators/BDV11 compatible Line Time Clock (LTC) control
Q-Bus Addresses	Controller registers: 774400-774406 Bootstrap prom: 773000-773776 and 765000-765776 LTC register: 777546
Design	High-speed bipolar microprocessor using 2901 bit-slice components
Physical	
Mounting	Any LSI-11 Quad slot in CPU or expansion box
Connectors	One 60-pin A cable flat connector and two 26-pin B cable connectors. (Flat cable type.)
Electrical	
Q-Bus Interface	DEC approved line drivers and receivers
Drive Interface	Differential line drivers and receivers. A cable accumulative length to 35 feet. B cable length to 25 feet.
Power	+5V,5%,5A.

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2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC02/L controller is shown in Figure 2-1. The controller is organized around a 8-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with two 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 1K words is implemented with twelve 1K x 4 PROMs.

The controller incorporates a 1K x 8 high-speed RAM buffer which is used to store the controller's device registers and one sector (512 bytes) of data buffering.

The A Cable Register (ACR) latches all A cable signals going to or form the disk drives. The inputs from the selected drive are testable by the microprocessor.

The Shift Register converts parallel write data from the data bus to serial data for the disk drives. The register also converts serial read data from the drives back into parallel data. Serial read and write data is provided to the ECC logic via the Shift Register.

Serial data from the drive is converted into eight-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data access from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 32-bit CRC mode for the headers. The actual ECC polynomial operation is done independently of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

The Q-Bus interface consists of 42 bidirectional and two unidirectional signal lines. The Q-Bus interface is used for programmed I/O, CPU interrupts, and data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA operations and transfers data between the Q-Bus data lines and the buffer.

2.2 PHYSICAL DESCRIPTION

The SC02/L controller consists of a single quad-size board which plugs directly into a LSI-11 chassis. The controller PCBA is shown in Figure 2-2.

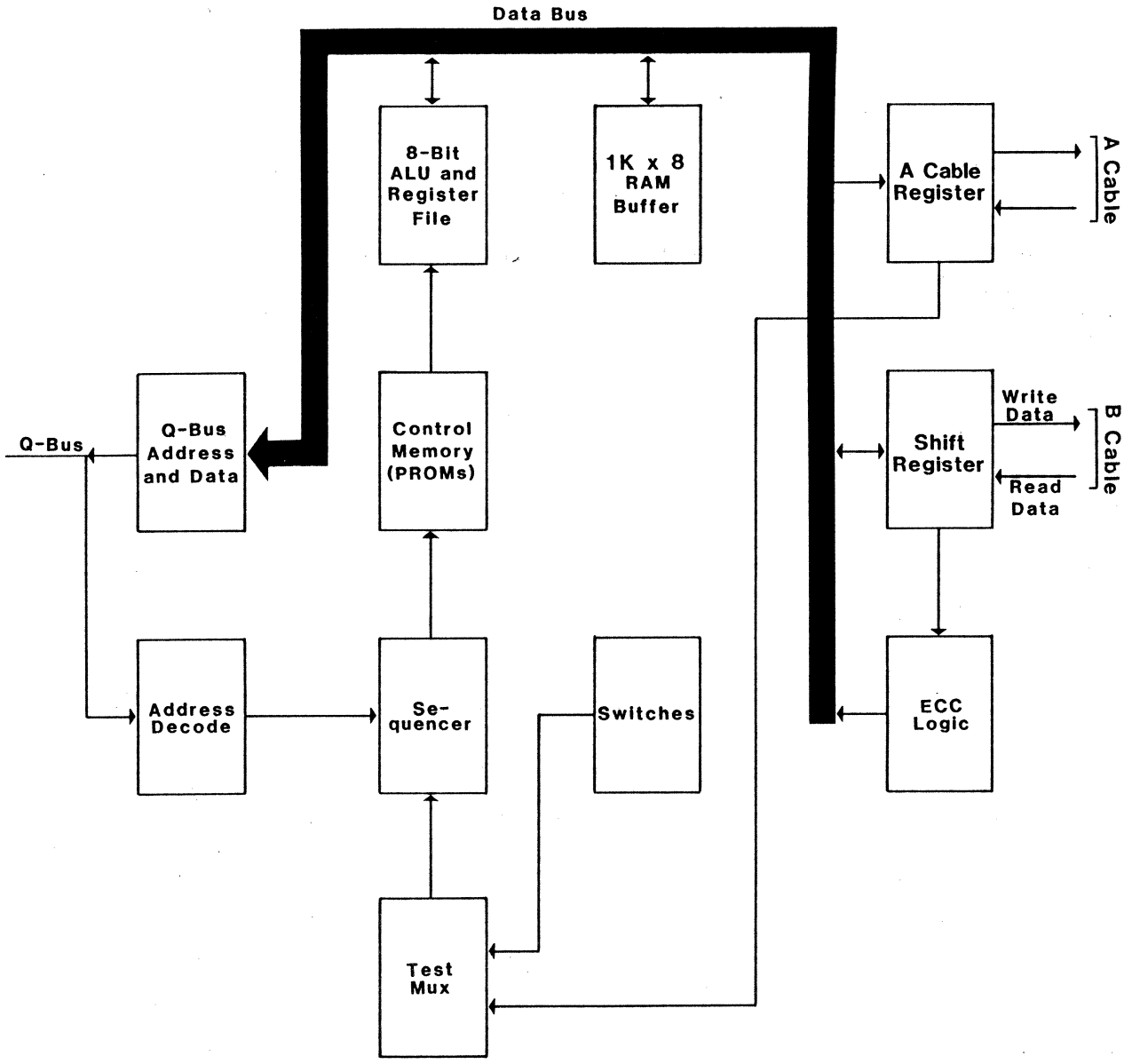
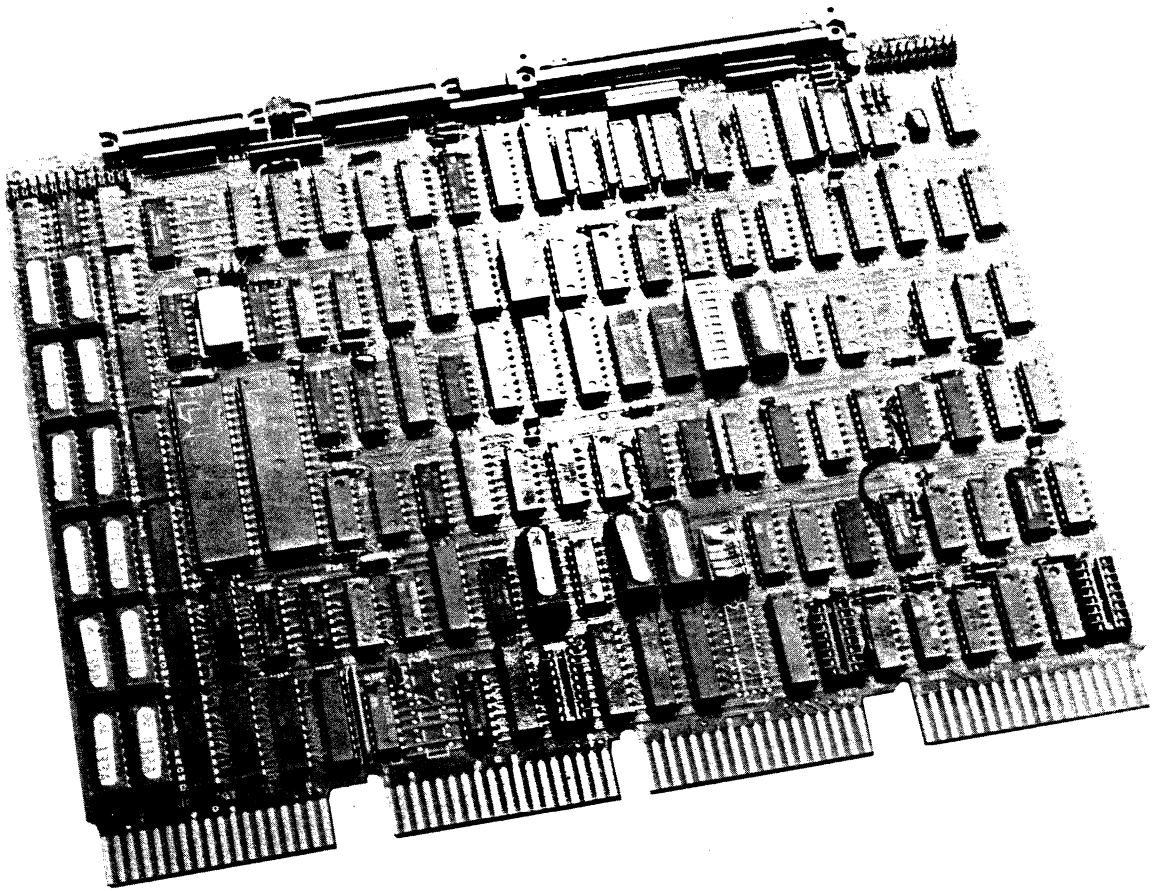


Figure 2-1 SC02 Block Diagram



SC0203-0029

Figure 2-2 SC02 Controller Board

2.2.1 Connectors

2.2.1.1 A Cable Connector

The 60-pin flat cable connector labeled J3 at the top edge of the board is for the A cable which daisy-chains to all the drives for control and status. Pin 1 is located on the left side of the connector.

2.2.1.2 B Cable Connector

The two 26-pin flat cable connectors labeled J1 and J2 are for the radial B cables to each of two physical drives which may be attached to the controller. Pin 1 is located on the left side of the connector. The two B cable ports are all identical and any drive may be plugged into any connector.

2.2.1.3 Test Connectors

Connectors J4 and J5 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2 Switches

There are three sets of switches labled SW1-SW3. SW1 is a four pole DIP "piano-type" switch accessible from the PC board edge. Locating SW1 such that it is accessible to the operator while the controller is imbedded in a LSI type chassis, makes the selection of common options such as hardware format simpler to perform.

The other two sets of switches SW2 and SW3 provide controller address decoding selection, option selection and drive configuration selection. (See Appendix A for a complete description of the switch functions.)

2.2.3 LED Indicator

There is an LED indicator mounted beside the connector at the top of the board. The controller executes an extensive self-test when powering up. The microprogrammed organization of the controller permits most logic other than the interface circuitry to the disk to be validated before the controller becomes ready. The LED lamp is turned ON as the controller starts its self-test and is turned OFF only when the controller successfully completes the test. If a malfunction is detected by the built-in diagnostics, the LED remains ON and the controller will not respond to program I/O. The LED blinks at approximately a one second rate if the self-test is successful but no drive is seen on-line. The LED also functions as an activity indicator during read and write operations.

2.2.4 Firmware PROMs

There are twelve PROM sockets, used for the control memory, located along the left edge of the board. The sockets are labeled ROM 0 through ROM 11 in a discontinuous physical order. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket.

2.2.5 Bootstrap PROMs

There are two sockets provided for the installation of optional bootstrap PROMs. The socket in location U101 receives P/N 014x and the socket in location U103 receives P/N 015x.

2.3 INTERFACES

2.3.1 Disk Interface

The controllers's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatable with these drives electrically and in timing.

The following defines the electrical interface and the recommended cables.

2.3.1.1 A Cable

The 60-conductor A cable is daisy-chained to all drives and terminated at the last drive. The signals in this cable are listed in Table 2-1 along with their function when the control tag (Tag 3) is asserted. The A cable should be a 30-twisted-pair flat cable with an impedance of 100 ohms and a cumulative length of no greater than 35 feet.

Spectra-Strip P/N 455-248-60 flat cable or its equivalent is recommended. It is possible to order A-Cable assemblies from Emulex that are made up in one of four lengths:

EMULEX P/N	LENGTH (FT.)
SU1111201	8.0
SU1111203	15.0
SU1111205	25.0
SU1111207	35.0

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
1,31	Tag 1		To
2,32	Tag 2		To
3,33	Tag 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	AM Found		From
21,51	Busy (dual-port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Pick		To
59	Power Sequence Hold		To
B Cable:			
8,20	Write Data		To
6,19	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
9,22	Unit Selected		From
10,23	Seek End		From
12,24	Not Used		From
13,26	Not Used		From

2.3.1.2 B Cable

The 26-conductor B cable is radial to all drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-1. The B cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 25 feet.

3M-P/N 3476/26 flat cable or its equivalent is recommended. It is possible to order B-cable assemblies from Emulex that are made up in one of four lengths:

EMULEX P/N	LENGTH (FT.)
SU1111202	8.0
SU1111204	15.0
SU1111206	25.0

2.3.2 Q-Bus Interface

The LSI-11 Bus consists of 42 bidirectional and 2 unidirectional signal lines. These form the lines along which the processor, memory and I/O devices communicate with each other.

Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The lines are divided as follows:

1. Twenty-two data/address lines - <BDAL00:BDAL21>
2. Six data transfer control lines - BBS7, BDIN, BDOUT, BRPLY, BSYNC, BWTBT
3. Three direct memory access control lines - BDMG, BDMR, BSACK
4. Six interrupt control lines - BEVNT, BIAK, BIRQ4, BIRQ5, BIRQ6, BIRQ7
5. Five system control lines - BDCOK, BHALT, BINIT, BPOK, BREF.

The MS four data/address lines (BDAL <21:18>) are used only for addressing and do not carry data. BDAL <17:16> reflect the parity status of the 16-bit data word during the data transfer portion of the bus cycle.

2.3.2.1 Interrupt Priority Level

The controller is hardwired to issue level 4 and level 5 interrupt requests. The level 4 request is necessary to allow compatibility with either a LSI-11 or LSI-11/2 processor.

Table 2-2
Q-Bus Connections

	A		B	
	1	2	1	2
A	BIRQ5	+5V	BDCOK	+5V
B	BIRQ6		BPOK	
C	BDAL16	GND	BDAL18	GND
D	BDAL17		BDAL19	
E		BDOUT	BDAL20	BDAL02
F		BRPLY	BDAL21	BDAL03
H		BDIN		BDAL04
J	GND	BSYNC	GND	BDAL05
K		BWTBT		BDAL06
L		BIRQ4		BDAL07
M	GND	BIAKI	GND	BDAL08
N	BDMR	BIAKO	BSACK	BDAL09
P	BHALT	BBS7	BIRQ7	BDAL10
R	BREF	BDMGI	BEVNT	BDAL11
S		BDMGO		BDAL12
T	GND	BINIT	GND	BDAL13
U		BDAL00		BDAL14
V		BDAL01		BDAL15

2.3.2.2 Register Address

The register address and the number of registers assigned to the controller are decoded by a PROM at U104. The selections available are determined by configuration switch SW1 as discussed in Appendix A.

2.3.2.3 DCOK and INIT Signals

The DCOK and INIT signals both perform a controller clear. The self-test is performed only when DC power is initially applied.

2.4 LOGICAL DISK FORMAT

To the system software, the SC02/L disk subsystem appears to be formatted exactly as would an RL01 or RL02. In actual fact, the controller firmware multiplies the logical address out to obtain a block address which is then divided by the physical drive configuration constants to provide an address for the physical drive. For this reason a 1:1 correspondence between logical and physical addresses will most likely not exist.

Depending upon the type and size of the disk drive, one to four logical units may be mapped on it. The controller can handle a maximum of four logical units distributed across a maximum of four physical disk drives.

2.4.1 Sector Format

2.4.1.1 Header Field

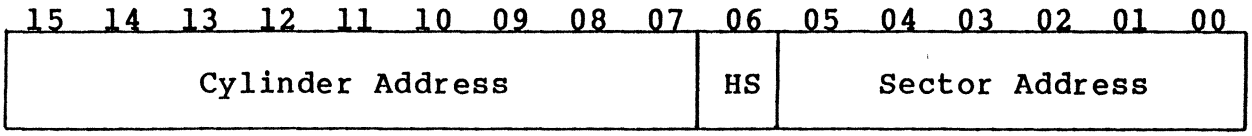
The logical header can be read by software by issuing the read header command. The header data is not acutally read from the disk, but is generated by the firmware in accordance with the logical position of the disk heads. The headers have the format illustrated in Figure 2-3.

2.5 PHYSICAL DISK FORMAT

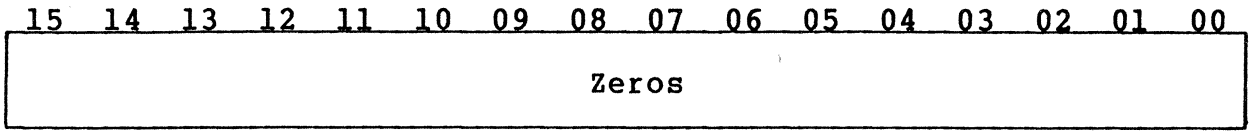
2.5.1 Disk Pack Organization

The formatting of a disk pack and the mapping of one or more logical drives onto a physical drive varies with the drive size. Some of this information is supplied by the configuration PROM. The rest is computed based upon configuration PROM information. In all cases, the headers actually written on the drives are not standard RL01/RL02 headers. In addition, a three-to-one or two-to-one sector interleave is generated by the hardware formatter. A two-to-one sector interleave is used when the physical disk drive has 23 sectors or less per track. Otherwise, a three-to-one interleave is used. Disk packs formatted with an SC02/L controller are not media compatible with other Emulex controllers or with RL01/RL02 packs.

Header Word 1:



Header Word 2:



Header Word 3:

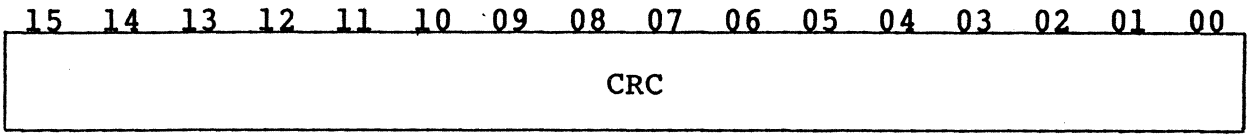
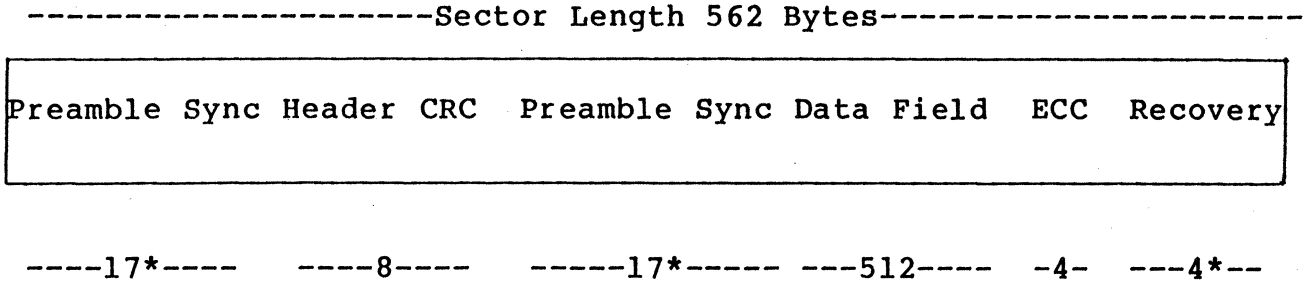


Figure 2-3 Logical Header Format



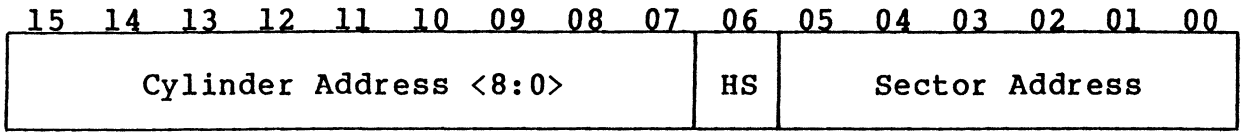
*Values shown are minimums which apply to most Winchester type units. However, these values may vary to accomodate different physical drive types and are determined by configuration PROM data.

Figure 2-4 Sector Format

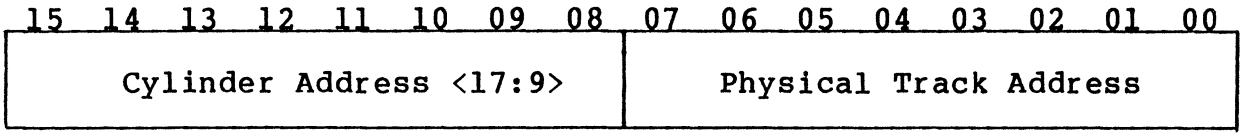
2.5.2 Mapping

Depending upon the type and size of the disk drive, one to four logical units may be mapped on it. The controller can handle a maximum of four logical units distributed across a maximum of four physical disk drives. A logical drive may not be mapped across a physical unit boundary.

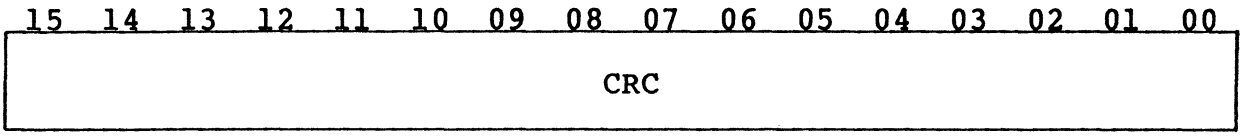
Header Word 1:



Header Word 2:



Header Word 3:



Header Word 4:

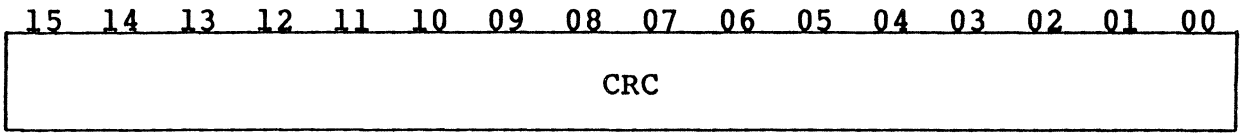


Figure 2-5 Physical Header Format

2.5.3 Sector Format

Each sector contains a detached two-word header and a 256 word data field. The header field is terminated with a two vertical check characters and the data field is terminated with a 32-bit ECC. The controller attempts corrections only on the data field, never on the header. Each field is preceded by at least 11 bytes of zero's and an eight-bit SYNC byte.

In detail, each sector is organized as illustrated in Figure 2-4.

2.5.3.1 Header Field

The header preamble is used to synchronize the Phase Locked Oscillator (PLO) in the drive to the data on the pack. The SYNC byte is used by the controller to synchronize to the data bytes and their boundaries, and by the drive to synchronize to the phase of the data stream. The two header data words are organized as illustrated in Figure 2-5.

2.5.3.2 Data Field

The data field preamble and SYNC bytes have the same functions as the header preamble and SYNC bytes. The data field itself is always 256 words long. Any unused portion of the sector will be terminated with zero bytes during a write operation. The 32-bit ECC is generated during a write, and is used during a read to check the validity of the data. Any single error burst anywhere in the data field of 11 bits or less may be corrected.

2.5.3.3 Postambles

The postambles provide areas for turning off the write amplifiers, for turning on read amplifiers, and for switching from read-to-write. Write splices will exist within all of these areas. The sector pulse postamble will also include a head-scatter area on removable media drives.

2.5.3.4 Recovery Area

The recovery area along with the preceeding postamble is required for head-scatter tolerances on removable media drives.

2.6 REPLACED TRACKS

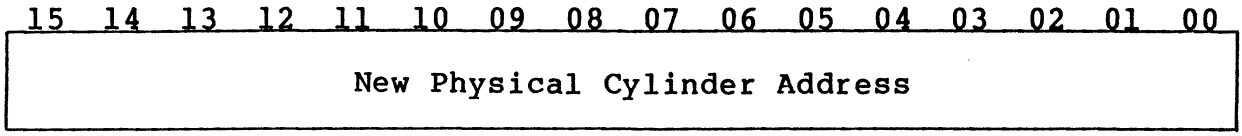
The four words of the Replaced Track Header are written consecutively over the entire corrupted track. The Replaced Track Header contains the address of the track that is being substituted for the corrupted track. The Replaced Track Header is illustrated in Figure 2-6, below.

The substitute track to which the Replaced Track Header points looks exactly as the corrupt track would if replacement had not been required. This duplication includes the cylinder and track addresses contained in the header for each sector.

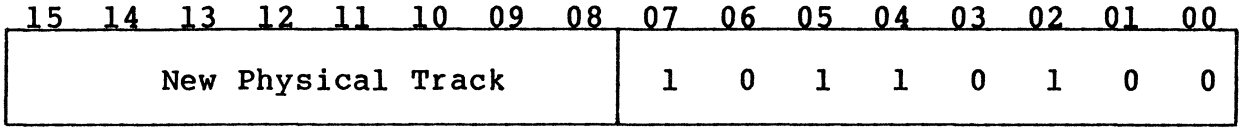
When a sector (and thus a track) has been identified as corrupt, its physical address can only be obtained by examining the controller's internal registers. This is necessary because the read header command implimented by the SC02/L gives only the logical track address and not the physical. The controller does not impliment a physical read header command.

To obtain the physical address of a bad sector, the program should issue a read of the preceding logical sector. Next, the program should issue the multipurpose command (0). This will cause the all of the firmware registers to be loaded into the data silo. The software may then access the registers by repeatedly reading the Multipurpose Register (MPR). Words 118, 119 and 120 will contain the physical address (cylinder, track and sector, respectively) of the logical sector immediately following the one just read, which will be the address desired.

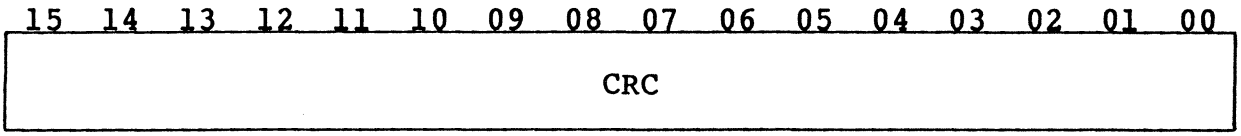
Header Word 1:



Header Word 2:



Header Word 3:



Header Word 4:

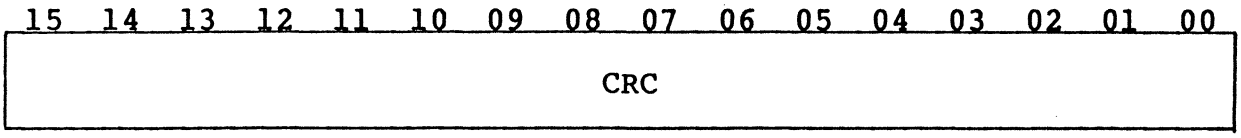


Figure 2-6. Replaced Track Header Format

Because a logical track may be mapped over two physical tracks, it is necessary to read each sector before and after the corrupt sector and examine the physical address of each. By reading each logical sector below and above the corrupt sector and watching the physical track address obtained with the mulipurpose command we can determine the physical track boundries in relation to the logical sectors. When the physical track address changes we know that the lower or upper limits of the track. We can then correlate the logical sector addresses with physical track limits.

This information is required so that the headers and data on the track with the corrupted sector can be moved to the replacement track. The information is also necessary to allow the appropriate logical sectors to be written with the replaced track headers.

2.7 GENERAL PROGRAMMING INFORMATION

2.7.1 Interrupts

The controller will request an interrupt if the IE bit and the CRDY bit are both set in the CSR. The IE bit is set or reset by the software and reset with the initialize condition. The CRDY bit is set by the hardware upon completion of a function or upon the setting of an error flag. It is also set by the initialize condition. It is reset by the software to cause the controller to start a function (negative GO bit). The interrupt vector address is 160. The normal priority level for the RL11 is BUS REQUEST 5. The RLV11 Controller uses the one priority level provided by the LSI-11 processor.

2.7.2 Seek Operations

The following sequence is an example of performing a seek function.

1. Issue read header function to drive and wait for interrupt or wait for CRDY.
2. Check error flag.
3. Read the header word from the MP register.
4. Calculate difference and direction for the seek.
5. Move difference word to the DA register.
6. Issue seek function to drive and wait for seek to be completed as indicated by drive ready bit.
7. Check error flag.

A software system that optimizes positional latency would keep current cylinder and head select information in core so that Steps 1, 2 and 3 would be unnecessary.

2.7.3 Overlapped Seeks

Since the controller comes ready and interrupts as soon as a seek is issued, it is possible to issue seeks to additional drives while the first is seeking. However, no interrupt occurs when the seeks are completed, so the transfer command should be issued to the drive requiring the shortest seek as soon as all seeks are issued. In this way, the drive completing its seek first will immediately perform its transfer and interrupt when done.

2.7.4 Data Transfer

Data transfer is via DMA facility. The SC02 provides, as does the RLV11, 256 words of FIFO (RAM) buffering which prevents data lates from occuring. Transfers to memory are initiated after the entire sector has been read. Transfers to the disk are initiated only after an entire sector of data has be loaded into the FIFO.

To do a data transfer, the software should perform the following steps:

1. Load BA register with address of first memory location to be transferred.
2. Load DA register with address of first disk location to be transferred.
3. Load WC register with two's complement of number of words to be transferred.
4. Issue read data or write data and wait for interrupt or test for ready.
5. Check error flag.

Other drives could do seeks or data transfers between the issuing of seek and the issuing of the data transfers.

2.7.5 Recovering of Data with Bad Headers

Function 7, read data without header check, is provided to allow the recovery of data should headers become unreadable. If constant HNF or HCRC errors are encountered on a particular sector so that the data is not recoverable by the standard read command, proceed as follows. Perform successive read header commands until the sector preceding the bad sector is found. Then, issue a read data without header check. The data portion of the next sector will be read without either header compare or header CRC check. Data CRC errors will be reported.

2.7.6 Error Correction

The controller automatically corrects correctable errors in the data during read commands using the ECC characters appended to each data dield. To allow the operating system to log errors, the correction operation will be only performed only on every other attempt to read a sector with an error. Correction is never attempted for bad disk data during write-check operations.

2.7.7 Deleted Commands

The SC02/L emulates the RLV11/RLV12 controller in its responses to all normal commands and register modifications.

2.7.8 Extended Commands

The SC02/L incorporates extended commands not implimented by the RLV11/RLV12 controllers. These commands allow the media to be formatted, allow track replacement to be accomplished, allow write protection of logical disk drives and allow various diagnostic functions. For details, see paragraph 5.2 of this manual.

2.7.9 22-Bit Memory Addressing

Twenty-two bit addressing capability is available as an option for the SC02. The Emulex part number for the option kit is SC0213102. The kit consists of a single AMD2908 IC which is placed in socket U127 on the SC02 PCBA.

Twenty-two bit memory addressing is enabled by closing SW2-7. In this mode the SC02/L is emulating the RLV12 which incorporated this feature. Bits <05:00> in the address extension register (BAE) then serve as address bits <21:16>. Address extension bits 17 and 16 are duplicated in the CSR (bits 05 and 04, respectively) and they may be modified or examined via either BAE or CSR.

WARNING

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an SC02 with the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. An SC02 without the addressing option will not be damaged if power is present on those lines.

2.7.10 Line Time Clock (LTC)

The Line Time Clock is a 60 Hz clock generated by the power supply and distributed on the backplane as the BEVNT signal. A high to low transition of this signal interrupts the processor. BEVNT has the highest external interrupt priority; only processor interrupts have higher priorities. If external interrupts are enabled (PS bit 07 = 0), the processor PC (R7) and PS words are pushed onto the processor stack. The LTC (or external event device) service routine is entered by vector address 100; the usual interrupt vector adddress input operation by the processor is not required since vector 100 is generated by the processor.

The LTC can be software controlled by using the Line Clock Register on the SC02/L. The Line Clock Register has a bus address of 777546. It is a one-bit, write-only register. Reads to this register return unspecified data. Bit 06 is the only bit implemented. A write to this register with bit 06 = 1 enables the line clock. A write to this register with bit 06 = 0 disables the line clock. The enable bit need not be set again after an interrupt has been processed. The clock will continue to interrupt until bit 06 is reset or an INIT is generated.

See paragraph 3.4.4.4 for information on how to configure the processor for use with the LTC.

2.7.11 Bootstrap Routines

Installing the Emulex bootstrap option kit (number SC0213001) makes available two bootstrap routines: the standard console bootstrap and auto-boot sequence. See paragraph 3.4.4.2 for installation instructions.

2.7.11.1 Standard Console Bootstrap

The CPU enters the standard console bootstrap routine at location 773000. The CPU board can be jumpered to start at location 773000 automatically on power-up (or external DCLO set-reset). See paragraph 3.4.4.2.

After performing several CPU tests, the bootstrap program will prompt the operator with a dollar sign ($) on the standard terminal (bus addresses 777560-777564). At this point the bootstrap routine expects terminal input. If no $ is printed, then the boot program failed one of the CPU tests it executed prior to entering terminal input mode.

When the $ prompt has been printed, the boot program is ready for input from the terminal. The user should enter one of the two-character codes from the Table 2-3 (plus a single octal number if one is required and the unit number to be booted is not zero) followed by a carriage return. The two-character codes represent bootstarp routine for specific device types. When the code is entered, the routine that the code represents will be executed. If the code is not recognized, a question mark (?) is printed, followed by the $. The code to use for the SC02/L is "DL".

If the code selected represents a peripheral device boot routine, then the controller will execute three more CPU tests and two memory tests prior to executing the actual boot. The two memory tests will check all available memory, but they require a minimum of 8K bytes (0-17776) to operate.

Table 2-3
Bootstap Routines

XC	=	Execute CPU tests 7-9 only.
XM	=	Execute memory tests only.
OD	=	ODT Halt. No routines executed. A proceed (P) returns the program to the terminal input mode.
MTn	=	TM11 mag tape boot. Can boot units 0-7.
DXn	=	RXV11 floppy disk boot. Can boot units 0-1.
DKn	=	RK05 disk boot. Can boot units 0-7.
RPn	=	RP02/3 disk boot. Can boot units 0-7.
DMn	=	RK06/7 disk boot. Can boot units 0-7.
DBn	=	RM02/3/5 disk boot. Can boot units 0-7.
DRn	=	RP04/5/6 disk boot. Can boot units 0-7.
DYn	=	RX211/RX02 disk boot. Can boot units 0-7.
DLn	=	RL01/02 disk boot. Can boot units 0-7.
DD	=	TU58 tape boot. Can boot unit 0 only.

Note: If "n" is not entered, a default unit number of 0 is assumed.

The following is a list of halt locations which the PROM program will execute should the boot be unsuccessful.

HALT Address	Reason for HALT
765320	Non-existent unit, unit not on-line and ready, controller ready = 0
765612	Read Error, Disk Error aborted read
765674	Read failed to complete within time limit
773434	Failure in CPU test #7
773530	Failure in CPU test #8
773550, 773556, or 773604	Failure in CPU test #9
773730	Failure in Memory test #1
773760	Failure in Memory test #2

2.7.11.2 Auto-Boot Sequence

The auto-boot sequence will automatically bootstrap the system without operator intervention when the system is powered up or when an external DCLO signal is generated.

The CPU enters the auto-boot sequence at location 765000. The LSI-11/23 CPU can be jumpered to start at location 765000 automatically. See paragraph 3.4.4.2.

After performing a memory test, the auto-boot program will first attempt to boot the system from an RK06/07. If none is present, it will look for an RP02/03. If there is no RP02/03, it will attempt to find an RL01/02. In all cases, the auto-boot program will only attempt to boot from drive zero.

If none of the above drives is present, the program will print the $ prompt and expect the operator to enter a device code as described in paragraph 2.7.11.1, above.

Section 3
INSTALLATION

This section describes the step-by-step procedure for installation of the SC02/L Disk Controller in a LSI-11 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the SC02, is covered in paragraph 3.1).

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Inspect the SC02.
2. Prepare the disk drives.
3. Prepare the LSI-11.
4. Configure the SC02.
5. Install the SC02.
6. Route the drive I/O cables.
7. Run the diagnostics.

3.1 INSPECTION

A visual inspection of the board is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROMs should be examined carefully to insure that they are firmly and completely seated in the sockets.

3.2 DISK DRIVE PREPARATION

3.2.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC02. This allows the I/O cable routing and length to be accurately judged. Place the drives side by side to make installation of the daisy-chained cable simpler.

3.2.2 Local/Remote

The LOCAL/REMOTE switch controls whether the drive can be powered up from the drive (local) or the controller (remote). Place the switch in the REMOTE position. With the LSI-11 powered down, press the START switch on the front panel of each of the drives (the

START LED will light, but the drive will not spin up and become ready). When the LSI-11 is powered up, the drives will spin up sequentially. This prevents the heavy current draw that would be caused if all of the drives were powered up at once. When in the remote mode the drives will power down when the LSI-11 is powered down. While the LSI-11 is powered ON, the drives may be powered up and down individually (to change disk media, for example) using the drive START switch.

3.2.3 Sectoring

See Appendix A, Configuration Selection, for the correct sector count settings for the disk drives in use. The exact method of entering the sector count differs from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure. A minimum of 576 bytes per sector are required for proper operation.

3.2.4 Unit Addressing

An ID plug in the range of 0-1 should be placed in the drive. Be careful that the drives do not have the same number. Some drives have their address selected by means of switches on one of the logic cards and do not use an ID plug. See the drive manuafacturer's manual for details.

3.3 SYSTEM PREPARATION

3.3.1 Powering Down the System

Power down the system and switch OFF the main AC breaker at the rear of the cabinet (the AC power indicator will remain lit). Slide the CPU out of the cabinet and remove the top cover. Tilt the card cage up to obtain access to the CPU and other moduals.

3.4 CONTROLLER SETUP

Several configuration setups must be made on the controller before inserting it into the chassis. These are made by SW1, SW2 and SW3.

3.4.1 Controller Address Selection

All Q-Bus controllers have a block of several command and status registers through which the system can command and monitor the controller. The registers are addressed sequentially from a starting address assigned to that device type, in this case a disk controller.

The starting address for the controller's Q-Bus registers is selected by DIP switch SW3. A normal starting address of 777440 is obtained by placing switch SW3-2 in the ON position. An alternate address of 776700 is available by closing SW3-3. Both SW3-3 and SW3-2 should not be closed at the same time.

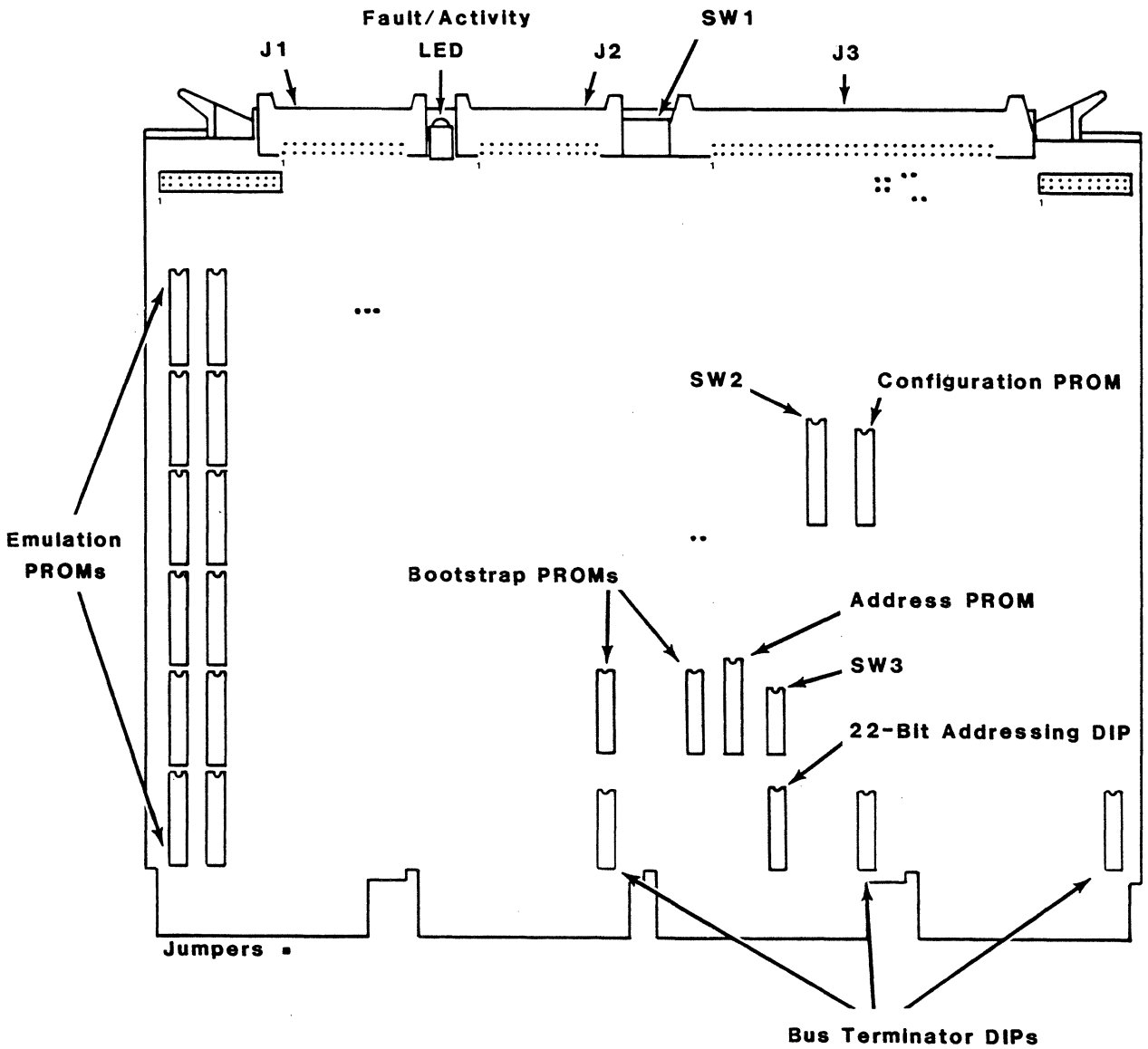


Figure 3-1 SC02 Controller Assembly

3.4.2 Interrupt Vector Address

One of two interrupt vector addresses is selected by means of switch SW2-7. The standard controller vector address of 214 is selected when the switch is open (OFF). Closing the switch selects a vector address of 140.

3.4.3 Drive Configuration Selection

The phrase "drive configuration selection" describes the process that is used to configure the SC02 to use a particular type of physical disk drive to perform the RL01/RL02 emulation. That is, you have a particular set of physical disk drives. You must tell the controller what kind of physical disk drive you are going to use. On the SC02, switches SW2-1 through SW2-6 are used for that purpose.

For ease of manual maintenance the configuration table for the SC02 is contained in Appendix A.

3.4.4 Option Installation

There are a number other SC02 options that can be implimented by the user. These features are selected by physically installing the option on the PCBA or enabling it using one of the option switches.

3.4.4.1 Q-Bus Terminator Option

To provide the equivalent of 120 ohms electrical termination to the

Q-Bus, DIP resistor networks are installed in U123, U129, and U135. These resistor packs provide a 180 ohm resistor connection to +5 volts and a 390 ohm resistor connection to ground on each Q-Bus line.

These three resistor networks may be ordered from Emulex or the customer may provide his own terminating resistor networks by using an equivalent part such as BOURNS P/N 4116R-003-181/391, or BECKMAN 898-5-r180/390, or CTS 761-5-R181/391.

WARNING

> Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an SC02 with the Q-Bus Terminator Option in such a system will damage the option ICs. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. If there is power on any of the above lines and you wish to use the terminator option, cut pins 1, 4, 5 and 14 of the IC in socket U129. An SC02 without the option will not be damaged if power is present on those lines.

3.4.4.2 Bootstrap PROM Option

The Bootstrap Option is a firmware routine executed by the CPU that loads the system memory with software that is stored on disk or tape. The option kit consists of two PROMs. Its Emulex part number is SC021301. See paragraph 2.7.11 for operating information.

To install the option, place the PROM labled 015x in socket U101 and the PROM labled 014x in socket U103.

The bootstrap option has two sections, standard console bootstrap and auto-boot. The standard console bootstrap routine is entered by the CPU at address 773000, DEC's conventional starting address. The auto boot sequence is entered at address 765000.

The LSI-11 and LSI-11/02 both require that power-up mode 2 be selected to take advantage of the standard console bootstrap option. This is done by installing jumper W6 and removing jumper W5 on the CPU PCBA. The configuration for both the LSI-11 and the LSI-11/02 is the same. The auto-boot routine is not available for these units.

The LSI-11/23 may be configured to take advantage of either the standard console boot or the auto-boot routines. This CPU also requires that power-up mode 2 be selected (install jumper W6 and remove jumper W5 on the CPU PCBA). The bootstrap starting address, however, is selected using jumpers W8 through W15. To select the standard console bootstrap routine install W8. This will cause the processor to default to starting address 773000. To use the auto-boot option, remove W8, W10 and W12; install W9, W11, W13, W14 and W15.

3.4.4.3 22-Bit Memory Addressing

Twenty-two bit addressing capability is available as an option for the SC02. The Emulex part number for the option kit is SC0213102. The kit consists of a single AMD2908 IC which is placed in socket U127 on the SC02 PCBA. See paragraph 2.7.9 for programming instructions.

WARNING

> Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an SC02 with the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. An SC02 without the addressing option will not be damaged if power is present on those lines.

3.4.4.4 Line Time Clock Option

The Line Time Clock Option allows program control of the Line Time Clock. This feature is enabled by closing (ON) SW3-5 on the SC02 PCBA. See paragraph 2.7.10 for programming instructions.

Before the LTC can be used, the CPU must be configured to enable that feature. On the LSI-11 and LSI-11/02, remove jumper W3 (BEVNT Line Enable). On the LSI-11/23, remove jumper W4 (BEVNT Line Enable). The LTC switch on the front panel must also be ON.

When using the SC02 with the RSTS operating system, the Line Time Clock Option must be OFF (SW3-5 = open). The CPU should be configured to enable the option, however.

3.5 PHYSICAL INSTALLATION

3.5.1 Slot Selection

If the three optional Q-Bus terminator resistor networks are installed, the SC02 should be installed in a quad slot such that it provides the termination required at the end of the bus.

If the optional Q-Bus terminators are not installed, the SC02 may be assigned to any desired slot since it uses the LSI four-level interrupt scheme to perform distributed interrupt arbitration.

3.5.2 Mounting

The controller board should be plugged into the LSI-11 backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the boards with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly in the throat of the connector before attempting to seat the board by means of the extractor handles.

3.6 CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-2.

3.6.1 A Cable

The 60-wire A cable should be plugged into the connector on the A board of the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the other drives. The last drive on the A cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board

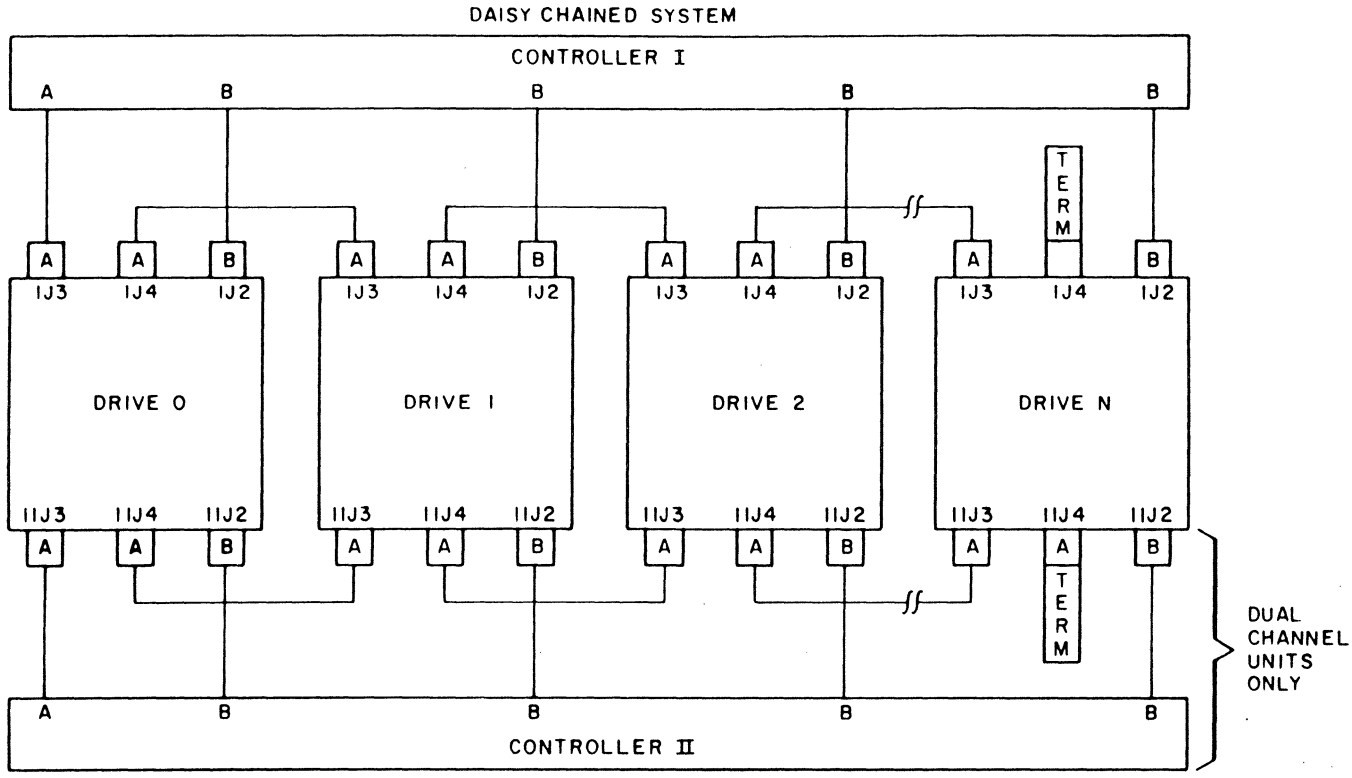


Figure 3-2 Cabling Diagram

connector is on the left. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

3.6.2 B Cable

Each drive must have a 26-wire B cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe.

NOTE: Observe the same caution on connector reversal given in paragraph 3.6.1.

3.6.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic

ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.7 TESTING

Note: The register addresses given below are 18-bit addresses. For 22-bit machines add 17000000 to obtain the correct address for each register (i.e., 777440 becomes 17777440).

3.7.1 Self-Test

When power is applied to the CPU, the controller automatically executes a built-in self test. This self test is not executed with every bus INIT but only on powering up. If the self test has been executed successfully, the LED on the top edge of the controller board will be OFF or flashing. The LED flashes when the controller cannot properly address at least one drive after successfully executing its self test. This will occur if the A and B cables are not properly plugged in, a drive is not powered up with a code plug, or two drives have an identical code plug. If the LED is ON steadily the controller did not pass its self test and the controller cannot be addressed from the CPU.

3.7.2 Register Examination

After powering up the CPU and noting that the LED indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. The Control Status Register (CSR) 7774400 will contain 000201 if the controller and drive 0 are ready.

3.7.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and bad sector file data in all sectors of the disk. This command does not verify the data or headers.

If the drive is on line, the formatting is carried out as follows. Repeat the operation for each drive to be formatted.

1. Deposit 000013 into DAR (774404).

2. Select the drive to be formatted by depositing the drive number in bits 09 and 08 of CSR (774400). Bit 02 must also be set simulaneously.

3. Examine CSR (774400). Bit 15 (error) should be zero, and bit 01 should be 1 (drive ready).

4. Deposit a number to be used as a pack ID in MPR (774406).

5. Deposit 100001_8 in BAR (774402) to enable the extended command set.

6. Deposit a hardware format command (34004 for drive 0, 34404 for drive 1, 35004 for drive 2 or 35404 for drive 3) for the appropriate dive in CSR (774400) to start formatting. The Activity LED will flash as long as the format operation is in progress. When it goes completely out, the operation is complete.

3.7.4 Diagnostics

The following DEC RL01/RL02 diagnostics should be run.

- ZRCMB0 - Bad Sector File Tool
- ZRLKB1 - Performance Exerciser

BLANK

The standard RLV12 has five registers that are used to control and monitor operations within the controller and disk drive units. In addition to the standard registers, the SC02/L incorporates three extra registers that are used to impliment extended features such as the ability to format the disk media. All of the registers are described in detail in the paragraphs below.

4.1 CONTROL STATUS REGISTER (CSR)

4.1.1 CSR Normal Functions

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	DE	NXM	E2	E1	E0	DS1	DS0	CRDY	IE	BA17	BA16	F2	F2	F0	DRDY

Composite Error (ERR) - Bit 15

When set, this bit indicates that one or more of the error bits (bits <14:10> is set. If the IE bit (bit 06 of CS) is set and an error occurs (which sets bit 07), and interrupt will be initiated.

Drive Error (DE) - Bit 14

This bit reports error status directly from the emulated drive. When set, it indicates that the selected drive has flagged an error. (The source of the error can be determined by executing a Get Status command.)

DE can be cleared by executing a Get Status command with bit 03 of the DA register set.

Non-Existent Memory (NXM) - Bit 13

This bit is set when the addressed memory does not respond within 10 to 20 usec of the beginning of a direct memory access (DMA) data transfer.

Data Late (DLT) or Header Not Found (HNF) - Bit 12

This bit is set during a write when the silo is empty but the word count has not yet reached zero (meaning that the bus request was ignored for too long). The OPI bit will not be set.

When this and OPI are both set, the controller could not find the correct sector to read or write (no header compare - HNF).

ERROR SUMMARY

ERROR NAME	BITS 12	11	10
OPI	0	0	1
Read Data CRC	0	1	0
Write Check	0	1	0
Header CRC	0	1	1
Data Late	1	0	0
Header Not Found	1	0	1

Data CRC (DCRC) or Header CRC (HCRC) or Write Check (WCE) - Bit 11

If OPI (bit 10) is cleared and this bit is set, a CRC error has occurred when reading the data (DCRC).

If OPI (bit 10) is set and bit 11 is also set, the CRC error has occurred on the header (HCRC).

If OPI (bit 10) is cleared and bit 11 is set and the function command was a write check, a write check error (WCE) has occurred.

NOTE: Cyclic redundancy checking is performed on the first and second header words, even though the second header word always contains zeros.

Operation Incomplete (OPI) - Bit 10

When set, this bit indicates that the current command could not be completed.

Drive Select (DS0, DS1) - Bits <09:08>

These bits determine which drive will communicate with the controller via the drive bus.

Controller Ready (CRDY) - Bits 07

When cleared by software, this bit indicates that the command in bits <03:01> is to be executed. When set, this bit indicates the controller is ready to accept another command.

Interrupt Enable (IE) - Bits 06

When this bit is set by software, the contoller is allowed to interrupt the processor at the normal command or error termination.

Bus Address Extension Bits (BA16, BA17) - Bits <05:04>

The two most significant bus address bits. Read and written as data bits 05 and 04 of the CS register but considered as address bits 16 and 17 of the bus address register.

Function Code - Bits <03:01>

These bits are set by software to indicate the command to be executed.

Command execution requires that bit 07 (controller ready) be cleared by software. A zero bit being transferred into bit 07 of the CSR can be considered a GO bit.

F2	F1	F0	Command	Octal Code
0	0	0	Maintenance	0
0	0	1	Write Check	1
0	1	0	Get Status	2
0	1	1	Seek	3
1	0	0	Read Header	4
1	0	1	Write Data	5
1	1	0	Read Data	6
1	1	1	Read Data Without Header Check	7

Drive Ready (DRDY) - Bit 0

When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a seek operation is initiated and set when the seek operation is completed.

4.1.2 CSR Extended Functions

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	1	1	1	0	0	0	0	0	0	0	F3	F2	F1	F0

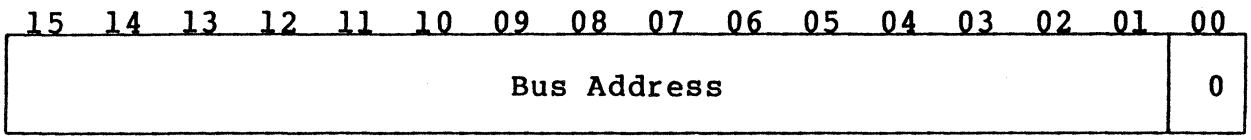
To enable the extended command set, BAR must be written with 100001_8. The command is then immediately written into CSR with bits <13:11> set to one and with the extended command function code set into bits <03:00>.

Function Code (<F3:F0>) - Bits <03:00>

The function code selects one of the extended commands as shown in the table below. All codes are even. Codes 6 through 16 are reserved.

Code No.	F3	F2	F1	F0	Command
0	0	0	0	0	Multipurpose Command
2	0	0	1	0	Write Header Command
4	0	1	0	0	Firmware Format Command

4.2 BUS ADDRESS REGISTER (BAR)



The Bus Address Register (BAR) is a 16-bit register with an address of 774402. Bits <15:01> can be read or written; bit 00 is always zero. Bus address bits 16 and 17 are contained in bits 05 and 04 of the CSR.

The BAR indicates the memory location involved in the data transfer during a normal read or write operation. The contents of the BAR are automatically incremented by two as each word is transferred between the bus and the I/O buffer. This register overflows into CSR bits 05 and 04.

The BAR is cleared by initializing the drive or by loading the register with zeros.

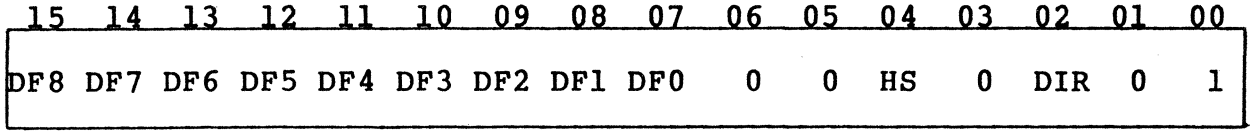
Bus Address - Bits <15:00>

These bits point to the UNIBUS address that data is to be transferred to/from (normally a memory address). Bit 00 is always zero. BA16 and BA17 are in CSR bits 05 and 04.

4.3 DISK ADDRESS REGISTER (DAR)

The Disk Address register (DAR) is a 16-bit register with an address of 774404. Its contents can have one of three meanings, depending on the function being performed. This register is cleared by initializing the device or loading the register with zeros. All 16 bits can be read or written by the processor.

4.3.1 DAR During a Seek Command



To perform a Seek function, it is necessary to provide cylinder address difference, head select, and head directional information to the selected drive as indicated.

Cylinder Address Difference (DF) 08:00 - Bits <15:07>

Indicates the number of cylinders the heads are to move on a seek.

Head Select (HS) - Bit 04

Indicates which head (disk surface) is selected. A one indicates the lower head; a zero, the upper head.

Direction (DIR) - Bit 02

This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits <15:07>).

4.3.2 DAR During Read or Write Data Command

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	HS	SA5	SA4	SA3	SA2	SA1	SA0

For a read or write operation, the DA register is loaded with the address of the first sector to be transferred. As each successive sector is transferred, the DA register is automatically incremented.

Cylinder Address (CA) 08:00 - Bits <15:07>

Address of the cylinders being accessed. (Range is 0 through 777, octal)

Head Select (HS) - Bits 06

Indicates which head (disk surface) is to be selected. A one indicates the lower head; a zero, the upper head.

Sector Address (SA) 05:00 - Bits <05:00>

Address of one of the 40 sectors on a track

4.3.3 DAR During a Get Status Command

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	0	0	0	0	RST	0	1	1

For a Get Status command, the DAR bits must be programmed as indicated in the figure above.

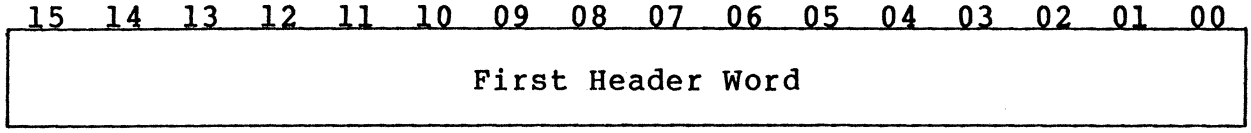
Reset (RST) - Bit 03

When this bit is set, the drive clears its error register before sending a status word to the controller.

Get Status (GS) - Bit 01

Must be a one, indicating to the drive that the status word is being requested. At the completion of the Get Status command, the drive status word can be read from the controller Multipurpose (MP) register (see paragraph 4.4). With this bit set, the drive ignores bits <15:08>.

4.3.4 DAR During a Write Header Command (extended)



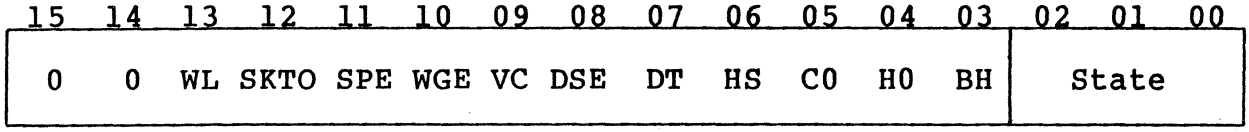
First Header Word - Bits <15:00>

Before executing a Write Header command, the first header word is loaded into DAR. See the discussions in paragraphs 2.5.3.2 and 2.6 for descriptions of the normal header format and replaced track header format, respectively.

4.4 MULTIPURPOSE REGISTER

The Multipurpose Register (MPR) is a 16-bit register with an address of 744406. This register has several different bit meanings, as explained below.

4.4.1 MPR after a Get Status Command



When a Get Status command (paragraph 4.3.3) is executed the status word is returned to the controller and transferred to the MPR. The contents of the MPR are defined as follows.

Write Lock (WL) - Bits 13

Set when the drive is logically or physically write protected.

Seek Time Out (SKTO) - Bit 12

Set when seek cannot be completed on a drive because of a drive fault or because it has gone off-line.

Write Gate Error (WGE) - Bit 10

Set if an attempt is made to write on a drive that is logically or physically write protected.

Volume Check (VC) - Bit 09

Set when physical drive becomes on-line and ready. Cleared by execution of a Get Status command with RST (bit 03) asserted.

Drive Type (DT) - Bit 07

A zero indicates an RL01; a one, an RL02.

Head Select (HS) - Bit 06

Indicates the currently selected head. A zero indicates the upper head; a one, the lower head.

Cover Open (CO) - Bit 05

Set when physical drive is not on-line and ready.

Heads Out (HO) - Bit 04

Set when physical drive is on-line and ready.

Brush Home (BH) - Bit 03

Set when physical drive is not on-line and ready.

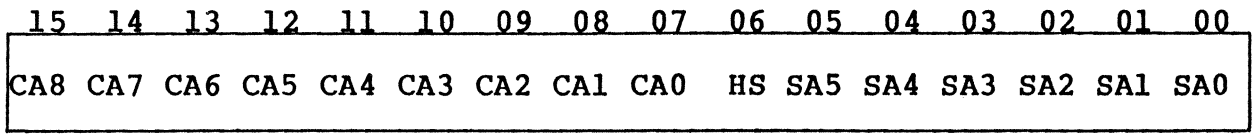
State (State) - Bits <02:00>

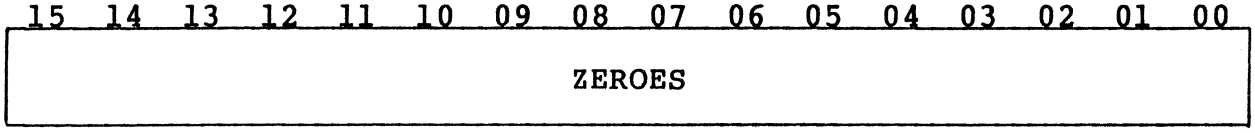
These bits define the state of the drive.

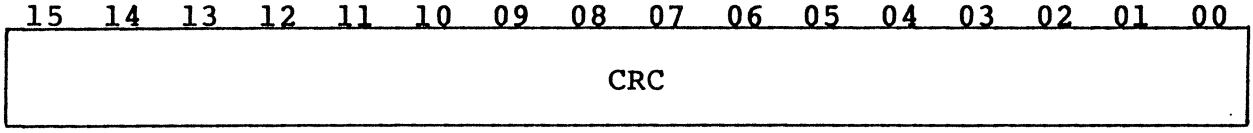
02	01	00	
0	0	0	Load Cartridge - drive exists but not on line
1	0	0	Seek - Seek state
1	0	1	Lock On - normal ready state

4.4.2 MPR after a Read Header Command

When a Read Header command is executed, the next header will be read and its three words will be stored in the data buffer and transferred to the MP register. The first word will contain sector address, head select, and cylinder address information. The second word will contain all zeros. The third word will contain the header CRC information. All three words can be read sequentially by the program.







Cylinder Address (CA) 08:00 - Bits <15:07>

Address of the cylinders being accessed. (Range is 0 through 777, octal)

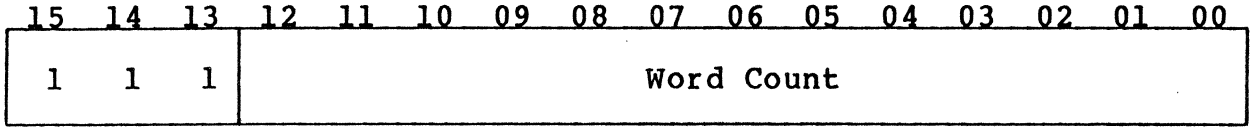
Head Select (HS) - Bits 06

Indicates which head (disk surface) is to be selected. A one indicates the lower head; a zero, the upper head.

Sector Address (SA) 05:00 - Bits <05:00>

Address of one of the 40 sectors on a track

4.4.3 MPR During Read/Write Data Commands



Before the reading or writing data, the program should load the word count into the MP register in two's complement form. The counter is incremented as each word is transferred. Usually, the reading or writing operation is terminated when the word counter reaches zero (overflows). The word counter can keep track of any number of data words, from one to the full 40-sector count of 5120 data words (decimal). Bits <15:13> must be ones.

Word Count (WC) 12:00 - Bits <12:00>

Contains the two's complement of total number of words to be transferred. Bit 00 is the LS bit.

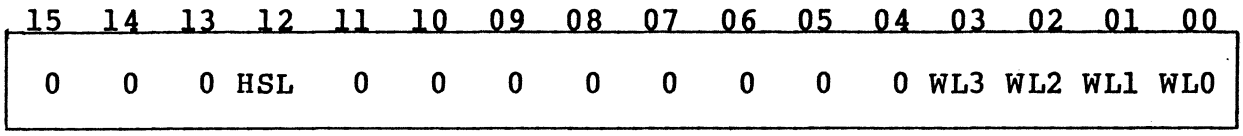
MPR PROGRAMMING NOTE - The RL01/RL02 Disk Drive will not do spiral read/writes. If data is to be transferred past the end of the last sector of a track, it is necessary to break up the operation into the following steps.

1. Program the data transfer to terminate at the end of the last sector of the track.

2. Program a seek to the next track. This can be either a head switch to the other surface but same cylinder or a head switch and move to the next cylinder.

3. Program the data transfer to continue at the start of the first sector at the next track.

4.4.4 MPR During Multipurpose Command (extended)



15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	HSL	0	0	0	0	0	0	0	0	WL3	WL2	WL1	WL0

The figure above defines the bits of the MPR during a Multipurpose Command. The bits should be set in this register prior to issuing the Multipurpose command.

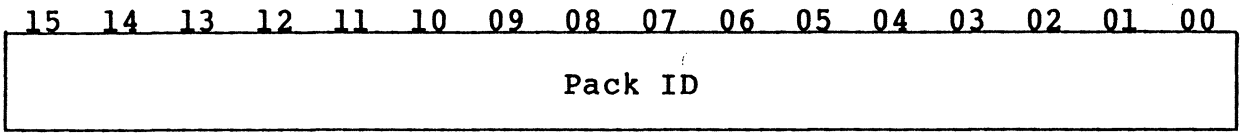
Header Search Limit (HSL) - Bit 12

When set, this bit limits header search attempts to one revolution of the disk instead of three.

Write Locked (WL) <3:0> - Bits <03:00>

When set, bits <03:00> cause logical drives 3 through 0 to be write locked, respectively. Each bit may be set independently of the others.

4.4.5 MPR During Write Header Command (extended)



15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Pack ID															

During Write Header commands the MPR is loaded with the Pack ID that is used for the Bad Sector File. The MPR must be loaded prior to the issuance of the Write Header Command.

Pack ID - Bits <15:00>

The Pack ID that is used for the Bad Sector File.

4.5 BUS ADDRESS EXTENSION (BAE) REGISTER

The Bus Address Extension Register is a 16-bit register with an address of 744410. This register has several different bit meanings as decribed below.

4.5.1 BAE During Read or Write Data Commands

15	14 13 12 11 10 09 08	07 06	05 04 03 02 01 00
0	Cylinder Address <15:09>	0 0	Bus Address <21:16>

Cylinder Address <15:09> - Bits <14:08>

These bits function as an extension of the cylinder address bits of DAR when expanded logical drives are configured on the subsystem. They are required to allow the larger cylinder addresses of the expanded logical disk to be specified.

Bus Address <21:16> - Bits <05:00>

These six bits serve as an extension of the BAR to allow 22-bit bus addresses to be specified for DMA transfers. Bits 00 and 01 (BA16 and BA17) are the same as bits 04 and 05 of the CSR. Bits 05:02 function as bus address bits 18:21 only if the RLV12 mode is enabled (SW2-7 ON).

4.5.2 BAE During Write Header Commands (extended)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Second Header Word

Second Header Word - Bits <15:00>

Prior to invoking a Write Header command, the second word of the header that is to be written is loaded into this register. See the discussions in paragraphs 2.5.3.2 and 2.6 for descriptions of the normal header format and replaced track header format, respectively.

4.6 REGISTER 5

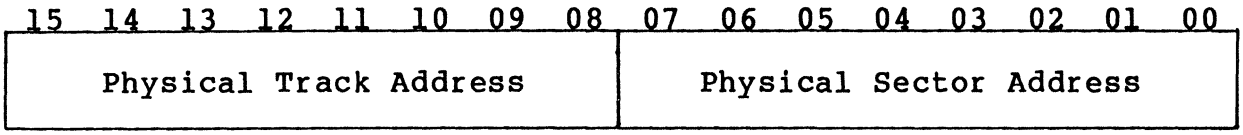
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Physical Cylinder Address

Physical Cylinder Address - Bits <15:00>

Before initiating a Write Header command, the physical cylinder address on which the header is to be written must be loaded into

this register. This register may be read or written anytime the controller is not busy.

4.7 REGISTER 6



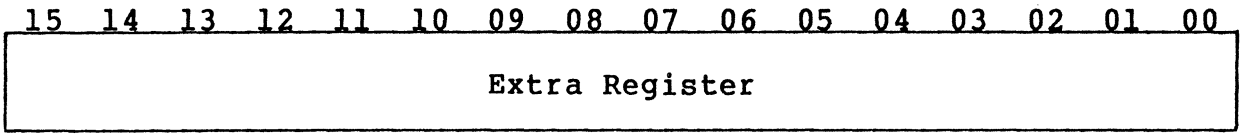
Physical Track Address - Bits <15:08>

Before initiating a Write Header command, the physical track address on which the header is to be written must be loaded into the MS byte of this register. Register 6 may be read or written anytime the controller is not busy.

Physical Sector Address - Bits <07:00>

Before initiating a Write Header command, the physical sector address of the sector to be written must be loaded into this the LS byte of this register. Register 6 may be read or written anytime the controller is not busy.

4.8 REGISTER 7



Extra Register - Bits <15:00>

Register 7 is an extra register that may be read or written if the controller is not busy. Data written to or read from this register has no significance.

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5.1 STANDARD FUNCTIONS

5.1.1 Write Check - Function Code 1

The write check command is used to verify that data was written on the disk correctly. It is used after writing a block of data onto the disk and compares it with the contents of its source data buffer in main memory. Because this comparison is performed in the controller, this source data must be transferred out of memory and into the controller silo.

Prior to issuing this command, the BA register must be loaded with the address of the first location of the data block in main memory. The word counter register must be loaded with the data block length. The DAR is then loaded with the starting disk address location. At this point, the write check command can be loaded into the CSR.

Once a header match is found, and the header CRC validates the match, the 128 words of data are read from the disk. The data is then compared serially with the serial data comming out of the silo (SER DATA OUT). Either a compare error or a data CRC error will set bit 11 in the CSR.

5.1.2 Get Status - Function Code 3

The Get Status command causes the status word from a drive to be transferred to the controller where the software can access it through the MPR. The software should first verifiy that the controller is ready to perform an operation (the drive does not have to be ready). Then, thesoftware should load the DAR with ones in bits 01 and 00, a reset bit at 03 and seros in the other locations. Next, the software should load the CSR with drive select bits, a negative GO bit, IE (if desired) and a code of 2 in the function bits. The controller will now command the selected drive to transfer it status word to the MPR in the controller. If the "reset" bit was set, the drive would reset its status register first.

5.1.3 Seek - Function Code 3

The seek operation causes the positioner to move (either forward or reverse) some number of cylinders. The software should first verify that the drive is ready to accept a command, then load the DAR with the difference word (difference between the present position and desired position). This word contains the number of cylinders to move (bits 15 through 07), the head select bit (04) and the direction bit (bit 02, 1=forward, 0=reverse). Bits 06, 05 and 01 must be reset and bit 00 must be set. After the DAR is

loaded, the software should load the CSR with the command word. This word should contain the drive select bits, the negative GO bit, IE bit if desired and a code of 3 in the function bits. The controller sends the Seek command to the selected drive, causing the drive to start its Seek operation. At this time, the contoller goes ready and interrupts if IE is set. The controller is now ready to accept another command to perform another operation on another drive while the Seek is occurring.

If the difference word is large enough that the heads attempt to move past the innermost or outermost limits, the head will stop at the guard band and retreat to the first even-numbered data track.

5.1.4 Read Header - Function Code 4

When a Read Header function is decoded, the controller will read the first header encountered on the selected drive and place the three header words in the silo. They pass through the silo and stop with the first word in the MP register. The software can then access the first word to determine the current sector, head, and cylinder address. When the software extracts the first word from the MP register, the third word automatically moves in the MP. This is the CRC word. The software can now access it for checking purposes. (This comamnd is simulated, no acutal read of header takes place. Each time command is peformed the next sequential header data will be used.)

5.1.5 Write Data - Function Code 5

When this function is decoded with CRDY cleared, the controller starts reading successive header words and comparing them to the DA register. When a match is found, the header CRC is checked and, if correct, that sector is written with the words from memory designated by the BA register. The BA and MP registers (word count in two's complement form) are incremented for each word transferred. For partial sector writes, the remaining sector area is filled with zeros. At the end of the sector, the sector portion of the DA register is incremented. The next sector is written if all the words have not been written. At the end of the transfer, CRDY is set and an interrupt made if IE is set.

5.1.6 Read Data - Function Code 6

When this function is decoded, the controller begins reading successive header words and comparing them to the contents of the DA register. When a match is found, the header CRC is checked and, if correct, that sector is read and the words are placed in the memory location designated by the BA register. Both the BA and MP registers (word count in two's complement form) are incremented for each word transferred. This operation continues until the contents of the MP register is all zeros. Data CRC is checked and the DA register is incremented at the end of each sector. If the word count has not overflowed; the next sector is read. Otherwise, CRDY is set and an interrupt is made if IE is set.

5.1.7 Read Data without Header Check - Function Code 7

When this function is decoded, the data portion of the sector following the next sector pulse is read and the words requested are placed in the memory locations designated by the BA register. The BA and MP registers (word count in two's complement form) are incremented for each word transferred. The header is neither compared nor checked for CRC errors. Data CRC is checked at the end of a sector. If the word count has not overflowed, the next sector is read. Otherwise, CRDY is set and an interrupt is made if IE is set.

5.2 EXTENDED COMMANDS

The SC02/L will execute an extended set of commands not found on the RLV11/RLV12 controller. To execute any of the extended commands, an enable flag must be set prior to issuing the command. To set the enable flag (flag exists only in firmware register), the Spare Register must contain a 1 in bit 15 and a 0 in bit 14 as the RKMR3 register is written (normally a read-only register) with all ones. The enable flag is cleared by a controller reset, subsystem clear, bus INIT, or by executing any command. The following commands are effective only if the enable flag is set. Attempting any extended command except "27" without the enable flag set will result in the illegal function (ILF) bit of RKDS being set along with the controller error (CERR) bit of RKCS1.

5.2.1 Hardware Format - Function Code 4

The hardware format command (code 4 in CSR) will cause the entire logical drive to be formatted. All headers are written and the data fields are written with the bad sector file format which includes the pack ID number. The number entered into the Multipurpose Register will be used for the pack ID. The word count, Disk Address Registers and Bus Address Registers are not used in this command. The controller will become ready and will interrupt the processor (if enabled) when finished.

5.2.2 Multipurpose Command - Function Code 0

This command has several functions, one of which is to write protect a logical drive. This command is executed by writing a "0" into the CSR after which bits <03:00> of the Multipurpose Register (MPR) will be copied and used as the write protect switches for drives <3:0> respectively. A set bit will cause a drive to be write protected; a reset bit will cause the drive to be not write protected only if the physical disk unit which the drive is mapped onto is also not write protected.

A second function of this command is to load a firmware Switch Register. When the command is executed, bits <15:04> of the MPR are copied to an internal firmware Switch Register. The Switch Register bits are cleared by writing into them with this command or

whenever a power-up sequence occurs on the controller. Only one switch (bit 12) is used presently. When it is set, the number of disk revolutions before a header search may abort is limited to one revolution. Normally the search is continued for four revolutions except for write check commands, for which the search is limited to one revolution also.

A third function of this command is to fill the data silo with the first 255 words of the Firmware Register block which contains the Controller Registers and configuration constants. After the command has completed, successive reads of the MPR will enable software to read this information for diagnostic purposes. Words 118, 119 and 120 are of particular use for the track replacement function. Those words contain the physcial cylinder, track and sector address, repectively, of the sector which follows the last sector to be read or written.

As with other commands, the controller will become ready and interrupt the processor (if enabled) when its function is completed.

5.2.3 Write Unit Headers - Function Code 2

This command is executed by writing a "2" command into CSR. The primary function of this command is to allow track replacement by rewriting the headers of bad tracks. Before issuing the header write command, the Register 5 must contain the physical cylinder address, the Register 6 must contain the physical track (MS byte) and sector (LS byte) addresses, the Multipurpose Register must contain the Pack ID to be used in the construction of the Bad Sector File, and the Disk Address Register and the Bus Address Extension Register must contain the first and second header words, respectively.

The controller takes care of generating the header CRC. For writing the headers on the replaced track, the first header word should contain the cylinder address of the new track. The MS byte of the second word should contain the address of the new track and the LS byte should contain the code (264_8) that the controller uses to recognize a replaced track.

The replacement track must then be written using this command with the normal header format exactly as it would be found on the track that is being replaced. The standard physical header format is illustrated in figure 2.5. The first word contains the LS cylinder address bits, the head select bit and the sector address for the logical drive. The second word contains the LS cylinder address bits and the track address of the physical drive. The CRC characters are written by the firmware.

The Firmware combines two logical sectors onto one physical sector on the disk. Consequently, only even numbered logical headers are written on the disk. This fact is transparent to normal software, but must be considered when writing new headers. Sector

interleaving is done by the firmware and is transparent in any case.

The multipurpose command may be used to determine the actual physical address of logical sectors.

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APPENDIX A

SC02/L CONFIGURATION AND OPTION SELECTION

A.1 INTRODUCTION

To allow the user of the SC02/L the greatest amount of flexibility in selecting disk drives for his system, the SC02/L supports a wide variety of disk types and offers a number of other user selectable options. This appendix is designed as a quick reference to the various switches which make this flexibility possible.

A.2 CONTROLLER CONFIGURATION

The SC02/L unit is capable of controlling a variety of disk drives of various sizes and types. The various drives that are supported are defined by the Configuration PROM. Table A-1 is a list of the drive types and sizes that are supported. The user may choose between the available options by means of configuration switch SW2. The correct switch settings for each of the various configurations are given in Table A-2.

A.2.1 Single Drive Installations

To find the configuration setting that is suitable for your single disk drive installation, use the following process. Note that all configurations require that the drive be hard sectored as noted in the Sec column of Table A-1. See the manufacture's drive installation manual for instructions.

1. Locate your drive type and size in Table A-1. Note down the configuration number(s) assigned to your drive. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for the drive.

2. Set the switches on the drive that determine the number of hard sectors per track according to the sector figure from Table A-1. Also set the drive number to 0 using switches or jumpers on the drive. See the installation manual provided by the drive manufacturer for instructions.

3. Find the configuration number for your drive in the CONF NO. column of Table A-2. If there is more than one number for an individual drive, start with the smallest. Note that for most configuration rows, specifications are given for two physical drives, Units 0 and 1.

4. When you find the proper row, compare the Physical Drive cylinder, track and sector figures for Unit 0 in Table A-2 with the numbers you noted down from Table A-1. The track and sector numbers must match; the cylinder number from Table A-2 must be smaller than the number from Table A-1.

If those conditions are not met, go on to the next higher configuration number, etc, until you find a match.

5. When you find a match, set the Configuration Switches (SW2) as indicated in Table A-2. (Generally, there is more than one match. In such cases, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuration you like best, and set the Configurations Switches accordingly.)

A.2.2 Multiple Drive Installations (same type drive)

To find the configuration setting that is suitable for your multiple disk drive installation (drives same size and type), use the following process. Note that all configurations require that the drives both be hard sectored as noted in the Sec column of Table A-1. See the manufacture's drive installation manual for instructions. All multiple drive configurations that use only one type of drive have configuration numbers with a letter suffix. Configuration numbers without the suffix should be ignored.

1. Locate your drive type and size in Table A-1. Note down the configuration number(s) assigned to your drives. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for the drives.

2. Find the configuration number for your drives in the CONF NO. column of Table A-2. If more than one number was given for the drives, start with the smallest. Note that for each configuration row, specifications are given for two types of physical drives, Units 0 and 1.

3. When you find the proper row, compare the Physical Drive cylinder, track and sector figures for both Units 0 and 1 in Table A-2 with the numbers you noted down from Table A-1. The track and sector figures must match; the cylinder number from Table A-2 must be smaller than the cylinder number from Table A-1. If those conditions are not met, go on to the next higher configuration number, etc, until you find a match.

4. When you find a match, set the Configuration Switches (SW2) as indicated in Table A-2. (Generally, there is more than one match. In such cases, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuration you like best, and set the Configuration Switches accordingly.)

5. Set the switches on the drive that determine the number of hard sectors per track according to the sector figure from Table A-1. Also assign each drive a unique drive number of 0 or 1 using an ID plug or switches on the drive. See

the installation manual provided by the drive manufacturer for instructions.

A.2.3 Multiple Drive Installations (different drive types)

To find the configuration settings that are suitable for your multiple disk drive installation (different drive size and type), use the following process. Note that all configurations require that the drives both be hard sectored as noted in the Sec column of Table A-1. See the manufacture's drive installation manual for instructions.

1. Locate your drive types and sizes in Table A-1. Note down the configuration code(s) assigned to each drive. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for each drive.

2. Once you have located and noted your drive configuration numbers, compare the numbers for each drive to one another. There must be at least one match if that drive combination is supported.

3. Consult Table A-2. Find the configuration number that both drive types have in common in the CONF NO. column. If there is more than one matched number for the drives, start with the smallest.

4. For each configuration row, specifications are given for two physical drives, Units 0 and 1. The two sets of cylinder, sector and track numbers will be different. Compare the physical cylinder, track and sector numbers for each unit with the corresponding numbers from Table A-1. The physical drive that matches the numbers for physical unit 0 becomes unit 0. The physical drive(s) whose numbers match physical drive number 1's becomes unit one. Not all of the physical cylinders need be used.

5. If there is more than one configuration supported, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuration you like best, and set the Configuration Switches (SW2) accordingly.

6. Set the switches on the drives that determine the number of hard sectors per track according to the sector figures from Table A-1. Set the drive number as discussed in paragraph 4, above. See the installation manual provided by the drive manufacturer for instructions.

TABLE A-1
DRIVES SUPPORTED

Mfg. - Model	Cyl	Trk	Sec	Configuration No.
Amcodyne 7110	644	4	32	13, 13
BASF 6172	614	3	23	4, 4A
BASF 6173	614	5	23	4, 4B, 11*, 11B*
CDC 9410	596	5	22	15, 15A, 15B
CDC 9455	206	4	32	6*, 6A, 6B*, 7*, 7A, 7B*
CDC 9448-32	823	2	35	5, 5A
CDC 9448-64	823	4	35	5, 5B
Century 2075	644	6	32	14A*, 14B*
FUJITSU 2311	589	4	35	11*, 11A
KENNEDY 7300	411	5	35	0, 0B
PRIAM 2050	525	3	23	3*, 3A, 3B*
PRIAM 3350	561	3	32	0, 0A
PRIAM 3350	561	3	35	1*, 1A, 1B*
PRIAM 3450	525	5	23	2*, 2A, 2B*
SLI 3100-2	656	3	20	12*, 12A, 12B*
SLI 3100-3	656	5	20	10, 10A
SLI 3100-4	656	7	20	10, 10B

*These configurations are non standard drive sizes; i.e., an RL01 with more or less than the standard 256 cylinders. Emulex will not supply diagnostic or operating system patches to support non-standard RL emulations. The number of cylinders that the affected non-standard logical has is given in parenthesis in Table A-2.

TABLE A-2
DRIVE CONFIGURATIONS

CONF	SW2-									Physical				Logical	
NO.	10	9	6	5	4	3	2	1	Unit	Cyl	Trk	Sec	Unit(s) = Dr Type	Rev
0	0	0	0	0	0	0	0	0	0	534	3	32	0,1 = RL02 2 = RL01	A
									1	118	5	35	3 = RL02	A
0A	0	C	0	0	0	0	0	0	0	534	3	32	0,1 = RL02 2 = RL01	A
									1	214	3	32	3 = RL02	A
0B	C	C	0	0	0	0	0	0	0	411	5	35	0-2 = RL02 3 = RL01	A
1	0	0	0	0	0	0	0	C	0	489	3	35	0,1 = RL02 2 = RL01	A
									1	196	3	35	3 = RL02	A
1A	0	C	0	0	0	0	0	C	0	489	3	35	0,1 = RL02 2 = RL01	A
									1	196	3	35	3 = RL02	A
1B	C	C	0	0	0	0	0	C	0	561	3	35	0,1 = RL02 2 = RL01(448)	A
									1	196	3	35	3 = RL02	A
2	0	0	0	0	0	0	C	0	0	446	5	23	0,1 = RL02 2 = RL01	A
									1	179	5	23	3 = RL02	A

TABLE A-2, cont.

CONF NO.	SW2- 10	9	6	5	4	3	2	1	Physical Unit	Cyl	Trk	Sec	Logical Unit(s) = Dr Type	Rev
2A	0	C	0	0	0	0	C	0	0	446	5	23	0,1 = RL02 2 = RL01	A
									1	446	2	23	3 = RL02	A
2B	C	C	0	0	0	0	C	0	0	524	5	23	0,1 = RL02 2 = RL01(480)	A
									1	179	5	23	3 = RL02	A
3	0	0	0	0	0	0	C	C	0	446	3	23	0 = RL02 1 = RL01	A
									1	525	3	23	2 = RL02 3 = RL01(392)	A
3A	0	C	0	0	0	0	C	C	0	446	3	23	0 = RL02 1 = RL01	A
									1	446	3	23	2 = RL02 3 = RL01	A
3B	C	C	0	0	0	0	C	C	0	525	3	23	0 = RL02 1 = RL01(392)	A
									1	525	3	23	2 = RL02 3 = RL01(392)	A
4	0	0	0	0	0	C	0	0	0	594	3	23	0,1 = RL02	A
									1	357	5	23	2,3 = RL02	A
4A	0	C	0	0	0	C	0	0	0	594	3	23	0,1 = RL02	A
									1	594	3	23	2,3 = RL02	A
4B	C	C	0	0	0	C	0	0	0	535	5	23	0-2 = RL02	A
									1	179	5	23	3 = RL02	A
5	0	0	0	0	0	C	0	C	0	586	2	35	0,1 = RL02	A
									1	586	2	35	2,3 = RL02	A
5A	0	C	0	0	0	C	0	C	0	586	2	35	0,1 = RL02	A
									1	586	2	35	2,3 = RL02	A
5B	C	C	0	0	0	C	0	C	0	586	4	35	0-3 = RL02	A
6	0	0	0	0	0	C	C	0	0	160	4	32	0,1 = RL01	A
									1	205	4	32	2,3 = RL01(328)	A
6A	0	C	0	0	0	C	C	0	0	160	4	32	0,1 = RL01	A
									1	160	4	32	2,3 = RL01	A
6B	C	C	0	0	0	C	C	0	0	205	4	32	0,1 = RL01(328)	A
									1	205	4	32	2,3 = RL01(328)	A
7	0	0	0	0	0	C	C	C	0	160	4	32	1,0 = RL01	A
									1	205	4	32	3,2 = RL01	A
7A	0	C	0	0	0	C	C	C	0	160	4	32	1,0 = RL01	A
									1	160	4	32	3,2 = RL01	A
7B	C	C	0	0	0	C	C	C	0	205	4	32	1,0 = RL01(328)	A
									1	205	4	32	3,2 = RL01(328)	A
10	0	0	0	0	C	0	0	0	0	615	5	20	0-2 = RL02	A
									1	147	7	20	3 = RL02	A
10A	0	C	0	0	C	0	0	0	0	615	5	20	0-2 = RL02	A
									1	205	5	20	3 = RL02	A
10B	C	C	0	0	C	0	0	0	0	586	7	20	0-3 = RL02	A
11	0	0	0	0	C	0	0	C	0	586	4	35	0-3 = RL02	A
11A	0	C	0	0	C	0	0	C	0	586	4	35	0-3 = RL02	A
11B	C	C	0	0	C	0	0	C	0	613	5	23	0,1 = RL02 2,3 = RL01(368)	A
12	0	0	0	0	C	0	C	0	0	512	3	20	0 = RL02 1 = RL01	A
									1	656	3	20	2 = RL02 3 = RL01(472)	A

TABLE A-2, cont.

CONF NO.	SW2- 10	9	6	5	4	3	2	1	Physical Unit	Cyl	Trk	Sec	Logical Unit(s) = Dr Type	Rev
12A	0	C	0	0	C	0	C	0	0	512	3	20	0 = RL02 1 = RL01	A
									1	512	3	20	2 = RL02 3 = RL01	A
12B	C	C	0	0	C	0	C	0	0	656	3	20	0 = RL02 1 = RL01(472)	A
									1	656	3	20	2 = RL02 3 = RL01(472)	A
13	O	O	O	O	C	O	C	C	0	644	4	32	0-3 = RL02	B
13A	O	C	O	O	C	O	C	C	0	644	4	32	0-3 = RL02	B
13B	C	C	O	O	C	O	C	C	(Do not select)					B
14	O	O	O	O	C	C	O	O	(Do not select)					
14A	O	C	O	O	C	C	O	O	0	644	6	32	0-3 = RL02 (1024)	C
14B	C	C	O	O	C	C	O	O	(Do not select)					
15	O	O	O	O	C	C	O	C	0	596	5	22	0-3 = RL02	C
									1	187	5	22	3 = RL02	C
15A	O	C	O	O	C	C	O	C	0	596	5	22	0-3 = RL02	C
									1	187	5	22	3 = RL02	C
15B	C	C	O	O	C	C	O	C	0	596	5	22	0-3 = RL02	C
									1	187	5	22	3 = RL02	C

A.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC02/L can be user selected. The functions of the switches that select those options are defined in Tables A-3, A-4 and A-5, below.

TABLE A-3
OPTION SWITCH SETTINGS

Option Sw	Open	Closed	Function
SW1-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW1-2			Not used[1]
SW1-3	Disable	Enable	Enhanced Features (impld seek, spiral read/write, etc.)
SW1-4	Disable	Enable	Drives to be write-locked on power-up

[1]All unused switches MUST BE OFF.

TABLE A-4
CONFIGURATION SWITCH SETTINGS

Config Sw	Open	Closed	Function
SW2-1			Drive Configuration[2]
SW2-2			Drive Configuration[2]
SW2-3			Drive Configuration[2]
SW2-4			Drive Configuration[2]
SW2-5			Drive Configuration[2]
SW2-6			Drive Configuration[2]
SW2-7	18 bits	22 bits	Address Mode (RLV12 mode when ON)
SW2-8	3:1	2:1	Sector Interleave
SW2-9			Drive Configuration[2]
SW2-10			Drive Configuration[2]

[1]All unused switches MUST BE OFF.
[2]See Table A-2 for settings.

TABLE A-5
ADDRESS SWITCH SETTINGS

Address Sw	Open	Closed	Function
SW3-1	160	214	Interrupt Vector
SW3-2		777340	Alternate Q-Bus Address[3]
SW3-3		774400	Standard Q-Bus Address[3]
SW3-4	Disable	Enable	Boot PROM Option
SW3-5	Disable	Enable	Line Clock Option
SW3-6	2K	1K	Microcode Address Range (must be open for SC02/L)

[1]All unused switches MUST BE OFF.
[3]Only one address may be selected. All other address switches MUST BE OFF.

BLANK

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