

SC12/A
(RP02/RP03 COMPATIBLE)
DISK CONTROLLER
TECHNICAL MANUAL



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SC12/A DISK CONTROLLER

The following documents make up the documentation package for the SC12/A Disk Controller:

Qty	Part Number	Revision Level	Description
1	SC1251002-00	F	SC12/A Technical Manual
1	PD9951002-00	D	PDP-11 Patch Manual



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1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC12/A Disk Controller. In addition, this manual provides diagnostics and application information.

1.2 OVERVIEW

1.2.1 General Description

The SC12/A Disk Controller is a one board embedded controller for PDP-11 computers manufactured by Digital Equipment Corporation (DEC). This controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC12/A controller emulates the RP11E disk controller manufactured by Digital Equipment Corporation for use with RP02 and RP03 disk drives.

1.2.2 SC12/A Emulation of RP02 and RP03

The RP11E provides a convenient controller architecture for a wide variety of modern technology type disks. It is supported by all DEC operating systems and is easy to program.

The SC12/A controller can handle two disk drives of the same or different capacities. The controller configures each drive from the information in a configuration PROM. This technique permits up to 64 different switch selectable combinations of disk drive configurations on the two controller ports.

1.3 FEATURES

1.3.1 Microprocessor Design

The SC12/A design incorporates a unique eight-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various capacities.

1.3.2 Packaging

The SC12/A is constructed on a single, quad-size, multi-layer printed circuit board assembly (PCBA) which plugs directly into the central processing unit (CPU) chassis or an expansion chassis. No cabling is required between the computer and the disk controller. The controller obtains its power from the chassis in which it is mounted.

1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the LED on and the controller cannot be addressed from the CPU.

1.3.4 Buffering

The controller contains a 1K x 8 high-speed random access memory (RAM) buffer. It is used to store the device registers of the controller plus a full 512 byte data sector. This buffering permits multiple sector reads with a 3-to-1 sector interlace format. Buffer operations eliminate the possibility of a data late condition and permit the controller to be operated at low bus priorities.

1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits in length and detecting bursts of longer length. The controller determines the location of the error and uses the ECC pattern to correct the error before the data is transferred to memory. See paragraph 2.5.4.

1.3.6 Option and Configuration Switches

DIP switches are used to configure the controller for various disk sizes, Unibus addresses and options. It is possible to select one of 64 possible combinations of disk characteristics for the two drives which can be handled by the controller, including mixtures of disk sizes.

1.3.7 Dual Port Capability

The SC12/A controller does not support programmable dual port capability. Those disk drives that have dual port hardware may be used in a dual port configuration if the port select switch is in the Channel I only or Channel II only position. The middle (programmable) position creates errors if two controllers access the drive at the same time.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Media Compatibility

In all cases, the headers written on the drives are not standard RP02/RP03 headers. In addition, a 3-to-1 sector interleave is generated by the hardware formatter. Packs may be formatted using the hardware formatting capability of the standard command set. Disk packs formatted with an SC12/A controller are media compatible with Emulex SC02/A controllers but not with DEC RP02/RP03 packs or Emulex SC11/A or SC01/A packs.

1.4.2 Disk Mapping

Depending upon the type and size of the disk drive, one to eight logical units may be mapped on it. Various mapping organizations are used; most of which do not leave direct 1:1 correlation between the logical and physical addresses.

1.4.3 Diagnostics

Emulex Corporation provides a diagnostic set that is specifically designed to test the SC12/A controller. The Emulex part number is PX9960302. It is recommended that the Emulex diagnostics be used rather than the DEC RP02/RP03 diagnostics to format the disk media. The interleaved format produced by the Emulex diagnostics is more efficient than DEC's standard format with the Emulex hardware.

1.4.4 Operating Systems

When emulating standard size RP02/RP03 disk subsystems the SC12/A is compatible with all DEC operating systems, and no modifications to the operating systems are required. When a non-standard capacity RP02/RP03 is emulated, the disk driver's maximum block count must be patched to reflect the different capacity.

Table 1-1
 RP11E/RP02/RP03 Disk Subsystem Characteristics

	Specifications	
Characteristics	RP02	RP03
Platters/Drive	11	11
MBytes/Logical Unit	20.8	41.6
Blocks/Drive	40,600	81,200
Tracks/Cylinder	2	2
Cylinders/Drive	203	406
Sectors/Track	10	10
Data Bytes/Sector	512	512
Drives/Controller, Max	8	8
Speed,RPM	2400	2400
Bit Density, (BPI)	2020	2020
Data Rate, (KBYTES/SEC)	204.8	204.8

Table 1-2
General Specification

Functional

Emulation	DEC RP02 and RP03
Media Format	3-to-1 sector interlace
Drive Interface	SMD
Drive Ports	2
Error Control	32-bit ECC for data and 32-bit CRC for headers. Correction of single data error burst of up to 11 bits.
Sector Size	256 words (512 bytes)
Sectors/Track	Selectable for each physical drive
Tracks/Cylinder	Selectable for each physical drive
Cylinders/Drive	Selectable for each physical drive
Drive Type	Selectable RP02 or RP03 for each physical drive
Computer Interface	Unibus
Vector Address	
Standard	254
Optional	150,370,374
Priority Level	Level 5
Data Buffering	1 Sector (256 words)
Data Transfer	High speed DMA operation
Self-Test	Extensive internal self-test on powering up

Table 1-2 (Cont.)
General Specification

Functional

Indicator	Fault/Activity LED
Unibus Addresses	Standard: 776700-776736 Alternate: 777440-776476
Design	High-speed bipolar microprocessor using 2901 bit-slice components

Physical

Packaging	One quad-sized board
Mounting	Any SPC slot in CPU or expansion box
Connectors	One 60-pin A Cable flat connector and two 26-pin B Cable connectors. (Flat cable type.)

Electrical

Unibus Interface	DEC approved line drivers and receivers
Drive Interface	Differential line drivers and receivers. A Cable cumulative length to 35 feet. B Cable length to 25 feet.
Power	+5V, 5%, 5 Amp. max.

2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC12/A controller is shown in Figure 2-1. The controller is organized around an eight-bit high-speed bipolar microprocessor. The arithmetic and logic unit (ALU) and register file portion of the microprocessor are implemented with two 2901 bit-slice components. The microinstruction is 48 bits in length and the control memory of 1K words is implemented with twelve 1K x 4 PROMs.

The controller incorporates a 1K x 8 high-speed RAM buffer which is used to store the controller's device registers and one sector (512 bytes) of data buffering.

The A Cable Register (ACR) provides the storage of all A cable signals going to the disk drives. The inputs from the selected drive are testable by the microprocessor.

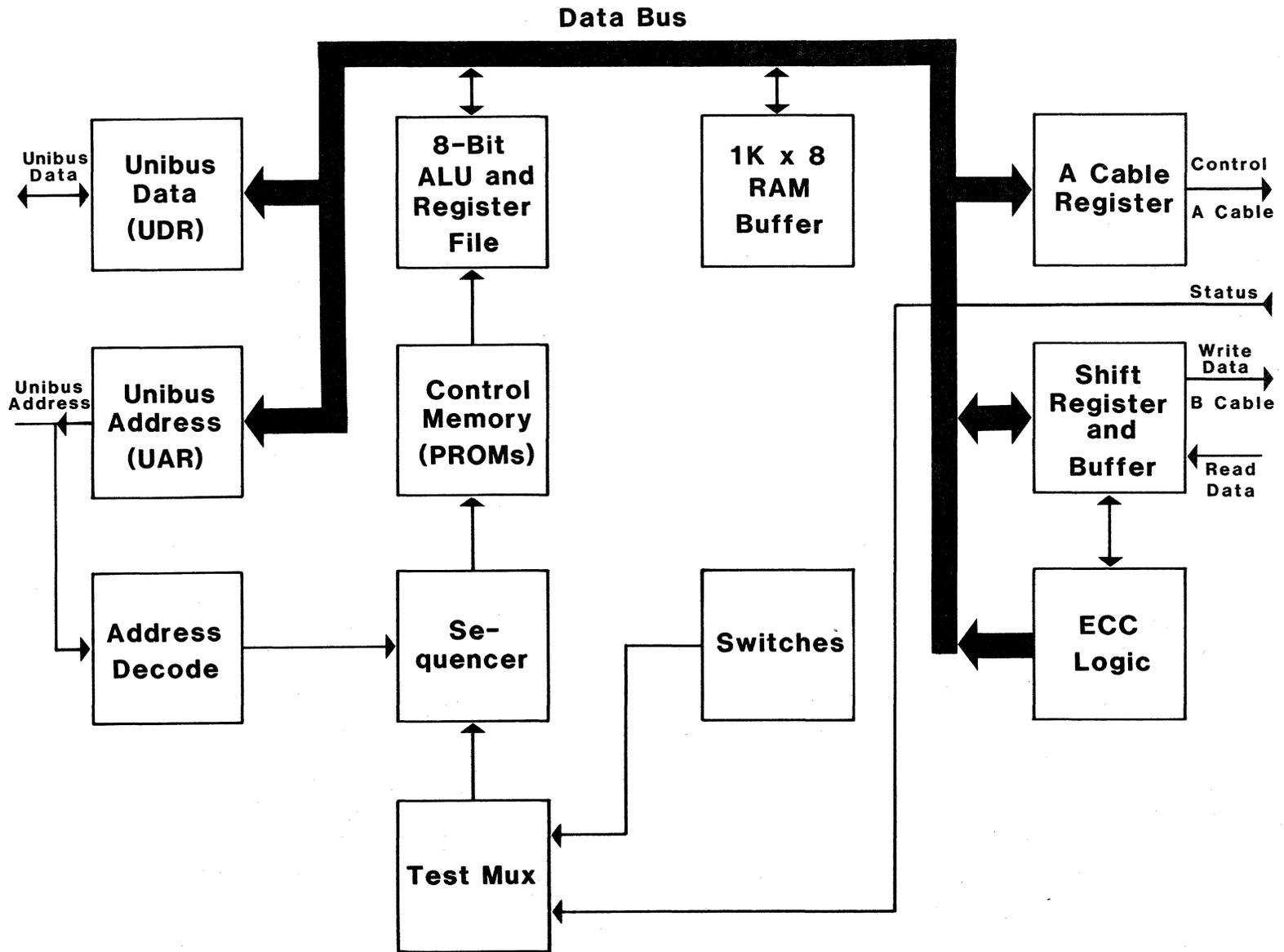
Serial data from the drive is converted into eight-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data access from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 32-bit CRC mode for the headers. The actual ECC polynomial operation is done independent of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

The Unibus interface consists of 18 address lines and 16 bi-directional data lines. The Unibus also carries interrupt vector address data, data control signals, and control signals for granting and receiving bus mastership. The Unibus interface is used for programmed input/output (I/O), CPU interrupts, and Data Transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all direct memory access (DMA) operations and transfers data between the Unibus data lines and the buffer.

2.2 PHYSICAL DESCRIPTION

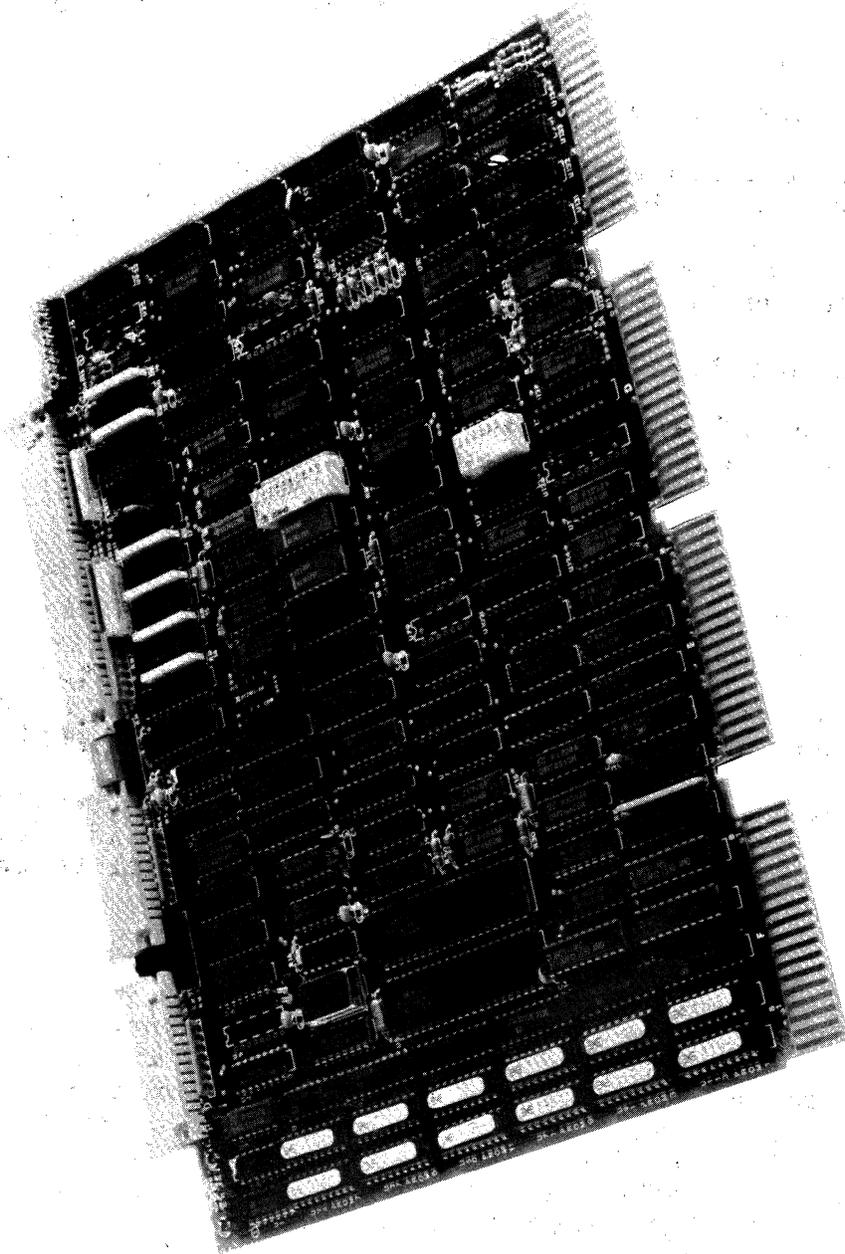
The SC12/A controller consists of a single quad-size board which plugs directly into a PDP-11 chassis.

The controller board is shown in Figure 2-2.



SC1202-0031

Figure 2-1 SC12 Block Diagram



SC1202-0032

Figure 2-2 SC12 Controller Board

2.2.1 Connectors

2.2.1.1 A Cable Connector

The 60-pin flat cable connector labeled J3 at the top edge of the board is for the A Cable which daisy-chains to all the drives for control and status. Pin 1 is located on the left side of the connector.

2.2.1.2 B Cable Connector

The two 26-pin flat cable connectors labeled J1 and J2 are for the radial B Cables to each of two physical drives which may be attached to the controller. Pin 1 is located on the left side of the connector. The two B Cable ports are both identical and any drive may be plugged into either connector.

2.2.1.3 Test Connectors

Connectors J4 and J5 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2 Switches

There are three sets of switches labeled SW1-SW3. SW1 is a four pole DIP 'piano-type' switch accessible from the PC board edge. Locating SW1 such that it is accessible to the operator while the controller is imbedded in a PDP type chassis, makes the selection of common options such as hardware format simpler to perform.

The other two sets of switches, SW2 and SW3 provide controller address decoding selection, option selection and drive configuration selection. (See Appendix A for a complete description of the switch functions.)

2.2.3 LED Indicator

There is an LED indicator mounted between the connectors at the top of the board. The controller executes an extensive self-test when powering up. The microprogrammed organization of the controller permits most logic other than the interface circuitry to the disk to be validated before the controller becomes ready. The LED is turned on as the controller starts its self-test and is turned off only when the controller successfully completes the test. If a malfunction is detected by the built-in diagnostics, the LED remains on and the controller will not respond to program I/O. The LED blinks at approximately a one second rate if the self-test is successful but no drive is seen on-line. The LED also functions as an activity indicator during read and write operations.

2.2.4 Firmware PROMs

There are twelve PROM sockets, used for the control memory, located along the left edge of the board. The sockets are labeled PROM 0 through PROM 11 in a discontinuous physical order. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket.

2.3 INTERFACES

2.3.1 Disk Interface

The controllers' disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatible with these drives electrically and in timing.

The following defines the electrical interface and the recommended cables.

2.3.1.1 A Cable

The 60-conductor A Cable is daisy-chained to both drives and terminated at the last drive. The signals in this cable, along with their function when the control tag (Tag 3) is asserted, are listed in Table 2-1. The A Cable should be 30 twisted pair flat cable with an impedance of 100 ohms and a cumulative length of no greater than 35 feet.

Spectra-Strip P/N 455-248-60 flat cable or its equivalent is recommended. It is possible to order A-Cable assemblies from Emulex that are made up in one of three lengths:

EMULEX P/N	LENGTH (FT.)
SU1111201	8.0
SU1111203	15.0
SU1111205	25.0
SU1111207	35.0

2.3.1.2 B Cable

The 26-conductor B Cable is radial to both drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-1. The B Cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 25 feet.

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	Not Used		From
21,51	Busy (dual port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,19	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	Not Used		From
22,9	Unit Selected		From
12,24	Not Used		From
13,26	Not Used		From

Table 2-2
SPC Unibus Connections

Column	C		D		E		F	
Pin	1	2	1	2	1	2	1	2
A	NPGIN	+5V		+5V		+5V		+5V
B	NPGOUT					-15V		-15V
C	PA	GND		GND	A12	GND		GND
D		D15		BR7	A17	A15	BBSY	
E		D14		BR6	MSYN	A16		
F		D13		BR5	A02	C1		
H	D11	D12		BR4	A01	A00		
J		D10			SSYN	C0	NPR	
K		D09		BG7IN	A14	A13		
L		D08	INIT	BG7OUT	A11			
M		D07		BG6IN			INTR	
N	DCLQ	D04		BG6OUT		A08		
P		D05		BG5IN	A10	A07		
R		D01		BG5OUT	A09			
S	PB	D00		BG4IN				
T	GND	D03	GND	BG4OUT	GND		GND	SACK
U		D02			A06	A04		
V	ACLO	D06			A05	A03		

3M-P/N 3476/26 flat cable or its equivalent is recommended. It is possible to order B-Cable assemblies from Emulex that are made up in one of four lengths:

EMULEX P/N	LENGTH (FT.)
SU1111202	8.0
SU1111204	15.0
SU1111206	25.0

2.3.2 Unibus Interface

The controller interfaces to the PDP-11 or VAX-11 Unibus via a Small Peripheral Controller (SPC) connector. The Unibus consists of 18 address lines and 16 bi-directional data lines, plus control signals for data and interrupt vector address transfer and for becoming bus master. The signal connections of the controller to the Unibus are shown in Table 2-2.

2.3.2.1 BR (Interrupt) Priority Level

The controller is hardwired for BR5. The other three Bus Grant signals are jumpered through.

2.3.2.2 Register Address

The register address and the number of registers assigned to the controller are decoded by a PROM at U127. The selections available are determined by configuration switch SW3 as discussed in Appendix A.

2.3.2.3 DCLO and INIT Signals

The DCLO and INIT signals both perform a controller clear. The self-test is performed only if DCLO has been asserted.

2.4 DISK FORMAT

2.4.1 Disk Organization

The formatting of a disk and the mapping of one or more logical drives onto a physical drive varies with the drive size. Some of this information is supplied directly from the configuration PROM. The rest is computed based upon configuration PROM information. In all cases, the headers actually written on the drives are not standard RP02/RP03 headers. In addition, a 3-to-1 sector interleave is generated by the hardware formatter. Disk packs formatted with an SC12/A controller are media compatible with Emulex SC02/A controllers but not with DEC RP02/RP03 packs or Emulex SC11/A and SC01/A packs.

2.4.2 Mapping

Depending upon the type and size of the disk drive, one to eight logical units may be mapped onto it. The controller can handle a maximum of eight logical units distributed across a maximum of two physical disk drives. Some drives are mapped by cylinders, i.e., "X" number of physical cylinders equals one logical unit. Some drives are mapped by tracks, i.e., "X" number of physical tracks equals one logical unit ("X" can be one, as would be the case with a CMD). The number of physical sectors per physical track is determined by the following three requirements:

1. A minimum of 570 bytes/sector is required.
2. There can be no sectors of less than 570 bytes unless the sector pulse for the "runt" sector can be suppressed in the drive or the configuration PROM notifies the firmware of the presence of the runt sector.
3. Removable media drives require a 574 bytes/sector minimum. For a typical SMD or CMD drive with 20160 bytes/track, 576 bytes/sector gives 35 sectors/track, all of equal size.

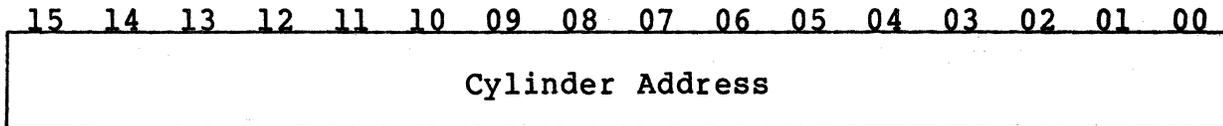
2.4.3 Sector Format

Each sector contains a detached two-word header and a 256 word data field. The header field is terminated with a 32-bit CRC and the data field is terminated with a 32-bit ECC. The controller attempts corrections only on the data field, never on the header. Each field is preceded by at least 11 bytes of zeros and an 8-bit SYNC byte.

In detail, each sector is organized as follows:

4+	Sector pulse postamble zero bytes (varies by drive type)
13	Header preamble zero bytes
1	Sync byte
4	Header bytes
4	Header CRC bytes
2	Header postamble zero bytes
13	Data field preamble zero bytes
1	Sync byte
512	Data bytes
4	Data ECC bytes
2	Data postamble zero bytes
10+	Recovery area (varies by drive type and number of sectors/tracks)
570+	Total Bytes

Header Word 1:



Header Word 2:

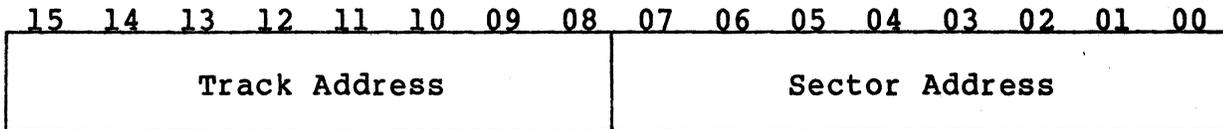


Figure 2-3 Header Format

2.4.3.1 Header Field

The header preamble is used to synchronize the Phase Locked Oscillator (PLO) in the drive to the data on the pack. The SYNC byte is used by the controller to synchronize to the data bytes and their boundaries, and by the drive to synchronize to the phase of the data stream. The two header data words are organized as follows:

Word #1 - Logical cylinder address, right justified.

Word #2 - Logical track and sector addresses, right justified; sector in low byte, track in high byte.

Neither the two data words nor the two CRC words for the header are available to the user (see Read Header command, paragraph 5.9). The header format is the same as the format followed by the cylinder address (RPCA) and disk address (RPDA) registers.

2.4.3.2 Data Field

The data field preamble and SYNC bytes have the same functions as the header preamble and SYNC bytes. The data field itself is always 256 words long. Any unused portion of the sector will be terminated with zero bytes during a write operation. The 32-bit ECC is generated during a write, and is used during a read to check the validity of the data. Any single error burst anywhere in the data field of 11 bits or less can be corrected. Correction is transparent, and is done before the data is sent to memory.

2.4.3.3 Postambles

The postambles provide areas for turning off the write amplifiers, for turning on read amplifiers, and for switching from read-to-write. Write splices will exist within all of these areas.

The sector pulse postamble will also include a head-scatter area on removable media drives.

2.4.3.4 Recovery Area

The recovery area is used for housekeeping operations during a format. A minimum of eight microseconds (ten bytes @ 9.67 MHz data rate) is required.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Clearing the Controller

A RESET is generated when the GO bit in RPCS is set with the function code bits all reset. A Controller RESET can be executed at any time, regardless of the state of the RDY bit in RPCS. No interrupt is generated at the completion of the reset operation.

A RESET clears the following registers:

- All bits in RPER, RPWC, RPBA, RPCA and RPDA.
- RPDS bits <07:00> (ATA bits), and bits <11:09> for every drive.
- RPCS bits <06:00>, <15:08>. The RDY bit (bit 07) is set.

A Bus INIT executes a RESET.

During Data Transfer operations (Read, Write, Write Check, Format), any Write to any controller register results in the execution of a RESET. During those operations the CPU may not write to any controller register while RDY equals zero. The user must either wait for an interrupt to be generated (which can't happen as long as RDY equals zero), or monitor the status of RDY with read-only instructions.

2.5.2 Interrupt Conditions

The controller generates an interrupt in the CPU due to the following conditions:

1. Upon termination of Data Transfer if Interrupt Done Enable (IDE) is set when the controller becomes ready (i.e., if IDE is set when RDY goes from zero to one).
2. Upon assertion of any attention bit while the controller is ready (RDY equals one), and the Attention Interrupt Enable (AIE) is set.
3. Upon termination of the initiate phase of a Seek or Home command if the Interrupt on Done Enable (IDE) is set when the controller becomes ready. This type of interrupt is usually used in overlapped seek drivers to initiate seeks in interrupt mode on two or more units.

4. When the program writes a one into IDE while RDY is set and IDE is reset. Writing a one into IDE when it is already set has no effect.

2.5.3 Termination of Data Transfers

A Data Transfer may terminate in any one of the following ways:

1. Normal Termination - Word count overflows to zero and the controller becomes ready at the end of the current sector.
2. Controller Error - An error occurs during a Data Transfer operation. The controller sets the appropriate error bit(s), terminates the Data Transfer immediately, and makes the controller ready.
3. Drive Error - An error occurs during a Seek or Data Transfer operation. The controller sets the appropriate error bit(s), terminates any Data Transfer that may be in progress, and makes the controller ready.
4. Program-Caused Abort - By performing a Controller Reset operation, the program can cause an abort of any operation. Status and error information are lost when this is done, and the controller becomes ready immediately.

2.5.4 Error Correction

The 32-bit ECC appended to every sector's data field allows the controller to detect read errors of any length, and correct single error bursts of one to 11 bits in length. However, not all read errors are corrected. The controller does not correct initial read errors, but flags the error instead to allow software logging. The next read error encountered after the first will result in a correction attempt. If the correction attempt is successful, then the corrected data is sent to the CPU and the controller continues as if no error existed. The Read Error Flag is also reset so that the next read error is seen as an initial read error. If the correction attempt is unsuccessful, then the error is flagged again. The Read Error Flag remains set so that the next attempted read of the bad sector also results in a correction attempt. INIT and RESET functions do not alter this flag. The user may manually reset the flag by writing (any data) into RPDB. Note that the ECH bit in RPER determines whether a read error correction was not attempted (ECH equals zero) or was unsuccessful (ECH equals one). The Data Check (DCK) bit in RPER will be set in either case. See paragraph 4.3, Error Register. No correction is ever attempted during a Write Check. A Write operation will reset the Read Error Flag.

Section 3 INSTALLATION

This section describes the step-by-step procedure for installation of the SC12/A Disk Controller in a PDP-11 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the SC12/A, is covered in paragraph 3.1).

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Inspect the SC12/A.
2. Prepare the disk drives.
3. Prepare the PDP-11.
4. Route the drive I/O cables.
5. Configure the SC12/A.
6. Install the SC12/A.
7. Run the diagnostics.

3.1 INSPECTION

A visual inspection of the board is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROMs should be examined carefully to insure that they are firmly and completely seated in the sockets.

3.2 DISK DRIVE PREPARATION

3.2.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC12/A. This allows the I/O cable routing and length to be accurately judged. Place the drives side by side to make installation of the daisy-chained A Cable simpler.

3.2.2 Local/Remote

The LOCAL/REMOTE switch controls whether the drive can be powered up from the drive (local) or the controller (remote). Place the switch in the REMOTE position. With the PDP-11 powered down, press the START switch on the front panel of each of the drives (the START LED will light, but the drive will not spin up and become

ready). When the PDP-11 is powered up, the drives will spin up sequentially. This prevents the heavy current draw that would be caused if all of the drives were powered up at once. When in the remote mode the drives will power down when the PDP-11 is powered down. While the PDP-11 is powered on, the drives may be powered up and down individually (to change disk media, for example) using the drive START switch.

3.2.3 Sectoring

See Appendix A, Configuration Selection, for the correct sector count settings for the disk drives in use. Because the procedure for entering the sector numbers differs from drive to drive, consult the drive manufacturer's installation manual for instructions.

3.2.4 Drive Numbering

A drive number of zero or one is assigned according to the configuration selected for the subsystem. Appendix A, Table A-2 defines the physical drive to drive (unit) number relationship. In any case, make sure that no two drives are assigned the same number.

Refer to the manual provided by the drive's manufacturer for instructions on selecting a number for your particular drive.

3.3 SYSTEM PREPARATION

3.3.1 Powering Down the System

Power down the system and switch OFF the main AC breaker at the rear of the cabinet (the AC power light will remain lit). Slide the CPU rack out of the cabinet and remove the card rack cover. Open the rear door of the cabinet.

3.4 CONTROLLER SETUP

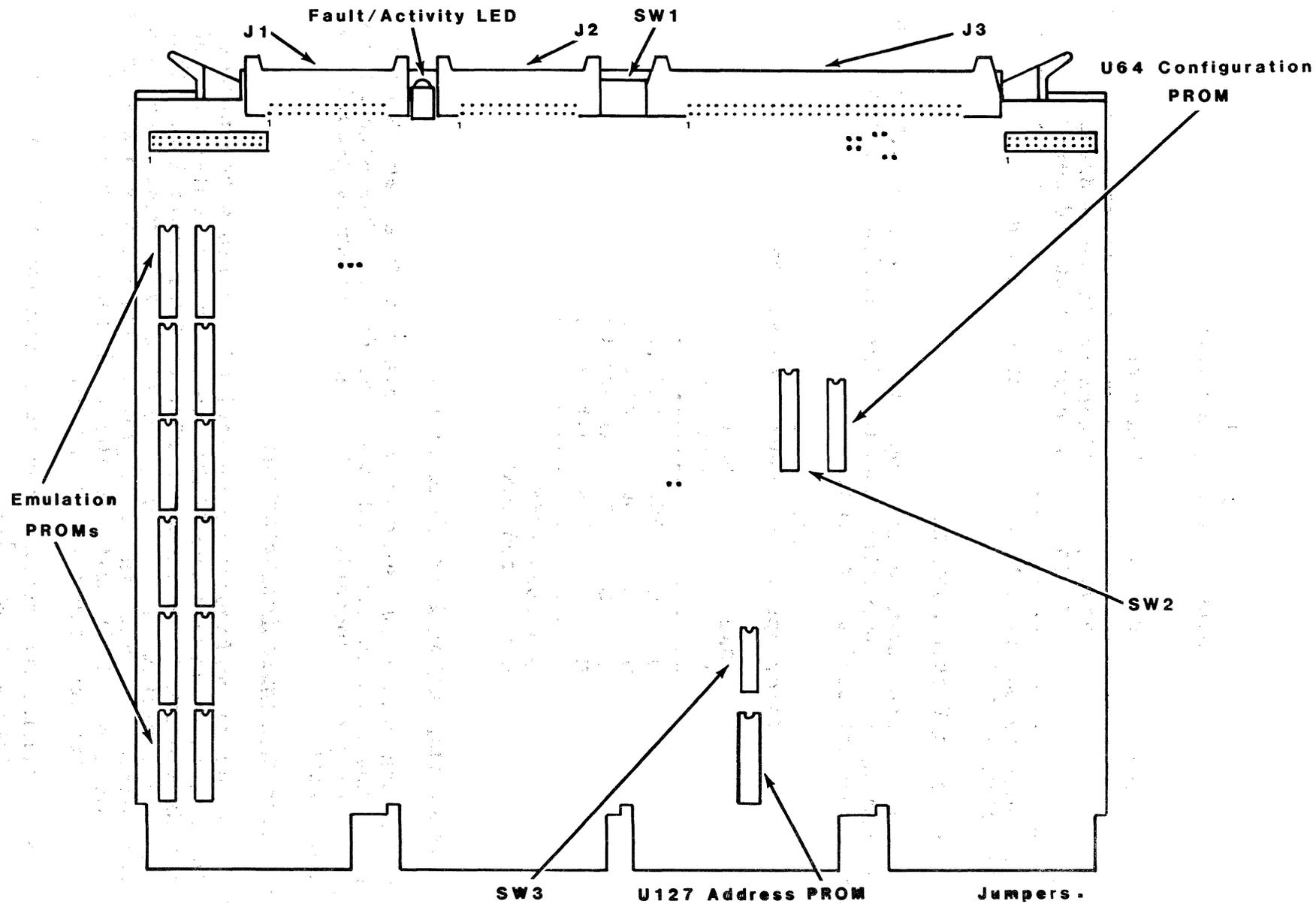
Several configuration setups must be made on the controller before inserting it into the chassis. These are made by SW1 and SW2.

Figure 3-1 shows an assembly diagram of the controller.

3.4.1 Controller Address Selection

All Unibus controllers have a block of several command and status registers through which the system can command and monitor the controller. The registers are addressed sequentially from a starting address assigned to that device type, in this case a disk controller.

The starting address for the controller's Unibus registers is selected by DIP switch SW3.



SC1202-0033

Figure 3-1 SC12 Controller Assembly

Table 3-1
Unibus Starting Addresses

Addr Sw	Open	Closed	Function
SW3-2		777440	Alternate Unibus Address ³
SW3-3		776700	Standard Unibus Address ³

³Only one address may be selected. All other address switches MUST BE OFF.

3.4.2 Interrupt Vector Address

The interrupt vector address is programmed by means of DIP switch SW2 located on the controller board. The available vector addresses are selected as follows.

Table 3-2
Interrupt Vector Address Selection

SW2-		Vector Address	
10	9		
O	O	254	Standard
O	C	150	Alternate
C	O	370	Alternate
C	C	374	Alternate

O = Open (OFF)
C = Closed (ON)

3.4.3 Index and Sector Pulse Selection

The SC12/A controller is designed to have the Index and Sector signals on the A Cable from each physical drive. The signals are necessary for proper operation of the sector counters associated with each drive.

3.4.4 Drive Configuration Selection

The phrase "drive configuration selection" describes the process that is used to configure the SC12/A to use a particular type of physical disk drive to perform the RP02 or RP03 emulation. That is, you have a particular set of physical disk drives. You must tell the controller what kind of physical disk drive you are going to use. On the SC12/A switches SW2-1 through SW2-6 on the controller board are used for that purpose.

For ease of manual maintenance the configuration table for the SC12/A is contained in Appendix A.

3.4.5 Option Switches

There are a number of other SCl2/A options that can be selected by the user. These features are selected using switches SW1 and SW2. See Appendix A for individual switch definitions.

3.4.5.1 Disable Logical to Physical Disk Addressing Mapping

Setting SW2-7 ON disables logical to physical disk address mapping.

The cylinder, track and sector configuration of DEC's RP02/RP03 does not match that of most SMD type drives. Consequently, logical to physical disk address mapping is used to convert the disk addresses generated by the DEC operating system to addresses appropriate to the physical drive.

This option is necessary if the user wishes to write a disk driver that specifies actual physical disk addresses rather than RP02/RP03 type addresses.

The controller will not operate with a DEC RP02/RP03 type disk driver when this option is enabled.

3.5 PHYSICAL INSTALLATION

3.5.1 Slot Selection

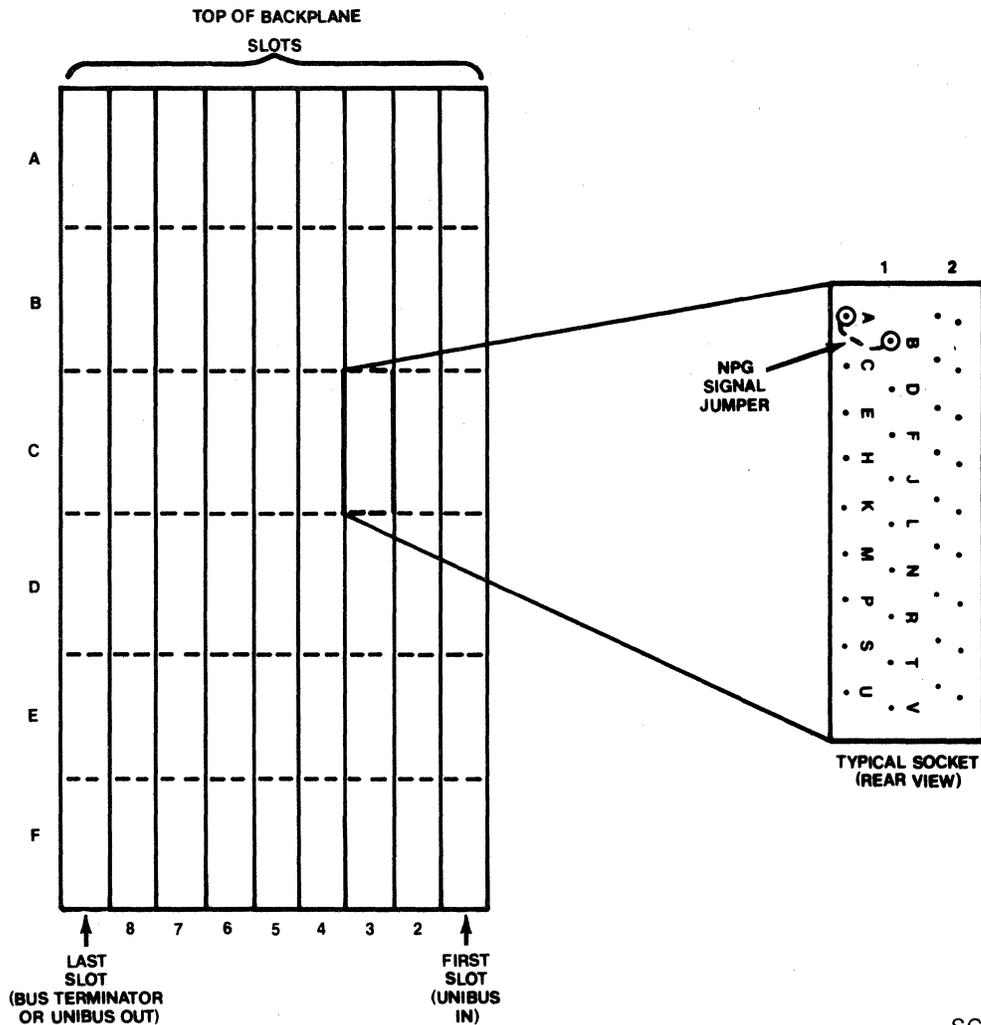
The controller may be placed in any SPC slot along the Unibus without regard to NPR priority. The controller contains adequate buffering to prevent data lates and will automatically get off the bus if any other device is waiting for the Unibus. If the system contains a Unibus repeater, the controller will not give priority to devices which are on the CPU side of the repeater when the controller is on the far side of the repeater. This may require that the controller be placed on the CPU side of the repeater or that all DMA devices be on the far side of the repeater.

3.5.2 NPG Signal Jumper

The NPG signal jumper between pins CA1 and CB1 on the backplane must be removed so that the NPG signal passes through the controller. See Figure 3-2.

3.5.3 Mounting

The controller board should be plugged into the PDP-11 backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the boards with the computer power OFF to avoid possible damage to the circuitry. Be sure that



SC1202-0001

Figure 3-2 NPG Signal Jumper Removal

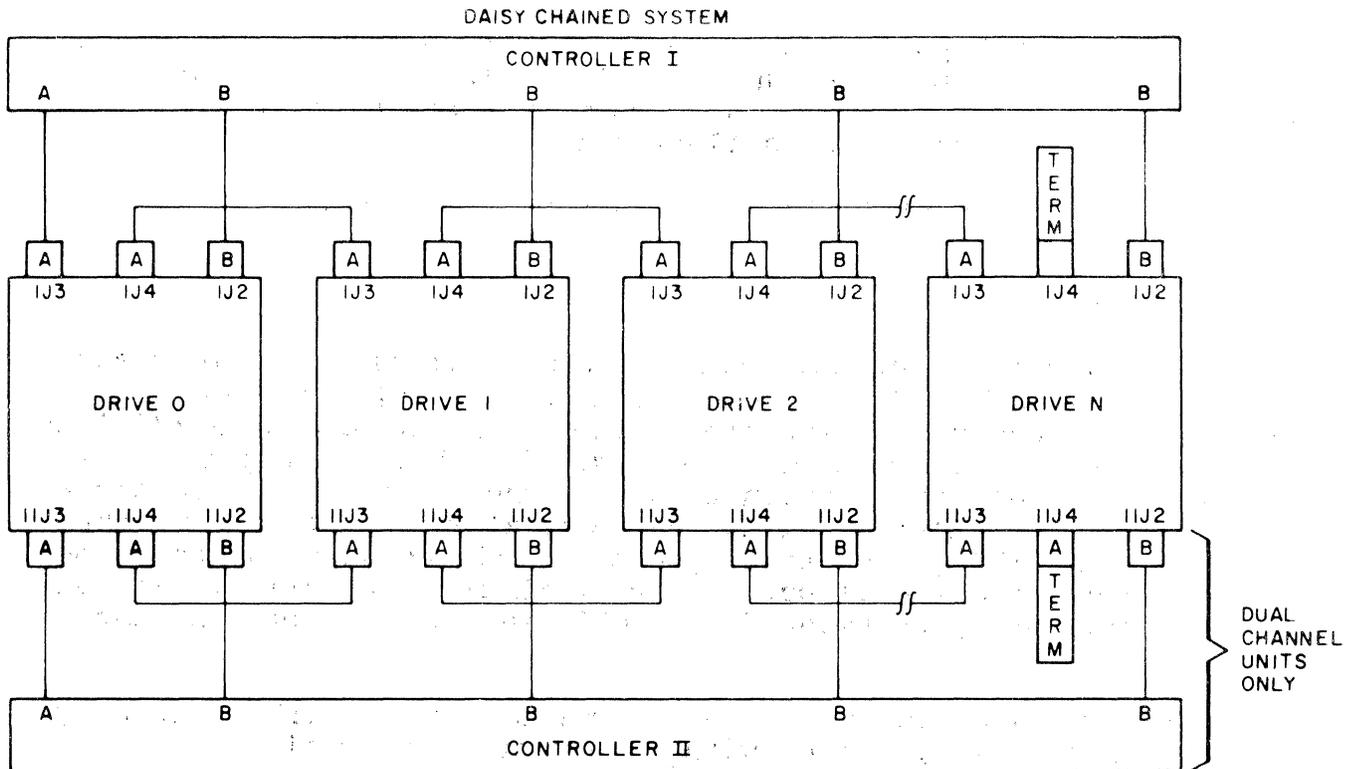
the board is properly positioned in the throat of the connector before attempting to seat the board by means of the extractor handles.

3.6 CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-3.

3.6.1 A Cable

The 60-wire A Cable should be plugged into J3 of the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the second drive.



NOTES:

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET

SC1202-0000

Figure 3-3 Cabling Diagram

The last drive on the A Cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A Cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the left. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cables will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

3.6.2 B Cable

Each drive must have a 26-wire B Cable wired from the drive to one of the B ports of the controller (J1 and J2). It makes no

difference which B port connection is used by a drive. No external terminators are used with the B Cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe.

NOTE: Observe the same caution on connector reversal given in paragraph 3.6.1.

3.6.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.7 TESTING

3.7.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. This self-test is not executed with every bus INIT but only on powering-up. If the self-test has been executed successfully, the Fault LED on the front edge of the controller board will be OFF or flashing. The Fault LED flashes when the controller cannot properly address at least one drive after successfully executing its self-test. This will occur if the A and B cables are not properly plugged in, a drive is not powered-up with a 0-1 code plug, or if the two drives have an identical code plug. If the Fault LED is ON steadily the controller did not pass its self-test and the controller cannot be addressed from the CPU.

3.7.2 Register Examination

After powering up the CPU and noting that the LED indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. The Control Status Register (RPCS) 776714 will contain 000200 if the controller is ready. To determine the on line status of the selected drive check the Device Status Register (RPDS) 776710 (see paragraph 4.2). If the CPU has a console emulator all the registers of the controller should be examined.

3.7.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and zero data in all sectors of the disk. This format does not verify the data or headers.

If the drive is on line, the formatting is carried out as follows:

1. Turn ON the hardware format enable switch SW1-4.*
2. Perform a controller clear by depositing 000001 into the Control Status Register (RPCS 776714).
3. To initiate a format, it is necessary to set the Mode bit (12) and the Header bit (11) to one in the RPCS. In addition, the desired logical drive number must be placed in bits 8, 9 and 10 of the RPCS and the Write function (bits 1, 2 and 3) plus the Go bit (0) must also be deposited in RPCS.

*Format enable can also be done by writing a 177777 into RPSH (776702) before doing Step 3.

LOGICAL DR.	DEPOSIT
0	014003
1	014403
2	015003
3	015403
4	016003
5	016403
6	017003
7	017403

3.7.4 Diagnostics

Emulex Corporation provides a diagnostic set that is specifically designed to test the SC12/A controller. The Emulex part number is PX9960302. It is recommended that the Emulex diagnostics be used rather than the DEC RP02/RP03 diagnostics to format the disk media. The interleaved format produced by the Emulex diagnostics is more efficient than DEC's standard format with the Emulex hardware.

BLANK

Table 4-1 summarizes the Controller's Register Set. A detailed description of each of the registers follows the table. The bus addresses that are listed are the standard addresses. Alternate addresses can be selected.

Table 4-1
Summary of SC12/A Registers

Bus Address	Register
776700	# Sectors Read Counter Low (RPSL)
776702	# Sectors Read Counter High (RPSH)
777704	# Sectors Corrected Counter (RPSC)
776706	# Sectors Uncorrected Counter (RPSU)
776710	Device Status Register (RPDS)
776712	Error Register (RPER)
776714	Control Status Register (RPCS)
776716	Word Count (RPWC)
776720	Bus Address (RPBA)
776722	Cylinder Address (RPCA)
776724	Disk Address (RPDA)
776726	Physical Address 1 (RPA1)
776730	Physical Address 2 (RPA2)
776732	Physical Address 3 (RPA3)
776734	Current Cylinder Address (RPCC)
776736	Data Buffer (RPDB)

4.1 SECTOR READ COUNTERS 776700-776706

- RPSL - 776700: Contains the low order 16 bits of the number-of-sectors-read counter.
- RPSH - 776702: Contains the high order 16 bits of the number-of-sectors-read counter.
- RPSC - 776704: Contains the number of sectors read that were in error and corrected.
- RPSU - 776706: Contains the number of sectors read that were in error and either not corrected or uncorrectable.

All four counters are read-write registers. None are reset by INIT or the RESET function. In addition, if a 17777 is written into RPSH, the write is ignored and a software "format enable" flag is set instead. If the next instruction executed is a Write Header command, the entire disk pack will be formatted. (See paragraph 5.4

for further details.) These registers may be written into with both word and byte operations.

4.2 DEVICE STATUS REGISTER (RPDS) 776710

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OCL	ONL	T3	HNF	SKE	SIP	FLT	WPT	ATA							
								7	6	5	4	3	2	1	0

The Device Status Register (RPDS) holds the current state of the selected drive and the Attention signals from each of the eight logical drives. The Attention bits are read/clear and, as such, can be selectively cleared by writing a one in the desired bit location(s). The other bits of RPDS are read-only. A drive is selected via bits <10:08> of RPCS.

On-Cylinder (OCL) - Bit 15

This bit is set after a successful head load (on cylinder). It is reset during any Seek operation and set again after the Seek is completed if no Seek Error exists.

On-Line (ONL) - Bit 14

The selected drive exists and is up to speed.

RP03 (T3) - Bit 13

This bit is a 1-bit if the selected drive is an RP03. This bit is a 0-bit for RP02 emulations.

Header Not Found (HNF) - Bit 12

The selected drive has completed three full revolutions without locating the addressed sector. This bit is reset at the start of any operation.

Seek Error (SKE) - Bit 11

This bit is set if a Seek Error is detected at the completion of a Seek for the selected unit.

Seek in Progress (SIP) - Bit 10

Set if the selected unit is currently executing a Seek or Home. This bit is reset at the completion of the Seek or Home.

Fault (FLT) - Bit 09

The selected unit has detected a fault condition within the drive and is prohibiting all operations. This bit is reset manually in the drive, and by a Home command (if possible).

Write Protected (WPT) - Bit 08

This bit is set when the Write Protect switch on the selected drive is set.

Attention Active 7-0 (ATA7-ATA0) - Bits <07:00>

Attention is set by a drive when a Seek or Home is completed. OCYL will be set after a successful Seek, and SKE will be set after an incomplete Seek. All Attention bits are cleared by INIT or the RESET function. Implied and mid-transfer Seeks do not set Attention bits.

4.3 ERROR REGISTER (RPER) 776712

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WPV	FUV	NXC	NXT	NXS	PGE	HRE	MER	MPE	ECH	DCK	TME	WCE	NXM	EPE	DKE

The Error Register (RPER) contains all error conditions generated within the controller. RPER is a read-only register. This register is cleared at the writing of the GO bit in RPCS, by INIT or by a RESET function.

Write Protect Violation (WPV) - Bit 15

Disk Write operation was attempted when WPT was true.

File Unsafe Violation (FUV) - Bit 14

Disk operation was attempted when FLT was true.

Non-Existent Cylinder (NXC) - Bit 13

Disk operation was attempted when the contents of the Cylinder Address Register was not within range.

Non-Existent Track (NXT) - Bit 12

Disk operation was attempted when the contents of the Track Address portion of the RPDA Register was not within range.

Non-Existent Sector (NXS) - Bit 11

Disk operation was attempted when the contents of the Sector Address portion of the RPDA Register was not within range.

Program Error (PGE) - Bit 10

A Data Transfer operation was attempted with the contents of RPWC equal to zero; an operation was attempted on an off-line drive or while another instruction was still in progress (RDY equals zero).

Also set if a Write Header command is attempted with the format enable flag/switch OFF.

Header Read Error (HRE) - Bit 09

CRC error was detected in a sector's header.

Mode Error (MER) - Bit 08

A header operation was attempted while the MDE bit in RPCS is reset. Both HDR and MDE must be set.

Memory Parity Error (MPE) - Bit 07

A Parity Error was detected during a DMA read from memory.

ECC Hard Error (ECH) - Bit 06

Used in conjunction with bit 05 to indicate that the data read was not correctable and a correction attempt was made.

Data Check (DCK) - Bit 05

Calculated ECC does not compare with that read from the disk, and either the data was not correctable or no correction was attempted.

Timing Error (TME) - Bit 04

Data field sync character not found or 256 data words not found.

Write Check Error (WCE) - Bit 03

Data read from the disk pack does not compare with data read from memory during a Write Check operation.

Non-Existent Memory (NXM) - Bit 02

More than 10 us was required to complete a DMA operation.

End of Pack Error (EPE) - Bit 01

Data Transfer (read or write) was attempted across the end of the last sector of the pack.

Disk Error (DKE) - Bit 00

OR condition of Header Not Found (HNF) and Seek Error (SKE).

4.4 CONTROL STATUS REGISTER (RPCS) 776714

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	HE	AIE	MDE	HDR	US2	US1	US0	RDY	IDE	A17	A16	F2	F1	F0	GO

Error (ERR) - Bit 15

OR of all errors. This is a read-only bit.

Hard Error (HE) - Bit 14

OR of all errors except data errors. This is a read-only bit.

Attention Interrupt Enable (AIE) - Bit 13

Causes the controller to set an interrupt request whenever any logical unit sets its ATA bit. This bit is cleared at the completion of the interrupt. Also cleared by INIT or RESET function; this is a read/write bit.

Mode (MDE) - Bit 12

Not used except that if bit 11 is set, this bit must also be set for diagnostic compatibility. This is a read/write bit; cleared by INIT or RESET function.

Header (HDR) - Bit 11

The function in the Function Field is a Header operation. This is a read/write bit; cleared by INIT or RESET function.

Unit Select (US2-US0) - Bits <10:08>

Specify the logical drive which is to be the subject of any controller action. These are read/write bits; cleared by INIT or RESET function. Note that the number of units that can be operated upon varies by drive types and number.

Ready (RDY) - Bit 07

When set indicates that the controller is in a condition to accept and execute a new operation.

Interrupt On Done (Error) Enable (IDE) - Bit 06

Causes the controller to raise an interrupt request when a disk operation is complete or if an error occurs. This is a read/write bit; cleared by INIT or RESET function. Not cleared at the completion of an interrupt.

Memory Extended Address (A17, A16) - Bits <05:04>

Specifies the 32K-word bank of memory used during Data Transfers. These are read/write bits; cleared by INIT or RESET function.

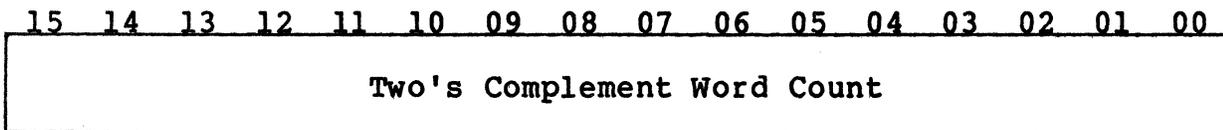
Function Bits (F2-F0) - Bits <03:01>

Specify the operation to be performed. These functions are described in detail in Section 5. These are read/write bits; cleared by INIT or RESET function.

GO (GO) - Bit 00

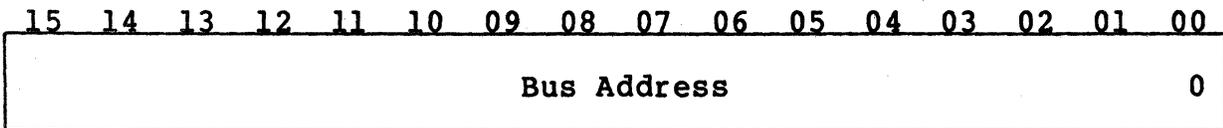
Set from the bus, causes the controller to initiate the operation encoded in bits <03:01> of the RPCS. This write-only bit always reads as a zero.

4.5 WORD COUNT REGISTER (RPWC) 776716



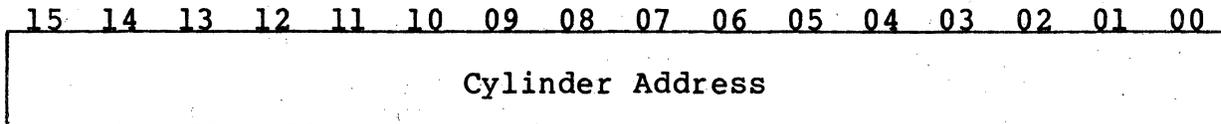
This register holds the two's complement of the number of data words to be transferred. This register is incremented by one after each transfer. Data Transfers are terminated when RPWC increments to zero. RPWC must be non-zero when a Data Transfer is initiated or a Programming Error (PGE) will be generated and no data will be transferred. RPWC can be written into with both word and byte operations.

4.6 BUS ADDRESS REGISTER (RPBA) 776720



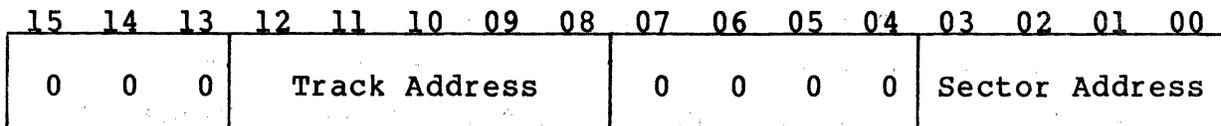
The Bus Address Register (RPBA) is loaded from the bus and specifies the bus address for Data Transfers during Read, Write, or Write Check operations. Transfers are always on a word basis; therefore, RPBA must be an even value. Incrementation by two takes place after a memory transaction has occurred. RPBA, therefore, is loaded with the address of the first location to be read from or written into. RPBA is a read/write register. The register is cleared by INIT or the RESET function. RPBA can be written into with both word and bytes operations.

4.7 CYLINDER ADDRESS REGISTER (RPCA) 776722



Bits <15:00> of the Cylinder Address Register (RPCA) are loaded from the bus and specify the disk cylinder for any disk operation. RPCA is a read/write register. It is cleared by INIT or the RESET function. RPCA can be written into with both word and byte operations.

4.8 DISK ADDRESS REGISTER (RPDA) 776724



If logical-to-physical mapping is in effect, then bits <03:00> of the Disk Address Register (RPDA) are loaded from the bus and specify the disk sector address for any operation other than Seek or Home. Bits <03:00> are read/write bits and are cleared by INIT or the RESET function. Bits <07:04> are read-only bits which are read as zeros. Bits <12:08> are loaded from the bus to specify the track address for any disk operation. Bits <12:08> are read/write bits and are cleared by INIT or the RESET function. Bits <15:13> are read-only bits which are read as zeros.

If logical-to-physical mapping is not in effect, then bits <07:00> specify the sector address and bits <15:08> specify the track address. All bits are read/write bits, and all bits are cleared by INIT or the RESET function.

RPDA can be written into with both word and byte operations.

4.9 PHYSICAL ADDRESSES (RPA1-RPA3) 776726-776732

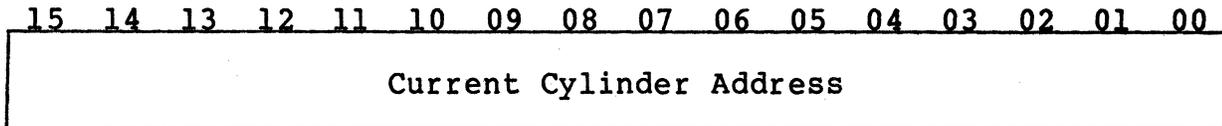
Whenever a seek is executed the physical address is saved in these three registers as follows:

RPA1 - 776726: Contains the physical cylinder number
RPA2 - 776730: Contains the physical track number
RPA3 - 776732: Contains the physical sector number

During multi-sector Data Transfers, RPA3 is incremented once after each sector is transferred. When this register increments past the maximum physical sector number for the drive, RPA2 and RPA1 are updated, RPA3 is cleared to zero, and a mid-transfer seek is executed.

RPA3 is a read-only register. RPA1 and RPA2 are also read-only registers with one qualification: attempting to write into RPA1 (any data) will replace the data currently in RPA1 with the maximum logical cylinder number for the selected unit. Similarly, any write into RPA2 will replace the data currently in RPA2 with the maximum track number (upper byte) and sector number (lower byte). These will be a 19 and a 9 respectively if logical-to-physical mapping is enabled. They will be actual limits per the configuration PROM if logical-to-physical mapping is disabled (in that case, RPA1 would also contain a physical address).

4.10 CURRENT CYLINDER ADDRESS (RPCC) 776734



The Current Cylinder Address (RPCC) register stores the contents of the selected logical unit's current logical cylinder address. This is a Read-Only register.

4.11 DATA BUFFER (RPDB) 776736

This is a read-only register. If a write check error occurs it contains the data word from the disk that caused the error. A write to this register (any data) will reset the read error flag. See paragraph 2.5.4 for error correction details.

Section 5
FUNCTION CODES

The controller provides the hardware for the execution of the eight different functions. Home Seek and Seek are designated initiate functions because their execution requires less than 30 us of controller time after the command is issued. For this period, the controller is busy. Initiate type commands require that the target unit be selected. Although a Seek may require 500 ms. for completion, a new unit number can be loaded into RPCS immediately. Reset requires only ten microseconds of time. Execute instructions, however, use all the time the controller requires for completing the function. The controller, therefore, is busy for the entire operation. Also, the target unit must be selected for the entire operation and cannot be deselected for beginning initiate-type functions.

<u>Function</u>	<u>Code</u>	<u>Type</u>	<u>Code + Go</u>
Reset	0	Initiate	1
Seek	4	Initiate	11
Home Seek	6	Initiate	15
Write	1	Execute	3
Read	2	Execute	5
Write Check	3	Execute	7
Write	5	Execute	13
Read	7	Execute	17

Functions are selected by loading a 3-bit field (F2:F0), of the Controller Status Register (RPCS) with an octal number equal to the function code. The function code and the GO bit may be written at the same time. GO must be set before any action takes place.

5.1 INITIATE FUNCTIONS

5.1.1 Reset (1)

The Reset function is a controller clear operation. This function is entered when the controller is initially cleared, or when the Function field contents equal 0 and the GO bit is set. This operation requires ten microseconds of controller time and no interrupt is generated upon completion. The RESET command can be executed even if the controller is in the NOT READY state. (See section 2.5.1 Clearing the Controller)

5.1.2 Seek (11)

The Seek function can be executed by loading its octal code (4) into the Function field and setting GO. The Seek operation positions the heads of the selected unit as specified by the

contents of the Cylinder Address and Disk Address registers. The unit Attention line, if it had been cleared previously, is raised when the Seek is completed. If the Seek is unsuccessful, the Seek Error status bit is set. At the successful completion of a Seek function, the on-cylinder status bit is set. While the Seek is in progress, the SIP bit (seek in progress) is set.

The Seek function allows the program to preposition the drive heads for the first block of data to be transferred. This prepositioning then results in a zero-cylinder seek (which usually takes less than 100 us) when the implied seek inherent within the Read, Write, and Write-Check functions occur.

On a multi-drive system, it is possible to initiate simultaneous Seek operations on several drives. The first drive to complete the Seek operation and respond by raising the Attention signal will cause an interrupt only if the Attention Interrupt Enable (AIE) bit has been set.

The programmer usually expects to be interrupted at the completion of any Seek operation, and sets the AIE bit accordingly. Because the Attention bits for each of the drives are effectively ORed, when any drive raises the Attention signal, an interrupt is generated. At the completion of the interrupt, the AIE bit is cleared by the controller, thus inhibiting further interrupts during the Data Transfer which normally follows. When the AIE bit is enabled again by the program, any remaining or new Attention bits initiate another interrupt and again clear AIE. In this way, each Attention can be handled individually or they can be handled collectively.

5.1.3 Home Seek (15)

The Home Seek function is executed by loading its function code (6) into the Function field and setting GO. The Home Seek function recovers the head position after a Seek Error. When this function is completed, the heads are placed at cylinder 0 and Unit Attention is set along with on-cylinder. This command does not alter RPCA or RPDA. A Home Seek should never cause a Seek Error. If it does, the drive requires maintenance. A fault clear is also issued to the drive. While the Home is in progress, the SIP bit is set.

5.2 EXECUTE FUNCTIONS

5.2.1 Write (3)

The Write function includes a Seek to the starting disk address (cylinder and track). This function is executed by loading its octal code (1) into the Function field and setting GO. WRITE transfers data from the CPU memory to the disk drive beginning with the memory location specified by the Bus Address Register. Each data word transferred increments the Bus address by 2 and Word Count by 1. The content of the RPWC at the beginning of the transfer determines the number of data words to be transferred.

When the RPWC overflows, Data Transfers cease on the Q Bus and the remainder of the present sector (if any) is filled with zeros. If RPWC is equal to zero when this function is executed, the write is aborted and a programming error (PGE) is indicated.

When this operation is performed, if the Data Transfer is sufficiently large enough to cause the heads to reposition to the next cylinder, the controller executes a mid-transfer Seek before continuing with the operation.

5.2.2 Read (5)

The Read function includes a Seek to the starting disk address (cylinder and track). This function is executed by loading its octal code (2) into the Function field and setting GO. READ transfers data from the disk drive to the CPU beginning with the memory location specified by the Bus Address register. Each data word transferred increments the Bus Address by 2 and Word Count by 1. The content of the RPWC at the beginning of the transfer determines the number of data words to be transferred. When the RPWC overflows, Data Transfers stop. The remainder of the present sector is retrieved and the ECC checked before RDY is set. If RPWC equals zero when this function is executed, the read is aborted and a programming error (PGE) is indicated.

When this operation is performed, if the Data Transfer is sufficiently large enough to cause the heads to reposition to the next cylinder, the controller executes a mid-transfer Seek before continuing with the operation.

5.2.3 Write Check (7)

The Write Check function includes a Seek to the starting disk address (cylinder and track). This function is executed by loading its octal code (3) into the Function Field and setting GO. The WRITE CHECK command is a combination of the Write and Read functions. Data words are transferred from CPU memory to the controller and simultaneously read from the disk drive and transferred to the controller. In the controller, the two words are compared. Discrepancies set the WCE error status bit and terminate the operation. Data remains unchanged both in memory and on the disk. If an error occurs, RPBA points to the memory location that follows the one that caused the error, and the RPDB register contains the disk data that caused the error. RPDA points to the sector that caused the error. If RPWC equals zero when this function is executed, the function is aborted and a programming error (PGE) is indicated.

When this operation is performed, if the Data Transfer is sufficiently large enough to cause the heads to reposition to the next cylinder, the controller executes a mid-transfer Seek before continuing the operation.

5.2.4 Write (13)

This Write function is identical to the other (Function equals one).

5.2.5 Read (17)

This Read function is identical to the other (Function equals two).

5.3 READ HEADER

This is a dummy command that is included for diagnostic compatibility only. Headers are not actually read from the disk, but are created by microcode in RP02/RP03 format. Note that the controller uses a different, more efficient, format for the disk headers. An RP02/RP03 header consists of three words with the following format:

Word #1 = All zeros

Word #2 = Cylinder address in bits <15:06>, track address in bits <05:01>, and a zero in bit 00.

Word #3 = Sector address in bits <03:00>.

Note that in an unmapped system with track addresses of six bits or more, the track address overflows into the cylinder address. Nothing is done to prevent this. If the contents of RPWC indicates more than 255 words are to be read by this function, then the read is aborted and a programming error (PGE) is indicated.

There is no method provided within this controller to read actual disk headers. The user's software must include a method for bypassing unusable sectors in non-error free media.

5.4 WRITE HEADER

With one exception, this command is illegal and results in a programming error (PGE). The exception is a pack format. The controller contains a formatting routine within the microcode. This format routine is executed via a Write Header command with the Format Enable flag set. The flag is set in one of two ways: first, by having the Format Enable switch ON (SW1-4) when the Write Header command is issued, and second, by writing a 177777 into RPSH (see section 4.1) just prior to issuing the Write Header command. The second method of setting the flag is temporary. The flag is reset when RDY goes from zero to one.

The actual format operation is done on the entire logical unit selected via RPCS bits <10:08>. Headers are created and written, and data fields of all zeros are created and written. Sectors are interleaved in a 3-to-1 organization to optimize system throughput. In mapped mode, any unused sectors on the last physical track are formatted with illegal headers and zero data fields so that they are not accidentally used during Read or Write operations.

5.5 Data Transfer ERRORS

If any error occurs which terminates a Data Transfer operation, then RPCA and RPDA contains the address of the sector that caused the error. During a Read operation, the data from the sector that caused the Read error is transferred to memory regardless of whether the data is correctable or not. Data Transfer errors include all DMA errors and all disk Read/Write errors.

Since Data Transfer errors result in RPCA and RPDA addressing the sector that caused the error, and since a Home Seek does not affect either RPCA or RPDA, error recovery routines do not have to reload either RPCA or RPDA. Note that a Read error that occurs during a Write Check results in a status that shows both a Read error and a Write Check error.

5-5

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APPENDIX A

SC12/A CONFIGURATION AND OPTION SELECTION

A.1 INTRODUCTION

To allow the user of the SC12/A the greatest amount of flexibility in selecting disk drives for his system, the SC12/A supports a wide variety of disk types and offers a number of other user selectable options. This appendix is designed as a quick reference to the various switches and jumpers which make this flexibility possible. For more detailed information about user selectable options see the Installation chapter in this manual.

A.2 DRIVE CONFIGURATION

The SC12/A unit is capable of controlling a wide variety of disk drives of various sizes and types. The various drives that are supported are defined by the configuration PROM. Table A-1 is a list of the drive types and sizes that are supported. The user may choose between the available options by means of configuration switch SW2. The switch settings for each of the various configurations are given in Table A-2.

A.2.1 Single Drive Installations

To find the configuration setting that is suitable for your single disk drive installation, use the following process. Note that all configurations require that the drive be hard sectored as noted in the Sec column of Table A-1. See the manufacturer's drive installation manual for instructions.

1. Locate your drive type and size in Table A-1. Note down the configuration code(s) assigned to your drive. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for the drive.
2. Find the configuration number for your drive in the CONF NO. column of Table A-2. If there is more than one number for an individual drive, start with the smallest. Note that for each configuration row, specifications are given for two physical drives, Unit 0 and 1.
3. When you find the proper row, compare the Physical Drive track and sector figures (but not the cylinder data) for Unit 0 in Table A-2 with the numbers you noted down from Table A-1. They must match. If they do not, go on to the next higher configuration number, etc, until you find a match.

4. When you find a match, set the Configuration Switches (SW2) as indicated in Table A-2. (Generally, there is more than one match. In such cases, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuration you like best, and set the Configurations Switches accordingly.)

A.2.2 Dual Drive Installations (same type drive)

To find the configuration setting that is suitable for your dual disk drive installation (drives same size and type), use the following process. Note that all configurations require that the drives both be hard sectored as noted in the Sec column of Table A-1. See the manufacturer's drive installation manual for instructions.

1. Locate your drive type and size in Table A-1. Note down the configuration code(s) assigned to your drives. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for the drives.
2. Find the configuration number for your drives in the CONF NO. column of Table A-2. If more than one number was given for the drives, start with the smallest. Note that for each configuration row, specifications are given for two physical drives, Unit 0 and 1. The physical cylinder, track and sector numbers for Unit 0 and 1 in that row must match. If they do not, go on to the next configuration number.
3. When you find the proper row, compare the Physical Drive track and sector figures for both Unit 0 and Unit 1 in Table A-2 with the track and sector numbers you noted down from Table A-1. They must match. If they do not, go on to the next higher configuration number, etc, until you find a match.
4. When you find a match, set the Configuration Switches (SW2) as indicated in Table A-2. (Generally, there is more than one match. In such cases, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuration you like best, and set the Configuration Switches accordingly.)

A.2.3 Dual Drive Installations (different drive types)

To find the configuration settings that are suitable for your dual disk drive installation (different drive size and type), use the following process. Note that all configurations require that the drives both be hard sectored as noted in the Sec column of Table A-1. See the manufacturer's drive installation manual for instructions.

1. Locate your drive types and sizes in Table A-1. Note down the configuration code(s) assigned to each drive. Note also the cylinder (Cyl), track (Trk) and sector (Sec) figures for each drive.
2. Once you have located and noted your drive configuration codes, compare the codes for each drive to one another. There must be at least one match if that drive combination is supported.
3. Consult Table A-2. Find the configuration number that both drives have in common in the CONF NO. column. If more than one number was given for the drive, start with the smallest.
4. For each configuration row, specifications are given for two physical drives, Unit 0 and 1. The two sets of numbers will be different. Compare the physical track and sector numbers for each unit with the corresponding numbers from Table A-1. The physical drive that matches the numbers for physical unit 0 becomes unit 0. The physical drive whose numbers match physical unit 1's becomes unit 1.
5. If there is more than one configuration supported, look at the Logical Unit and Drive Type column for each configuration where a match was found. Choose the Logical configuration you like best, and set the Configuration Switches (SW2) accordingly.

TABLE A-1
DRIVES SUPPORTED

Mfg.	Model	Cyl	Trk	Sec	Configurations
AMPEX	940	411	5	32	52
AMPEX	93160	1645	5	35	13,50
BALL	BD160	1645	5	35	13
BASF	6172	614	3	23	23
BASF	6173	614	5	23	24
CENTURY	T82	815	5	35	4,5,44
CENTURY	T82RM	823	5	35	4,5,6,11,44,51
CDC	9448-32	823	2	35	0,2
CDC	9448-64	823	4	35	1
CDC	9448-96	823	6	35	0
CDC	9448-96	823	6	32	3
CDC	9455	206	4	32	20
CDC	9457	624	4	32	47
CDC	9762	823	5	35	4,5,6,11,44,51
CDC	9730-12	320	2	35	35

TABLE A-1, cont.

Mfg.	Model	Cyl	Trk	Sec	Configurations
CDC	9730-24	320	4	35	34
CDC	9730-80	823	5	35	4,5,6,11,44,51
CDC	9730-160	823	10	35	7,10,11
FUJITSU	2311	589	4	34	25
FUJITSU	2312	589	7	34	26,53
FUJITSU	2284	823	10	34	41,42,43
FUJITSU	2284	823	10	35	51
KENNEDY	5300-70	700	5	35	4
KENNEDY	5300-70	700	5	32	36,40
KENNEDY	5300-80	823	5	35	4,5,6,11,44,51
MEMOREX	612-84	350	12	35	15
NISSEI	NP30-40	370	5	35	31
NISSEI	NP30-80	370	11	35	32
NISSEI	NP30-120	568	11	35	33
OKIDATA	3306	339	12	32	37,40
PRIAM	3350	561	3	32	12
PRIAM	3350	561	3	35	14
PRIAM	6650	1122	3	35	16
PRIAM	15450	1122	7	35	17
PRIAM	2050	525	3	23	21
PRIAM	3450	525	5	23	22
PRIAM	7050	1049	5	23	45,46
SLI	Sheyenne 3	656	5	19	27
SLI	Sheyenne 4	656	7	19	30

TABLE A-2
SC12/AX CONFIGURATION PROM 195 REV L

CONF NO.	SW2-						Unit	Physical			Unit(s)	Dr = Type	Cyl	Cap	Rev
	6	5	4	3	2	1		Cyl	Trk	Sec					
0	0	0	0	0	0	0	0	823	6	35	0,1,2,3,4,5	= RP02	144	14.7	A
							1	823	2	35					
1	0	0	0	0	0	C	0	823	4	35	0,1,2,3	= RP02	144	14.7	A
							1	823	4	35					
2	0	0	0	0	C	O	0	823	2	35	0,1	= RP02	144	14.7	A
							1	823	2	35					
3	0	0	0	0	C	C	0	823	6	32	0,1,2,3,4,5	= RP02	131	13.4	A
							1	823	2	32					
4	0	0	0	C	O	O	0	700	5	35	0,1,2	= RP02	203	Std	A
							1	700	5	35					
5	0	0	0	C	O	C	0	815	5	35	0,1,2	= RP02	237	24.2	A
							1	815	5	35					
6	0	0	0	C	C	O	0	823	5	35	0	= RP03	720	73.7	A
							1	823	5	35					
7	0	0	0	C	C	C	0	823	10	35	0,1,2	= RP03	406	Std	A
							1	823	10	35					

TABLE A-2, cont.

CONF NO.	SW2-							Physical			Unit(s)	Dr = Type	Cyl	Cap	Rev
	6	5	4	3	2	1	Unit	Cyl	Trk	Sec					
11	0	0	C	0	0	C	0	823	10	35	0,1,2,3,4,5,6	= RP02	203	Std	F
							1	823	5	35		7 = RP03	720	73.7	A
12	0	0	C	0	C	0	0	561	3	35		0 = RP02	203	Std	A
							1	561	3	35		1 = RP02	203	Std	A
13	0	0	C	0	C	C	0	1645	5	35	0,1,2,3,4,5,6	= RP02	203	Std	A
							1	1645	5	35		7 = RP03	1312	134	A
14	0	0	C	C	0	0	0	561	3	35		0 = RP02	294	30.1	A
							1	561	3	35		1 = RP02	294	30.1	A
15	0	0	C	C	0	C	0	350	12	35	0,1,2	= RP02	245	25.0	A
							1	350	12	35	3,4,5	= RP02	245	25.0	A
16	0	0	C	C	C	0	0	1122	3	35		0 = RP03	589	60.3	A
							1	1122	3	35		1 = RP03	589	60.3	A
17	0	0	C	C	C	C	0	1122	7	35		0 = RP03	1312	134	B
							1	1122	7	35		1 = RP03	1312	134	B
20	0	C	0	0	0	0	0	206	4	32	0,1	= RP02	65	6.6	B
							1	206	4	32	2,3	= RP02	65	6.6	B
21	0	C	0	0	0	C	0	525	3	23		0 = RP02	181	18.5	A
							1	525	3	23		1 = RP02	181	18.5	A
22	0	C	0	0	C	0	0	525	5	23		0 = RP02	301	30.8	D
							1	525	5	23		1 = RP02	301	30.8	D
23	0	C	0	0	C	C	0	614	3	23		0 = RP02	211	21.6	A
							1	614	3	23		1 = RP02	211	21.6	A
24	0	C	0	C	0	0	0	614	5	23		0 = RP02	353	36.1	A
							1	614	5	23		1 = RP02	353	36.1	A
25	0	C	0	C	0	C	0	589	4	34		0 = RP02	400	40.9	B
							1	589	4	34		1 = RP02	400	40.9	B
26	0	C	0	C	C	0	0	589	7	34		0 = RP03	700	71.6	B
							1	589	7	34		1 = RP03	700	71.6	B
27	0	C	0	C	C	C	0	656	5	19		0 = RP02	311	31.8	A
							1	656	5	19		1 = RP02	311	31.8	A
30	0	C	C	0	0	0	0	656	7	19		0 = RP03	436	44.6	A
							1	656	7	19		1 = RP03	436	44.6	A
31	0	C	C	0	0	C	0	370	5	35		0 = RP02	323	33.0	B
							1	370	5	35		1 = RP02	323	33.0	B
32	0	C	C	0	C	0	0	370	11	35	0,1,2	= RP02	203	Std	D
							1	370	11	35	3,4,5	= RP02	203	Std	D
33	0	C	C	0	C	C	0	568	11	35	0,1	= RP03	497	50.8	D
							1	568	11	35	2,3	= RP03	497	50.8	D
34	0	C	C	C	0	0	0	320	4	35		0 = RP02	224	22.9	C
							1	320	4	35		0 = RP02	224	22.9	C
35	0	C	C	C	0	C	0	320	2	35		0 = RP02	112	11.4	C
							1	320	2	35		0 = RP02	112	11.4	C
36	0	C	C	C	C	0	0	700	5	32		0 = RP03	560	57.3	C
							1	700	5	32		0 = RP03	560	57.3	C
37	0	C	C	C	C	C	0	339	12	32	0,1,2	= RP02	203	Std	E
							1	339	12	32	3,4,5	= RP02	203	Std	E
40	C	0	0	0	0	0	0	339	12	32	0,1,2	= RP02	203	Std	E
							1	700	5	35	3,4,5	= RP02	203	Std	E

TABLE A-2, cont.

CONF NO.	SW2-						Unit	Physical			Unit(s)	Dr =	Type	Cyl	Cap	Rev
	6	5	4	3	2	1		Cyl	Trk	Sec						
40	C	O	O	O	O	O	0	339	12	32	0,1,2 =	RP02	203	Std	E	
							1	700	5	35		3,4,5 =	RP02	203	Std	E
41	C	O	O	O	O	C	0	823	10	34	0,1 =	RP03	699	71.5	F	
							1	823	10	34		6,7 =	RP03	699	71.5	F
42	C	O	O	O	C	O	0	823	10	34	0,1,2 =	RP03	406	Std	F	
							1	823	10	34		3,4,5 =	RP03	406	Std	F
43	C	O	O	O	C	C	0	823	10	34	0,1,2,3,4,5 =	RP02	203	Std	F	
							1	823	10	34		6,7 =	RP03	699	71.5	F
44	C	O	O	C	O	O	0	823	5	35	0 =	RP03	406	Std	G	
							1	823	5	35		1 =	RP03	406	Std	G
45	C	O	O	C	O	C	0	525	5	23	0 =	RP03	602	61.6	G	
							1	525	5	23		1 =	RP03	602	61.6	G
46	C	O	O	C	C	O	0	525	5	23	0,1 =	RP02	301	30.8	G	
							1	525	5	23		2,3 =	RP02	301	30.8	G
47	C	O	O	C	C	C	0	624	4	32	0,1 =	RP02	199	20.4	K	
							1	624	4	32		2,3 =	RP02	199	20.4	K
50	C	O	C	O	O	O	0	1645	5	35	0 =	RP03	1439	147.3	H	
							1	1645	5	35		1 =	RP03	1439	147.3	H
51	C	O	C	O	O	C	0	823	10	35	0,1,2,3,4,5 =	RP02	203	Std	J	
							1	823	5	35		6 =	RP03	720	73.7	J
52	C	O	C	O	C	O	0	411	5	32	0 =	RP02	328	33.5	K	
							1	411	5	32		1 =	RP02	328	33.5	K
53	C	O	C	O	C	C	0	589	7	34	0,1,2 =	RP02	203	STD	L	
							1	589	7	34		3,4,5 =	RP02	203	STD	L

NOTES: C = Closed (ON), O = Open (OFF)

A.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC12/A can be user selected. The functions of the switches that select those options are defined in Tables A-3, A-4 and A-5, below.

TABLE A-3
OPTION SWITCH SETTINGS

Option Sw	Open	Closed	Function
SW1-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW1-2			Not used ¹
SW1-3	Disabled	Enabled	No ECC correction on any operation
SW1-4	Disable	Enable	Firmware media format ²

¹All unused switches MUST BE OFF.

²See paragraph 3.7.3.

TABLE A-4
CONFIGURATION SWITCH SETTINGS

Config Sw	Open	Closed	Function
SW2-1			Drive Configuration ²
SW2-2			Drive Configuration ²
SW2-3			Drive Configuration ²
SW2-4			Drive Configuration ²
SW2-5			Drive Configuration ²
SW2-6			Drive Configuration ²
SW2-7	Enable	Disable	Logical to physical disk address mapping ⁴
SW2-8			Not used ¹
SW2-9			Interrupt vector select ³
SW2-10			Interrupt vector select ³

¹All unused switches MUST BE OFF.

²See Table A-2 for settings

³See Table 3-2 for settings

⁴See paragraph 3.4.5.1.

TABLE A-5
ADDRESS SWITCH SETTINGS

Address Sw	Open	Closed	Function
SW3-1			Not used ¹
SW3-2		777440	Alternate Unibus Address ³
SW3-3		776700	Standard Unibus Address ³
SW3-4			Not used ¹
SW3-5			Not used ¹
SW3-6	Disable	Enable	1k Microcode Address Range (normally closed)

¹All unused switches MUST BE OFF.

³Only one address may be selected. All other address switches MUST BE OFF.

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