EMULEX MICRO DEVICES

SCSI CHIP

ESP201/101*

FEATURES

- ❑ Conformity with ANSI X3.131 SCSI standard
- ❑ Synchronous data transfers of up to 5 MBPS
  - — Programmable synchronous transfer period
  - — Programmable synchronous offsets up to 15 bytes
- ❑ Asynchronous data transfers up to 7 MBPS
- ❑ DMA burst transfer rate up to 12 MBPS
- ❑ Functional enhancements and speed improvements over ESP200/100A
- ❑ New SCSI-2 features available to reduce microprocessor interrupts
- ❑ Reselect3 Sequence
- ❑ Reset ATN command
- ❑ Differential mode enhancements:
  - — Totem pole drivers on REQ/ACK
  - — SCSI bus input/output delay
- ❑ 16- or 24-bit Transfer Counter
- ❑ On-chip, single-ended SCSI transceivers (48-mA drivers)
- ❑ Initiator or Target mode
- ❑ Hot pluggability
- ❑ Pipelined command structure
- ❑ 16-byte data FIFO between DMA and SCSI channels
- ❑ Clock rates up to 25 MHz
- ❑ Low power dissipation
- ❑ SCSI sequences implemented without microprocessor intervention

** ESP201 also refers to ESP101, except where noted.*

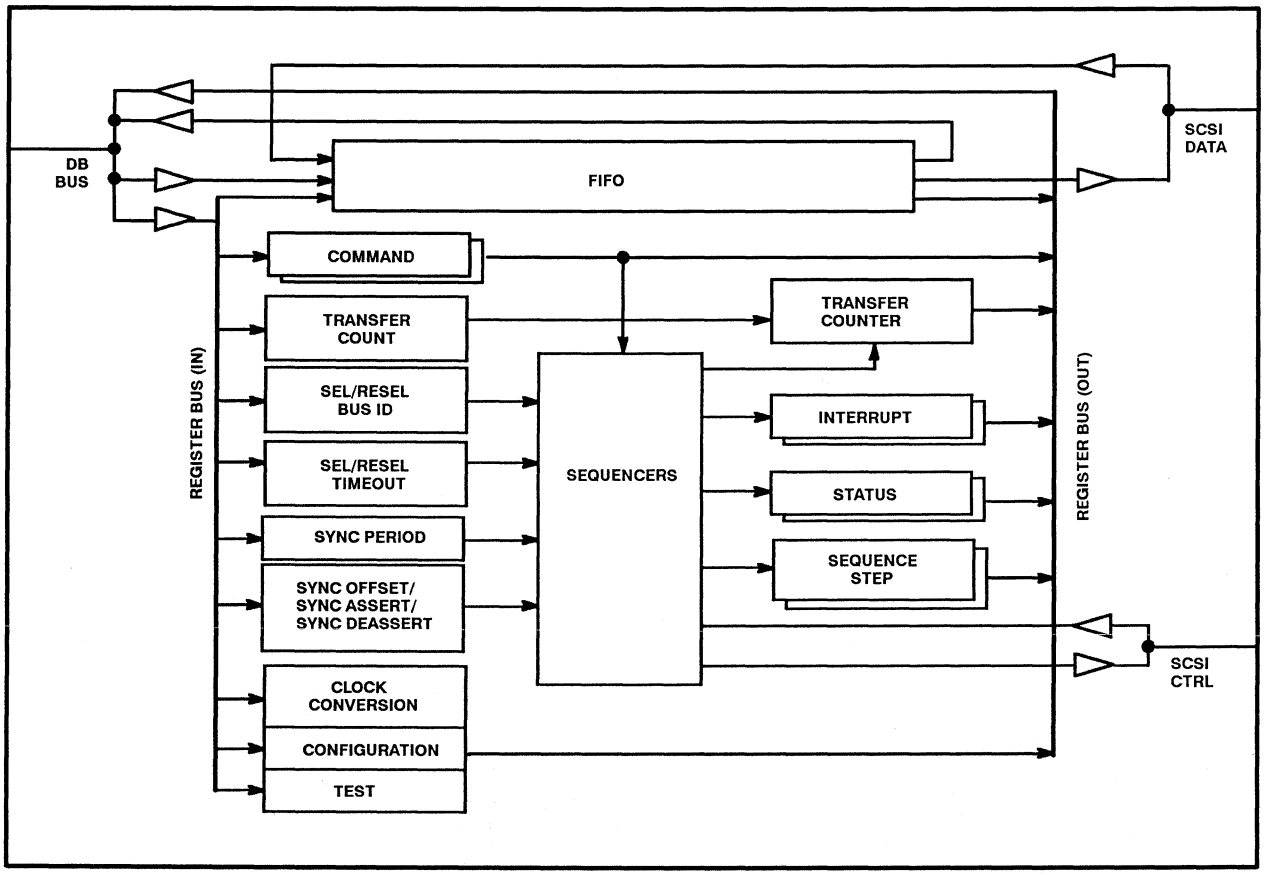


Figure 1. ESP201 Block Diagram

PRODUCT DESCRIPTION

The ESP201 is the high-performance enhancement to the Emulex ESP200 SCSI Processor. The ESP201 implements the detailed protocol of the SCSI Bus standard.

The ESP201 operates in both the Initiator and Target roles, and can therefore be used in both host adapter and peripheral applications. The ESP201 performs such functions as bus arbitration, selection of a Target, or reselection of an Initiator. It handles message, command, status, and data transfer between the SCSI Bus and the chip's 16-byte internal FIFO, or a buffer memory. The above functions are internal processes that the ESP201 chip performs without microprocessor intervention.

SYSTEM ORGANIZATION

The ESP201 chip provides hosts or targets with a SCSI solution for implementing the protocol of the SCSI Bus. The ESP101 checks and generates SCSI parity. The ESP201 also allows parity pass-through.

Applications include SCSI port processing for workstations and PCs as well as peripheral devices such as tape, scanners, and printers.

The ESP201 is pin compatible and functionally backward compatible with the ESP200. In addition, the following features and enhancements are included:

- ❑ Reselect3 Sequence
- ❑ Reset ATN command
- ❑ Differential mode enhancements:
  - — Totem pole drivers on REQ/ACK
  - — SCSI bus input/output delay
- ❑ Improved DMA transfer rate

The ESP201 has been optimized for interaction with a DMA controller and the controlling processor. Common SCSI Bus sequences that typically require significant amounts of processing time and microprocessor interaction have been reduced to single commands. These SCSI commands are listed in Table 1.

Table 1. Single SCSI Commands

Command	Description
Selection	Arbitration, target selection, transmission of an optional 1-byte (or 3-byte) message followed by a multiple-byte command.
Reselection	Arbitration, Initiator reselection, and transmission of a 1-byte (or 3-byte) Identify message.
Bus-Initiated Selection	Transmission of the selection bus ID, a 1-byte Identify or null message, a 2-byte Queue Tag message (if SCSI-2 mode), and a multiple-byte command.
Bus-Initiated Reselection	Transmission of the reselection bus ID followed by a 1-byte Identify message.
Target Command Complete	Transmission of a status byte and a 1-byte message.
Target Disconnect Sequence	Transmission of two 1-byte messages followed by disconnection from the SCSI Bus.
Initiator Command Complete	Transmission of a status byte and a 1-byte message.
Reselect3 Sequence	Transmission of a 1-byte Identify message and a 2-byte Queue Tag message.

INTERFACES

The ESP201 has two separate interfaces: the Buffer Data Bus and the SCSI Bus. Pins that support these interfaces and other chip operations are shown in Figure 2.

The buffer data interface supports DMA Request, DMA Acknowledge, and microprocessor interrupt signals. For DMA operations, the buffer interface manages access timing and generates all buffer memory addresses.

The SCSI Bus interface consists of an 8-bit input bus and an 8-bit output bus. The TGS/DIFFM pin (ESP201) or DIFFM pin (ESP101) configures the SCSI interface for single-ended or differential mode operations.

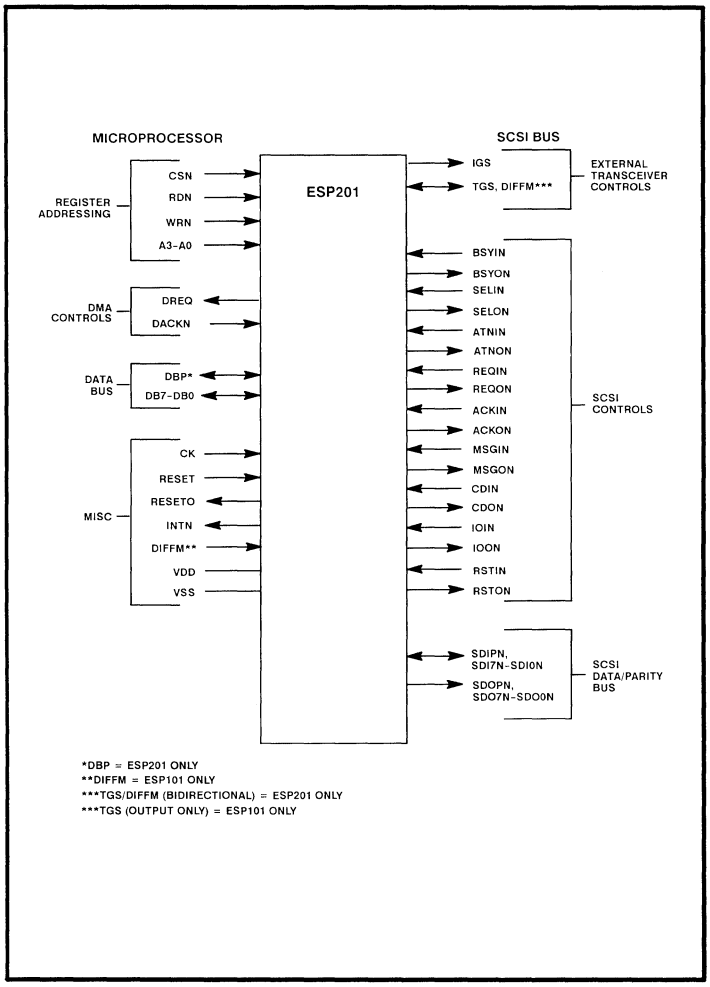


Figure 2. ESP201 Functional Signal Grouping

PIN DESCRIPTIONS

The ESP201 is available in a 68-pin PLCC package and an 80-pin PQFP package. The pin diagrams for these packages are illustrated in figures 3 and 4.

REGISTERS

The ESP201 registers are used by the microprocessor to configure, command, and monitor the SCSI Bus, and to pass data through the chip to the SCSI Bus. The ESP201 registers are summarized in Figure 5.

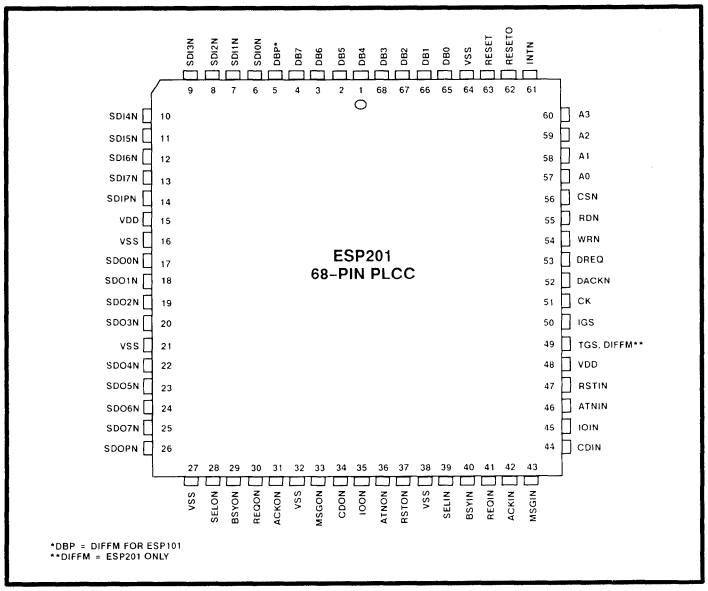


Figure 3. ESP201 68-Pin PLCC Pin Diagram

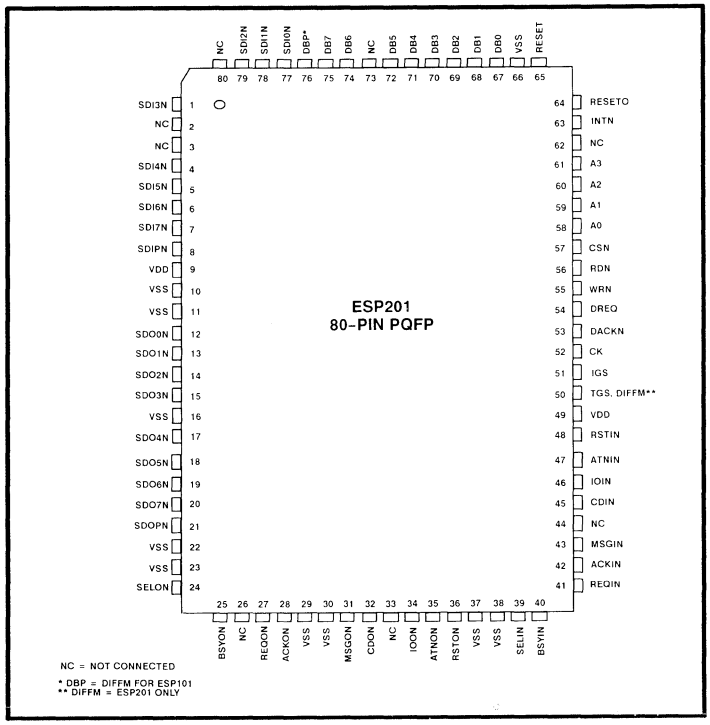


Figure 4. ESP201 80-Pin PQFP Pin Diagram

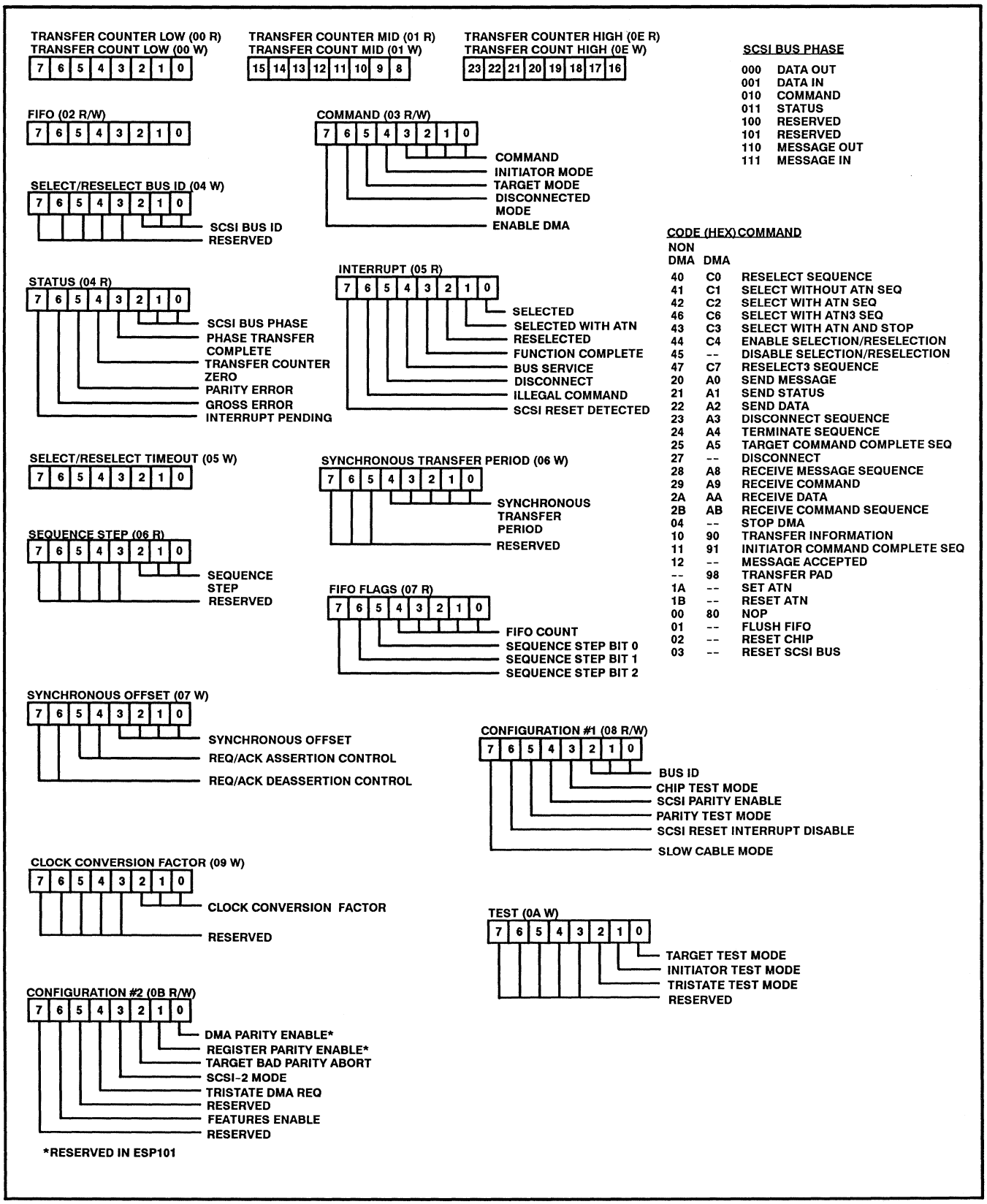


Figure 5. ESP201 Register Set

ELECTRICAL CHARACTERISTICS

Table 2. Absolute Maximum Stress Ratings

Symbol	Description	Min	Max	Unit
T_{STG}	Storage Temperature	-55	150	°C
V_{DD}	Supply Voltage	-0.5	7	V
V_{IN}	Input Voltage	V_{SS} - 0.5	V_{DD} + 0.5	V
I_{LP}[1]	Latch-Up Current	-100	100	mA
ESD[2]	Electrostatic Discharge (All except SCSI pins)	-3000	3000	V
ESD[2]	Electrostatic Discharge (SCSI pins)	-4000	4000	V

[1]Test conditions of $-2V < V_{PIN} < +8V$

[2]Test using the human body model -- 100pF at 1.5 KW (MIL-STD-883C method 3015)

Table 3. Operating Conditions

Symbol	Description	Minimum	Maximum	Unit
V_{DD}	Supply Voltage	4.5	5.5	V
I_{DD}[1]	Supply Current (Static I_{DD})		2	mA
I_{DD}[2]	Supply Current (Dynamic I_{DD})			mA
T_A	Ambient Temperature	0	70	°C

[1]Static I_{DD} refers to all inputs at V_{DD}, all outputs open circuit, and all bidirectional pins configured as inputs.

[2]Dynamic I_{DD} is dependent on the application.

DC CHARACTERISTICS

Table 4. Input Signals

Symbol	Description	Minimum	Maximum	Unit	Test Condition
A3-A0, WRN, DIFFM					
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
I_{IN}	Input Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Capacitance		10	pF	
ATNIN, ACKIN, BSYIN, REQIN, RSTIN, SELIN, MSGIN, CDIN, IOIN					
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
V_H	Hysteresis	200	700	mV	
I_{IL}	Input Current	-10	10	µA	$V_{IN} = 0$
C_{IN}	Capacitance		10	pF	
I_{IH}	Input High Leakage Current	-10	10	µA	$V_{IN} = 2.7V$ $0 < V_{DD} < 5.5$

Symbol	Description	Minimum	Maximum	Unit	Test Condition
		CSN, RDN, DACKN, CK, RESET			
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
V_H	Hysteresis	200	700	mV	
I_{IN}	Input Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Capacitance		10	pF	

Table 5. Output Signals

Symbol	Description	Minimum	Maximum	Unit	Test Condition
		DREQ, IGS			
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -4 mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
C_{OUT}	Capacitance		10	pF	
		INTN			
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
C_{OUT}	Capacitance		10	pF	
		RESETO			
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -8 mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
C_{OUT}	Capacitance		10	pF	
		ACKON, ATNON, REQON, BSYON, RSTON, SELON, MSGON, CDON, IOON, SDOPN, SDO7N-SDO0N			
V_{OL}	Output Low Voltage		0.5	V	I_{OL} = 48 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
S_{FT}	Signal Fall Time	4		ns	SCSI Termination
C_{OUT}	Capacitance		10	pF	

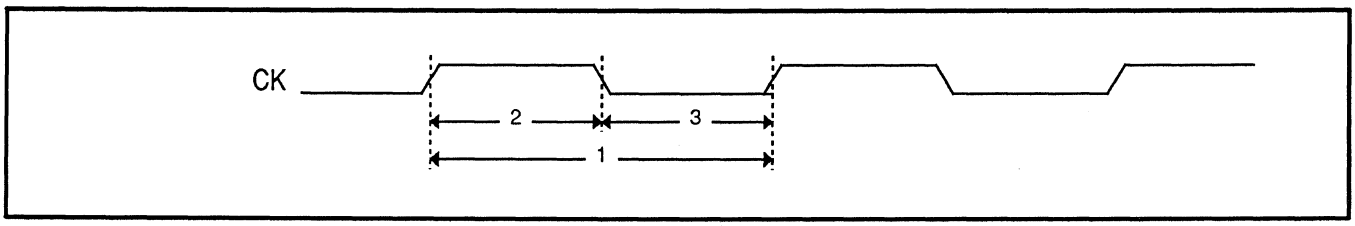
Table 6. Bidirectional Signals

Symbol	Description	Minimum	Maximum	Unit	Test Condition
		DB7-DB0, DBP*			
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
I_{IL}	Input Low Leakage	-660	-75	µA	V_{IN} = 0
I_{IH}	Input High Leakage	0	20	µA	$V_{IN} = V_{DD}$
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -4 mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA
C_{IO}	Capacitance		10	pF	

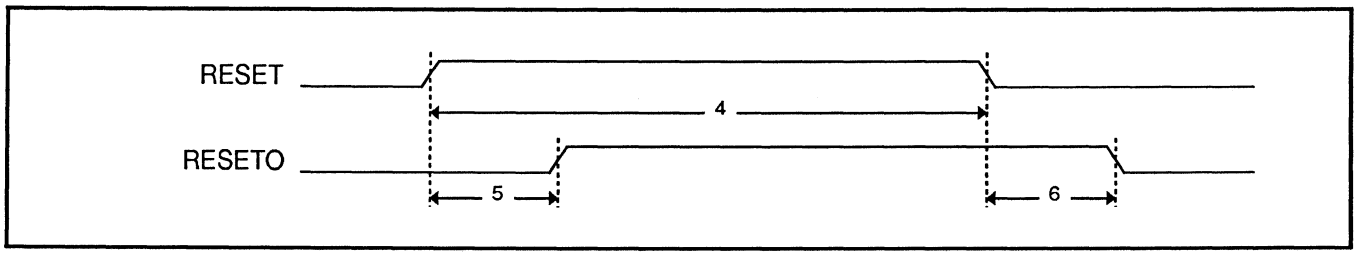
Symbol	Description	Minimum	Maximum	Unit	Test Condition
	SDIPN, SDI7N-SDI0N				
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
V_H	Hysteresis	200	700	mV	
I_{IN}	Input Current	-10	10	µA	$0 \leq V_{IN} \leq V_{DD}$
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -2 mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA
C_{IO}	Capacitance		10	pF	
	TGS**				
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
I_{IL}	Input Low Leakage	-660	-75	µA	V_{IN} = 0
I_{IH}	Input High Leakage	0	20	µA	V_{IN} = V_{DD}
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -8 mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8 mA
C_{IO}	Capacitance		10	pF	

* DBP applies to the ESP201 only.

** TGS is output-only in the ESP101.



CLOCK INPUT



RESET INPUT/OUTPUT

Figure 6. Clock Input and Reset Input/Output

AC TIMING

The following figures and table values are illustrative of the ESP201 chip timing characteristics. For more information, refer to the Emulex *ESP201/101 SCSI Processor Technical Manual*, VLSI51011-00 Rev A.

SYSTEM INTERFACE TIMING

Clock input, reset input/output, and interrupt output timing is listed below and illustrated in figures 6 and 7.

CLOCK INPUT						
#	Symbol	Description	Min	Max	Unit	Note
1	T_{CP}	Clock Period (1 ÷ Frequency)			ns	
	T_{CS}	Synchronization Latency	T_{CL}	$T_{CL} + T_{CP}$	ns	
	F_{CPA}	Clock Frequency, Asynchronous	12	25	MHz	
	F_{CPS}	Clock Frequency, Synchronous	20	25	MHz	
2	T_{CH}	Clock High	14.58	$0.65 \bullet T_{CP}$	ns	1
3	T_{CL}	Clock Low	14.58	$0.65 \bullet T_{CP}$	ns	1
RESET INPUT						
4	T_{RST}	RESET Pulse Width	200		ns	
RESET OUTPUT						
5	T_{RH}	RESET High To RESETO High		50	ns	
6	T_{RL}	RESET Low To RESETO Low		50	ns	
INTERRUPT OUTPUT						
7	T_{RI}	RDN Low to INTN High		75	ns	
8	T_{ICY}	RDN High to INTN Low	T_{CS}		ns	

NOTES

1. For synchronous SCSI transfers, the clock must also meet the following requirements: $(2 \bullet T_{CP} + T_{CL} \geq 97.92$ ns) and $(2 \bullet T_{CP} + T_{CH} \geq 97.92$ ns).

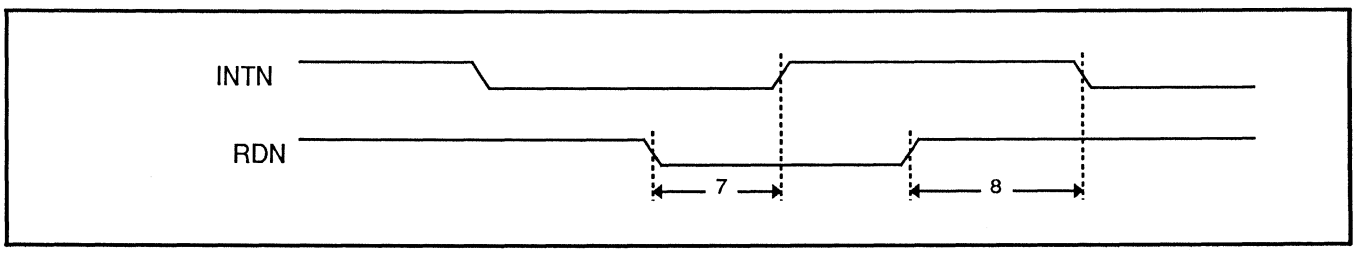


Figure 7. Interrupt Output

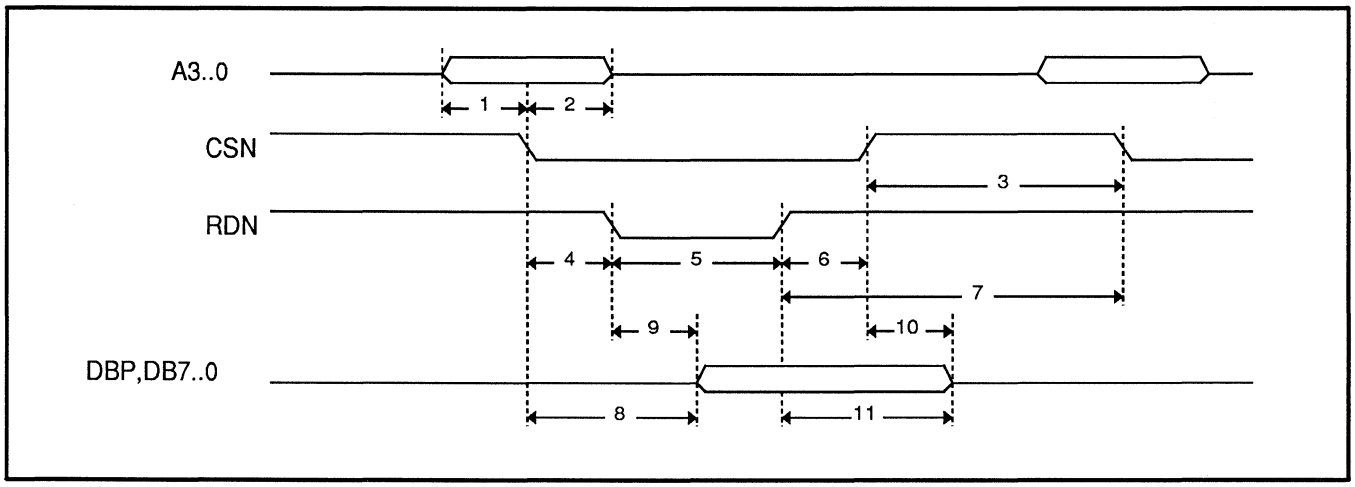
REGISTER INTERFACE TIMING

Register interface timing is listed below and illustrated in Figure 8.

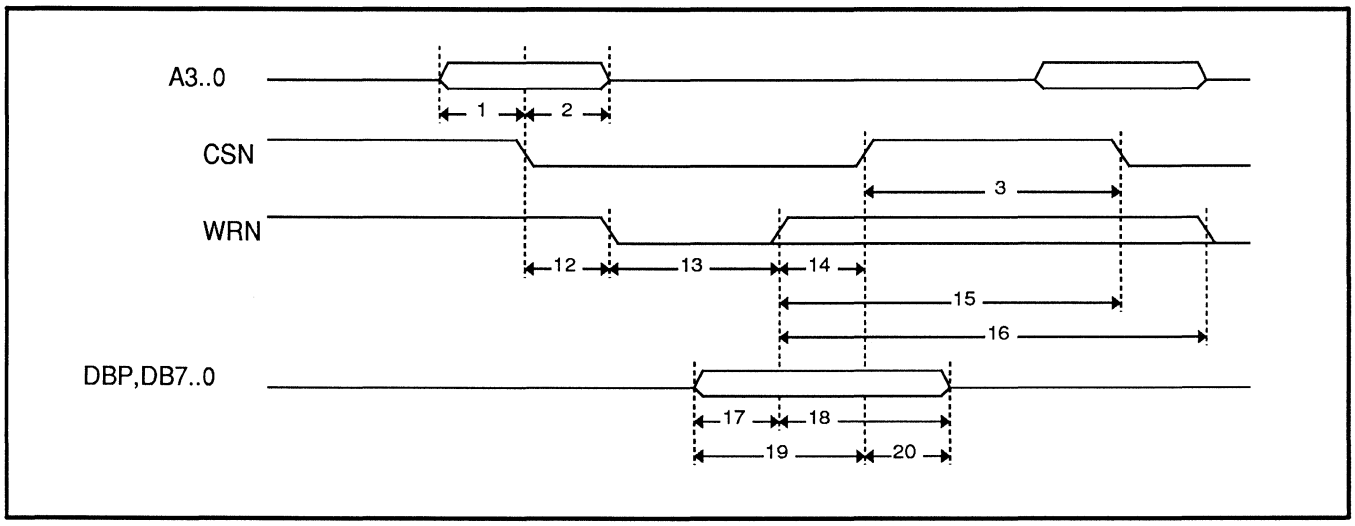
#	Symbol	Description	Min	Max	Unit	Note
1	T_{RASC}	Address Setup to CSN	0		ns	
2	T_{RAHC}	Address Hold from CSN	50		ns	
3	T_{RCCY}	CSN High to CSN Low	40		ns	1
		READ CYCLE				
4	T_{RCSR}	CSN Low to RDN Low	0		ns	
5	T_{RRD}	RDN Pulse Width	25		ns	
6	T_{RCHR1}	RDN High to CSN High	0		ns	
7	T_{RCHR2}	RDN High to CSN Low	40		ns	
8	T_{RDC}	CSN Low to Data		40	ns	2
9	T_{RDR}	RDN Low to Data		25	ns	2
10	T_{RDHC}	CSN High to Data Release	2	25	ns	3
11	T_{RDHR}	RDN High to Data Release	2	25	ns	3
		WRITE CYCLE				
12	T_{RCSW}	CSN Low to WRN Low	0		ns	4
13	T_{RWR}	WRN Pulse Width	25		ns	
14	T_{RCHW}	WRN High to CSN High	0		ns	4
15	T_{RWH}	WRN High to CSN Low	40		ns	
16	T_{RWCY}	WRN High to WRN Low	40		ns	1
17	T_{RDW}	Data Setup to WRN High	8		ns	5
18	T_{RDHW}	Data Hold from WRN High	0		ns	6
19	T_{RDWC}	Data Setup to CSN High	10		ns	5
20	T_{RDHWC}	Data Hold from CSN High	35		ns	6

NOTES

1. If WRN is held low T_{RCCY} is 35ns (min).
2. Both T_{RDC} and T_{RDR} specifications must be met.
3. RDN edges may precede or follow CSN edges.
4. WRN edges may precede or follow CSN edges.
5. Either T_{RDW} or T_{RDWC} specification must be met.
6. Either T_{RDHW} or T_{RDHWC} specification must be met.



REGISTER READ



REGISTER WRITE

Figure 8. Register Access

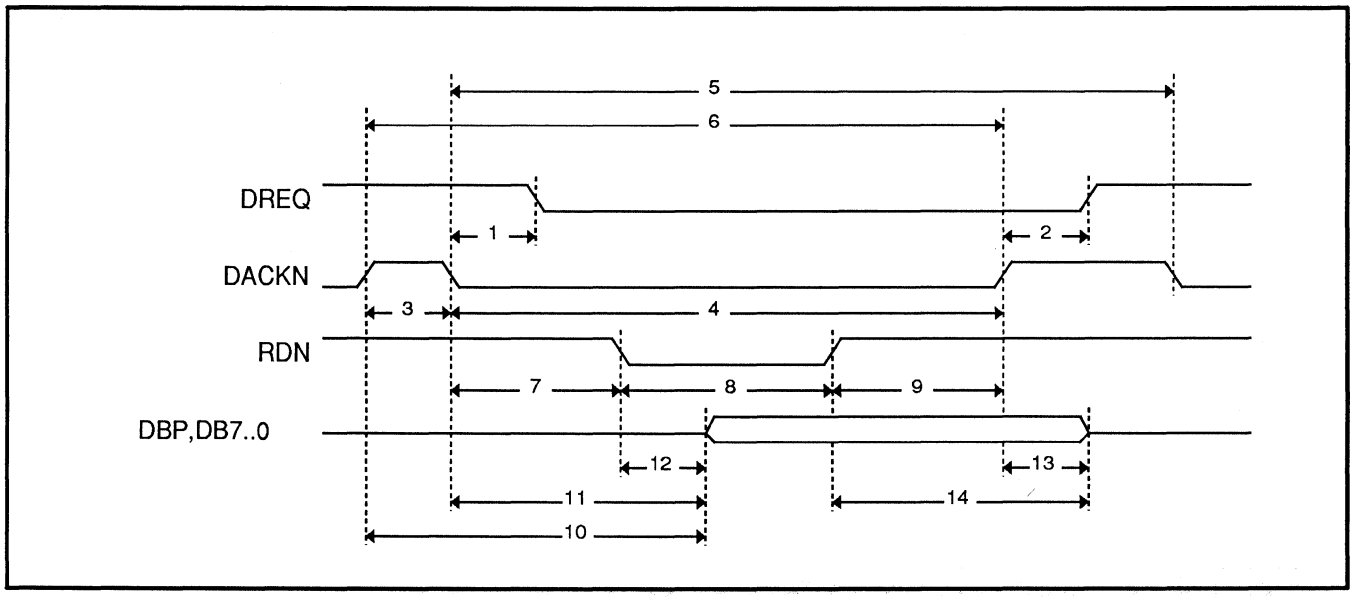
DMA INTERFACE TIMING

DMA interface timing is listed below and illustrated in Figure 9.

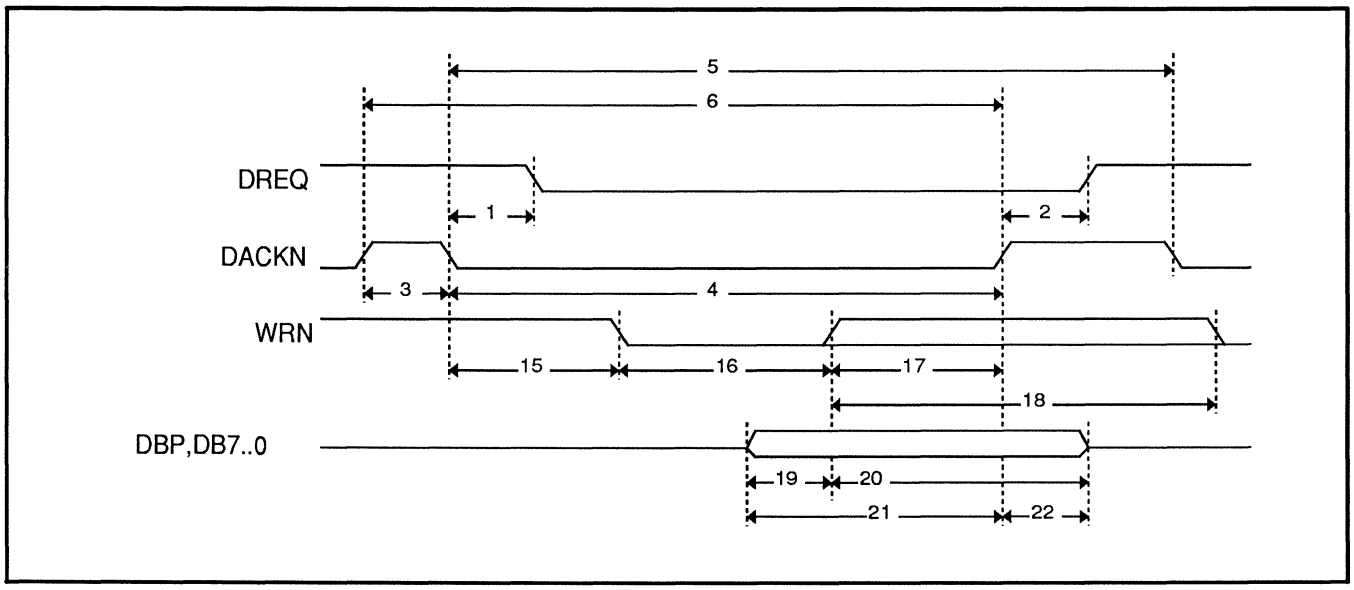
#	Symbol	Description	Min	Max	Unit	Note
1	T_{DARL}	DACKN Low to DREQ Low		20	ns	1
2	T_{DRH}	DACKN High to DREQ High		20	ns	2
3	T_{DACY}	DACKN High to DACKN Low	12		ns	3
4	T_{ACK}	DACKN Pulse Width	35		ns	
5	T_{ACP0}	DACKN Low to DACKN Low	75		ns	
6	T_{ACP1}	DACKN High to DACKN High	$T_{CS}+30$ $-T_{DACY}$ and $2T_{CP}$		ns	4
		READ CYCLE				
7	T_{DAR}	DACKN Low to RDN Low	0		ns	5
8	T_{DRD}	RDN Pulse Width	T_{DDRL}		ns	
9	T_{DRA}	RDN High to DACKN High	0		ns	6
10	T_{DDAH}	DACKN High to Data		30	ns	7
11	T_{DDAL}	DACKN Low to Data		25	ns	7
12	T_{DDRL}	RDN Low to Data		25	ns	7
13	T_{DADR}	DACKN High to Data Release	2	25	ns	
14	T_{DRDR}	RDN High to Data Release	2	25	ns	
		WRITE CYCLE				
15	T_{DAW}	DACKN Low to WRN Low	0		ns	8
16	T_{DWR}	WRN Pulse Width	30		ns	
17	T_{DWA}	WRN High to DACKN High	0		ns	9
18	T_{DWCY}	WRN High to WRN Low	30		ns	
19	T_{DDW}	Data Setup to WRN High	8		ns	10
20	T_{DHW}	Data Hold from WRN High	0		ns	11
21	T_{DDWA}	Data Setup to DACKN High	10		ns	10
22	T_{DHWA}	Data Hold from DACKN High	10		ns	11

NOTES

1. Negation pending.
2. Assertion pending.
3. If WRN is held low T_{DACY} = 30 ns (min).
4. Synchronous transfers only.
5. RDN low may precede DACKN low.
6. RDN high may follow DACKN high.
7. Both T_{DDAH} and T_{DDAL} specifications must be met.
8. WRN low may precede DACKN low.
9. WRN high may follow DACKN high.
10. Either T_{DDW} or T_{DDWA} specification must be met.
11. Either T_{DHW} or T_{DHWA} specification must be met.



DMA READ



DMA WRITE

Figure 9. DMA Access

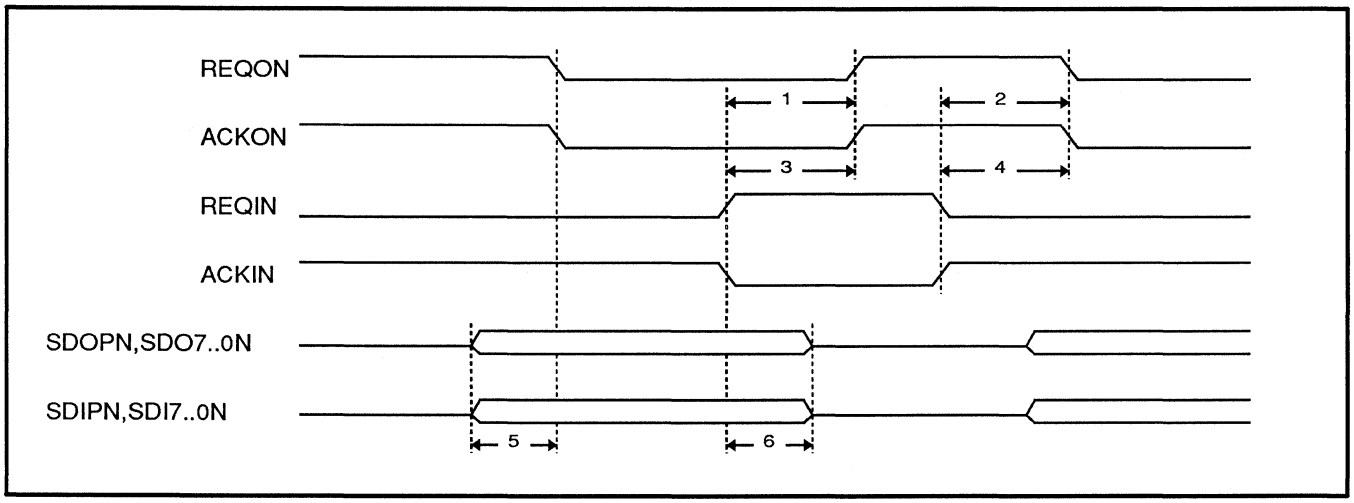
SCSI INTERFACE TIMING - ASYNCHRONOUS

SCSI interface asynchronous timing is listed below and illustrated in Figure 10.

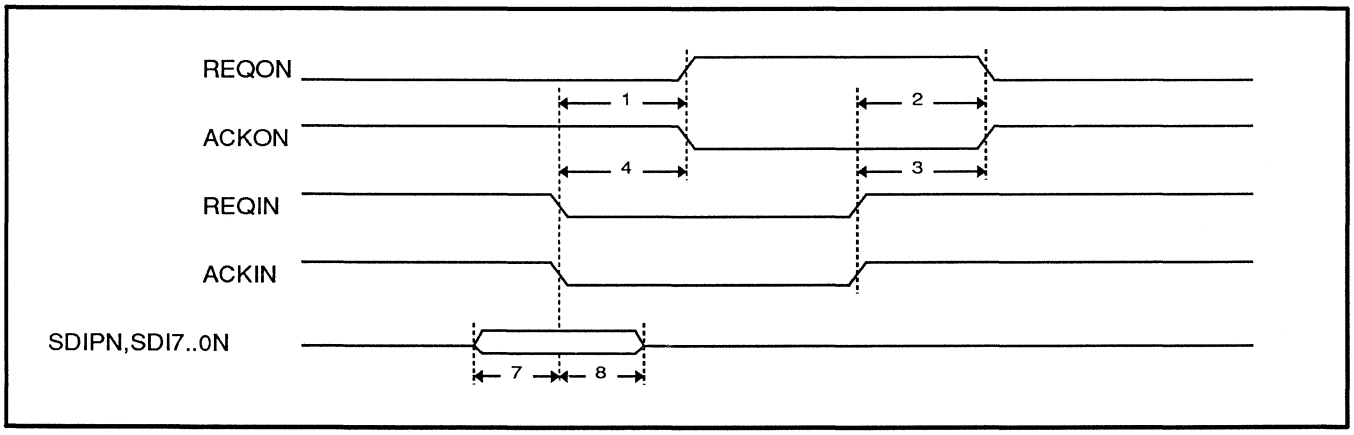
#	Symbol	Description	Min	Max	Unit	Note
		SINGLE-ENDED MODE[1]				
1	T_{AAR01}	ACKIN Low to REQON High		50	ns	
2	T_{AAR02}	ACKIN High to REQON Low		45	ns	3, 6
3	T_{ARA01}	REQIN High to ACKON High		50	ns	
4	T_{ARA02}	REQIN Low to ACKON Low		50	ns	4, 6
		Output Cycle				
5	T_{ARDSO}	Data Setup to REQON Low	60		ns	
5	T_{AADSO}	Data Setup to ACKON Low	60		ns	
6	T_{ARHDO}	Data Hold from REQIN High	5		ns	5
6	T_{AAHDO}	Data Hold from ACKIN Low	5		ns	5
		DIFFERENTIAL MODE[2]				
1	T_{AAR01}	ACKIN Low to REQON High		30	ns	
2	T_{AAR02}	ACKIN High to REQON Low		30	ns	3, 6
3	T_{ARA01}	REQIN High to ACKON High		25	ns	
4	T_{ARA02}	REQIN Low to ACKON Low		30	ns	4, 6
		Output Cycle				
5	T_{ARDSO}	Data Setup to REQON Low	70		ns	
5	T_{AADSO}	Data Setup to ACKON Low	70		ns	
6	T_{ARHDO}	Data Hold from REQIN High	5		ns	5
6	T_{AAHDO}	Data Hold from ACKIN Low	5		ns	5
		INPUT CYCLE				
7	T_{ARDSI}	Data Setup to REQIN Low	0		ns	
7	T_{AADSI}	Data Setup to ACKIN Low	0		ns	
8	T_{ARHDI}	Data Hold from REQIN Low		18	ns	
8	T_{AAHDI}	Data Hold from ACKIN Low		18	ns	

NOTES

1. 200pF loading, data out on lines SDOPN, SDO7N-0N.
2. Data out on lines SDIPN, SDI7N-0N.
3. T_{ARDSO} specification must also be met (output cycle only).
4. T_{AADSO} specification must also be met (output cycle only).
5. FIFO is not empty.
6. FIFO is not full (input cycle only).



ASYNCHRONOUS OUTPUT



ASYNCHRONOUS INPUT

Figure 10. SCSI Asynchronous Timing

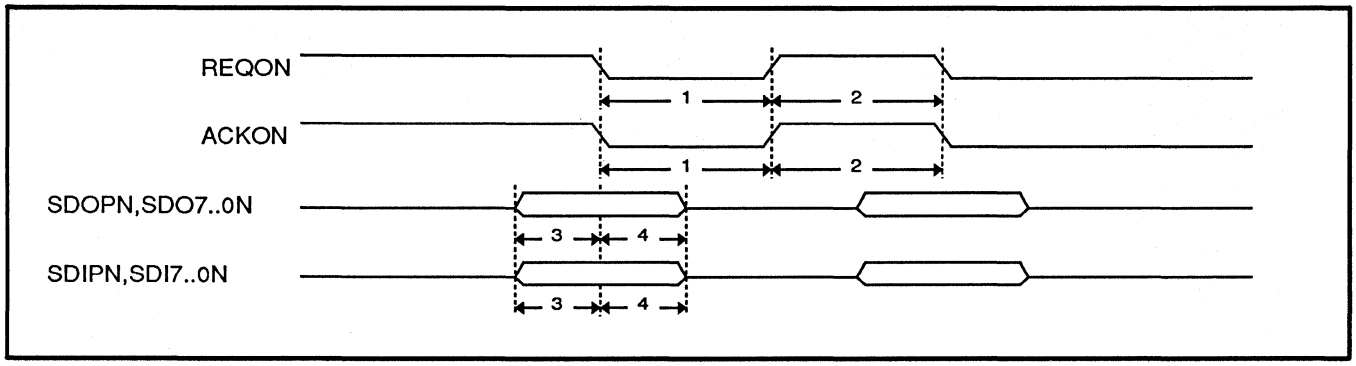
SCSI INTERFACE TIMING - SYNCHRONOUS

SCSI interface synchronous timing is listed below and illustrated in Figure 11.

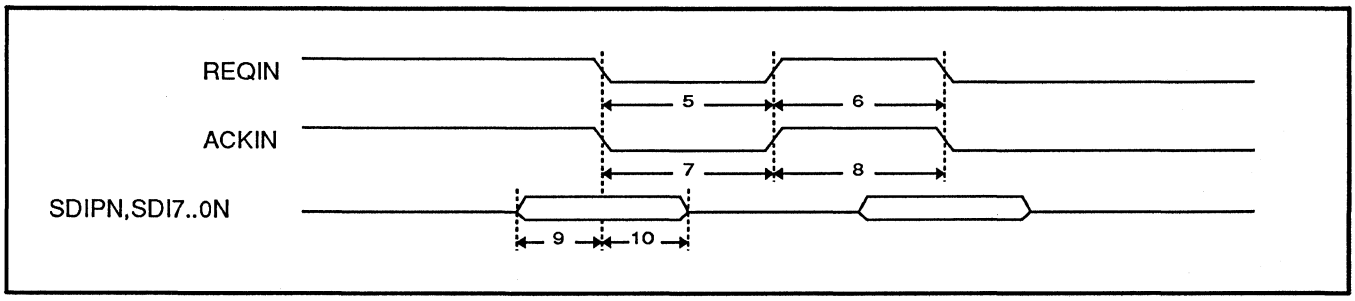
#	Symbol	Description	Min	Max	Unit	Note
		OUTPUT CYCLE				
		Single-Ended Mode[1]				
1	T_{SASTO}	REQON/ACKON Assertion Period	90		ns	
2	T_{SNEGO}	REQON/ACKON Negation Period	90		ns	
3	T_{SDSO}	Data Setup to REQON Low/ACKON Low	55		ns	
4	T_{SHDO}	Data Hold from REQON Low/ACKON Low	100		ns	
		Differential Mode[2]				
1	T_{SASTO}	REQON/ACKON Assertion Period	96		ns	
2	T_{SNEGO}	REQON/ACKON Negation Period	96		ns	
3	T_{SDSO}	Data Setup to REQON Low/ACKON Low	65		ns	
4	T_{SHDO}	Data Hold from REQON Low/ACKON Low	110		ns	
		INPUT CYCLE				
5	T_{SRASTI}	REQIN Assertion Period	27		ns	
6	T_{SRNEGI}	REQIN Negation Period	20		ns	
7	T_{SAASTI}	ACKIN Assertion Period	20		ns	
8	T_{SANEGI}	ACKIN Negation Period	20		ns	
9	T_{SDSI}	Data Setup to REQIN Low/ACKIN Low	5		ns	
10	T_{SHDI}	Data Hold from REQIN Low/ACKIN Low	15		ns	

NOTES

1. 5MBytes/sec max., data out on lines SDOPN, SDO7N-0N.
2. 5MBytes/sec max., data out on lines SDIPN, SDI7N-0N.



SYNCHRONOUS OUTPUT



SYNCHRONOUS INPUT

Figure 11. SCSI Synchronous Timing

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