

## HISTORY

- 1919 Sherman Fairchild invented a design for a revolutionary shutter for aerial cameras - subsequently opening a manufacturing plant in a loft in the New York City Garment District
- 1920 Fairchild Aerial Camera Corporation formed - involved in design and manufacture of aircraft, aerial cameras, and other aviation industry products
- 1936 Aircraft and engine manufacturing organized into separate company (became known as Fairchild Hiller Corporation in 1964)
- 1944 Aerial camera and electronics-oriented company interests renamed Fairchild Camera and Instrument Corporation
- 1955 Planar process for manufacturing transistors and integrated circuits developed in garage of scientist in Palo Alto - FC&I financially backed venture and urged formation of new company
- 1957 Fairchild Semiconductor incorporated at Palo Alto, California
- 1958 First major semiconductor order received by Fairchild Semiconductor
- 1959 Fairchild Semiconductor absorbed into FC&I
- 1965 Fairchild Semiconductor test equipment operation spins off as separate division - new name: Fairchild Instrumentation Division
- 1969 Instrumentation Division becomes Systems Technology Division

# TEST SYSTEM EVOLUTION

- 1963 Series 500 Transistor/Diode tester
- 1964 Series 4000 Integrated Circuit tester
- 1967 Series 600 Transistor/Diode tester
- 1968 Series 5000D I.C. tester (DC Parametric tester)  
5800 DTVM test bay (AC parametric test capability)  
Series 8000A computer controlled IC test system (function tester)
- 1969 Series 5000C computer controlled I.C. tester (DC parametric tester)  
Series 600C computer controlled transistor/diode tester  
5400 Function Test Head module added to 5000C tester
- 1970 Sentry 400 computer controlled MSI/LSI test system  
(functional and DC parametric test capabilities)  
Super-Sentry 400 (high-speed functional testing)

Sentry 100/200/300/400/500/600

Series 700T

Sentry 610

RANGER

670

PATT

System 11

System 12

Sentry II

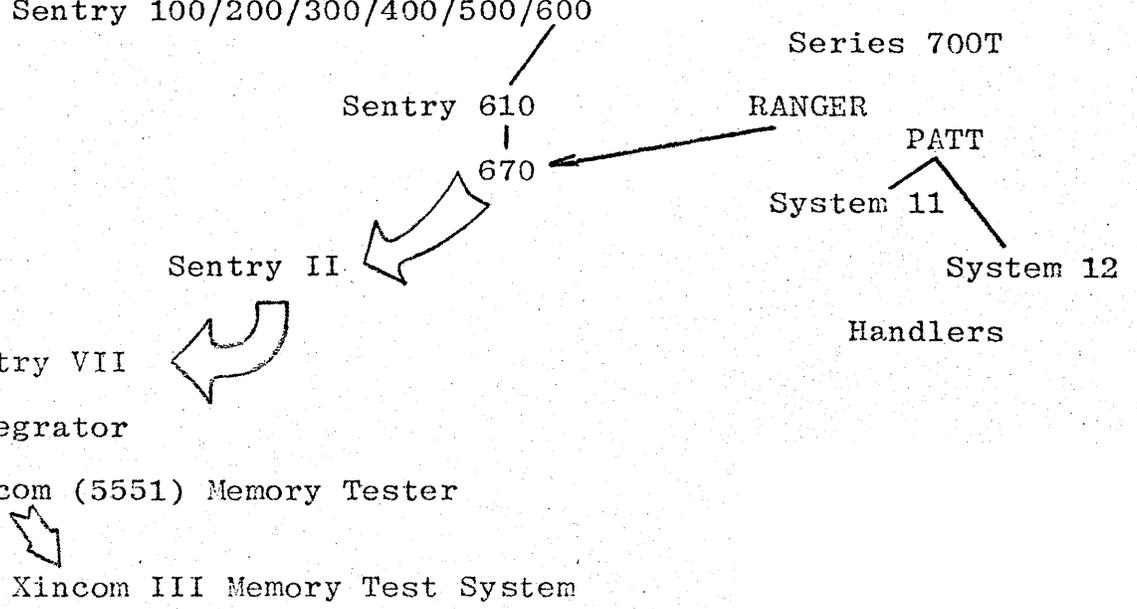
Handlers

1976 Sentry VII

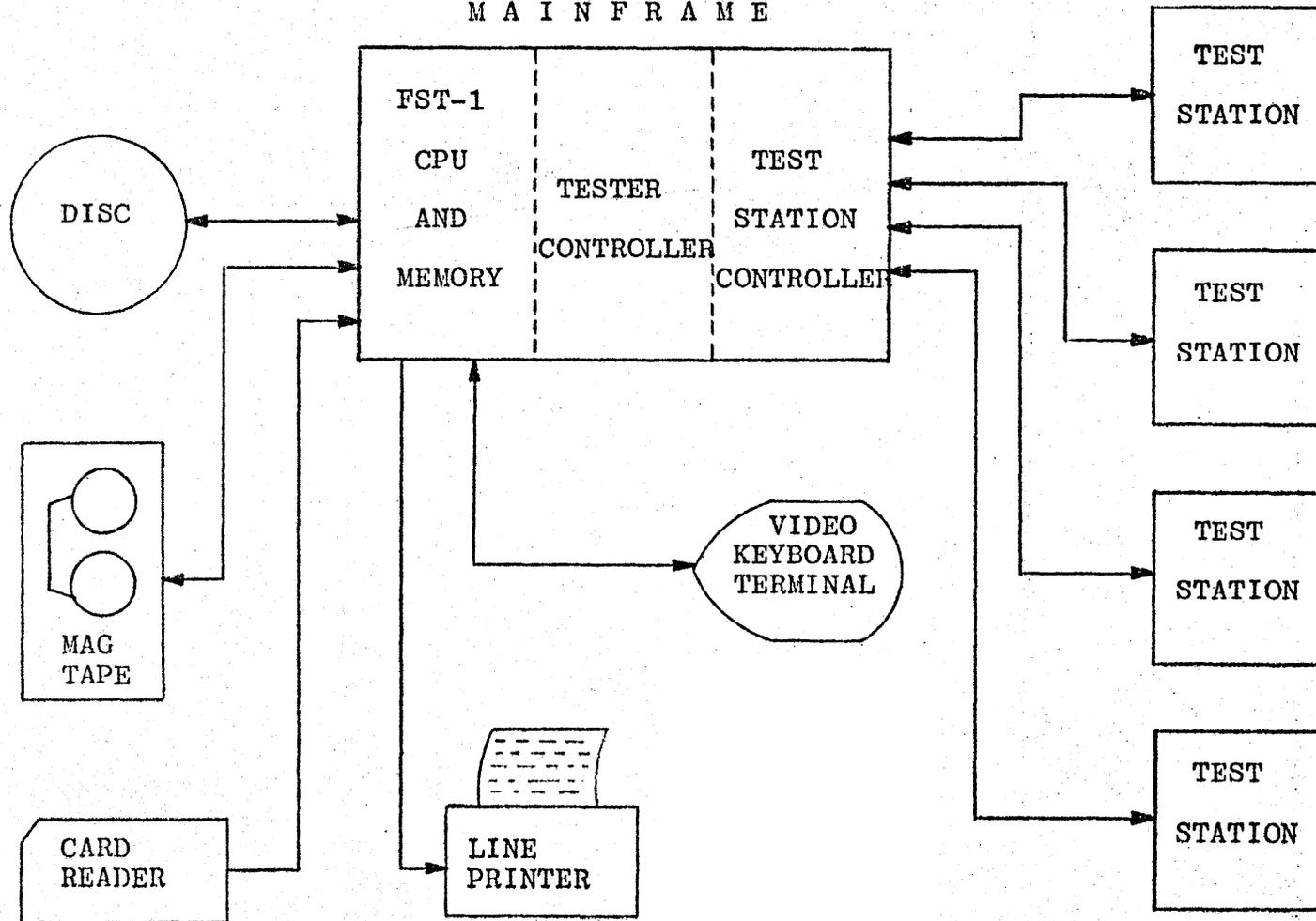
Integrator

Xincom (5551) Memory Tester

Xincom III Memory Test System



M A I N F R A M E



SENTRY II SYSTEM CONFIGURATION

## COMPUTER

- \* FST-1 GENERAL PURPOSE DIGITAL COMPUTER
  - 16K OF CORE MEMORY FOR ON-LINE STORAGE OF OPERATING SYSTEM SOFTWARE AND USER PROGRAM.
  - INTERFACE TO SYSTEM PERIPHERALS

## TESTER CONTROLLER

- \* USER PROGRAMMABLE POWER SUPPLIES
  - 3 DPS SUPPLIES (VF/IF 1,2,3) FOR POWER/BIAS PINS
  - 4 RVS SUPPLIES (EO,E1,EBO,EB1) FOR DATA INPUT STIMULUS
  - 4 RVS SUPPLIES (EAO,EAI,ECO,EC1) FOR CLOCK INPUT STIMULUS
  - 2 RVS SUPPLIES (SO,S1) FOR OUTPUT COMPARISON REFERENCE VOLTAGES
- \* MAINFRAME MULTIPLEXER

## HIGH SPEED TEST STATION CONTROLLER

- \* THE H.S.T.S. CONTROLLER CONTAINS LOCAL MEMORY AND TIMING GENERATORS WHICH ARE SHARED BY EACH ASSOCIATED TEST HEAD FOR PERFORMING FUNCTIONAL TESTING.
  - LOCAL MEMORY VARIABLE IN SIZE
    - UP TO 60 X 1024 FOR 5 MHZ SYSTEMS
    - UP TO 60 X 2048 FOR 10 MHZ SYSTEMS
  - LOCAL MEMORY HAS A LIMITED REPERTOIRE OF INSTRUCTIONS WHICH ALLOW IT TO PERFORM LIKE A SEPARATE LIMITED OPERATION COMPUTER ONCE AN OPERATION HAS BEEN INITIATED.
  - TIMING GENERATORS PROVIDE INDEPENDENT PROGRAMMABLE TIME CONTROL (PULSE DELAY AND WIDTH) FOR INPUT PINS (DATA AND/OR CLOCK), AS WELL AS OUTPUT COMPARATOR STROBES.
    - TG1 - 6 FOR INPUT PINS
    - TG7 - 8 FOR OUTPUT STROBES
  - DATA PINS NORMALLY OPERATE NRZ (NON-RETURN TO ZERO) BUT MAY BE PROGRAMMED TO RZ (RETURN TO ZERO).
  - CLOCK PINS AUTOMATICALLY OPERATE RZ.
  - OUTPUT PINS MAY BE SINGLE STROBED OR DOUBLE STROBED.
- \* THE H.S.T.S. CONTROLLER CONTAINS ONE PROGRAMMABLE PMU (PRECISION MEASUREMENT UNIT) WHICH IS SHARED BY EACH ASSOCIATED TEST HEAD WHEN PERFORMING DC PARAMETRIC TESTING.
  - PMU CAN FORCE VOLTAGE/MEASURE CURRENT OR FORCE CURRENT/MEASURE VOLTAGE AT ANY TESTER PIN.
    - MEASURE ACTUAL PARAMETER
    - GO/NO-GO PARAMETER TEST
  - PMU CAN MEASURE DPS VOLTAGES/CURRENTS OR RVS VOLTAGES AT INTERNAL TESTER NODES.
  - PMU HAS FIXED RANGE AS WELL AS AUTO RANGING CAPABILITY.

## TEST STATION

- \* UP TO FOUR TEST STATIONS ARE ALLOWED. TEST STATIONS CAN BE INTERMIXED FROM ANY OF THE FOLLOWING CONFIGURATIONS:
  - WAFER PROBER STATION
  - HAND INSERTION STATION
  - AUTO HANDLER STATION
  - ENVIRONMENTAL CHAMBER STATION
  
- \* REGARDLESS OF THE CONFIGURATION, THE TEST HEAD AT ANY TEST STATION CONTAINS THE PIN ELECTRONICS (OR THE CAPABILITY) TO SUPPORT UP TO 60 TESTER PINS.
  - ANY PIN MAY BE PROGRAMMED AS:
    - POWER SUPPLY/BIAS PIN
    - OUTPUT PIN
    - CLOCK INPUT PIN
    - INPUT/OUTPUT PIN
  - ANY PIN MAY BE SWITCHED FROM AN INPUT TO AN OUTPUT (AND VICE VERSA) AT A REAL TIME TEST RATE UNDER PROGRAM CONTROL.
  - EACH PIN HAS IT'S OWN SEPARATE INPUT DRIVER AND OUTPUT COMPARATOR CIRCUITS.
  - ANY PIN MAY BE CONNECTED TO OR DISCONNECTED FROM AUXILLARY USER SUPPLIED CIRCUITS ON THE TEST HEAD PERFORMANCE BOARD VIA PROGRAMMABLE UTILITY RELAYS.
  
- \* THE TEST STATION CONTAINS A USER PROGRAMMABLE EXTERNAL INTERFACE REGISTER (EIR) WHICH CAN BE USED FOR FUNCTIONS SUCH AS:
  - CATEGORY SORTING (AUTO OR VISUAL)
  - WAFER PROBER INKING CONTROL

## PERIPHERALS

### \* DISC

- AN ON-LINE (REAL-TIME) BULK STORAGE MEDIA FOR SYSTEM SOFTWARE AND USER DEVELOPED PROGRAMS

### \* MAGNETIC TAPE

- AN ON-LINE (USUALLY NON-REAL-TIME) BULK STORAGE MEDIA WHICH PROVIDES 3 MAIN CAPABILITIES
  - BACK-UP (DBUP) COPY OF COMPLETE SOFTWARE ON DISC
  - SELECTED PROGRAM STORAGE
  - STORAGE OF USER GATHERED DATA FOR DATA REDUCTION

### \* VIDEO KEYBOARD TERMINAL

- PROVIDES PRIMARY SYSTEM/USER INTERACTIVE COMMUNICATIONS FACILITY

### \* CARD READER

- PRIMARILY USED TO INPUT USER'S SOURCE PROGRAMS INTO THE SYSTEM FOR SUBSEQUENT STORAGE, TRANSLATION, AND EXECUTION

### \* LINE PRINTER

- PROVIDES HARD COPY DOCUMENTATION FOR THE USER FROM OPERATIONS SUCH AS: FDUMP, COMPILE, AND DATALOG

## SYSTEM SOFTWARE

TWO MAJOR CATEGORIES OF SOFTWARE ARE SUPPLIED WITH THE SENTRY SYSTEM - GENERAL PURPOSE COMPUTER SOFTWARE AND SPECIALIZED TEST SYSTEM CONTROL SOFTWARE.

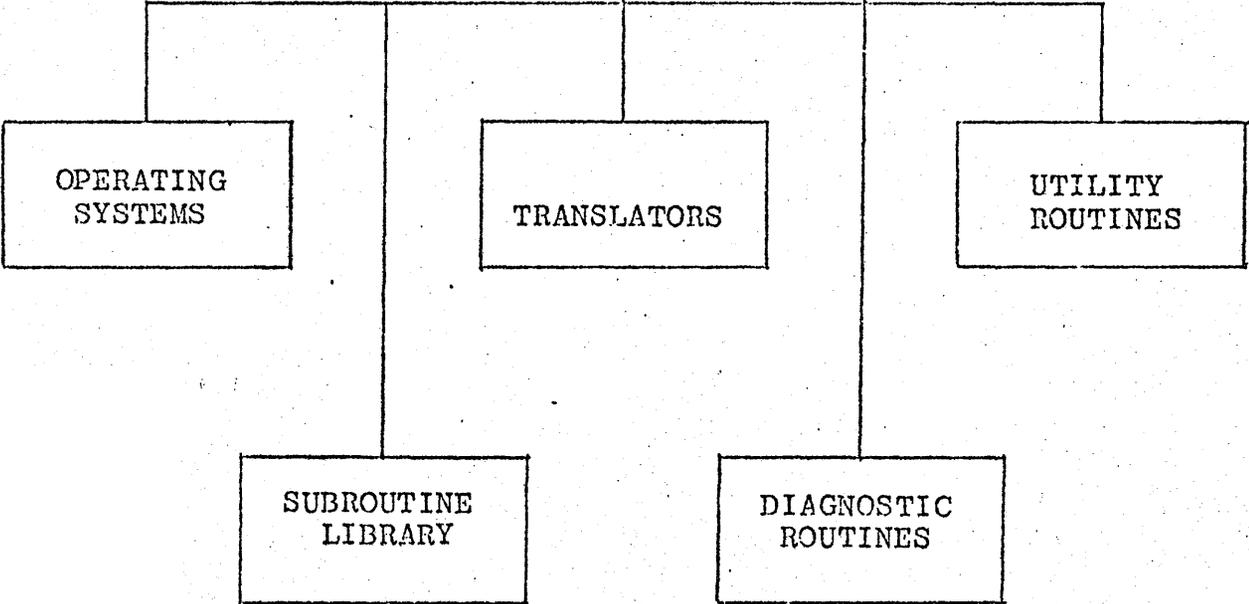
### GENERAL

- \* ASSEMBLER
- \* SUBROUTINE LIBRARY
- \* DISC OPERATING SYSTEM (DOPSY)
- \* UTILITIES
- \* COMPUTER AND PERIPHERAL DIAGNOSTICS

### SPECIAL

- \* TEST LANGUAGE COMPILER (FACTOR)
- \* TESTER OPERATING SYSTEM (TOPSY)
- \* TESTER DIAGNOSTICS

SENTRY SYSTEM  
SOFTWARE



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## SENTRY

## SOFTWARE

### ASSEMBLERS AND COMPILERS

- \* FST-1 ASSEMBLER
- \* FACTOR COMPILER

### SUBROUTINE LIBRARY

- \* CODE CONVERSIONS
- \* I/O ROUTINES
- \* DISC FILE PROCESSING ROUTINES
- \* FLOATING POINT ARITHMETIC ROUTINES

### OPERATING SYSTEMS

- \* DOPSY - DISC OPERATING SYSTEM
- \* TOPSY - TESTER OPERATING SYSTEM

### UTILITY ROUTINES

- \* LOADERS
- \* EDITORS
- \* COPY ROUTINES
- \* DUMP ROUTINES
- \* DEBUG ROUTINES
- \* FILE COMPARISON ROUTINES
- \* FILE VERIFICATION ROUTINES
- \* CALCULATOR ROUTINES
- \* NUMBER CONVERSION ROUTINES

## OPERATING SYSTEMS

EXTRACTED FROM THE BOOK BY THE SAME NAME AND  
WRITTEN BY HARRY KATZAN, JR.

AN "OPERATING SYSTEM" IS AN ORGANIZED COLLECTION OF PROGRAMS SPECIFICALLY DESIGNED TO FACILITATE THE CREATION OF COMPUTER PROGRAMS AND TO CONTROL THEIR EXECUTION ON A COMPUTER SYSTEM.

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IN THE SENTRY TEST SYSTEM ENVIRONMENT, THE DISC OPERATING SYSTEM (DOPSY) PERFORMS THE FUNCTION OF CREATING THE "DEVICE TEST PROGRAM" - WHICH WAS WRITTEN IN THE FACTOR COMPILER LANGUAGE - AND TRANSLATING IT INTO MACHINE EXECUTABLE CODE. THE TESTER OPERATING SYSTEM (TOPSY) IS THEN USED TO ACTUALLY EXECUTE THE TRANSLATED DEVICE TEST PROGRAM.

WHEN DEALING WITH A GENERAL PURPOSE/SPECIAL PURPOSE PROGRAM WRITTEN IN THE FST-1 ASSEMBLY LANGUAGE AND WILL NOT BE EXECUTED BY TOPSY, THEN DOPSY WILL PERFORM BOTH THE FUNCTIONS OF CREATING AND EXECUTING THE PROGRAM.

## DIAGNOSTICS

### CPU AND PERIPHERAL DIAGNOSTICS

SPUD	OVERALL CPU CHECK
NDXDI	INDEX REGISTER DIAGNOSTIC
PYRDI	ADDER PYRAMID DIAGNOSTIC
ATXDI	INDEX REGISTER DIAGNOSTIC
MEMDI	MEMORY TEST
MEMV3	MEMORY TEST
DSKDI	DISC DIAGNOSTIC - DESTRUCTIVE
DSKTST	DISC TEST
SPARWB	DISC TEST FOR MAINTENANCE SECTORS
DSKDMP	DISC DUMP TO LINE PRINTER
TTYDI	TELETYPE/VKT DIAGNOSTIC
CRDIA	CARD READER DIAGNOSTIC
LPDIA	DATA PRODUCTS LINE PRINTER DIAGNOSTIC
LSDIA	CENTRONICS SERIAL PRINTER DIAGNOSTIC
MGTDIA	MAGNETIC TAPE UNIT DIAGNOSTIC

### TESTER DIAGNOSTICS

TVFY	TESTER VERIFICATION PROGRAM
SPDG	SEQUENCE PROCESSOR MODULE DIAGNOSTIC
PPOD	PATTERN PROCESSOR MODULE DIAGNOSTIC
XXXX	ASSORTED FACTOR DEVICE TEST PROGRAMS