

FLOATING POINT
SYSTEMS, INC.

FPS-100 SPECIFICATIONS

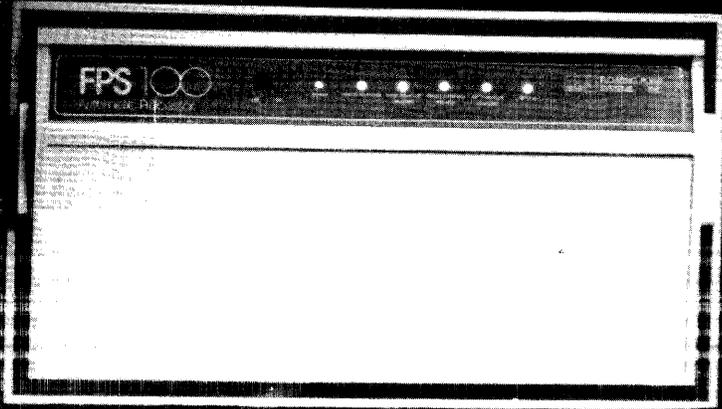
FPS 100
Arithmetic Processor

FPS 100
ARITHMETIC PROCESSOR

power real time mode host interrupt direct memory AP interrupt AP mode
off on enabled transfer enabled

FPS 100
Arithmetic Processor

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FPS-100

BENEFITS

- High performance
- High throughput
- Eight decimal-digit accuracy
- Real-time capabilities
- Performs up to 10 concurrent operations.....
- Easy to use
- Easy to configure into systems
- Dependability

FEATURES

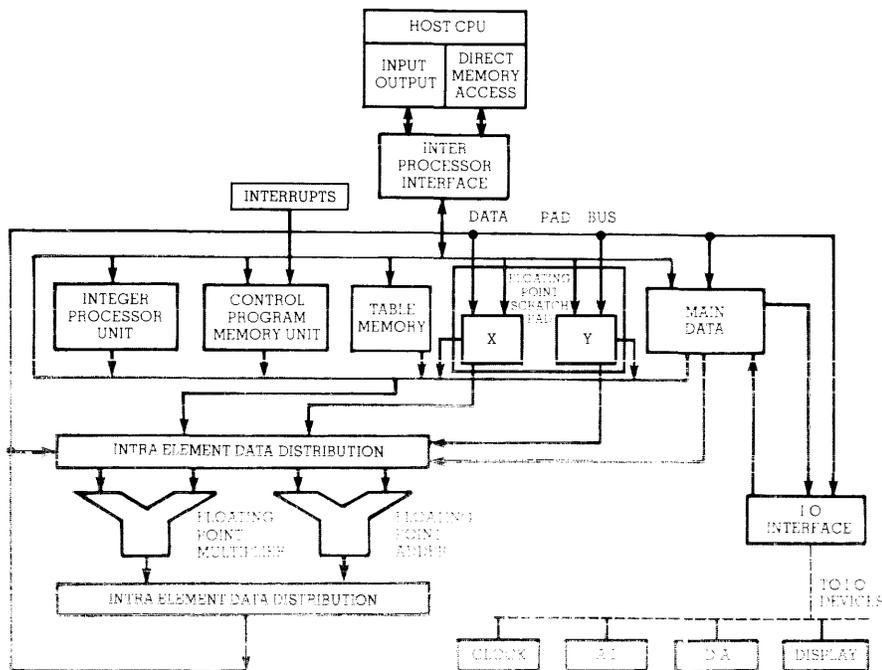
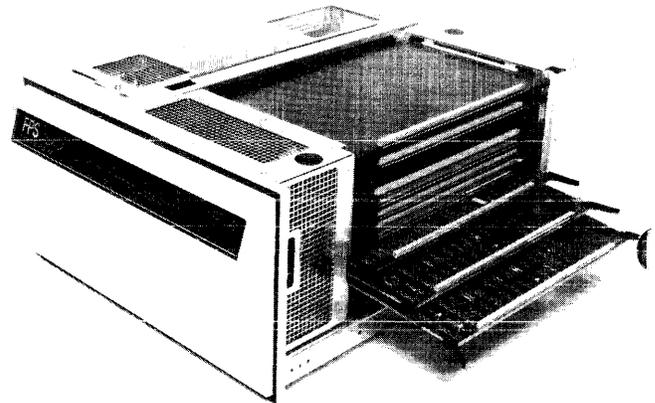
- Advanced architecture with seven independent parallel data paths, separate memories, host-independent I/O
- 8-million floating-point operations per second
- 38-bit floating-point arithmetic
- External and internal priority interrupts
- 64-bit instruction word
- Virtually all software necessary for simplified programming and development
- Compact, self-contained, low-power draw
- Continues the tradition of quality from the array processor leader; over 1000 systems shipped worldwide

General Description

The FPS-100 provides users with the most flexible and comprehensive combination of hardware and software available on an array processor today. The FPS-100 operates as an attached or peripheral arithmetic processor. While the user's host computer program maintains overall control, the FPS-100 executes either proven FPS library routines or user-developed application programs. Data to be processed is acquired either from the host computer or directly from an external source.

The unique SUPER-100 executive is available to provide resident FPS-100 task management and control. Making effective use of the priority interrupt structure, SUPER-100 creates a responsive real-time operating environment.

Optimum applications performance is attainable through the highly parallel and pipelined FPS-100 architecture, which employs multiple data paths and memory units.



Processor Specifications

Processor Cycle Time 250nsec

Data Characteristics

Word Format: 38-bit floating-point
Mantissa—
28-bit 2's complement
Exponent—
10-bit biased binary exponent
Dynamic Range: 3.7×10^{-155} to 6.7×10^{153}

Registers

Floating Point
Scratch Pad 64 × 38-bits
Integer Data Registers 16 × 16-bits
Subroutine Return Stack 16 × 12-bits

Memory Units	Type	Word Size (Bits)	Capacity
Main Data	MOS	38	8, 16, 32, or 64K words
Program Source	RAM	64	1K or 4K words
Table Memory	ROM	38	2.5K or 4.5K
Table Memory	RAM	38	Optional, 4K or 8K words

Arithmetic Operation

Floating Point

Floating Point
Data Width: 38-bits
Operation: Pipeline, internally synchronous parallel processing
Floating Point Add: Every 250nsec, 500nsec for completion
Floating Point Multiply: Every 250nsec, 750nsec for completion
Accuracy: Maximum relative error of 7.5×10^{-9} per arithmetic operation or precision of 8.1 decimal digits

Integer

Integer Width: 16-bits
Operation: Immediate synchronous parallel processing

Interrupts

The priority interrupt structure consists of 3 unique internal levels and 15 external interrupts. Each may be individually controlled, enabled/disabled.

Internal: Trap • Supervisor call
SRS • Subroutine stack overflow
Exception • Floating Point overflow, underflow, divide by zero
External: 15 I/O • 1 used by real-time clock
• 2 used by host interface
• 12 user defined

Real-Time Clock

The real-time clock is fully programmable from 1μsec to 16.38msec/count in fifteen discrete timing intervals. Additionally, three registers associated with the clock are user addressable: clock counter, clock count set, and clock control. An external clock source may be used; clock interrupts are generated by the FPS-100.

Software

To aid the user in the development and execution of real-time programs, the FPS-100 offers three distinct categories of software:

- Systems Software
- Program Development Software
- Applications Software

Systems Software

Super-100

The FPS-100 multitasking operating system (Super 100) provides a complete operating environment in which to execute real-time programs. Processor time allocation, programmed processing services, inter-task synchronization and communication, plus simplified uniform asynchronous I/O services are highlights of the Super 100 operating system.

RTS

RTS, the Real-Time Supervisor, is tailored for those applications requiring interrupt support in small program source environments.

Host System Interface

APEX (Array Processor Executive) resides in the host computer system and provides the means of communication between the host and the FPS-100. Operating systems of leading minicomputer suppliers are supported by FPS-100 software packages.

Program Development Software

Languages

- Vector Function Chainer
A special language which streamlines the use of library routines.
- Assembler
The FPS-100 processor assembly language.

Development Aids

- FPS-100 Simulator
Takes generated routines and uses the host to simulate array processor execution.
- FPS-100 Debugger
Completely debugs array processor routines by detecting and locating program errors on the arithmetic processor

Applications Software

- Standard Math Library
Consists of 225 math routines covering simple vector addition to complete Fast Fourier Transformation (FFT)
- Advanced Math Library
Advanced math routines covering function generation, integration, Eigenvalue/Eigenvalues and specialized matrix routines.
- Signal Processing Library
Supplements the math library with unique signal processing routines, including histogram analysis, window functions and spectral averaging.
- Image Processing Library
The library contains filtering, convolution and Fast Fourier Transform (FFT) routines needed to filter and enhance monochrome color and scanner images.

- Test and Verification Software (TVS)
Test and Verification Software performs complete testing of the array processor's internal structure and the host array processor interface.

Configurations

Basic

FPS-100 standard configurations are implemented in a 15-slot, 10½" chassis including power supplies, control panel, and standard 19" rack mounting hardware. Included are:

- FPS-100 Array Processor
- Program source memory, 1K words
- Table memory, ROM, 2.5K words
- Main data memory, 8K, 16K, 32K, or 64K words

Options

Processor Options

Real-Time Option

The real-time option consists of the real-time clock and priority interrupts.

- | | |
|---------------------|---|
| Priority Interrupts | • Provides priority interrupt structure, 3 internal, 15 external interrupts |
| Real-time Clock | • Programmable, 1μsec to 16.38msec, 15 intervals |

I/O Expansion Chassis

A chassis which provides 10 additional I/O slots for system expansion. Power is supplied by main chassis.

Memory

Main Data Memory

Main Data Memory is upgradeable to a maximum of 64K words.

Table Memory

Table Memory is available in 2.5K or 4.5K ROM and 4K or 8K RAM.

Program Memory

Program Memory is available in 1K or 4K words.

Mass Storage

- | | |
|---------|--|
| DSK 80 | • Eighty (80) M Byte storage module disk with programmable I/O processor, formatter, and control software. |
| DSK 300 | • Three hundred (300) M Byte storage module disk with programmable I/O processor, formatter, and control software. |

Computer Interfaces

- Digital Equipment Corp. PDP-11 Series (Unibus®).
- Data General Nova or Eclipse
- Factory quote available on request for other interfaces

FLOATING POINT SYSTEMS, INC.
CALL TOLL FREE 800-547-1445
P.O. Box 23489, Portland, Oregon 97223
(503) 841-8151, TLX. 360475 FLOATPOINT PTL
In Europe & U.K. Floating Point Systems SA Ltd
100, rue de la Woluwe, 1200 Brussels, Belgium
(32) 280543, TLX. (945) 28870 FPSE CH

Input/Output Interfaces

The following interfaces allow the user to implement real-time data transfer to and from the FPS-100.

- IOP-16 General purpose 16-bit interface 1.0 megawords/sec AP input, .8 megawords/sec AP output*.
- IOP-38 General purpose 38-bit interface 1.0 megawords/sec AP input, .8 megawords/sec AP output*.
- GPIOP General purpose programmable I/O processor 1.9 megawords/sec data rate**.

*Average transfer rate

**Maximum transfer rate

Performance

Algorithm	Execution Times (ms)
1024 pt. real FFT	4.00
4096 pt. real FFT	18.80
256 × 256 2D real FFT	589.82
1024 × 32 pt. convolution	9.90
1000 element vector square root	2.77
1000 element dot product	.75
100 × 100 matrix inverse	1766.00

Environmental

Electrical

Voltage (a.c.)	120 ± 10%	220 ± 10%
Current (max):		
Standard chassis	8.40A	4.40A
Standard + I/O	14.60A	8.25A
NEMA Plug	5-20P	6-15P
Frequency:	47-63Hz	
Power Factor:	0.7 approx.	
Meets U.L. 478		

Temperature

Operating:	10° to 40°C
Storage:	-40° to 65°C

Humidity

Relative Humidity range: 0-90% non-condensing

Physical

Standard Chassis

Dimension: 10½" × 19" × 24" • 26.67 × 48.26 × 60.96 cm.

Weight: 93 lbs. including power supplies • 42.27 Kg.

I/O Chassis

Dimension: 8¾" × 19" × 24" • 22.23 × 48.26 × 60.96 cm.

Weight: 20 lbs. (not implemented) • 9.0 Kg.

Cooling

Standard Chassis: 300 CFM
With I/O Chassis: 500 CFM

Heat Dissipation:

Standard Plus I/O: 1500 BTU/HR max

FPS SCIENTIFIC COMPUTERS. ACCESSIBLE SUPERCOMPUTING FOR CLASSIFIED ENVIRONMENTS.

Ever since Floating Point Systems introduced the first members of its scientific computer family, defense contractors have benefited from their capacity to make supercomputing affordable on a single-project or single-unit basis.

Thanks to their size, accessibility and price, FPS Scientific Computers are ideal systems for secure sites. Yet there is no compromise in required computing power: even the largest numerically intensive FORTRAN programs can be run on an FPS computer. Each incorporates advanced, parallel pipelined processors, with peak speeds ranging from 11 to 341 million floating point operations per second (MFLOPS).

Base configuration pricing for the FPS Scientific Computer Family ranges from \$310,000 to \$650,000—making supercomputing speed economically feasible, as well as physically practical, for sites where it never was before.

Strategic Benefits

FPS Scientific Computers demand no special environmental considerations—neither unusual power requirements nor the extravagant cooling of traditional supercomputers.

Removable disks and memory clearing routines ensure comprehensive protection of sensitive programs and data.

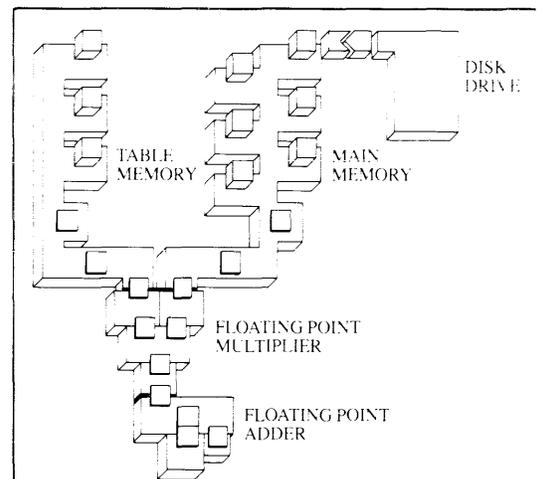
Performance Benefits

Accessibility. Numerically-intensive computation is available on-site. On demand. Without waiting in queue. Without timeshare costs. Without tying up your general-purpose computer with supercomputer tasks.

Configurability. Three computers, each highly flexible and expandable, let you fit performance to the job. As you initiate new projects, you can reconfigure your computer accordingly.

Compatibility. The FPS FORTRAN Compiler optimizes standard FORTRAN code to the family's parallel-pipelined architecture in a form that is nearly as efficient as hand-coded assembly language.

Accuracy. All three FPS computers incorporate a full 64-bit architecture. Registers, memory locations and data paths all use a 64-bit word length to produce the precision (15 decimal digits) demanded for scientific calculation without paying a performance penalty for that accuracy.



Pipelining is key to the FPS family's high-speed performance and to its inherent flexibility. The arithmetic units and memories are organized as "assembly lines" which can initiate multiple commands within each clock cycle. These assembly lines can be connected together in various combinations under software control, allowing users to customize their own vector operations instead of being restricted to a small set of vector instructions.

Utility. FPS offers one of the largest libraries of matrix algebra, general mathematics and statistics of its kind. These include the popular Boeing Computer Services Library and the Fast Matrix Solution Library, which was developed and optimized specifically for the FPS Scientific Computer Family. These libraries, plus one of the best selections of third-party applications software, help you put your FPS computer into action quickly.

Dependability. FPS brings to bear some 15 years of computer support and service. Diagnostics, training, and documentation are proven to rank with the best.

The Family

The Floating Point Systems computer family currently includes:

The FPS-164. An 11 MFLOPS peak speed scalar machine with multiple pipelined units. Performs both full matrix and sparse matrix operations without major code restructuring. Standard configuration includes 256K words of memory, with main memory expandable to 7.25 Mwords. A fully-functional configuration starts at \$310,000.

The FPS-164/MAX. Configurable via as many as 15 special matrix algebra accelerator (MAX) modules to achieve peak performance from 33 to 341 MFLOPS on a set of commonly used matrix operations. The FPS-164/MAX can run many of these computations as fast or faster than supercomputers costing many times more to purchase and operate. Standard base configuration starts at about \$440,000.

The FPS-264. The newest FPS Scientific Computer, rated at 38 MFLOPS, achieves 4-5 times the speed of the FPS-164 on many applications. It is the best choice for conventionally-written FORTRAN programs (in contrast to optimized code tailored specifically for the FPS-164/MAX). Base configurations start at \$640,000.

Disk Subsystems

Storage capacity can be configured to accommodate the data required for the largest and most intensive programs. The new RD64 Disk Subsystem employs as many as four 300 Megabyte *removable* disk drives per controller, with a maximum of six controllers per system.

That's as much as 7,200 Megabytes of secure disk storage obtainable for permanent or scratch files on any FPS system.

Front-end Computers

The FPS Scientific Computer Family is currently compatible with:

- Digital Equipment Corporation VAX[®] 11/780, 750 and 730 Series systems operating under VMS (UNIBUS Channel).
- IBM 370, 303X, 308X and 43xx systems operating under MVS and VM/CMS (Block Multiplexor Channel).
- Apollo DOMAIN Series.
- Sperry 1100 Series.

In addition, you can depend on Floating Point Systems to support new computer systems with compatible interfacing promptly and expertly.

Software Tools

The System Job Executive (SJE) operating system supports interactive, multi-user and batch processing. Capabilities include job management commands, permanent and scratch file management supporting FORTRAN-77 I/O, and run-time overlays.

The FPS optimizing FORTRAN-77 Compiler lets you adapt code to the FPS pipelined architecture quickly and efficiently, without understanding the architecture itself. It includes extensions for asynchronous I/O and for enhancing compatibility with other compilers.

The Overlay Linker permits execution of programs whose memory requirements exceed available system memory. Overlay transfers execute automatically from the FPS-RD64 Disk Subsystem according to a user-defined overlay structure.

Other tools include an assembler, object librarian, interactive debugger—plus extensive subroutine libraries and extensive third-party solutions software.

Applications

The FPS Family is a proven effective performer in meeting the challenges of structural analysis, computational fluid dynamics, electro-magnetic modeling, electronic circuit design and many other computationally intensive tasks called for by today's defense technologies.

For specific information and consultation, call 1-800-547-1445, Ext. 1467 or Ext. 1734. Or contact your Floating Point Systems representative.

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Floating Point Systems knows that finding a scientific computer to meet the diverse requirements of today's classified projects can be a challenge. Supercomputer performance has become a necessity for many defense-related applications, yet price and installation requirements have made traditional supercomputer selections impractical for such projects.

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