GEK 36010

GE-PAC® 30
CONTROL COMPUTER

INSTRUCTION MANUAL
SYSTEM TEST SET

GENERAL ELECTRIC

SYSTEM TEST SET INSTRUCTION MANUAL

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SYSTEM TEST SET INSTRUCTION MANUAL

1. INTRODUCTION

The GE-PAC 30 System Test Set (often referred to as a Test Set) is a maintenance test device which permits manual control of a GE-PAC 30 Digital System. Indicators on the Test Set display the contents of all pertinent registers and buses within the system. The System Test Set may be used in maintaining systems with standard Read-Only-Memories (ROMs), and is required if a special maintenance ROM (X-Ray ROM) is used. The plug-in X-Ray ROM is substituted for the normal ROM in the system under test. X-Ray ROM details are provided in separate publications. The System Test Set or System Test Set/X-Ray ROM combination permits rapid check-out and/or trouble analysis of a GE-PAC 30 Digital System. The System Test Set is compatible with other GE-PAC 30 Digital Systems. Unless otherwise noted, all comments in this manual apply equally to all Digital System Models.

2. SET-UP PROCEDURE

Use the following procedure to connect the System Test Set to the Digital System.

CAUTION

Remove power from the Digital System and disconnect it from its power source before proceeding.

1. Carefully remove the cable assemblies from their storage compartment in the System Test Set.
2. Connect the P1 through P3 cable connectors to the J1 through J3 connectors on the rear of the Test Set. Refer to Figure 1.
3. Connect the other end of the cables to the back panel of the Digital System. Refer to Figure 1.
4. The System Test Set derives its power from the Digital System. Connect the power cable as follows:

Voltage	Wire Color	Location[1]	Use
+15	Orange	TB4-2	Memory Voltage Reference
+ 5	Red	TB5-3	Lamp Supply
GRD	Black	TB5-6	Lamp Ground

5. Clip the final lead (used for the memory threshold adjustment) to the back panel as follows:

GE-PAC 30-1 and -2 - **119-ME1-0**
(Back panel pin 119,0 Field, ME1 board)

6. Check that all connectors are mated properly and apply power to the system.

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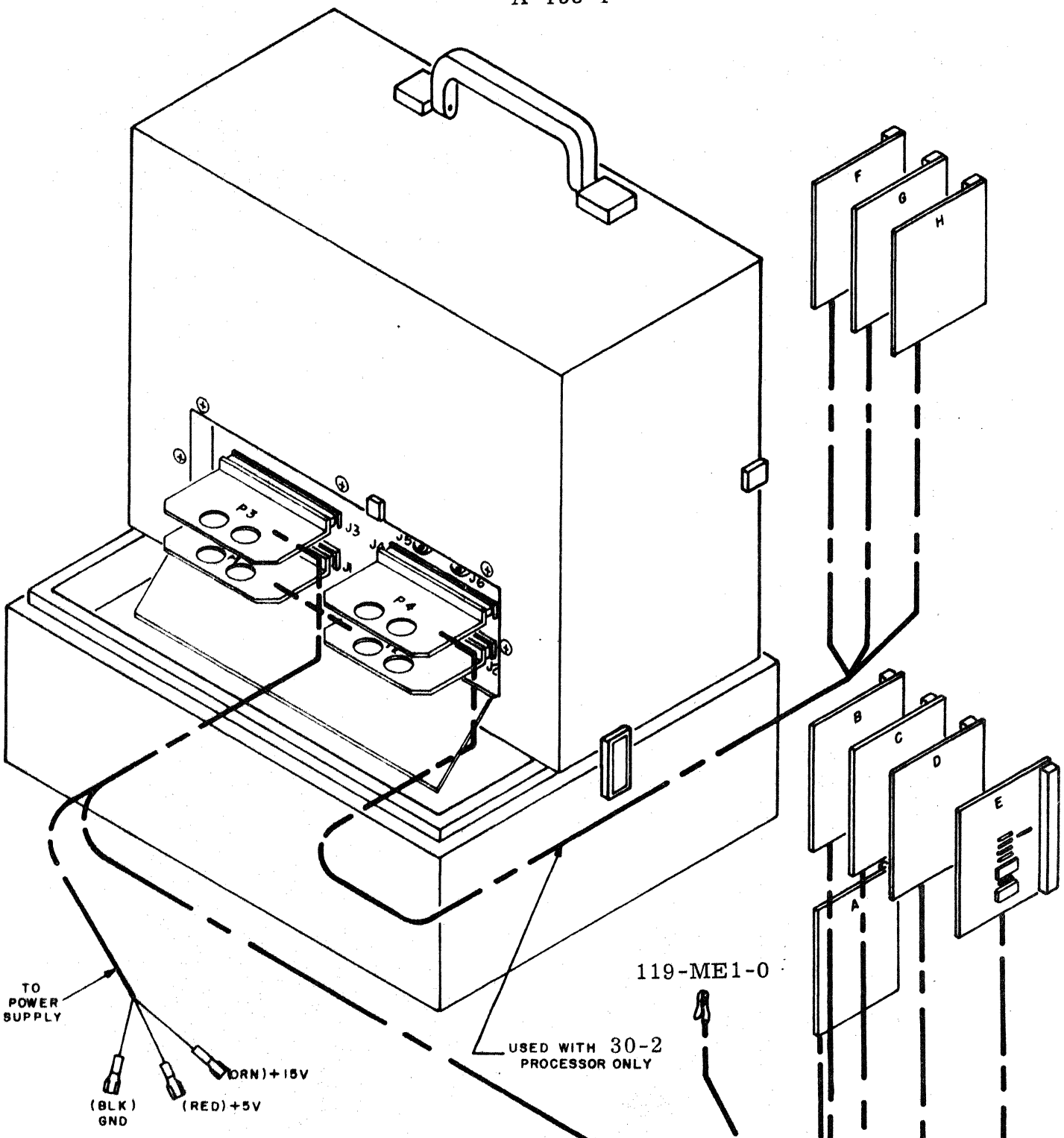
1. The locations provided are on the vendor power supply. If a GE-PAC 30 power supply is provided with the system, use points on the back panel. The supply voltages are marked on the back panel.



MODEL	CONNECTOR A	B	C	D	E	F	G	H
30-01	RMI-0 ROWS 1,2	RMI-1 ROWS 1,2	BS1-1 ROWS 1,2	BS2-1 ROWS 1,2	CO2-1 ROWS 0,1	NA	NA	NA
30-02 (WW)	RMI-0 ROWS 1,2	RMI-1 ROWS 1,2	BS3-1 ROWS 1,2	BS2-1 ROWS 1,2	CO1-1 ROWS 0,1	CO2-1 ROWS 1,2	BS0-1 ROWS 1,2	BS1-1 ROWS 1,2
30-02 (CU)	RMI-0 ROWS 1,2	RMI-1 ROWS 1,2	BS3-1 ROWS 1,2	BS2-1 ROWS 1,2	CO0-1 ROWS 0,1	CO1-1 ROWS 1,2	BS0-1 ROWS 1,2	BS1-1 ROWS 1,2

Figure 1. System Test Set Cabling

3. CONTROLS, INDICATORS AND JACKS

Each of the controls and indicators on the System Test Set control panel is described in the following paragraphs. Refer to Figure 2.

3.1 Controls

MEM VOLT — The MEMory VOLTage potentiometer is used to vary the bias in the core memory. The potentiometer is connected only when the MEM Switch is depressed.

EXT CLK — The EXTernal CLocK potentiometer is used to vary the frequency of a test clock which may be substituted for the system clock. The potentiometer is connected only when the EXT Switch is depressed.

MEM — When depressed, the MEMory Switch enables the MEM VOLT potentiometer which is used to test the bias margins in the core memory. This switch should normally be released - if not, marginal core memory operation may result.

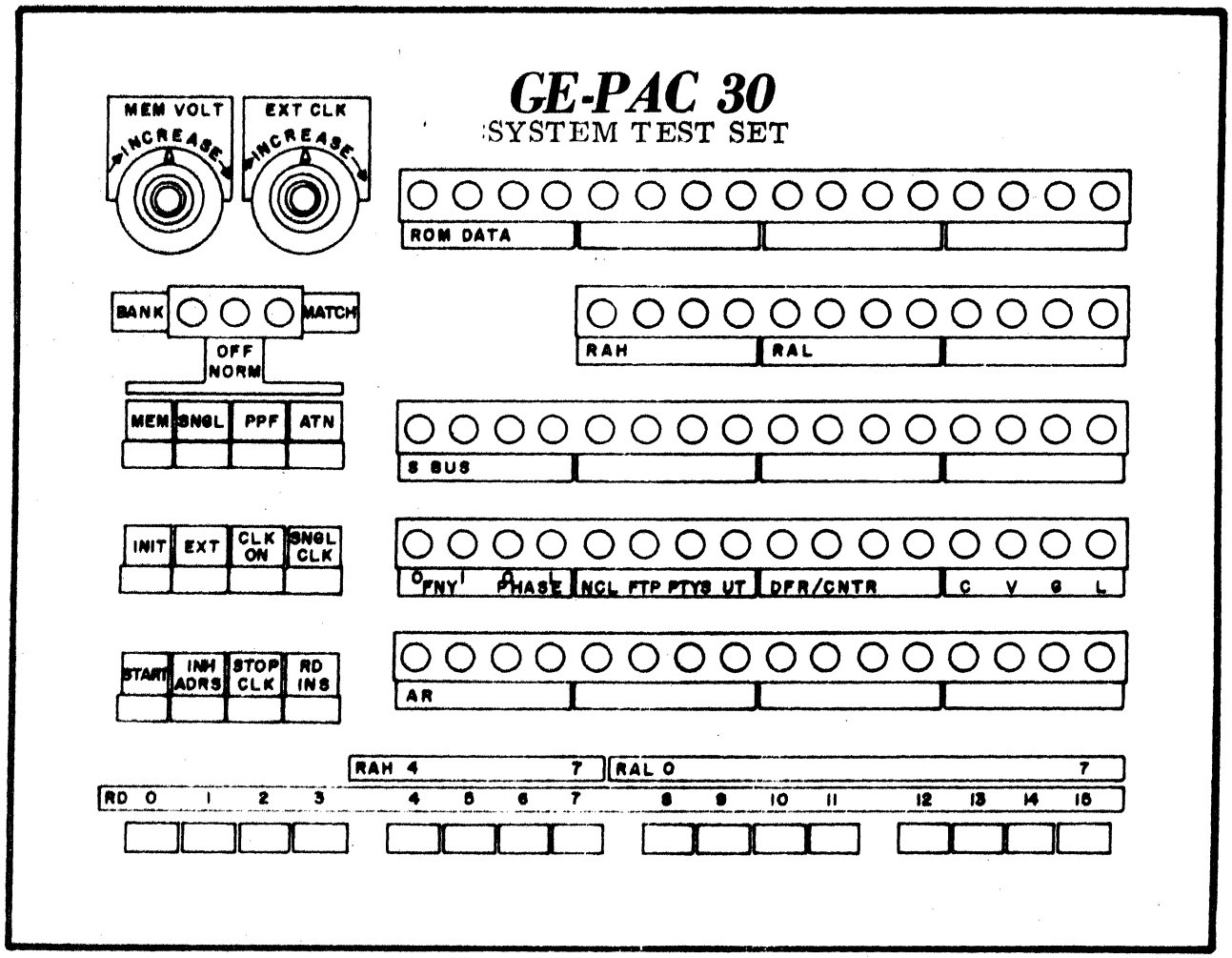


Figure 2. Control Panel Layout

ATN, PPF, and SNGL — These switches are used as sense switches for the X-Ray. (See Section 4.) If an X-Ray ROM is not in place in the computer, these switches should all be released. The OFF NORMal lamp lights if any are depressed.

INIT — The INITialize Switch performs the same function as the INITIALIZE Switch on the front panel, the Initialize relay in the Processor is released. This stops the clock momentarily, and clears the ROM address register and other flip-flops in the system.

EXT — When depressed, the EXTernal Switch enables the clock frequency to be controlled by the EXT CLK potentiometer. If the switch is released, the crystal-controlled clock in the Processor is enabled. This switch should not be operated while the clock is running.

CLK ON — Depressing the CLocK ON Switch, followed by depressing START, causes the system clock to run. The clock may be stopped by releasing the CLocK ON Switch, or on an address match when STOP CLocK is depressed.

SNGL CLK — If the clock is off, depressing the SiNGLe CLocK Switch generates a single clock pulse, to execute one micro-instruction at a time.

START — Depressing the START Switch permits the clock to start running if CLK ON is depressed. The first micro-instruction to be executed is the instruction currently in the ROM data register.

INH ADRS — Depressing the INHibit ADdReSs Switch stops the ROM address register clock when the Data Switches match the ROM address. Note that the Processor clock is still running and ROM readouts are still strobed into the ROM DATA register even though the ROM address register clock is stopped. This micro-instruction will be executed repeatedly.

STOP CLK — Depressing the STOP CLocK Switch enables a continuous match between the ROM address register and the 12 least significant bits of the Data Switches. The Processor clock is stopped when a match is detected.

RD INS — Operation of the Read INStruction momentary Switch causes the contents of the Data Switches to be loaded into the ROM DATA Register. This may be observed on the ROM DATA lamps. The switch is disabled when the clock is running, i.e. CLK ON depressed.

Data Switches — These 16 Data Switches, across the bottom of the panel, are used to perform a dual function:

1. The data set into these switches is inserted into the ROM DATA Register when RD INS is depressed with the clock stopped.

- or -

2. The right-most 12 bits may be used as a constant to match against the ROM address register.

3.2 Indicators

The indicators light when the associated bit of flip-flop is set.

ROM DATA — The 16 ROM DATA lamps indicate the contents of the last address read from the ROM.

BANK — Indicates the state of the Bank flip-flop in 30-1 or 30-2 Digital Systems.

OFF NORMAL — Indicates that a least one of the following switches are depressed: MEM, SNGL, PPF, or ATN.

MATCH — Indicates a match condition between the 12-bit ROM Address Register (RAH and RAL) and 12 Right-most Data Switches.

RAH — These lamps monitor the 4 most significant bits of the second rank of the ROM Address Register.

RAL — These lamps monitor the 8 least significant bits of ROM Address Register. Ordinarily, these lamps display the address of the next instruction to be executed.

S BUS — Indicates the contents of the S Bus. For the 30-1, only the right-most 8 bits are applicable. For the 30-2, all bits are used.

DFR/IF — For the 30-1, the right-most 8 bits display the contents of DFR. For the 30-2, the right-most 4 bits display the contents of the Flag Register; C, V, G, and L. The next 4 bits display the state of the Counter Register.

The remaining 8 bits in this row of lamps are used for 30-2 Systems only. Eight flip-flops are displayed as indicated on the display panel.

AR — Indicates the contents of the AR. For the 30-1, only the right-most 8 bits are applicable. For the 30-2, all 16 bits are used.

3.3 Jacks

J5 — BNC connector for Scope Sync. · The output of J5 is ground when there is a match of ROM Address and the right-most 12 Data Switches.

J6 — BNC connector. Output of J6 is CLOD inverted three times.

4. OPERATING PROCEDURES

The following procedures assume that an X-Ray ROM is used in conjunction with the Test Set.

4.1 Initial Start-Up

1. Connect the Systems Test Set as outlined in Section 2.
2. Before power is applied to the system, carefully remove the ROM mother-board and substitute the X-Ray ROM.
3. Slide the Display Controller mother-board out of the card file far enough to disconnect the back panel connectors. It is not necessary to remove the cables from the front of the Display Controller.
4. Release all switches on the Test Set except CLK ON. Depress CLK ON.
5. Turn the Digital System power on.
6. Depress the momentary START Switch. This starts the X-Ray running.

4.2 ROM Program Execution

The ROM program may be started at any address by using the following procedure to load the starting address of the ROM subroutine into the ROM Address Register.

1. Release the CLK ON Switch to stop the system clock.
2. Depress INIT to initialize the system.
3. For 30-1, insert X'5D' (Load RAH) on Data Switches 0 through 7. For 30-2, insert X'5O' on Data Switches 0 thru 7.
4. Set Data Switches 8 through 15 to the desired RAH address.
5. Depress the RD INS pushbutton and the SNGL CLK pushbutton to load the RAH Master Register.
6. For 30-1, insert X'5E' (Load RAL) on Data Switches 0 through 7. For 30-2, insert X'51' on Data Switches thru 7.
7. Set Data Switches 8 through 15 to the desired RAL address.
8. Depress the RD INS pushbutton and the SNGL CLK pushbutton to load the RAL Register and the RAH Slave Register. The starting address is now displayed on the RAH and RAL indicators.
9. Depress SNGL CLK. The system fetches the micro-instruction at the selected address and executes that instruction.

The system may be stepped through each micro-instruction by continuing to depress SNGL CLK, or CLK ON may be depressed to run the micro-program at normal speed.

4.3 Address Match

The System Test Set permits halting the system in either of two modes when the micro-program reaches a designated address. If an address is selected and STOP CLK is depressed, the system executes the instruction at the selected address, and then fetches the next instruction, but does not execute it. If, instead of STOP CLK, INH ADRS is depressed, the ROM Address Register is frozen at the selected address and the instruction at that address is executed repeatedly. Use the following procedure for address matching:

1. Set the desired match address on the Data Switches.

   NOTE

   Do not select an address at which the ROM micro-instruction is a Load RAL or an executed Branch.

2. Depress STOP CLK or INH ADRS depending upon the mode of the operation desired.

3. Resume operation after a match by simply releasing INH ADRS, or by releasing STOP CLK and depressing START.

4.4 X-Ray Control

When running the X-Ray ROM program, it is often desirable to have the program continously loop through certain tests, or to loop through all X-Rays and only stop on errors. This is accomplished by using the PPF, ATN, and SNGL Switches as sense switches which are interrogated by the X-Ray program after a set of tests. The function of each switch is:

1. SNGL - When SNGL is released, it grounds AUTOLD1. The X-Ray continously loops through the Processor X-Rays and the Memory X-Ray.

   When SNGL is depressed, the X-Ray ROM loops in the Wait loop after each set of tests.

2. ATN - When ATN is depressed, it grounds ATN0. The X-Ray loops in one set of tests. The operator selects the particular set of tests by stepping the system through the X-Rays with the EXECUTE pushbutton. Just prior to executing the test to be repeated, the ATN pushbutton is depressed.

3. PPF - If the PPF Switch is depressed, it grounds PPF0. The micro-program loops in the Wait loop if the X-Ray detects an error. The AR indicators also display an error pointer code at this time.

If the program is looping in the Wait loop as a result of the PPF and/or SNGL Switches, the program may be continued by depressing the EXECUTE pushbutton on the Display Panel twice.

The previous descriptions of the SNGL, ATN, and PPF Switch operation are applicable for the Processor X-Rays

(START 0 through START 6), and for the Memory X-Ray (START 10). The START 7 X-Ray tests the Primary Power Fail circuit and the False Sync logic. During START 7, the SNGL, ATN, and PPF Switches have a different significance. To begin execution of the START 7 X-Ray, depress PPF and then INIT. If the SNGL Switch is depressed, the program loops at the end of the test (though not in the Wait loop). If the SNGL Switch is released, the micro-program continously repeats START 7.

4.5 Core Memory Marginal Test

Use the following procedure to determine the core memory threshold margins:

1. Continously loop through the START 10 X-Ray with the PPF Switch depressed to assure that no errors are detected.

2. Connect a voltmeter between ground and the VT testpoint on the Digital System back panel (pin 211-1 of MEM0 or MEM1).

3. Set the MEM VOLT potentiometer to its mid position and depress the MEM Switch.

4. Vary the MEM VOLT potentiometer to obtain readings from 3 volts to 5 volts. If the Memory X-Ray fails between these limits, the memory requires adjustment or repair. Refer to the Memory Section of the Digital System Maintenance Manual.

4.6 System Clock Marginal Test

If a trouble exists in the system, and it is suspected that the problem is related to speed, the variable clock on the System Test Set may be used as an aid to isolate the problem.

Use the following procedure to employ this feature.

1. Monitor the CD0 test point on the Digital System back panel with an oscilloscope.

2. Start the X-Ray running through all Processor tests, SNGL and ATN Switches released, PPF Switch depressed.

3. Release CLK ON, and PPF.

4. Turn the EXT CLK potentiometer fully counter-clockwise.

5. Operate the EXT, CLK ON, INIT, and PPF Switches.

When START is operated, the X-Ray program runs with the clock at approximately .2MHZ. If the program runs at this speed, increase the clock speed in discrete steps until a failure occurs. Five or ten seconds should be allowed between each setting to insure that the X-Ray completes at least 1 cycle.

NOTE

The clock in the Test Set is variable over a wide range and can be adjusted to be much faster than the computer crystal frequency. The crystal frequency should not be exceeded by more than 10% when running this test. The X-Rays should normally be run with the EXT Switch released.

5. FUNCTIONAL DESCRIPTION

The following description refers to the

ten sheet System Test Set schematic provided in Appendix 1 at the rear of this manual (70B113927).

Sheet 1 of the schematic shows the A Section of each of the Data/Address switches on the bottom of the System Test Set panel, and the interconnection of the switches to the Processor back panel. As shown on Figure 1 earlier in this manual, J1 and J2 are on the rear of the System Test Set. Connectors P1 and P2 are on the cable assemblies, while the diodes shown enclosed within dotted lines are mounted on the connectors which mate with the back panel (RMI-0 and RMI-1). Note the momentary (non-latching) Read Instruction switch contacts shown in the lower left area of Sheet 1. When RD INS Switch is depressed, the condition of switches S00 through S15 is gated into the ROM Data Register.

Sheet 2 of the schematic shows the ROM DATA lamps on the System Test Set Control Panel, and the gates which drive them. Note that there is not gating involved. Thus, the ROM Data lamps continously display the contents of the RD Register in the Digital System.

Sheet 3 shows the least significant 8 bits of the AR display and the S Bus display. Sheet 4 shows the most significant 8 bits of these displays, which are required only with 30-2 Digital Systems.

Sheet 5 shows part of the cable which is used with the 30-2. The sheet provides the Instruction Register display in such systems. Note the output from area R9 of this sheet to 6R9. This ground inhibits the inputs shown on the top right of Sheet 6.

The left half of Sheet 6 shows the RAH display logic. The four outputs to Sheet 8 are high when the RAH bit matches the corresponding S4 through S7 switch condition. For example, if S4 is depressed and RAH04 is set, the MRAH041 signal is high. The right half of Sheet 6 shows the DFR display logic if the Digital System is a 30-1 (see the preceding paragraph if the Digital System is a 30-2).

Sheet 7 shows the RAL display logic. Note that outputs to the address match logic on Sheet 8 are similar to those shown on Sheet 6 and described earlier in this Section.

The ROM address match logic is shown on the left side of Sheet 8. When the ROM address matches the configuration set in Switches 4 through 15, the output from the gate shown in area C5 goes high. This output is applied to four gates shown in area C6 through C9. Going from the top to bottom, the first gate lights the MATCH indicator on the Control Panel. If the INH ADRS Switch on the Control Panel is set, the next gate sends a signal to the Processor to inhibit incrementing the ROM address. If the STOP CLK Switch on the Control Panel is set, the output from the next gate stops the System Test Set clock (Sheet 9). The last gate provides an output to the ADD MATCH jack on the rear of the System Test Set. This output is typically used to trigger an oscilloscope at a selected ROM address.

The logic shown in the H and J area of Sheet 8 provides the Digital System clock to the CLOCK jack on the rear of the System Test Set, and to the Stop Clock gate discussed in the preceding paragraph. The PPF, ATN, and SNGL Switches are shown in areas L6 and M6. Note that in addition to supplying signals to the Processor, these three switches and the MEM Switch are ORed to light the OFF NORMAL indicator. The final circuit on Sheet 8 lights the BANK indicator when the Bank flip-flop in the 30-1 or 30-2 Processor is set.

Sheet 9 of the schematic shows the System Test Set clock and control logic. Assume first that the normal Processor internal clock is being used. In this case, the CLK ON Switch,shown in area G6, is depressed to remove the ground from IC05-10 (area C7). The CLKOFF0 signal is then forced high via gates at B7 and C2 when the START Switch at E7 is depressed. The Processor clock runs normally until a STP0 signal is received on an ROM address match, or until the CLK ON Switch is released.

If the External (System Test Set) clock is used, the EXT Switch,shown in area A8, is depressed. The normally-open contacts close to generate a CLKOFF0 signal which stops the Processor clock until EXT is released. The normally-closed contacts release the flip-flop shown in area C9. When CLK ON is depressed, followed by START, the flip-flop is set. The high output from the flip-flop enables the gate shown in area F9. The other input to the gate is the output from the external clock multivibrator circuit which is shown in the lower right area of Sheet 9. The output from the gate in area F9 generates the EXTCLK0 signal to the Processor via gates shown in areas G2 and H2. The clock continues to run at the frequency selected by the EXT CLK potentiometer shown in area M6, until the flip-flop shown in area C9 is reset. The flip-flop may be reset one of three ways: by SCLR1 from the Processor, by STP0 from Sheet 8, or by the CLK ON Switch (shown in area E6) being released. Note the SNGL CLK Switch shown in area H7. If the CLK ON Switch is released, the flip-flop shown in areas G8 and H8 is set each time the SNGL CLK Switch is depressed. The flip-flop output produces a clock pulse each time SNGL CLK is depressed.

The Initialize Switch, shown in area H6, produces a POW0 signal to the Processor each time it is depressed. The MEM VOLT potentiometer selects a memory threshold voltage which is applied to the Processor if the MEM Switch is depressed and the clip lead is installed.

6. MAINTENANCE

Maintenance on the System Test Set itself is normally restricted to the periodic replacement of indicator lamps. The lamps slip straight out from the front. It is normally possible to remove the lamp by hand. The replacement lamp, GE-PAC 30 Part Number 33-011 or Sylvania Part Number 12ESB, is simply pushed into place by hand.

If a trouble is encountered in the System Test Set, use the Functional Description provided in Section 5 and the schematics provided in Appendix 1 to locate the malfunction.

APPENDIX 1

DRAWINGS

This Appendix provides the schematic drawings necessary to maintain the System Test Set. The drawings are designated 70B113927, Sheets 1 through 10.

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE: SCHEMATIC, SYSTEM TEST SET

DRAWING NUMBER: 70B113927 | CONT. 1 | PAGE 0

FIRST MADE FOR: GEPAC-30

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				

REISSUED

A	ISSUED												

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

MADE BY: J D LIMA 10-20-71 | APPROVAL: A.P.

ISSUED: L. SHAW/JDL 10-21-71

REV.

DWG. NO. 70B113927 | CONT. 1 | PAGE 0

PRINTS TO: K7-08

PCE 2981

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE SCHEMATIC,
SYSTEM TEST SET
FMF GE-PAC 30 | FCF

DWG. NO (28-001 B08)
70B113927
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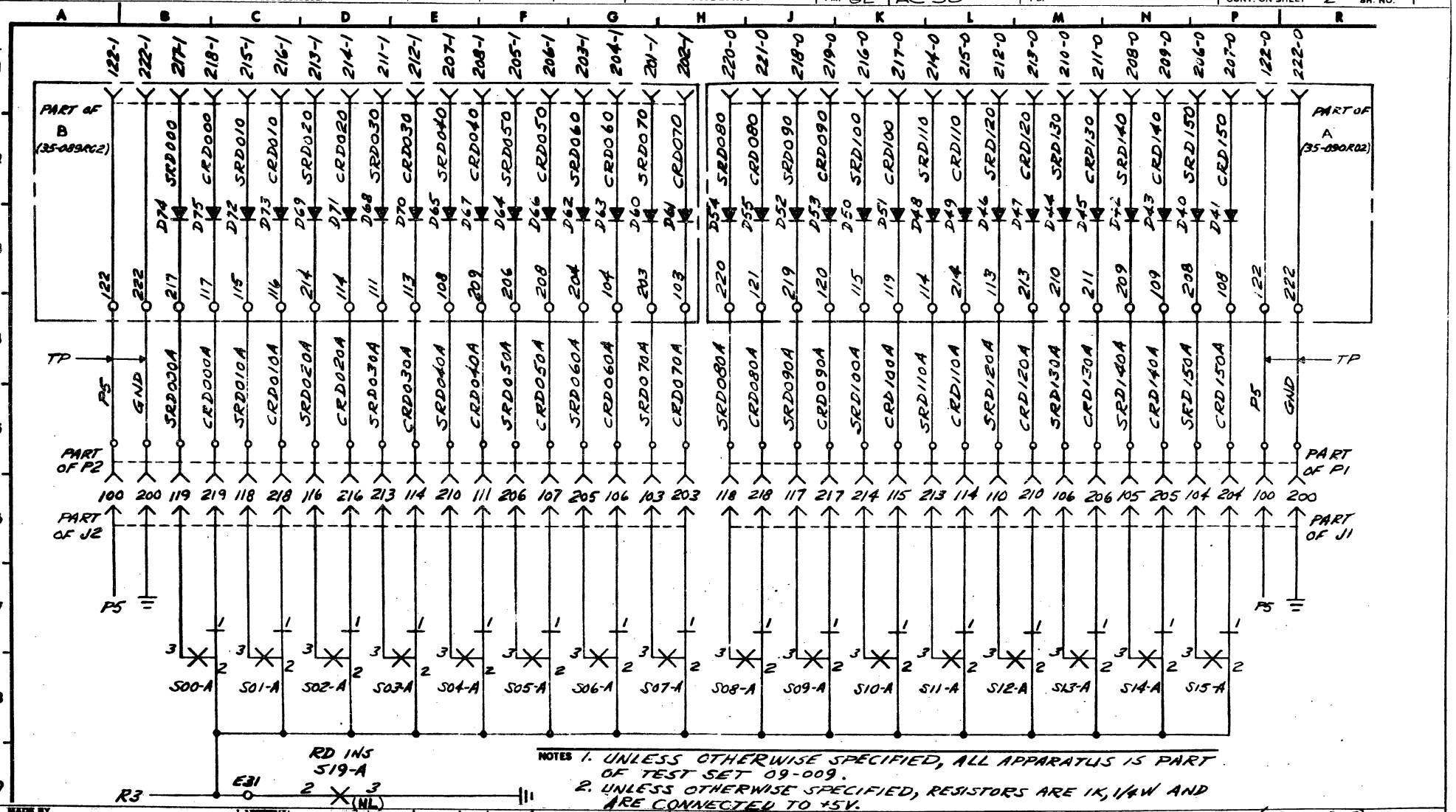

NOTES
1. UNLESS OTHERWISE SPECIFIED, ALL APPARATUS IS PART OF TEST SET 09-009.
2. UNLESS OTHERWISE SPECIFIED, RESISTORS ARE 1K, 1/4W AND ARE CONNECTED TO +5V.

MADE BY	APPROVAL	DES.	REV.	DWG. NO (28-001 B08)
J.D. LIMA 10-19-71		CHKR.		70B113927
ISSUED L SHAW/JDL 10-21-71				CONT ON SHEET 2 SH NO. 1

PC 444

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		FRACTIONS	DECIMALS	ANGLES
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GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE SCHEMATIC,
SYSTEM TEST SET
FMF GE-PAC 30 | FCF

DWG. NO. (28-001 B08) 70B113927
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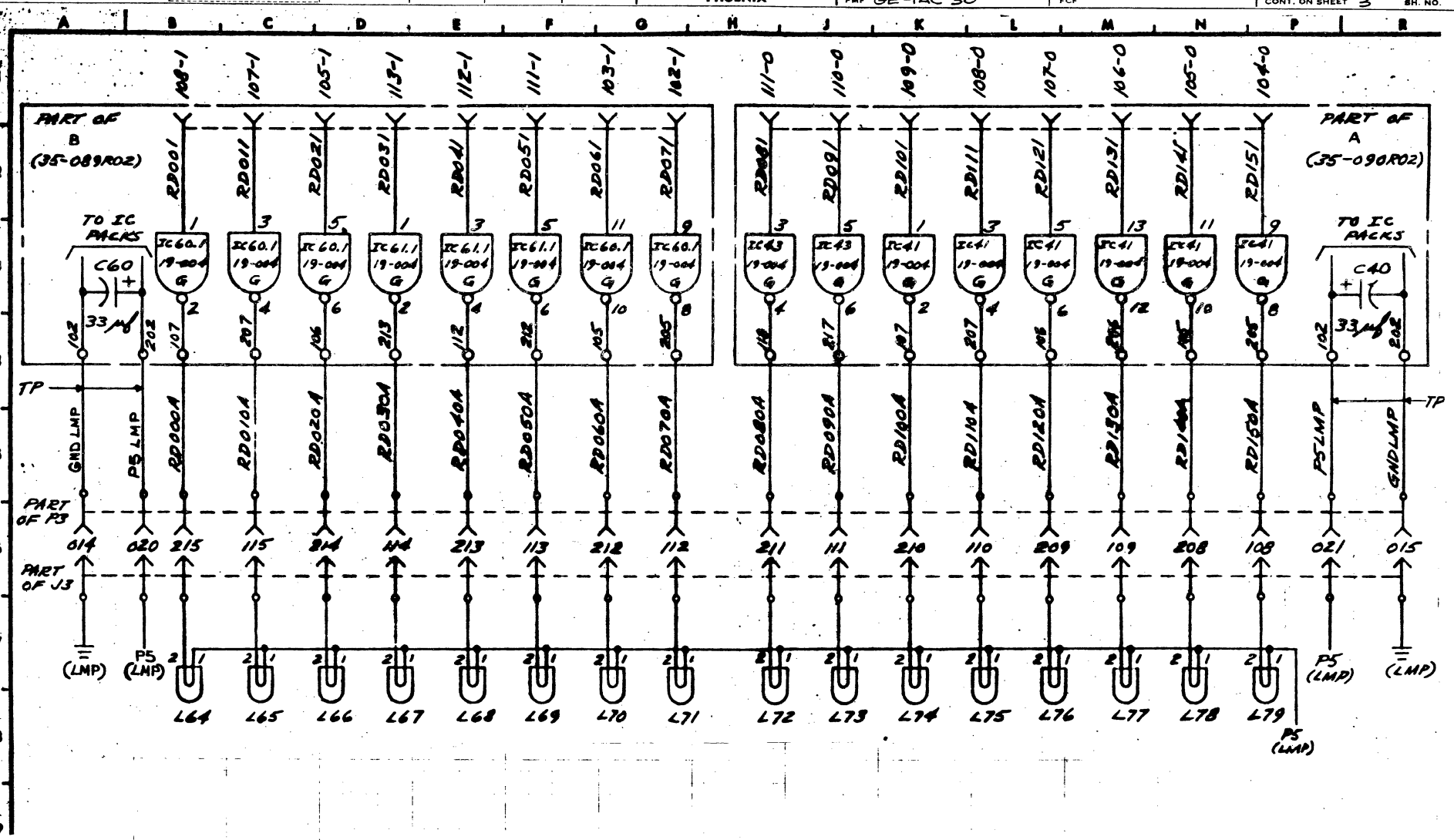

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FRACTIONS: ± DECIMALS: ± ANGLES: ±

GENERAL ELECTRIC
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PHOENIX

TITLE SCHEMATIC,
SYSTEM TEST SET
FMF GE-PAC 30 | FCF

DWG. NO. (28-001 B08)
70B113927
CONT. ON SHEET 4 SH. NO. 3

A B C D E F G H J K L M N P R

1 2 3 4 5 6 7 8 9

122-1 222-1 211-1 212-1 213-1 214-1 218-1 219-1 220-1 221-1 211-1 212-1 213-1 214-1 218-1 219-1 220-1 221-1 122-1 222-1

D (35-087R02)

C (35-097R02)

TO IC PACKS

C80.2 33μf

C80.1 33μf

TO IC PACKS

IC80.2 19-004 G

IC81.2 19-004 G

IC80.1 19-004 G

IC81.1 19-004 G

S001 (S081) S011 (S091) S021 (S101) S031 (S111) AR001 (AR081) AR011 (AR091) AR021 (AR101) AR031 (AR111)

S041 (S121) S051 (S131) S061 (S141) S071 (S151) AR041 (AR121) AR051 (AR131) AR061 (AR141) AR071 (AR151)

122 121 117 116 111 112 113 114 115 118 119 120

TP TP

PS GND PSLMP GNDLMP

S000A (S080A) S010A (S090A) S020A (S100A) S030A (S110A) AR000A (AR080A) AR010A (AR090A) AR020A (AR100A) AR030A (AR110A)

S040A (S120A) S050A (S130A) S060A (S140A) S070A (S150A) AR040A (AR120A) AR050A (AR130A) AR060A (AR140A) AR070A (AR150A)

PART OF P1 PART OF A3 PART OF P1

122 222 018 012 206 106 205 105 220 120 219 119 204 104 203 103 218 118 217 117 019 013 120 220

PART OF J1 PART OF J3 PART OF J1

2 1

L40 L41 L42 L43 L08 L09 L10 L11 L44 L45 L46 L47 L12 L13 L14 L15

PS (LMP) (LMP) PS (LMP) (LMP)

PS PS

SHEET NOTE: MNEMONIC DESIGNATIONS IN PARENTHESIS ARE FOR MODEL 30-2 USE ONLY.

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GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

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FMF: GE-PAC 30 | FCF

DWG. NO. (28-001 BOB) 70B113927
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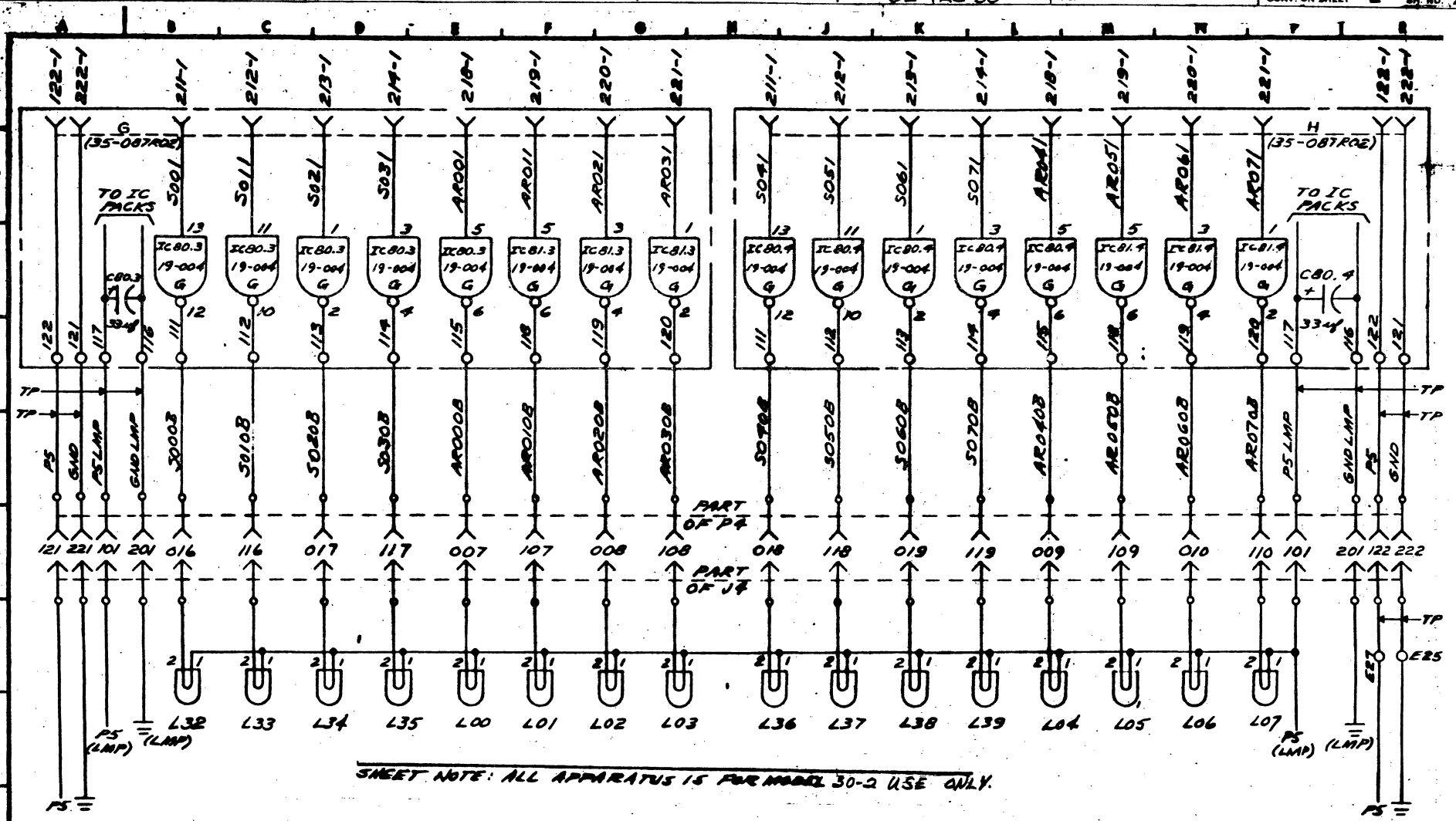

SHEET NOTE: ALL APPARATUS IS FOR MODEL 30-2 USE ONLY.

ISSUED BY	APPROVAL	ENGR.	REV.	DWG. NO.
J D LIMA 10-19-71				(28-001 BOB) 70B113927
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DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

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FMF GE-PAC 30 | FCF

DWG. NO. (28-001 B08) 70B113927
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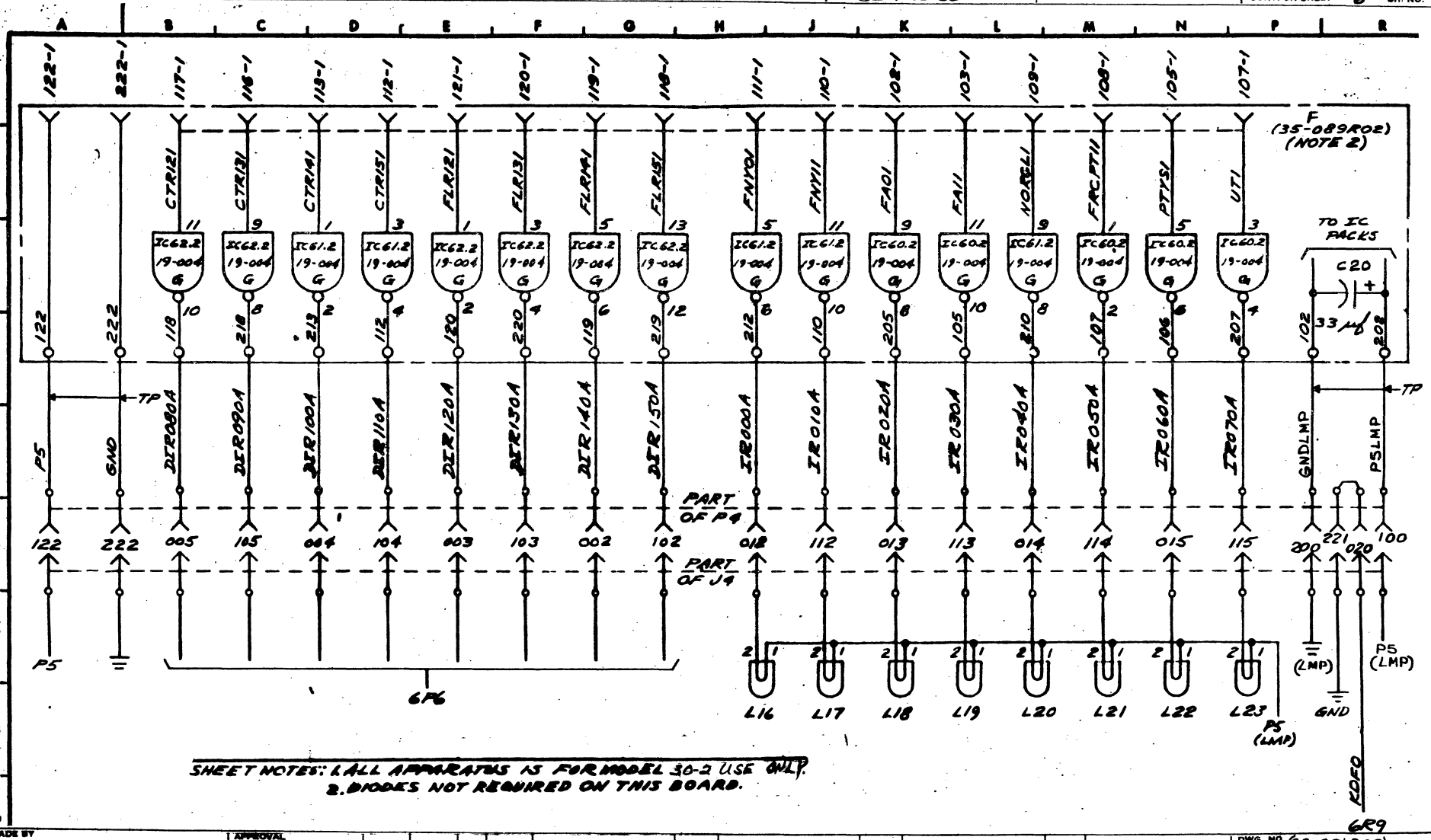

SHEET NOTES: 1. ALL APPARATUS AS FOR MODEL 30-2 USE GWLP.
2. DIODES NOT REQUIRED ON THIS BOARD.

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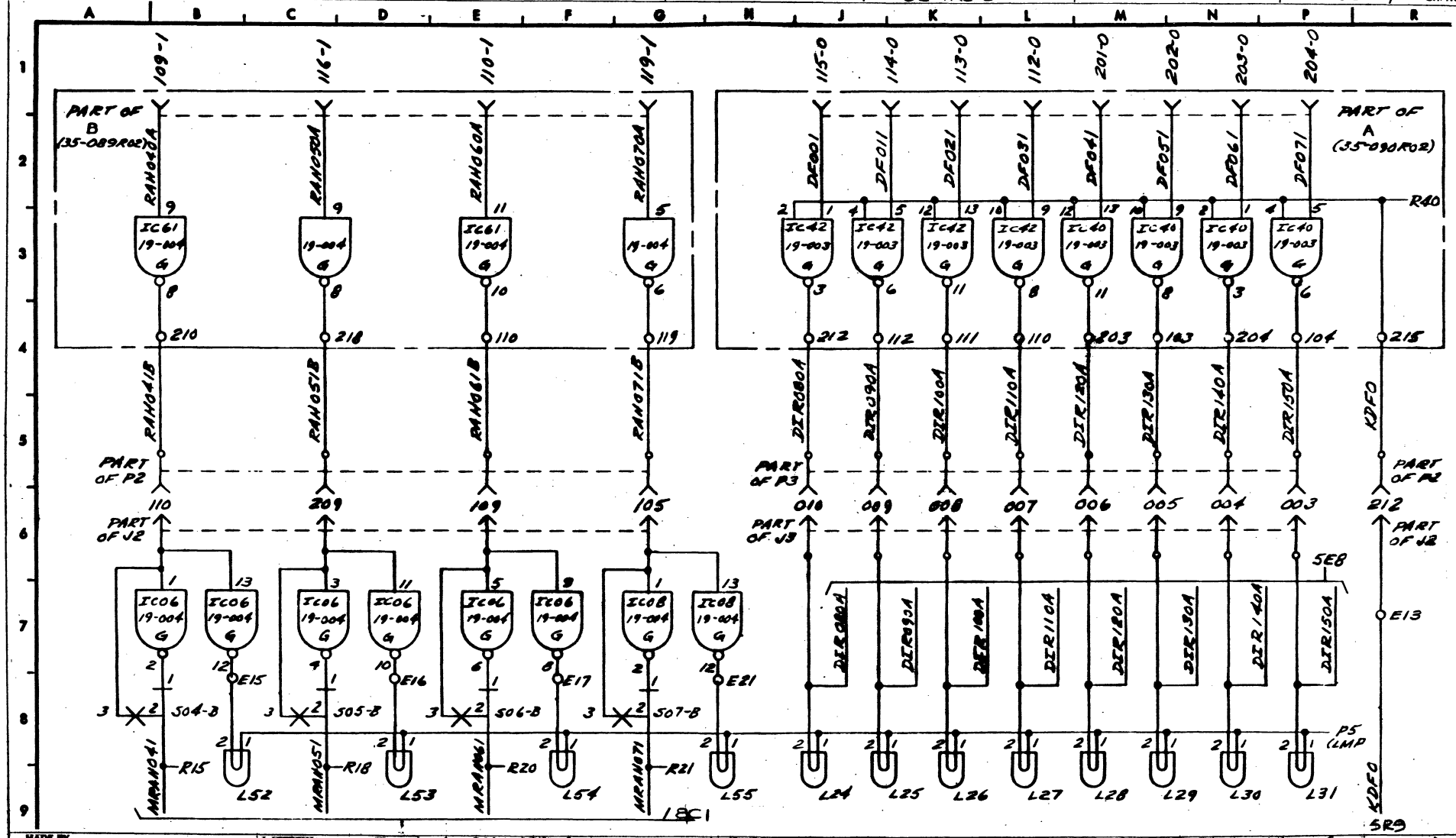
ISSUED L.SHAW/JDL 10-21-71
PC 444

APPROVAL
DES.
CHKR.
REV.

DWG. NO. (28-001 B08) 70B113927
CONT ON SHEET 6 SH NO. 5

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—					GENERAL ELECTRIC	TITLE	DWG. NO. (28-001 BOB)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS			PROCESS COMPUTER	SCHEMATIC,	70B113927
			FRACTIONS	DECIMALS	ANGLES	PHOENIX	SYSTEM TEST SET	
		√	±	±	±		FMF GE-PAC 30 | FCF	CONT. ON SHEET 7 SH. NO. 6



MADE BY	APPROVAL	DES.	REV.	DWG. NO. (28-001 BOB)
J D LIMA 10-19-71		CHKR.		70B113927
ISSUED L. SHAW/JDL 10-21-71				CONT ON SHEET 7 SH NO. 6

PC 444

DIST.

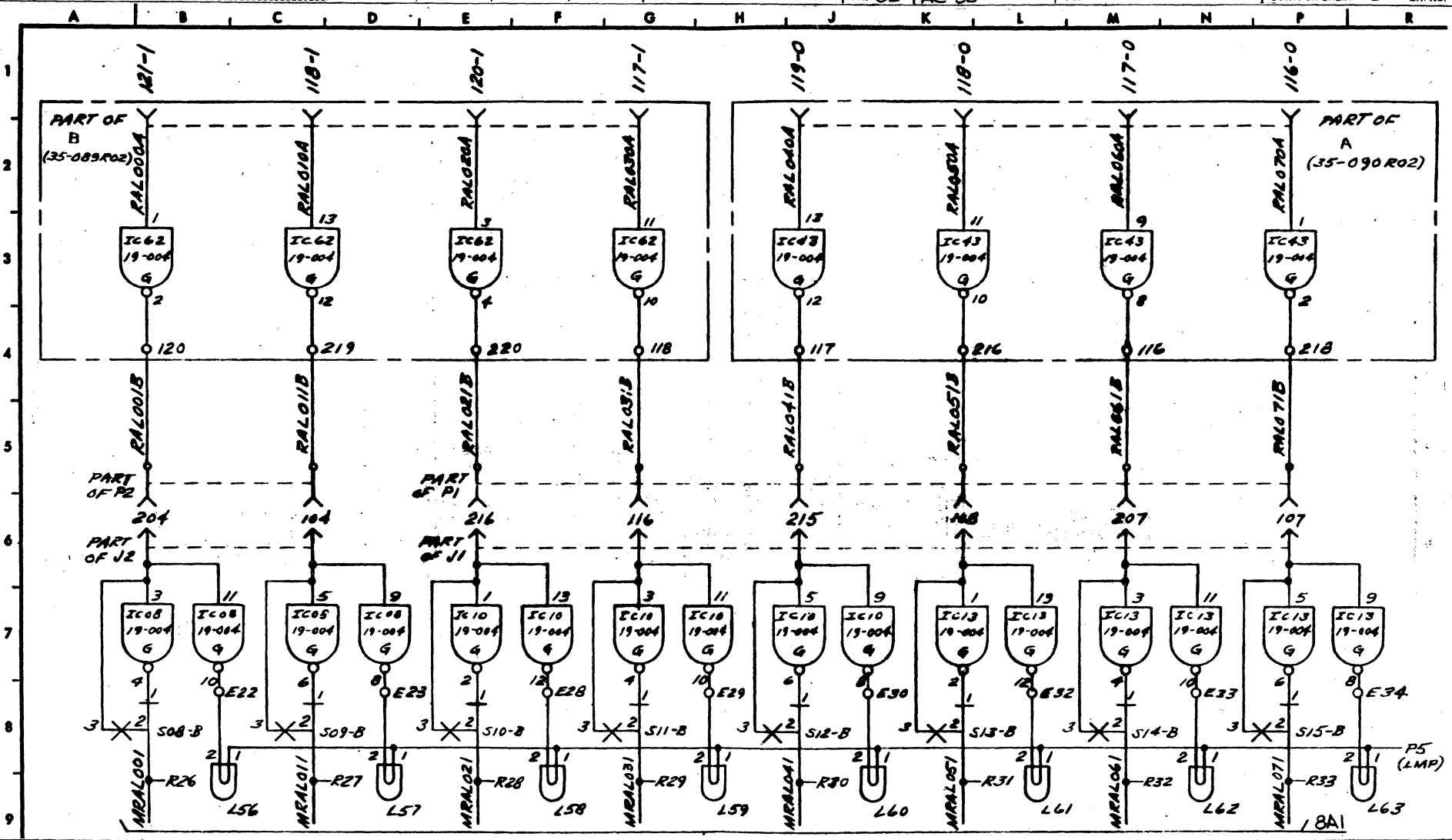
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

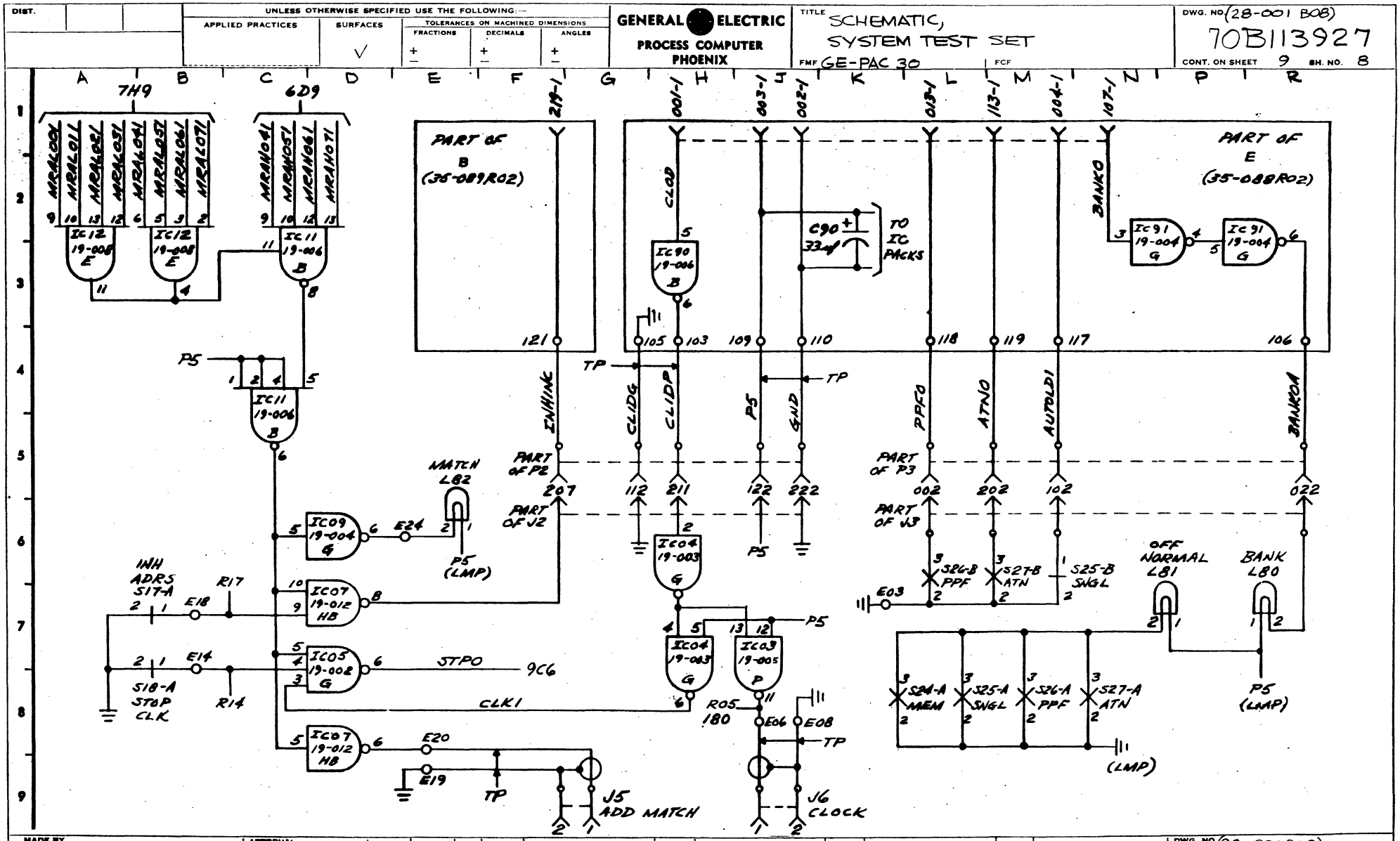
TITLE: SCHEMATIC, SYSTEM TEST SET
FMF GE-PAC 30 | FCF

DWG. NO. (28-001 B08) 70B113927
CONT. ON SHEET 8 SH. NO. 7



MADE BY	APPROVAL	DES.	REV.	DWG. NO. (28-001 B08) 70B113927
J D LIMA 10-19-21		CHKR.		CONT ON SHEET 8 SH NO. 7
ISSUED L SHAW/JDL 10-21-71				

PC 444


DIST.
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES
SURFACES
TOLERANCES ON MACHINED DIMENSIONS
FRACTIONS
DECIMALS
ANGLES
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX
TITLE SCHEMATIC, SYSTEM TEST SET
FMF GE-PAC 30
FCF
DWG. NO (28-001 B08) 70B113927
CONT. ON SHEET 9 SH. NO. 8
7H9
6D9
MRALOOL
MRALOIL
MRALO2L
MRALO3L
MRALO4L
MRALO5L
MRALO6L
MRALO7L
MRAHO4L
MRAHO5L
MRAHO6L
MRAHO7L
IC12 19-008 E
IC11 19-006 B
PART OF B (35-089R02)
PART OF E (35-088R02)
IC90 19-006 B
IC91 19-004 G
C90 33μf
TO IC PACKS
CLOD
BANKO
ENHINC
CLIDG
CLIDP
GND
PPFO
ATNO
AUTOLDI
BANKOA
PART OF P2
PART OF J2
PART OF P3
PART OF J3
MATCH L82
IC09 19-004 G
IC07 19-012 HB
IC05 19-002 G
IC04 19-003 G
IC03 19-005 P
IC07 19-012 HB
INH ADRS SIT-A
S18-A STOP CLK
S26-B PPF
S27-B ATN
S25-B SNGL
OFF NORMAL L81
BANK L80
S24-A MEM
S25-A SNGL
S26-A PPF
S27-A ATN
P5 (LAMP)
(LAMP)
STPO
9C6
CLK1
J5 ADD MATCH
J6 CLOCK
TP
P5
E03
E06
E08
E14
E18
E19
E20
E24
R05 180
R14
R17
MADE BY J D LIMA 10-19-71
ISSUED L. SHAW/JDL 10-21-71
APPROVAL
DES.
CHKR.
REV.
PC 444
DWG. NO (28-001 B08) 70B113927
CONT ON SHEET 9 SH NO. 8

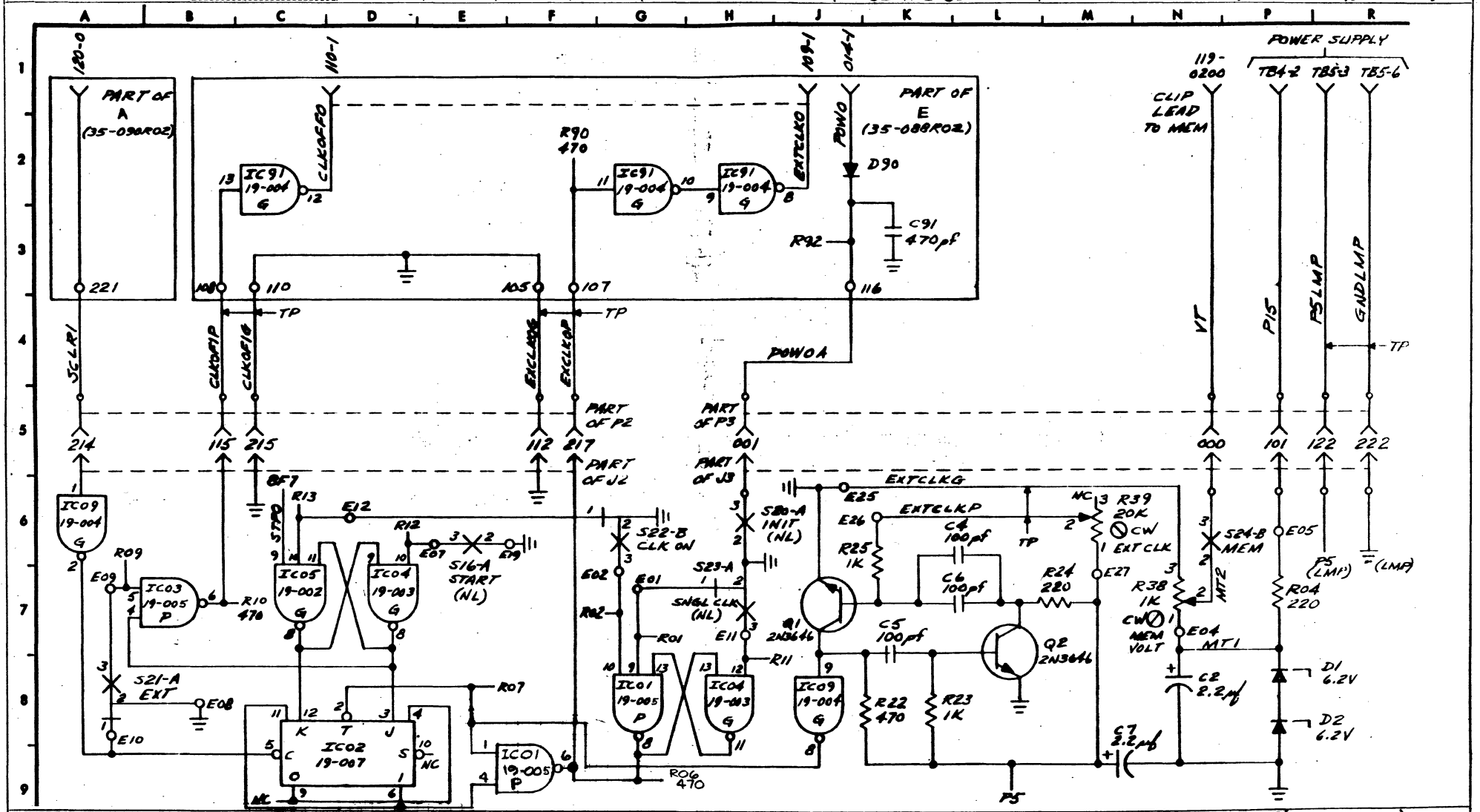
DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS, DECIMALS, ANGLES
SURFACES: √
FRACTIONS: ± | DECIMALS: ± | ANGLES: ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE SCHEMATIC,
SYSTEM TEST SET
FMF GE-PAC 30 | FCF

DWG. NO. (28-001 B08)
70B113927
CONT. ON SHEET 10 SH. NO. 9



MADE BY J D LIMA 10-19-71
ISSUED L. SHAW/JDL 10-21-71
APPROVAL
DES.
CHKR.
REV.

DWG. NO. (28-001 B08)
70B113927
CONT ON SHEET 10 SH. NO. 9

PC 444

GENERAL ELECTRIC

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	✓	±	±	±

REV NO. 70B113927 CONT ON SHEET F SH NO. 10

TITLE SCHEMATIC
SYSTEM TEST SET

FIRST MADE FOR GE-PAC 30

CONNECTOR BOARD			COMPUTER LOCATION			
CABLE	TYPE	DESIGNATION	30-1(COPPER)	(WW) 30-2	30-2(COPPER)	30-2(COPPER) MASS CORE
17-035	35-089	B	10-1	10-1	10-1	11-1
17-035	35-090	A	10-0	10-0	10-0	11-0
17-035	35-087	C	11-1	18-1	15-1	16-1
17-035	35-087	D	12-1	17-1	14-1	15-1
17-035	35-088	E	14-1	13-1	11-1	12-1
17-038	35-087	G	--	15-1	12-1	13-1
17-038	35-087	H	--	16-1	13-1	14-1
17-038	35-089	F	--	19-1	16-1	17-1

REVISIONS

PRINTS TO

MADE BY J.D. LIMA 10-20-71
ISSUED L.SHAW/JDL 10-21-71

APPROVALS

PROCESS COMP. DIV OR DEPT
PHOENIX LOCATION

70B113927 CONT ON SHEET F SH NO. 10

(28-001B08)

FF-808-P (7-70) PRINTED IN U.S.A.