PCP-127

GE-PAC *30
CONTROL COMPUTER

LOGIC MODULE HANDBOOK

GENERAL ELECTRIC

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GE-PAC 30
CONTROL COMPUTER

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GENERAL ELECTRIC

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CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

GE-PAC 30 Digital Systems feature easy field expansion and easy integration into more complex systems. The GE-PAC 30 Logic Modules described in this handbook are flexible building blocks which may be used to implement such expansions or system design. The Logic Modules are simple, reliable, and economical. In addition to the medium speed Series Logic Modules described in this manual, a high speed Series of Logic Modules is available in many of the same logic configurations.

The Medium Speed Series Logic Modules consist of medium speed DTL gates and associated circuitry. The important electrical features of this series of logic elements include: operation from a single power supply potential, high noise immunity, high fan-out capability, low power dissipation, and the capability for "wired-OR" connections. The DTL logic has typical stage delays of 25 nanoseconds.

The High Speed Series Logic Modules use TTL gates and are input, output, and power compatible with DTL modules. Because of the totem-pole output configuration in TTL circuits, the "wired-OR" may not be used. The TTL logic has a maximum propagation delay of 10 nanoseconds, and somewhat higher fanout capability.

1.2 PHYSICAL DESCRIPTION

The mechanical packaging of the Logic Modules employs a "daughter-board" - "mother-board" arrangement. The efficient use of space realized by this method results in very high packaging density.

The circuit components are placed on the daughter-boards. Daughter-boards connect via a set of 16 pins into any one of the 40 locations on a mother-board.

There are two sizes of daughter-boards: a #2 board which plugs onto one mother-board location, and a #3 board which plugs onto two mother-board locations. Each mother-board location has mounting pins which correspond to the daughter-board pins. The mother-board pins have wire-wrap extensions that protrude through the board to the wiring side. The user can therefore interconnect the daughter-board circuits in any configuration desired. There are 138 wire-wrap pins available at the back of the mother-board near the board connectors to facilitate interconnection between mother-boards. The mother-boards fit into a standard 19" rack mounted cage. The mother-boards are 9.75" by 10.5". Up to 13 mother-boards can be inserted into a single card file.

There are 35 1K ohm resistors distributed throughout the mother-board for use in logic speed-up applications or as power gate loads. One side of each resistor is connected to +5 volts. The other side of each resistor has wire-wrap terminal for convenience.

The mother-board is drilled to accept up to eight trimming potentiometers (GE-PAC 30 Part Number 21-003F01 or 21-003F02) in locations 45 and 47, and up to four SPDT reed relays (GE-PAC 30 Part Number 36-001) in locations 00, 10, 20, and 30. The leads of these components all have separate wire-wrap terminals.

Each mother-board location is designated by two numbers. The first is the horizontal

coordinate, and the second is the vertical coordinate. Figure 1-1 shows the mother-board field numbers printed on the board. The daughter-board pin numbers are designated from 00 to 70 for the lower set of pins, and from 11 to 81 for the upper set of pins. If a daughter-board is the #2 size, meaning it covers only one mother-board location, all pin designations are followed by a -0. For instance, 60-0. However, on a #3 daughter-board which covers two mother-board locations and has four rows of pins, the difference between pin 60 on either set is indicated by -0 or -1. The -0 identifies pin 60 lying in the lower mother-board location. A -1 follows the pin 60 lying in the higher mother-board location. The -0 and -1 terminology is used when referring to a daughter-board alone. When referring to a particular pin and the mother-board location on which it is located, the -0 or -1 is not necessary since the mother-board location number automatically differentiates between two different pins on a #3 board. An example of a mother-board wire-wrap pin number is 11-07. The 11 is the daughter-board pin number and the 07 is the mother-board location number. This particular mother-board pin is the upper right pin on the upper right mother-board location as viewed from the component side of the mother-board.

Two connectors are provided at the rear of the mother-board. These 69-pin connectors link the mother-board to the back panel wiring.

Figures 1-1 through 1-3 illustrate the physical layout described in this section.

Figure 1-1 shows a mother-board viewed from the daughter-board side. The numbers 00 to 47 are the mother-board location numbers. Each number designates one location or #2 daughter-board location. The wide plated land around the edge of the board is a low impedance bus which distributes ground throughout the board. The reverse side of the board has an identical bus to distribute +5 volts. At the right side of the board are two 69 pin connectors connecting the mother-board wiring with the back panel wiring. The thin leads running vertically the length of the board bring +5 volts to each field. Therefore, +5 volts and ground are automatically connected to every daughter-board upon insertion into any one of the 40 mother-board locations. Figure 1-1 shows 35 1k ohm resistors mounted between the fields. One side of

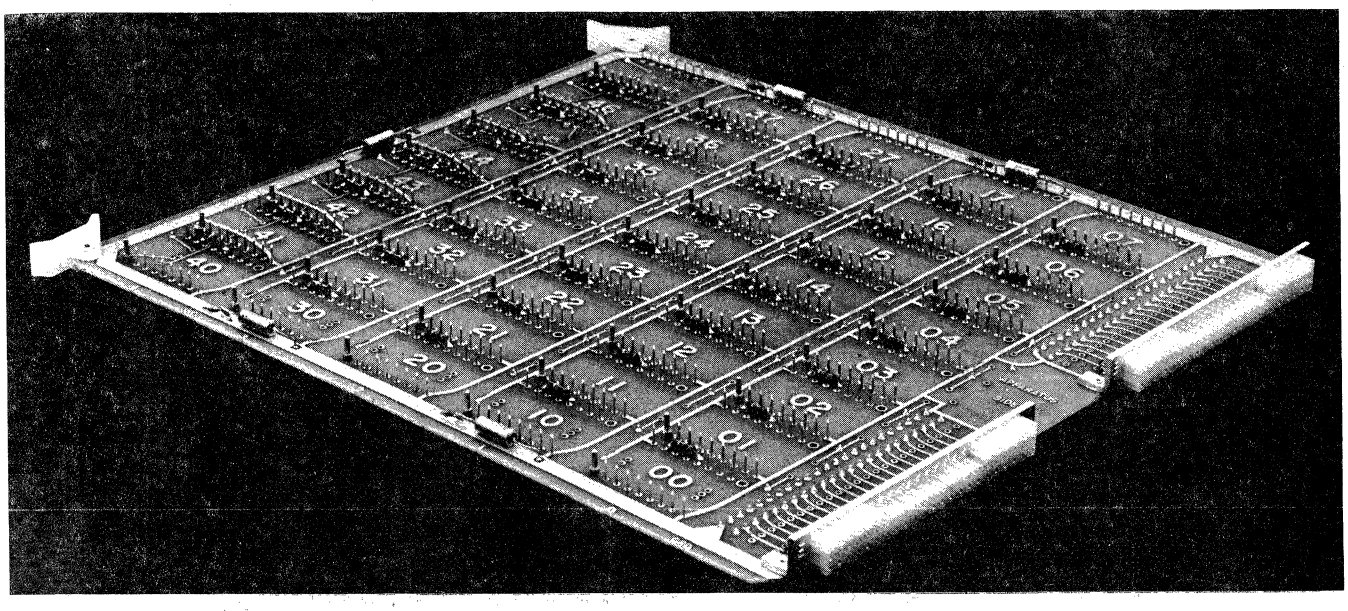


Figure 1-1. Mother Board Configuration

each resistor is connected to +5 volts. The other side of each resistor is brought out to a wire-wrap pin (such as R04, R24, R41, etc.) for connection where needed. The principal application for these resistors is as load resistors for the P type gates since these gates have no internal load connected to the output.

Pairs of feed through holes in the vertical columns between daughter-board locations are provided for mounting external circuit accessories such as diodes, resistors, capacitors, etc. Each feed through hole is connected to the wire-wrap pin (R04, R24, R41, etc.) which connects to +5 volts through a 1K pull-up resistor. Simple or complex networks can be formed by appropriate connections between component wire-wrap pins and daughter-board wire-wrap pins. If a pair of feed through holes are to be used for mounting a single component not requiring the services of the 1K pull-up resistors, the resistors must be removed from the two "R" locations used by the component.

Figure 1-2 shows both sides of a mother-board. The apparatus (component) side is shown on the left. Note the ground bus on the perimeter of the apparatus side. Five decoupling capacitors from the ground bus to the +5 volt bus on the other side of the board are also shown. The wiring side of the board is shown on the right side of Figure 1-2. Note that in addition to the Field designation, pin designations are also provided.

Figure 1-3 shows both sides of a typical #2 daughter-board. Note the connectors and keys on the component side view (left side of Figure 1-3). Additional information can be found in the Systems Interface Manual, GE-PAC 30, Publications Number PCP-126.

1.3 ELECTRICAL DESCRIPTION

GE-PAC 30 logic modules are available in Medium Speed 930 Series DTL integrated circuits, or High Speed Series using TTL integrated circuits. Both series are input-output compatible and use +5V and ground power levels. Discrete transistors

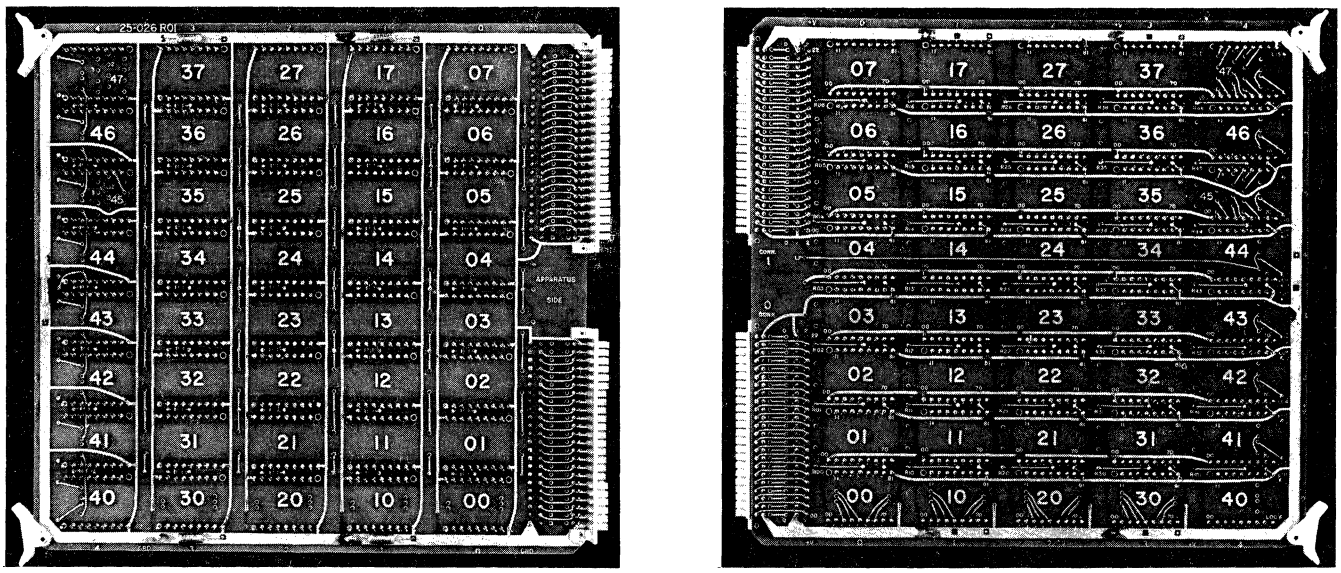


Figure 1-2. Typical Mother-Board, Front and Rear Views

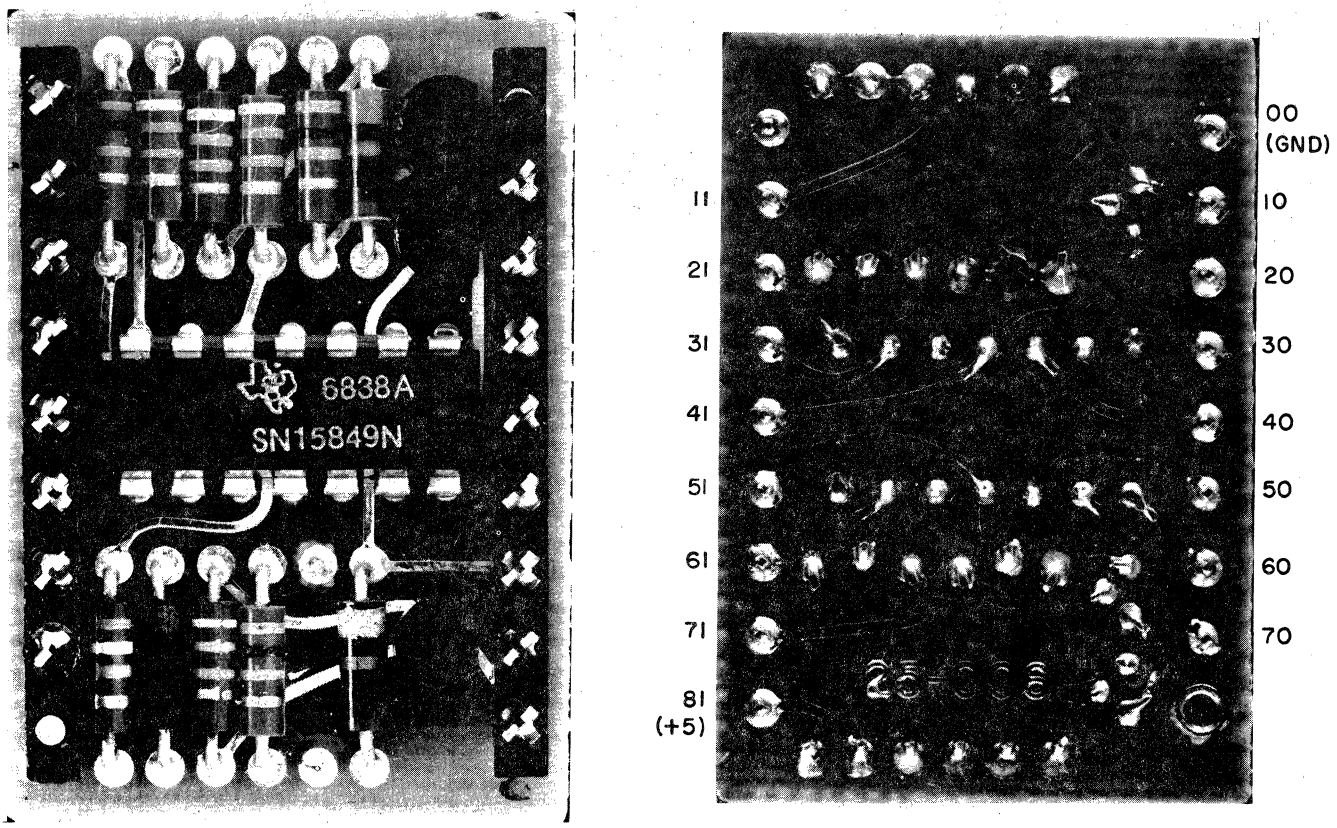


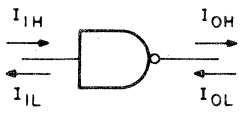
Figure 1-3. Typical Daughter-Board, Front and Rear Views

are used on certain interfacing modules for level conversion or power.

All logic gates are inverting AND (NAND) gates. Five types are used, and are designated as G (standard DTL) gates, P (Power) gates, B (Buffer, high capacitance drive) gates, HG (standard TTL) gates, and HB (TTL Buffer) gates. Figure 1-4 lists the gate type, its output collector arrangement, and minimum logic current levels. Figure 1-5 gives the logic voltage level limits and margins, and Figure 1-6 gives the propagation delays.

Flip-flop circuits are made up of cross coupled gates or J-K double rank integrated circuits. Flip-flops formed by cross coupled gates are shown as such, and the gate characteristics apply. The J-K flip-flop truth table is given in Figure 1-7.

Fan-out for both DTL and TTL logic modules are detailed in Figure 1-8. When the DTL and TTL series are not mixed, the fan-out rules are simple and are listed in the Short



DESIGNATION	TYPE	OUTPUT	I_{IH} uA	I_{IL} ma	I_{OH} ma	I_{OL} ma
G gate	DTL	2K Pull up	10	1.6	1.8	10.2
P gate	DTL	Open Collector	10	1.6	-50uA	36
B gate	DTL	Totem Pole 150 Ω	10	1.6	2.0	34
HG gate	TTL	Totem Pole 80 Ω	80	2.1	2	20
HB gate	TTL	Totem Pole 50 Ω	120	4.2	4	60

RULES:

G gates and P gates may be OR-tied. B, HG and HB gates may not be OR-tied.

P gates may be used to drive non-logic loads such as lamps or transformers.

Max. I_{OL} = 100ma at V_{OL} = 1 volt

Max. I_{OL} = 240ma per I.C.

Caution: when driving lamps take into account "cold" resistance

Caution: when driving transformers, flyback voltage must not exceed 12 V.

Note P gate collectors may be paralleled up to 4 collectors.

Figure 1-4. General Information on Logic Gates

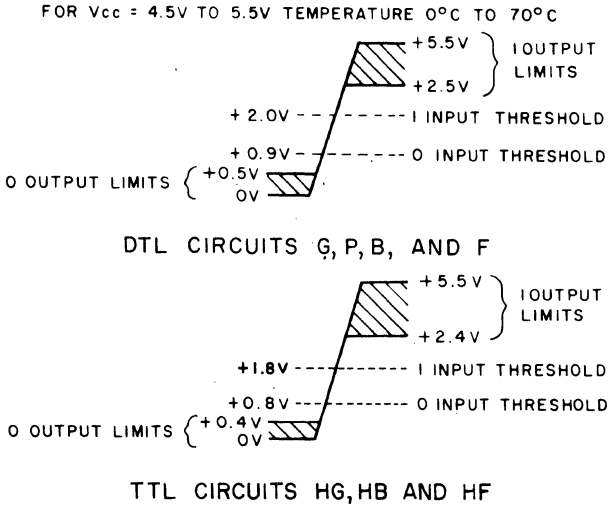
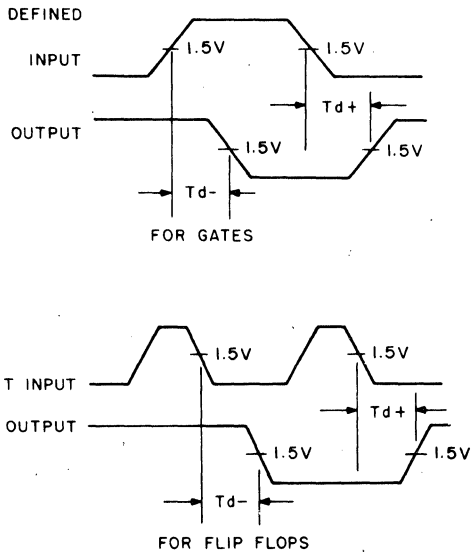


Figure 1-5. Logic Level Margins

Form Rule table. When loading includes a combination of DTL and TTL series gates or flip-flops, it becomes more complex and requires summing currents.

Figure 1-9 shows fan in and fan out current units for DTL, TTL, and flip-flops. These apply only within the same IC family. When DTL and TTL are mixed, the load and drive factors equation is used to determine correct loading.



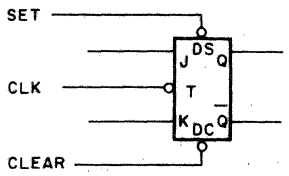
Typical Delays for Estimating

TYPE	Td- in nanoseconds	Td+ in nanoseconds
G, P, or B	10	25
HG or HB	10	10
F	25	50
HF	10	10

Limits and Test Conditions. C = Output Capacitance to GND
R = Output Resistance to +5V.

TYPE	R	C	Td- Min.	Td- Max.	Td+ Min.	Td+ Max.
G	400	50pf.	10	30		
G	3.9K	30pf.			15	50
P	150	100pf.	10	35		
P	510	20pf.			15	50
B	150	500pf.	15	40		
B	510	500pf.			25	80
F	400	30pf.	15	55		
F	2K	30pf.			25	75
HG		15pf.	3	10	4	12
HB		15pf.	3	12	4	12
HF		25pf.	10	18	10	18

Figure 1-6. Propagation Delay



J-K TRUTH TABLE

J Input	K Input	Qn	Qn + 1
0 0	0 0	0 1	0 1
1 1	1 1	0 1	1 0
0 0	1 1	0 1	0 0
1 1	0 0	0 1	1 1

All J-K Flip-Flops are triggered on the Negative going edge of the clock (T) input.

Figure 1-7. J-K Flip-Flop Truth Table

(T) input = 40 nanosec min.

J & K must be steady for 20 nanosec prior to falling edge of (T)

Short form rules (where loads are not mixed DTL and TTL)

DRIVER CAN DRIVE	G	P	B	HG	HB
G gate	7	7	7	5	2
P gate (1000Ω to +5)	21	21	21	17	8
B gate	25	25	25	16	8
HG gate	12	12	12	10	5
HB gate	36	36	36	30	15

NOTE: A DTL Or-tie reduces fanout by 2

For Flip-Flops and mixtures of DTL and TTL Logic calculate fanout with Load and Drive factors equation using fanin and fanout current units.

Load and Drive Factors

A = High Level Load Factor = Current supplied to input when high

B = Low Level Load Factor = Current drawn from input when low.

C = High Level Drive Factor = Current supplied by output when high.

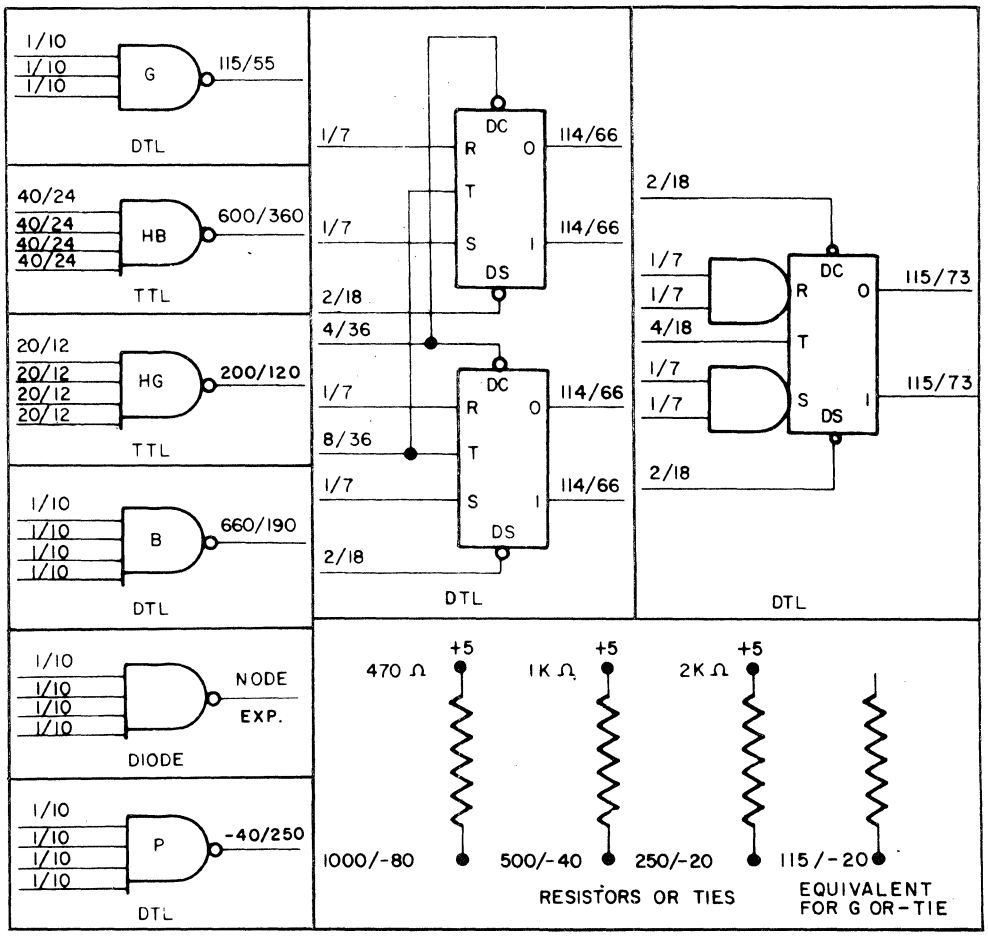
D = Low Level Drive Factor = Current sinked into output when low.

A and C are arbitrary units of current. B and D arbitrary units of current not equal to A and C.

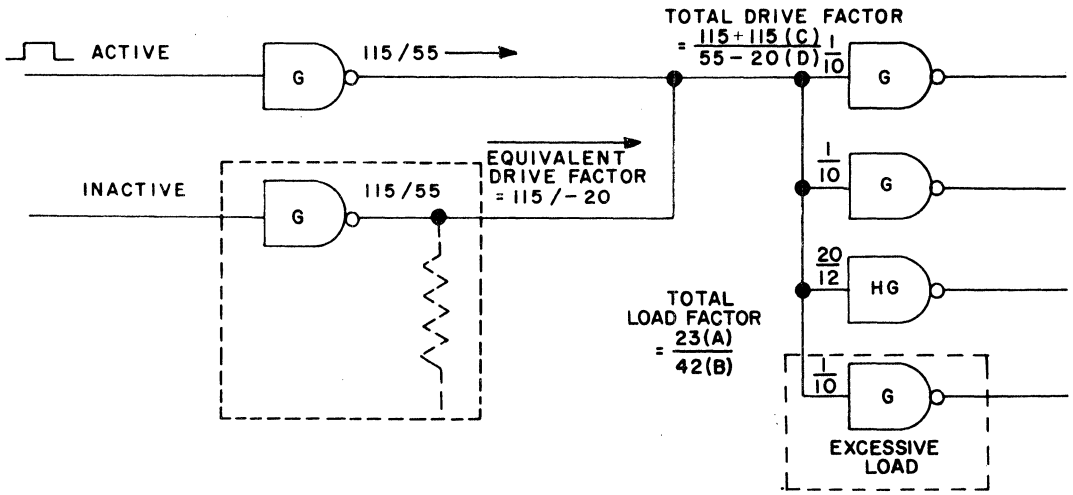
C must be greater than or equal to the summation of A's.

D must be greater than or equal to the summation of B's.

Figure 1-8. Loading Rules for Flip-Flops and DTL-TTL Mixtures



EXAMPLES OF LOAD AND DRIVE FACTOR CALCULATIONS FOR MIXING DTL AND TTL LOGIC:



APPLYING FACTOR EQUATION TO ABOVE LOGIC:

$$\frac{A}{B} \lesseqgtr \frac{C}{D} = \frac{23}{42} \lesseqgtr \frac{330}{35}$$

THIS IS NOT PERMISSABLE SINCE B IS LARGER THAN D. IF LAST GATE IS OMITTED, B = 32 AND $\frac{22}{32} \lesseqgtr \frac{330}{35}$**, WHICH MEETS LOADING RULE REQUIREMENTS FOR DTL AND TTL LOGIC MIXING.**

Figure 1-9. Fan Out and Fan In Current Units for Flip-Flop, DTL, and TTL Logic

CHAPTER 2

GENERAL PURPOSE LOGIC MODULES

2.1 INTRODUCTION

This Chapter describes the General Purpose Logic Modules which are used to implement most gating logic in GE-PAC 30 Digital Systems. A logic diagram, a brief description, and specifications are provided for each type of daughter-board. Many boards contain two uncommitted 1K pull-up resistors. To aid in locating data on the various modules, each description references the GE-PAC 30 part number, and each description starts at the top of a page. Fan in and fan out capabilities refer to logic within a family. When a pull-up is used, deduct four units of fan out. Appendix 1 is provided as a quick reference to the Logic Module Diagrams. The Systems Interface Manual, GE-PAC 30 Publication Number PCP-126, is helpful as it contains system configurations, logic designs, wiring information, etc.

2.2 35-001 QUAD 2 INPUT NAND GATE (DTL)

The 35-001 Quad 2 Input Nand Gate board, shown on Figure 2-1, contains four 2-input G type NAND gates. The gates have low capacitance, diode type inputs. Each output has an internal 2K load resistor. The outputs may be OR tied, but the fan-out capability should be decreased by two units for each such OR tie. Note that two uncommitted pull-up resistors are also provided on the 35-001 board.

2.2.1 Specifications

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	24 milliamps @ +5 volts plus 5 milliamps for each resistor in use.
Size:	Number 2 daughter-board

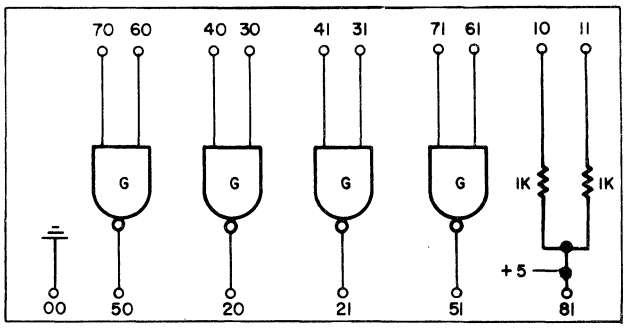


Figure 2-1. 35-001 Quad 2 Input NAND Gate, Logic Diagram

2.3 35-116 QUAD 2 INPUT NAND (TTL)

The 35-116 board shown on Figure 2-2, contains four two-input HG type gates. No internal load resistor is contained on the output, prohibiting an OR tie. Two pull-up resistors are also provided.

2.3.1 Specifications:

Average Propagation Delay:	10 nanoseconds per gate
Power Requirements:	36 milliamps @ +5 volts plus 5 milliamps for each resistor in use
Size:	Number 2 daughterboard

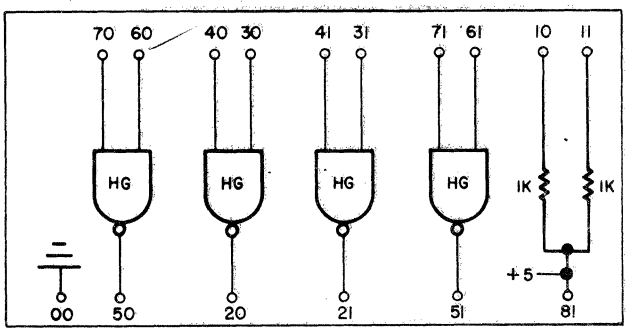


Figure 2-2. 35-116 Quad 2 Input NAND Gate, Logic Diagram

2.4 35-002 TRIPLE 3 INPUT NAND GATE (DTL)

The 35-002 Triple 3 Input NAND Gate board, shown in Figure 2-3, contains three 3-input G type NAND gates.

2.4.1 Specifications:

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	18 milliamps @ +5 volts plus 5 milliamps for each resistor in use
Size:	Number 2 daughterboard

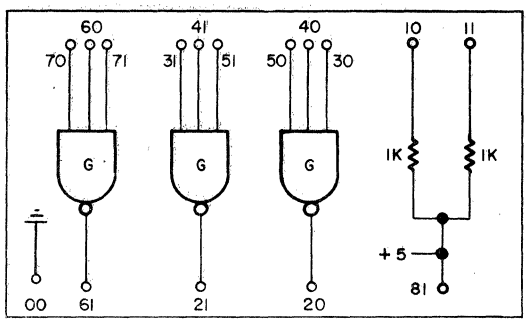


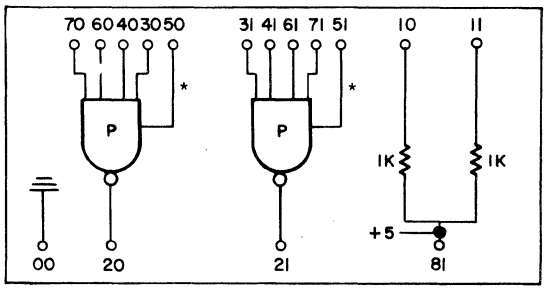
Figure 2-3. 35-002 Triple 3 Input NAND Gate, Logic Diagram

2.5 35-003 DUAL 4 INPUT NAND POWER GATE (DTL)

The 35-003 board, shown on Figure 2-4, contains two 4-input NAND gates. This board has the advantage of access to an expander node, which allows the user to increase the fan-in capability to any desired number by using diodes or expander modules. These are P gates, which require external pull-up resistors.

2.5.1 Specifications:

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	22 milliamps @ +5 volts plus 5 milliamps for each resistor in use
Size:	Number 2 daughter-board



* MUST HAVE DIODE INPUTS

Figure 2-4. 35-003 Dual 4 Input NAND Power Gate, Logic Diagram

2.6 35-117 TRIPLE 3 INPUT NAND GATE (TTL)

The 35-117 board shown on Figure 2-5, contains three 3-input HG type NAND gates. Two 1K ohm resistors are provided for external use.

2.6.1 Specifications:

Average Propagation Delay:	10 nanoseconds per gate
Power Requirements:	27 milliamps @ +5 volts plus 5 milliamps for each resistor in use
Size:	Number 2 daughter-board

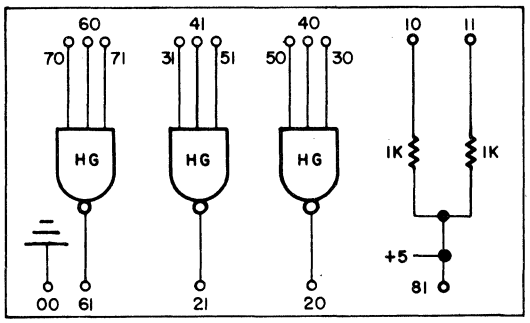


Figure 2-5. 35-117 Triple 3 Input NAND Gate, Logic Diagram

2.7 35-118 DUAL 4 INPUT NAND GATE (TTL)

The 35-118 board shown on Figure 2-6, contains two 4-input NAND gates. The gates are of the HG type. Two 1K ohm resistors are provided for external use.

2.7.1 Specifications:

Average Propagation Delay:	10 nanoseconds per gate
Power Requirement:	18 milliamps @ +5 volts plus 5 milliamps for each resistor in use
Size:	Number 2 daughterboard

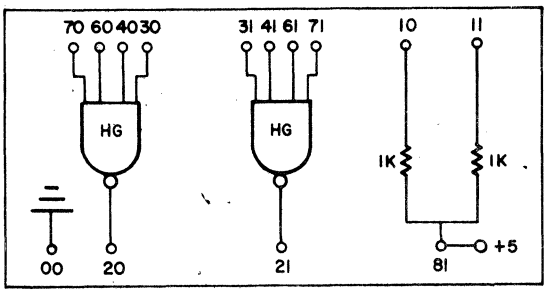


Figure 2-6. 35-118 Dual 4 Input NAND Gate, Logic Diagram

2.8 35-128 DUAL 4 INPUT BUFFER GATE (TTL)

The 35-128 board shown on Figure 2-7, contains two 4-input HB type NAND gates. Two 1K resistors are mounted for external use.

2.8.1 Specifications:

Average Propagation Delay:	10 nanoseconds per gate
Power Requirement:	32 milliamps @ +5 volts plus 5 ma for each resistor used
Size:	Number 2 daughterboards

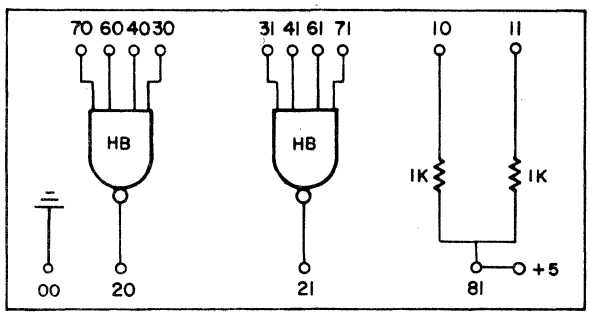


Figure 2-7. 35-128 Dual 4 Input Buffer Gate Logic Diagram

2.9 35-013 4 BIT COUNTER CARRY (DTL)

The 35-013 board, shown on Figure 2-8, contains four gates with inputs tied together as shown. The expander node on one gate is brought out through two diodes. The board also contains a separate 3 input low-level gate.

2.9.1 Specifications:

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	30 milliamps @ +5 volts
Size:	Number 2 daughter-board

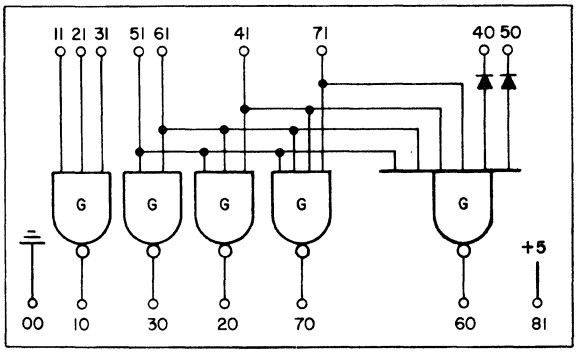


Figure 2-8. 35-013 4 Bit Counter Carry, Logic Diagram

2.10 35-019 1 OUT OF 8 DECODER (DTL)

The 35-019 board, shown on Figure 2-9, contains eight P type gates wired to obtain a general purpose 1 out of 8 decoder. With proper strapping and interconnection, two 35-019 boards can be used to obtain a 1 out of 16 decoder. Four 35-019 boards can be used to obtain a 1 out of 32 decoder. Figure 2-10 illustrates methods of interconnecting 35-019 boards. These are P gates, which require external pull-up resistors.

2.10.1 Specifications:

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	40 milliamps @ +5 volts plus 5 milliamps for each resistor in use
Size:	Number 3 daughter-board

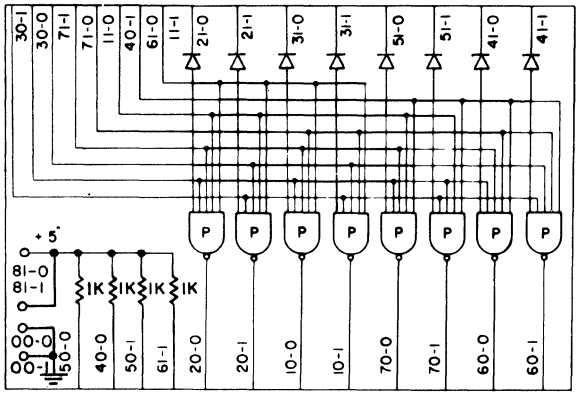
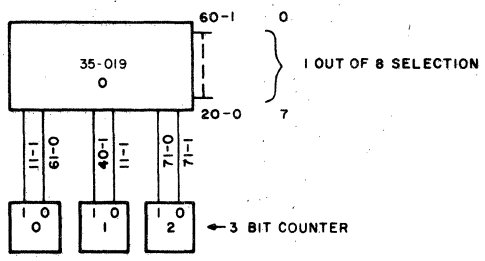
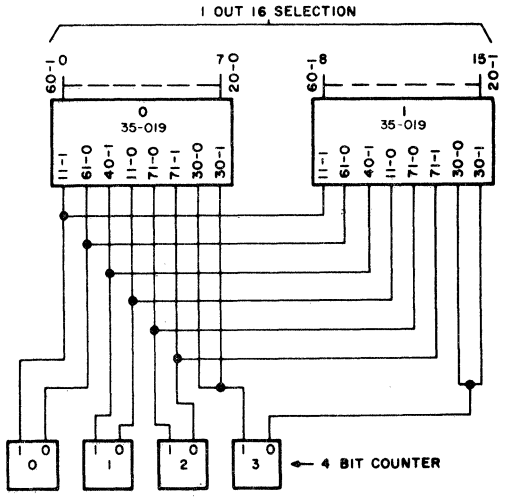


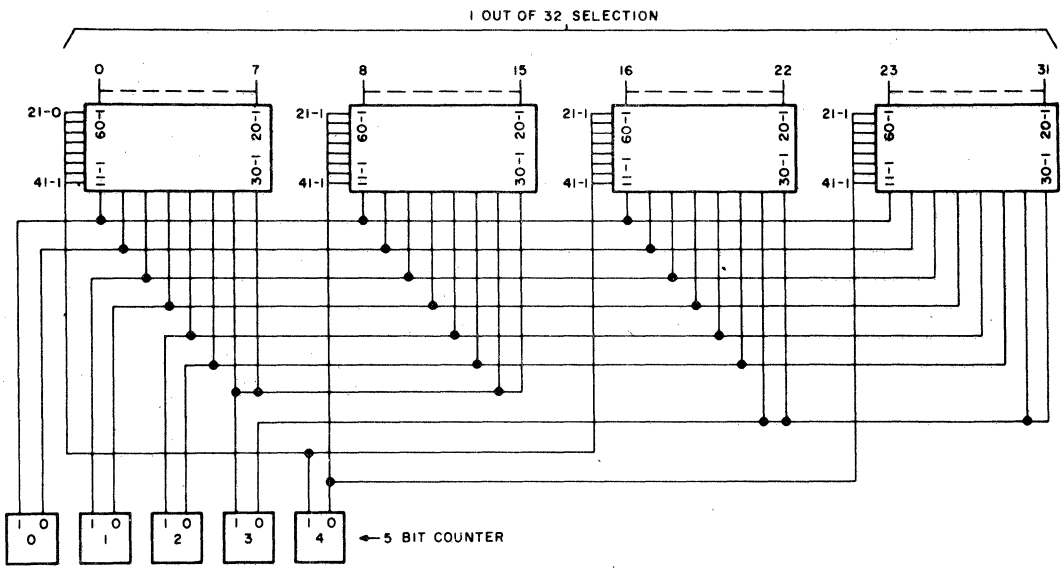
Figure 2-9. 35-019 1 Out of 8 Decoder, Logic Diagram



a. 1 out of 8 circuit



b. 1 out of 16 circuit



c. 1 out of 32 circuit

Figure 2-10. 35-019 1 Out of 8 Decoder, Interconnection Diagrams

2.11 35-064 1 OUT OF 8 DECODER BUFFER (DTL)

The 35-064 board shown on Figure 2-11, contains eight B type gates wired to obtain a one-out-of-eight decoder buffer. The 35-064 board facilitates the charging of the large capacitance created by a high number of fan out leads. Figure 2-10 shows possible expansion to 1 out of 32 selections.

2.11.1 Specifications:

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	43 milliamps @+5 volts plus 5 milliamps for each resistor in use.
Size:	Number 2 daughterboard

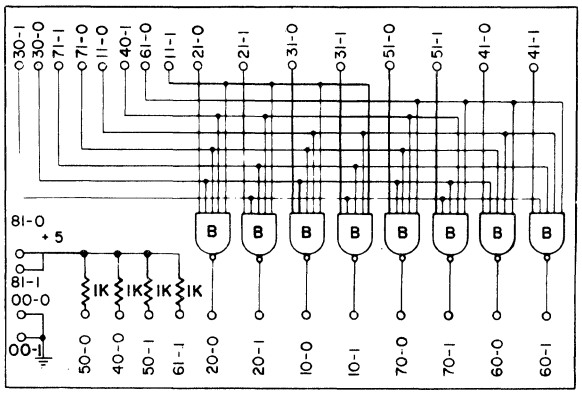


Figure 2-11. 35-064 1 Out of 8 Decoder Buffer, Logic Diagram

2.12 35-020 HEX GATED POWER GATE (DTL)

The 35-020 power gate, shown on Figure 2-12, consists of 6 dual-input power gates with two common inputs. This board is useful for high-current applications such as bus drivers, lamp drivers, etc. For use as a regular gate, external load resistors are required.

2.12.1 Specifications:

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	65 milliamps @ +5 volts
Size:	Number 2 daughterboard

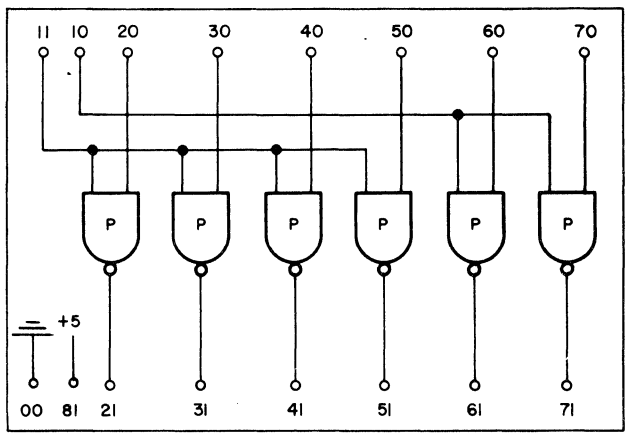


Figure 2-12. 35-020 Hex Gated Power Gate, Logic Diagram

2.13 35-021 QUAD GATED NOR GATE (DTL)

The 35-021 board, shown on Figure 2-13, consists of 4 gated NOR circuits operating from mutual gate leads.

2.13.1 Specifications:

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	48 milliamps @ +5 volts
Size:	Number 2 daughter-board

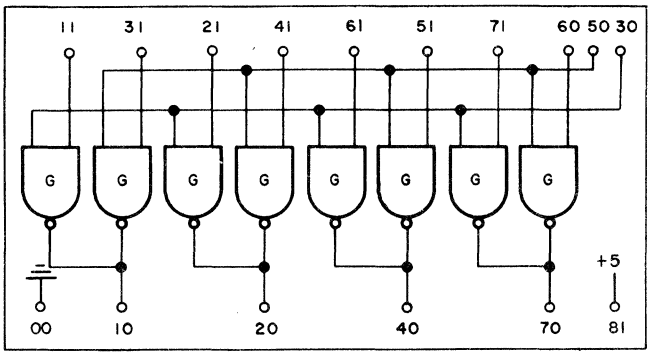


Figure 2-13. 35-021 Quad Gated NOR Gate, Logic Diagram

2.14 35-022 INPUT NAND GATE (DTL)

The 35-022 board, shown on Figure 2-14, is a NAND gate which combines high fan in capability with a high fan out capability. External pull-up resistors must be supplied on the outputs.

2.14.1 Specifications:

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	23 milliamps @ +5 volts
Size:	Number 2 daughter-board

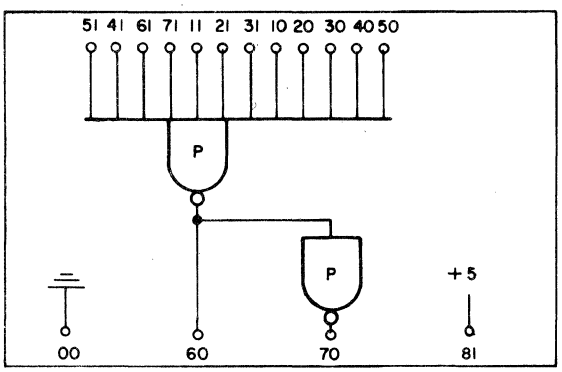


Figure 2-14. 35-022 12 Input NAND Gate, Logic Diagram

2.15 35-119 SINGLE 8 INPUT NAND GATE (TTL)

The 35-119 board shown in Figure 2-15 is a HG type NAND gate which combines high fan in capability with a medium fan out capability. Two 1K ohm resistors are supplied for external use.

2.15.1 Specifications:

Average Propagation Delay:	10 nanoseconds per gate
Power Requirement:	9 milliamps @ +5 volts plus 5 milliamps for each resistor in use
Size:	Number 2 daughterboard

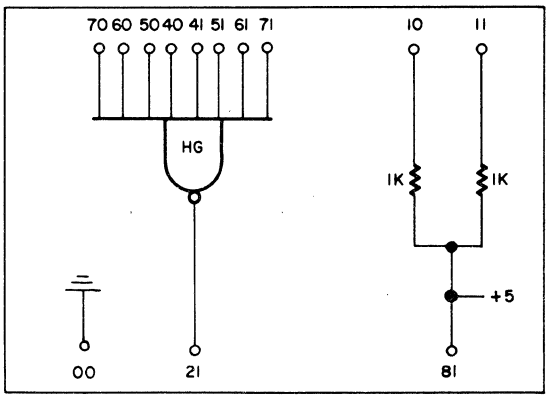


Figure 2-15. 35-119 8 Input NAND Gate, Logic Diagram

2.16 35-023 QUAD GATED BUFFER (DTL)

The 35-023 board, shown on Figure 2-16, consists of four three-input buffer gates with two common inputs as shown.

2.16.1 Specifications:

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	60 milliamps @ +5 volts
Size:	Number 2 daughterboard

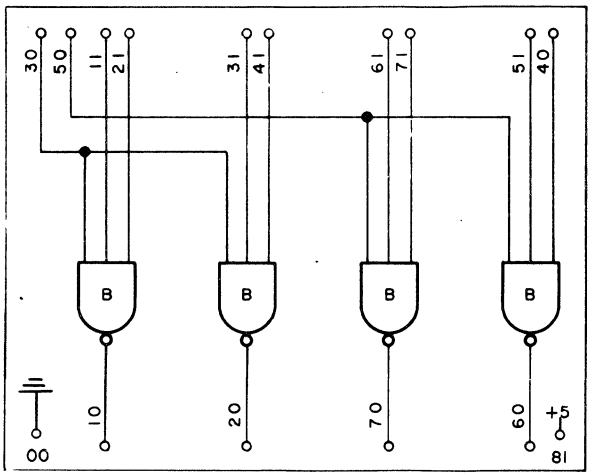


Figure 2-16. 35-023 Quad Gated Buffer, Logic Diagram

2.17 35-059 QUAD GATED BUFFER (TTL)

The 35-059 board shown on Figure 2-17, consists of four three-input HB type gates with two common inputs as shown.

2.17.1 Specifications

Average Propagation Delay:	10 nanoseconds per gate
Power Requirement:	35 milliamps @ +5 volts
Size:	Number 2 daughter-board

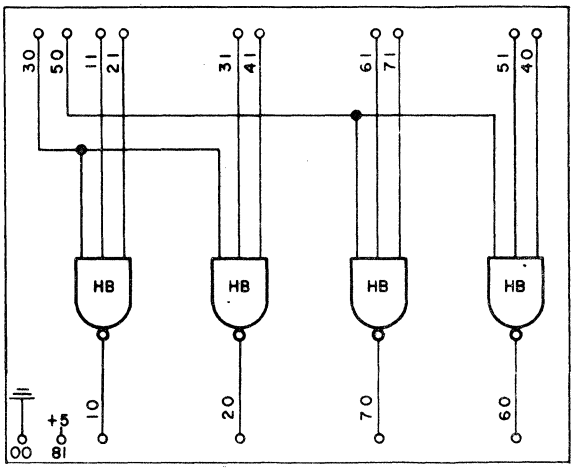


Figure 2-17. 35-059 Quad Gated Buffer, Logic Diagram

2.18 35-060 HEX INVERTER (DTL)

The 35-060 board, shown on Figure 2-18, consists of 6 inverting gates. Each low level gate has a 2K ohm load resistor internally connected. The outputs may be tied together to obtain an OR function, but the fan-out capability should be decreased by 2 for each such OR tie.

2.18.1 Specifications:

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	36 milliamps @ +5 volts plus 5 milliamps for each resistor in use
Size:	Number 2 daughter-board

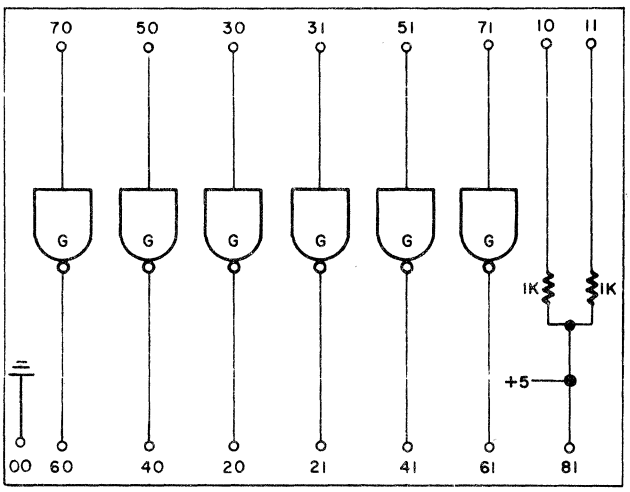


Figure 2-18. 35-060 Hex Inverter, Logic Diagram

2.19 35-115 HEX INVERTER (TTL)

The 35-115 board shown on Figure 2-19, consists of six HG type gates. No internal load resistor is contained on the output, prohibiting an OR tie. Two 1K resistors connected to +5 volts are provided for pullup applications.

2.19.1 Specifications:

Average Propagation Delay:	10 nanoseconds per gate
Power Requirement:	54 milliamps @ +5 volts plus 5 milliamps for each resistor in use
Size:	Number 2 daughterboard

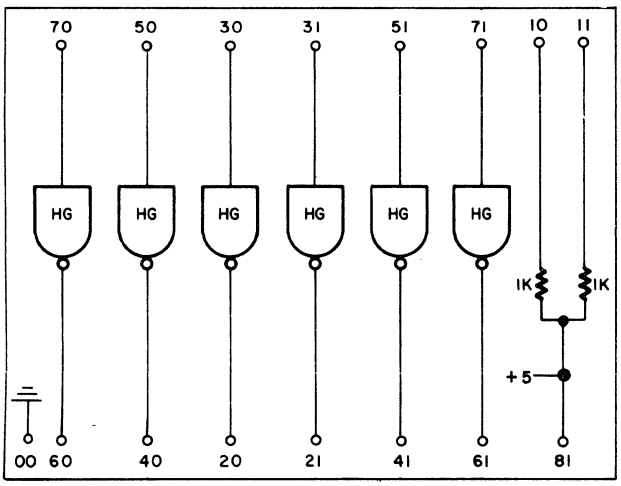


Figure 2-19. 35-115 Hex Inverter Logic Diagram

OR

2.20 35-040 SINGLE-DOUBLE RAIL CONVERTER (DTL)

The 35-040 board, shown on Figure 2-20 contains four converters which produce a double rail output from a single rail input. The four converters share common input gating.

2.20.1 Specifications:

Average Propagation Delay:	25 nanoseconds per stage
Power Requirement:	40 milliamps @ +5 volts
Size:	Number 2 daughterboard

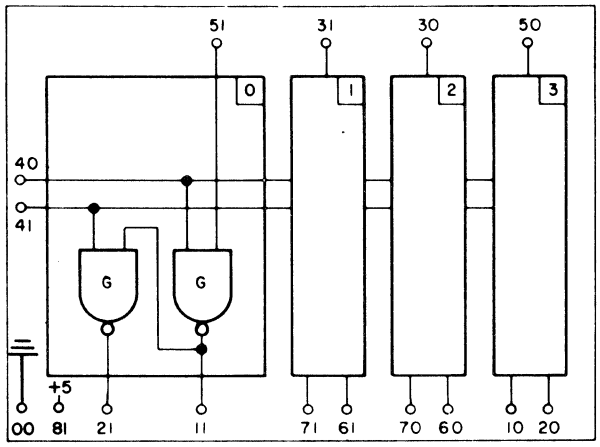


Figure 2-20. 35-040 Single-Double Rail Converter, Logic Diagram

2.21 35-045 FOURTEEN 1K RESISTOR MODULE

The 35-045 board, shown on Figure 2-21, has fourteen 1K resistors which may be used as load resistors for P type gates.

2.21.1 Specifications:

Power Requirement:	5 milliamperes for each resistor in use.
Size:	Number 2 daughter-board

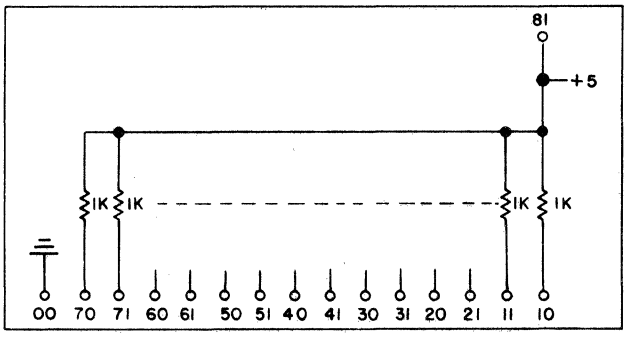


Figure 2-21. 35-045 Fourteen 1K Resistor Module, Logic Diagram

2.22 35-099 BUS TERMINATING RESISTOR MODULE

The 35-099 board shown on Figure 2-22 has ten 180 ohm resistors and four 1K ohm resistors used for termination of bus lines.

2.22.1 Specifications:

Power Requirement:	300 milliamps @ +5 volts
Size:	Number 2 daughter-board

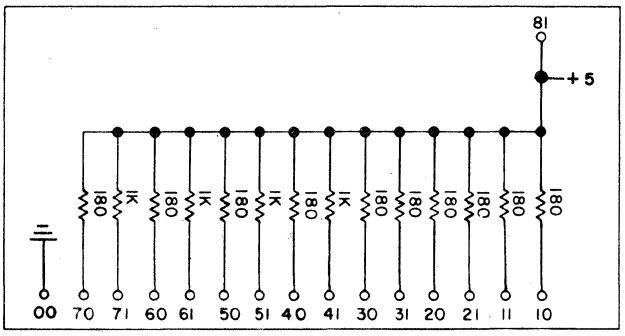


Figure 2-22. 35-099 Bus Terminating Resistor Module, Logic Diagram

2.23 35-122 FOURTEEN 220 OHM RESISTOR MODULE

The 35-122 shown on Figure 2-23 has fourteen 220 ohm resistors which may be used as load resistors for P type gates.

2.23.1 Specifications:

Power Requirement:	310 milliamps @+5 volts
Size:	Number 2 daughter-board

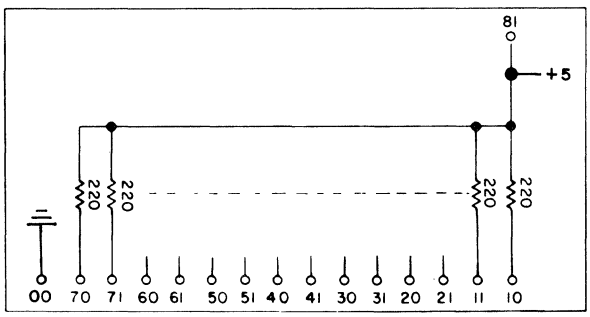


Figure 2-23. 35-122 Fourteen 220 Ohm Resistor Module Logic Diagram

CHAPTER 3

REGISTER LOGIC MODULES

3.1 INTRODUCTION

This Chapter describes the daughter-boards used to form registers in GE-PAC 30 systems. A brief description, a logic diagram, and a list of specifications are provided for each type of register module.

3.2 35-009 4 BIT RS REGISTER WITH GATES (DTL)

The 35-009 board, shown on Figure 3-1, consists of 4 flip-flops. The Set-Reset Function can be controlled by either the Direct Double Rail Inputs or by the Single-to-Double Rail Conversion Gates. The four circuits share each of two gated inputs.

One output side of each flip-flop contains a power gate for high fan out capabilities or to drive a 30 MA or 40 MA display lamp. The power gates have a common gated input.

3.2.1 Specifications

Average Propagation Delay:	25 nanoseconds per stage
Power Requirement:	120 milliamps @ +5 volts
Size:	Number 3 daughter-board

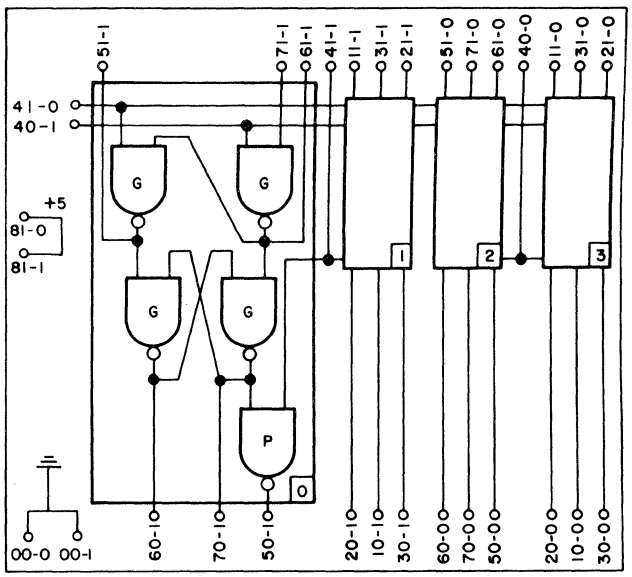


Figure 3-1. 35-009 4 Bit RS Register with Gates, Logic Diagram

3.3 35-015 4 BIT JK REGISTER (DTL)

The 35-015 board, shown on Figure 3-2, consists of 4 JK flip-flops with common gating leads and a G gate between the J and K leads of each flip-flop. Two separate power gates with a common input are also provided on the 35-015 board; these gates require external pull-up resistors.

3.3.1 Specifications

Average Propagation Delay:	40 nanoseconds
Power Requirement:	110 milliamps @ +5 volts
Size:	Number 3 daughter-board

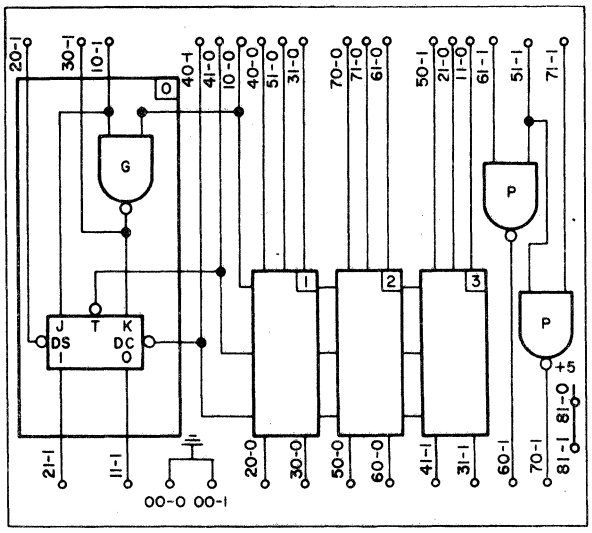


Figure 3-2. 35-015 4 Bit JK Register, Logic,Diagram

3.4 35-134 FOUR BIT SERIAL PARALLEL CONVERTER (DTL)

The 35-134 board shown on Figure 3-3, is a 4-bit buffer and shift register. Provisions are made for gated parallel load and clocked serial output. Three separate clock inputs are provided so that individual clear (pin 51), load (pin 21), and shift (pin 41) sources may be used. Modules may be cascaded to form registers of any desired length.

3.4.1 Specifications:

Power Requirement:	90 milliamps @ +5 volts
Size:	Number 2 daughter-board

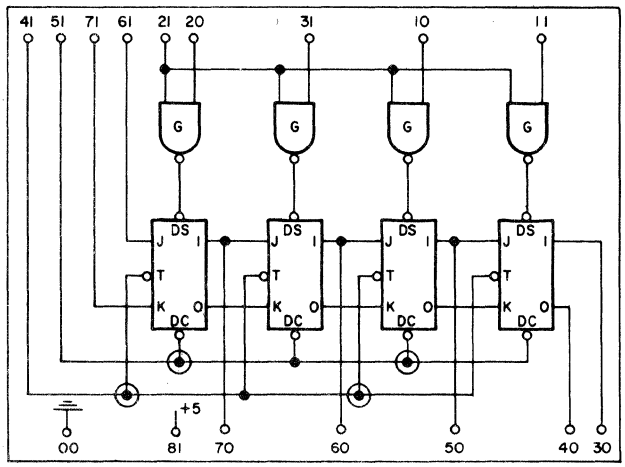


Figure 3-3. 35-134 Four Bit Serial Parallel Converter, Logic Diagram

3.5 35-016 DUAL JK FLIP-FLOP (DTL)

The 35-016 board, shown on Figure 3-4, contains 2 clocked JK flip-flops which operate on a master-slave principle. Information enters the master while the toggle input signal is high, and transfers to the slave when the toggle goes low. Since operation depends only on voltage level, any waveshape having the proper voltage levels may be used as a toggle signal. Input buffers provide isolation between the master and the input leads, thereby enhancing noise immunity. Set and clear leads are provided to allow direct access to the slave flip-flop.

Figure 3-5 shows the timing for a 35-016 board. The flip-flops on this board operate on a clocked basis. Information on the J or K leads is gated into the master flip-flop when the toggle clock lead, T, is pulsed high. The clock pulse should be a minimum of 40 nanoseconds wide. During this period the data must not change on the J or K inputs. When the clock pulse goes low, information transfers from the master to the slave. From that point on, the slave flip-flop serves as a permanent memory for the information.

3.5.1 Specifications

Average Propagation Delay:	40 nanoseconds
Power Requirement:	30 milliamps @ +5 volts
Size:	Number 2 daughterboard

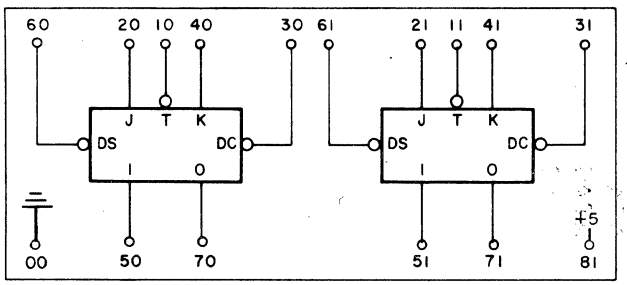


Figure 3-4. 35-016 Dual JK Flip-Flop, Logic Diagram

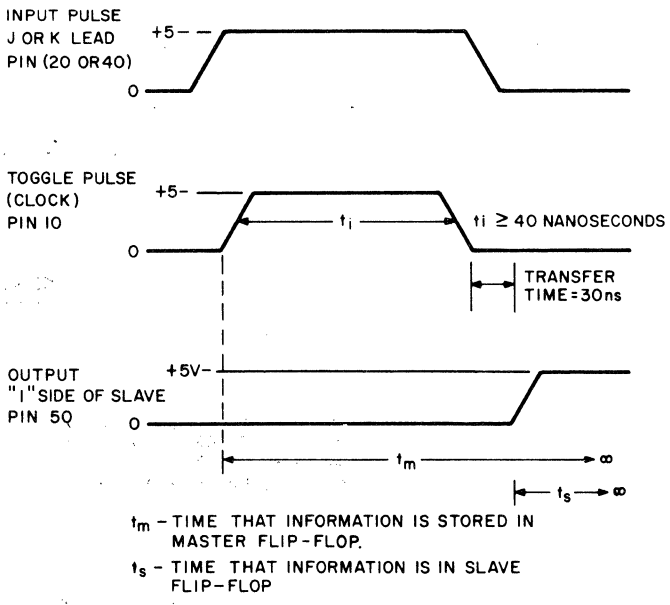


Figure 3-5. 35-016 Dual JK Flip-Flop, Timing Diagram

3.6 35-157 CLOCKED FLIP-FLOP (DTL)

The 35-157 board shown on Figure 3-6, contains one clocked flip-flop operating on the master/slave principle. Information enters a dual input AND master when the input on the toggle (T) is high and then transfers to the slave when the toggle signal goes low. The DS and DC inputs take precedence regardless of master inputs. The 35-157 Clocked Flip-Flop can be converted to a J-K flip-flop by connecting terminals 31 to 50 (or 40) and 20 to 51 (or 61).

Figure 3-7 shows the timing for the 35-157 board. Information gated into the master flip-flop while the toggle input is high may be changed up to 40 nanoseconds before the toggle input signal goes low. During the 40 nanosecond period before the toggle falls, information on the DS and DC inputs must **remain stable and high. When the toggle input goes low, information is transferred from the master to the slave.**

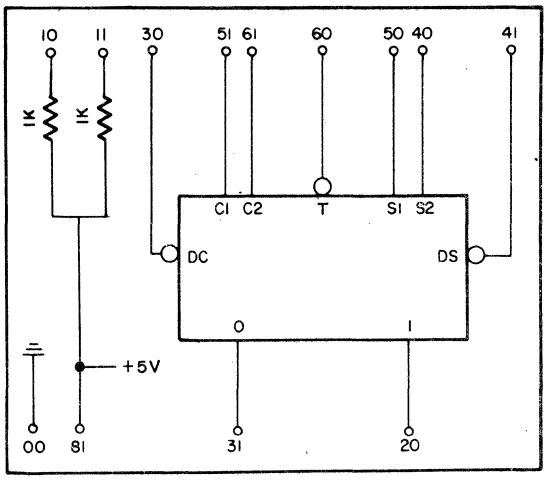
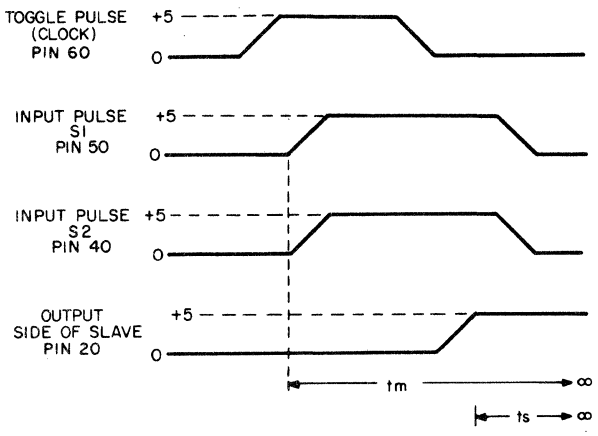


Figure 3-6. 35-157 Clocked Flip-Flop, Logic Diagram

3.6.1 Specifications:

Average Propagation Delay:	40 nanoseconds
Power Requirement:	20 milliamps @ +5 volts plus 5 milliamps for each resistor used.
Size:	Number 2 daughter-board



tm - TIME THAT INFORMATION IS STORED IN MASTER FLIP-FLOP
ts - TIME THAT INFORMATION IS IN SLAVE FLIP-FLOP

Figure 3-7. 35-157 Clocked Flip-Flop, Timing Diagram

3.7 35-136 FOUR-BIT COUNTER (DTL)

The 35-136 board shown on Figure 3-8, is two 2-bit counters using JK flip-flops. Provisions are made for gated parallel loading. Pin 31 provides for the clearing of all four flip-flops on a clocked input. Pins 71 and 11 allow incrementing the flip-flops by pairs with a clocked input. Figure 3-9 is a diagram showing how to connect the four flip-flops to form a ripple counter circuit.

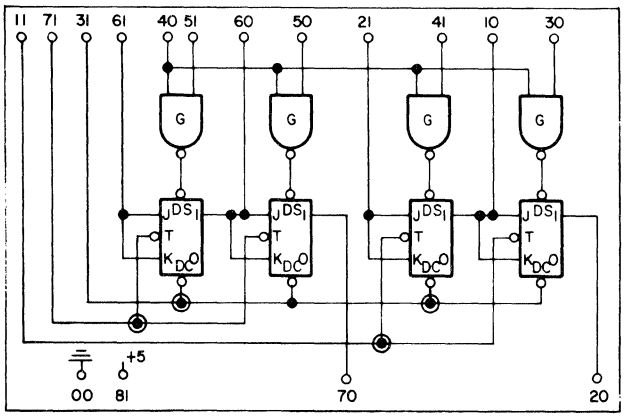


Figure 3-8. 35-136 Four-Bit Counter, Logic Diagram

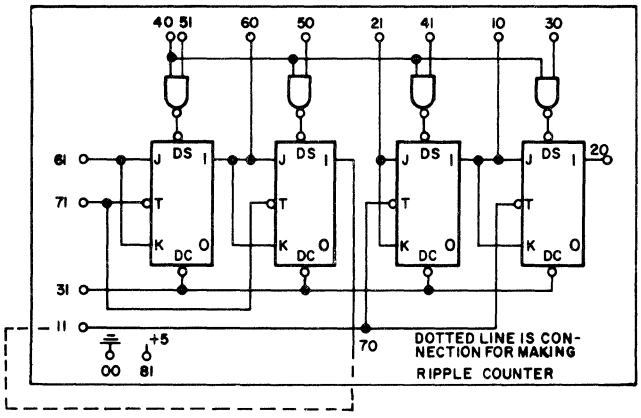


Figure 3-9. 35-136 Four Bit Counter, Wired as a Ripple Counter

Figure 3-10 is a diagram showing how to connect the four flip-flops by the use of external gates into a fast carry counter circuit. Incrementing of a ripple counter is done serially by pairs, while in the fast carry configuration, incrementing is done in parallel.

3.7.1 Specifications:

Power Requirement: 90 milliamps @ +5 volts

Size: Number 2 daughterboard

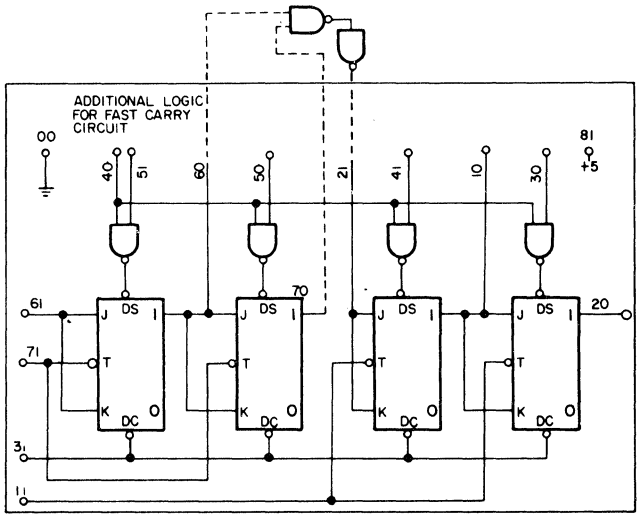


Figure 3-10. 35-136 Four Bit Counter, Wired as a Fast Carry Circuit

3.8 35-014 FOUR BIT BY EIGHT WORD REGISTER STACK (CTL)

The 35-014 board is a 32 bit register arranged as eight, four bit words as shown in Figure 3-11. The memory cells are true dual rank non-destructive readout registers with isolated input (S) and output (D) buses. A register may be interrogated repeatedly without disturbing its content. One word may be written into while reading another. Also, the same information may be written into two different words simultaneously. It is also permissable to read a word while writing new information into that word. The data will change on the negative going edge of the Write pulse (WO-W7) with bit to bit stagger not exceeding 10 nanoseconds.

The 35-014 board uses Complementary Transistor Logic (CTL) which is not generally compatible with DTL or TTL circuits. The 35-041 board (see **Page 3-9**) is designed to drive the 35-014 Register Stack. Figure 3-12 lists the Drive Voltage and Current Requirements for the Register Stack and Figure 3-13 gives the Switching Times.

Figure 3-14 shows a typical circuit using the 35-014 Register Stack and the 35-041 Driver to form an eight word, four bit register. Figure 3-15 shows how this may be extended to a 16 word, 16 bit register stack.

Fan out of the B gates on the inputs (SO-S15) and on the 35-041 Driver is sufficient to operate the 16 by 16 stack.

3.8.1 Specifications

Power Requirements: 250 milliamps @ +5 volts

Size: Number 3 daughter board

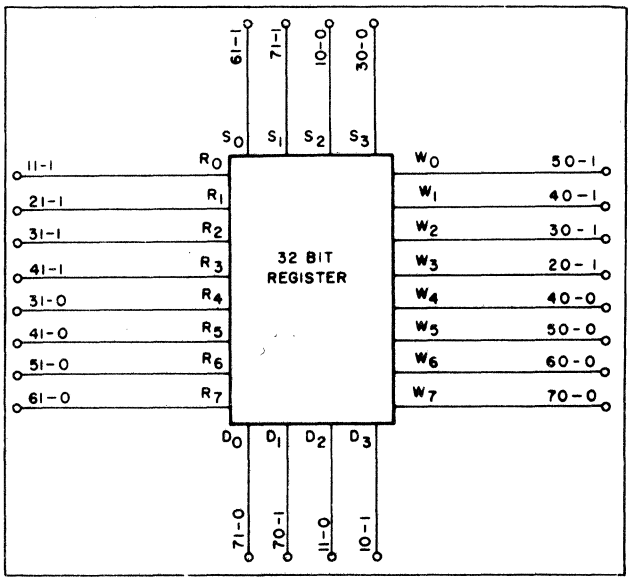


Figure 3-11. 35-014 Four Bit By Eight Word Register Stack, Logic Diagram

D.C. TESTS (V_{CC} = 4.5 V, T = 25°C)

DESCRIPTION	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS	EQUIV CT μL LOAD
Read Input Current	(R_0–R_7) = 2.5V		4.4	mA ea.	1.5
Data Input Current	(S_0–S_4) = 2.5V		4.4	mA ea.	1.5
Write Input Current	(W_0–W_7) = 2.5V		8.8	mA ea.	3
Output Voltage (High State)	(D_0–D_4) = -10 mA	2.35		V	
Output Voltage (Low State)	(D_0–D_4) = -1 mA		-0.36	V	
Output Leakage	(D_0–D_4) = 4 V		5	μA	

INPUT LEVEL: Maximum permissible "low" level = 0.8 V. Maximum required "high" level: 1.25 V.

Figure 3-12. Drive Voltage and Current Requirements for Register Stack

SWITCHING TIME:

t_1 25 ns MIN
t_2 10 ns MIN
t_3 10 ns MIN
t_4 10 ns MIN
t_5 25 ns MAX
t_6 25 ns MAX
t_7 25 ns MIN

NOTE:

1) DOTTED LINES REPRESENT CELL STORING "LOW" LEVEL
2) t_7 REPRESENTS TIME INTERVAL BETWEEN READ PULSES FOR ERROR-FREE READOUT

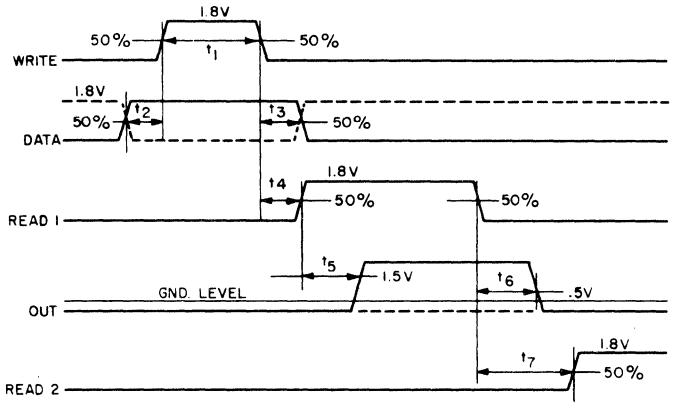


Figure 3-13. Switching Times for Register Stack

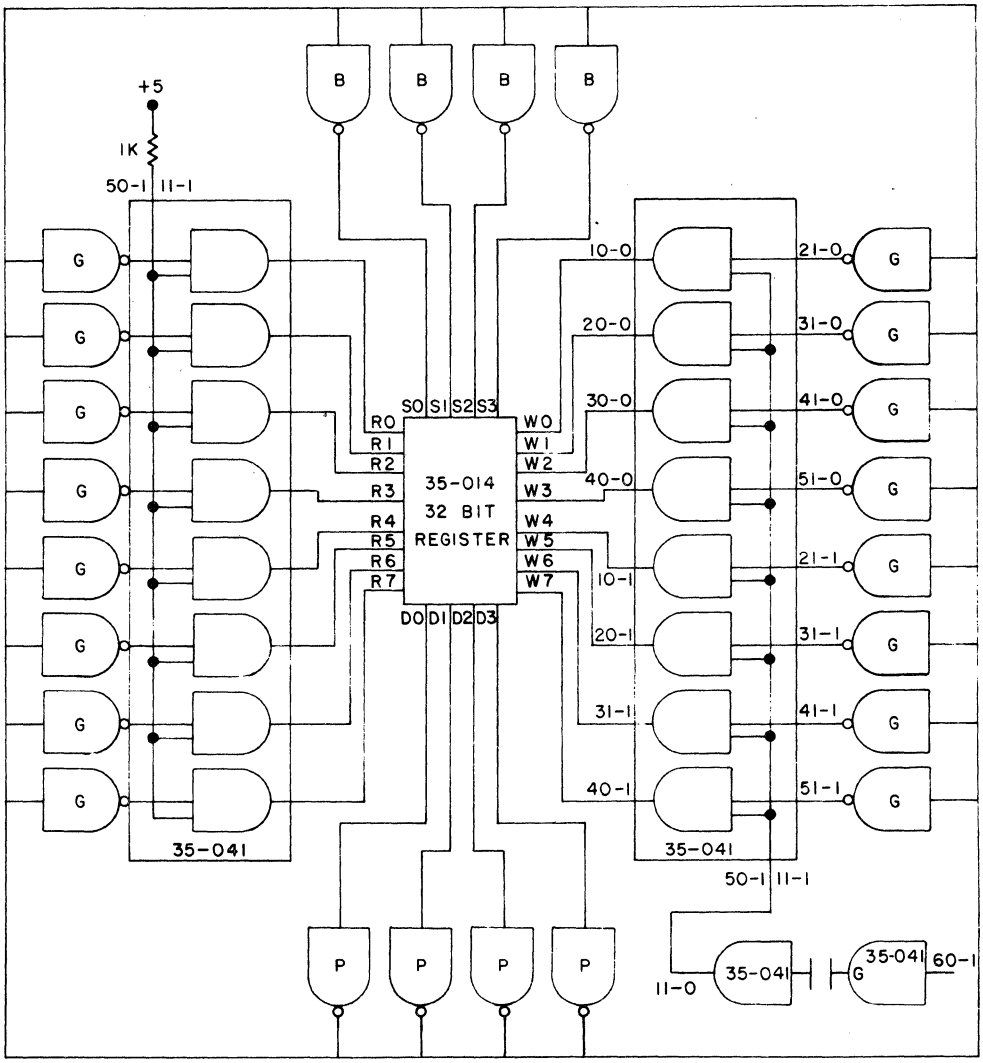


Figure 3-14. Typical Circuit Forming an Eight Word Four Bit Register

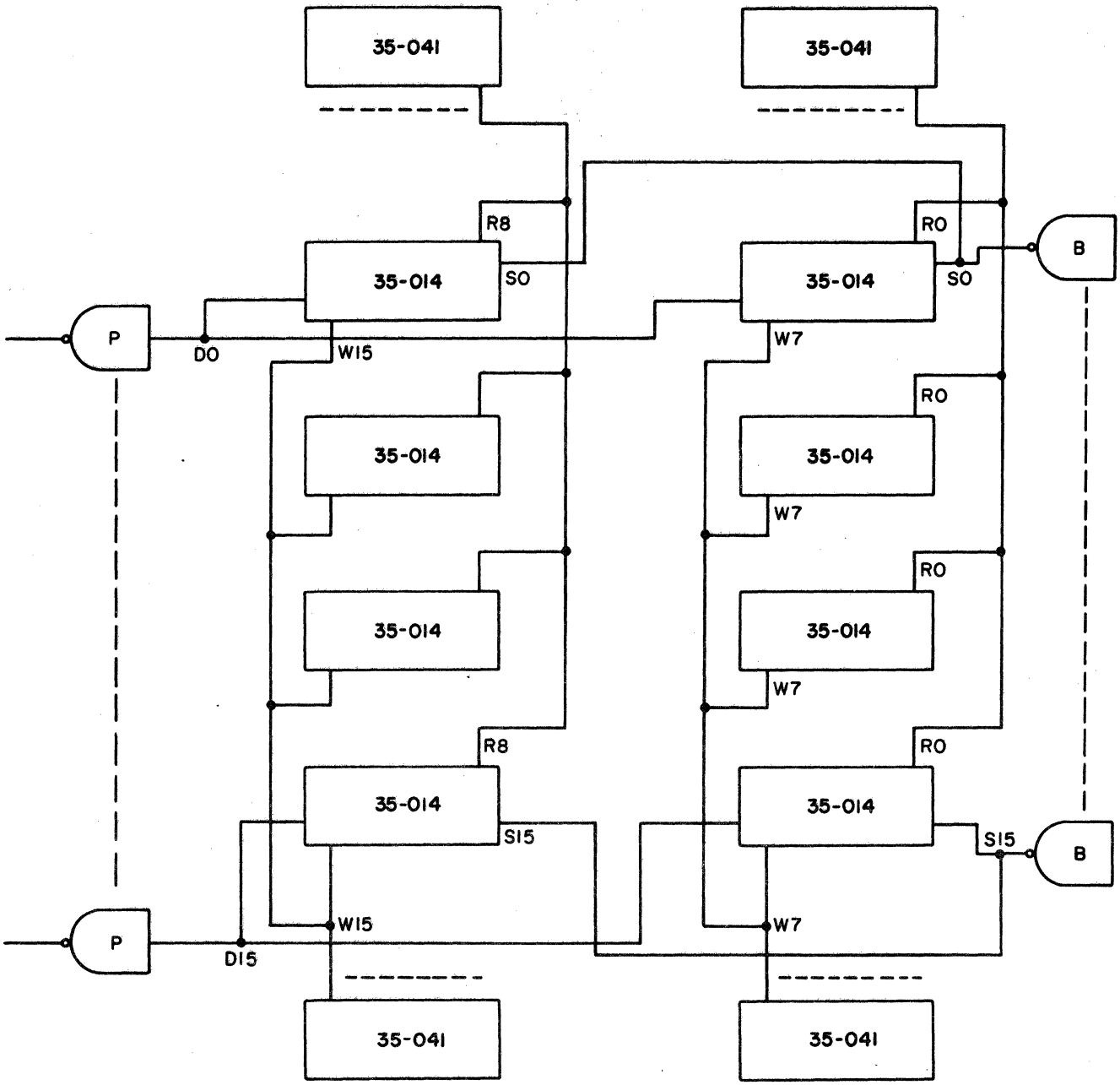


Figure 3-15. Sixteen Bit, Sixteen Register Stack

3.9 35-041 EIGHT BIT STACK DRIVER (DTL)

The 35-041 board, shown on Figure 3-16 contains 8 driver circuits, 1 differentiator circuit, and 3 additional general purpose gates. The driver circuits supply a positive 3 volt pulse whenever both inputs go high. The differentiator circuit generates a positive 5 volt pulse 25 nanoseconds wide on pin 11-0, whenever pin 60-1 goes high, which is generally used to generate a "Write" clocking pulse. (See Figure 3-14). The 35-041 board provides an interface from DTL or TTL circuits to CTL circuits. It is designed as a driver for the 35-014 Register Stack. See 3.8.

3.9.1 Specifications

Average Propagation Delay:	25 nanoseconds per gate
Power Requirement:	100 milliamps @ +5 volts
Size:	Number 3 daughter board

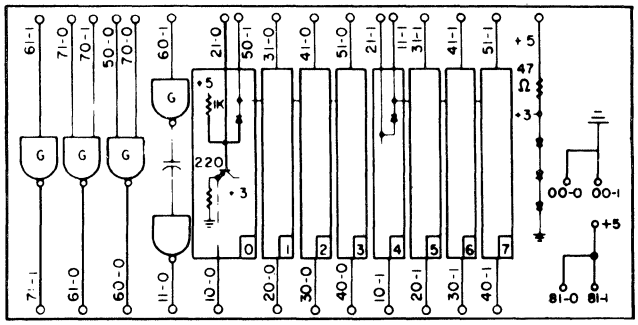


Figure 3-16. 35-041 Eight Bit Stack Driver, Logic Diagram

CHAPTER 4

TIMING LOGIC MODULES

4.1 INTRODUCTION

This Chapter describes the daughter-boards used to provide relatively wide tolerance timing functions in GE-PAC 30 Digital Systems.

The circuits are intended for use where 5% to 10% variation can be tolerated.

The 35-027 and 35-053 are differentiator type timing circuits and should not exceed 50% duty cycle. The temperature coefficient is typically .125%/C° and delay varies 2% to 3% with ±10% variation in +5 volts. The 35-008 is a one shot multivibrator useable to a duty cycle of 80%. Delay variation is less than 3% for supply voltage +5 volts ±10% over the temperature range of 0°C to 50°C with the internal timing capacitor. Absolute delay accuracy requires trimming the delay resistance to compensate for transistor junction variations.

4.2 35-027 DUAL DIFFERENTIATOR (DTL)

The 35-027 Logic Module, shown on Figure 4-1, contains two independent differentiator circuits which may be used any of three ways:

1. They may be used to develop two different pulses of arbitrary widths.
2. They may be interconnected to produce a delay with a variable run time and a variable output pulse width.
3. They may be cross-coupled to form a variable frequency clock generator.

External capacitors and resistors determine the differentiator time constants. The capacitors are connected from pin 30 to pin 40, and pin 31 to pin 41. Resistors must be connected from pin 40 to +5 volts and pin 41 to +5 volts. The capacitor and resistor form a differentiation circuit which turns off the following gate. The 35-027 is not a precision delay element. The output pulse width is typically 0.9RC seconds using the internal Buffer gate input. Delay depends however on the high output voltage of the B gate which varies over a considerable range from unit to unit. Output pulse width is more predictable if the capacitor is driven by an external DTL Power (P) gate since the high state output voltage is nearer the supply voltage. In any case delay is a function of supply voltage and it is recommended that the resistor R be a potentiometer to allow adjustment for circuit parameters. For small capacitor values delay is less predictable because of the effect of stray capacitance. Maximum and minimum values for R and C are listed in Table 4-1. Note the minimum values of R and C may not be used simultaneously as it would result in a 2 nanosecond delay.

Run time from 200 nanosecond to several seconds is obtainable (e.g. C = 250 μf, and R = 47 K gives approximately 12 second delay.)

T_{in} must exceed T_{run} and recovery time is 500C or 200 nanoseconds whichever is greater. If the input capacitor is driven by a DTL power gate with a pull up resistor R_1, Recovery Time is approximately $3R_1C$ or 200 nanoseconds. To produce a variable frequency clock circuit, pin 70 is connected to pin 21, and pin 71 is connected to pin 10. Typical waveforms of the 35-027 board when used as a differentiator are shown in Figure 4-2.

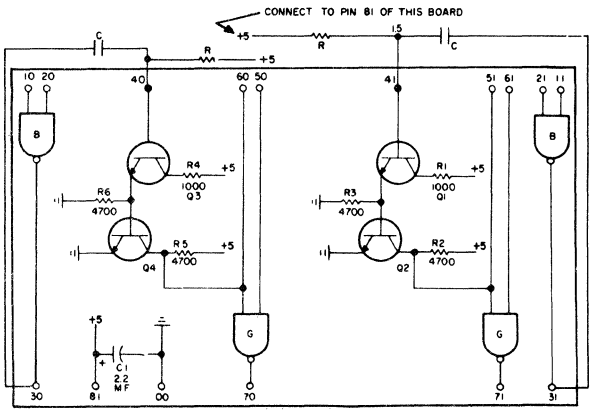


Figure 4-1. 35-027 Dual Differentiator, Logic Diagram

Table 4-1. Differentiator Data

Value	Minimum	Maximum
Resistance in Ohms (R)	200	100K
Capacitance in Picofarads (C)	10	Note 1
Time in Nanoseconds (T)	200	Note 2

NOTES: 1. C may be any value as long as leakage current is less than 20 microamperes.
2. Values of T up to several seconds are practical

4.2.1 Specifications

Power Requirement:	27 milliamps @ +5 volts
Duty Cycle:	50%
Size:	Number 2 daughter-board

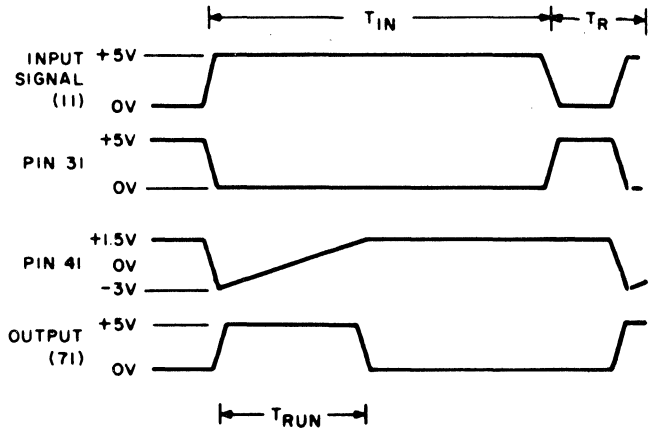
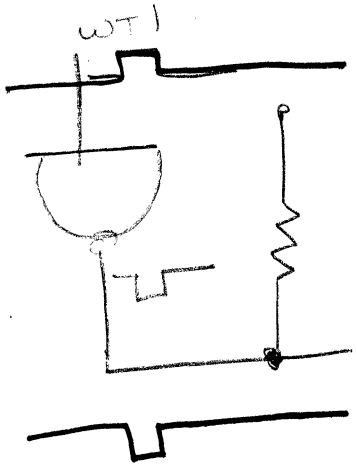


Figure 4-2. 35-027 Dual Differentiator, Timing Diagram



$T_{RUN} = \frac{1000 \times 10^{-9}\ \text{pf.}}{.082 \times 10^{3}} \approx 82 \times 10^{-6}\ \text{n.s.}$

.1 mf. ≈ $.1 \times 10^{-6}$

4.3 35-008 VARIABLE DELAY GENERATOR (DTL)

The 35-008 Logic Module, shown on Figure 4-3, provides a delay generator with provisions for external control. Both input, and output gating are provided. A positive going 100 nanosecond output pulse, which starts after the delay time, is provided from pin 50. Pin 71 provides a positive going signal for the duration of the delay. A negative spike on pin 71 will terminate the delay. Pin 71 should not be used without buffering. A spare G Gate is also provided on the 35-008 board.

The length of the delay is determined by the value of a capacitor connected between pins 10 and 20, and a resistor connected from pin 11 to +5 volts. The total delay is approximately equal to .8RC seconds. The minimum delay of 50 nanoseconds is obtained by applying +5 volts directly to pin 11. The delay generator can be run at duty cycles up to about 80%. The input pulse duration may be greater or less than the delay. Recovery time from the end of T_p should be at least 25% of T_p + Td. Figure 4-4 shows the timing relationships on the 35-008 board. Table 4-2 lists the maximum and minimum values for R and C.

4.3.1 Specifications

Power Requirement:	45 milliamps @ +5 volts
Duty Cycle:	80%
Size:	Number 2 daughterboard

Table 4-2. Delay Generator Data

Value	Minimum	Maximum
Resistance in Ohms (R)	1000 Internal	15K external
Capacitance in Picofarads (C)	47 Internal	See Note
Time in Nanoseconds (T)	50	RC +50

NOTE: C may be any value as long as leakage current is less than 20 microamperes.

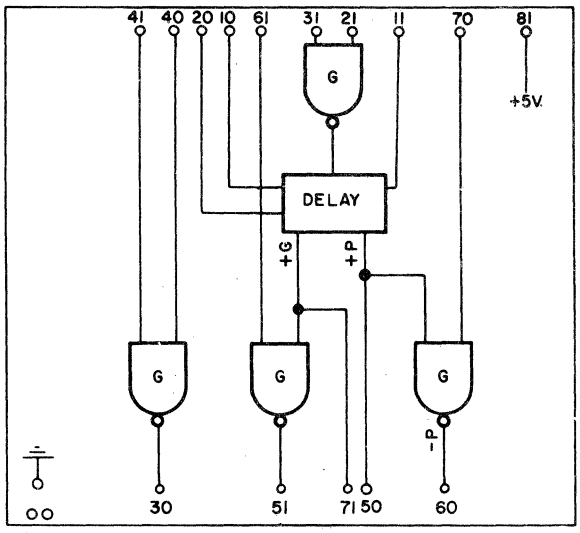


Figure 4-3. 35-008 Variable Delay Generator, Logic Diagram

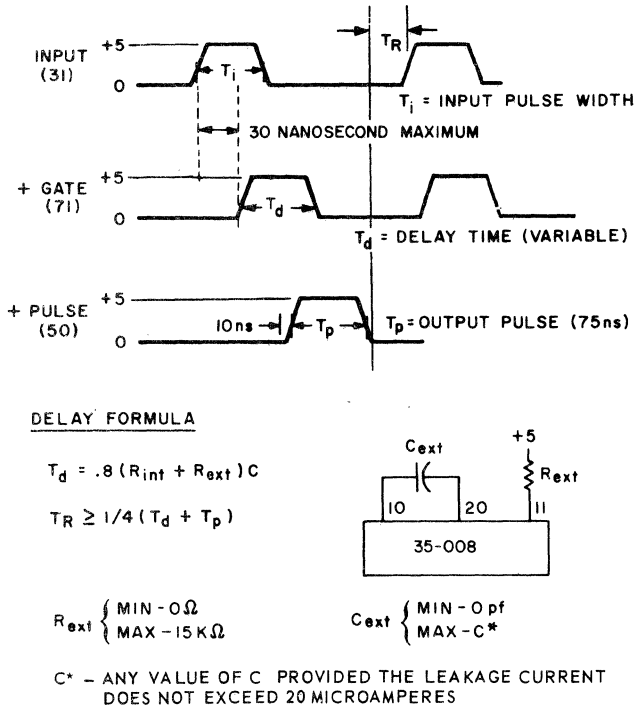


Figure 4-4. 35-008 Variable Delay Generator, Timing Diagram

4.4 35-053 DUAL ADJUSTABLE TIMING NETWORK (DTL)

The 35-053 board as shown on Figure 4-5, contains two identical circuits that provide a variable delay pulse of variable width. The delay of the pulse is controlled by an internal RC network and an externally mounted potentiometer connected between +5 volts and pin 11 (or 30). The pulse width is controlled by an internal RC network and an externally mounted potentiometer connected from +5 volts to pin 50 (or 41). A minimum pulse delay and pulse width of 80 nanoseconds is controlled by the internal RC networks of each circuit. Circuit configurator allows for the input pulse to be shorter in duration than the delay. Table 4-3 lists the minimum values for R and C. Figure 4-6 shows the timing relationship on the 35-053 board.

NOTE

This circuit is a non-precision delay element recommended for use with potentiometers to trim out circuit variations. In addition, the external resistor leads should be short and should be returned to pin 81 of this daughter board.

4.4.1 Specifications:

Power Requirements: 58 milliamps @ +5 volts

Duty Cycle: 50%

Size: Number 2 daughterboard

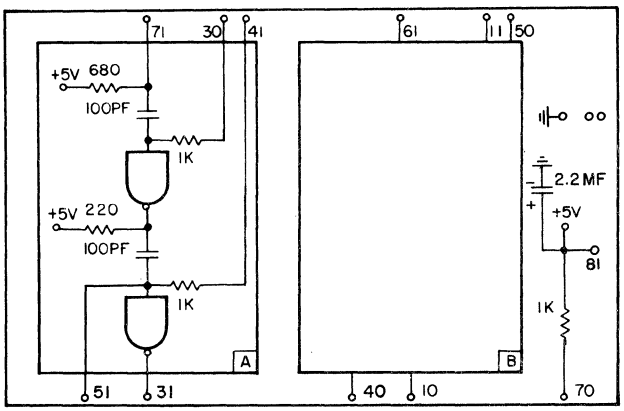


Figure 4-5. 35-053 Dual Adjustable Timing Network, Logic Diagram

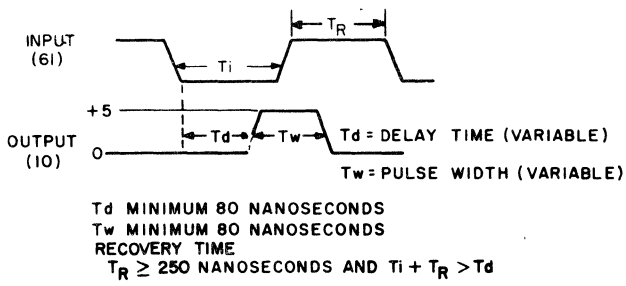


Figure 4-6. 35-053 Dual Adjustable Timing Network, Timing Diagram

Table 4-3. Dual Adjustable Timing Network Data

Value	Pulse Width Control		Pulse Delay Control	
	Minimum	Maximum	Minimum	Maximum
Resistance in Ohms (R)	1K Internal	10K External	1K Internal	10K External
Capacitance in Picofarads (C)	100	100	100	100
Time in Nanoseconds (T) Approx.	80	0.9RC*	80	0.9RC*

*Where R = External resistance plus the internal 1000 ohms.

CHAPTER 5
DRIVERS AND RECEIVERS

5.1 INTRODUCTION

This Chapter describes the daughter-boards used as drivers and receivers for GE-PAC 30 Digital System bus and communication lines. A brief description, a logic diagram, and technical description are provided for each type of module.

5.2 35-046 NEGATIVE TO POSITIVE CONVERTER (DTL)

The 35-046 board shown on Figure 5-1 converts logic signals in the 0 volts to -12 volts range to logic levels of +5 volts to 0 volts. Each 35-046 daughter-board contains six identical circuits for logic level conversion and a 1000 ohm resistor connected to +5 volts for general use as a logic node pullup. The common bias at pin 10 can be set at ground or some negative level to establish an input threshold.

NOTE

In order to work directly into DTL logic, this common bias should not exceed -0.75 volts. Larger negative bias values require some limiting resistance or voltage shift network on the output or the DTL load package may be damaged.

5.2.1 Specifications:

Power Requirements: 3 milliamps @ +5 volts plus 5 ma. if R3 is used.

Size: Number 2 daughter-board

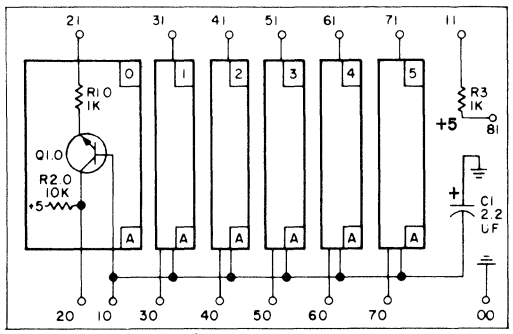


Figure 5-1. 35-046 Negative to Positive Converter, Logic Diagram

5.3 35-079 MULTIPLEXED BUS DRIVER (DTL)

The 35-079 board shown on Figure 5-2 consists of two identical circuits each capable of gating one of three true signals to a common bus lead. The three enable inputs, pins 51, 31, and 30, are common to both circuits as is the output enable, pin 41. Both inputs may be expanded to gate more than three signals to the bus by using inputs on pins 60 and 10.

5.3.1 Specifications:

Power Requirements: 50 milliamps @ +5 volts

Size: Number 2 daughterboard

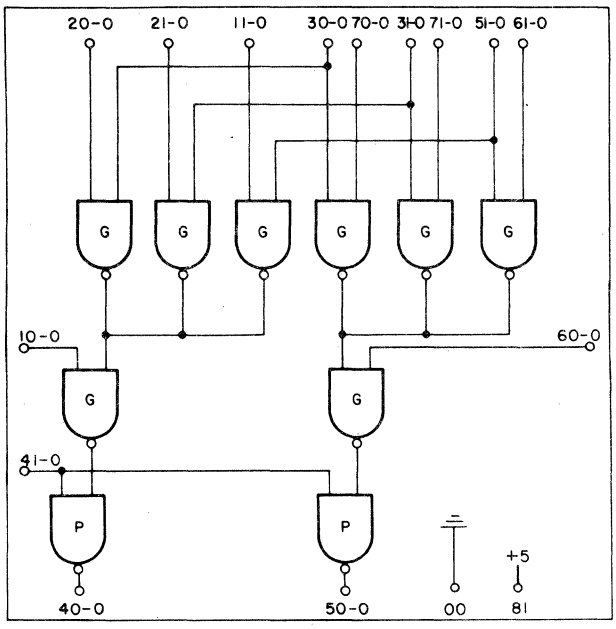


Figure 5-2. 35-079 Multiplexed Bus Driver, Logic Diagram

5.4 35-154 360 BUS RECEIVER (DTL)

The 35-154 board shown on Figure 5-3, provides two receivers for converting IBM 360 input logic to GE-PAC 30 standard logic. IBM logic is characterized by 1.7 volts or more considered as a logic one and inputs of .7 volts or less considered as a logic zero. Both voltage levels are relative to ground of the receiver circuit.

5.4.1 Specifications:

Power Requirement: 35 milliamps @ +5 volts
2 milliamps @ -5.5 volts

Size: Number 2 daughterboard

NOTE

The -5.5 volts is not a standard GE-PAC 30 voltage and must be derived from the -16 volt (15 to 18.5) memory power supply.

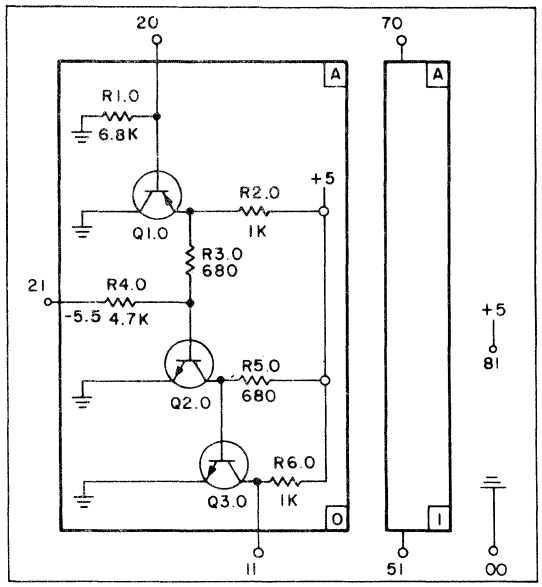


Figure 5-3. 35-154 360 Bus Receiver, Logic Diagram

5.5 35-155 360 BUS DRIVER (DTL)

The 35-155 board shown on Figure 5-4, contains four identical line driving circuits to interface with an IBM 360 system. GE-PAC 30 input logic levels of +5 volts and 0 volts are changed to logic levels standards of 1.7 volts and above considered as logic one and .7 volts or less considered as a logic zero.

5.5.1 Specifications:

Power Requirement: 310 milliamps @ +5 volts

Size: Number 2 daughterboard

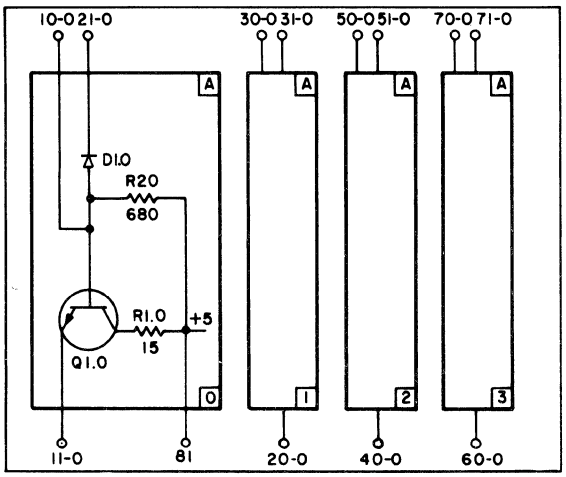


Figure 5-4. 35-155 360 Bus Driver, Logic Diagram

5.6 35-162 TRIPLE BIPOLAR DRIVER (DTL)

The 35-162 board shown on Figure 5-5, consists of three circuits for driving communications lines in compliance with EIA standard RS-232B or other applications requiring bipolar output levels. An GE-PAC 30 logic level input of +5 volts outputs a -6 volts signal while a logic level input of 0 volts outputs a signal of a +6 volts. The 2.5V bias network may be bypassed externally, if necessary. Use of resistors to +5 volts and/or ground can modify the value of the bias.

5.6.1 Specification:

Power Requirements: 6 milliamps @ +5 volts
30 milliamps @ +15 volts
30 milliamps @ -15 volts

Size: Number 2 daughterboard

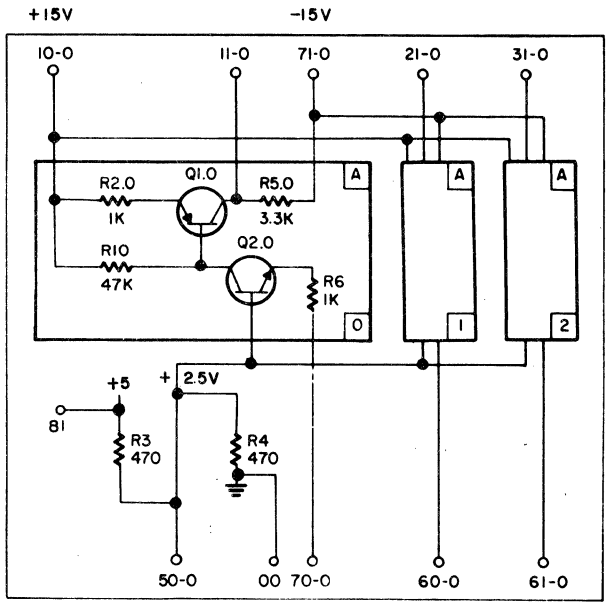


Figure 5-5. 35-162 Triple Bipolar Driver, Logic Diagram

5.7 35-163 QUAD BIPOLAR RECEIVER (DTL)

The 35-163 board, shown on Figure 5-6, consists of four circuits for receiving bipolar input signals and converting them to GE-PAC 30 standard logic levels. These circuits are designed to meet specifications as covered in EIA standard RS232B. A signal more positive than +3 volts produces a logic zero output and a signal more negative than -3 volts produces a logic one output. Pins 71, 70, 11, and 10 facilitate addition of external capacitors for reduction of a line noise. These pins can also be used to provide a slight negative bias (47K at -15v) for fail safe lines.

5.7.1 Specifications:

Power Requirements: 20 milliamps @ +5 volts

Size: Number 2 daughterboard

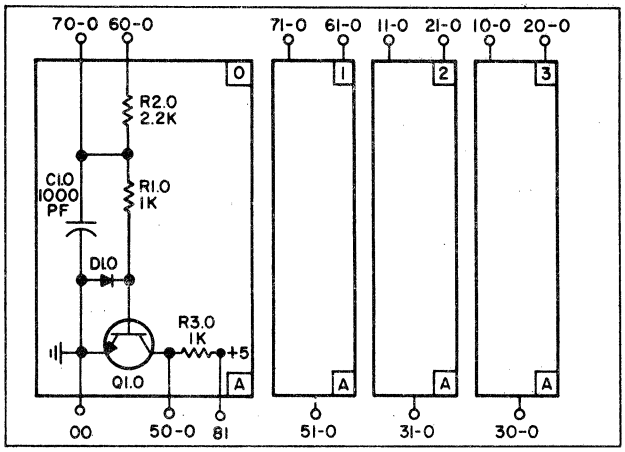


Figure 5-6. 35-163 Quad Bipolar Receiver, Logic Diagram

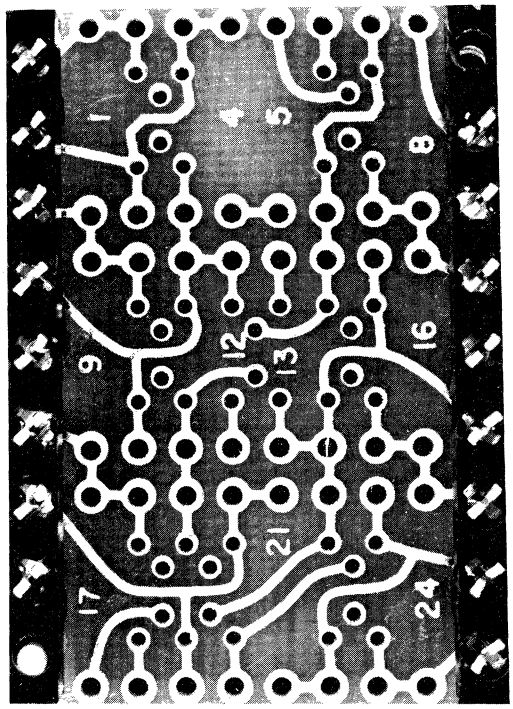
CHAPTER 6
MECHANICAL COMPONENTS

6.1 INTRODUCTION

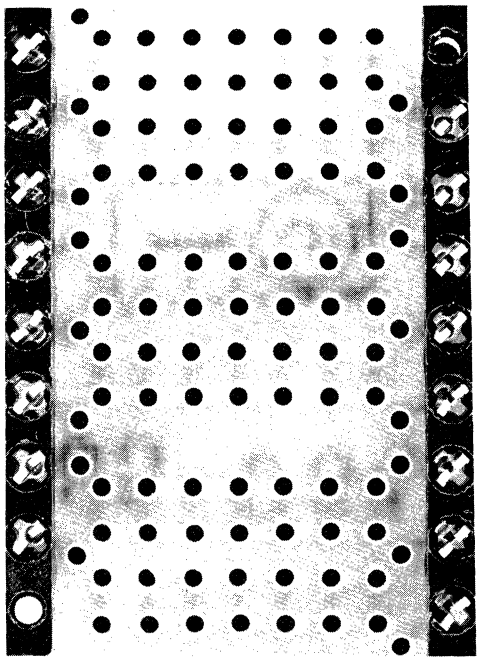
This Chapter describes several general purpose components available for custom applications. Included are a utility daughter-board designed to mount discrete component circuits, a general purpose mother-board, and a card file. A brief description and a photograph of each unit is provided. Additional information may be found in the Systems Interface Manual, GE-PAC 30 Publications Number PCP-126.

6.2 35-084, 35-085, and 35-038 UTILITY DAUGHTER-BOARDS

Blank number 2 size (1.1" by 0.25") daughter-boards are available. The 35-085 board, shown on Figure 6-1a, is designed to mount discrete components. The 35-084 board, shown on Figure 6-1b, is designed to mount dual in-line integrated circuit modules. The 35-038 Board is a Strap Board in which the daughter-board pins can be cross connected in any desirable configuration. The 35-038F00 version contains pins for wire-wrapping; the 35-038F01 is used for soldered cross connections. Typical applications are as address strap boards in core memory blocks and I/O controllers. Each board is equipped with 16 pins for electrical connection, and 1 guide pin to assure proper mechanical alignment on the mother-board field.



a. 35-085 Board-Discrete Components



b. 35-084 Board-Integrated Circuits

Figure 6-1. Utility Daughter-Boards

6.3 35-050 GENERAL PURPOSE MOTHER-BOARD

The 35-050 General Purpose Mother-Board provides locations for up to 40 number 2 daughter-boards, up to 20 number 3 daughter-boards, or any combination of the two sizes. The 35-050 board is supplied with wire wrap pins installed, printed wiring supplying ground and +5 volts to each field, 16 test points on the outer end of the Mother-Board, thirty-five 1K pull-up resistors connected to +5 volts, and two 69-pin connectors. The size of the mother-board is 9.75" by 10.5" by 0.5".

Pairs of feed through holes in the vertical columns between daughter-board locations are provided for mounting external circuit accessories such as diodes, resistors, capacitors, etc. Each feed through hole is connected to the wire-wrap pin (R04, R24, R41, etc.) which connects to +5 volts through a 1K pull-up resistor. Simple or complex networks can be formed by appropriate connections between component wire-wrap pins and daughter-board wire-wrap pins. If a pair of feed through holes is to be used for mounting a single component not requiring the services of the 1K pull-up resistors, the resistors must be removed from the two "R" locations used by the component.

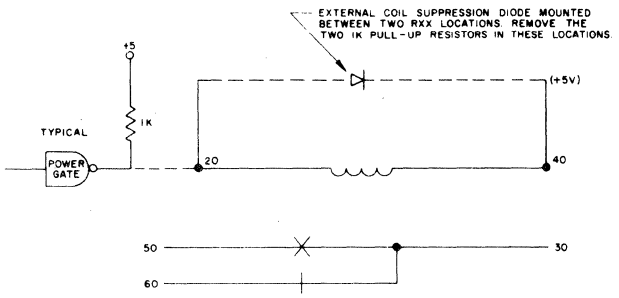
The 35-050 mother-board also has provisions for mounting 16 indicating lamps (GE-PAC 30 Part Number 33-011 or Sylvania Part Number 12ESB) in locations 40 through 47 (in locations 45 and 47 if potentiometers are not used). Each of these daughter-board locations has two pairs of feed through holes for connecting two lamps. The bottom holes of each pair are connected together to a common wire-wrap pin provided for lamp power. The top hole in each pair connects to a test point at the outer end of the mother-board. P type gates are used to drive these lamps.

Up to eight trimpots can be accommodated in locations 45 and 47. GE-PAC 30 Part Number 21-003F01 (Bourns Type 2600P-102 or equivalent, 1K ± 10%, 1W) and/or Part Number 21-003F02 (Bourns Type 2600P-103 or equivalent, 10K ± 10%, 1W) are used in these locations.

Four SPDT reed relays, GE-PAC 30 Part Number 36-001, can be plugged into locations 00, 10, 20, and 30 respectively. Each location provides appropriate holes that will accept the relay pins. The type of relay applicable, its specifications, and circuit follow.

Magnecraft Electric - Type W104MPCX-1 Reed Relay SPDT, True Form C, no biasing magnet

Coil - DC: 5 volts, 70 ohms
Operate Time: 1 ms. avg. Release 1 ms avg.
Contact Bounce: Less than 0.5 ms avg. - N. O. contacts
Less than 2.0 ms avg. - N. C. contacts
Contact Load Rating: 3V max. @ 0.25 A max or
28V max. non-inductive
Contact Resistance: 150 milliohms avg.
Capacitance across Contacts: 1.5 Pf avg.
Life Expectancy: 10 million cycles at full load
Operating Position: Any



6.4 12-001 CARD FILE

The 12-001 Card File, and back panel assembly, shown on Figure 6-2, mounts in a standard 19" rack and requires 10 1/2" of front panel space. The back panel will accept 13 wire-wrap mother-boards and is available in intermediate sizes on special order. Efficient power distribution is provided by the use of laminated bus bars. The bus bars extend the length of the back panel and have wire-wrap pins adjacent to each back panel connector to permit connections to appropriate circuits. Bus bars are available with 1, 2 or 3 conductors to meet other requirements. Cooling fan assemblies can be supplied.

6.5 35-104 STANDARD I/O BOARD

The 35-104 Standard I/O Mother-Board which is shown on Figure 6-3, is essentially a mother-board which contains the bus communication and interrupt circuits used on most device controllers. (See System Interface Manual PCP-126for circuit details) The integrated-circuit logic that provides these features is mounted directly on the mother-board in a field near the lower connector (Connector 0). The address straps for device number selection are wired in a field at location 20. The standard I/O Board provides 28 daughter-board locations, 23 1K pull-up resistors connected to +5 volts, and 16 test points on the

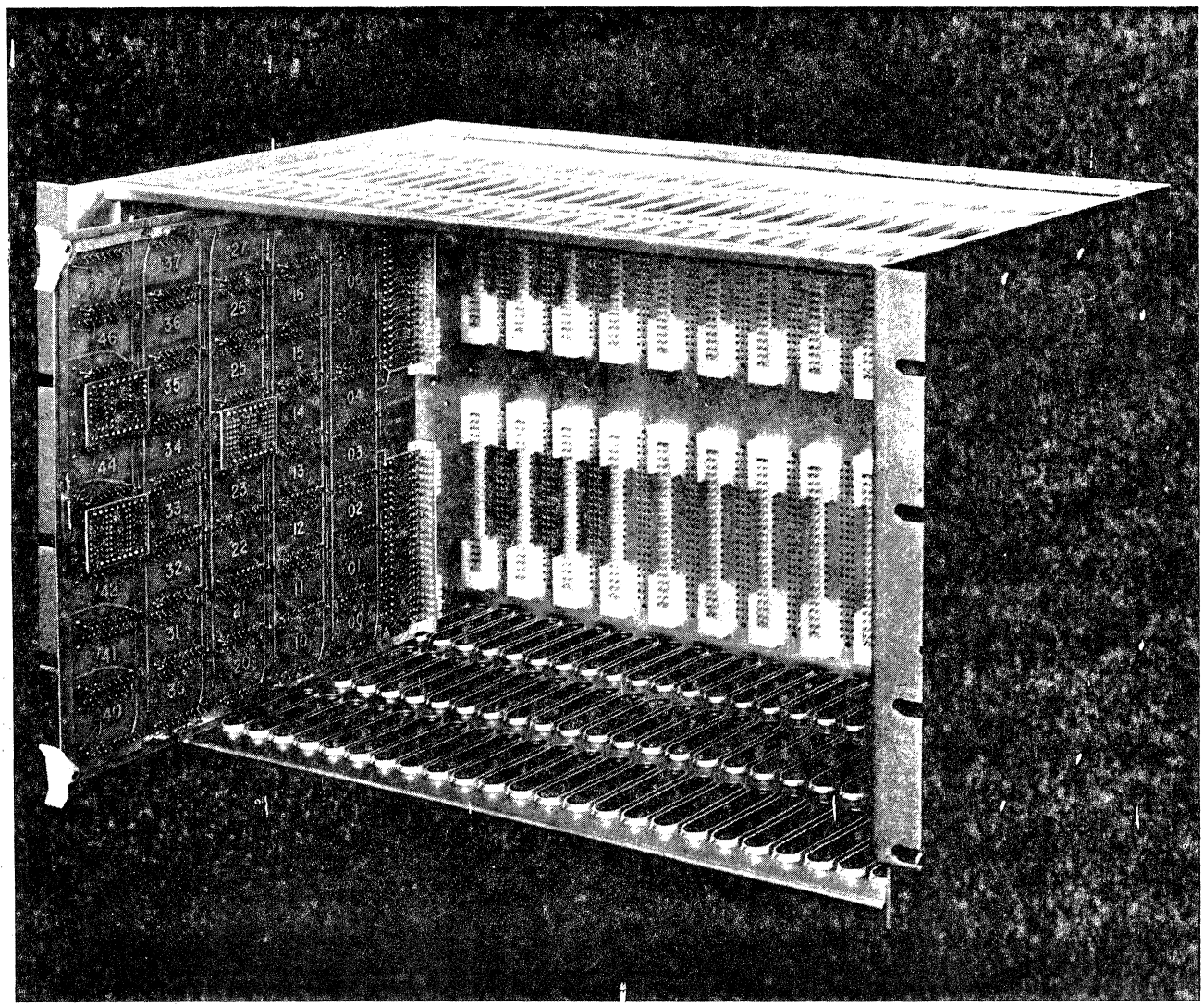


Figure 6-2. 12-001 Card File

outer end of the mother-board. The size of the mother-board is 9.75" by 10.5" by 0.5".

Pairs of feed through holes in the vertical columns between daughter-board locations are provided for mounting external circuit accessories such as diodes, resistors, capacitors, etc. Each feed through hole is connected to the wire-wrap pin (R04, R24, R41, etc.) which connects to +5 volts through a 1K pull-up resistor. Simple or complex networks can be formed by appropriate connections between component wire-wrap pins and daughter-board wire-wrap pins. If a pair of feed through holes is to be used for mounting a single component not requiring the services of the 1K pull-up resistors, the resistors must be removed from the two "R" locations used by the component.

Up to eight trimpots can be accommodated in locations 45 and 47. Generally, GE-PAC 30 Part Number 21-003F01 (Bourns Type 2600P-102 or equivalent, 1K

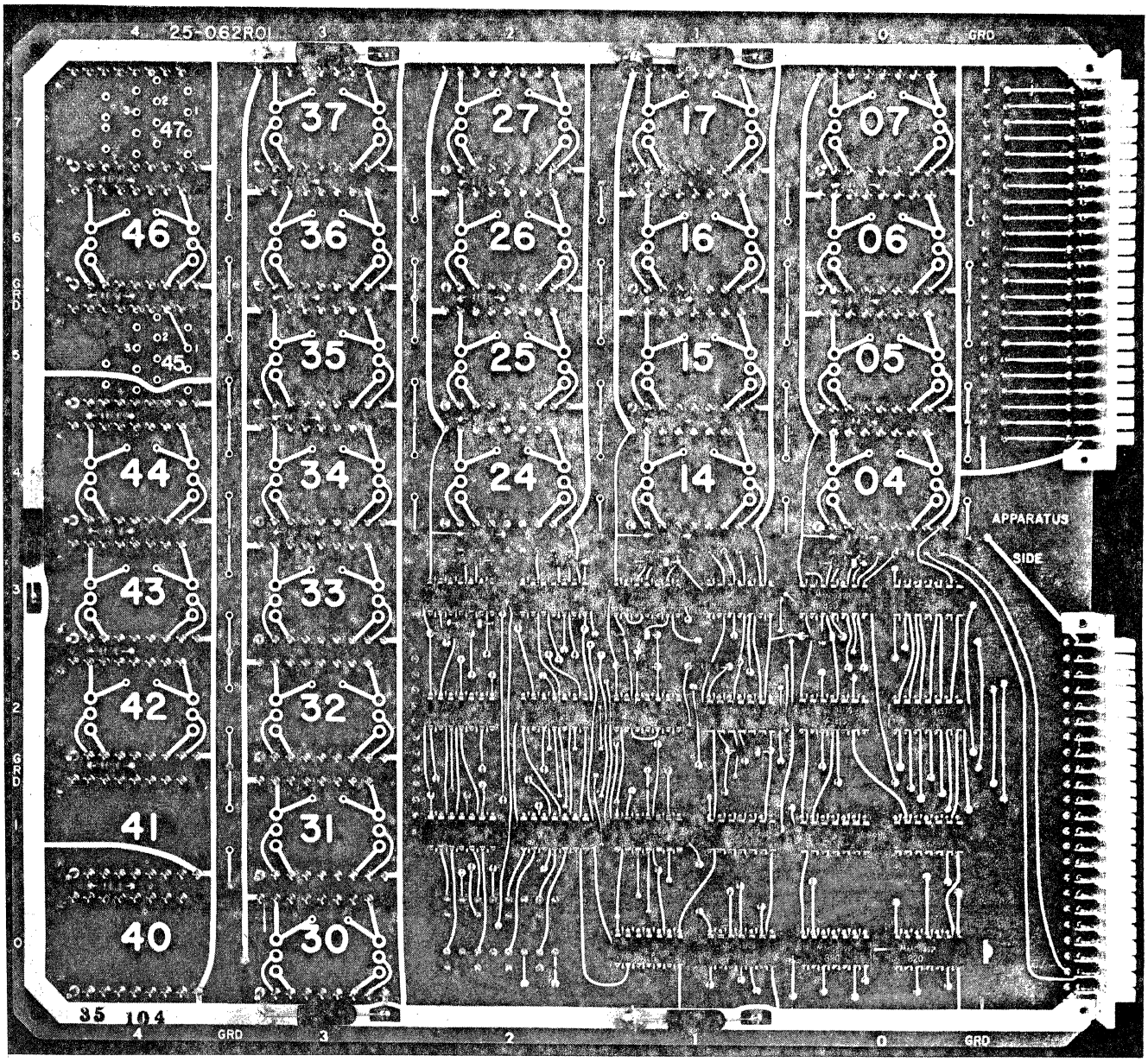
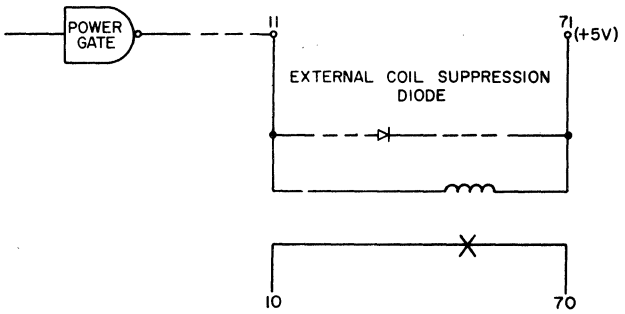


Figure 6-3. Apparatus Side of Standard I/O Mother-Board

± 10%, 1W) and/or Part Number 21-003F02 (Bourns Type 2600P-103 or equivalent, 10K ± 10%, 1W) are used in these locations.

In addition, space to mount up to 24 reed relays, GE-PAC 30 Part Number 36-005 in various daughter-board locations is available (Note that the relays for the 35-104 are not the same as those used on the 35-050 board). Each relay location is identifiable by six feed through holes. Six clips (in two groups of three each) are soldered in the six holes. The relay is then inserted into these clips. It is recommended that GE-PAC 30 Part Number 26-043 (Berg Electric 4559 or equivalent) clips be used. Each grouping of six holes has a guide hole to insure correct insertion of the relay. Two smaller holes, between terminals 11 and 71, in each grouping are for mounting coil suppression diodes. The type of relay applicable, its specifications, and circuit follow.

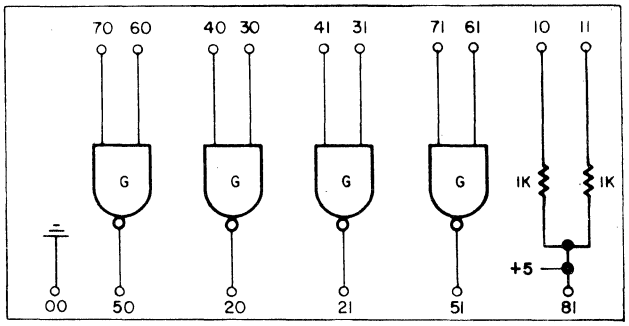
IBM Type 766060 Reed Relay 1 position, Form A, Pick
Coil - DC: 5 volts, 241 ohms, 25 ma.
Operate Time: 2 ms
Release Time: 2 ms
Contact Rating: 500 ma @ 50 vdc
25 ma @ 115 vac
Breakdown Voltage: 300 vdc
Contact Resistance: 100 milliohms
Life Expectance: 150 million operations



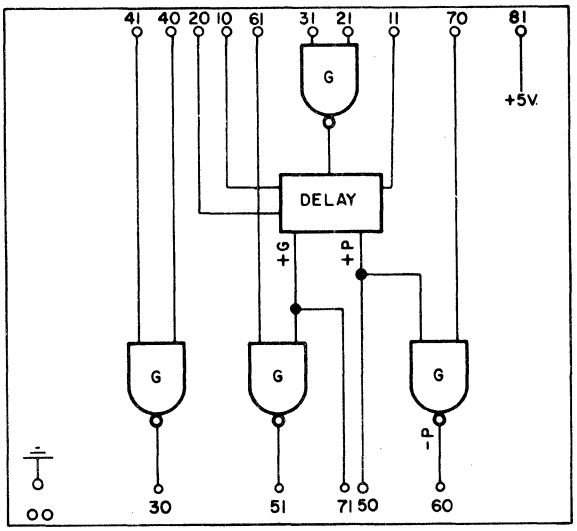
6.6 35-069 BACK PANEL CONNECTOR

The 35-069 Back Panel Connector is a female connector unit with 46 terminals that can be inserted over any male back panel connector to provide external access to a mother-board. All 46 female terminals are brought out to 46 wire-wrap pins for external wiring options.

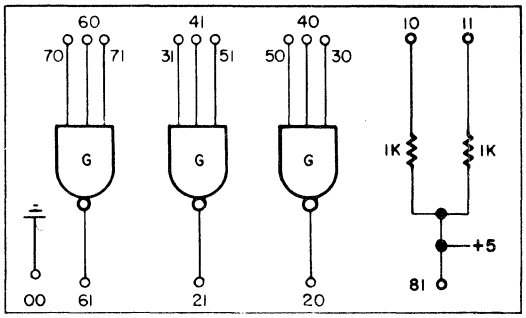
APPENDIX 1
LOGIC SCHEMATIC SUMMARY



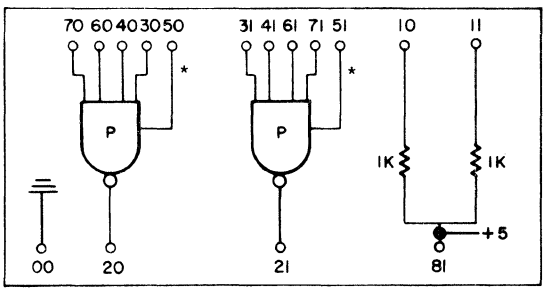
35-001 Quad 2 Input NAND Gate, Logic Diagram



35-008 Variable Delay Generator, Logic Diagram

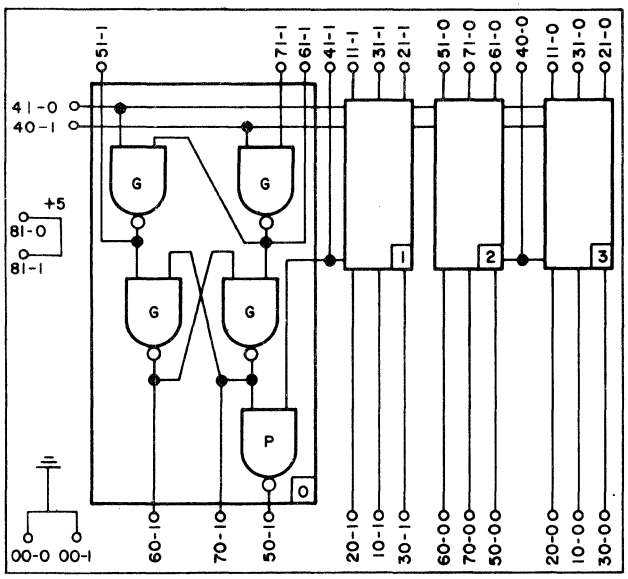


35-002 Triple 3 Input NAND Gate, Logic Diagram

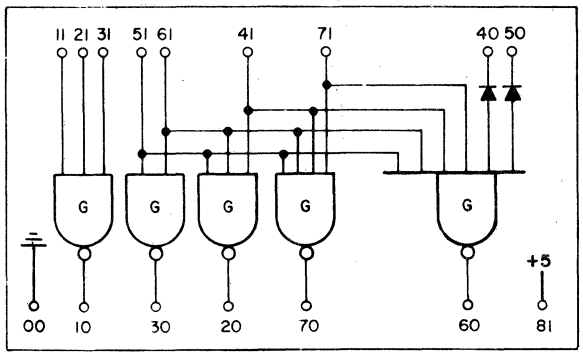


*MUST HAVE DIODE INPUTS

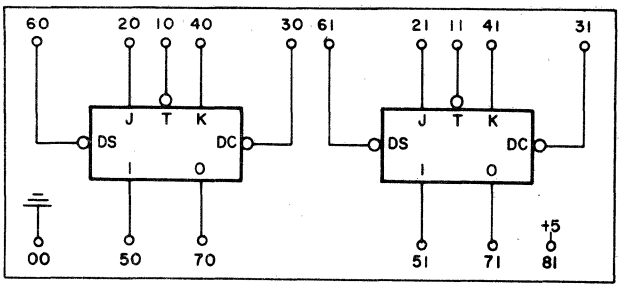
35-003 Dual 4 Input NAND Power Gate, Logic Diagram



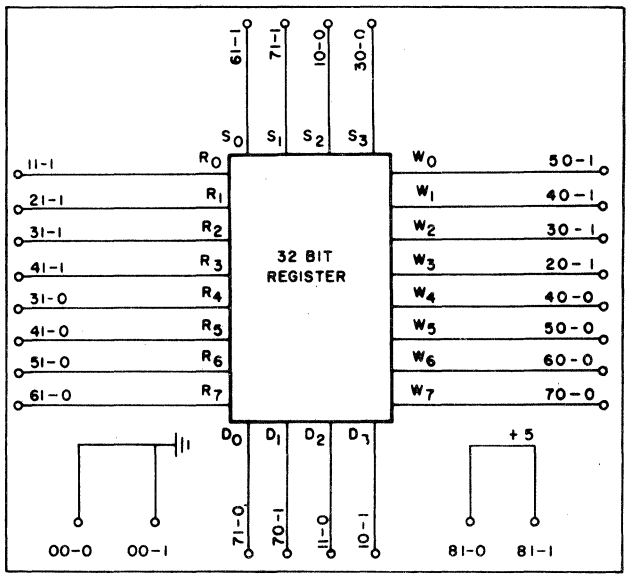
35-009 4 Bit RS Register with Gates, Logic Diagram



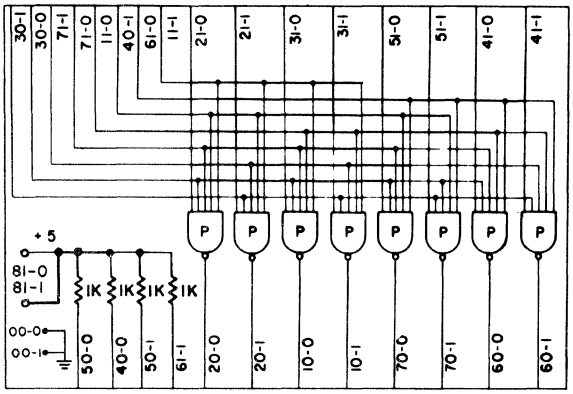
35-013 4 Bit Counter Carry, Logic Diagram



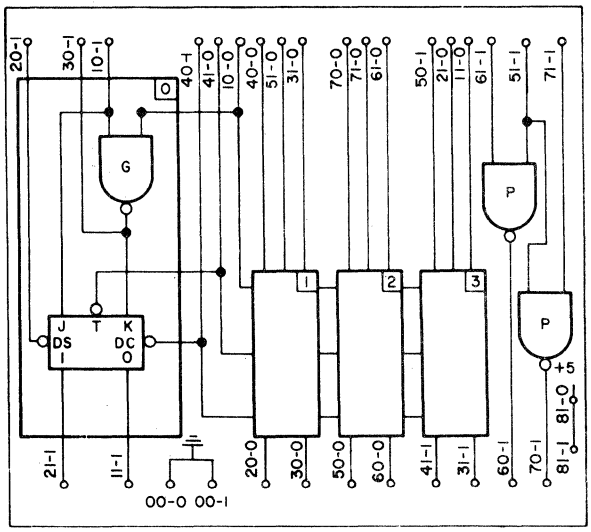
35-016 Dual JK Flip-Flop, Logic Diagram



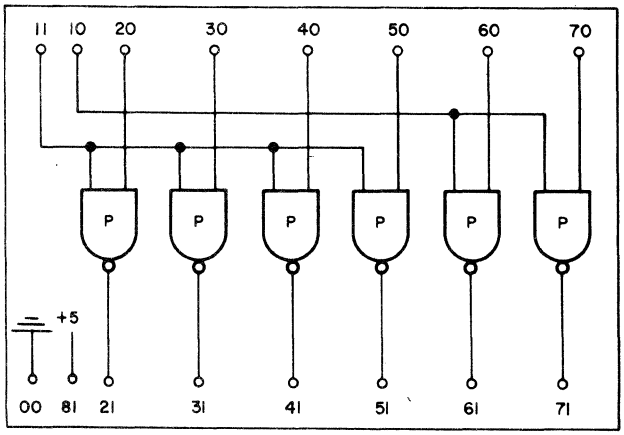
35-014 4 Bit By 8 Word Register Stack, Logic Diagram



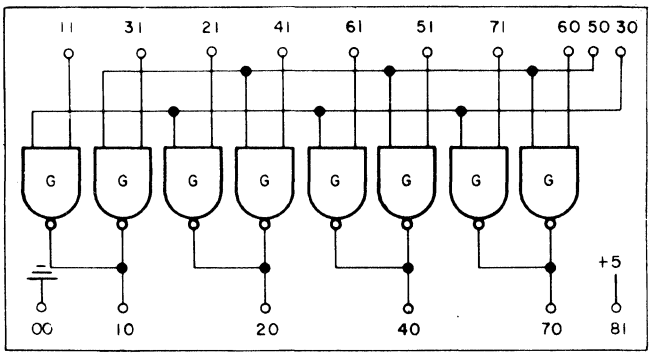
35-019 1 Out of 8 Decoder, Logic Diagram



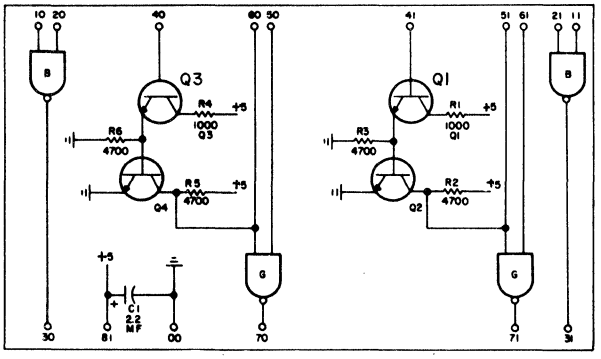
35-015 4 Bit JK Register, Logic Diagram



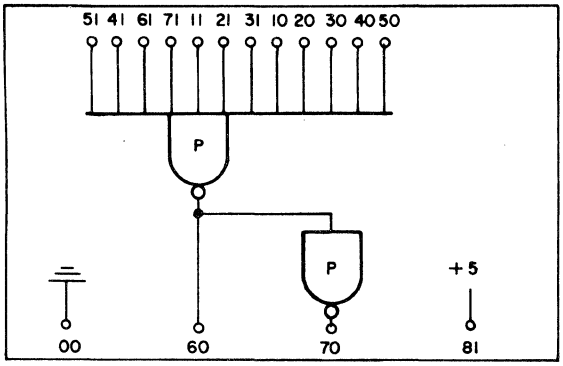
35-020 Hex Gated Power Gate, Logic Diagram



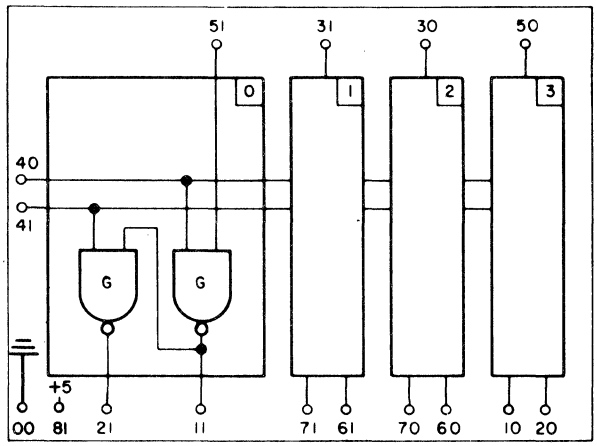
35-021 Quad Gated NOR Gate,
Logic Diagram



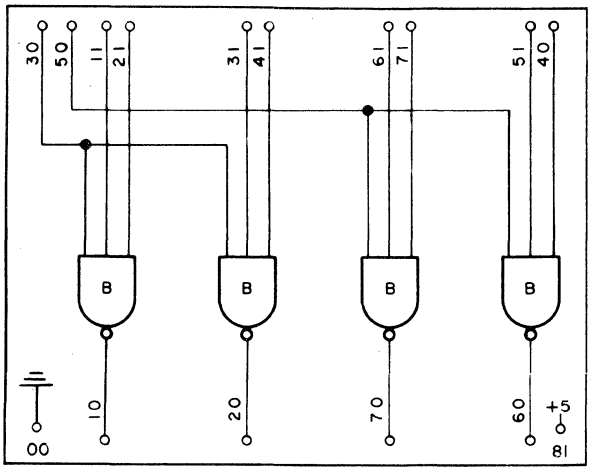
35-027 Dual Differentiator, Logic Diagram



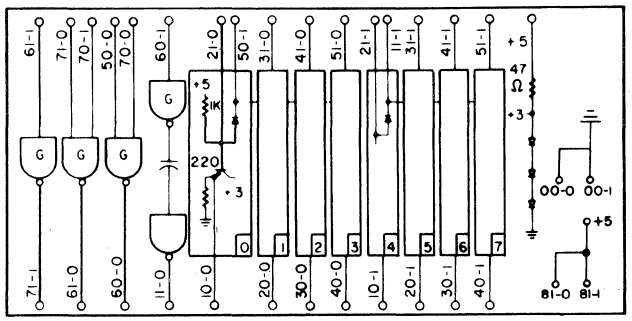
35-022 12 Input NAND Gate,
Logic Diagram



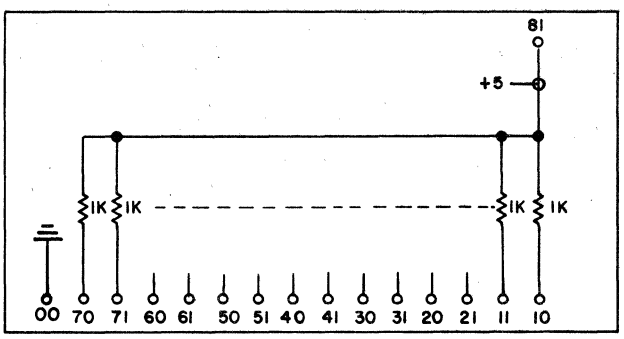
35-040 Single-Double Rail Converter,
Logic Diagram



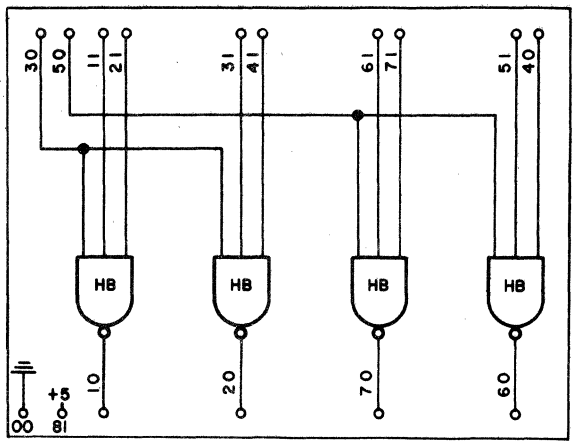
35-023 Quad Gated Buffer, Logic Diagram



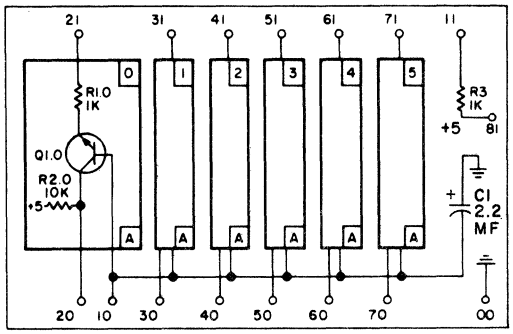
35-041 8 Bit Stack Driver,
Logic Diagram



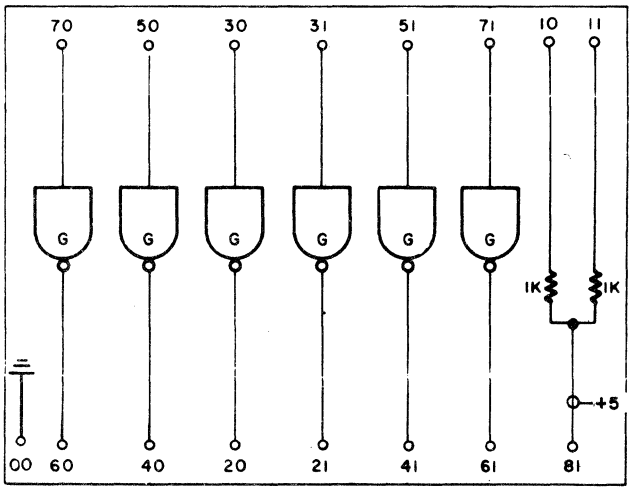
35-045 Fourteen 1K Resistor Module, Logic Diagram



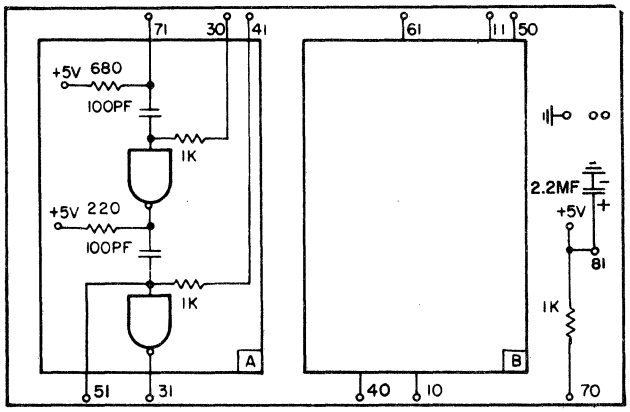
35-059 Quad Gated Buffer, Logic Diagram



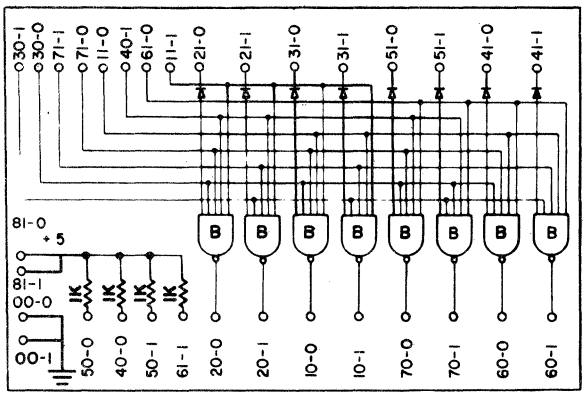
35-046 Negative to Positive Converter, Logic Diagram



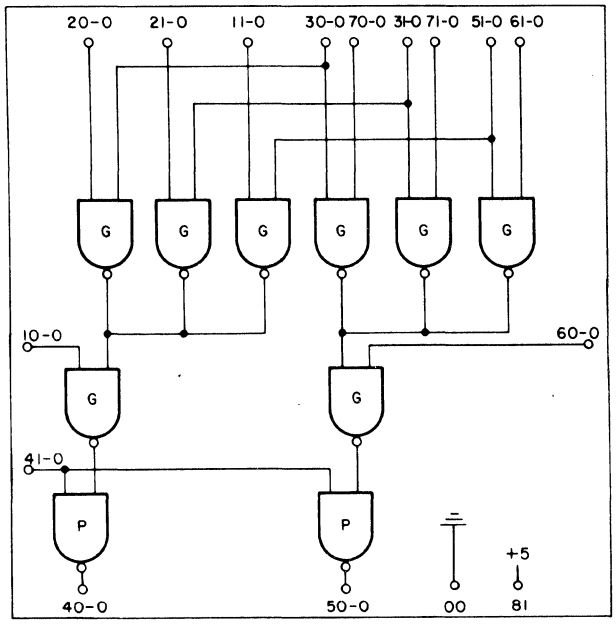
35-060 Hex Inverter, Logic Diagram



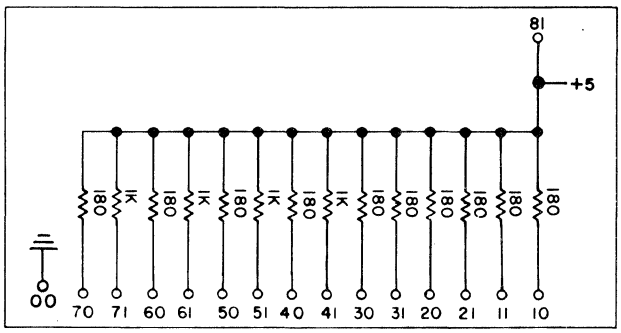
35-053R02 Dual Adjustable Timing Network, Logic Diagram



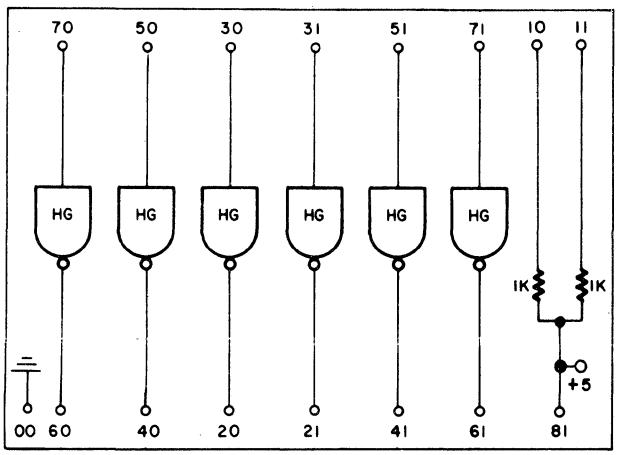
35-064 1 Out of 8 Decoder Buffer, Logic Diagram



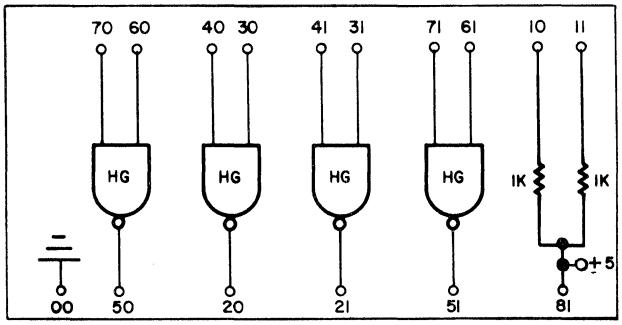
35-079 Multiplexed Bus Driver, Logic Diagram



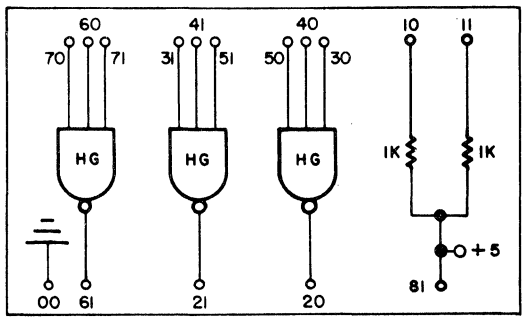
35-099 Bus Terminating Resistor Module, Logic Diagram



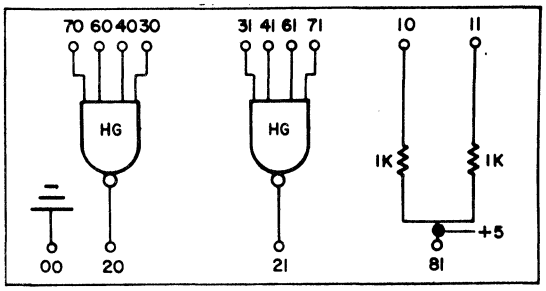
35-115 Hex Inverter, Logic Diagram



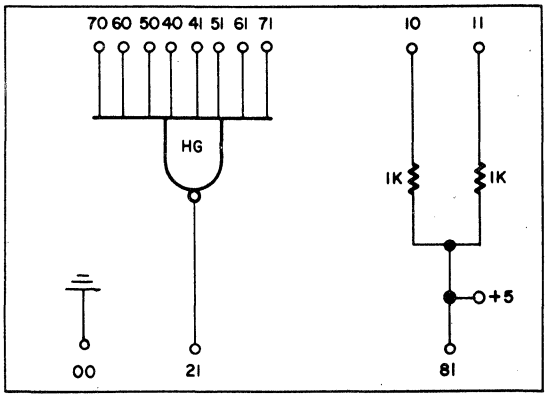
35-116 Quad 2 Input NAND Gate, Logic Diagram



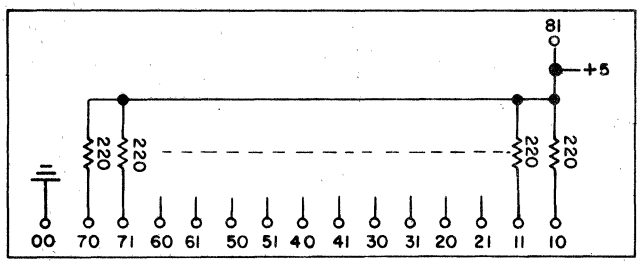
35-117 Triple 3 Input NAND Gate, Logic Diagram



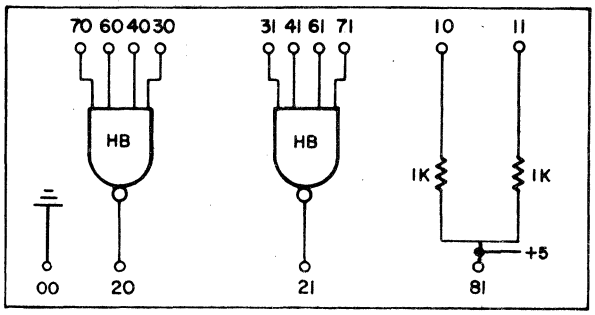
35-118 Dual 4 Input NAND Gate, Logic Diagram



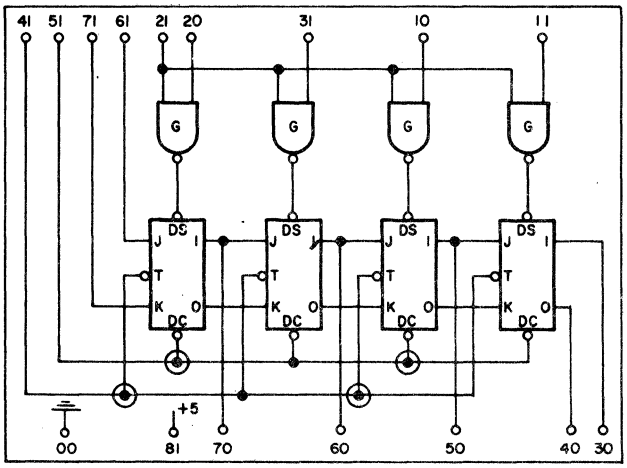
35-119 8 Input NAND Gate, Logic Diagram



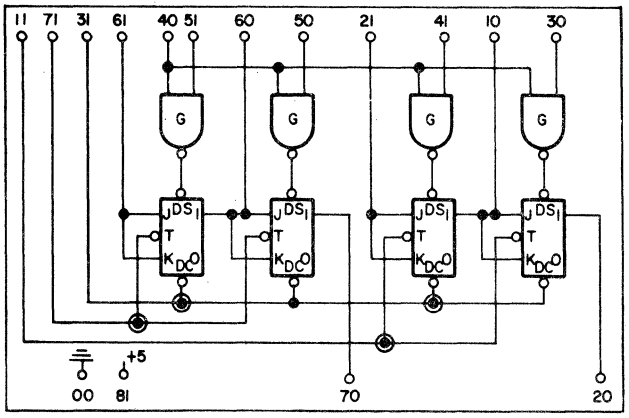
35-122 Fourteen 220 Ohm Resistor Module, Logic Diagram



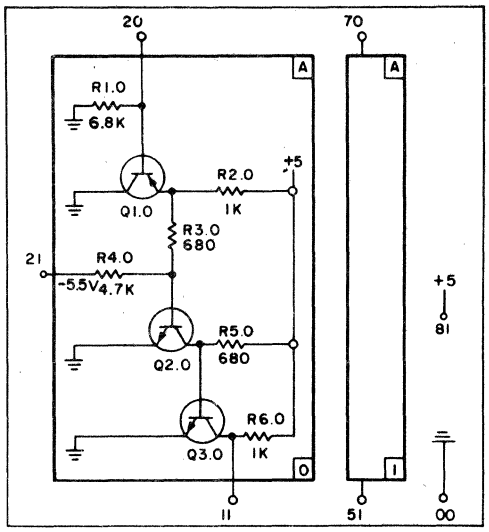
35-128 Dual 4 Input Buffer Gate, Logic Diagram



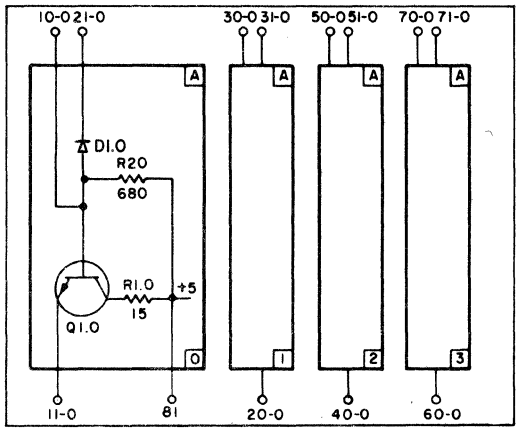
35-134 Four Bit Serial Parallel Converter, Logic Diagram



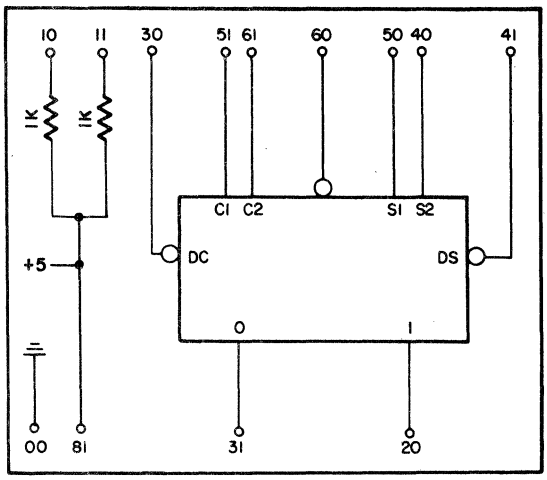
35-136 Four-Bit Counter, Logic Diagram



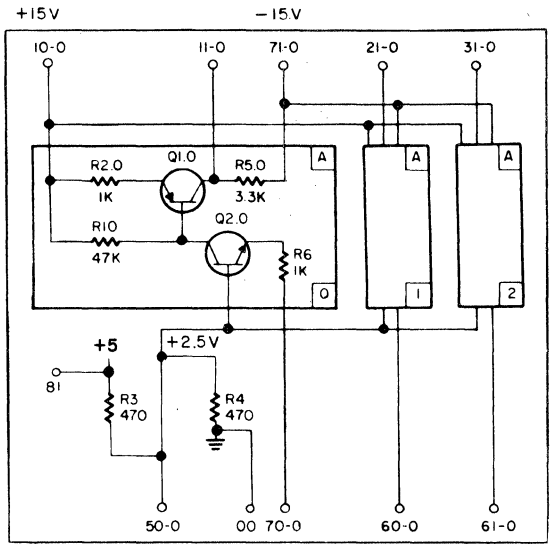
35-154 360 Bus Receiver, Logic Diagram



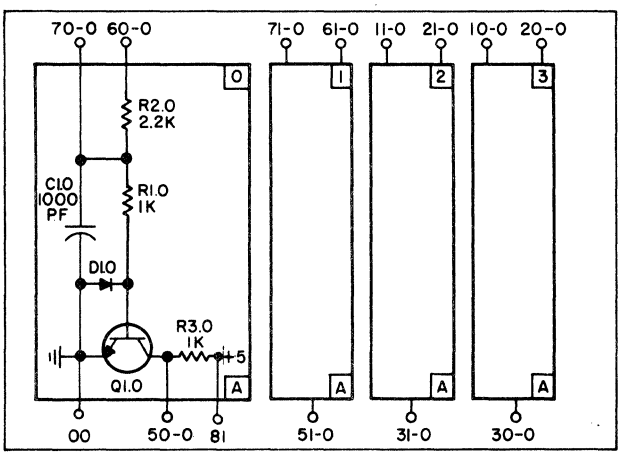
35-155 360 Bus Driver, Logic Diagram



35-157 Clocked Flip-Flop, Logic Diagram



35-162 Triple Bipolar Driver,
Logic Diagram



35-163 Quad Bipolar Receiver,
Logic Diagram

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