GE Number 3010AE21-T

KEYBOARD PRINTER I/O CONTROLLER MAINTENANCE MANUAL

Consists of:	Installation Specification	02-123R01A20
	Maintenance Specification	02-123R02A21
	Schematic	02-123R05D08

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March, 1972

1. GENERAL

The Keyboard Printer I/O Controller is a one mother-board interface which adapts the Selector Channel or Multiplexor Channel Bus to either the General Electric Terminet 300 Terminal, the Model 37 Teletype, or the 33/35 Teletype in the Full-Duplex Mode. It is also capable of adapting either the Terminet or Model 37 via a 103A Data Set, or equivalent Data Set, to the Selector Channel or Multiplexor Channel Bus.

2. TERMINET 300 AND MODEL 37 CONNECTIONS

The Controller may be installed in any I/O slot of a main or expansion file. Remove RACK0/TACK0 strap between back panel Terminals 114-0 and 214-0 at the location of controller.

Install 17-069F01 cable between location 40 of Controller and the connector plate (14-090 or 14-127) at the rear of the cabinet. (See Figure 1.) Install 17-082F01 cable between connector and the device (Terminet 300 or Model 37 TTY).

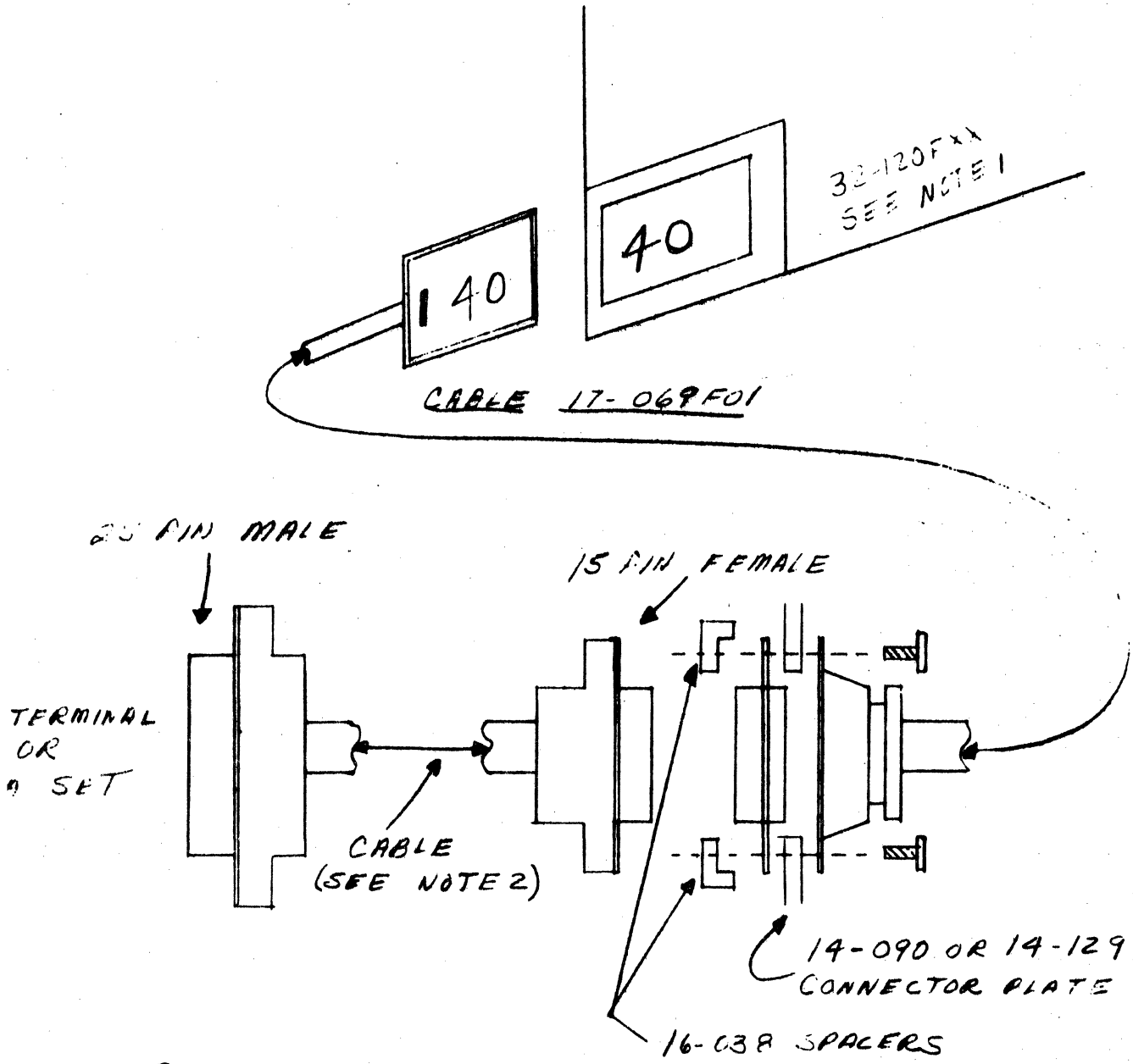
3. 103A DATA SET CONNECTION

Repeat Step 2, except use a 17-050 cable between connector plate and Data Set (see Figure 1).

4. 33/35 TELETYPE INSTALLATION (See Figure 2)

The Controller may be installed in any I/O slot of a main or expansion file. Remove RACK0/TACK0 strap between back panel Terminals 114-0 and 214-0 at location of Controller. Install 17-031 cable as shown in Figure 2.

Load and run Test Program 06-083M14 or 06-004M14.



TE 1 32-120F02 — MODEL 37 TELETYPE

32-120 F03 — GENERAL ELECTRIC TERMINET 300

E 2 CABLE SELECTION

DIRECT CONNECTION TO TERMINAL USE 17-082F01

CONNECTION TO DATA SET USE 17-050F01

CONTROLLER CONNECTIONS

FIGURE 1

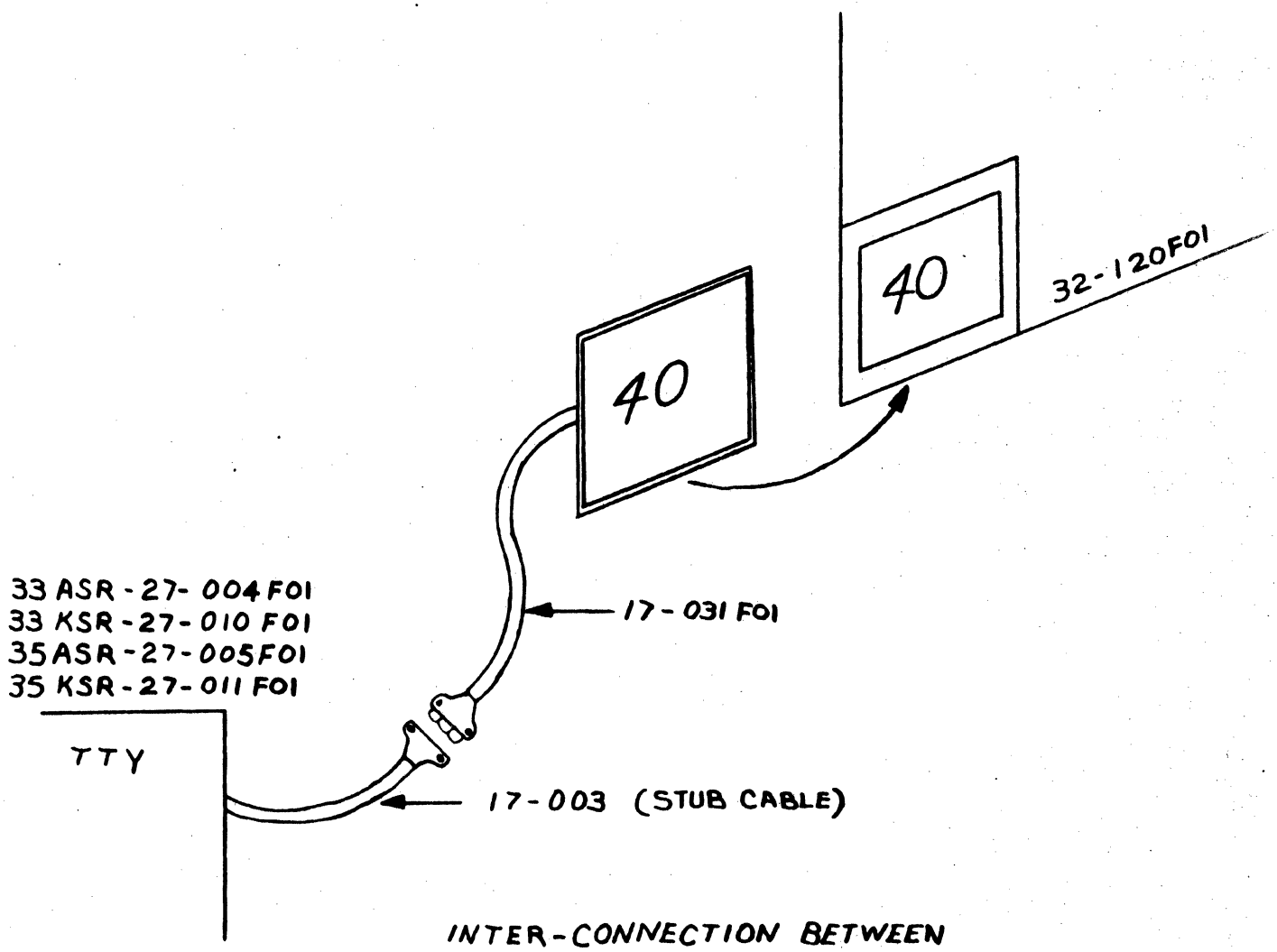

40
40
32-120F01
33 ASR-27-004 F01
33 KSR-27-010 F01
35 ASR-27-005F01
35 KSR-27-011 F01
17-031 F01
TTY
17-003 (STUB CABLE)
INTER-CONNECTION BETWEEN
TTY AND CONTROLLER

FIG. 2

KEYBOARD PRINTER I/O CONTROLLER MAINTENANCE SPECIFICATION

TABLE OF CONTENTS

ILLUSTRATIONS

KEYBOARD PRINTER I/O CONTROLLER MAINTENANCE SPECIFICATION

1. INTRODUCTION

The Keyboard Printer I/O Controller is used to adapt various keyboard printer terminals to an INTERDATA Digital System. It converts serial eight level ASCII code (see Figure 1) to parallel form for processing by the computer.

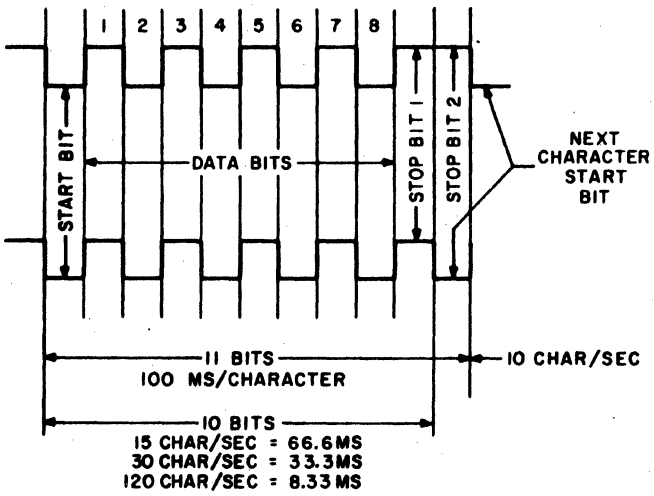


Figure 1. Serial ASCII Code U (Even Parity) Ten and Eleven-Bit Code

The following list gives several terminals which the Keyboard Printer I/O Controller will adapt to an INTERDATA Digital System.

1.	33 ASR/KSR Teletype	10 characters/second
2.	35 ASR/KSR Teletype	10 characters/second
3.	Model 37 Teletype	15 characters/second
4.	General Electric Terminet 300	30 characters/second

Other equivalent type terminals, which operate with the eight level ASCII code, could also be adapted to an INTERDATA Digital System by the K P I/O Controller. All terminals must be equipped for full-duplex operation. In addition to adapting the terminals directly to the computer, the K P I/O Controller can also support the terminals via a 103A Data Set. That is, a terminal may be separated from the Controller by 103A Data Sets.

Other optional features are:

1. Programmable speed control for Terminet 300 at 30 and 120 characters/second.
2. Hardware option to convert the Controller to operate with one Start bit, seven Data bits, and one Stop bit.

2. SCOPE

This Maintenance Specification is provided to describe the Keyboard Printer I/O Controller in sufficient detail to allow a digital technician to troubleshoot and maintain the interface. The following manuals will assist in understanding and maintaining the system as a whole.

29-193	INTERDATA K P I/O Operation and Programming Manual
	Vendor operating and service manuals for the particular terminal being used

3. BLOCK DIAGRAM ANALYSIS

The block diagram of the K P I/O Controller is shown on Sheet 4 of the Functional Schematic 02-123D08.

The circuitry for addressing, interrupt, and DRL line drivers is configured in the same manner as that of the Standard I/O Board. Refer to System Interface Manual, Publication Number 29-003. The DAL RCVRS, Control Line RCVR, SCLR0 gates, ADRS CKT, ACK gates, and the ATN/ACK CKT make up the standard I/O portion of the Controller.

The control circuits consist of Command flip-flops (Read or Write, etc.), circuits to direct the flow of information (Terminal to Processor or Processor to Terminal), and circuits to control the timer when transmitting to or receiving from the terminal.

On receiving from the terminal, the serial information is sampled by the timer and placed in a Data Register (shift register). When the end of character is detected, the information is placed in a byte Buffer Register from which the Processor takes the parallel data. The byte buffer allows the Processor one character time to accept the data.

ransmitting to the terminal, the information is placed ctly into the Data Register (shift register) and then t serially to the terminal under the control of the timer.

NOTE

On receiving, the data is taken from bit 0 to 7 of the Data Register; and on transmitting, the data is inserted into bit 1 to 8 of the Data Register.

coupler adapts the Controller to the terminal, i.e. either INTERDATA teletype levels, or to the RS 232 nterface levels.

Status gates place the status of the Controller on the X-CH Bus to the Processor. The Data Request gates ce the data on the MPX-CH Bus to the Processor.

tional speed control is available. The two speeds for Terminet 300 are 30 and 120 characters per second. ier speeds can be made available by changing the Char- er Timer. A four to one speed change can be made ler program control.

FUNCTIONAL DESCRIPTION ANALYSIS

e functional description of the K P I/O Controller is sed upon the Functional Schematic, 02-123D08.

4.1 Status and Commands

e definitions for the Status and Command bytes for the P I/O Interface are shown in Table 1. Since the interce is both an input and output device, the direction in ich the data is being handled is determined by the Read Write Mode. In the Read Mode, the interface is conioned to receive information from the terminal and nsfer it to the Processor. For transferring informan from the Processor to the terminal, the Write Mode required.

4.2 Initialization

hen the INITIALIZE pushbutton on the Processor is deessed, SCLR0 is applied to the interface to clear any nding interrupt, condition the interface for the Read, ock Mode, and Disable/Disarm the interrupt circuit.

4.3 Multiplexor Bus Communication

mmunication between the Processor and the interface via the standard I/O portion of the Controller, 02-123)8, Sheet 1. See System Interface Manual, Publication mber 29-003, for a description of the standard I/O eration.

4.4 Interrupt Circuit

The interrupt circuit is normally set up to allow queuing of interrupts in the Device Disable Mode. A hardware option (ARM, DISARM) may be incorporated to inhibit queuing of interrupts. This may be accomplished by strapping SCLR0C to EBL1 and removing the pull-up resistor at 12RR1. (See 02-123D08-1, Note 2.) The Interrupt flip-flop is held in the clear state until the ARM Command is received from the Processor.

4.5 Write Mode

In the Write Mode, the Controller is conditioned for outputting from the Processor to the terminal. The eleven-bit Shift Register (02-123D08-2) is used to convert the eight-bit data byte to a ten or eleven-bit serial pulse chain. The register is loaded in the following manner. The leading edge of DAG0 is differentiated to produce SRD0. SRD0 first sets DR00 through DRN0 and clears DRX. The SRD0 pulse is short and disappears before DAG0. On the remaining time of DAG0, data is loaded into register DR01 through DR08 by inserting zeros where they appear on DAL000A through DAL070A, DRN is cleared, and DRX is set for an eleven-bit code or cleared for a ten-bit code. The DT flip-flop is cleared, along with setting the Timing flip-flop, TMG, which starts the timer by DAG1A. With DT1 low, zeros will be shifted into the register and propagated by Shift pulse, TRD1. The serial output from DRN, which is produced by shifting the content of the register, is gated with DT0 and TMG1 to produce TRNS0.

The hardware option of eleven or ten-bit code is obtained by the presence or absence of the fifteen ohm resistor, 14RR1. For an eleven-bit code, resistor 14RR1 is removed to allow DRX to be set for the second Stop bit.

On output, the end of character gate is generated when the content of DRX, DR00 through DR07, is all zeros and TRD1 goes high. The Timing flip-flop, TMG, is cleared by EOC0 which stops the timer. When the timer stops, the last shift pulse is generated and shifts the content of the Shift Register one more time.

The Start bit is contained in DRN and the one or two Stop bits are contained in DRX and/or DR0. One Stop bit for ten-bit code, and two Stop bits for eleven-bit code.

The interface BSY condition goes true in the Write Mode as soon as the timer starts (02-123D08-3). It remains true until the information is shifted from the Data Register. With the detection of End Of Character, the BSY condition goes false and an interrupt is generated by setting the ATN flip-flop (see Figure 2A). When changing from the Read to Write Mode, an interrupt is also generated (see Figure 2B).

TABLE 1. KEYBOARD I/O CONTROLLER
STATUS AND COMMAND BYTE CODING

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE	ERR		BRK	STBY RING*	BSY	EX		DU
COMMAND BYTE	DISABLE*	ENABLE*	UNBLOCK	BLOCK	WRT	READ	CB1*	CB2*

ERR The Error bit is set when a character is not taken from the controller buffer before another character from the terminal has been assembled. ERR is reset on OC Read, Data Request, and System Initialization.

BRK The Break bit is set at the end of one character time when the line is held in the space condition for a period greater than a character period.

STBY RING* The Standby bit is used with the General Electric Terminet 300. It is set when the terminal is on-line and reset on the following conditions:

1. Manually placing terminal in Standby Mode.
2. Issuing an End Of Transmission character, EOT, to the terminal.
3. When the terminal is manually placed in the 120 character/second operation.

When supporting the Terminet 300 via a 103 Data Set, this Status bit indicates the presence of the ON state of the Data Set Ring lead.

BSY Read Mode - The Busy bit is normally set and is reset when data is available for transfer to the Processor.

Write Mode - The Busy bit is normally reset and is set when data is being transferred to the terminal.

EX The Examine bit is set when BRK or ERR bits are set.

DU The Device Unavailable bit is set as follows:

Terminal	
33/35 TTY	Power off or Local Mode.
Mode 37 TTY	Power off and when Reader, Punch, and Printer are all off-line.
Terminet 300	Power off or Local Mode.
103A Data Set	Carrier lead of the Data Set is in the Off state.

DISABLE* Disables device interrupts; allows queuing of interrupts.

ENABLE* Enables device Interrupts.

UNBLOCK Allows Printer to print data entered via the keyboard or tape reader.

BLOCK Disables the UNBLOCK feature.

*See Optional Features (4.11)

TABLE 1 (Continued)

WRT	The Write Command is used to place the interface in the Write Mode, which allows data to be transferred to the device.
READ	The Read Command is used to place the interface in the Read Mode, which allows data to be transferred from the device.
CB1* CB2*	These two Control bits are decoded to obtain the following interface command.

1. CB1 = 0, CB2 = 0 — This condition is used when operating with the 33/35/37 TTY and to select the 30 character/second rate of the Terminet 300.
2. CB1 = 1, CB2 = 1 — This condition selects the 120 character/second rate of the Terminet 300.
3. CB1 = 1, CB2 = 0 — This condition places the DUR lead in the ON state.
4. CB1 = 0, CB2 = 1 — This condition places the DUR lead in the OFF state.

*See Optional Features (4.11)

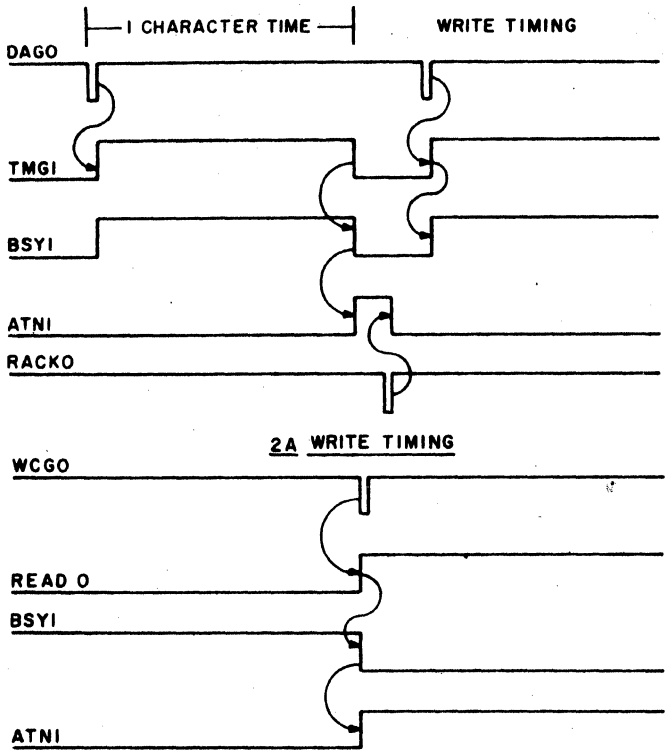


Figure 2. Read to Write Timing

4.6 Read Mode

The Controller is placed in the Read Mode by the appropriate Output Command, to transfer information from the terminal to the Processor. The input operation (see 02-123D08, 1 and 2) is initiated when the Start bit of the serial information is received by the input coupling circuits. The Timing flip-flop (TMG) is set when the normal, closed loop, high state of DD1 goes low. The RDY flip-flop has been in the set state, and together with TMG0, will have generated AST0 and AST1. As DD0A goes high, ST0 is generated and sets TMG, DT, TMD, clears RDY, and produces SDR0. SDR0 loads the Shift Register, DR00 through DRN, with all ones. DRX is cleared by SDR0.

Shift pulses (TRD1) are generated which sample the serial data near the center of each bit and insert it, one bit at a time, into the Shift Register. When the Start bit has been shifted through to DR07, the next TRD1 pulse, gated by DRS0 and DT1, generates EOC0. When EOC0 occurs, the timer is stopped and the EOC pulse shifts the Data Register one more time. With the last shift, the Stop bit is contained in DRX.

NOTE

On input, the interface is always conditioned for the ten-bit code: One Start, eight Data, and one Stop bit.

The information contained in DR00 through DR07 is transferred to a Byte Buffer Register (02-123D08-3) when the Stop bit is shifted into DRX. When DRX goes high and DRN contains the leading zero, LBBG is generated and gated by READ0 to load the information into the Byte Register (DR001B through DR071B). When the Byte Register is loaded, RB1 goes low, the Controller becomes non-busy at this time, and an interrupt is generated (see Figure 3). The Controller stays non-busy until the Processor takes the data from the Byte Register. The Byte Register retains the information for one character time.

4.7 Timing Circuits

The timer (02-123D08-2) is a gated oscillator type timer and consists of a 35-037 Timing Network, a 35-027 Pulse Differentiator, and a 35-020 Gated Pulse Inverter. Frequency of the timer is a function of the 35-037 Timing Network. The following frequencies are used for particular character rates:

Option F	10 characters/second	440 Hz	
	15 characters/second	600 Hz	
Option G	30 characters/second	4800 Hz	Programmable Speed Control
	120 characters/second	4800 Hz	

For the ten and fifteen characters/second rate, the basic frequency is divided by four, and the programmable speed control is inhibited by the fifteen ohm resistor, 15RR1. SC1 is forced high, which enables the TRD0A gates for the character rate which requires a division of four. With the resistor 15RR1 removed, the state of the SC flip-flop is under the control of the two control bits, CB1 and CB2. When the SC flip-flop is set (SC1 high), a division of the basic timer frequency is four. A division of sixteen occurs when the SC flip-flop is reset. For the ten and fifteen characters/second rate, the basic frequency is divided by four. The programmable speed control option is not incorporated.

The program speed control option is incorporated by equipping the Controller with the dual JK flip-flop at location 42R (3K2). With the speed control option, the frequency of TRD1 is selected by the state of the SC flip-flop, which is under the control of the two control bits, CB1 and CB2. When the SC flip-flop is set (SC is high), a division of the basic timer frequency is four. A division of sixteen occurs when the SC flip-flop is reset (SC0 is high).

At the 30 and 120 characters/second rates, the basic frequency is divided by four for the 120 characters/second rate, and by sixteen for the 30 characters/second rate.

4.8 Command, Status, and Data Request Circuits

The interface (see 02-123D08-2 and 3) is placed in the different operating modes by an Output Command with the appropriate bit in the byte being set. Bits six and seven of the Command byte are decoded to produce four interface controls.

1. Low speed character rate.
2. High speed character rate.
3. Data Unit Ready (ON). } DUR
4. Data Unit Ready (OFF). }

tional program control of the DUR lead can be incor-
rated by removing the fifteen ohm resistor, 20LR2.
ta Unit Ready has several functions. If the Controller
directly connected to a Terminet 300, Model 37 Tele-
ɔe or equivalent terminal, the DUR lead functions as
ta Set Ready ON or OFF. When the above terminals
e separated from the Controller by 103A Data Sets, the
JR lead serves as Data Terminal Ready ON or OFF.
ɪrmally, this optional feature is not incorporated and
ɜ DUR lead is forced in the ON state (DUR = high).

ɪe Status and Data information is returned to the Proces-
r via DRL000A lines. The Status and Data gates are
own on 02-123D08-3.

ɪe DRG1 pulse gates the true content of the Byte Buffer
ɜgister onto the DRLXX0A lines.

4.9 Coupler Circuits

he coupler circuits (02-123D08-2) adapt the terminals
terface to the Controller. Option D (daughter-board
ɜ-156) converts the RS 232-B interface levels to levels
hich the Controller can accommodate. Option E (daugh-
ɪr-board 35-097) adapts the standard 33/35 TTY to the
ontroller.

4.10 Line Break, Block and Unblock Circuits

line break condition is detected if the DD0 (02-123D08-
) lead is high (Line condition is spacing) for a period
reater than one character time. When the line goes to
ɪe spacing condition (DD0 high),the timer starts and
uns for one character period, the RDY flip-flop does
ot get set by the EOC1 pulse because DD1 is still low.
'his inhibits the setting of the RDY flip-flop. When the
ɪmer stops, TMG0, DD0A, and RDY0 are all high and
ɪe BRK bit is generated. When BRK1 goes high, the
yte Buffer Register is cleared and the BSY bit pulsed
ɔw to generate an interrupt. BRK1 remains high as long
s the Break condition exists on the line.

ɪ the Write Mode, an incoming line break is detected in
similar manner as in the Read Mode. The only differ-
nce is that the RDY flip-flop is reset by DAG1 (02-123
)08-2) instead of ST0. If the Controller is idle in the
Vrite Mode, the Timing flip-flop is set by ST0 and reset
y CTMG0 on detecting the all zeros condition (EOC) in
he Shift Register. During the time TMG1 is high (02-
23D08-3), the BSY bit is set when TMG1 goes low, BSY
oes low and generates an interrupt. If the Controller is
ctive and a line break occurs, the BRK bit is set when
he timer stops after the character has been transmitted.
ɪlso, at this time, BSY goes low and creates an interrupt.

erial feedback to the printer of the Keyboard/Reader in-
ɔrmation is controlled by the Block flip-flop (02-123D08-
). If the Unblock Command is given to the Controller,
the serial output from the receiver (DD0A, 02-123D08-2) is turned around and sent back on the Transmit Line to the terminal. In the Block Mode, the turn-around on the data is inhibited. In the Write Mode, the Block/Unblock function does not affect transmitting to the terminal.

4.11 Optional Features

The following optional features are available:

1. Programmable speed control (see Section 4.7, Timing Circuits).
2. Programmable control of Data Unit Ready lead (see Section 4.8, Command, Status, and Request Circuits).
3. Ten or eleven-bit ASCII code operation (see Section 4.5, Write Mode).
4. ARM/DISARM Interrupt service (see Section 4.4, Interrupt Circuit).
5. Interrupt or Ring lead going from off to on. Remove fifteen ohm resistor 17LR5. The interface must be in the Read Mode for Ring to generate interrupt.
6. Nine-bit operation: one Start, seven Data, and one Stop bit (e.g. 2741 or 1050 terminal). Option B, 02-123D08-2, is normally incorporated for ten or eleven-bit ASCII operation. For nine-bit operation, option C is incorporated, which removes the DR00 flip-flop from the Shift Register.

5. TIMING DIAGRAM

Figures 2 and 3 show the timing for the Read and Write Modes of operation for data transfer.

6. MAINTENANCE

Refer to the vendor operating and service manuals for maintenance information on the terminal being used. The overall operation of the terminal and interface can be checked by running the appropriate test program (06-004M14 or 06-083M14).

Test points useful for troubleshooting are located on the front edge of the board. See 02-123D08-4.

The only adjustment on the interface is the adjustment of the potentiometer on the timing network 35-037 location 45. A check of the timing can be made as follows:

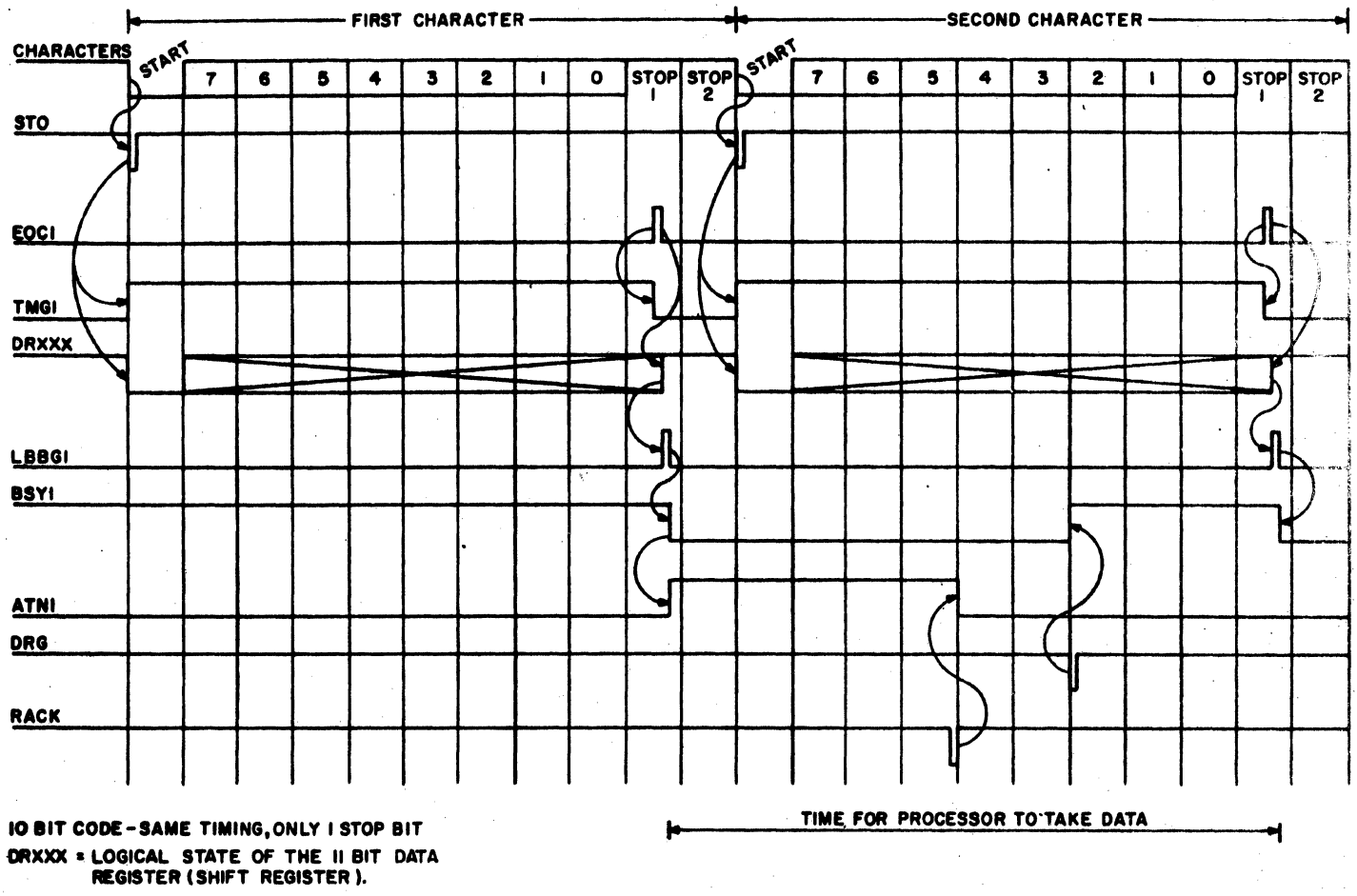


Figure 3. Read Timing for Eleven-Bit ASCII Character

1. Initialize the interface.
2. Ground Test Point Y.
3. Connect an oscilloscope to Test Point E. Vertical scale 2 volts/cm.

   Horizontal scale
   - 10 ms/cm for 10 and 15 characters/second
   - 5 ms/cm for 30 characters/second
   - 2 ms/cm for 120 characters/second

   Sync: Negative
4. Generate a continuous stream of information from the terminal by tape or via the REPEAT Key function of the Keyboard.
5. A negative pulse should occur at the following times:

   a. every 100 milliseconds — 10 characters/second
   b. every 66.6 milliseconds — 15 characters/second
   c. every 33.3 milliseconds See Step 8. — 30 characters/second
   d. every 8.3 milliseconds See Step 8. — 120 characters/second
6. The negative pulse should have the following pulse widths at a temperature of 25°C:

   a. 14 milliseconds ± 0.2 — 10 characters/second
   b. 3 milliseconds ± 0.2 — 15 characters/second
   c. 0.4 milliseconds ± 0.05 See Step 8. — 120 characters/second
   d. 2 milliseconds ± 0.5 See Step 8. — 30 characters/second

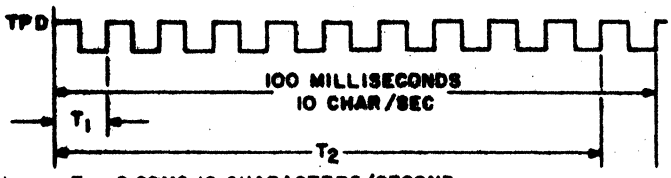
7. The width of the negative pulse can be adjusted by the potentiometer on the daughter-board at location 45. To adjust the pulse width, a continuous stream of information is required from the terminal. If an adjustment is required, adjust potentiometer for the time specified in Step 6.

8. An alternate method of adjusting the timing is to ground Test Point P instead of Test Point Y, and adjust the potentiometer for the waveform shown in Figure 4.

NOTE

The Speed Control (SC) flip flop must be in the proper state when the 30 and 120 characters timing is adjusted.

If the timer cannot be adjusted correctly, check the +15 volts on the interface board. If still not proper, replace the 35-027 daughter-board in location 46, the 35-037 daughter-board in location 45, and/or the 35-020 daughter-board in location 44 (02-123D08-2).



T_1 = 9.09MS 10 CHARACTERS/SECOND
T_1 = 6.66MS 15 CHARACTERS/SECOND
T_1 = 3.33MS 30 CHARACTERS/SECOND
T = .833MS 120 CHARACTERS/SECOND

T_2 = 66.6MS 15 CHARACTERS/SECOND
T_2 = 33.3MS 30 CHARACTERS/SECOND
T_2 = 8.33 MS 120 CHARACTERS/SECOND

TMGO/TP - P(TP) AT GND.

Figure 4. Character Timer Adjustment

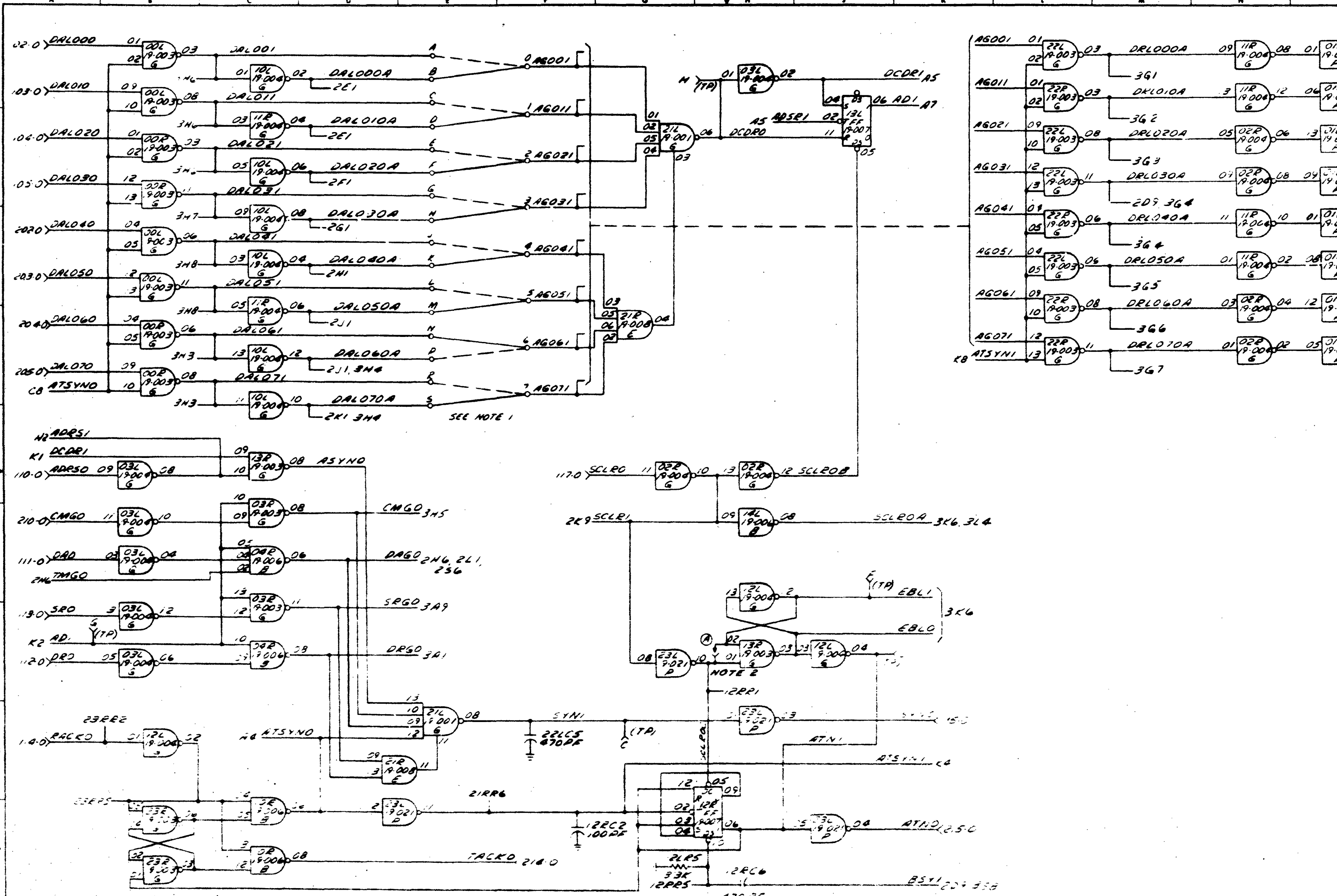
MNEMONIC LIST

he following alphabetical list briefly describes the mnemonics used in the Keyboard Printer I/O Controller. The loca-on on 02-123D08 is also provided.

NEMONIC	MEANING	LOCATION
D	Address flip-flop.	1K1
TN	Attention flip-flop.	1K8
TSYN	Return Address Strobe.	1K8
LK	Block flip-flop.	3L7
RK	Line Break Indication.	2S8
SY	Interface Busy Status.	3S8
L's	Control Line	
ADRS0	Address	1A5
DA0	Data Available	1A6
DR0	Data Request	1A7
SR0	Status Request	1A7
CMD0	Command	1A6
DT0	Clear on Data Transfer.	2M9
DU	Control Data Unit.	3L4
MG0	CMD Signal Gated by AD flip-flop.	1E5
AG0	DA Signal Gated by AD flip-flop.	1E6
AL	Data Available Lines.	1A1-1A4
D	Device Data.	2H7
R00 through R07	Data Register flip-flops.	2E2-2L2

MNEMONIC	MEANING	LOCATION
DRL	Data Request Lines.	1S1-1S4
DRN	Data Register Contains Start Bit on Output.	2M3
DRS	Data Register Contains Start Bit on Input.	2K3
DRX	Data Register Contains Stop Bit.	2C2
DT	Direction Transfer flip-flop.	2S9
DUR	Data Unit Ready Lead.	2A8
EBL	Enable Attention flip-flop	1K7
EOC	End Of Character	2J7
ERR	Error	3E8
EX	Examine Status Condition.	3F7
LBBG	Load Byte Buffer.	3C2
RACK0	Received ACK Signal.	1A8
RDY	Ready flip-flop.	2K8
SB/RG	Standby or Ring.	2A9
SC	Speed Control.	4M3
SCLR	System Clear.	1G5
SRD	Set Data Register.	2S5
SRG0	SR Signal Gated by flip-flop.	1E6
ST0	Start Gate (Read Mode).	2J8
SYN	System Sync.	1K8
TACK	Transmitted ACK Signal.	1E9
TMA	Timer frequency F.	2N5
TMB	Timer frequency F.	2L6
TMC	Timer Counter F/2.	2N4
TMD	Timer Counter F/4.	2R4
TME	Timer Counter F/8.	3K2
TMF	Timer Counter F/16.	2L2
TMG	Timer flip-flop.	2S7
TRD	Toggle Register Data.	3S1
TRNS	Transmit Data to Terminal.	2S7

INTERDATA



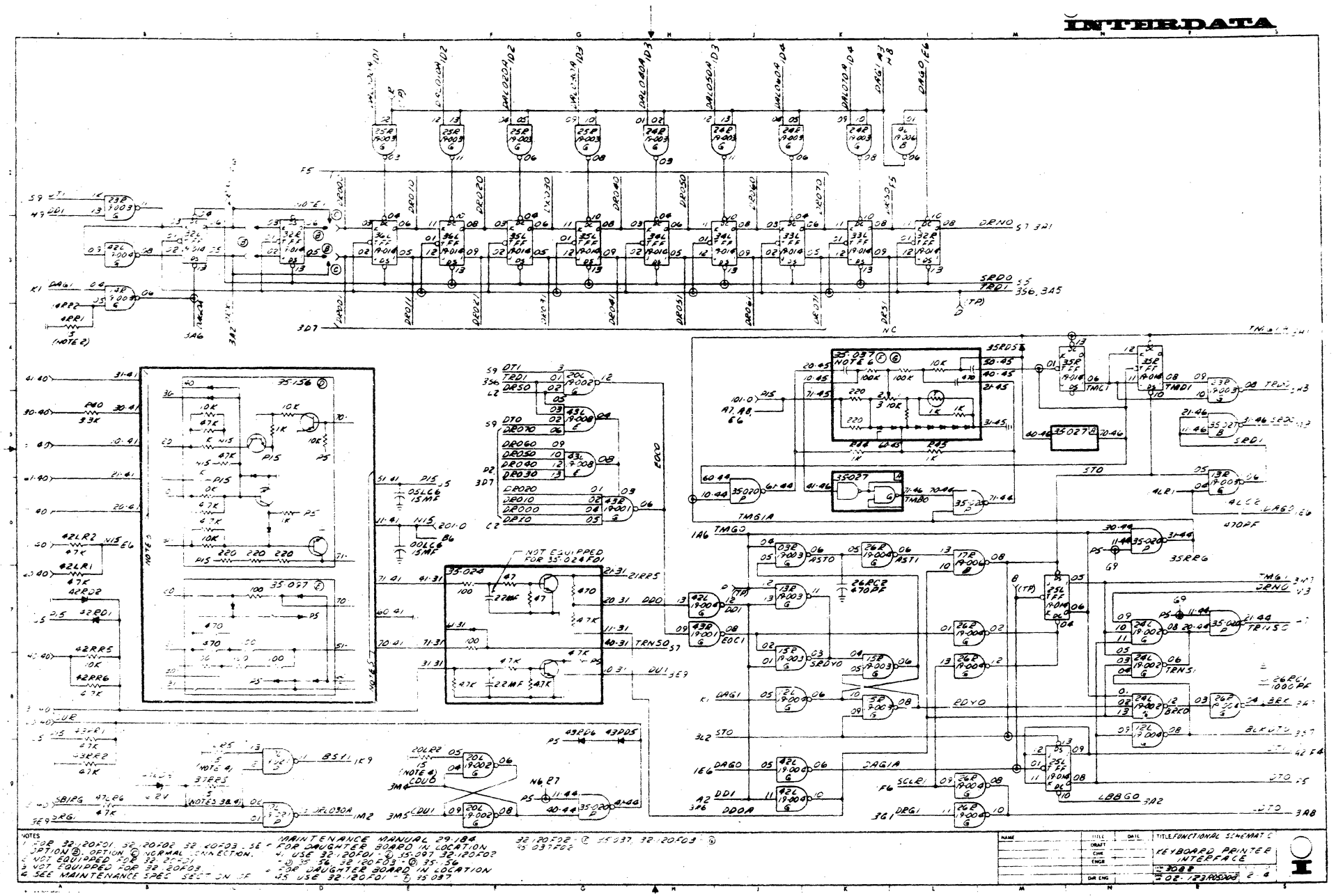
FOR REV INFO PRIOR TO R02 SEE 02-123 A07

SH. 2 ADDED NOTE ON LOC. F7 SH. 3 ADDED COMP FOR TERMINET 300 LOC R4					
RM	RS	956		6-22-71	R02
SH 3 LOC D8 IC IN LOC 0AL WAS 19-021 19-041; SH 4 UPDATED COMMAND STATUS TABLE LOC 9A.					
RM	RS	943			R03
IN SH2 LOC 3B ADDED CONN 3A5 TO 14R & 32L IN SH3 LOC 3A, 5B ADDED 32L. LOC M6 ADDED CKT TO READ 1 LINE					
RM	RS	1271		1-19/72	R04
IN SHT 3 LOC M6 REMOVED 25LC5 & 26LR2. LOC E5L-6 INCORPORATED CKT PREVIOUSLY FOR TERMINET 300(32-120 F03) ONLY					
RM	RS	1375			R05

NOTES
1. STRAP FOR Ø2 ADDRESS NORMALLY
2. NORMALLY NOT EQUIPPED, USED ONLY FOR ARM-D SARM INTERRUPT FUNCTION SEE MAINTENANCE SPEC SECTION OF MAINTENANCE MANUAL 29-184

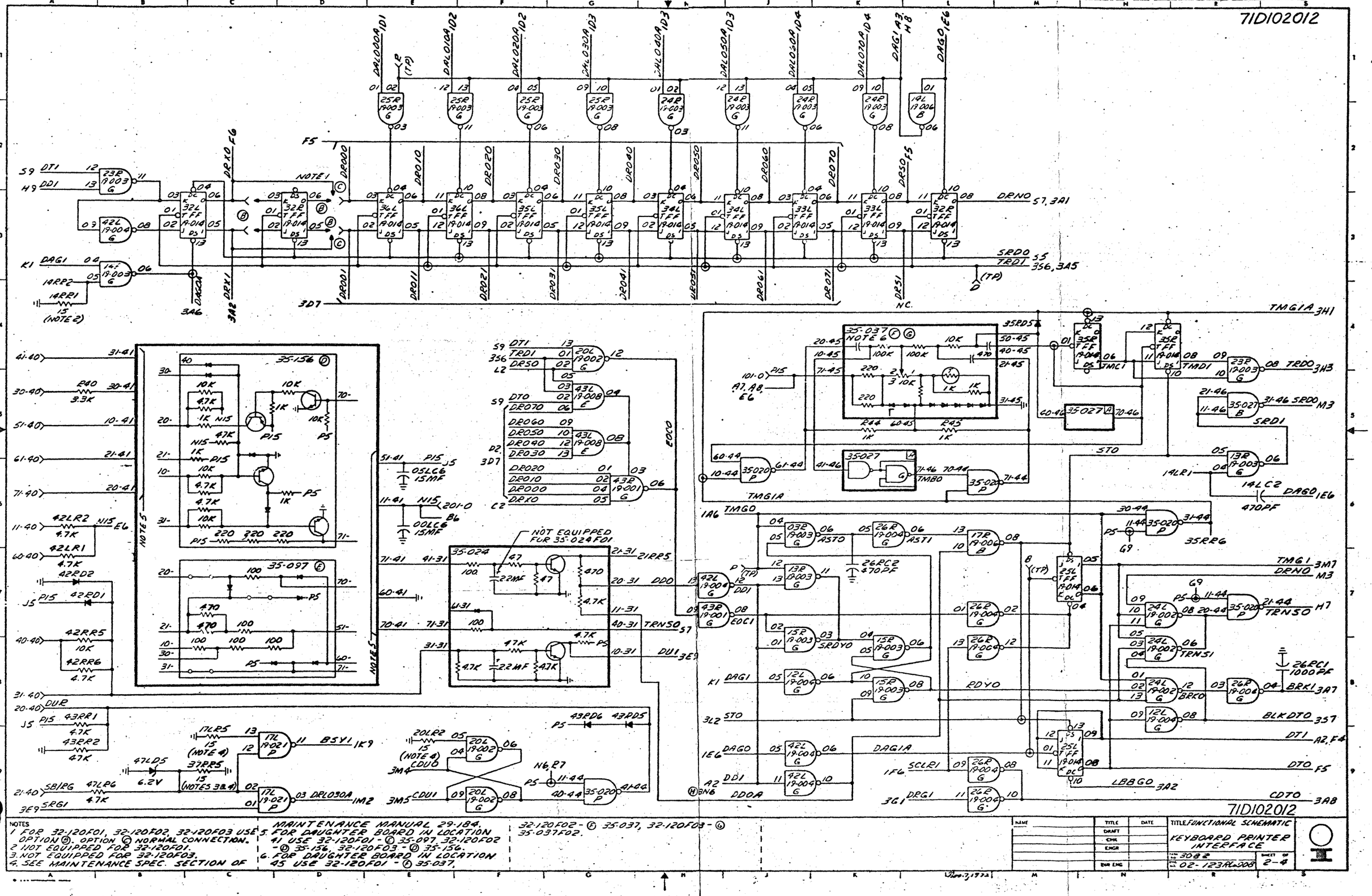
L.A. YOUNG
P.E. JONES

FUNCTIONAL SCHEMATIC
KEYBOARD PRINTER INTERFACE


INTERDATA
NOTES
1. FOR 32:20F01 - SEE MAINTENANCE MANUAL 29:184
2. OPTION (A) OPTION (B) OPTION (C) NORMAL CONNECTION.
3. NOT EQUIPPED FOR 32:20F03.
4. USE 32:20F01 - (C) 35:037, 32:20F02
5. USE 32:20F01 - (C) 35:037
6. SEE MAINTENANCE SPEC SECTION 35
32:20F02 - (C) 35:037, 32:20F03 - (B) 35:036
35:037F02
- (B) 35:036, 32:20F03 - (A) 35:036
- FOR DAUGHTER BOARD IN LOCATION
- FOR DAUGHTER BOARD IN LOCATION
NOT EQUIPPED FOR 35:024 FD1
TITLE/FUNCTIONAL SCHEMATIC
KEYBOARD PRINTER INTERFACE
DWG 3088
SIZE B
SHEET 2 OF 4

INTERDATA

71D102012



NOTES

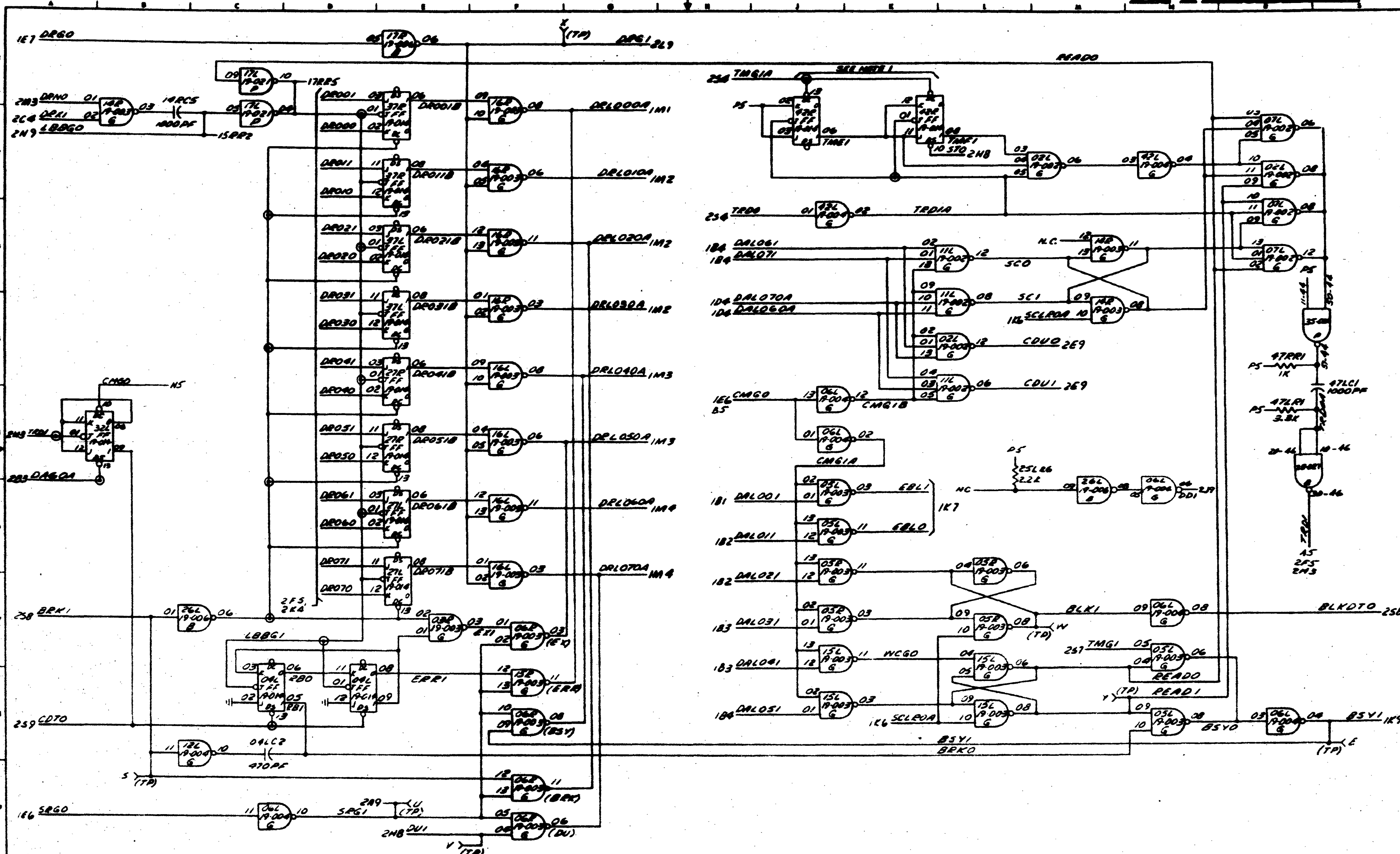
1. FOR 32-120FOI, 32-120FO2, 32-120FO3 USE OPTION D. OPTION G NORMAL CONNECTION.
2. NOT EQUIPPED FOR 32-120FOI.
3. NOT EQUIPPED FOR 32-120FO3.
4. SEE MAINTENANCE SPEC. SECTION OF MAINTENANCE MANUAL 29-184.
5. FOR DAUGHTER BOARD IN LOCATION 41 USE 32-120FOI - E 35-097, 32-120FO2 - D 35-156, 32-120FO3 - D 35-156.
6. FOR DAUGHTER BOARD IN LOCATION 45 USE 32-120FOI - F 35-037, 32-120FO2 - F 35-037, 32-120FO3 - G 35-037FO2.

NAME	TITLE	DATE	TITLE/FUNCTIONAL SCHEMATIC
	DRAFT		KEYBOARD PRINTER INTERFACE
	CHK		SIZE 3082 SHEET OF 2-4
	ENGR		DWG NO 02-123FA-3082
	DIR ENG		

Rev. 7, 1972

71D102012

INTERDATA



NOTES
1. IC IN LOC 42R NOT EQUIPPED FOR 32-120F01 AND 32-120F02.

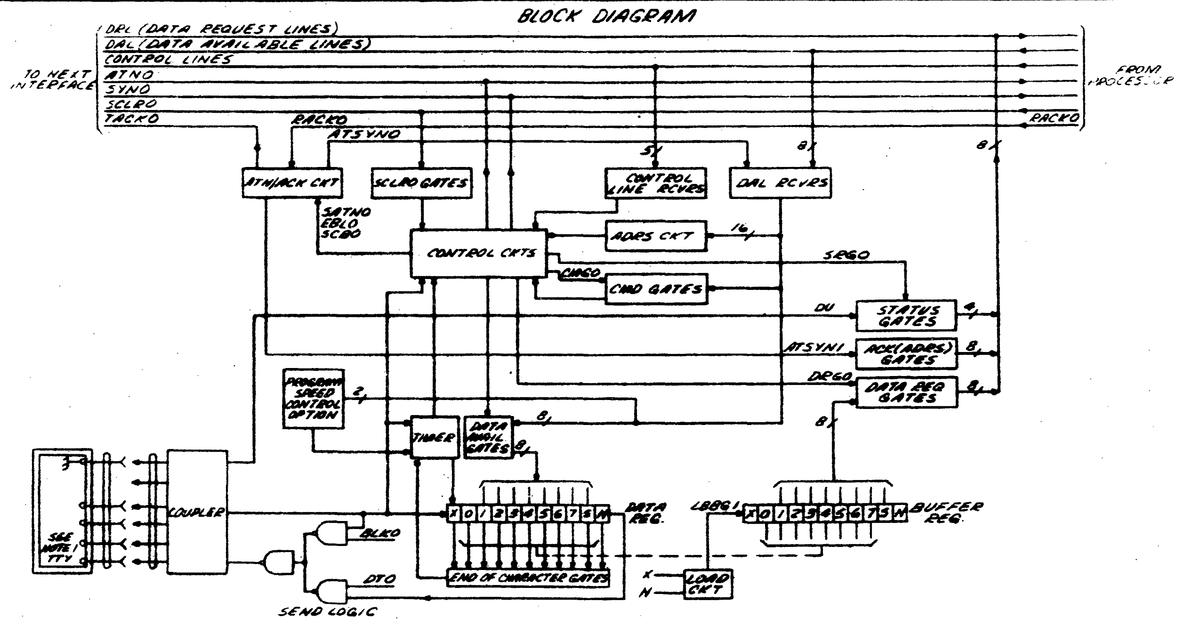
TITLE FUNCTIONAL SCHEMATIC
KEYBOARD PRINTER INTERFACE

02-123 R05 D08

3-4

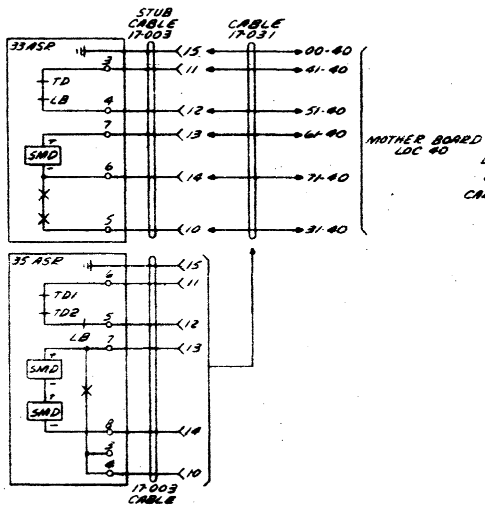
INTERDATA

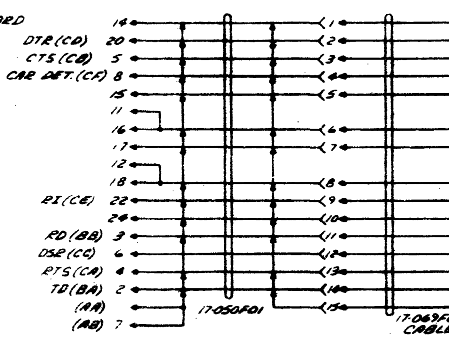
BLOCK DIAGRAM


DRL (DATA REQUEST LINES)
DAL (DATA AVAILABLE LINES)
CONTROL LINES
TO NEXT INTERFACE
ATNO
SYNO
SCLRO
TACKO
RACKO
ATSYNO
FROM PROCESSOR
ATN/ACK CKT
SCLRO GATES
CONTROL LINE RCVRS
DAL RCVRS
SATNO
EBLO
SCBO
CONTROL CKTS
ADRS CKT
CMGO
CMD GATES
SRGO
DU
STATUS GATES
ATSYN1
ACK(ADRS) GATES
DRGO
DATA REQ GATES
PROGRAM SPEED CONTROL OPTION
TIMER
DATA AVAIL GATES
COUPLER
SEE NOTE 1 TTY
BLKO
DTO
SEND LOGIC
X 0 1 2 3 4 5 6 7 S M
DATA REG.
END OF CHARACTER GATES
LBBG1
BUFFER REG.
LOAD CKT

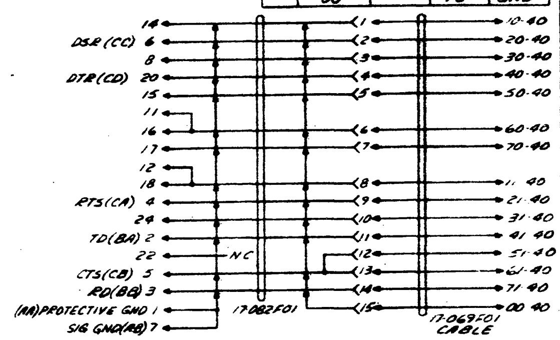
TP	DESIGNATION	LOC.
Y	READ1	3M8
X	DRG1	3G1
W	BLK1	3M7
V	DU1	3E9
U	SRG1	3E9
T		
S	BRK1	3B9
R	DAG1	2E1
P	TMGO	2J7
N		
M		
K		
J	ATN1	1K7
H	DCDRO	1G1
G	AD1	1A7
F	EBL1	J6
E	BSY1	3S8
D	TRD1	2L8
C	SYN1	1G8
B	DAG1A	2M7
A	GND	

CMD	BIT	STATUS
DISABLE	0	ERR
ENABLE	1	
UNBLOCK	2	BRK
BLOCK	3	STB/RING*
WRITE	4	BSY
READ	5	EX
CB1	6	
CB2	7	DU





103A DATA SET CONNECTION



TERMINET 300 & MOD 37 TTY

CONN POS	21		
MOTH BD	KPIO		
VERT POS	HORIZ POS		
	0	1	2
1 22			
1 21			
1 20			
1 19			
1 18			
1 17			
1 16			
1 15			
1 14			
1 13			
1 12			
1 11			
1 10			
1 09			
1 08			
1 07			
1 06			
1 05			
1 04			
1 03			
1 02			
1 01			
1 00			
0 22		PS	GND
0 21			
0 20			
0 19			
0 18			
0 17		SCLRO	
0 16			
0 15		SYNO	ATNO
0 14		RACKO	TACKO
0 13		SRO	
0 12		DRO	
0 11		DAO	
0 10		ADRSO	CMGO
0 09		DRL030	DRL070
0 08		DRL020	DRL060
0 07		DRL010	DRL050
0 06		DRL000	DRL040
0 05		DAL030	DAL070
0 04		DAL020	DAL060
0 03		DAL010	DAL050
0 02		DAL000	DAL040
0 01		P15	N15
0 00		PS	GND

NOTES

1. 33ASR/KSR, 35ASR/KSR, MOD 37 TTY GE TERM 300, 103 D S
2. * - SEE MAINTENANCE SPEC OF MAINTENANCE MANUAL 29-184.

TITLE FUNCTIONAL SCHEMATIC KEYBOARD PRINTER INTERFACE

30-88 | 02-23 F05 D08 | SHEET 4-4