6-13

GENERAL ELECTRIC

70A111187

PRINT DIST.		CONT. ON 1	SH. NO. 0
K7-19	CARD READER INTERFACE PRODUCT SPECIFICATION		

GENERAL NOTES

F.C.F.
FMF: GE-PAC 30

APPROVED BY: Harry Romisch DATE: March 29, 1971

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	Issue P				
B	ANI-076 REV SHTS 0,1	2-9-71 JDL			

ISSUED
A ISSUED
Jo Jo 15, 1971

ode By
C Alessandro APR 2, 1971

To A

PCE 20A 7-68

3000AE41-T

1. Documentation

The following documents are supplied with each controller interface:

1 each	70B113888	(FS-55)	Schematic
1 each	70A111136		Installation Specification
1 each	70A111086		Maintenance "
1 each	70A111671		Test "
1 each	70A112458		Test Tape

2. Parts List 70A104048G51

1 each	70A110365 G1 (32-084)	Mother Board
1 each	70A110177 G1 (17-053F02)	Cable

3. Dimensions

3.1 Cable - 15 feet

3.2 Mother Board - 9½inches x 10½inches

4. Weight

4.1 Mother Board and Cable - 1 pound

5. Power Requirements

5.1 5 volts ±10%, 0.75 amps

6. Environmental

6.1	Temperature	0° to 50° C
6.2	Vibration	Equals or
6.3	Humidity	Exceeds Processor

K7-19

PRINTS TO

7. Description

7.1 The interface board described in this specification is intended for use with the Soroban Model 6002 card reader. It consists of one mother-board and a connecting cable. The standard address is X'04'. Cards are selected on demand and can be processed by the Card Reader at a maximum rate of 225 cards per minute. The interface can be added to any of the GE-PAC 30 computes to obtain card reading services.

7.2 The interface stores the twelve data columns, as the card reader sends them out, for transfer to memory upon computer requests. A status byte gives an indication of the status of the Card Reader and interface at any time during operation.

K 7-19

PRINTS TO

The Controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the System Interface Manual, Publication Number PCP126, sections on Mechanical Layout and Wiring, Interrupt Control and Multiplexor, and Selector Channel Wiring Data.

Figure 1 shows proper cable connection between mother-board and Card Reader.

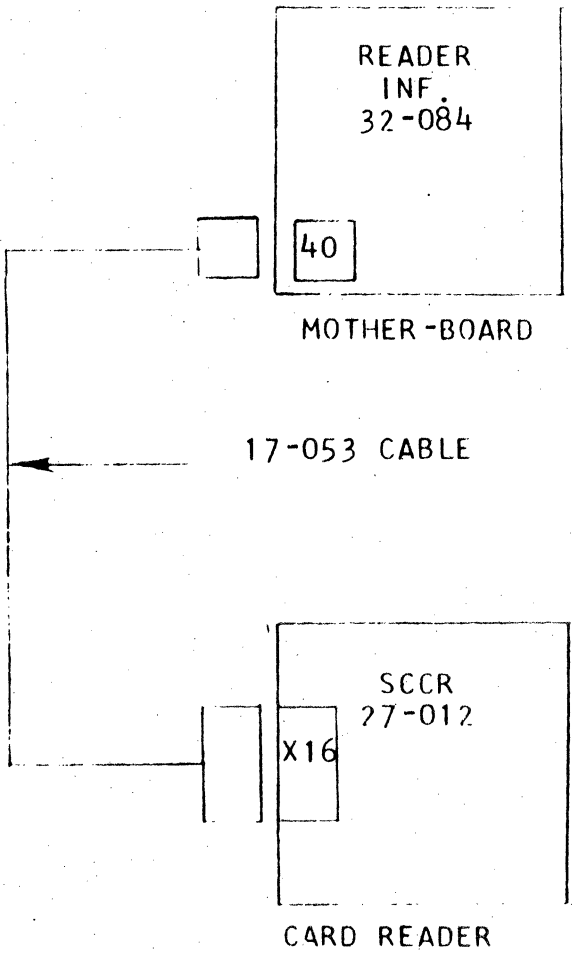


FIGURE 1

K7 20

PRINTS TO

GENERAL ELECTRIC

70A111086

PRINT DIST. K7-21 CGE

CARD READER INTERFACE
MAINTENANCE SPECIFICATION

CONT. ON 1 SH. NO. 0
(02-042A21)

GENERAL NOTES

F.C.F.
FMF: GE-PAC 30

APPROVED BY: E. G. White DATE: Oct 31, 69

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	Issue				
A1	AN1-076 REV SHTS 0,4,10	JDL 7-8-71			
M	Release to dwg file	Sept 1, 1972			

REISSUED

A	Issue
A1	JULY 15, 1971

Made By: E. White

Issue Date: Nov. 5, 1969

PROCESS COMPUTER
PHOENIX, ARIZ.

Dwg. No. 70A111086
Cont. on 1 Sh. No. 0

TABLE OF CONTENTS

ILLUSTRATIONS

1. GENERAL DESCRIPTION

1.1 Introduction. The 27-012 Card Reader is an extremely compact unit for photoelectric reading of data punched in standard unit record cards. It employs a fiber optic read station and a vacuum throat feed assembly. A special "wide strobe" read technique is used to preclude loss of data, even on cards which have been mispunched by as much as plus or minus one-half column.

A card Feed command causes the card to move over the photo-read-cells column by column, starting with column one. Every column read (blank columns are read as all bits zero) generates a data strobe for that column and initiates a data transfer cycle. The first Read Data instruction from the Processor reads the top six rows of the column; the second Read Data instruction reads the bottom six rows of that column. Figure 1 is an example of the data byte format. Light current checks and card motion checks are continuously performed to verify the operation of the Card Reader.

1.2 Scope of Manual. The basic purposes of this specification are to provide general information on the Card Reader and a functional description of the interface operations during a Read instruction. The functional description is divided into the following areas: Status, Commands, Addressing, and Read operation. Included also is a section on general maintenance, and a mnemonic listing of all signals and their definitions.

2. OPERATOR CONTROLS

2.1 Power. The lighted POWER pushbutton applies AC power to all circuits. The pushbutton is lit when the power is on.

2.2 Motor Start. The lighted MOTOR pushbutton starts the drive motor if no error indicator lights are lit. The pushbutton is lit when the drive motor is running.

2.3 Read Start. The lighted START pushbutton clears all error indicators and advances the Card Reader to the "Ready" state to begin a read cycle upon receipt of the proper signal. The pushbutton is lit when the switch is depressed and no errors have been detected.

2.4 Read Stop. The lighted STOP pushbutton inhibits further read cycles until Read START is again depressed. Read STOP action is delayed until the current read cycle is completed. The pushbutton is lit when the switch is depressed, or if the Card Reader is stopped due to an error detection.

3. STATUS INDICATOR LIGHTS

3.1 Power On. The indicator on the POWER Switch is illuminated when power is applied to the Card Reader.

ROW NUMBER			12	11	0	1	2	3	First Data Byte
BIT NUMBER	0	1	2	3	4	5	6	7	
ROW NUMBER			4	5	6	7	8	9	Second Data Byte

NOTE: Bit numbers 0 and 1 should always be zero.

Figure 1. Data Byte Format

3.2 Motor On. The MOTOR Switch indicator is illuminated when the motor is running.

3.3 Read Start. The START Switch is illuminated when the switch is depressed and no malfunctions have been detected.

3.4 Read Stop. The STOP Switch is illuminated when the switch is depressed or the Card Reader has stopped due to a trouble detection, as described in the following paragraphs.

3.5 Pick Fail. If a card fails to be picked upon command, the PICK FAIL indicator is illuminated.

3.6 Card Motion Error. If the interval between the time selected card enters the Read Station and the time the card leaves, does not correspond to 85 ±1/3 columns (the total card width), the CARD MOTION indicator illuminates.

3.7 Light Current Error. When all photo-read-cells do not conduct whenever a card is not in the Read Station, the LIGHT CURRENT indicator illuminates.

3.8 Dark Current Error. The DARK CURRENT indicator illuminates if all photo-read-cells do not go dark for some instant between the beginning of the card and column 1, or between column 80 and the end of the card.

4. FUNCTIONAL DESCRIPTION

4.1 Commands. Any meaningful command or combination of commands can be issued by the Processor to the Card Reader Interface. The specific command is sent on the DAL lines followed by the Command (CMDO) signal on the Control Line. Table 1 illustrates the Command Byte Codes and provides an explanation of their functions. The CMDO signal is inverted and ANDed with AD1 to produce CMGO (Gated Command). This signal is again inverted to gate the bits from the DAL's to the Command flip-flop 70B113888 (FS55) SH.3

If this controller is to be allowed interrupt service, DAL bit one is set. DAL011 is ANDed with CMG1 to set the Interrupt Enable (EBL) flip-flop. Interrupts are generated by this interface when a character is strobed into the Buffer Register. The interrupt condition is saved in the Attention (ATN) flip-flop. EBL, set, gates a saved ATN Interrupt Condition onto the Processor I/O Bus as ATNO.

TABLE 1
CARD READER STATUS AND COMMAND BYTE DATA
(HEX ADDRESS 04)

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE	EOV	TBL	HE	NMTN	BSY	EX	EOM	DU
COMMAND BYTE	DISABLE	ENABLE	FEED					

EOV — The EOV bit is set when the data is not taken from the Device Controller buffer before the next column of data arrives from the read station. This bit is reset by a FEED Command.

TBL/DU — These bits are set when the Card Reader fails to pick a card upon command, or when an error condition occurs in the Card Reader. The error conditions are:

1. Card Motion Error
2. Light Current Error
3. Dark Current Error

These error conditions prevent the reading of any more cards until manually reset by the operator.

HE — The HE bit is set when the last card in the input hopper has been read. When HE sets, NMTN is set. The HE bit must be manually reset by the operator.

NMTN — The NMTN is set except for the time between a FEED command and the time it takes for a card to pass through the read station.

4. FUNCTIONAL DESCRIPTION (CONT.)

4.1 Commands (Cont.)

BSY The BSY bit is set while the Device Controller is awaiting data from the Card Reader. It resets when the data is available to be transferred.

EX The EX bit sets when any one of bits 0,1,2, or 3 of the Status byte is set.

EOM The EOM bit is set whenever NMTN is set, and when the input hopper becomes empty.

DISABLE This command disables the Card Reader Device Interrupt.

ENABLE This Command enables the Card Reader Device Interrupt.

FEED This command initiates a new card feed cycle; however, no action occurs if TBL, DU, or HE is set.

If the controller is to be denied interrupt service, DAL bit zero is set. DAL001 is ANDed with CMG1 to reset EBL. Interrupt conditions may still be saved in the ATN flip-flop, but ATNO cannot be generated.

The Feed Bit being set, enables a new card feed cycle to occur in the Card Reader if TBL, DU, or HE is not set and the Card Reader is not in the middle of a Read operation. A requirement of one Feed Command per card is necessary, since the reader terminates a Read cycle after reading the eightieth column.

4.2 Status. To enable the Processor to check on operational conditions of a particular Input/Output device, a system of information feedback known as Device Status has been provided. The information gated from the particular device to the Processor is used for programming control. Table 1 illustrates the status byte code and provides an explanation of their function for the Card Reader.

The signals for Trouble (TBL), Device Unavailable (DU), and Hopper Empty (HE) are initiated directly from the Card Reader, while the remaining six status bits are from the interface. The Processor initiates a Status Request by activating the Status Request (SRO) Line (FS5503). SRO is inverted and ANDed with the output from the Address flip-flop, AD1, producing the output SRGO. Approximately 200 nanoseconds after SRGO becomes active, a SYN signal is sent to the Processor indicating that the device addressed has received the Status Request. SRGO is inverted and acts as a gating control to place the status information on the zero active DRL Lines (FS55-4) which return it to the Processor.

4. FUNCTIONAL DESCRIPTION (CONT.)

4.3 Addressing. Prior to receiving any commands, the Card Reader interface must receive its address and respond properly. This is done through micro-sequences which first send the address X'04' on the Data Available Lines (DAL's)(FS55-1), and then the ADRSO signal on the Control Line (FS55-3). The DAL lines go through single-to-double rail converters and address strapping terminals which drive a decoding network. The output from this decoding network is ANDed with the inverted signal from the ADRSO Line to set the Address flip-flop (AD).

After a delay of approximately 200 nanoseconds, the SYN1 signal goes high. SYN1 is inverted and tested by the Processor to determine if the Interface has responded to its address. The AD flip-flop being set, enables other modes of operation (e.g., Reading, Status Request, etc.) by the Interface.

4.4 Read Operation. Previous to a Read operation being performed by the Card Reader, a System Clear (SCLRO) signal is sent by the Processor to initialize the interface. With SCLRO active, the Attention and Feed flip-flops are placed in a reset state.

When a Feed command is issued by the Processor to the Card Reader Interface, the Command (CMDO) line becomes active (FS55-3). The CMDO signal is inverted and ANDed with the set output from the Address (AD1) flip-flop producing the signal CMGO. Approximately 200 nanoseconds after CMGO becomes active, a SYN signal is returned to the Processor indicating that the Command was received by the Interface. The CMGO signal is inverted and ANDed with DAL021 (FS55-5) causing the Feed (FD) flip-flop to be set. The output from the ANDing of CMG1 and DAL021 produces an Initialize signal (INITO). INITO causes the Overflow (EOV) flip-flop and the Check (CK) flip-flop to become reset (FS55-6). The set output from the Feed (FD1) flip-flop is ANDed with the reader derived Ready signal (IRDYO) which indicates that there is no card in the Read Station, no errors have been detected, and the Reader is in the Start Read Condition. The output from this AND condition is the Read Command signal (IRCO).

IRCO going active causes the Reader to pick one card from the hopper, move it to the Read Station, and start the internal control for reading the card one column at a time. Approximately 150 microseconds after IRCO becomes active, IRDYO becomes inactive due to a card in the Read Station.

4. FUNCTIONAL DESCRIPTION (CONT.)

4.4 Read Operation (Cont.)

The DATA flip-flop inhibits the resetting of the FEED flip-flop by the IRDYO signal until at lease one column of information has been read by the Reader and sent to the interface.

As the card passes through the Read Station, all twelve rows of a column are read at one time. As each column is read, a Data Strobe (IDSO) signal (FS55-5) initiated from the Reader is sent to the interface. The incoming signal is inverted, and passed through a wave shaping network generating the Column Strobe signals KCR1A, KCR1B, and KRCO. The KCR1A and KCR1B signals gate the information from the Column Load (CL) Lines of the Reader into the Interface Buffer Register (FS55-7). The KCR1B signal goes to the trigger of the Check (CK flip-flop causing it to complement. CKO, now active, will cause Busy (BSY) to become inactive indicating that there is now data in the Interface Buffer Register (FS55-4). CKO passing through a differentiating network, will also cause the BSATN1 signal to become active. BSATN1 causes the Attention (ATN) flip-flop to become set (FS55-3) and request an interrupt by the Processor. BSASTN1 is also set when the FD flip-flop becomes reset. The CK1 output goes to the J input of the EOV flip-flop. If another column is read by the Card Reader before the data in the Buffer Register is sent to the Processor, gating signal KCR1B causes the EOV flip-flop to set, indicating the error.

With an Interrupt Request issued by the Card Reader Interface, two Data Requests (DRO) would be issued by the Processor. The first DRO would be received by the Card Reader Interface inverted and ANDed with the output of the Address flip-flop deriving the signal DRGO (FS55-3). Approximately 200 nanoseconds after the signal was received, a SYN pulse would be sent to the Processor indicating that the Interface has received the command. The signal DRGO passes through an inverter and is ANDed with CLSTO generating the signal DG11 (FS55-6). DG11 then gates the first half-column from the Buffer Register to the Processor (FS55-4). DRGO is inverted and fed to the trigger of the CLST flip-flop. When DRGO becomes inactive, the trailing edge of the signal causes the flip-flop to complement and become set. The second DRGO pulse will now gate out the second half-column of the data from the Buffer Register with the Signal DG21.

4. FUNCTIONAL DESCRIPTION (CONT.)

4.4 Read Operation (Cont.)

If a third DRGO was sent by the Processor before a new column had been read by the Reader, the output of CLSTO and DRGO, ANDed, would set the CK flip-flop via its DS input. When the next column was read, the signal KCR1B active, would cause this EOV flip-flop to be set to indicate the error.

The Read process continues until the completion of the 80th column, at which time the card passes from the Read Station causing the IRYDO signal to become active and tiggling the FD flip-flop to a reset state. The FD flip-flop in a reset state, generates EOM and terminates the instruction.

If, at any time during a Read operation, the feed hopper of the Reader becomes empty, the signal IHE1 (Hopper Empty) becomes active (FS55-5). The signal is inverted and fed into the HELCK (Hopper Empty Lock) flip-flop causing the zero output to become active. After passing through a differentiating network, the signal is ORed with SCLROA, then inverted and fed into the DC input of the FD flip-flop causing it to become reset. This will cause the Read operation to terminate at the completion of the card in the Read Station. The Processor will perform a status check loop until the card hopper has been refilled and the Reader put back on-line manually. The HELCK flip-flop also prevents any multiple resetting of the FEED flip-flop until the cards are loaded into the hopper and the Reader is brought up to the ready condition.

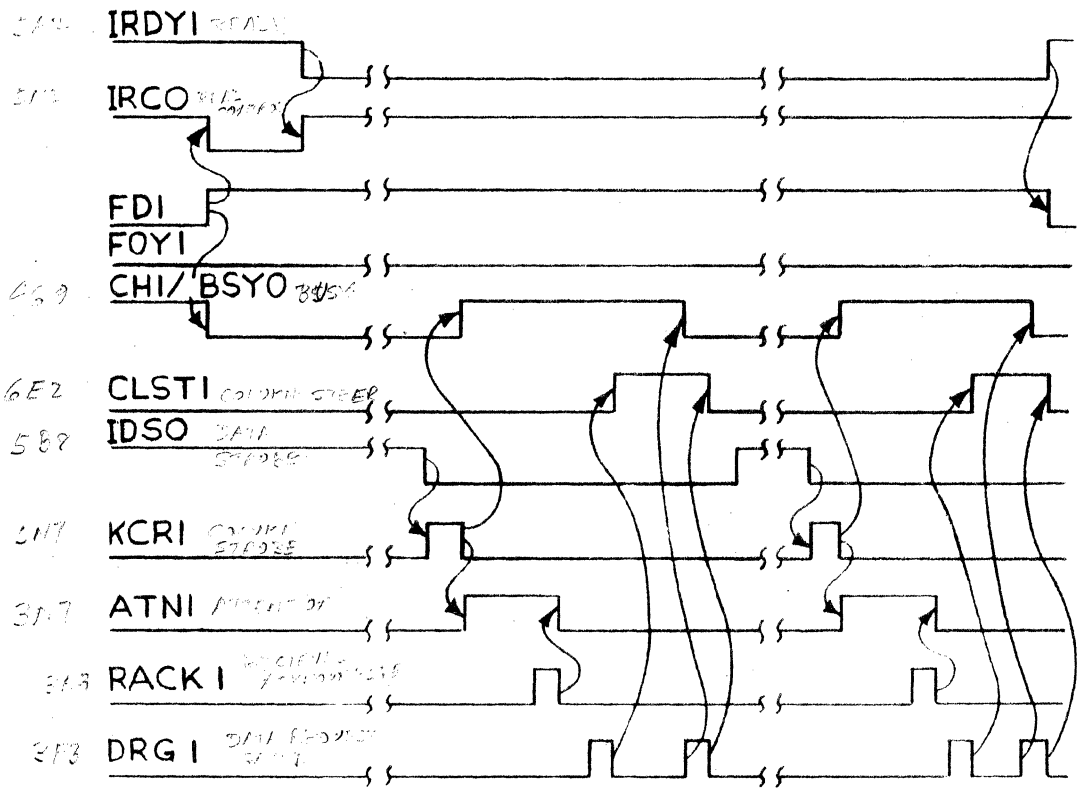


FIGURE 2. CARD READER INTERFACE TIMING

5. MAINTENANCE

The Card Reader Interface is asynchronous in operation with the Processor and Reader. A timing chart, Figure 2, showing relative relationships of all major signals is provided for Interface Maintenance Checks.

Refer to the appropriate vendor maintenance manuals for maintenance information on the Card Reader itself. The overall operation of both the Card Reader and the Interface may be checked by running the Card Reader Test Program as described in Publication Number 70A112458 For operation and programming information, see the Card Reader Operation and Programming Information contained in the GE-PAC 30/3010 General Description Manual. Functional Schematics for the Card Reader are designated (FS-55) 70B113888.

6. MNEMONICS

The following alphabetical list briefly describes the mnemonics used in the Card Reader Device Controller. The source on FS55 for each signal is also provided.

MNEMONICS	MEANING	FS55 LOCATION
AD	Address flip-flop	1P2
ADRS	Address	2D1
AGOX	Address Gated	1H2
ARACK	Attention Received Acknowledge	3C9
ATN	Attention flip-flop	3N7
ATSYN	Attention Syne	3M9
BSATN	B Input to Set Attention	6P9
BSY	Busy	4G9
CK	Check flip-flop	6J5
CLX	Column Load	7A1
CLST	Column Steer flip-flop	6E2
CMD	Command	3B2
CRXX1	Column Read	7B9

6. MNEMONICS (CONT.)

MNEMONICS	MEANING	FS55 LOCATION
CMG	Command Gated	3H2
DALOX	Data Available Lines	1A4
DATA	Data flip-flop	5P4
DGX1	Data Gating Control	6H2
DR	Data Request	3B3
DRG	Data Request Gated	3F3
DRLOX	Data Request Lines	2K
DU	Device Unavailable	4M8
EBL	Enable	3P2
EOM	End of Medium	4N3
EOV	Overflow flip-flop	6N4
FEED	Feed flip-flop	5K2
HELCK	Hopper Empty Lock	4R4
IDS	Data Strobe	5B8
IHE	Hopper Empty	4P4
INIT	Initialize	5R4
IPF	Pick Fail	4P7
IRC	Read Control	5N2
IRDY	Ready	5A2
ITRR	Read Trouble	4P7
KCR	Column Strobe	5N7

6. MNEMONICS (CONT.)

MNEMONICS	MEANING	FS55 LOCATION
RACK	Received Acknowledge	3A8
SCLR	System Clear	1R8
SR	Status Request	3A4
SRG	Status Request Gated	3H4
SYN	Sync	3B5
TACK	Transmit Acknowledge	3A9

MS 5-7

GENERAL ELECTRIC
PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE
FUNCTIONAL SCHEMATIC
CARD READER INTERFACE

DRAWING NUMBER 70B113888 | CONT 0A | PAGE 0
FIRST MADE FOR GE-PAC 30
(FS55)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	ISSUED				

REISSUED
C. Dodio.

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS55)

DRAWN BY L. Moraes Nov 19/69
ISSUED Dec. 22, 1969
APPROVAL E.G. Wilson Dec 19, 69

DRAWING NO. 70B113888 | CONT 0A | PAGE 0
PRINTED TO: X708

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING: APPLIED PRACTICES | SURFACES ✓ | TOLERANCES ON MACHINE DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

TITLE: FUNCTIONAL SCHEMATIC CARD READER INTERFACE
FOR GE-PAC 30

DWG NO (FS55) 70B113888
CONT ON SHEET 1 SH NO 0A

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	1	2																		
DPL RCVRS & ADDRESS CKT	1	1	2																		
DPL LINE DRIVERS	2	1	2																		
CONTROL LINE RCVRS, SYNC & INTERRUPT LOGIC	3	1	2																		
STATUS AND DATA GATING	4	1	2																		
CONTROL LOGIC	5	1	2																		
DATA STEERING AND OVERFLOW LOGIC	6	1	2																		
BUFFER REGISTER	7	1	2																		
BACK PANEL MAP	8	1	2																		
BLOCK DIAGRAM	9	1	2																		
	10	1	2																		
	ISSUE DATE	8-15-68	5-16-69																		

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD ASSEMBLY	32-004 R01

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.
3. IN THE EVENT THAT THE REVISION LEVEL STAMPED ON THE PWB DOES NOT CORRESPOND TO THAT IN THE SUPPORTING INFORMATION TABLE, PLEASE REQUEST SCHEMATIC OF THE CORRECT REVISION LEVEL FROM "GENERAL ELECTRIC COMPANY 40 FEDERAL ST WEST LYNN, MASSACHUSETTS 01905".

MADE BY: J. Moraes Nov 18, '67
ISSUED: DEC 22 1969
APPROVAL: E. C. White Dec 19, 69

REV C ISSUE

DWG NO (FS55) 70B113888
CONT ON SHEET 1 SH NO 0A

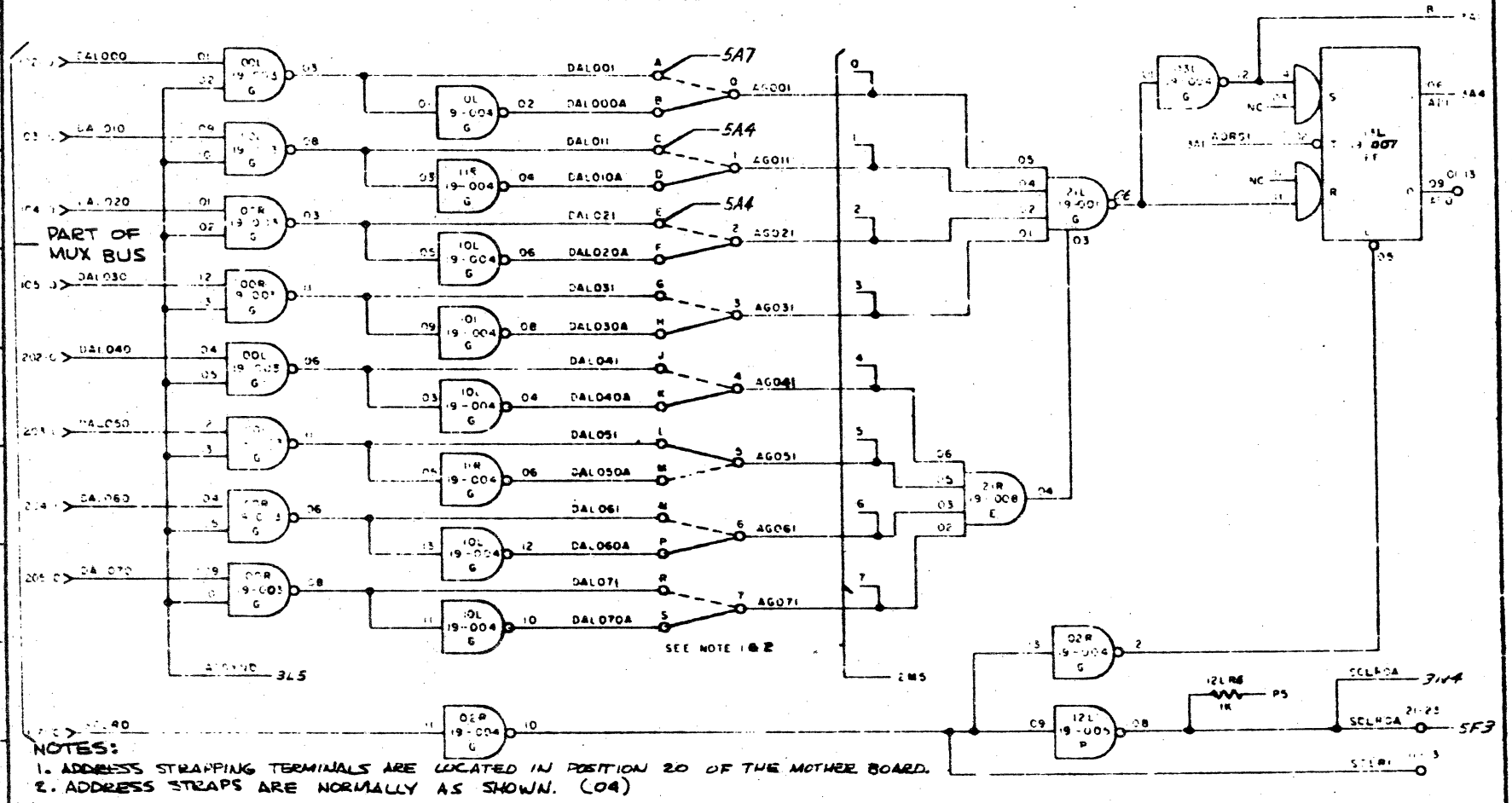
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING — APPLIED PRACTICES | SURFACES √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER PHOENIX

TITLE: FUNCTIONAL SCHEMATIC
CARD READER INTERFACE
FOR GE-PAC 30

DWG NO (FS55) 708113888
CONT ON SHEET 2 SH NO 1

DAL RCVRS & ADDRESS CKT



NOTES:
1. ADDRESS STRAPPING TERMINALS ARE LOCATED IN POSITION 20 OF THE MOTHER BOARD.
2. ADDRESS STRAPS ARE NORMALLY AS SHOWN. (04)

DRAWN	APPROVAL	CHG					DWG NO
J. Morris Nov 18, '69	E. C. White Dec 19, 69			C	ISSUE		(FS55) 708113888
ISSUED DEC 22 1969		CHKD					CONT ON SHEET 2 SH NO 1

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING — APPLIED PRACTICES | SURFACES √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

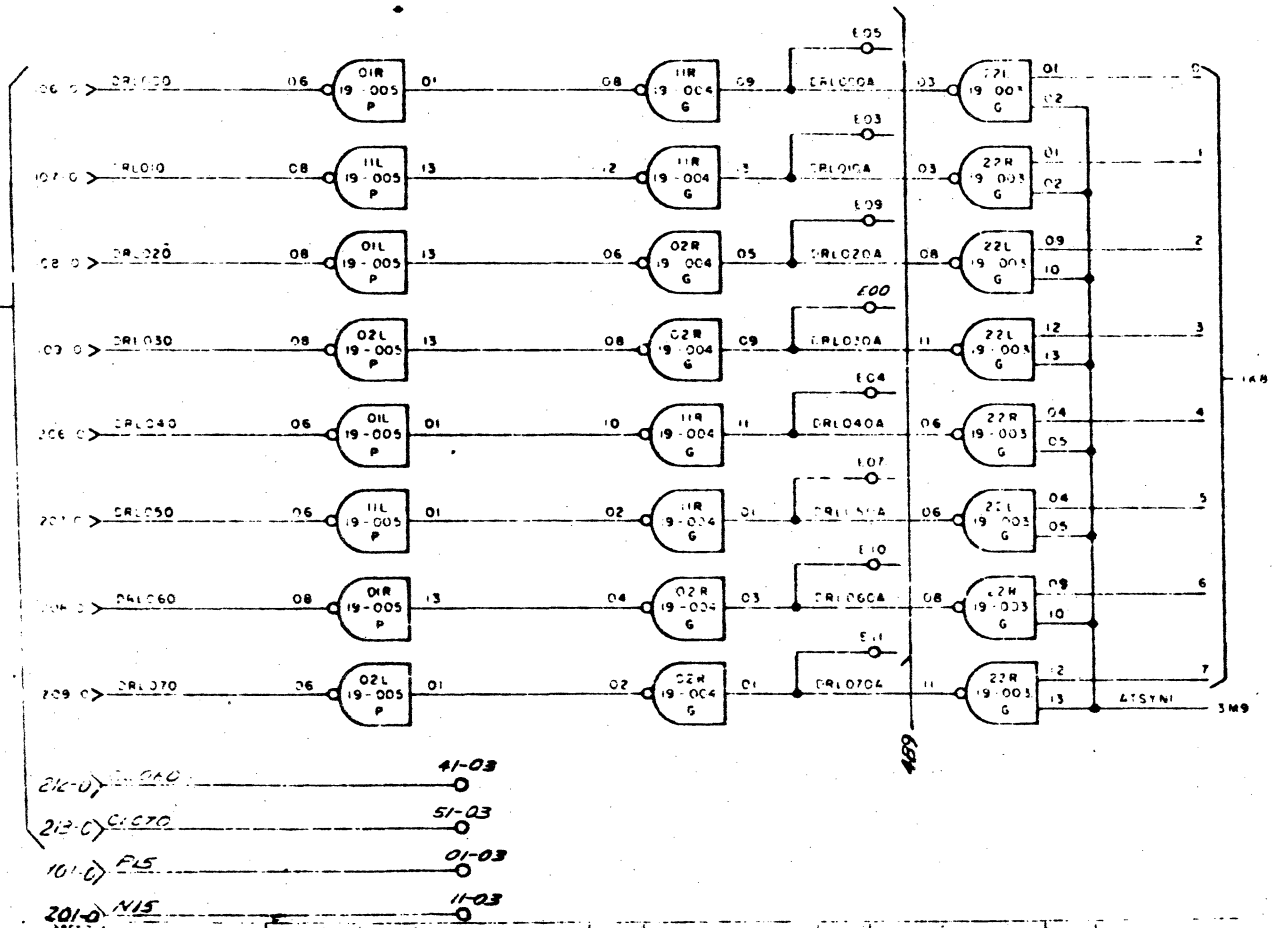
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
CARD READER INTERFACE
FOR GE-PAC 30 | PCP

DWG NO (FS55)
70B113888
CONT ON SHEET 3 SH NO 2

DRL LINE DRIVERS

PART OF MUX BUS



201-C) DRL040 → 41-03
213-C) DRL070 → 51-03
101-C) FL5 → 01-03
201-C) N15 → 11-03

DRAWN J Morse Nov 18, '69	APPROVED E.C. White Dec 19, 69	DES		C	ISSUE	
RELEASED DEC 22 1969		CHKD				

DWG NO (FS55)
70B113888
CONT ON SHEET 3 SH NO 2

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
CARD READER INTERFACE
EMP GE-PAC 30

DWG NO (FS55)
708113888
CONT ON SHEET 4 SH NO 3

CONTROL LINE RCVRS, SYNC & INTERRUPT LOGIC

PART OF MUX BUS

NOTE 1 : PART OF WIRE WRAP CONNECTOR PINS FOR SYSTEM USE.

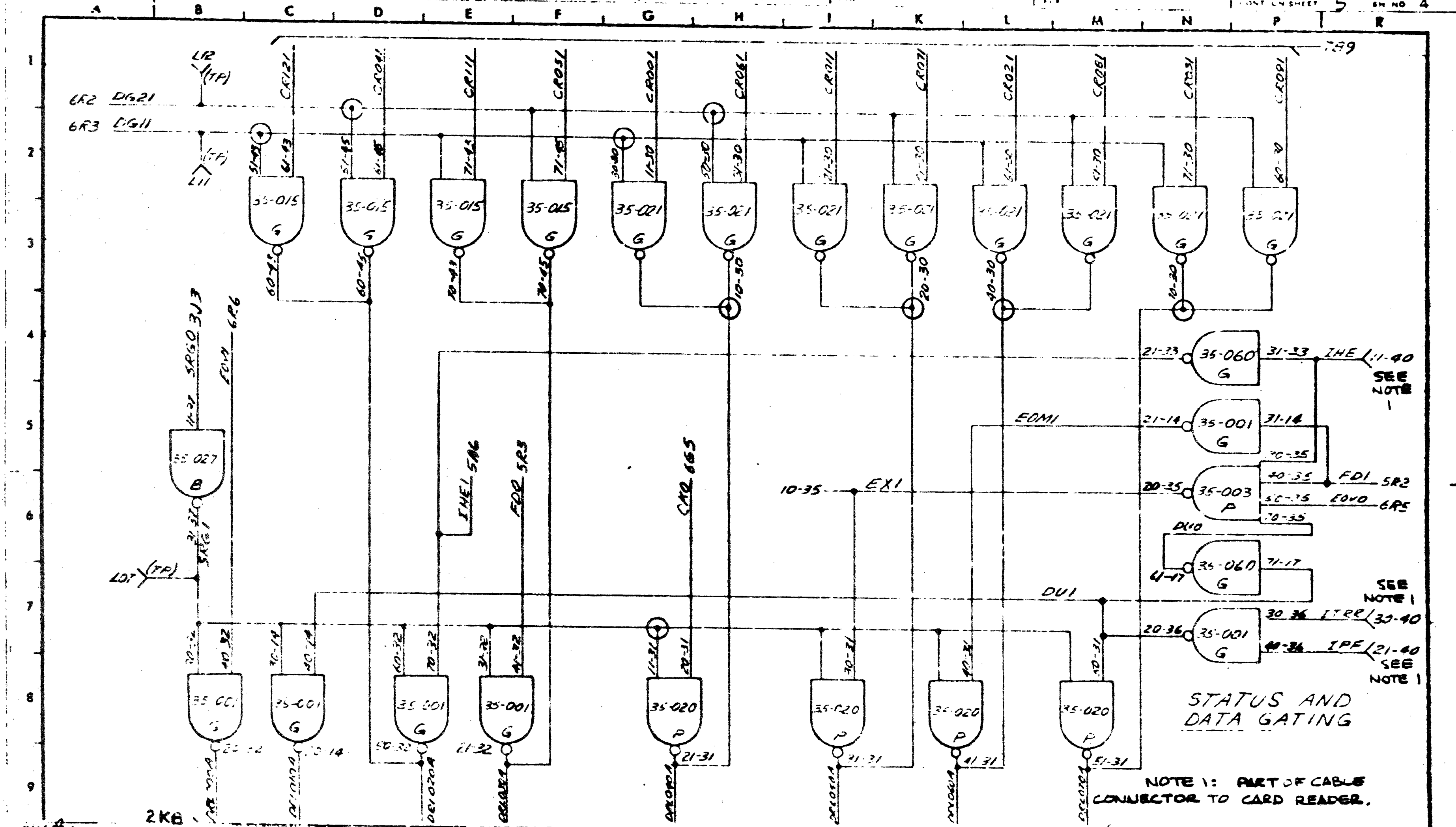
MADE BY	Nov 18, '69	E G White	C	ISSUE
ISSUED	DEC 22 1969	Dec 19 69		

DWG NO (FS55)
708113888
CONT ON SHEET 4 SH NO 3

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

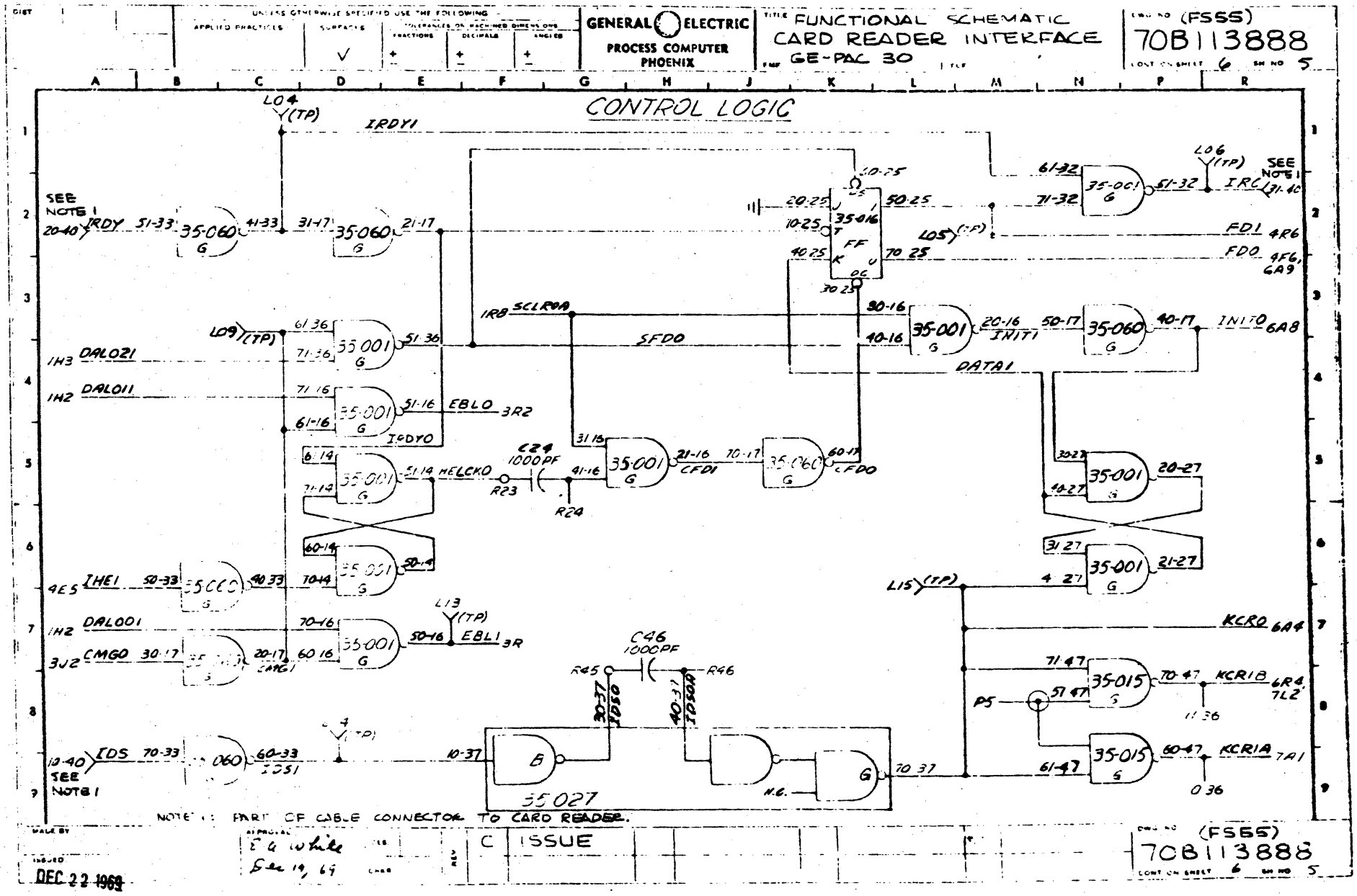
FUNCTIONAL SCHEMATIC
CARD READER INTERFACE
GE-PAC 30

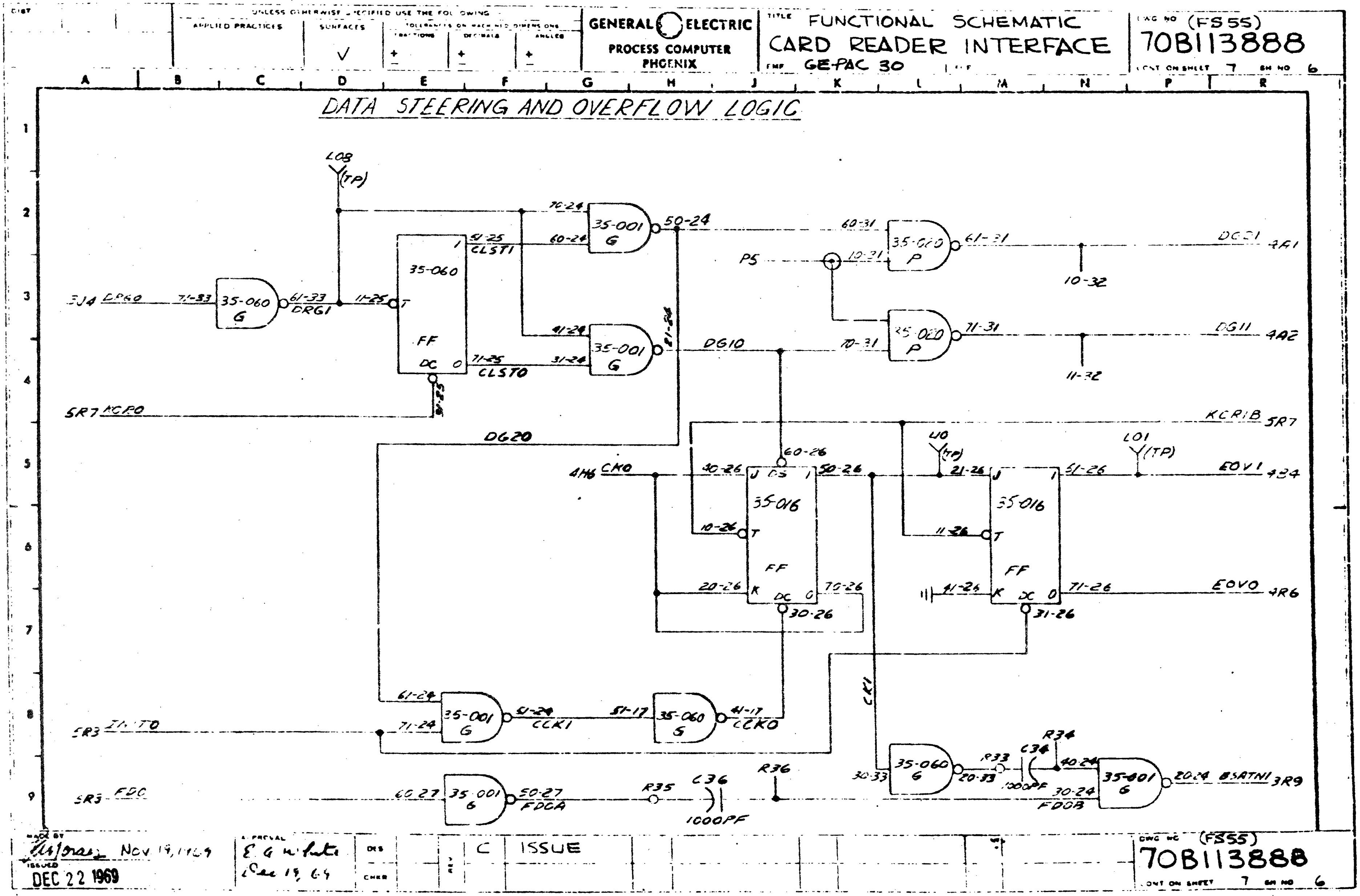
DWG NO (FS55) 70B113888
CONT ON SHEET 5 SH NO 4



MADE BY: Moraz
ISSUED: DEC 22 1969
APPROVAL: E G White Dec 19, 69
REV C ISSUE

DWG NO (FS55) 70B113888
CONT ON SHEET 5 SH NO 4


GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX
TITLE FUNCTIONAL SCHEMATIC
CARD READER INTERFACE
GE-PAC 30
DWG NO (FSSS)
70B113888
CONTROL LOGIC
IRDYI
SEE NOTE 1
IRDY
DALO21
DALO11
DALO01
CMGO
IDS
IHEI
SCLR0A
SFDO
DATAI
INIT0
EBL0
EBL1
IOBYO
CFDI
CFDO
HELCK0
C29 1000PF
C46 1000PF
R23
R24
R45
R46
FF
35-016
35-001
35-060
35-015
35-027
FD1
FD0
KCR0
KCR1B
KCR1A
LO4 (TP)
LO5 (TP)
LO6 (TP)
LO9 (TP)
L13 (TP)
L15 (TP)
L7 (TP)
NOTE 1: PART OF CABLE CONNECTOR TO CARD READER.
ISSUE C
DEC 22 1969
DWG NO (FSSS)
70B113888

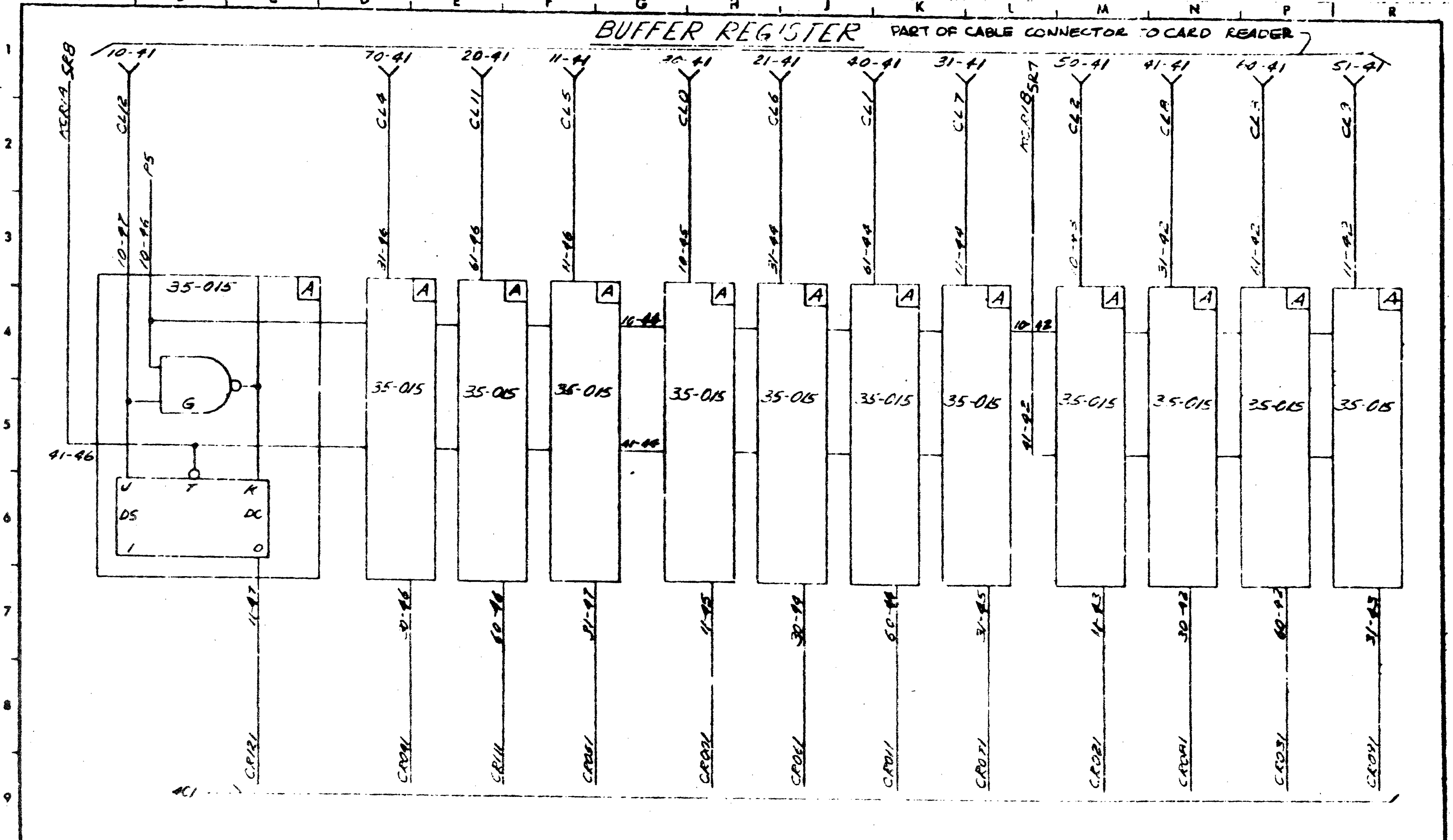

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX
FUNCTIONAL SCHEMATIC
CARD READER INTERFACE
GE-PAC 30
(FS55)
70B113888
DATA STEERING AND OVERFLOW LOGIC
35-001 G
35-060 G
35-060
FF
35-060 P
35-016
35-060 S
35-001 G
CLSTI
CLSTO
DRGI
DG10
DG20
DG11
DG21
KCRIB 5R7
EOVI
EOVO
CKO
CKI
CCKO
FDCA
FDOB
BSATNI
PS
R33
R34
R35
R36
C34
C36
1000PF
ISSUE
DEC 22 1969

GENERAL ELECTRIC PROCESS COMPUTER PHOENIX

FUNCTIONAL SCHEMATIC
CARD READER INTERFACE

GE-PAC 30

DWG NO (FSSS) 70B113888 CONT ON SHEET 8 SH NO 7



MADE BY Nov 1969
ISSUED DEC 22 1969
APPROVAL Dec 19, 69
C ISSUE

DWG NO (FSSS) 70B113888 CONT ON SHEET 8 SH NO 7

DIST

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
CARD READER INTERFACE

FMP GE-PAC 30 | FCP

DWG NO (FS55)
70B113888

CONT ON SHEET | SH NO

BACK PANEL MAP

CONN POS / MOTH. BD / VERT. POS	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2
1	22																	
	21																	
	20																	
	19																	
	18																	
	17																	
	16																	
	15																	
	14																	
	13																	
	12																	
	11																	
	10																	
	09																	
	08																	
	07																	
	06																	
	05																	
	04																	
	03																	
	02																	
	01																	
	00																	

0	22	P5	GND
	21		
	20		
	19		
	18		
	17	RCLRO	
	16		
	15	SYNO	ATNO
	14	RACKO	TACKO
	13	SRQ	CLOTO
	12	DRQ	CLOSO
	11	DAO	
	10	ADRSO	CMDO
	09	DRLO30	DRLO70
	08	DRLO20	DRLO60
	07	DRLO10	DRLO50
	06	DRLOOO	DRLO40
	05	DRL030	DRLO7O
	04	DRL020	DRL060
	03	DRL010	DRLO5O
	02	DRLOOO	DRLO4O
	01	P15	N15
	00	P5	GND

MADE BY		APPROVAL							
[signature]	Nov 19, 1969	E C White	DES			C	ISSUE		
CHKD		Dec 19, 69	CHKD						
DEC 22 1969									

DWG NO (FS55)
70B113888

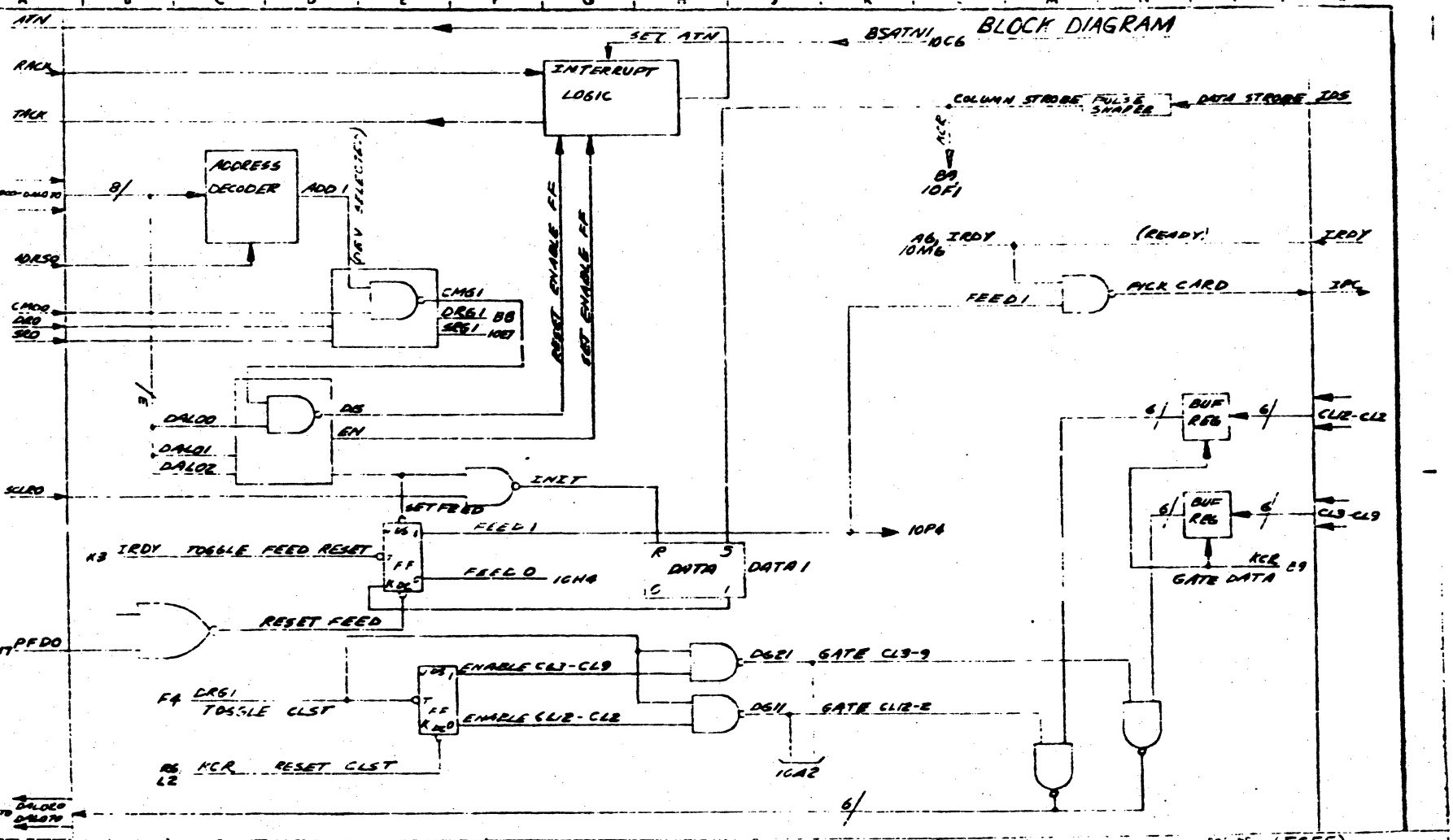
CONT ON SHEET 3 | SH NO 8

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

FUNCTIONAL SCHEMATIC
CARD READER INTERFACE
FOR GE-PAC 30

(FS5S)
70B113888

BLOCK DIAGRAM



C ISSUE

DEC 22 1969

(FS6S)
70B113888

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

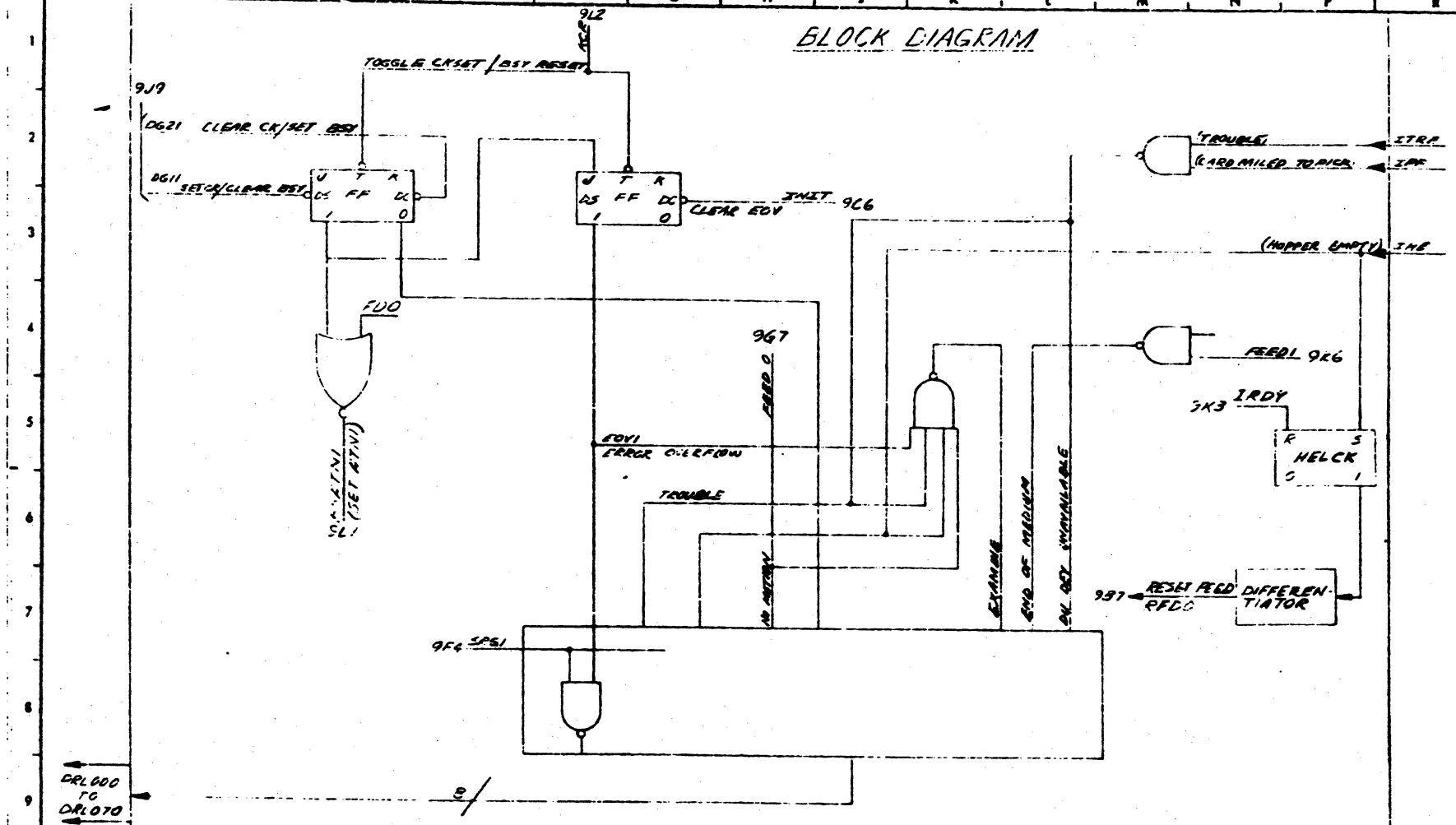
APPLIED PRACTICES	SURFACES	FRACT DIMS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
CARD READER INTERFACE
FOR GE-PAC 30

ENG NO (FSSS) 70B113888
CONT ON SHEET F SH NO 10

BLOCK DIAGRAM



MADE BY		APPROVAL		DES		C	ISSUE	ENG NO (FSSS) 70B113888
H. Holmes	Nov 19, 1969	E.A. White		CHKD				CONT ON SHEET F SH NO 10
ISSUED DEC 22 1969		Dec 19, 69						