GENERAL ELECTRIC

70A111197

PRINT DIST. K7-20

EIGHT-LINE INTERRUPT MODULE
INSTALLATION SPECIFICATION

CONT. ON 1 SH. NO. 0
(02-067A20)

GENERAL NOTES

F.C.F.
FMF: GE-PAC 30

APPROVED BY: E. G. White   DATE: April 15, 70

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
	ISSUE				
B	REV SH. 2 PER	[illegible]			
[illegible]	AN 3WDW-44-028	JUL 15, 70			
B1	REV ALL SHTS PER				
	AN 1-064	J Lima 8-25-71			

REISSUED

A	ISSUE
B	July 21 1970
B1	8-26-71

Made By W. Wong 4-8-'70

Issue Date April 15 1970

PROCESS COMPUTER
PHOENIX, ARIZ.

Dwg. No. 70A111197
Cont. on 1
Sh. No. 0

PCE .5A 7-62

REVISIONS

1. UNPACKING

When this module is shipped with a Processor, it is installed in the chassis so there is no special unpacking procedure. It is only necessary to insure that the module is properly seated in its connector. However, if the Eight-Line Interrupt Module is shipped as an expansion unit, unpack it carefully and check for breakage and damage to components.

2. PHYSICAL CHARACTERISTICS

This module consists of a standard 9 3/4 inch by 10 1/2 inch mother-board and two 17-069F04 cables.

3. LOCATION

The mother-board connects into any I/O slot in the Processor or expansion chassis.

4. CABLES AND WIRING

Refer to Table 3 for information on the connection of the 17-069F04 cables.

Verify that the strap lead between 214-0 and 114-0 (RACK/TACK jumper) is removed from the wiring side of the Processor or expansion card file on the slot chosen for the module. This allows the necessary Interrupt Receive and Acknowledge signals from the Processor to enter the module.

5. DEVICE ADDRESSING

This module is shipped with Device Address X'20' to X'27' factory wired. However, the module can be addressed by four sets of device numbers. The various device addressing include X'20' to X'27', X'28' to X'2F', X'30' to X'37', or X'38' to X'3F'. The module is strapped internally, using 55-038 strap boards for the desired device address. Strapping must be performed for the interrupt address return.

5. (Continued)

Table 1 shows the 35-038 board strapping required (if any) for each of the possible addresses.

TABLE 1 DEVICE ADDRESS MATCH

DEVICE ADDRESS	FROM	TO
X'20' to X'27'	00 00	20 10
X'28' to X'2F'	00	10
X'30' to X'37'	00	20
X'38' to X'3F'	none	

The address can be changed as shown in Figure 1 and Table 2.

6. INSTALLATION CHECK

Run Test Program 70A112463 to determine that the module is correctly installed and operating properly. If not operating properly, verify use time and duration of interrupt signals.

Waveform Transition - Smooth transition
Less than 1.5 microsecond rise and fall times

Waveform Duration - Must be active for a minimum of 4.0 microseconds. To be active, level must exceed 3.0 volts but not greater than 5 volts

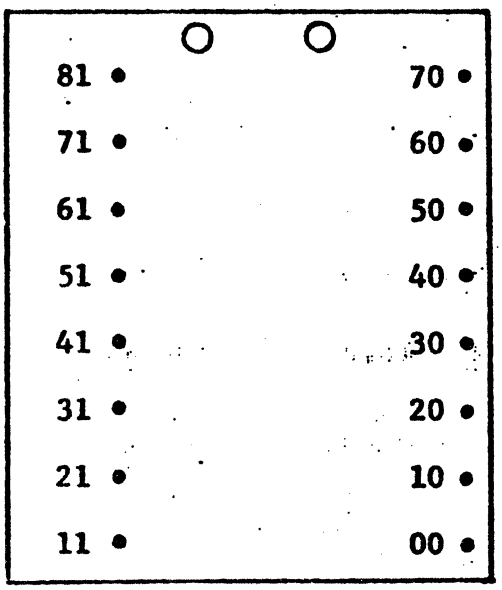


Figure 1. 35-038 Strap Board

1. Pins 70 and 11 go to the inputs to the Address NAND gate.

2. Pins 50 and 21 are ONE inputs.

3. Pins 60 and 31 are ZERO inputs.

TABLE 2. DEVICE ADDRESSING

Pins Going To Address NAND Gate	Pins	Level	Hexadecimal Weight	Examples of Device Addressing	
				X'20'-X'27'	X'38'-X'3F'
70	60 50	0 1	10	60 to 70	50 to 70
11	31 21	0 1	8	11 to 31	11 to 21

TABLE 3. CABLE TERMINATIONS

DESIGNATION	TERMINAL LOCATION
IL71	10-40
IL61	20-40
IL51	30-40
IL41	40-40
IL31	50-40
IL21	60-40
IL11	70-40
IL01	11-40
ACK71	10-42
ACK61	20-42
ACK51	30-42
ACK41	40-42
ACK31	50-42
ACK21	60-42
ACK11	70-42
ACK01	11-42

GENERAL ELECTRIC

70A111199

PRINT DIST. K7-19	PRODUCT SPECIFICATION EIGHT LINE INTERRUPT MODULE	CONT. ON 1	SH. NO. 0
		(02-067A19)	

GENERAL NOTES

F.C.F.

FMT: GE-PAC 30

APPROVED BY: E. G. White DATE: June 11 '70

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
	ISSUE				
A1	ANI-064 REV SHTS 0,1,2	7-9-71 JDL			

REISSUED

A ISSUE

Originator	Issue Date	PROCESS	Dwg. No. 70A111199
E.A. WHITE, June 11,'70	June 23, 1970	COMPUTER PHOENIX, ARIZ.	Cont. on 1 Sh. No. 0

TITLE
PRODUCT SPECIFICATION
EIGHT LINE INTERRUPT MODULE
FIRST MADE FOR GE-PAC 30 (02-067A19)

REVISIONS
A1

1.0 DOCUMENTATION

The following documents and programs are supplied with the Eight Line Interrupt Module:

70B113366	Schematic (FS6)
70A111199	Product Specification
70A111197	Installation Spec.
70A111240	Maintenance Spec.
70A112463	TEST PROGRAM

2.0 PARTS LIST

The Eight Line Interrupt Module consists of:

1 each 32-019 Mother-Board
2 each 17-069F04-12 foot cables, open end

3.0 DIMENSIONS

The Mother-Board has the following dimensions:

Height	9.75 inches
Width	10.5 inches

4.0 WEIGHT

The Mother-Board and cable weigh approximately three pounds.

5.0 POWER - +5volts DC ±10% @ 0.75 amps

6.0 ENVIRONMENTAL

6.1 Temperature 0 - 50°C
6.2 Humidity
6.3 Vibration Equal to or exceeds processor

7.0 DESCRIPTION

7.1 GENERAL

The Eight Line Interrupt Module provides hardware means for assigning interrupts on a priority basis.

7.2 The interface can be connected directly to the I/O MPX Bus.

7.3 The interface contains eight Attention flip-flops: one for each interrupt.

PRINTS TO

7.4 The interface contains eight Arm flip-flops: one for each interrupt. Any Attention can be prevented from being set by resetting the proper Arm bit.

7.5 The interface contains eight Mask flip-flops: one for each interrupt. Any interrupt can be queued up in an Attention flip-flop but be prevented from interrupting the Processor by setting of the proper Mask bit.

7.6 The interface requires 8 device addresses; one for each interrupt.

8.0 ACCEPTANCE TEST

The interface must execute the test program as specified in 70A112463 in order to be considered operational. The program should be run under prescribed voltage variations.

GENERAL ELECTRIC

70A111240

PRINT DIST. 7-21

LIGHT-LINE INTERRUPT MODULE
MAINTENANCE SPECIFICATION

CONT. ON 1 SH. NO. 0
(02-067A21)

GENERAL NOTES

F.C.F.
FMF: GE-PAC30

APPROVED BY: E. A. White DATE: April 15, 70

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
	ISSUE				
A1	ANI-064 REV SHTS 03	JDL 7-6-71			

RE'ISSUED

A	ISSUE
A1	JUL 15 1971

By W. Wong 4-8-70

Issue Date April 15, 1970

PROCESS COMPUTER PHOENIX, ARIZ.

Dwg. No. 70A111240
Cont. on 1
Sh. No. 0

ICE 3A 7-68

TITLE EIGHT-LINE INTERRUPT MODULE MAINTENANCE SPECIFICATION

FIRST MADE FOR GE-PAC 30 (02-067A21)

REVISIONS

1. INTRODUCTION

Eight-Line Interrupt Module, Mother-Board 32-019, provides a means for interrupting the Processor by eight different interrupt lines supplied by an external device. This moduie has the capability of controlling the interrupt by either allowing the interrupt to occur, or inhibiting or delaying the interrupt until a later time.

2. BLOCK DIAGRAM

The Block Diagram for the Eight-Line Interrupt Module is shown in Figure 1. As shown in Figure 1, successive Write Data Commands are sent to the Arm Register and to the Mask Register. The output from the Arm Register plus the chosen Interrupt Line (IL0 through IL7) from external equipment is fed into the appropriate Queue Register. If the Mask Register does not block the interrupt, an Interrupt signal is sent to the Processor. The Processor responds with an Interrupt Acknowledge (RACK0) pulse and the pulse proceeds through the Daisy-Chain Priority until it encounters the circuit involved with the chosen interrupt. An Interrupt Acknowledge is then gated to the external equipment and to the Processor. IL0 is the highest priority interrupt and IL7 the lowest.

PRINTS TO

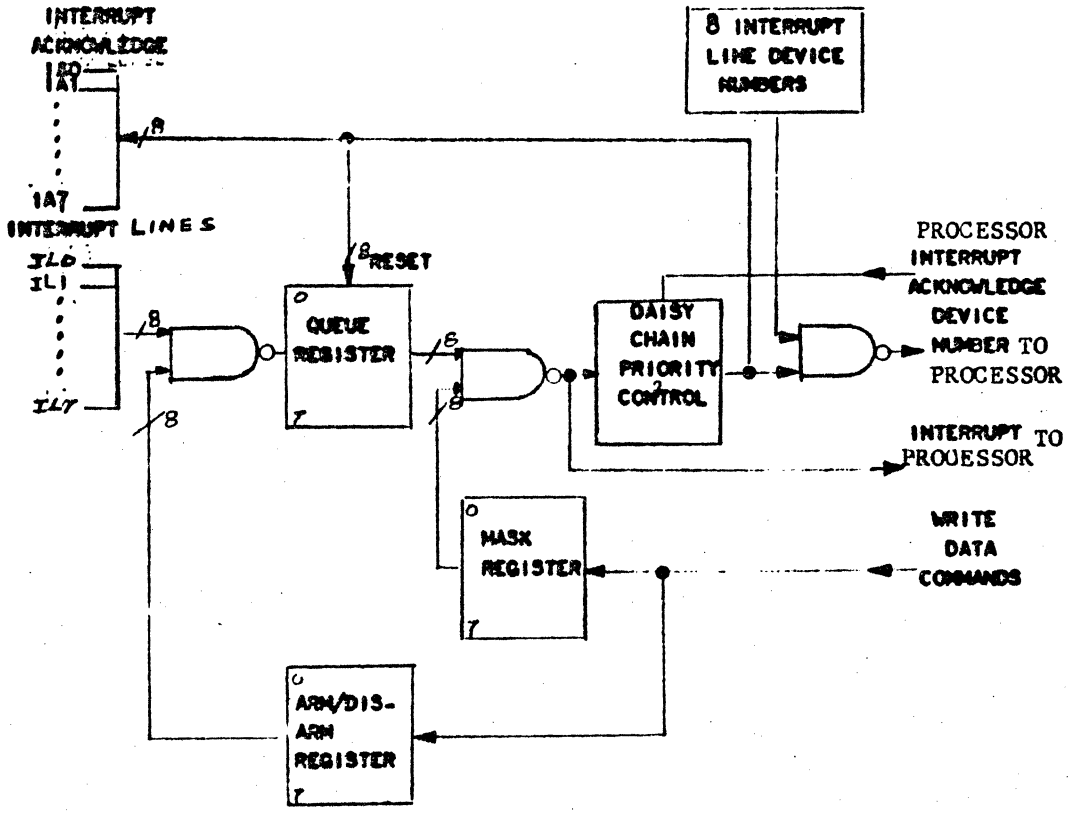


FIGURE 1. EIGHT LINE INTERRUPT MODULE, BLOCK DIAGRAM

3. FUNCTIONAL DESCRIPTION

The functional description of the Eight-Line Interrupt Module is based on the Schematic 70B113366(FS6).

3.1 Device Addressing

Each of the eight external interrupt lines is assigned its own device number. This module can have as its device number any of the following: X'20' to X'27', X'28' to X'2F', X'30' to X'37', or X'38' to X'3F'. This is accomplished by arranging the straps on the 35-038 strap board on FS6 - 1H5, as shown in Table 1.

TABLE 1

STRAP CONNECTION FOR DEVICE ADDRESSING

FROM	TO	DEVICE ADDRESS
00-47 60-47 31-47 00-47	20-47 7C-47 11-47 10-47	X'20' to X'27'
60-47 21-47 00-47	70-47 11-47 10-47	X'28' to X'2F'
50-47 31-47 00-47	70-47 11-47 20-47	X'30' to X'37'
50-47 21-47	70-47 11-47	X'38' to X'3F'

3.2 Initialization

To prepare for the operation of this module, the ARM Registers, shown on Sheet 2, the MASK Registers, shown on Sheet 3, and the Write Data flip-flop on 1M2 must be reset. This is accomplished in either one of two methods. Depressing the INITIALIZE pushbutton on the Processor Display Panel outputs SCLR0 to one input of the NAND gate on 1L8. The resultant high output is inverted and the low inputs from three inverters are used to clear the two registers and the Write Data flip-flop. The other method is by a Command pulse (CMD0) gated from the Processor which is inverted and the resultant high is applied at one input to the NAND gate on 1G8. When the other input to the NAND gate

3.2 Initialization (Cont'd)

is high, the gate is enabled, the signal is buffered and is used to reset the two registers and the Write Data flip-flop.

3.3 Addressing Input

When the Processor gates the correct address for this module via the Data Available Lines (DAL), the pulses are inverted to present all high inputs to the Address NAND gate on 1H3. The NAND gate is enabled, its output is inverted, and a high is applied at one input to the NAND gate on 1M3. At the same time, ADRS0, from the Processor is inverted and the resultant high is applied at the other input to the NAND gate on 1M3. The gate is enabled, sending ADSY0 to several places:

1. It is inverted and buffered to send SYN0 to the Processor.

2. ADSY0 is applied to one input of the NAND gate on 1L5. If ADSY0 is high, the second input to the NAND gate (ADRS1) will reset the Address flip-flop (low on 61-03 at 1L6).

3. It is applied to one input of the flip-flop configuration on 1L6 (41-03). If this line is active (low), it will set the Address flip-flop.

The output from the one side of the flip-flop configuration is applied as one input to several NAND gates at 1F7. This will either enable or disable the control lines coming from the I/O Bus.

3.4 Write Data

The first Write Data (DA0) pulse from the Processor is inverted to enable the NAND gate at 1F7 and produce DASY0. This pulse sends SYN0 to the Processor. DASY0 is inverted and the resultant pulse is sent to the T input of the Write Control flip-flop on 1L2 and to NAND gate at 1N2. The lagging edge of the pulse sets the flip-flop. However, since both inputs to the NAND gate on 1N2 are high at the same time, the gate is enabled. The resultant low is applied at the input to the Arm NAND gate at 1N4, producing ARM1.

The second Write Data (DA0) pulse follows the same path as the first DA0 until it reaches the Write Control flip-flop at 1L2. Since the flip-flop is set, the lagging edge of the pulse resets it. However, as both inputs to the NAND gate on 1N1 are high at the same time, the gate is enabled and the resultant low is inverted to produce MASK1.

3.5 Arm and Mask Registers

There are eight Arm flip-flops and eight Mask flip-flops; one Arm and one Mask flip-flop for each interrupt line. Since the logic for the flip-flops is identical, the description of logic for one flip-flop will be the same for the others.

As shown on Sheet 2 of FS6, when the Data Available Lines from the Processor which include DAL070 is gated to the module, DAL071 is applied as the J input to the Arm Register.

When DAO is gated from the Processor, ARM1 sets the register which applies a high level to the NAND gate at 2B5.

An Interrupt Line (IL71) from external equipment is applied to the other input of the NAND gate, enabling the gate and causing a low to be applied to the S input of the Queue flip-flop on 2B7. This low sets the Queue flip-flop. However, since the Mask Register, shown on 3B5, is in a reset condition, the ATN71 line is held to ground. If a DAL071 pulse is sent with the next DAO which produces a MASK1 pulse, the Mask Register is set and the ground is removed from ATN71.

3.6 Daisy-Chain Procedure

When an ATN line is high, an ATNO pulse is sent to the Processor, which responds with a RACKO pulse, as shown on 5L8. This pulse initiates a search through the daisy-chain network of flip-flop configurations and NAND gates shown on Sheets 4 and 5 until it reaches the circuit containing the high ATN line. At that time, the appropriate ATSY line goes low and the appropriate ACK line goes high. The ACK line is returned to the external equipment as an Interrupt Acknowledge. It also resets the ATN flip-flop on Sheet 2, removing the ATN high level.

3.7 Output to the Processor

As shown on Sheet 6 of FS6, there are eight ATSY lines, each representing one of the eight interrupt lines. If all the lines are high, there is no output via the Data Request Lines to the Processor. However, when an ATSY line goes low, the output from the NAND gate on 6M4 goes high. The output is buffered and sent as SYNO to the Processor. The appropriate NAND gates are enabled and the DRL signal (020, 030, 040) is sent to the Processor. At the same time the appropriate NAND gates whose outputs are tied to DRL050, DRL060, and DRL070 are enabled and sent to the Processor, indicating the Device Address of the interrupt line.

3.8 Status Request

As shown on Sheet 1 of FS6, the Processor sends Status Request (SRO) to the module. SRO is inverted and presents a high to one input of the NAND gate on 1P9. When the other input to the NAND gate is high, the gate is enabled and the resultant low, SRSYO is buffered to send SYNO to the Processor.

4. MNEMONICS LIST

This section provides an alphabetical list of the mnemonics used in the Eight-Line Interrupt Module. A brief description of each mnemonic and a reference to its source on the Schematic FS6 are also provided.

MNEMONIC	MEANING	LOCATION
ACKO1 through ACK31	Acknowledge Pulse: External equipment apprised of the fact that this is the chosen Interrupt Line.	5D8 through 5N8
ACK41 through ACK71	Acknowledge Pulse: External equipment apprised of the fact that this is the chosen Interrupt Line.	4D8 through 4N8
ADRSO	Address Signal: The Processor sends an Address signal to the module.	1B7
ADSYNO	Address Sinc: Tells Processor that Module has received Address.	1R4
ARM1	Arm Pulse: Toggles the Arm Register.	1R4
ATNO	Attention: Attention pulse to the Processor.	4B8
ATNO1 through ATN71	Attention: Set output from ATN flip-flop.	2B9 through 2N9
ATSY00 through ATSY30	Attention Sync Lines: Attention Sync Lines determining Interrupt Line.	5D4 through 5N4
ATSY40 through ATSY70	Attention Sync Lines: Attention Sync Lines determining Interrupt Line.	4D4 through 4N4
CDSYO	Command Sync: Informs Processor CMDO has been received.	1H9

MNEMONIC	MEANING	LOCATION
CMD0	Command: Clears all registers and Write Data flip-flop.	1B8
DA0	Write Data: Sends data to Arm and Mask Registers alternately.	1B7
DAL000 through DAL070	Data Available Lines: Data gated from the Processor.	1B2 through 1B6
DAL001 through DAL071	Data Available Lines High: Sets either the Arm or Mask Register.	1F1 through 1F6
DASY0	Write Data Sync: Informs Processor that Module has received DA0 pulse.	1H9
DRL020 through DRL040	Data Request Lines: Sends Data to the Processor.	6M7 through 6M9
DRL050 through DRL070	Data Request Lines: Sends Data to the Processor.	6C5 through 6E5
IL0 through IL7	Interrupt Lines: Interrupt of each line from external equipment.	2B4 through 2P4
MASK1	Mask Pulse: Toggles the Mask Register.	1R3
RACK0	Receive Acknowledge: Receive acknowledgement from the Processor.	5L8
SCLR0	System Clear: Clears the registers and the Write Data flip-flop.	1K8
SR0	Status Request: Request of status from the Processor.	1B9
SRSY0	Status Request Sync: Informs the Processor that SR0 has been received by the module.	1G9
SYN0	Synchronization Line: Informs the Processor that the various signals have been received.	6R4
TACK0	Transfer Acknowledge: Part of the daisy-chain procedure.	4B1

REVISIONS

PRINTS TO

GENERAL ELECTRIC

70A110443

PRINT DIST.	PROGRAMMING SPECIFICATION	CONT. ON 1	SH. NO. 0
K7-15	8-LINE INTERRUPT MODULE		

GENERAL NOTES

F.C.F.
FMF:

APPROVED BY: _____ DATE: 12-6-71

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	Issue				

REISSUED

A	Issued				

Made By	Issue Date		Dwg. No. 70A110443
J. Lima/LAP	DEC 9 1971	PROCESS COMPUTER PHOENIX, ARIZ.	Cont. on 1 Sh. No. 0

FCE 20A 7-62

1. INTRODUCTION

The 8-Line Interrupt Module allows external interrupts to be generated by eight external circuits. These interrupts may be selectively armed or disarmed, enabled or disabled, under program control. If a line is disarmed, any signal on that line is not sensed by the module in any way. If armed, a signal on a line is queued (stored) in an interrupt flip-flop. This flip-flop, being set, interrupts the processor when and if the line is enabled. Processor interrupts occur only if a line is both armed and enabled.

Device Numbers X'20' - X'27' are normally assigned to this device. Write and Output Command Instructions may be addressed to any of these. Acknowledging an interrupt will return the number corresponding to the line causing the interrupt, and a status byte of zeros.

Hardware design requires that the 8 interrupts have 8 consecutive addresses of the form:

X'NO' - X'N7' or X'N8' - N'NF'

Where N = 2 or 3

Note that interrupt lines which are not connected externally will cause interrupts if they are armed and enabled.

2. STATUS AND COMMAND BYTES

No status or command byte exists for this device.

3. PROGRAMMING CONSIDERATIONS

This module contains an 8-bit arm register and an 8-bit enable register. A one-bit, in either register, arms or enables the corresponding interrupt. Two Write Data (WD or WDR) Instructions (using any of the eight device addresses for this equipment) are used to update the arm and enable registers. The first Write Data (WD or WDR) sets up the arm register while the second sets up the enable register. The most significant bit in the register affects the lowest address interrupt line which has highest priority.

Any Output Command (OC or OCR) Instruction to this device will disarm, disable, and clear all eight interrupts. It will also reset Write steering. Depressing INITIALIZE on the Processor has the same effect.

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE

FUNCTIONAL SCHEMATIC, INTERRUPT MODULE

DRAWING NUMBER 708113366 | CONT OA | PAGE 0

FIRST MADE FOR GE-PAC 30

(FS6)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				
B	REV SH OA PER	A. J Lewis			
E&W	AN 6WDW-44-023	JUNE 9 '70			

REISSUED

A. Dove
B. July 1, 1970

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS6)

MADE BY	APPROVAL										DWG NO	CONT	PAGE
[illegible] 2/13/70	E.G. White										708113366	OA	0
ISSUED Feb 19, 1970	2-13-70										PRINTS TO K7-08		

PCR 20

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE	DWG NO (FS6)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC, INTERRUPT MODULE	70B113366
		√	±	±	±	FMP GE-PAC 50 | FCF	CONT ON SHEET | SH. NO OA	

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX, SUPPORTING INFO.	OA	-	-	3																	
FUNCTIONAL SCHEMATIC	1	1	2	3																	
	2	1	2	3																	
	3	1	2	3																	
	4	1	2	3																	
	5	1	2	3																	
	6	1	2	3																	
BACK PANEL MAP	7	-	-	3																	
ISSUE DATE		7-12-67		10-14-68																	

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD ASSEMBLY	32-019 R03
TOP ASSEMBLY	02-067 R03

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.
3. IN THE EVENT THAT THE REVISION LEVEL STAMPED ON THE PWB DOES NOT CORRESPOND TO THAT IN THE SUPPORTING INFORMATION TABLE, PLEASE REQUEST SCHEMATIC OF THE CORRECT REVISION LEVEL FROM: GENERAL ELECTRIC.
   40 FEDERAL STREET
   WEST LYNN, MASS. 01905

MADE BY	APPROVAL	DES.	REV.								DWG. NO. (FS-6)
R.H. Clare 2/13/70	E. A. White 2/13/70	CHKR.		B							70B113366
ISSUED Feb. 19, 1970 FC 444											CONT ON SHEET | SH. NO. OA

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING -

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

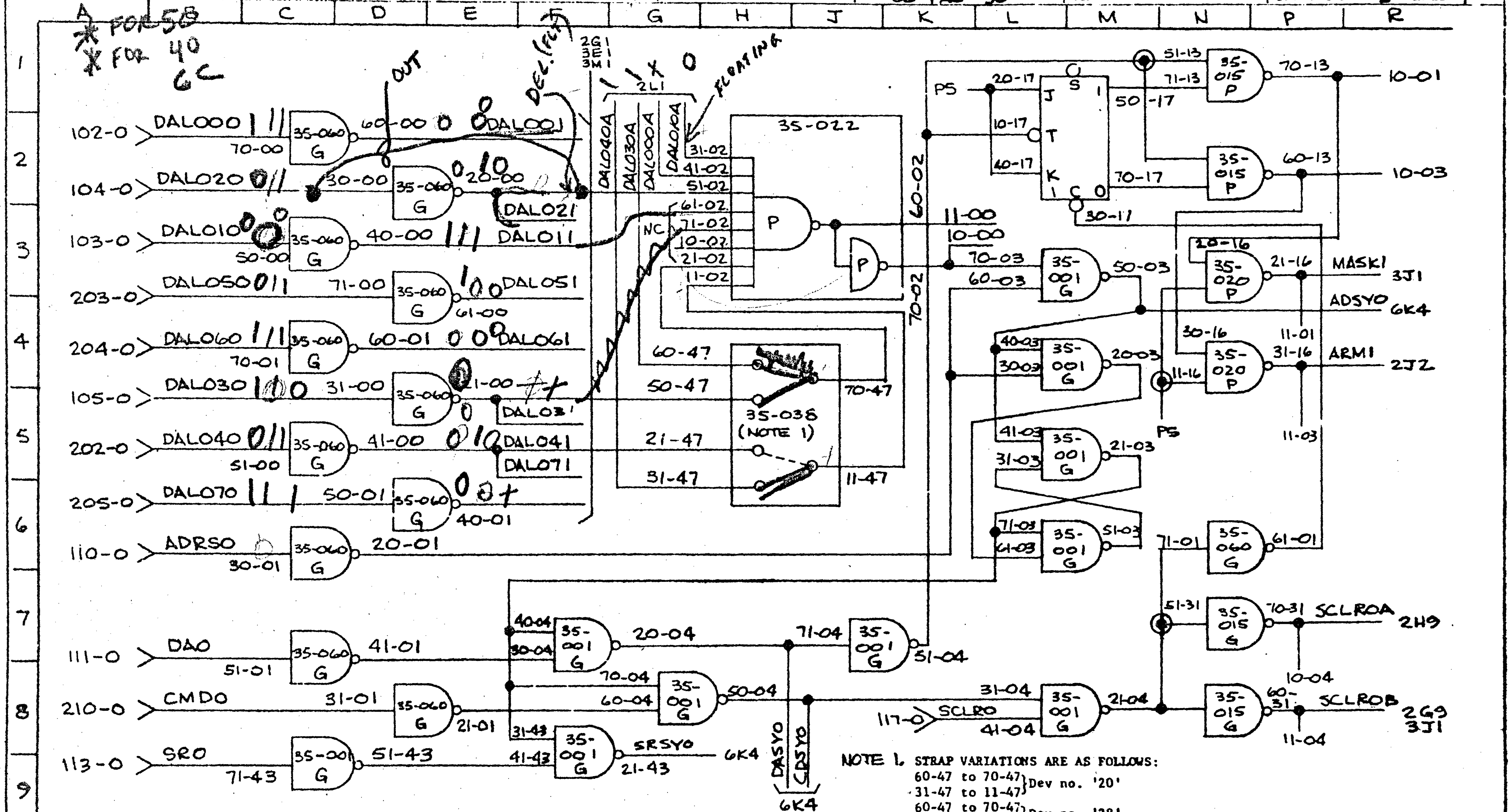
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC, INTERRUPT MODULE

FMF GE-PAC 30

DWG NO (FS6) 70B113366

CONT ON SHEET 2 SH NO. 1



NOTE 1. STRAP VARIATIONS ARE AS FOLLOWS:

60-47 to 70-47 }
31-47 to 11-47 } Dev no. '20'

60-47 to 70-47 }
21-47 to 11-47 } Dev no. '28'

50-47 to 70-47 }
31-47 to 11-47 } Dev no. '30'

50-47 to 70-47 }
21-47 to 11-47 } Dev no. '38'

MADE BY	APPROVAL	DES.	REV.
2/13/70	E. G. White		
Feb. 19, 1970	Feb 13, 70	CHKR.	

PC 444

DWG. NO. (FS-6) 70B113366

CONT ON SHEET 2 SH NO. 1

WIRE CHANGES TO INT. MODULES 4, 5 & 6

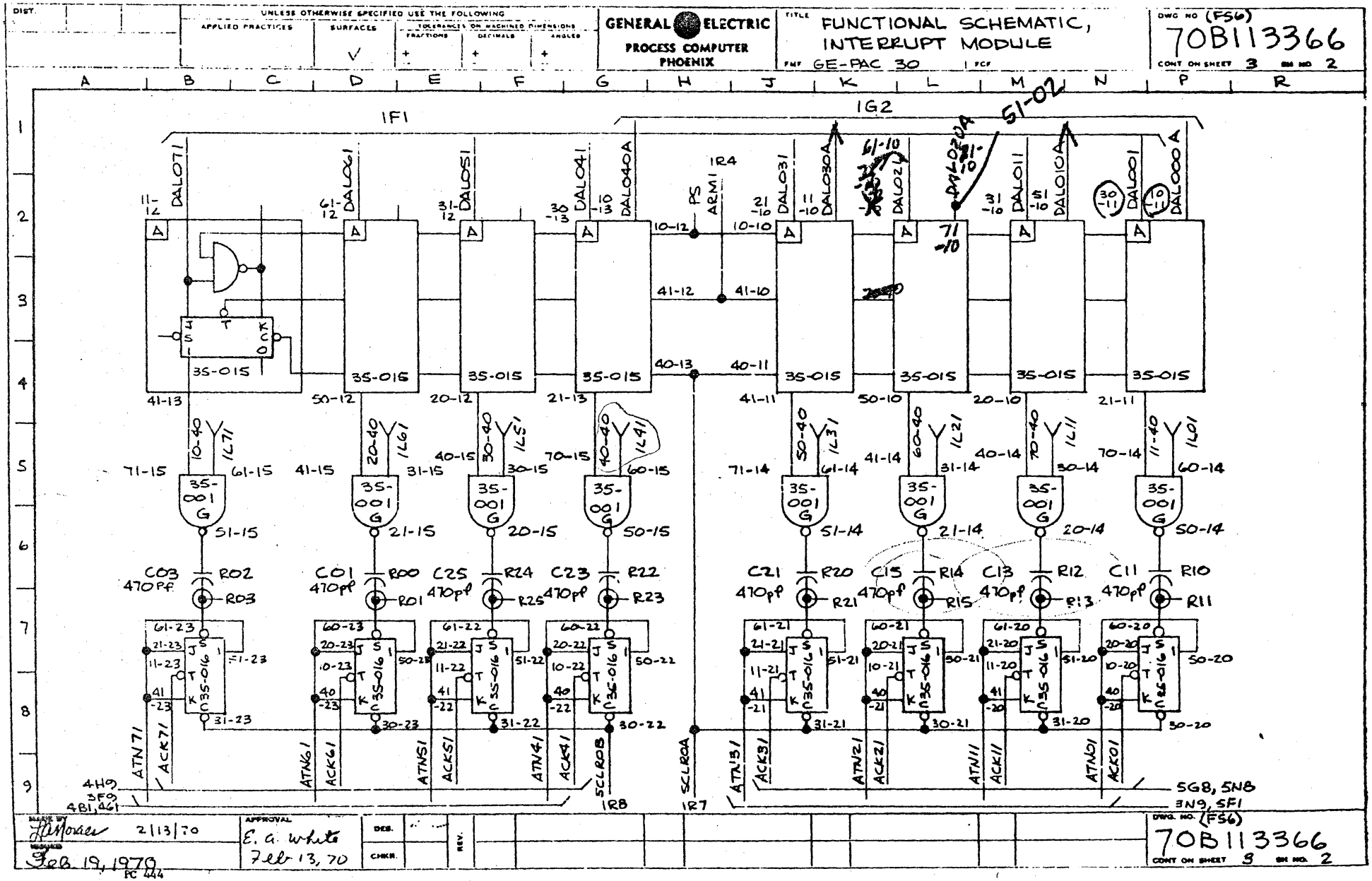
ADDRESS 40-47 (DB47 STRAP FOR 20)

1.	DELETE	31-02	TO	51-10	DALO10A
	DELETE	20-00	TO	51-02	DALO21
	DELETE	51-02	TO	61-10	DAL21
	DELETE	70-33	TO	108-0	DRLO20*
2.	ADD	40-00	TO	61-02	DALO11
	ADD	20-60	TO	61-10	DALO21
	ADD	71-10	TO	51-02	DALO20A
	ADD	70-33	TO	107-0	DRLO10

ADDRESS 48-4F (DB47 STRAP FOR 28)

SAME AS ABOVE

ADDRESS 50-57 (DB47 STRAP FOR 30)


GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX
FUNCTIONAL SCHEMATIC, INTERRUPT MODULE
GE-PAC 30
70B113366
IF1
IG2
IR4
IR8
IR7
35-015
35-016
35-001 G
C03 470pf
C01 470pf
C25 470pf
C23 470pf
C21 470pf
C15 470pf
C13 470pf
C11 470pf
ATN71
ACK71
ATN61
ACK61
ATN51
ACK51
ATN41
ACK41
SCLR08
SCLR04
ATN31
ACK31
ATN21
ACK21
ATN11
ACK11
ATN01
ACK01
SG8, SN8
SN9, SF1
4H9
3F9
4B1, 4G1
Feb 19, 1970
PC 444

DIST

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACH REQ'D REMOVING: FRACTIONS ± | DECIMALS ± | ANGLES ±

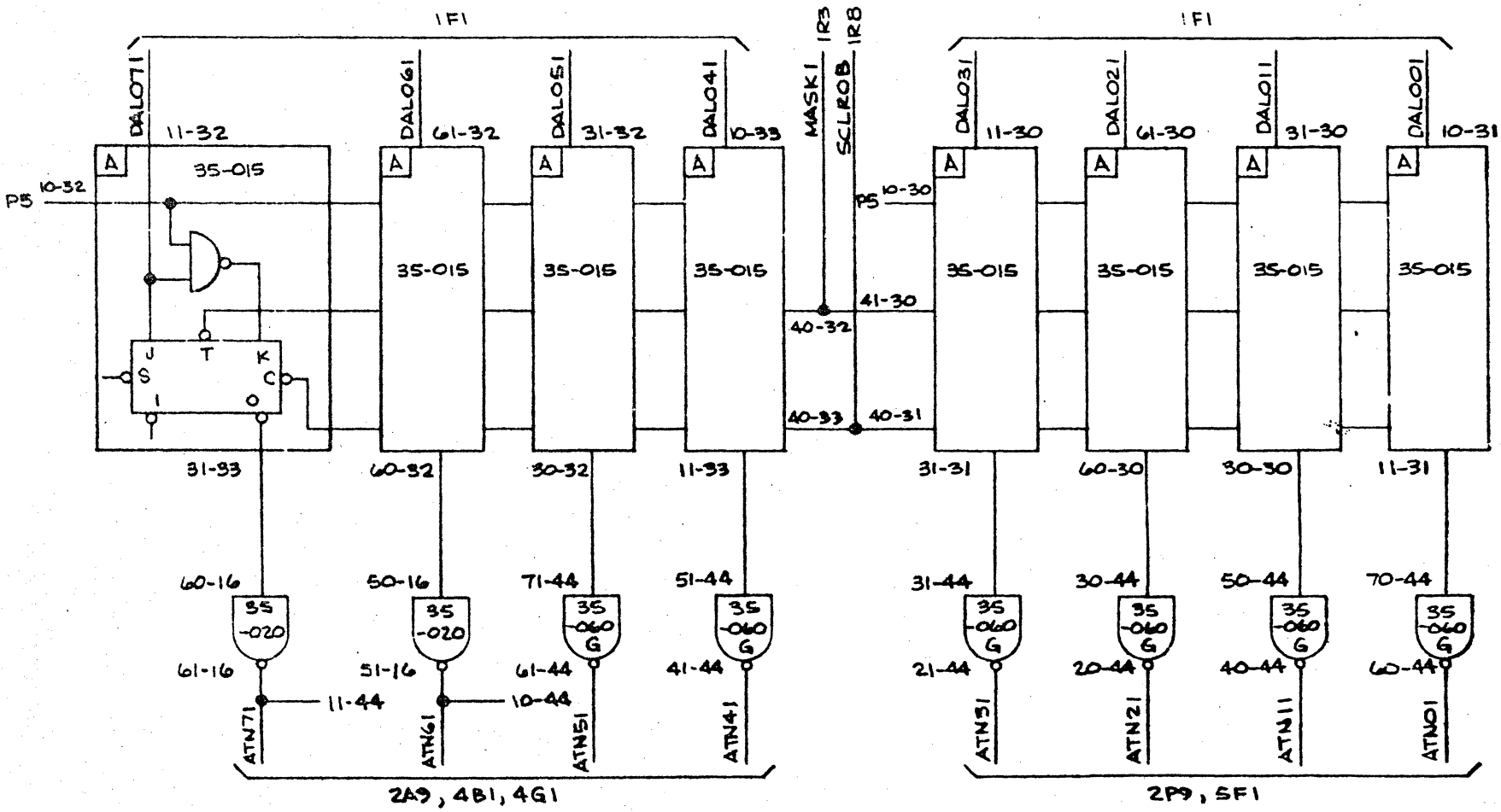
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC, INTERRUPT MODULE

FMF GE-PAC 30 | FCF

DWG NO (FSG) 70B113366
CONT ON SHEET 4 SH NO 3

A B C D E F G H J K L M N P R



DRWN J Moreau 2/13/70	APPROVAL E. G. White Feb 13, 70	DES		REV										DWG NO (FSG) 70B113366	
Feb 19, 1970 K W		CHKR												CONT ON SHEET 4	SH NO 3

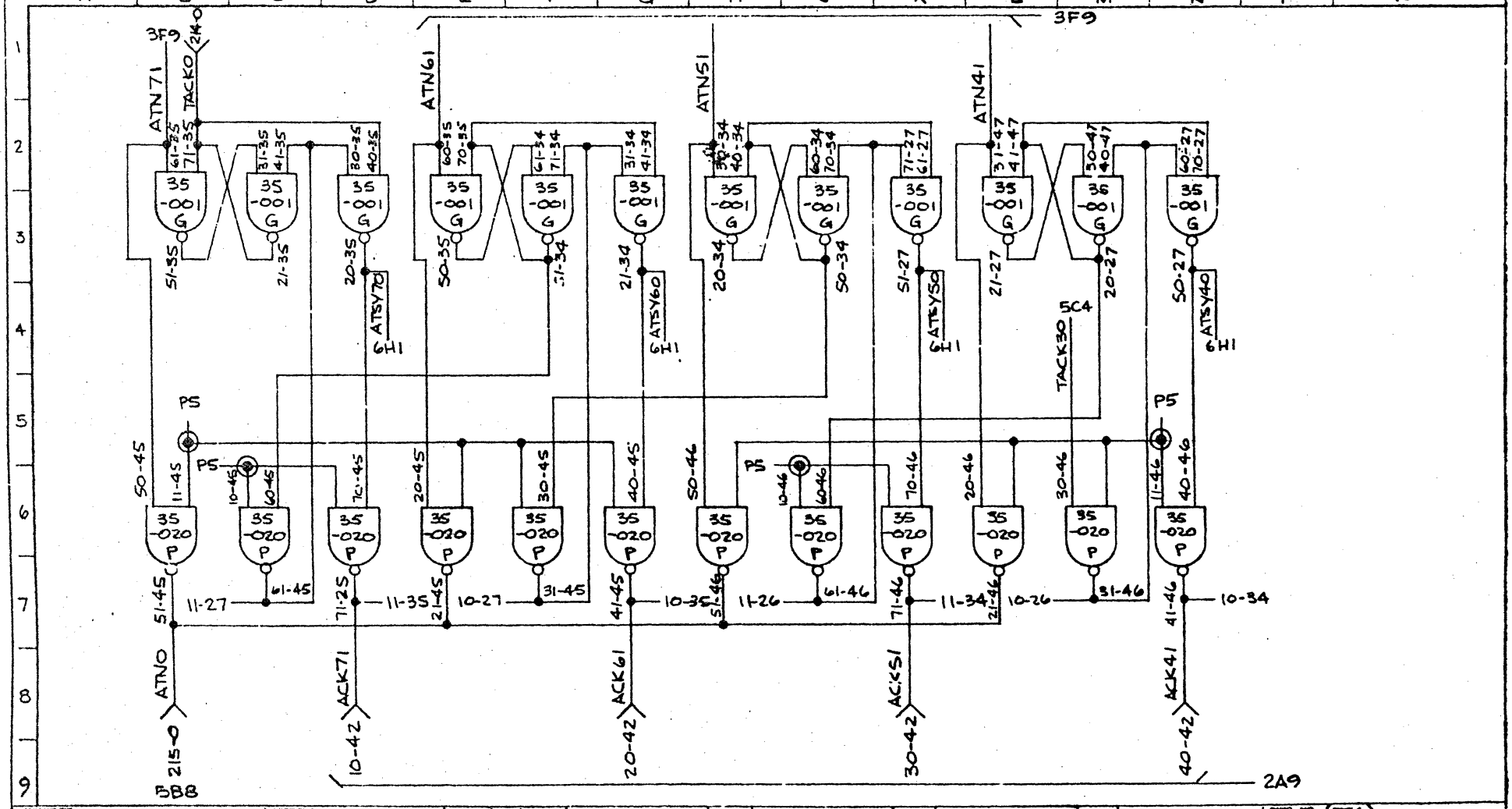
DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

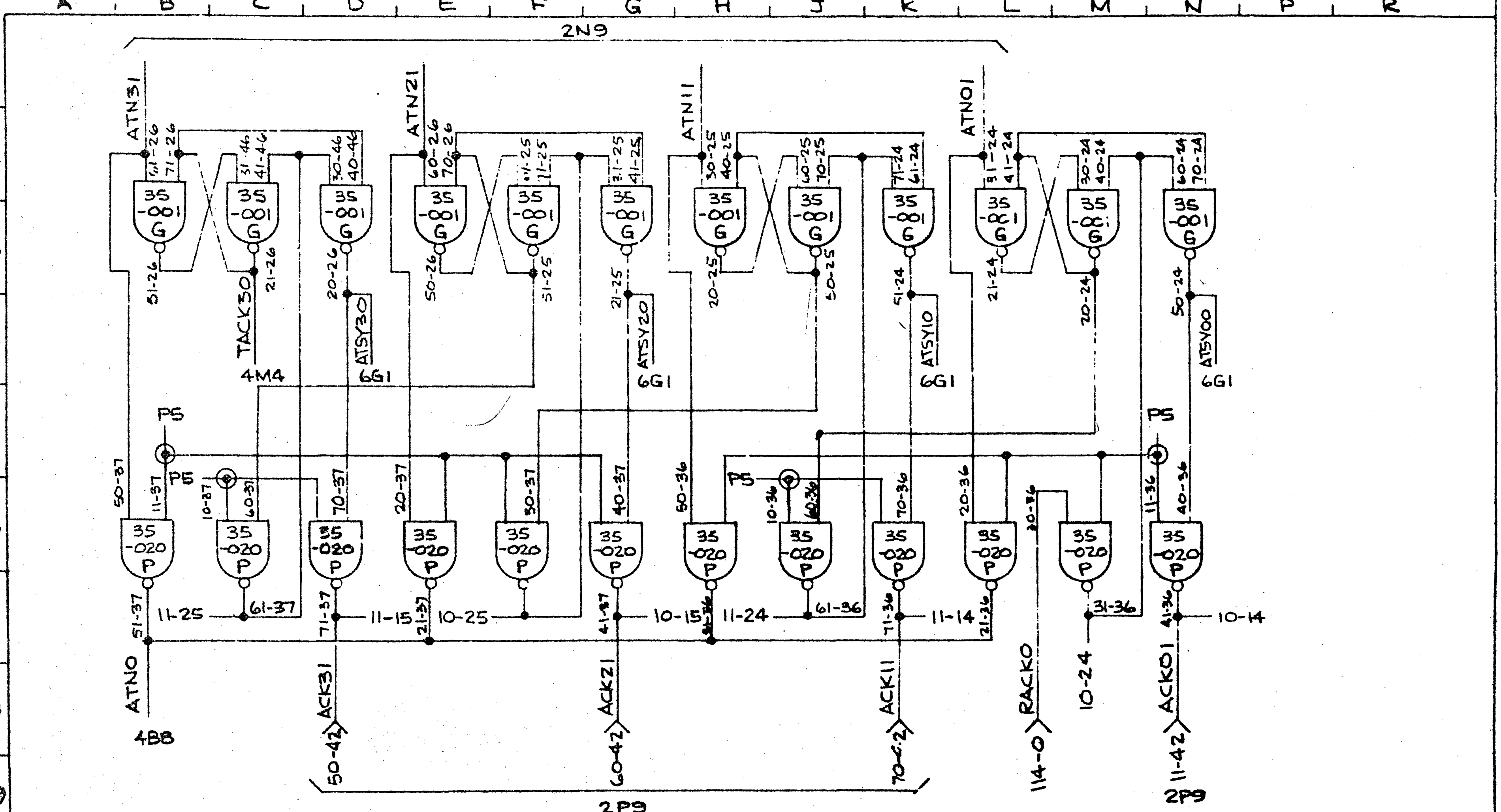
TITLE FUNCTIONAL SCHEMATIC, INTERRUPT MODULE
PMF GE-PAC 30 | ECP

DWG NO (PSG) 70B113366
CONT ON SHEET 5 SH NO 4



DRAWN BY	DATE	APPROVAL		DWG. NO. (PSG)
L. Moreau	2/13/70	E.G. White	DES.	70B113366
ISSUED Feb 19, 1970 PC 444		Feb 13, 70	CHKR.	CONT ON SHEET 5 SH NO. 4

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE	DWG NO (PS6)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC, INTERRUPT MODULE	70B113366
		√	±	±	±		FMF GE-PAC 30	CONT ON SHEET 6 SH NO 5



MADE BY		APPROVAL	DES.		REV.	DWG. NO. (PS6)
LaMoreaux 2/13/70		E. G. White				70B113366
ISSUED Feb. 19, 1970	PC 444	Feb 13, 70	CHKR			CONT ON SHEET 6 SH NO. 5

DIST.

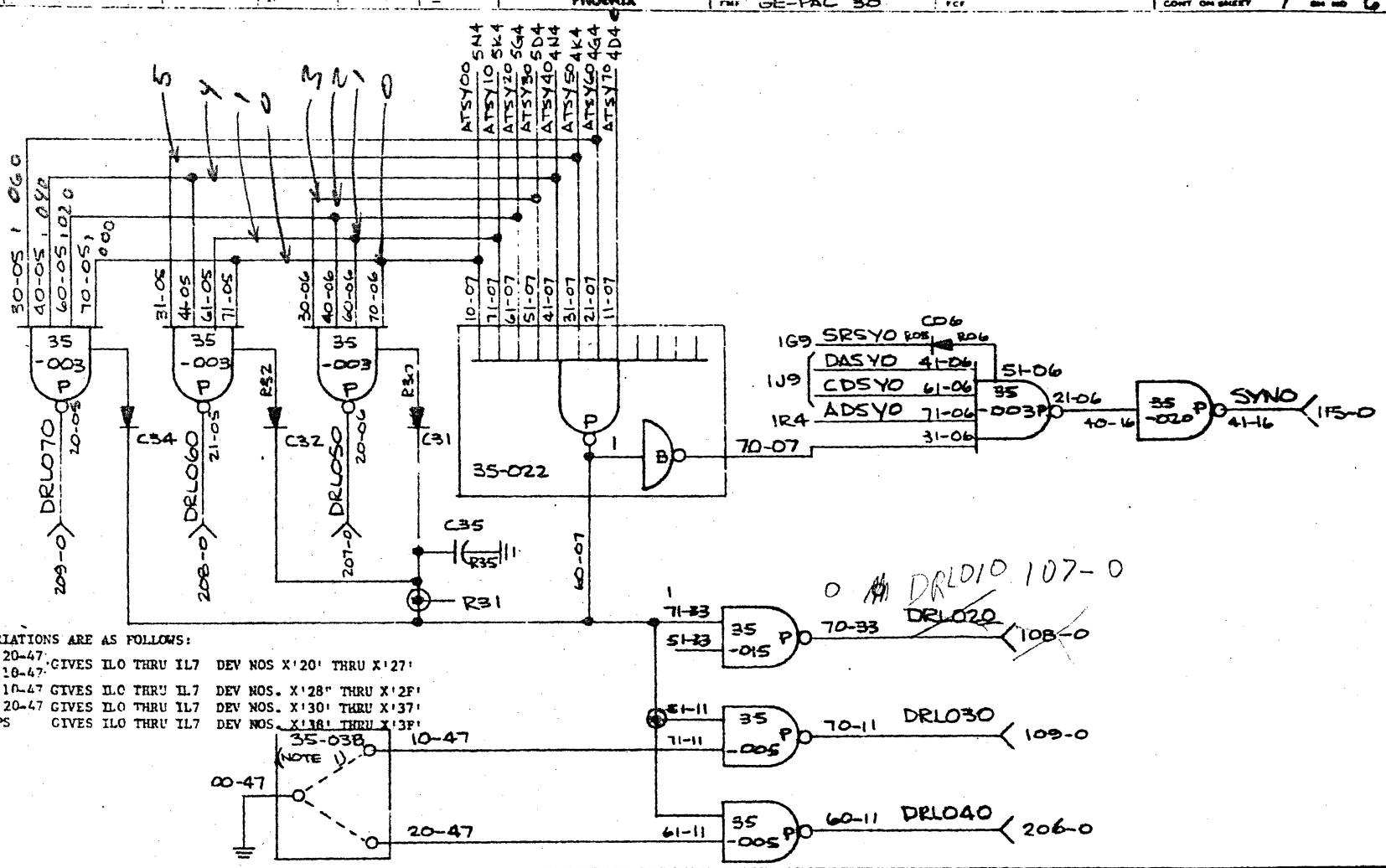
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE: FUNCTIONAL SCHEMATIC, INTERRUPT MODULE
FMF: GE-PAC 30 FCF:

DWG NO (FSG) 70B113366
CONT ON SHEET 7 REV NO 6



NOTES: 1. STRAP VARIATIONS ARE AS FOLLOWS:
00-47 TO 20-47 GIVES IL0 THRU IL7 DEV NOS X'20' THRU X'27'
00-47 TO 10-47 GIVES IL0 THRU IL7 DEV NOS. X'28" THRU X'2F'
00-47 TO 20-47 GIVES IL0 THRU IL7 DEV NOS. X'30' THRU X'37'
NO STRAPS GIVES IL0 THRU IL7 DEV NOS. X'38' THRU X'3F'

0 # DRL010 107-0

A | B | C | D | E | F | G | H | J | K | L | M | N | P | R

DRAWN L.L. Moraca 2/13-70
APPROVAL E.C. White Feb 13 70
DES.
CHECK
REV.
ISSUED Feb 19, 1970 PC 444

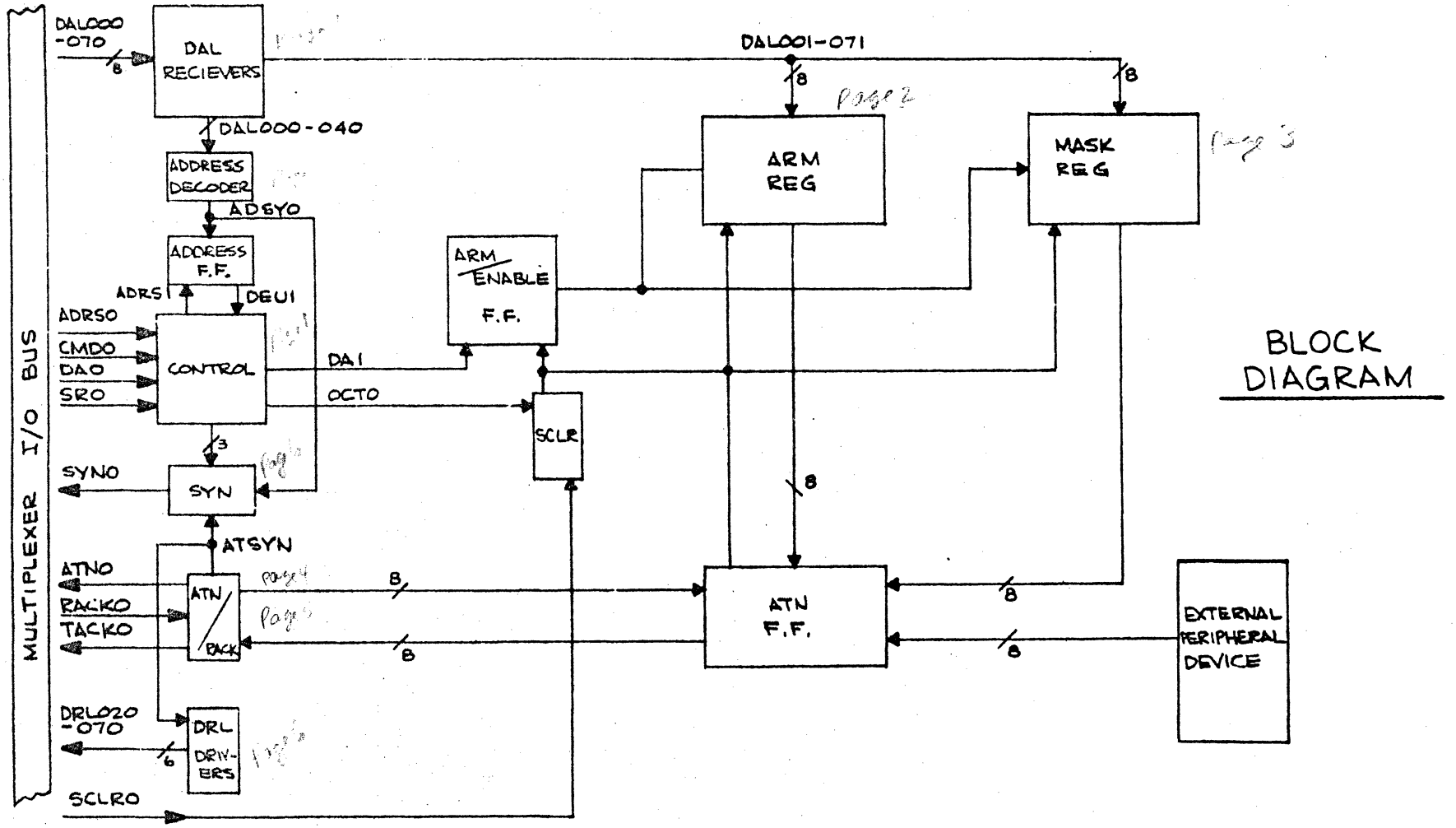
DWG NO (FSG) 70B113366
CONT ON SHEET 7 REV NO 6

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE	DWG NO (FS6)
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS			PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC INTERRUPT MODULE	70B113366
		FRACTIONS	DECIMALS	ANGLES		FMF GE-PAC 30 1 FCF	CONT. ON SHEET 8 SH NO 7
	√	±	±	±			

BACK PANEL MAP

CONN POS				
MOTH. BD				
VERT. POS		HORIZ POS		
		0	1	2
1	22			
	21			
	20			
	19			
	18			
	17			
	16			
	15			
	14			
	13			
	12			
	11			
	10			
	09			
	08			
	07			
	06			
	05			
	04			
	03			
	02			
	01			
	00			
0	22			
	21			
	20			
	19			
	18			
	17		SOLRO	
	16			
	15		SYNO	ATNO
	14		RACKO	TACKO
	13			
	12		SRO	
	11		DAO	
	10		ADRSO	CMDO
	09		DRLO30	DRLO10
	08		DRLO20	DRLO40
	07			DRLO50
	06			DRLO40
	05		DALO30	DALO10
	04		DALO20	DALO40
	03		DALO10	DALO50
	02		DALOOO	DALO40
	01			
	00			

DRAWN BY	APPROVAL			REV.								DWG. NO. (FS6)
L Moses 2/19/70	E.G. White Feb 13, 70	DES.										70B113366
CHECKED Feb. 19, 1970 PC 444		CHKR										CONT ON SHEET 8 SH NO. 7


MULTIPLEXER I/O BUS
DAL000 -070
8
DAL RECIEVERS
DAL000-040
DAL001-071
8
8
ADDRESS DECODER
ADSYO
ADDRESS F.F.
ADRS1
DEL1
ADRSO
CMDO
DAO
SRO
CONTROL
DA1
OCTO
ARM ENABLE F.F.
SCLR
ARM REG
MASK REG
Page 2
Page 3
3
SYNO
SYN
8
ATSYN
ATNO
RACKO
TACKO
ATN / PACK
8
8
ATN F.F.
8
8
EXTERNAL PERIPHERAL DEVICE
DRL020 -070
6
DRL DRIVERS
SCLRO
BLOCK DIAGRAM