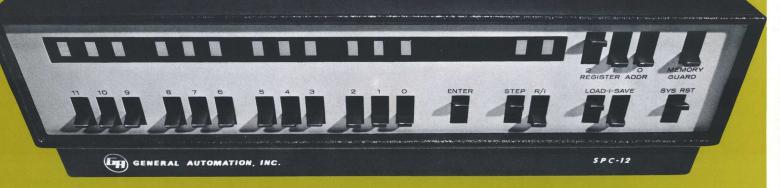
A New Value...
The \$5,000
INDUSTRIAL
COMPUTER



# **SPC-12**

# automation computer



**GENERAL AUTOMATION, INC.**Automation Products Division

## **SPC-12 Processor Features:**

High performance and low cost • Programming simplicity and optimization • Over 15 hardware registers • Over 230,000 instructions per second • Over 450,000 words per second I/O • Adds in less than 6 µsec • Direct memory transfer logic • Power failure detection and automatic restart logic • Memory expansion to 16,384 words.

# **Automation Safety Features:**

Stall alarm (option) • Power fail protection and automatic restart (option) • Console lock • Widetemperature memories • I/O system safe line • 24 v battery operation (option) • Industrial reliability • Wire-free construction.

## **Automation Execution Features:**

Relative time clock • Interrupt system • List processing instruction set • Shared commands • Over 50 basic commands • Three hardware index registers • Four hardware accumulators • Generalized real-time monitors • Functional programs.

## Contents:

Description	1
Organization	2
Addressing	4
Instruction Repertoire	5
Instruction Classes	6
Programmer's Console	8
Software	9
I/O Systems	10
System Interface Units	12
Fail Safe Group	14
Specifications	15
Ordering Information	16



© COPYRIGHT 1968 GENERAL AUTOMATION, INC.

# **Description**



The SPC-12 Automation Computer is a new kind of digital computer—designed to work with and on the same level as the industrial machinery, mechanisms, process instrumentation, communication networks, and data equipment it controls. Its product scope includes the SPC-12 computer, system interfacing units, control software, and automation technology services. In combination they make possible complete industrial computer subsystems for automation projects which offer significant advantages in technology, price/performance, reliability, and maintainability.

The SPC-12 is powerful. It can execute stored programs in excess of 230,000 instructions per second, and can input or output data in excess of 460,000 words per second. Its instruction repertoire minimizes core-memory storage requirements while processing real-time control programs efficiently. The processor is optimized for real-time control processing, having registers than can be used as accumulators or index registers, a list processing command set, and General Automation's exclusive "shared command" technique to give memory up to 50% greater utility. Control function facilities are standard-relativetime clock, external priority interrupt, parallel I/O bus, and serial I/O channel. The standard computer includes a 4,096 by 8-bit word memory (expandable to 16,384 words) with a full cycle time of 2.16 µsec. It provides a parallel adder—six addressing modes—eight 12-bit hardware registers, including an accumulator, an index, and two index/accumulator registers - 50 basic commands - a priority interrupt system — a relative-time clock — a console lock and a teletypewriter interface.

The SPC-12 is easily interfaced. More than 30 system interface units allow multiple functions and technologies to be integrated into one SPC-12 system, minimizing hardware and service costs. The units interface the SPC-12 with communication networks, instru-

ments, mechanisms, devices, sensors, computer peripheral devices, displays, and keyboards.

The SPC-12 is easily programmed. Two levels of software are available with the SPC-12—programming aids and generalized real-time monitors. The programming aids—subroutine library, hardware tests, basic utility system, conversational assembly system, etc.—are designed to minimize the elapsed time required to prepare functional programs. The real-time monitors, designed for application in communication, instruments, mechanisms, and devices, can be applied requiring only programming of the unique functions of a specific application.

The SPC-12 is reliable. The SPC-12 provides exceptional margins for speed, temperature, power, and noise to operate dependably in an industrial environment. Construction is aimed at industrial reliability, using integrated circuits, wire-free assembly, wide temperature (Lithium) memories, 100% environmental testing, and factory burn-in before shipment. Typical memory signal-to-noise margins are over 100% greater than normal industry practice.

The SPC-12 is versatile. With its one-package enclosure, which contains an integral power supply and cooling system, the SPC-12 offers great versatility in application, such as: place stored intelligence into industrial machinery; collect and process data in hospitals and medical laboratories; concentrate, store, forward, switch, and separate data in communication systems; receive and generate data in display systems; count and control traffic; automate production and testing processes; and scan, log, and alarm data in process control.

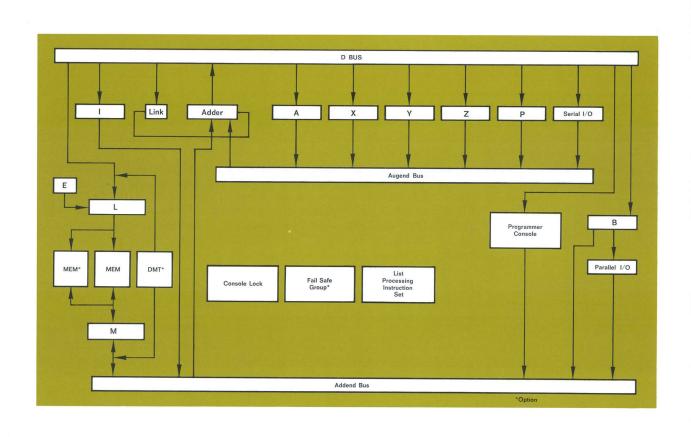
The SPC-12 offers you an automation computer subsystem that will do more work at less cost than any other computer or special-purpose hardware subsystem available today.

# **Organization**

The dual-purpose registers and common bus organization of the SPC-12 are designed to process real-time control data efficiently and easily. The 12-bit organization efficiently processes data for direct, indirect, and indexed addressing to 4,096 words of memory, and is

equally effective with 8-bit byte data. Thus, when generating addresses, the SPC-12 functions as a 12-bit parallel processor. When processing data, the SPC-12 operates as an 8-bit parallel processor.

UNIT	DESCRIPTION	FUNCTION		
L	Memory Location Register 12 Bit	Contains the address of data or instruction being addressed in memory.		
М	Memory Data Register 8 Bit	Contains the data or instruction fetched or stored in memory.		
Ι.,	Instruction Register 12 Bit	Contains the instruction being executed.		
Adder	Parallel Adder 12 Bit Programmable	Parallel, twos complement, binary adder. Adds 12 bits for addressing, adds 8 bits for processing.		
Α	Accumulator 12 Bit Programmable	Holds the results of arithmetic and logical operations. Can be used as a 12-bit accumulator for address generation or 8-bit accumulator for arithmetic or information processing.		
Х	Index Register/Accumulator 12 Bit Programmable	Holds 12-bit address index. When an instruction is tagged, the contents are automatically added to address field to form effective operand address. Also can function same as A register		
Υ	Index Register/Accumulator 12 Bit Programmable	Holds 12-bit address index. When an instruction is tagged, the contents are automatically added to address field to form effective operand address. Also can function same as A register		
Z	Index Register/Accumulator 12 Bit Programmable	Hold 12-bit address index. When an instruction is tagged, the contents are automatically added to the address field of instruction to form effective operand address. Also can function same as A register.		
Р	Program Counter Register 12 Bit Programmable	Holds address of the instruction being executed. Automatically incremented during instruction execution. Also, can be programmed with register, skip, arithmetic, or jump instructions		
В	Buffer Register 12 Bit Programmable	Buffer register for processor. Buffers I/O information, memory transfers, operands to adder.		
Link	Link Register 1 Bit Programmable	Holds carry from arithmetic operations and bit O from shift operations. Used with logical or with multiple precision arithmetic operations. Can be tested, set, reset.		
Е	Extend Memory Register 3 Bit Programmable	Memory addressing control for SPC-12s with memory capacity greater than 4,096 words.		
ВВ	High Order 4 Bits of B 4 Bit Programmable	Addressable to transfer high order 4 bits to low order 4 bits.		
YY	High Order 4 Bits of Y 4 Bit Programmable	Addressable as a 4 bit register and/or accumulator.		
ZZ	High Order 4 Bits of Z 4 Bit Programmable	Addressable as a 4 bit register and/or accumulator.		



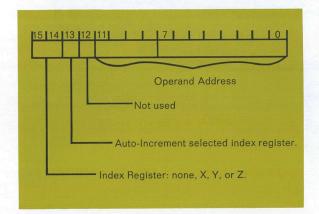


# Addressing

The 12-bit processor organization of the SPC-12 overcomes the addressing complexity and handicap of 8-bit computers. It permits direct, indexed, and indirect addressing to any location in the 4,096-word memory. The memory extend register permits mode switching for direct, indexed, and indirect addressing to 16,384 words.

**Direct Addressing.** The Load B, Store B, Jump instructions have a 2-byte format. The low-order 12-bit address field will directly address any byte in a 4,096-byte memory. For an SPC-12 with greater than 4,096 words, the memory extend register is set under program control to specify which memory bank is to be addressed.

Indirect Addressing. When indirect addressing is specified, the effective operand address is developed from the indirect address word. The 12-bit operand address may be the effective operand address or may be modified by a selected index register, and then the modified address becomes the effective operand address. The format of the indirect address word is:



**Auto-index Incrementing.** When indirect addressing is used, it is possible to specify indexing in the indirect address word. In addition to being able to index the address field of an indirect address word, it is also possible to automatically increment the contents of the selected index register. Thus, when indexing and incrementing are specified, the selected index register is incremented by I before the forming of the effective operand address.

Indexing. Three hardware index registers are provided in the basic SPC-12 and may be selected for use by those instructions whose address fields may be indexed. When indexing is specified, the contents of the selected index register are added to the address field of the instruction to form the effective operand address.

Indexing may occur before indirect addressing, after indirect addressing, or both before and after indirect addressing. When specified, indexing always occurs prior to the forming of the indirect address and/or the effective operand address.

**Literal Addressing.** Several commands in the SPC-12 instruction repertoire may specify literal addressing. This feature selects as the operand the contents of the memory location immediately following the location of the current instruction.

**Extended Memory Addressing.** Addressing of operands and instructions in a SPC-12 with memory larger than 4,096 words is accomplished by using extended memory addressing. This capability is provided by the E register, which serves to extend the 12-bit register and to enable addressing of up to 16,384 memory locations. Loading of the E register is done under program control.

# **Instruction Repertoire**

Mnemonic		Description	Cycles	
oad B Store		B lumn Class		

STB	m m, X m m, X m	Load B register Load B register, indexed Store B register Store B register, indexed Extend Load B register Jump to m	3 3 3 4 2
-----	-----------------------------	---	-----------------------

## Skip Class

SKS	N	Skip if Link Set	1
SKR	N	Skip if Link Reset	1 1
SKP	N	Skip if Plus	1 1
SKM	N	Skip if Minus	l i
SKZ	N	Skip if Zero	1 1
SKN	N	Skip if Not Zero	l i
SKF	N	Skip if I/O False	1 1
SKT	N	Skip if I/O True	1

 $\begin{array}{l} X = \text{indexed} \\ B = B \text{ Register} \\ r = A, X, Y, Z, P \text{ or B registers} \\ v = \text{literal value} \\ N = 0, 2, 4, \text{ or 6} \\ t = X, Y, Z \\ a = \text{auto-increment index tag} \\ I = \text{indirect address} \end{array}$ 

Mnemonic	Mnemonic Description	
Arithmetic	, Logical Class	
AAD r, B	Add B to r	2

AAD	r, B	Add B to r	2
AAD	r, v	Add v to r	3
ASU	r, B	Subtract B from r	2
ASU	r, v	Subtract v from r	3
ALD	r, v	Load v into r	3
AZE	r	Zero r	2
AND	r, B	Logical AND B with r	2
AND	r, v	Logical AND v with r	3
AOR	r, B	Logical OR B with r	2
AOR	r, v	Logical OR v with r	3
AXR	r. B	Logical Exclusive OR B with r	2
AXR	r. v	Logical Exclusive OR v with r	3

## Register Transfer Class

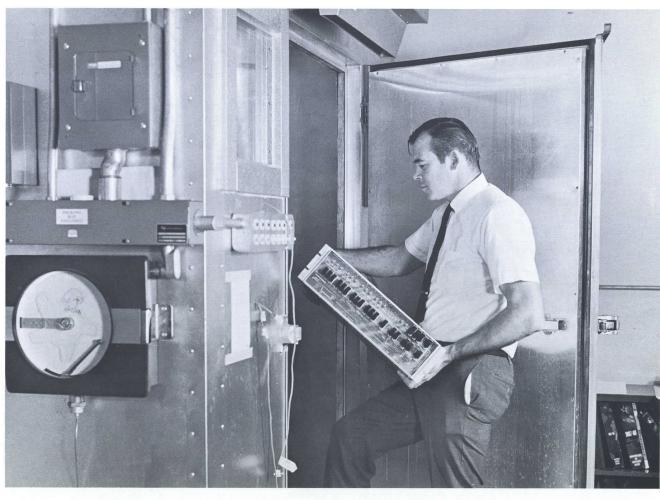
RTR	r, r	Transfer r to r	2
RIC	r, r	Transfer & Increment r to r	2
RDC	r, r	Transfer & Decrement r to r	2
RLK	r, r	Transfer & Add Link, r to r	2

Mnemonic		Description		Cycles	
Control.	Shift.	1/0	Class		

PLR		Pulse Link Reset	2
PLS		Pulse Link Set	2
TBB		Transfer BB to B	2
TBE		Transfer B to E register	2
SHR	r	Shift Right r	2
SHC	r	Shift Circular r	2
SHL	r	Shift Circular Link r	2
SHI	r	Shift Serial In r	2
SHRO	r	Shift Right & Serial Out r	2
SHCO	r	Shift Circular & Serial	2
00		Out r	_
SHLO	r	Shift Circular Link &	2
		Serial Out r	
SHIO	r	Shift Serial In & Out r	2
FOB		Function Out from B	2 2
		register	
DOB		Data Out from B register	2
DIB		Data In to B register	2
INE		Interrupt Enable	3

## **Augmented Memory Addressing Class**

GNL r, t, I GNA r, t, I GNS r, t, I	Load r Add to r Store from r	3 3
GNZ r, t, I	Store from r Store and clear r Indirect address word	3 (+2)



## Instruction Classes

The SPC-12 instruction repertoire has six classes of instruction. These six classes are:

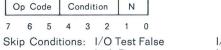
#### LOAD B, STORE B, JUMP CLASS

This class contains the four basic instructions of **Load B** from memory, **Store B** in memory, **Load B** extended (12 bits of data), and **Jump Unconditionally.** Each of these instructions provides direct addressing to 4,096 locations.



#### SKIP CLASS

This class contains one basic instruction which can be coded to skip 0, 2, 4, 6 locations when the coded **Condition** is satisfied.

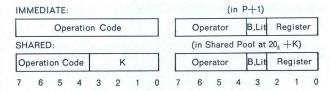


nditions: I/O Test False I/O Test True
Link Reset Link Set
Adder Result Non Zero Adder Result Zero
Adder Result Minus Adder Result Plus

#### ARITHMETIC, LOGICAL CLASS

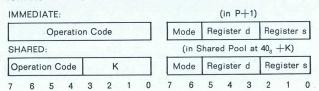
The Arithmetic, Logical Class contains instructions to **Load**, **Clear**, **Add**, **Subtract**, **OR**, **AND**, or **Exclusive OR** the A, X, Y, Z, or P registers with B or a literal addressed operand.

A Class instructions have 2 bytes, where the second byte can be stored in P+1 or in a shared pool of 16 locations, starting at location  $20_8$  +K. The common pool is termed "Shared," since other A Class instructions can address and execute the same second byte. The term "Immediate" signifies that the second byte of the instruction is dedicated and will be fetched from location P+1. The formats for A Class instructions are:



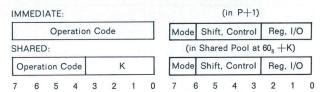
#### REGISTER TRANSFER CLASS

This class contains four basic instructions which can be coded to transfer a source register (s) to a destination register (d). The transfer can be coded to **Add Link, Increment, Decrement,** or **Not Change** the quantity transferred. R Class instructions have 2 bytes, where the second byte can be stored in P+1 or in a shared pool of 16 locations, starting at  $40_8$  +K. The formats for R Class instructions are:



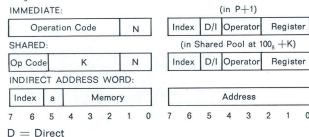
### CONTROL, SHIFT, I/O CLASS

This class contains Shift, Set/Reset Link, Transfer BB to B, Serial input/output, Parallel input/output, Transfer B to Memory Extend Register, and Interrupt control instructions. P Class instructions have 2 bytes, where the second byte can be stored in P+1 or in a shared pool of 16 locations, starting at  $60_8$  +K. The formats for P Class instructions are:



#### LIST PROCESSING INSTRUCTIONS, AUGMENTED MEMORY ADDRESSING CLASS

This class contains four basic instructions for **Storing and Clearing** registers, **Storing** registers, **Loading** registers, and **Adding from memory** to registers. The G Class can specify indexing by X, Y, or Z and indirect addressing. G Class instructions have 2 bytes, where the second byte can be stored in P+1 or in a shared pool of 16 locations, starting at  $100_8$  +K. The formats for G Class instructions are:



I = Indirect
a = Auto-increment

The power of a G-Class instruction is illustrated with the following example.

One 8-bit byte of in-line coding can perform these seven dimensions of operand addressing.

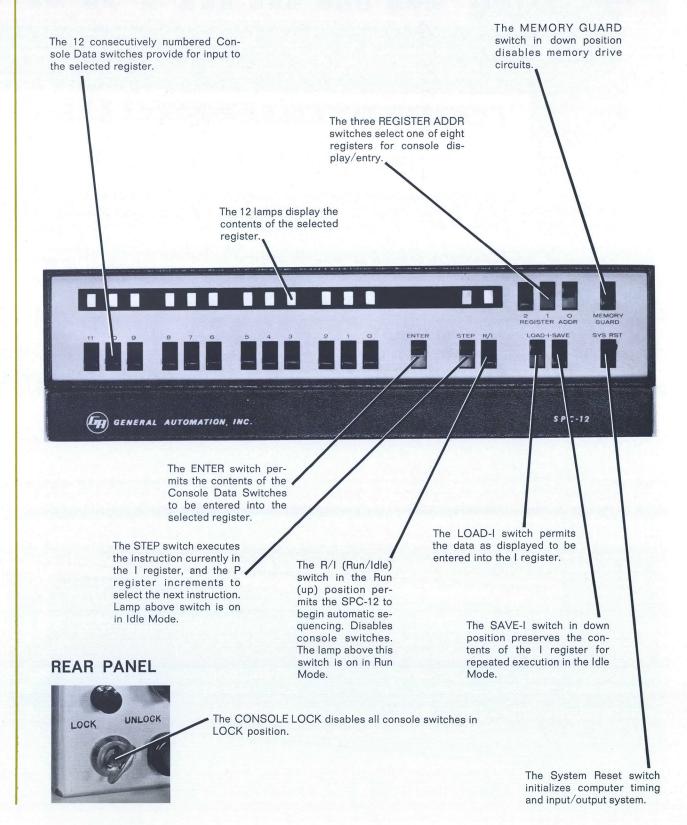
Operation	N	Register	Index	Indirect	Index	Auto
Clear	6	PΖ	Z		Z	Z+1
Add	4					
Store	2	ВΥ	Υ		Υ	Y+1
Load	0	AX	X	<b>A</b>	X	X+1

Operation N Register Index Indirect Index Auto
Code Increment
Index



# **Programmer's Console**

The Programmer's Console is operable only when the SPC-12 is in the  $\bf Idle\ Mode\ (R/I\ switch\ down\ and\ Console\ Lock\ in\ UNLOCK\ position).$ 



## Software

Standard program systems provided with the computer comprise the Conversational Assembly System, the Basic Utility System, and a subroutine library.

Conversational Assembly System. The Conversational Assembly System is a symbolic assembly program that minimizes the time required for assembling a program. It permits the programmer to recover from errors on-line without having to restart the assembly process. With this system the programmer can insert corrections from the keyboard during assembly. The assembler also provides the programmer with a means of entering linkage, mapping, and common data. With this system, instructions, data, memory addresses, and address modifiers can be coded and entered in symbolic notation.

The assembler provides 11 pseudo-operation codes. A single pass of the input source program is sufficient to completely assemble the program.

Basic Utility System. The Basic Utility System enables the programmer to trace through his program to correct errors, to enter and execute test cases, and verify results. The system operates on-line with a teletypewriter. Data can be input, instructions can be changed, and small programs can be executed using the keyboard for input.

Subroutine Library. The Subroutine Library includes a package of often-used utility programs, I/O programs, mathematical subroutines, and a hardware maintenance and verification subsystem. The utility package contains routines for loading, punching, and listing programs, as well as aids for debugging and updating programs. I/O routines are available for such peripheral equipment as the Teletype Model 33 or 35, Send/Receive sets, standard communication modem interfaces, discrete digital inputs and outputs, contact closure and sensing units, analog-to-digital and digital-to-analog conversion subsystems, and other standard peripheral devices.

Also provided is a library of mathematical subroutines which include multiple precision fixedpoint addition, subtraction, multiplication, and division routines.

**Supplemental Software.** In addition to the standard software package, total solutions or services in software applications are available to SPC-12 users from the process analysis programming staff of the Automation Sciences Division of General Automation, Inc. A substantial library of real-time monitors, executive control systems, process control functional programs, utility routines, and I/O drivers are operational and maintained for application to SPC-12 user projects.



# I/O Systems

## Parallel I/O System

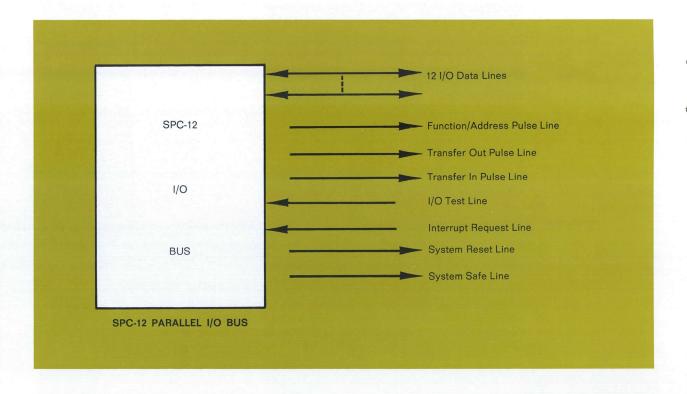
The parallel input/output system of the SPC-12 minimizes the need for external hardware. Three instructions of the SPC-12 provide a maximum amount of control of the I/O System without sacrifice of speed or efficiency. These three instructions address the device and the data transfers:

output function/address from B register, input data to the B register, and output data from the B register.

Execution of an I/O program does not interfere with information being processed in the accumulators. All data and address transfers take place through the B register, a 12-bit buffer register. The arithmetic characteristics of the I/O data can be tested prior to storage or further manipulation.

The parallel I/O system provides flexibility through a single set of data and control lines to interface readily to a wide variety of external equipments simultaneously. The 12-bit data bus of the I/O permits efficient handling of 8, 12, 16, and 24-bit data transfers. The design permits extended use of a data channel in that an I/O channel can be separated into an input channel and an output channel to operate two uni-direction devices.

The SPC-12 never needs modification for adding new peripherals or interfaces; such expansions can be achieved in the field. New devices are added by simply connecting the I/O bus from the last to the new device.



## Parallel Input/Output Specifications

PARAMETER	SPECIFICATION		
Signal Levels	Data $\pm 5$ volts $=$ ''1'', 0 volts $=$ ''0''		
	Control $\pm 5$ volts $=$ ''0'', 0 volts $=$ ''1''		
Noise Immunity	+5 volts levels		
	Line current (for termination and load)—125 ma @ 0° C		
	Twisted-pair cable		
	Wide margin timing		
Expansion	I/O Bus Drive Current—Data Lines = 105 ma @ 0° C		
	—Control Lines = 70 ma @ 0° C		
Timing	Output function/address from B register $=$ 4.32 $\mu$ sec.		
	Output data from B register $=$ 4.32 $\mu$ sec.		
	Input data to B register $=$ 4.32 $\mu$ sec.		

## Serial I/O System

The serial input/output system is a unique data transfer channel that permits the input and output of serial data. Operation of the serial I/O is independent of the parallel I/O system.

The serial I/O bus is a 3-wire, full duplex, 48 vdc, 20 ma, telegraph grade line. Typically connected to a Teletype ASR 33 or 35, it permits operation up to 2000 feet away. Two instructions of the SPC-12 provide complete control of the serial I/O system:

input serial data to the A, X, Y, or Z register, and output serial data from the A, X, Y, or Z register.

### Interrupt System

This system provides the ability to interrupt program sequencing to service requests from: external equipment, automatic restart, and the relative-time clock. The external equipment interrupts are serviced over the interrupt request line of the parallel I/O system. The interrupt request line can service numerous external devices where the service priorities are established under program control. Interrupt priorities can also be established by hardware by

adding interrupt expander units. Each unit provides the ability to service eight interrupt lines, with priority determination, address generation and arm/disarm facilities for each level. When an interrupt is acknowledged, the contents of the program counter are saved, and program control is transferred to a unique and dedicated location.

### **Direct Memory Transfer**

The SPC-12 has a plug-in expansion provision for the hardware direct memory transfer channel option. The DMT provides for input/output rates in excess of 460,000 bytes per second under hardware control The DMT addressing control is fully buffered so that sequential block transfers can occur without a "setup" interval occurring between transfers. External devices can control the interleave and burst mode, direction of transfer, and activation of transfer. In the interleave mode, transfers can occur at any rate up to 100,000 bytes per second. Each transfer takes only one memory cycle from the SPC-12. Rates between 100,000 and 460,000 bytes per second can be provided in the burst mode. The processor is stalled during the burst mode.

# **System Interface Units**

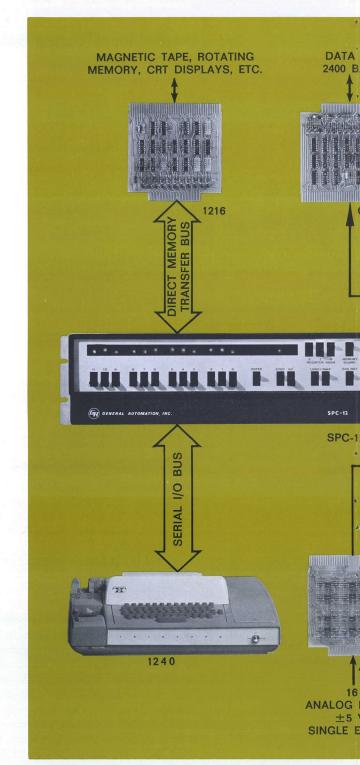
SPC-12s are designed to combine multiple technologies into one computer subsystem economically and easily. This is accomplished with a completely new family of interface and controller system units.

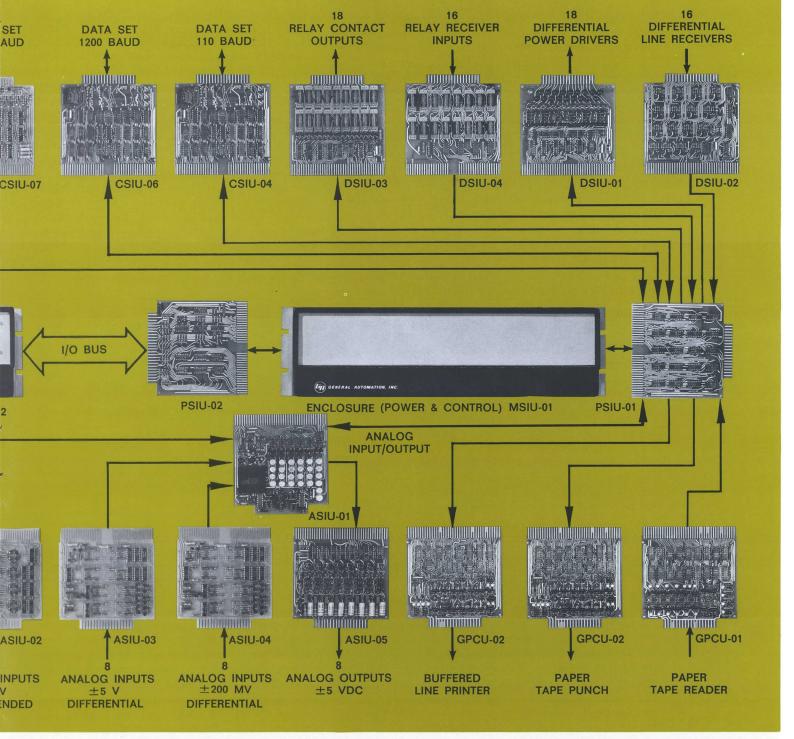
The family consists of more than 30 units for interfacing and controlling: communication data sets; instruments; sensors; computer peripherals; mechanisms and devices; and displays and keyboards. The family has been designed complete with a common enclosure, power, cooling unit, and ease of interconnection.

Each system interface unit is a functional entity which eliminates redundant and excessive electronics. The functional approach automatically provides a new level of ease for system configuring, servicing, field expansions, and module economy. The common enclosure houses up to 21 system interface units.

An optional SPC-12 internal mounting assembly which accommodates up to nine system interface units can be used in those applications where the SPC-12 will not require more than 4,096 words of memory.

System interface units preserve the SPC-12 high performance-versus-cost advantages and provide a new ease of implementing a system.





# Fail Safe Group

In addition to the reliability designed and manufactured into the SPC-12, three additional safeguards are offered to assure total system fail-safe operation. These fail-safe provisions protect the computer system from the costly consequences usually associated with power interruptions, power transients, component breakdown, programming bugs, or system shutdown. The fail safe group gives ultimate protection to operations and processes without the need for human surveillance.

## **Power Failure Detection and Automatic**

Restart. The Power Failure Detection logic monitors the input power (ac or dc) and causes an automatic and orderly shutdown if power fails. When power returns to normal, the detection logic initiates the Automatic Restart sequence, which delays to allow for system settling, generates a system reset signal, and then places the SPC-12 into Run mode at a unique and dedicated location. When a power failure has caused an interruption of normal operations, a signal is generated on the system safe line of the parallel I/O system which can be used for an audio/visual alarm and/or automatic switchover

**Stall Alarm.** While the Stall Alarm warns of any abnormality in system operation, it is particularly valuable in the event of improper program sequencing due to component breakdown or previously undetected program bugs. It provides an orderly halt to instruction execution and generates a signal through the system safe line of the parallel I/O system which can be used for audio/visual alarm and/or automatic switchover. A unique instruction is provided with the stall alarm to both arm the alarm and to maintain it in a reset condition during normal operation. The instruction is executed normally at intervals less than 250 ms. Any longer interval will actuate the alarm sequence.

Battery Power. Where it is desirable to maintain system operation independent of the fluctuations or availability of common ac power, the Battery Power adapter permits operation from a dc source such as a battery. Battery power would normally be maintained at peak output capability by a charger operating from the ac source. Should the ac source fail.

the fully charged battery would permit continued operation for a number of hours.

## Reliability

SPC's are designed to work around the clock in unattended operation. Every SPC-12 is manufactured to produce the highest level of reliability. The design follows stringent worse case criteria. The computer has no processor wires and has fewer components, fewer connectors, and dissipates less power than any other full-scale general purpose digital computer commercially offered. Before an SPC-12 is assembled, all components and subsystems are subjected to 100% testing and inspection.

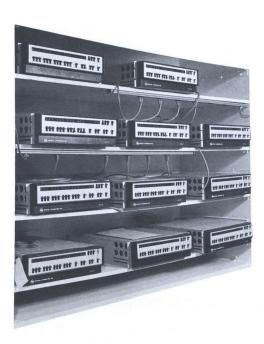
Each SPC-12 is successfully operated in an environmental test chamber, followed by a burn-in period prior to shipment. This exhaustive testing eliminates defective components which have infant mortality tendencies. SPC-12s plug in, work, and keep working.



### **Maintainability**

SPC-12 design constitutes a breakthrough in maintainability. The computer contains only three printed circuit boards: master interconnect, memory, and processor. Any one of these boards can be replaced by a service person without computer maintenance training within five minutes. Test and verify programs indicate which, if any, of the three is not functioning. All parts are completely interchangeable; even memory stacks with loaded programs can be interchanged. The SPC-12 is the least likely element in an electronic processing or control system to fail. It does not add, but rather eliminates, expensive service costs.

# Specifications:



#### TYPE

A digital, automation computer. Single address, parallel processor.

#### **MEMORY**

Random access. Wide temperature ferrite magnetic core memory storage. 4,096 8-bit bytes (expandable to 16,384 bytes). Memory cycle time of 2.16  $\mu$ sec; access time, 600 nsec.

#### **ADDRESSING**

Six modes. Direct addressing to 4,096 bytes. Literal addressing. Indexing. Indirect. Auto Index incrementing. Extended addressing.

#### ARITHMETIC

Parallel. Binary, fixed point, twos complement.

#### **INSTRUCTIONS**

Single and double word instructions. 50 basic instructions within six classes: Load B, Store B, Jump; Skip; Arithmetic, Logical; Register Transfer; Control, Shift, I/O; List Processing Instruction Set.

#### SPEED

Instruction Execute Times

Add/subtract registers	$4.32~\mu sec$
Load/store from/to memory	6.48 μsec
Add/subtract memory	6.48 μsec
Input I/O bus to B register	$4.32~\mu sec$
Output B register to I/O bus	4.32 μsec

#### INPUT/OUTPUT

12-bit parallel I/O bus. Serial I/O bus. Automatic priority interrupt, relative-time clock; optional fail safe group and direct memory transfer.

#### PANEL

Programmer's console. Includes 12 data switches and indicators. Register selection switches. Six control switches. Console lock.

#### **SOFTWARE**

Software includes: conversational assembly system, basic utility system, subroutine library, hardware test and verify programs, and optional generalized real-time monitors and applied programming services.

#### OPTIONS

Expansion to 16K memory. Read-only memory. Fail safe group, with power fail detection, automatic restart, and stall alarm. Direct memory transfer channel and control unit. Priority interrupt expander unit. Over thirty system interface units. Mounting hardware. Battery power adapter (24 vdc input). Teletypewriter. Peripheral equipment. Real-time monitors. Application, programming and engineering services. Hardware optimization engineering for minimum recurring cost systems.

**DIMENSIONS**, including power supply and cooling Height 51/4 inches. Width 171/2 inches. Depth 20 inches.

**WEIGHT,** including power supply and cooling 29 lbs.

TEMPERATURE, Operable

0 to 50° C.

**HUMIDITY**, Operable

90% relative.

#### **POWER**

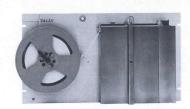
115 volts ac  $\,\pm\,10\%.$  Single phase. Frequency of 47 to 63 hz. 24 vdc power supply optional.

#### INSTALLATION

One piece packaging includes enclosure, power supply and cooling, permitting table top or standard 19" rack mounting.

# **Ordering Information**







8 channels, output analog storage,  $\pm 5 \rm v,$  decay rate = 2 mv/sec @ 25° C.

		PROCES UNITS —	SOR SYSTEM INTERFACE PSIU
Model Number	Description	Model Number	Description
1200	SPC-12 Stored Program Controller, 4096 words of core memory, three (3) hardware index registers, control panel, real-time clock, priority interrupt control with interrupt line, and serial data transmission interface for telephone and Teletype (ASR-33/-35/-37) communication; includes enclosure, cooling unit and power supply, 0 to 50°C	PSIU-01	Function Interface Translator (FIT); includes 8 sense lines, 8 input channel selects, 8 output channel selects, 8 control pulses, interrupt arm/disarm.
		PSIU-02	I/O Cable Interface Translator (CIT); twelve data driver/receiver pairs and termination registors for all data and control lines.
1201	First additional 4096 words of core memory, 0 to 50 $^{\circ}$ C	PSIU-03	Priority interrupt expander unit, contains eight priority interrupt lines with address generation, line receivers, and arm/disarm for each level.
1202	Second additional 4096 words of core memory; requires Model 1290 memory enclosure, cooling unit and power supply, 0 to 50° C	DIGITAL SYSTEM INTERFACE UNITS – DSIU	
1000	Third additional 4000 areads of some manner of	DSIU-01	
1203	Third additional 4096 words of core memory, 0 to 50° C	DSI0-01	Eighteen (18) buffered, differential power drivers 40v, 125 ma.
1210	Power Failure Detection and Automatic Restart Feature	DSIU-02	Sixteen (16) differential line receivers, 24v max with selectable threshold and filtering.
1212	Stall Alarm	DSIU-03	Eighteen (18) buffered form A contact outputs, 12 va max, (24 vdc, 0.2 amp).
1216	First Direct Memory Transfer (DMT) Control Unit and Input/Output Channel; includes memory address register, block length register and comparator	DSIU-04	Sixteen (16) relay receiver inputs, 1000 ohms $\pm20\%,8$ to 20 vdc input voltage.
1240	Model 33 Automatic Send Receive (ASR-33)		
1242	Model 35 Automatic Send Receive (ASR-35)	ANALOG SYSTEM INTERFACE UNITS — ASIU	
1290	Memory enclosure, cooling unit and power supply	ASIU-01	Analog input/output unit, 11 bit plus sign, $\pm 5 \rm v$ ADC/DAC, 3 $\mu \rm s/bit$ conversion rate.
1292	Battery power adapter (24 vdc input)	ASIU-02	16 channels, single ended input analog multiplexer, $\pm 5 \mathrm{v}.$
1299	Teletype Modification Kit; hardware and instruc- tions for modifying the ASR-33 for full duplex operation	ASIU-03	8 channels, differential input analog multiplexer, $\pm 5 \text{v}$ , 2v common mode voltage.
		ASIU-04	8 channels, differential input analog multiplexer, $\pm200$ mv, 2v common mode voltage.

ASIU-05





Model Number



Description

# COMMUNICATION SYSTEM INTERFACE UNITS

Description

Model Number

CSIU-01	Controller for Teletype Models 33, 35, and 37, Automatic Send/Receive Set (ASR-33/-35/-37) or Keyboard Send/Receive Set (KSR-33/-35/-37); half duplex operation; includes character buffer and serial-to-parallel/parallel-to-serial converter.  RFL Tone Unit Interface (1800 bits/second); half duplex operation; includes character buffer and	CSIU-07H CSIU-07F	Bell System Model 201B2 Data Set Controller; half duplex operation; includes character buffer and serial-to-parallel/parallel-to-serial converter. Bell System Model 201B2 Data Set Controller; full duplex operation; includes character buffer and serial-to-parallel/parallel-to-serial converter.
CSIU-03H	serial-to-parallel/parallel-to-serial converter.  Bell System Model 103A2 Data Set Controller; half duplex operation; includes character buffer	GENERAL UNITS — (	IZED PERIPHERAL CONTROLLER GPCU
CSIU-03F	and serial-to-parallel/parallel-to-serial converter.  Bell System Model 103A2 Data Set Controller; full duplex operation; includes character buffer and serial-to-parallel/parallel-to-serial converter.	GPCU-01	Generalized buffer input controller (GBIC) 8-bit data buffer, 12 line receivers, 4 pulse generators, 4 buffered line drivers, 2 data exchange FF1s, parity check.
CSIU-04H	Bell System Model 103A2 Data Set Controller and Model 801 Automatic Calling Unit (ACU) Controller; half duplex operation; includes char- acter buffer and serial-to-parallel/parallel-to-	GPCU-02	Generalized buffer output controller (GBOC) 12-bit data buffer, 12 line drivers 4-line receivers, 4 pulse generators, 2 data exchange FF's, parity generator.
CSIU-04F	Bell System Model 103A2 Data Set Controller and Model 801 Automatic Calling Unit (ACU)	GPCU-03	Generalized buffer input/output controller (GBIO) 8-bit data buffer with line drivers, 4-bit data buffer with line receivers, 4 line receivers.
	Controller; full duplex operation; includes character buffer and serial-to-parallel/parallel-to-serial converter.	GPCU-04	Generalized mag tape controller (GMTC).
CSIU-05H	Bell System Model 202C2 Data Set Controller; half duplex operation and supervisory channel control; includes character buffer and serial-to-parallel/parallel-to-serial converter.	GPCU-05	Generalized disc memory controller (GDMC).  ANEOUS SYSTEM UNITS
CSIU-05F	Bell System Model 202C2 Data Set Controller; full duplex operation; includes character buffer and serial-to-parallel/parallel-to-serial converter.	MSIU-01	Option enclosure, power supply, cooling unit, and mounting for 21 interface units.
CSIU-06H	Bell System Model 202C2 Data Set Controller and Model 801 Automatic Calling Unit (ACU) Controller; half duplex operation and supervis- ory channel control; includes character buffer	MSIU-02 MSIU-03	Option enclosure, cooling unit, power supply, 1 Model PSIU-01 and 1 Model PSIU-02.  Internal mounting assembly mounting for up to 9 interface units, limited to 4K memory proc-
CSIU-06F	and serial-to-parallel/parallel-to-serial converter.  Bell System Model 202C2 Data Set Controller	MSIU-04	essors.  Universal interface unit (provision for mounting
	and Model 801 Automatic Calling Unit (ACU) Controller; full duplex operation; includes character buffer and serial-to-parallel/parallel-to-serial converter.	MSIU-05	and wiring up to 20 IC's). Unit extender.

# **General Automation Technology**

The SPC-12 is a General Automation, Inc. total product line. This complete line comprises the computer, computer options, system interface units, peripheral controllers, peripherals, programming aids, and automation technology services. Automation technology services include application analysis, applied programming, development engineering, product optimization, and systems engineering. Any combination of these products and services can be selected and applied to accomplish a computer based automation project.

