SW10 MAINTENANCE MANUAL

General Terminal Corporation

SW10
MAINTENANCE
MANUAL

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The following related documents are available from GTC:

SW10 Users Manual	PN 970004-001
SW10 Reference Card	PN 970008-001
TV Monitor Manual	PN 05018-001

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SW10 TERMINAL

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1.0 INTRODUCTION

This manual is intended to be used by service personnel who must perform diagnostic tests on and repair of the SW10 terminal. It is assumed that the technician is familiar with basic data communication techniques and normal SW10 terminal operation. The following manuals should be consulted is conjunction with this manual:

SW10 USERS MANUAL	970004-001
TV MONITOR MANUAL	05018-001

Only the domestic model of the SW10 is discussed in this manual. Differences between the domestic and international power supplys are shown on schematic 720019 sheet 2.

1.1 GENERAL DESCRIPTION

The SW10 is a microprocessor (Z8) based terminal with a detached ANSI keyboard. The operating parameters may be modified by the operator during SETUP mode.

The terminal allows the operator to serially transmit data to or receive data from a remote host CPU. The information is passed over a full duplex channel at selectable baud rates up to a maximum of 9600bps.

The 12 inch (diagonal) screen is arranged in an 80 column and 24 row format plus a 25th status line. Each character is displayed as a 5x7 dot matrix on a 7x10 field. A non-interlaced (overlap) scan method is used to refresh each frame at a 60Hz (or 50Hz) rate.

Interfacing is thru a main port and a printer port. Both are rear panel RS-232C connectors. The printer port is a gated port which, if desired, allows data received from the main port to be passed thru the printer port without being displayed on the screen.

The terminal operating parameters are changed from the keyboard. There are no physical switches. Figure 1-1 lists the changeable parameters. The underline condition is the state selected at time of manufacture.

PHYSICAL CHARACTERISTICS

	DISPLAY	KEYBOARD
HEIGHT	11.5" (29cm)	2.5" (6.4cm)
WIDTH	13" (33cm)	17" (41cm)
DEPTH	12" (30cm)	8" (20cm)
WEIGHT	22 lbs(10kg)	4 lbs(1.8kg)

VOLTAGE/FREQ 105-135 Vac 50/60Hz 61 Watts
TEMPERATURE (C) 5 to 40 Oper/-30 to 65 Stor
HUMIDITY 5% to 80% non-condensing

DISPLAY CHARACTERISTICS

SCREEN SIZE	12" Diagonal
VIEWING AREA	8.25" x 6.25"
SCREEN CAPACITY	1920 Characters
DISPLAY MATRIX	80 x 24 + Status
SCREEN PHOSPHOR	P31(Grn) or P4(Wht)
CHARACTER SET	128 ASCII
CHARACTER MATRIX	5x7 on 7x10 field
CURSOR	Reverse Video Block

MAIN PORT INTERFACE

RS-232C Asynchronous
Selectable XON/XOFF
50 - 9600 Baud Full Duplex
Space/Mark/Even/Odd Parity

PRINTER PORT INTERFACE

RS-232C Asynchronous
Screen Print
Printer Controller Mode
Handles PRINTER BUSY

SETUP MODE PARAMETERS

#01>	MODE	ONLINE/LOCAL
#02>	BAUD	50 THRU 9600
#03>	PARITY	SPACE/MARK/EVEN/ODD
#04>	MODE	VT100/VT52/PROGRAM
#05>	AUTO NEW LINE	ON/OFF
#06>	AUTO WRAP	ON/OFF
#07>	LINE END	STD/DEC
#08>	CURSOR BLINK	ON/OFF
#09>	CAPS LOCK	ON/OFF
#10>	MARGIN BELL	ON/OFF
#11>	SHIFT 3	#/ENGLISH POUND
#12>	POWER FREQUENCY	50/60 HERTZ
#13>	PRINTER BUSY	LOW/HIGH
#14>	KEYBOARD	1 / 2
#15>	PASSTHRU	ONLY/DISPLAY
#16>	AUTO REPEAT	ON/OFF
#17>	PROTECTED PRINT	ON/OFF
#18>	AUTO XON	ENABLE/DISABLE
#19>	LOCAL ECHO	ON/OFF
#20>	KEY CLICK	ON/OFF
#21>	SLOW SCROLL	ON/OFF
#22>	REVERSE VIDEO	ON/OFF
#23>	BRIGHTNESS	1 THRU 16 (8)

Figure 1-1 SW10 Specifications

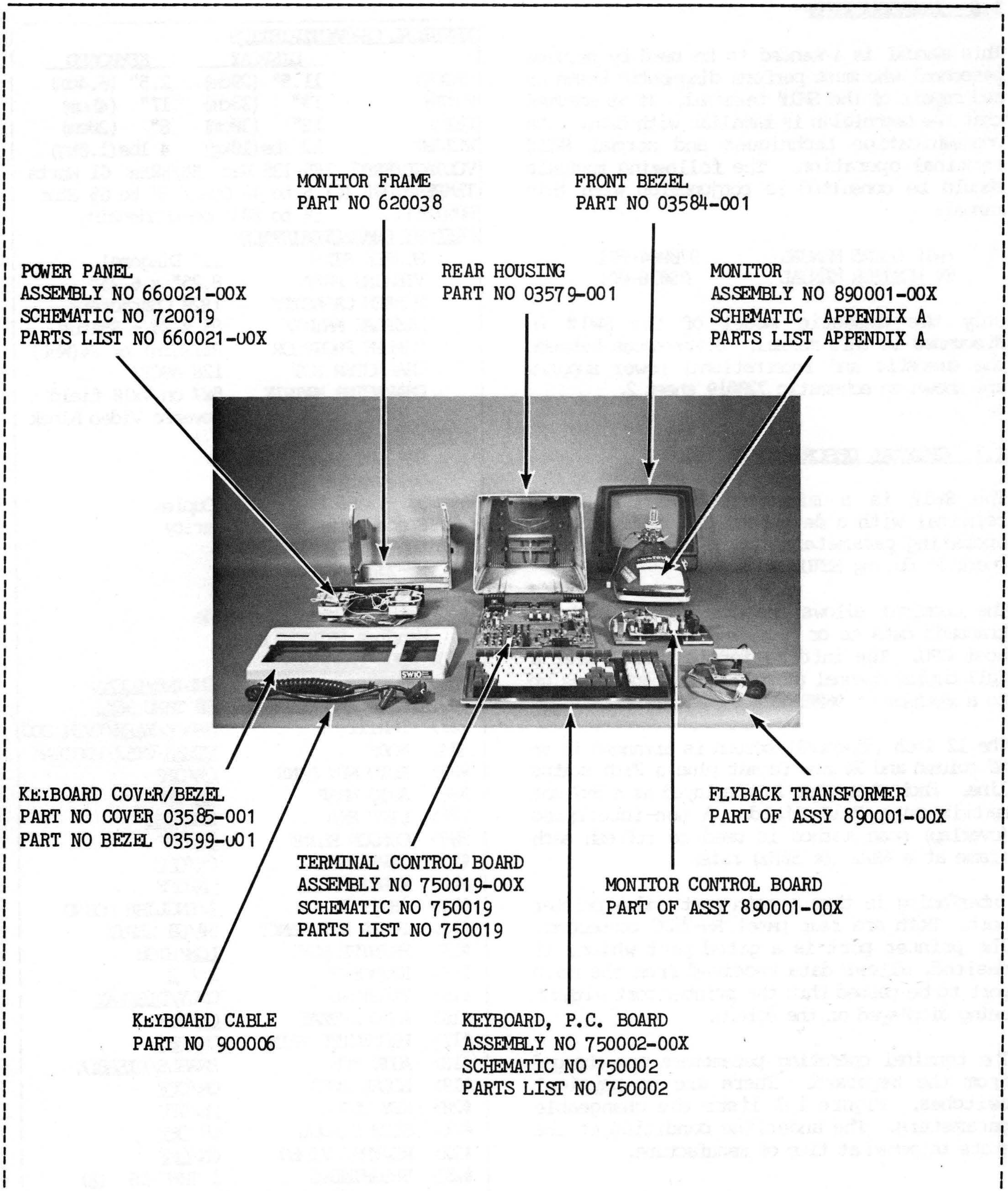


Figure 1-2. Illustrated Parts Breakdown

2.0 TESTING & TEST AIDS

This section describes test procedures that may be used to check the operating condition of the terminal. They may also be used to isolate failures to the terminal, the modem, or the transmission lines.

2.1 POWER-ON AUTOMATIC TESTS

When power is applied the terminal will perform a series of five internal diagnostic test to determine the condition of its ROM, RAM, and NVM circuits. If an error is detected, the testing will stop and an error message will appear on the status line indicating the nature of the problem.

a. ROM TESTS

The ROM contents are read out and a checksum is calculated. This number is compared to a previously stored checksum. If the numbers match, the test is successful.

b. Z8 TEST

A block of ROM is written into the 128 bytes of Z8 RAM. A bit by bit comparison of the ROM and RAM is made.

c. RAM 1 TEST

This test checks the condition of the 2K of display RAM by writing a block of ROM into the RAM and making a bit by bit comparison at each memory location.

d. RAM 2 TEST

This test checks the 1K of scratch pad RAM. A block of ROM is written into the RAM and a bit by bit comparison is made at each memory location.

e. NVM TEST

The NVM (non-volatile memory) is essentially an electrically alterable ROM and is subjected to the same tests as the program ROM. The contents of the NVM is read and a checksum is calculated. This number is compared to a checksum stored in the NVM. If the numbers match, the NVM is successful.

Each time a parameter is changed and saved, a new checksum is calculated and stored.

If an NVM error is detected, a set of default parameters will be entered into the NVM. This allows the operator to trouble-shoot the terminal with a known set of conditions. These default conditions are listed in Section 1.

MESSAGE		MEANING
Error:	ROM	Checksum error
Error:	Z8	Error in 128 bytes of Z8 RAM
Error:	RAM 1	Error in display RAM
Error:	RAM 2	Error in scratch pad RAM
Error:	NVM	Error in non-volatile memory
Error:	Comm	Error in communications interface

Figure 2-1. Status Line Error Messages

2.2 OFF LINE CONFIDENCE TESTS

Place the terminal in the SETUP mode by pressing the <SETUP> key. Next, press the <SHIFT> + <D> keys. This loads the terminal with a known set of operating parameters under which the unit can be tested. These parameters will be displayed on the screen. Exit the SETUP mode by pressing the <SETUP> key again.

Enter the command sequence ESC #8. The screen will be filled with "E"'s. Verify that each display location contains a character. The screen may be cleared by pressing <SHIFT> and <FUNCTION>.

Exercise the terminal from the keyboard using all the upper and lower case keys, all the numbers, and all the special symbols and punctuation marks. Verify that the cursor control keys and the numeric pad keys are operating correctly. Perform carriage return, line feed, tab, etc., operations. Enter data into position 80 of line 24 to test for proper scrolling operation.

The power up test can be started from the keyboard three ways:

1. From the SETUP mode, press <SHIFT><D>.

2. Enter the sequence ESC [2;1y. This will cause the tests to be performed once.

3. Enter the sequence ESC [2;9y. The test will run continuously. However, no beep will sound after the successful completion of each test.

NOTE: The continuous test will terminate only when an error is detected or when power is removed.

2.3 ON LINE INTERFACE TESTS

a. Main Interface Tests

The Main interface may be tested by installing a turn-around plug (shown in Figure 2-2) and invoking the Data Loop-back confidence test. Entering the command sequence ESC [2; 10y initiates the tests. Data is routed out pin 2 and received back in pin 3. The status line will display the message "WAIT", indicating the test is in progress. The test will continue until a failure occurs or power is removed. As described above, a failure will cause an error message to be displayed on the status and the tests will be terminated.

With the connector in place, test all the function and control keys. Test all the commands listed in the Users Manual in Section 3.3. If the data shown on the screen is the same as that being keyed in, the test is considered successful.

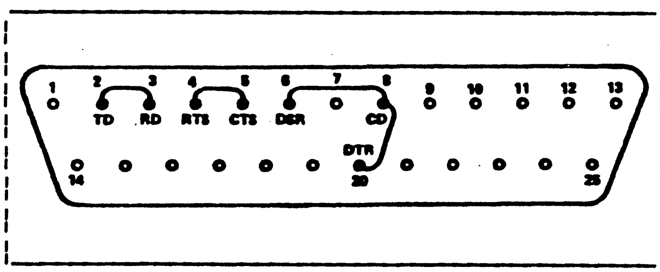


Figure 2-2. Turn Around Plug

b. Printer Interface Tests

If a printer is attached, the printer interface may be tested by typing several lines of characters on the screen in some recognizable pattern. Perform the Print Page operation ESC [0F. Check the printout to verify that the data was printed exactly as it appeared on the screen.

The Print Controller mode may be tested by entering ESC [5F. This enables the Printer and disables data from being displayed on the screen. Next, ask the host to send back some known data. The data should not be displayed on the screen but should be sent directly to the printer. The screen is enabled (and the Print Controller disabled) by entering an ESC X.

2.4 ALTERNATE TWO-WAY TEST

By using a cross-coupled cable, a two-way test can be conducted using a second terminal to simulate the host. Place both terminals on-line and connect the cable between the main ports. Data entered on one keyboard should appear on the screen of the other terminal.

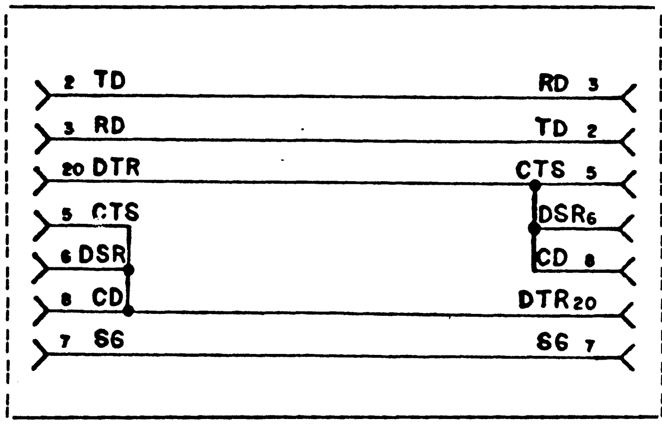


Figure 2-3. Cross Coupler Cable

2.5 FAULT ISOLATION

This section is provided to assist the technician in isolating a terminal problem to one of the major subassemblies, i.e., keyboard, terminal control board, or monitor circuits. Refer to Figure 2-8 for location of the test points.

2.5.1 Keyboard

The keyboard sends KROW signals to the microprocessor circuits in response to KMUX signals. If only a few keys are inoperative the problem could be a bad KMUX, a bad multiplexer, bad keys, or a broken connection. Each KMUX waveform will be different but all

KROW signals will appear the same. The KMUX signals are always present but the KROW signals appear only when a key is pressed. Consult schematic 720002.

Figure 2-8 shows the location of the six power supply test points. These test points check the voltages at the output of their regulators. If the desired voltage levels are not present, refer to the power supply schematic. Trace the voltages back towards the transformer until the problem is located.

2.5.2 Terminal Control Board

When power is first applied, the SW10 performs a series of internal diagnostic tests. These tests check the RAM, ROM, NVM, most of the microprocessor, and a large portion of the VTAC. If a problem is encountered an error message will appear on the status line indicating the nature of the problem.

The video data output of the terminal control board can be viewed at U3-12 (or J3-5). This is a complex signal whose wave shape will be dependent on the key being pressed. Figure 2-8 shows a typical wave form. If the video data signal at U3-12 is present but the data is not being displayed on the screen, the monitor is probably at fault. Refer to the TV Monitor Manual (GTC# 05018-001) for a detailed theory of operation and other information regarding operation of the monitor circuits.

```
Transmitted Data (TD)......<—..................................
Received Data (RD).........—>..............................   :
Request To Send (RTS)......<—...........................   :  :
Clear To Send (CTS)........—>........................   :  :  :
Data Set Ready (DSR).......—>.....................   :  :  :  :
GROUND...........................................  :  :  :  :  :
Carrier Detect (CD)........—>..................  :  :  :  :  :  :
                                              .  .  .  .  .  .  .
                             Ø13Ø  Ø  Ø  Ø  Ø8 Ø7 Ø6 Ø5 Ø4 Ø3 Ø2 Ø1
          MAIN PORT
          RS-232C CONNECTOR   Ø25Ø24Ø23Ø  Ø  Ø20Ø  Ø17Ø  Ø  Ø  Ø14

                              -: -: +:        :     +:
                               :  :  :        :      :
-Receive Current Loop......—>..:  :  :        :      :
-Transmit Current Loop.....<—.....:  :        :      :
+Receive Current Loop......—>........:        :      :
Data Terminal Ready (DTR)..<—.................:      :
+Transmit Current Loop.....<—........................:


Receive Data (RD)..........—>..................................
Transmit Data (TD).........<—..............................   :
Request To Send (RTS)......—>...........................   :  :
Clear To Send (CTS)........<—........................   :  :  :
Data Set Ready (DSR).......<—.....................   :  :  :  :
GROUND...........................................  :  :  :  :  :
Carrier Detect (CD)........<—..................  :  :  :  :  :  :
                                              .  .  .  .  .  .  .
                             Ø13Ø  Ø  Ø  Ø  Ø8 Ø7 Ø6 Ø5 Ø4 Ø3 Ø2 Ø1
          PRINTER PORT
          RS-232C CONNECTOR   Ø25Ø  Ø  Ø  Ø  Ø20Ø19Ø  Ø  Ø  Ø  Ø14

                                              :  :
Data Terminal Ready (DTR).........—>..........:  :
Secondary Request to Send (SRTS)..—>.............:
```

Figure 2-4. SW10 Interface Connectors

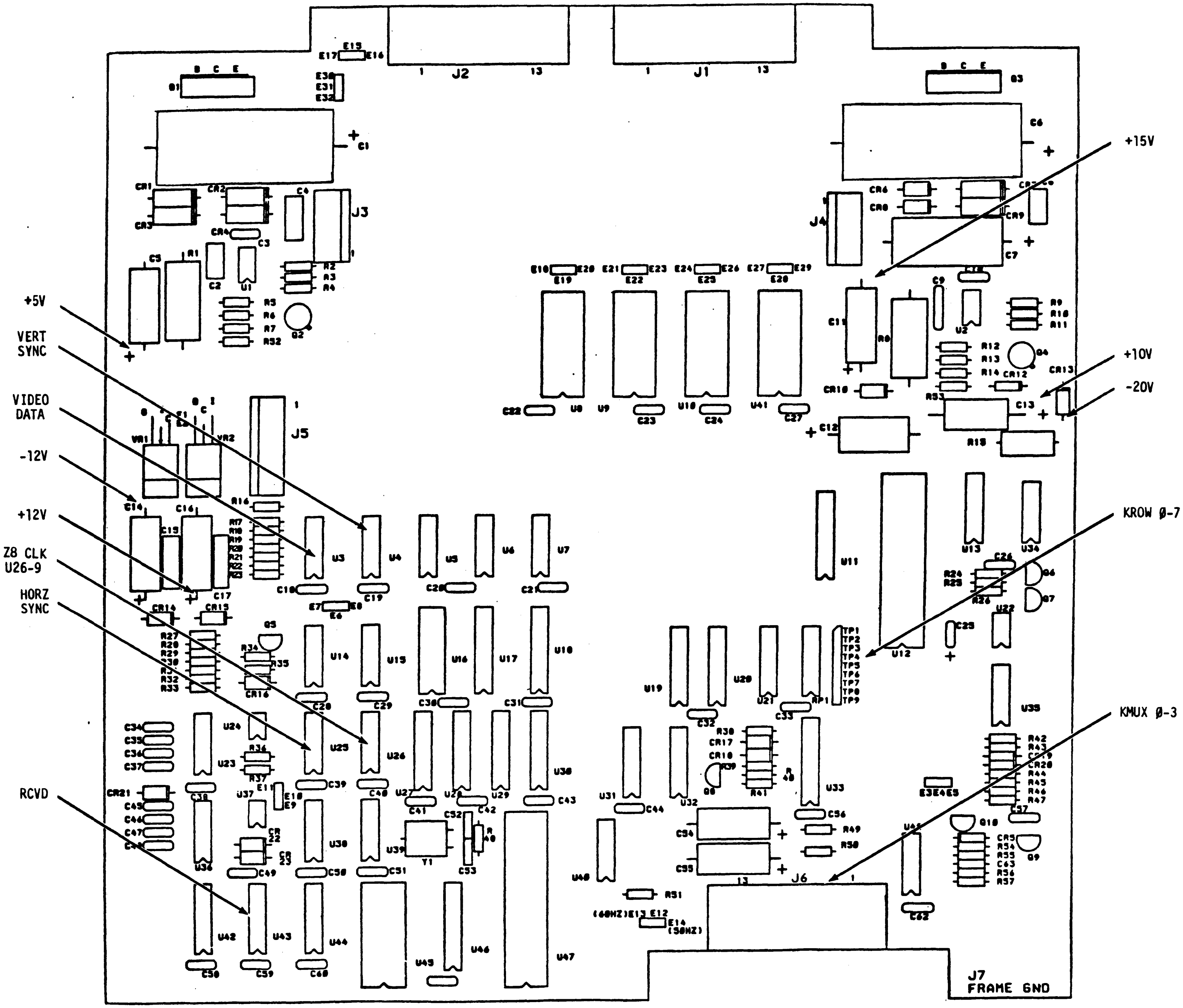


Figure 2-5. Terminal Control Board Test Points

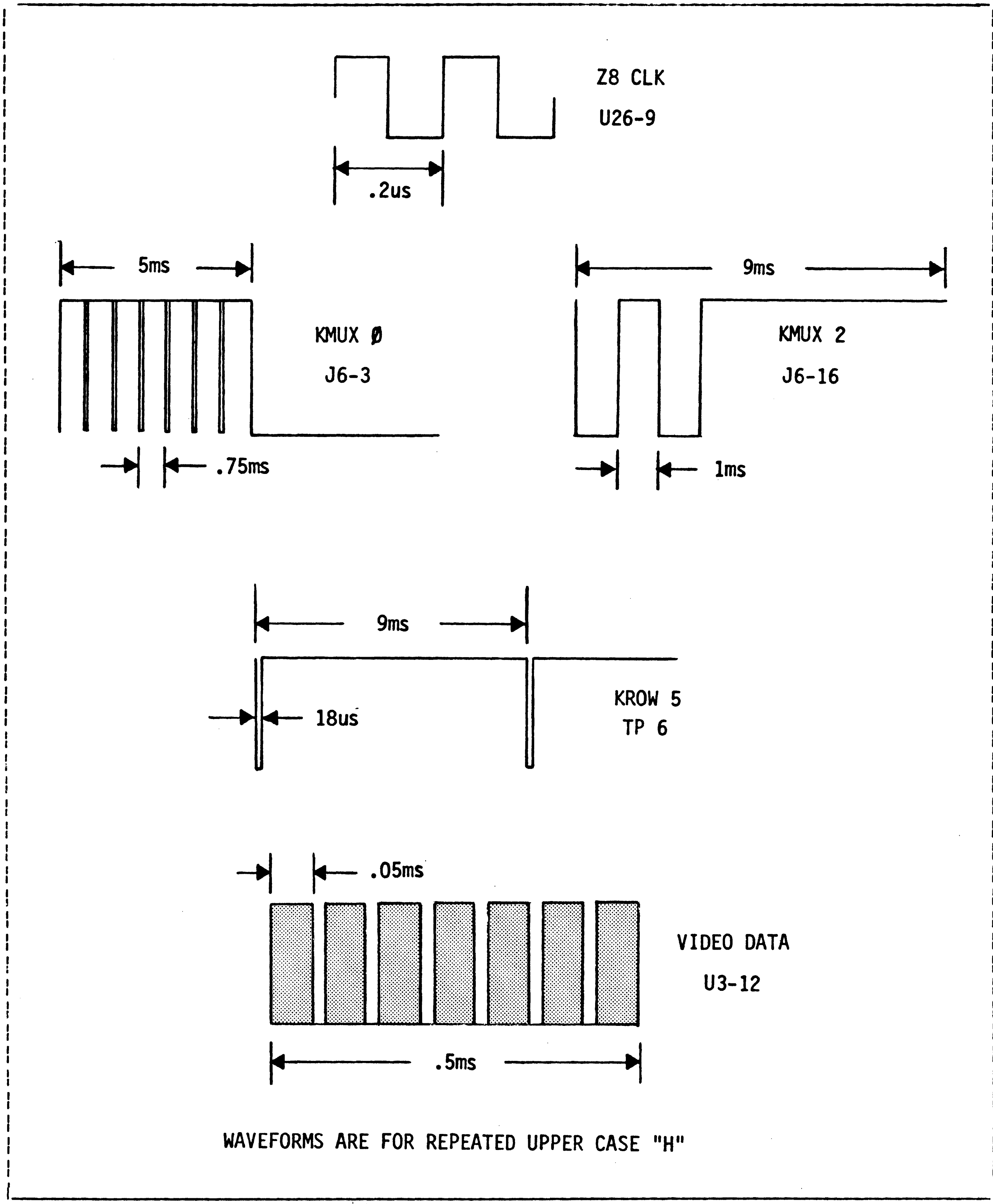


Figure 2-6. Typical Waveforms

3.0 THEORY OF OPERATIONS

The Theory of Operations is divided into two sections. The first section is a general discussion of the major functional elements of the SW10. The second section is detailed circuit description of terminal operations. Product Specifications information for the Z8 microprocessor is provided in Appendix A.

3.1 GENERAL

Functionally, the SW10 is composed of four major elements. They are the keyboard assembly, the terminal control board, the monitor assembly, and the power transformers. Figure 3-1 shows the basic flow of terminal signals and voltages between these components.

3.1.1 Keyboard

The keyboard is a typewriter style input device used by the operator to communicate with the terminal, the CPU, or any connected peripheral device. The SW10 uses a scanning type keyboard which, utilizing commands from the microprocessor, sequentially interrogates each key position to determine if a key has been pressed. If a key has been pressed, the keyboard sends out the a signal to the terminal control board.

The scanning technique allows two keys to be pressed at a time and still be sensed by the encoder. This is called "2-key rollover".

The keyboard also contains the speaker for the keyclick and bell tone.

3.1.2 Terminal Control Board

The terminal control board is a single PC board assembly that controls all display and communications functions of the terminal. It contains a Z8 microprocessor for managing all terminal operations, video processing circuits for converting data into screen presentations, non-volatile memory (NVM) for storing the user settable operating parameters, and interface circuits for controlling terminal communications.

The terminal control board firmware consists of 12K bytes of EPROM for program operations, 2K bytes of RAM for display memory, and 1024 bytes of scratch pad RAM.

3.1.3 Monitor Assembly

The monitor assembly is made up of three parts; the monitor control board, the flyback transformer, and the CRT (cathode ray tube). The monitor control board receives vertical and horizontal sync signals and video output signals from the terminal control board. The standard monitor is a conventional 12 inch P-31 green phosphor CRT using a raster scan non-interlaced (overlap) refresh technique. (P-4 white is optionally available.) A detailed description of the monitor assembly operations can be found in the TV Documentation Manual (GTC# 05018-001).

3.1.4 Power Transformers

Two power transformers are mounted on the power panel at the rear of the terminal. The transformers deliver stepped-down AC voltages to the terminal control board where the voltages are rectified and regulated. Input voltages ranging from 100 volts to 240 volts can be accommodated by means of jumpering on the primaries of the transformers.

3.2 DETAILED THEORY OF OPERATIONS

The following section is a detailed discussion of the operation of the subassemblies mentioned in Section 3.1. These sub-assemblies are, in order of discussion, the keyboard, the terminal control board, the monitor control board, and the power transformers. Terminal control board schematic set 720019 and keyboard schematic 720002 should be referred to while reading this section.

3.2.1 Keyboard Assembly

The keyboard is composed of 96 keys arranged in a matrix which is under microprocessor control and is scanned to detect key depressions.

Figure 3-2 is a signal flow diagram for the keyboard circuits. Schematic 720002 shows the keyboard matrix and scanning multiplexer. Keyboard scanning is initiated by the microprocessor. Data bits D0 through D7 from the microprocessor are applied to Function

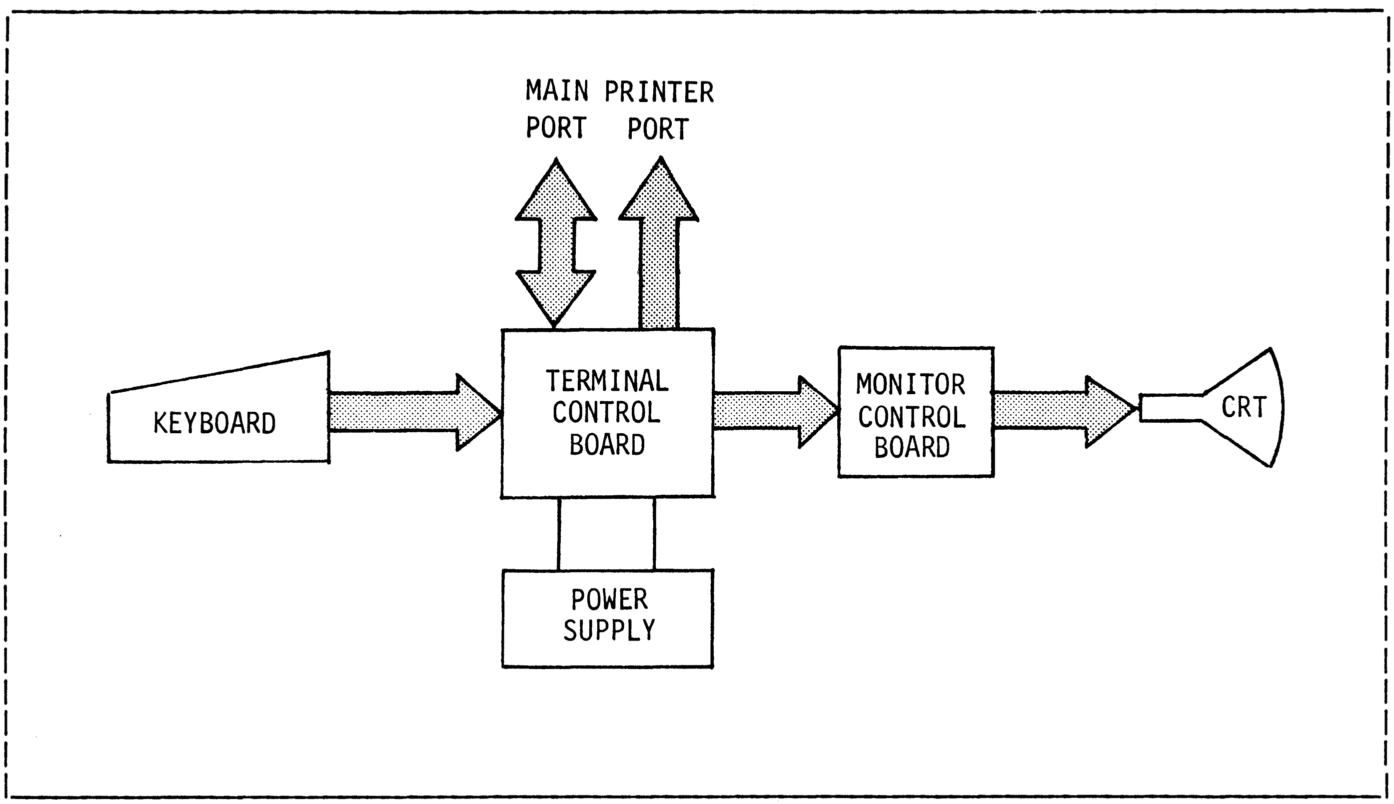


Figure 3-1. SW10 Block Diagram

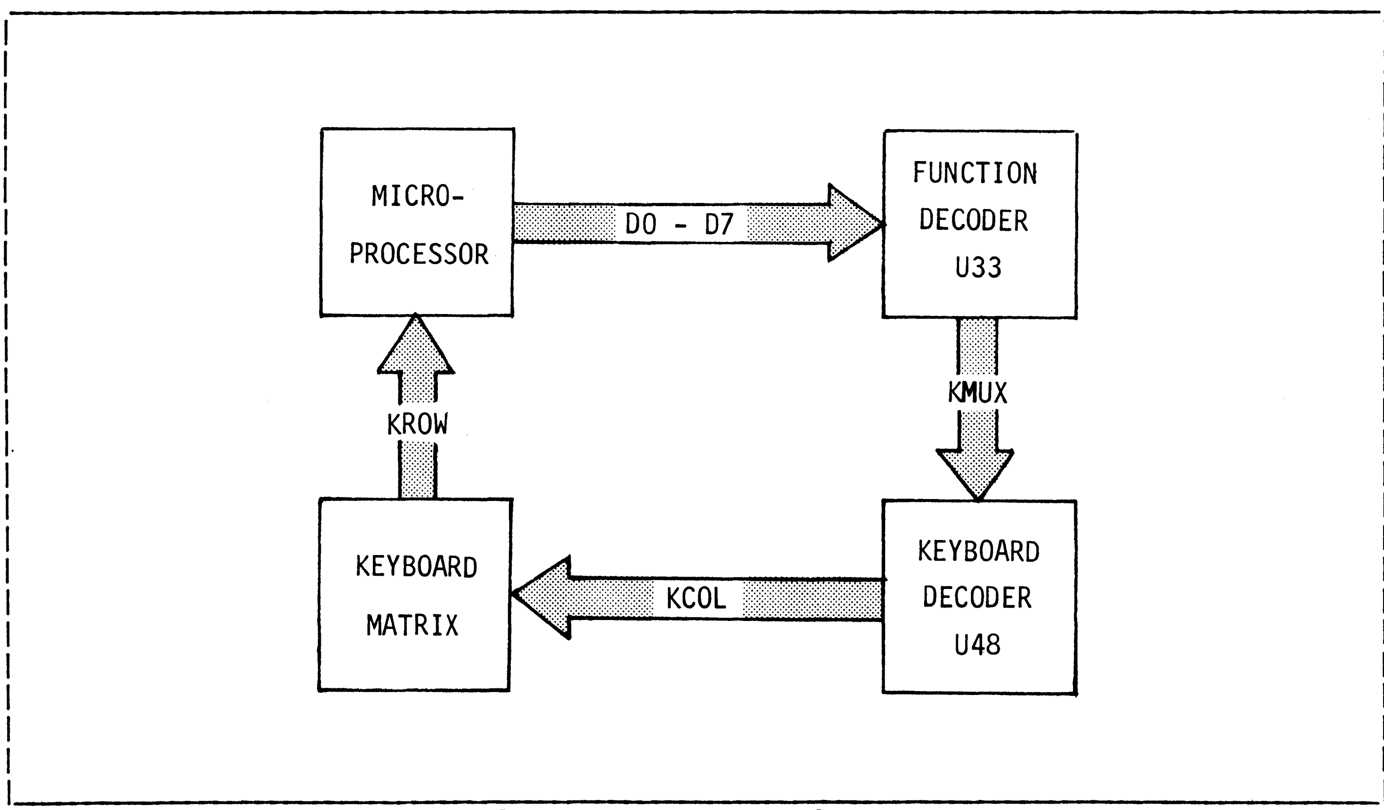


Figure 3-2. Keyboard Scanning Sequence

Decoder #1 (U33 sneet 4) which generates keyboard multiplexing terms KMUXØ through KMUX3. These terms, applied to the column scanning multiplexer U48, are the hexidecimal equivalent of the keyboard column number to be scanned. U48, a 4 to 16 decoder, selects one of the outputs KCOLØ through KCOL13, driving it low. This supplies a low to one side of all the key contacts in the selected column. When a key in that column is pressed, the appropriate row is driven low. The microprocessor is prepared to receive inputs from the KROW lines. Since the microprocessor knows which column is being scanned it will be able to determine which key was pressed when it senses one of the KROW lines going low. The KCOL outputs are selected in a sequential manner and only one of these lines is low at any given time.

As an example, assume that KMUX1 and KMUX2 are high and the other two inputs are low. This is a hex six and output KCOL5 at U48-6 will be driven low. This low is presented to keys B, V, C, X, Z, \, RTN, and '. If the Z key were pressed, KROW3 will go low. This low-true signal will be sent to the microprocessor. The microprocessor will perform a look-up in a ROM table and determine that a KMUX1 and KMUX2 plus a KROW3 is equivalent to an ASCII character lower case z.

3.2.2 Terminal Control Board

Figure 3-3 shows the terminal control board divided into 15 functional blocks. These blocks are:

[1] Address Initialization Circuit
[2] Microprocessor circuits
[3] Program PROM
[4] Scratch pad RAM
[5] Display RAM
[6] Video timer and controller (VTAC)
[7] System Clock
[8] Row buffer
[9] Video generator
[1Ø] Function Decoder #2
[11] Function Decoder #1
[12] Non-Voilatile Memory (NVM)
[13] Interface Circuits
[14] Bell amp
[15] Power supply

The keyboard and the monitor are not part of the terminal control board, but are shown on the drawing for data flow information only. The signals shown on Figure 3-3 are the major signals. Additional information may be exchanged between blocks.

[1] ADDRESS INITIALIZATION CIRCUIT (Sh 3)

The Z8681 used in the SW1Ø requires a starting address of 8ØØ instead of ØØ. Therefore, the reset pulse must be applied to U12 for six clock pulses to allow the microprocessor to step to the proper address. The delay circuit consists of Q1Ø, U4Ø, U48 and associated components.

When power is first applied U4Ø-6 will be held low for a period of time determined by C55 and R5Ø. This low will cause a hi at U48-2 and a corresponding low at U48-6 and U48-4. The low at U48-6 is applied to U12-6. The low at U48-4 allows C63 to charge, keeping Q1Ø turned off. When C55/R5Ø times out, U4Ø-6 will go hi, U48-2 will go low, and U48-6 will go hi, removing the ground from U12-6. U48-4 will also go low allowing C63 to discharge and turning Q1Ø on. U12-6 will go hi. Zener diode CR5 provides voltage protection for U12.

[2] MICROPROCESSOR (Sh 3)

The heart of the SW1Ø is the Z8 microprocessor. It controls all of the input and output operations of the terminal. Under program control, the microprocessor will fetch data, execute instructions, and respond to the needs of various terminal circuits. The Z8 fulfills the need for high-speed data handling by having 32 ports dedicated to input/output operations. The 32 I/O pins are arranged into four ports of 8 lines each. Under program control, these ports provide address, timing, and status signals. The SW1Ø uses Port Ø as the high order memory address output. Port 1 is a combination data I/O and low order memory address output port. Port 2 is used by two different circuits. It serves as a data input port for the keyboard and is the I/O port used by the NVM. Port 3 has four input and four output lines. The input ports P3-Ø thru P3-3 are used for communication input and for signaling the start of a video data transfer. The output ports, P3-4 thru P3-7, are used for

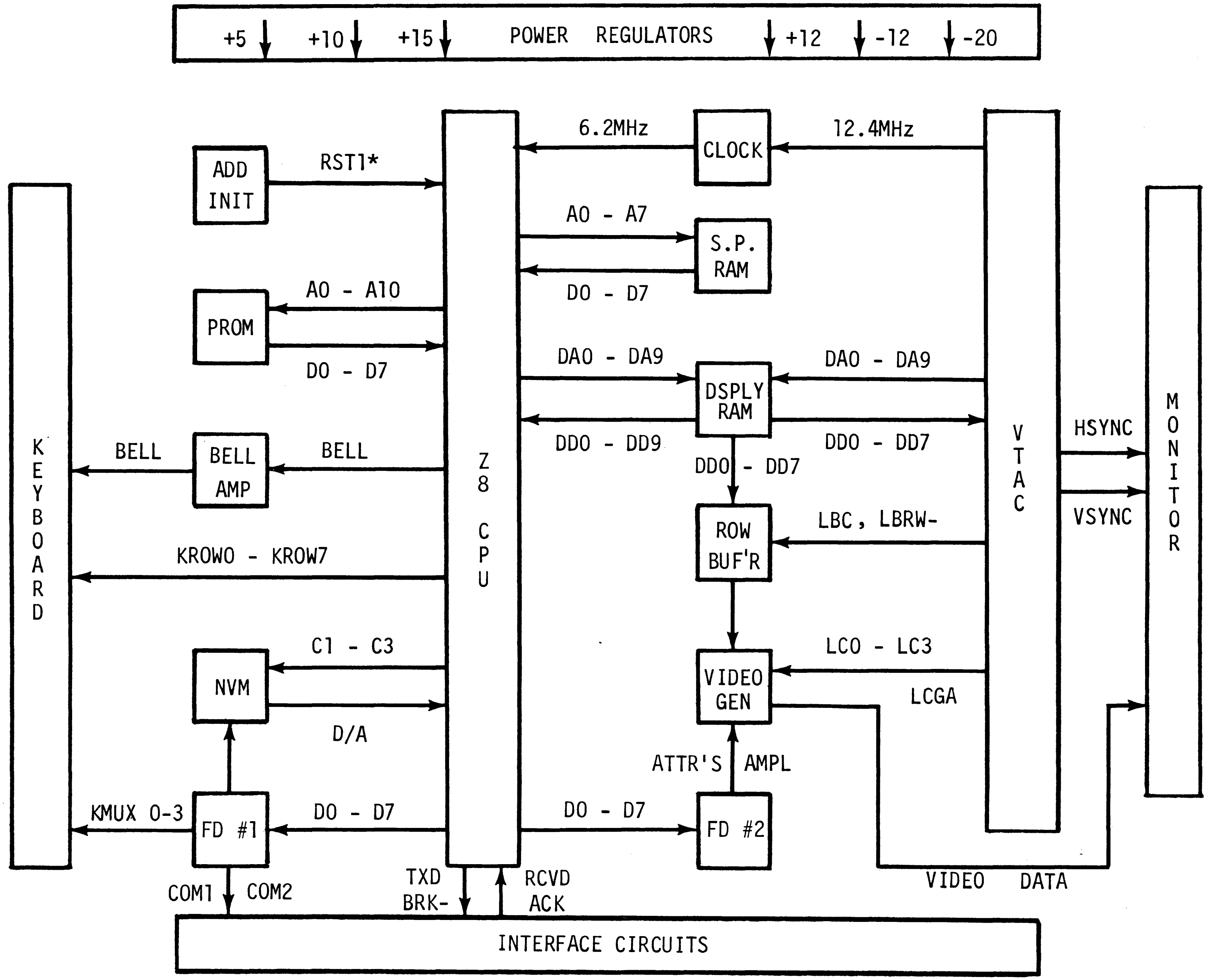


Figure 3-3. Terminal Control Board Signal Flow Diagram

controlling memory I/O operations, communications output operations, and controlling the bell.

The microprocessor uses a 16 bit address bus. The high order address bits determine if an output operation will take place, if the VTAC will be selected, if a change in video output should occur, or if a specific memory IC will be selected. The lower order address bits select the exact memory location.

The low order address bits, A0 through A7, appear at Port 1 of U12 and the high order address bits, A8 through A15, are on Port 0. The Z8 (U12) also outputs two strobe pulses. They are the Address Strobe Not (AS-) at pin 9 and the Data Strobe Not (DS-) at pin 8. When AS- at U11-11 goes high, the address bits on Port 1 are latched into U11 and onto the address bus. Since the high order bits are always present there is no need to latch them onto the address bus.

The microprocessor circuits consist of the Z8, U12, tri-state buffer U21, latch U11, plus decoder U13 and its associated gates.

U13 is a dual 2-to-4 decoder. The top half selects scratch pad RAM or display RAM. The lower section selects a specific memory element for the microprocessor to work with. Program Selection Not (PMS-) determines which section will be active.

If the microprocessor wishes to access the scratch pad or display RAM, term PMS- will be low. This term, along with Data Strobe Not (DS-), provides an enable at pin 1 of U13. If A11 and A12 are low the scratch pad RAM will be selected and SMO- at pin 4 will go low. If A11 is high and A12 is low, the display RAM will be selected and Display Memory Select Not term DMS- will be low. If A12 is high, neither output will be selected.

When the microprocessor wishes to access the program memory, term PMS- will be high, and along with the Data Strobe Not (DS-) will enable the lower portion of U13. Table 3-1 shows the procedure used in selecting a specific memory element. The selected PROM will be output enabled at pin 20.

INPUT PIN 14	INPUT PIN 13	OUTPUT PIN 12	OUTPUT PIN 11	OUTPUT PIN 10	OUTPUT PIN 9
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

Table 3-1 PROM ENABLE

Port 2 is an I/O port used by the keyboard and by the non-volatile memory (NVM) circuitry. Tri-state buffer U21 is utilized for discriminating between information coming from the keyboard and information going to the NVM. The selection is determined by signal NVM applied to the anode of CR17. When this signal is high, microprocessor information will be sent to the NVM circuits. When signal NVM is low, the tri-state buffer is enabled, allowing keyboard information to be passed thru U21 and on to the microprocessor.

[3] PROGRAM PROM (Sh 3)

The program memory consists of 12K of EPROM contaned in 4 IC's, U8, U9, U10, and U41. The address location of each PROM is shown on the schematic. When the microprocessor wishes to access the program memory, all four EPROM's will be Chip Enabled (CE) by the write term WR- which is low during a read operation. However, only one PROM will be Output Enabled (OE) as previously discussed.

U17 is a bi-directional tri-state isolator that determines if the program memory data bus or the display memory data bus is connected to the microprocessor data bus.

[4] SCRATCH PAD RAM (Sh 4)

The scratch pad RAM is a section of memory in which the microprocessor temporarily stores the information it needs to execute the control program. It consists of two 512 x 8 ICs, U19 and U20, for a total of 1024 bytes. The scratch pad RAM is selected when Scratch Memory Not (SMO-), applied at pin 8, is low. A second term, Memory Write Not (MWR-), on pin 10 will determine if the operation is a read or write operation. MWR- is a combination of Data

Strobe Not (DS-) and the write command signal WR-. If MWR- is low, data will be written into RAM.

If MWR- is high, data will be read from scratch pad memory. Scratch RAM addresses come directly from the microprocessor and data out goes directly to the microprocessor. These memory elements are unavailable for use by any other circuit.

[5] DISPLAY RAM (Sh 4)

The display RAM (U27, U28, U29 and U30) is the portion of memory which stores the data to be displayed on the screen. The display RAM is accessable by the microprocessor and the VTAC. The microprocessor can read from and write into the display RAM, but the VTAC can only perform a read operation. When the microprocessor wishes to access the display RAM, the Display Memory Select Not term DMS- from U13-5 (Sh 3) goes low. This signal, applied to U17-9, connects the microprocessor data bus to the display RAM data bus. If the microprocessor wishes to write data into display RAM, the write signal WR- at U17-11 will be low. If WR- is high, a read operation will occur. Z8ACC- will be low, connecting the microprocessor and display RAM address buses. Display Memory Select Not DMS- is also applied to U5-4 and U6-4 where it is used as an enable for selecting the low order RAM U27 and U30, or the high order RAM U28 and U29.

Normally the display RAM is under the control of the microprocessor. However, every tenth scan line, the VTAC must access the display RAM to fill its row buffers with the ASCII character information for the next line. At this time, signal IBWR- goes low, indicating that data will be entered into the row buffer. VTAC outputs A0 through A11 are the data address bits. The output of either U15-6 or U6-3 will be low, selecting the high order or low order RAM chips. Since the VTAC can only read data from RAM, pin 10 of the RAM ICs will be high, inhibiting any write operations. The display data out is entered into row buffer U16 (sheet 5). During this VTAC operation Z8ACC- is high, causing the microprocessor I/O buffer to be in a float state, thereby separating the microprocessor and the VTAC address buses and allowing the Z8 to perform other tasks, such as keyboard scanning.

[6] VIDEO TIMING AND CONTROL (VTAC) (Sh 4)

The VTAC generates all necessary video timing signals for the monitor circuits. It also provides timing signals for the memory, buffers, and the dot generation circuits plus cursor and blanking signals. The VTAC circuit is composed of U47 and crystal Y1.

The VTAC contains three independent registers which store screen presentation attributes. The three registers determine where the top of page will begin, where the character row will begin, and where the cursor will be displayed. The registers are loaded in response to signals RA and RB which come from Function Decoder #2 (U18 sheet 5). These signals are generated by data outputs from the microprocessor. When A15 (microprocessor output), A14 (VTAC select), and DS (Data Strobe) are true and RA and RB are true, the data on VTAC lines DA0 through DA11 will be loaded into the VTAC registers. The microprocessor feeds new information into the VTAC regarding top of line, row start, etc.

The timing outputs from the VTAC are the horizontal and vertical sync signals, vertical blanking signals, and scan line outputs. The horizontal sync and vertical sync are used to directly drive the monitor at the proper frequency. The vertical sync output, which determines the refresh rate of the information being displayed on the screen, is set by the 50/60 Hertz input on pin 3. This pin is jumpered to either +5 volts or ground. The vertical blanking signal output from the VTAC is used to signal the microprocessor when a vertical scan has been completed. This essentially is an interrupt to the microprocessor which gives it the information it needs to determine at which point to do a screen scroll or memory change operation. If the operation were performed in the middle of a screen refresh sequence it would cause the screen to blink noticeably.

The LC0, LC1, LC2, and LC3 outputs of the VTAC are the scan line outputs. The screen is painted in a raster scan fashion. Each line of characters on the screen is actually made up of a series of dots (see Figure 3-4). This scan line information from the VTAC is sent to the character generator. It allows the character generator to keep track of which line is being scanned to insure the cnaracter generator outputs the proper dot pattern.

The VTAC output signal CUR on pin 19 is true during the period of time the cursor is to be displayed. The VTAC keeps track of the current cursor location at all times. The location of the cursor is determined by the contents of registers RA and RB.

The VTAC provides timing signals to the display RAM, the display RAM buffer, and tne display data buffered latch. These very rapid signals must occur in an exact sequence to enable the passing of information from the display RAM to the row buffer U16. From U16 it is gated on a character by character basis into the character generator for dot processing. Signal LBWR- (Line Buffer Write Not) allows the display RAM to be accessed and pass its information into the line buffer. The LBC signal (Load Buffer Clock) is used to move the information from the display RAM into the 8 bit wide, 80 bit long shift register. The LCGA signal (Latch Character Generator Address) latches this information into an 8 bit latch, U46, and on into the cnaracter generator.

The VTAC circuit also contains the crystal oscillator. This is used to generate the 12.2472 MHz dot clock signal used for strobing the individual dots out of the display circuitry. The dot clock output is also used in the clock generator circuitry.

[7] SYSTEM CLOCK (Sh 4)

The system clock is derived from a crystal-controlled oscillator operating at 12.2472MHz. The clock is an input into the VTAC for use in system synchronization. The dotclock output (pin 23) is buffered by U4 and fed into U26, a divide by two flip-flop. The resulting output, Z8CLK, is a 6.1236MHz clock with a 50% duty cycle. This is the clock frequency used by the Z8.

[8] ROW BUFFER (Sh 5)

The row buffer is composed of 80 bit shift register U16. Under the direction of the VTAC, it accepts a group of 80 characters from the display RAM and passes that data to the character generator.

The VTAC (U47) addresses the display RAM (U27 through U30), retrieves the information, and places it on the display data lines (DD0-DD7) to the row buffer. At the appropriate time the VTAC will output signals LBWR- (Line Buffer Write Not) and LBC (Line Buffer Clock), which will gate the display data into the 80 bit line buffer U16. Once 80 columns of data has been entered into U16, the VTAC and microprocessor disassociate themselves from the display circuits and attend to other terminal functions.

When the VTAC determines that all 80 columns of data has been transferred to the video generator circuits it will fetch a new group of 80 characters from the display RAM and route it to the display buffer and the above process is repeated.

[9] VIDEO GENERATOR (Sh 5)

The video generator circuitry accepts parallel inputs from the row buffer into the character generator. The output of the character generator goes to a parallel to serial shift register which outputs a stream of serial data. This data stream is acted upon by various attribute determining gates and flip-lops. The video generator circuit is shown on the top half of schematic sheet 5.

U46, an eight bit register, accepts parallel data inputs from the row buffer. Signal LCGA (Latch Character Generator Address) gates one character at a time into the register. The 8 bit ASCII word is then presented to the character generator U45.

The character generator is a 4096 byte PROM. The data on address lines A4 through A10 selects a particular character in the character generator. The character is formed by a 5x7 dot matrix on a 7 dot by 10 scan line field. Scan line counter signals LC0, LC1, LC2, and LC3 determine which line is currently being scanned. The character generator will output the appropriate dot pattern for that particular scan line of the character. When Load Video Shift Register (LVSR) from the VTAC goes high, the dot pattern will be loaded into U44, a parallel to serial shift register. The output on pin 9 will be a serial data stream.

The clock at pin 2 of U44 comes from U38-6 and is normally in step with the DOTCLK- applied at pin 4. Occasionally the character generator will output a cnaracter which requires dot slide. When this occurs, the least significant bit at pin 9 of the character generator will be high. This signal is applied to the D input of U39-5, the dot slide flip-flop. When term LVSR goes low the output of U4-2 goes high and sets flip-flop U39. The resulting high output at pin 5 will inhibit EXCLUSIVE OR U38 and pin 6 will go low. Data can no longer be clocked out of U44. LRC (Line Rate Clock) will reset U39 again enabling U38. This action has effectively delayed the dot clock input to U44 by 1/2 clock time and consequently has delayed the output by 1/2 clock time. This results in the dots on that particular scan line being shifted 1/2 position to the right. This technique, known as dot slide, rounds off the corners making a more natural looking character. Refer to Figure 3-4.

U39-9 is an attribute flip-flop which can be set and reset on a character by character basis. When U39 is set, the attribute will be selected. What the attribute will be is determined by the jumpering between E6, E7, E8, and E9, E10, and E11. If jumpers are installed from E6 to E7 and E9 to E10 reverse video will be the selected attribute. If the jumper is from E6 to E8 and E10 to E11, half intensity will be the attribute. If the attribute has been selected, the output of U46-12 will be high. When LVSR (Load Video Shift Register) from the VTAC goes high, the attribute flip-flop will set. If the E6 to E8 jumper is installed, U39 being set will cause U3-2 to go low, placing R21 in parallel with the brightness determing resistor network R17 through R23, thus reducing the selected brightness by half. If U39 is set and E9 is jumpered to E10, the output of the attribute flip-flop will be entered into EXCLUSIVE OR gate U38 pin 9. The serial video data stream is entered into U38-10. As long as pin 9 is high the U38 will act as an inverter, thereby reversing the video output at pin 8. When flip-flop U39 is reset, pin 9 of U38 will go low and the video data stream at pin 10 will pass through U38 unaffected.

Function Decoder #2 (U18) outputs a reverse video signal (RVID-) which is used to reverse the video presentation of the entire screen. When RVID-, applied at U38-1, goes low, EXCLUSIVE OR U38-3 will operate as an inverter, resulting in the video data being presented as dark dots on a light background.

The cursor is displayed as a block 8 scan lines high and one character wide. LC0 and LC3 at U14-2 and U14-1 are line counting signals which indicate the line being scanned. When the CRT

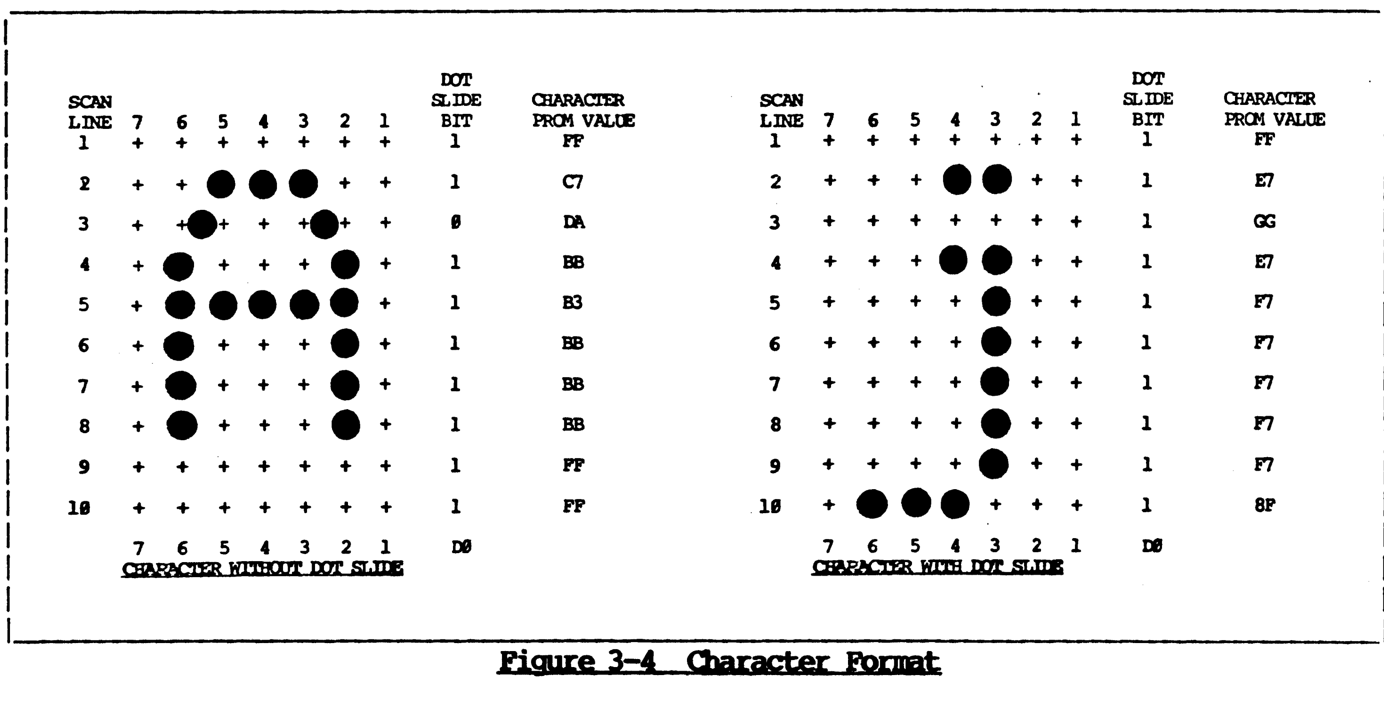


Figure 3-4 Character Format

beam is positioned correctly to display the cursor, the VTAC will output signal CUR. This signal is entered into U25-5. Signal CBLINK- from U18-15 will be a constant high if the cursor is to be non-blinking. CBLINK- will change at a 1 Hz rate if blinking is desired. It is gated with the line counting signal and ANDed with signal CUR. The output at U25-6 will be a cursor signal blinking at a 1 Hertz rate.

The video blanking portion of the video generator circuit is composed of flip-flop U26-6, buffer U5-11, and inverter U14-8. The purpose of the video blanking is to prevent flickering or apparent changes of information on the screen when data is being clocked into the video shift register U44. The LVSR signal that load enables the video shift register also sets video blanking flip-flop U26. The false input at pin 6 is buffered, inverted and fed into U14-12 where it interrupts the video data out.

[10] FUNCTION DECODER #2 (Sh 5)

Function decoder #2 is composed of U18 and its associated gates and inverters. This decoder determines the brightness level of the screen, selects normal or reverse video, puts the cursor in its solid or blinking mode, and generates two signals to be used by the VTAC for video presentation.

When power is first applied, the reset signal RST2- at pin 1 will set all of U18 outputs to a low state. The level of input bits D0 through D7 will be determined by the microprocessor.

If output command bit A15 and the attribute selection bit A13 are true, then U15-11 is enabled. When strobe term DS- goes true, a clock pulse will appear at U18-11 gating the input data into the decoder. The decoder outputs on pins 2, 19, 5, and 16 drive four hex inverters which form a variable voltage divider network with 16 possible outputs. If all four decoder outputs are low, only R22 and R23 are in the divider network. Video amplitude signal VAMPL will be at its highest level. When one or more of the decoder outputs goes high it places additional resistance in parallel with R23 reducing the level of VAMPL. The reverse video output RVID- is sent to the video generator logic. When RVID- is true the video presentation will be dark characters on a light background.

CBLINK- is the cursor blink command. This output from pin 15 also goes to the video generator circuits. The signal level is under microprocessor control and causes the cursor to blink.

The last two outputs, RA and RB, are sent to the VTAC where they are used to change the screen presentation or move the cursor.

[11] FUNCTION DECODER #1 (Sh 4)

Function Decoder #1 consists of U33 and NAND gate U7-6.

The function decoder accepts data inputs from the microprocessor and develops signals which determine the keyboard scanning sequence, decides if the NVM should be enabled, determines the direction of data flow through the communications ports, and generates a Request-to-Send signal.

When power is first applied to the terminal, reset term RST2-, applied at pin 1, will set all of the decoder outputs low. The microprocessor will establish the level of input data bits D0 through D7. NAND gate U7-6 supplies the clock pulse for the decoder. A15 at U7-3 will be high when the microprocessor wishes to output data. A12 at U7-5 will be high when U33 is to be the output device. When data strobe signal DS goes low, the clock signal at pin 11 will go high , and the data on the input lines will be gated into the decoder.

The first four outputs, keyboard mux terms KMUX0 through KMUX3, are used by the keyboard to scan the fourteen columns of the keyboard matrix.

The output at pin 6 is NVM-. This signal enables the non-volatile memory circuitry. Refer to paragraph [12].

Outputs COM1 and COM2 are used by the communication ports to determine tne routing of transmitted and received data. Refer to paragraph [13].

The final output is the Request-to-Send signal

RTS1. This term is sent out the main port announcing the desire of the terminal to transmit data.

[12] NON-VOLATILE MEMORY (NVM) (Sh 3)

The NVM (non-volatile memory) stores the operating parameters for the terminal. When the terminal is turned on the contents of the NVM is fed into the microprocessor U12 which uses this data to set the initial operating condition.

The use of NVM offers two advantages. First, since it is an electrically alterable device, changes can be entered from the keyboard, eliminating the need for mechanical switches. Second, since the memory is non-volatile, the contents of the EPROM are not lost when power is removed.

The non-volatile memory (NVM) circuitry is composed of Q6, Q7, Q9, 6 line buffers (U35), and NVM IC U22. U22 is a 336 bit (21 x 16) electrically alterable ROM (EAROM). This device stores all the operating parameters of the terminal.

Q9 is normally on, applying a ground to U22-3 and preventing the clock pulse from entering U22. Q6 is normally off, so term NVM is low. This low signal, applied to U21, allows the keyboard data to be passed thru to the microprocessor. Q7 is also off so the -20V is not applied to U22-1.

When an NVM operation is desired, term NVM- from Function Decoder #1 (U33, sh 4) will be low. This signal is applied to the junction of R44 and R46. At this time, three things happen. First, Q9 turns off and removes the ground from pin 3 allowing the clock pulse to enter U22. Secondly, Q6 turns on making term NVM true. This signal is applied to the tri-state buffers where it blocks the keyboard inputs and allows the microprocessor to write data out to the NVM. Third, Q6 turning on causes Q7 to turn on, applying -20V to U22-1. CR17 and R38 in the tri-state circuits protect U21 from any large negative spikes which may pass thru the base-emitter junction of Q7.

Since the NVM uses unusual voltages (-20v and +10v) its input and output lines are connected to CMOS line buffers. These buffers are capable of withstanding the negative spikes of the NVM. Diodes CR19 and CR20 provide protection for the sending and receiving devices. When writing information into the NVM, the D/A line is driven negative and CR20 passes this signal into the I/O port, pin 8. When reading information from the NVM, a low-going pulse passes through CR19 and U35 to the RD line of the microprocessor. The clock and circulation control signals C1, C2, and C3 are also buffered by U35. The levels on C1, C2, and C3 determine the type of NVM operation that will occur, i.e., ERASE, READ, WRITE, etc. Refer to Appendix A for NVM specifications.

[13] INTERFACE CIRCUITS (Sh 5)

Interfacing with external equipment is accomplished through RS-232C communication ports. Serial data is received and transmitted through conventional receiver and driver ICs for EIA signals and through optically coupled isolators for current loop signals.

Two dual 4 to 1 multiplexers are used to determine which port will be connected to the microprocessor I/O. Two communication signals, COM 1 and COM 2 from Function Decoder #1 (U33 sh 4) determine which input in the multiplexer will be connected to one of the outputs. The chart on sheet 5 shows the condition of the two communication signals in various modes.

When the host is sending data to the terminal it is received at J1 pin 3 where it is routed through U23-11, an RS-232C receiver chip which converts the +12V and -12V signals into 0 volts and +5V respectively. The 0 to +5 varying signals will be fed into OR gate U15-3. The output will be sent to 4 inputs on U43. If the data is to be used by the terminal only, COM 1 will be high and COM 2 will be low. This will cause the received data to be routed out pin 7 of U43 and on to the microprocessor.

If the terminal is in PASSTHRU DISPLAY mode where data will be displayed on the screen and also be routed out the printer port, COM 1 and COM 2 will both be high. Now, in addition to the data being routed out pin 7, it will also be routed out U43 pin 9. It enters level shifter U36 and goes on out printer connector J2.

The transmitting of data from the terminal is handled in a similar fashion. The data is entered into U25-12 and applied to U42 and U43. If the PASSTHRU mode is turned on or if the buffered printer is selected, the data will go out U43 to J2. If the terminal is in NORMAL transmit mode the data will be routed through U42-9, thru level shifter U36-11, and out J1 pin 2.

The current loop receivers and drivers are optically coupled isolators. These isolators are operated by a current passing through a light emitting diode which is internal to the MCT 210 isolator causing it to light and activate an internal photo transistor. When current passes through the diode and the light activated transistor is stimulated, current flows through the collector to emitter junction. U37-4 will go high whenever current is being passed through the current loop received section. Diode CR22 is provided to allow a closed current loop to occur when the current source is applied in a reverse polarity.

The current loop output stage operates very similiary to the receive stage. In the transmit circuitry, when data is present at U42-9, level shifter U36-8 drives the light emitting diode in U24. When pin 4 of U24 goes high, Q5 is turned off and current does not flow through the transmit portion of the current loop.

When a jumper is inserted between E31 and E32, the SW10 will act as the current source. If E31 is jumpered to E32, the terminal will sink current.

As discussed in paragraph [11] the signals RTS (Request-to-Send) is raised by the microprocessor when the terminal desires to transmit data. It is entered into U36 where its 0 and +5 volt levels will be changed to plus and minus 12 volts, respectively.

[14] BELL AMP (Sh 4)

Q8 is the Bell amp. It is used to drive the audio transducer on the keyboard. The microprocessor outputs a BELL signal at pin 40. When this signal is low, Q8 is forward biased and +5V is applied to the + side of transducer LS1, causing it to beep. The speaker is mounted on the keyboard PC board. R39 is a current limiting resistor and CR18 protects Q8 against negative spikes.

[15] POWER SUPPLY (Sh 2)

+5 Volt Regulator

The +5V regulator section is composed of a full wave bridge rectifier, linear voltage regulator U1, drive transistor Q2, and past transistor Q1.

The AC from the secondary of T1 is rectified by CR1 through CR4. The rectified output is filtered by C1 and fed to the unregulated input of U1 and to the emitter and collector of Q2 and Q1 respectively. R5 and R7 form a voltage divider network between the +5 volt regulated output and ground. R6 and R52 are trimming resistors selected at time of manufacture. If the regulated output should drop below +5V, the decrease in voltage would be sensed by the divider network and coupled to U1-6, the feedback terminal of the linear regulator. As a result, the booster output voltage at U1-2 would decrease, causing drive transistor Q2 to conduct harder. This in turn causes pass transistor Q1 to conduct harder bringing the +5V output back up to the desired level. The inversed conditions would exist if the +5V were to rise above normal.

R3 and R4 form another voltage divider network. This one is used for current sensing. If the current level is exceeded, U1 will enter a voltage feedback condition. R1 is a current limiting resistor.

C5 is a filter capacitor. Additional .01 uf capacitors are scattered throughout the logic board for decoupling of the +5 volt supply.

+15 Volt Regulator

The +15V regulator functions identically to the +5V regulator circuit. CR7 and CR9 form a full wave rectifier for this section. Some of the circuit components are different, most noteably the current sensing resistors R10 and R11. This allows a substantially smaller amount of current to pass through the regulator before voltage foldback begins.

±12 Volt Regulator

Regulation of the +12V is accomplished by a 78M12 3-terminal voltage regulator. Its input is the same rectified voltage used by the +15V section (approximately 18V) and the output is a constant +12V. C16 provides filtering and CR15 provides negative spike protection.

The -12V regulator, VR1, uses the -18V (approximately) which has been rectified by CR6 and CR8. It outputs a constant -12V which is filtered by C14 and protected against positive spikes by CR14.

-20 Volt Regulator

The -20 volts is regulated by Zener diode CR13. CR10 provides half-way rectification. C12 is a filtering capacitor. R15 is a voltage dropping resistor.

+10 Volt Regulator

The output of VR2, the +12V regulator, is applied across dropping resistor R16. Zener diode CR12 provides a constant +10V output. C13 is a filter capacitor.

The -20V output and the +10V output are used by the NVM circuits only. Due to the very light power requirements of these circuits, Zener regulation is adequate.

3.2.3 Monitor Assembly

The monitor assembly consists of three separate sub-assemblies. They are the CRT, the monitor control board, and the flyback transformer. Since GTC uses a variety of monitors, the following information is of a general nature. A detailed theory of operations for a particular monitor is contained in the TV Monitor Documentation Manual (GTC Part Number 05018-001).

Three signals are sent to the monitor control board from the terminal control board. These are the video data signal, the vertical sync, and the horizontal sync signal. The terminal control board also provides the +15 volts for operation of all monitor control board circuitry.

The video data signal from the video generator controls the brilliance (intensity) of the CRT beam. When the video data pulse goes high, the associated inverting transistor on the monitor control board drives the CRT cathode more negative. This causes the beam to become brighter. Half intensity and reverse video control the amplitude of the video data signals and hence the brightness of the beam.

The horizontal sync pulse is an output of the VTAC (schematic sheet 4) and performs two functions. It generates the basic horizontal scan frequency of 15,750 Hertz. This horizontal oscilator frequency drives the flyback transformer which generates the 12000 volt second anode voltage. The horizontal sync pulse also drives the horizontal deflection circuits which move the beam left and right on the screen.

The vertical sync pulse, also an output of the VTAC, controls the top to bottom movement of the beam. The low level signal is amplified on the monitor control board and sent directly to the deflection yoke.

3.2.4 Power Panel Assembly

The power panel contains the ON/OFF power switch, a line fuse, and two power transformers. The power panel is located in the inside lower rear of the terminal and is accessable by removing the monitor and logic board frame.

The two power transformers can accept an input voltage ranging from 100 volts to 240 volts. The power supply schematic (720019 sh 2) shows the jumpering required for the particular input voltage encountered. T1 is a 25 watt transformer used to supply stepped-down AC voltages to the +5 volt rectification circuits. T2 is a 40 watt transformer which supplies power for the remaining circuits. The AC input is a conventional 3-wire power plug. The ground pin is connected to chassis ground. The power switch and a 1 Amp fuse are in the hot line.

The power transformers are located as far from the monitor as possible to minimize flux-density and eliminate swimming on the screen. The transformer must be installed in the proper orientation or magnetic interference will result.

3.3 MNEMONICS

A0-A7	LOW ORDER BITS 0 THRU 7
A8-A15	HIGH ORDER BITS 8 THRU 15
ACK	ACKNOWLEDGE
AS-	ADDRESS STROBE NOT
AUX DTR	AUXILIARY DATA TERMINAL READY
AUX RECV	AUXILIARY RECEIVE
BELL	BELL
BRK-	BREAK NOT
CBLINK-	CURSOR BLINK NOT
CD	CARRIER DETECT
CLK	CLOCK
CLR TO SEND	CLEAR TO SEND
CL IN +/-	CURRENT LOOP RECEIVE +/-
CL OUT +/-	CURRENT LOOP TRANSMIT +/-
COM1	COMMUNICATIONS ONE
COM2	COMMUNICATIONS TWO
CTS	CLEAR TO SEND
CUR	CURSOR
D0-D7	DATA BITS 0 THRU 7
D/A	DATA/ADDRESS
DA0-DA9	DISPLAY ADDRESS 0 THRU 9
DD0-DD7	DISPLAY DATA 0 THRU 7
DMS-	DISPLAY MEMORY SELECT NOT
DOT CLK-	DOT CLOCK NOT
DSR	DATA SET READY
DS	DATA STROBE
DS-	DATA STROBE NOT
DTR	DATA TERMINAL READY
HORZ SYNC	HORIZONTAL SYNC
HSYNC	HORIZONTAL SYNC
KMUX0-3	KEYBOARD MUX 0-3
KROW0-7	KEYBOARD ROW 0-7
LBC	LINE BUFFER COUNTER
LBWR-	LINE BUFFER WRITE NOT
LC0	LINE COUNT 0
LC1	LINE COUNT 1
LC2	LINE COUNT 2
LC3	LINE COUNT 3
LCGA	LATCH CHARACTER GEN ADDRESS
LRC	LINE RATE CLOCK
LVSR	LOAD VIDEO SHIFT REGISTER
MWR-	MEMORY WRITE NOT
NVM	NON-VOLATILE MEMORY
NVM-	NON-VOLATILE MEMORY NOT
PMS-	PROGRAM MEMORY SELECT
PMS0-3	PROGRAM MEMORY SELECT
PRINT DATA	PRINT DATA
RA	REGISTER A
RB	REGISTER B
RCVD	RECEIVED
RD	RECEIVED DATA
RECV DATA	RECEIVE DATA
RST1	RESET 1
RST1*-	RESET 1* NOT
RST2	RESET 2
RTS	REQUEST TO SEND
RVID	REVERSE VIDEO NOT
SMO-	SCRATCH PAD MEMORY SELECT
SPKR +/-	SPEAKER +/-
TXD	TRANSMIT DATA
VBLANK	VIDEO BLANK
VERT SYNC	VERTICAL SYNC
VIDEO DATA	VIDEO DATA
VSYNC	VERTICAL SYNC
WR-	WRITE NOT
Z8ACC-	Z8 ACCESS NOT
Z8CLK	Z8 CLOCK

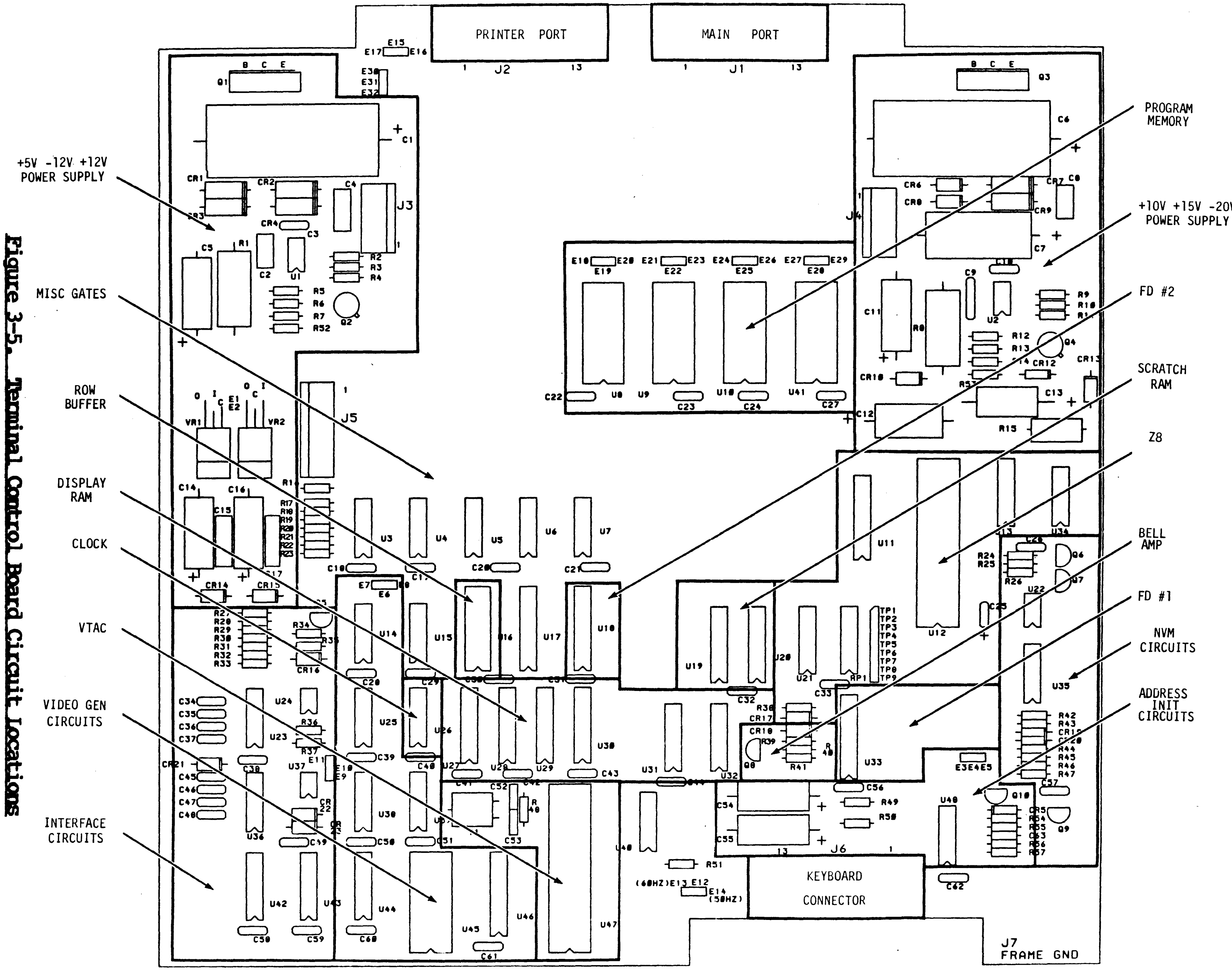


Figure 3-5. Terminal Control Board Circuit Locations

4.0 DISASSEMBLY PROCEDURES

This section contains information pertaining to the removal and replacement of the subassemblies. The SW10 can be broken down into seven major subassemblies. They are the logic board, the monitor, the monitor control board, the flyback transformer, the power panel, the keyboard, and the case. The following tools are required:

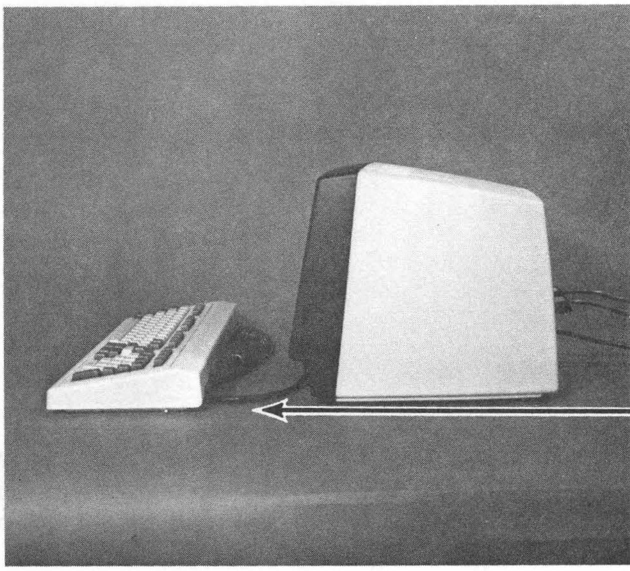
- #1 & #2 Phillips screwdriver
- needle-nose pliers
- 3/8 & 5/16" socket or wrench
- Test lead with clips.

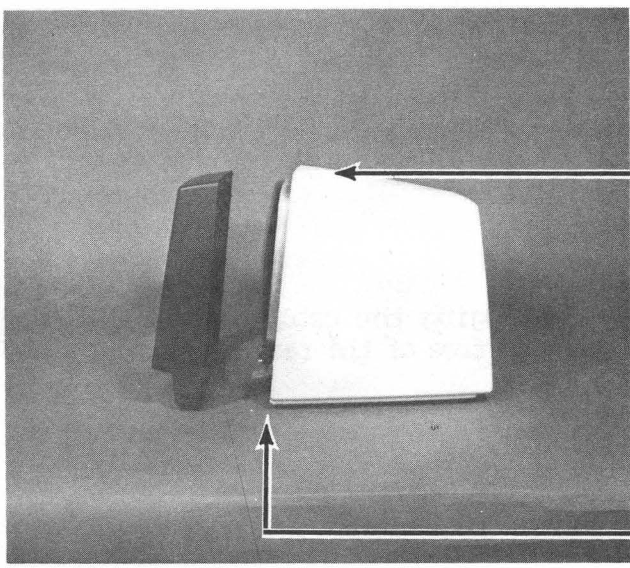
Perform the following steps when disassembling the SW10. Disassemble only to the extent needed to test or replace a part. When reassemblying the terminal, reverse the procedures outlined in this section.

The SW10 does not require any routine maintenance. However, occasional removal of dust from inside the terminal, particularly around the CRT, will help insure trouble-free operation. Periodic cleaning of the screen and case is recommended. Small scratches in the case can be removed with a fine rubbing compound.

4.1 REMOVING THE FRONT BEZEL

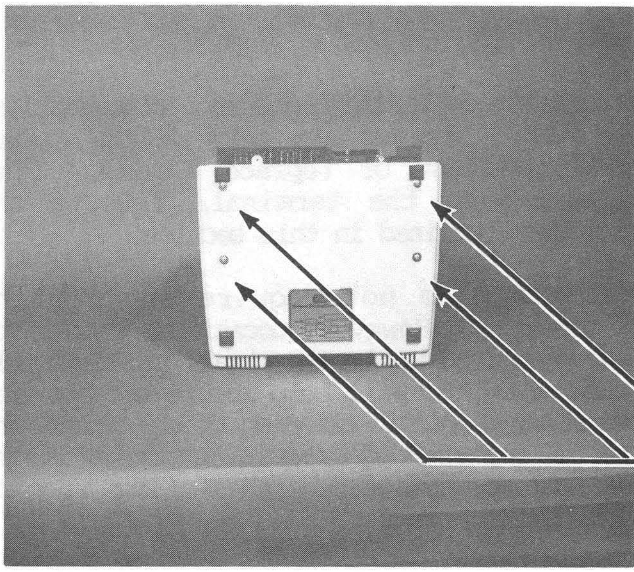
Turn off the power. Unplug the keyboard, the data cable, the printer cable, and the power cable.



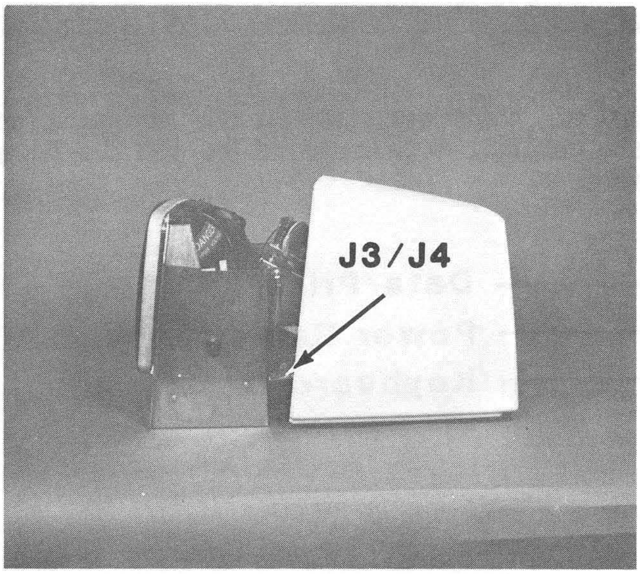


Remove two bezel mounting screws from the top and two screws from the bottom.

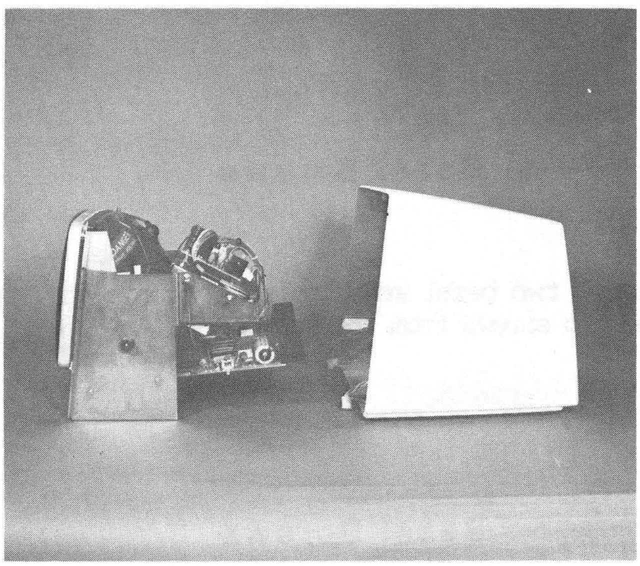
4.2 REMOVING THE MOUNTING FRAME



To remove the frame from the rear housing, remove the four bottom mounting screws.

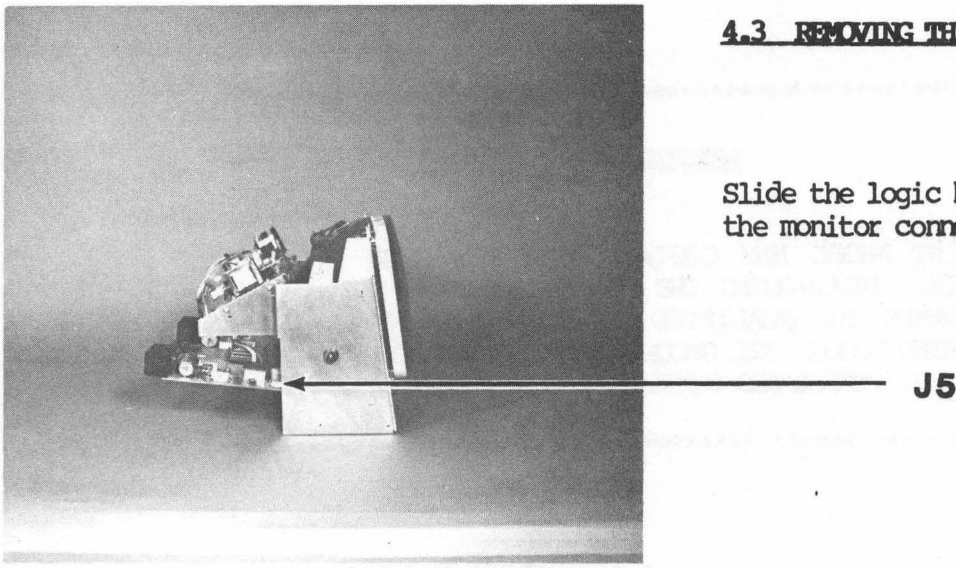


Pull the frame out as far as possible. Reach in and unplug the transformer connectors J3 and J4 connected to the right rear and left rear of the logic control board.

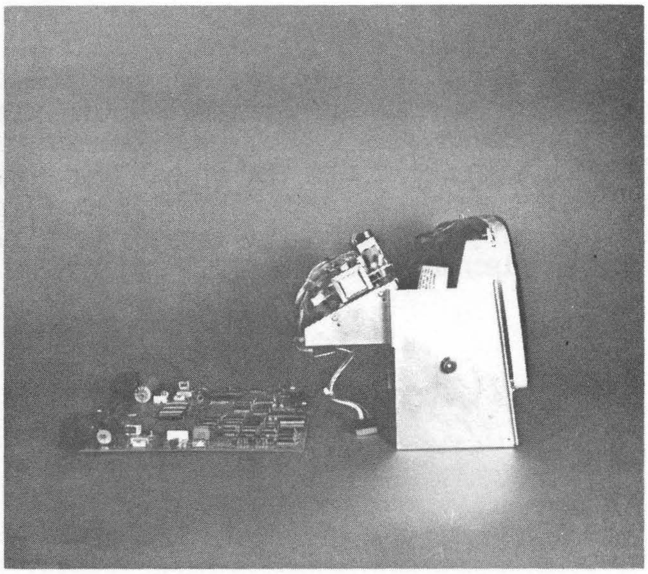


After unpluging the cables, pull the frame forward and free of the rear housing.

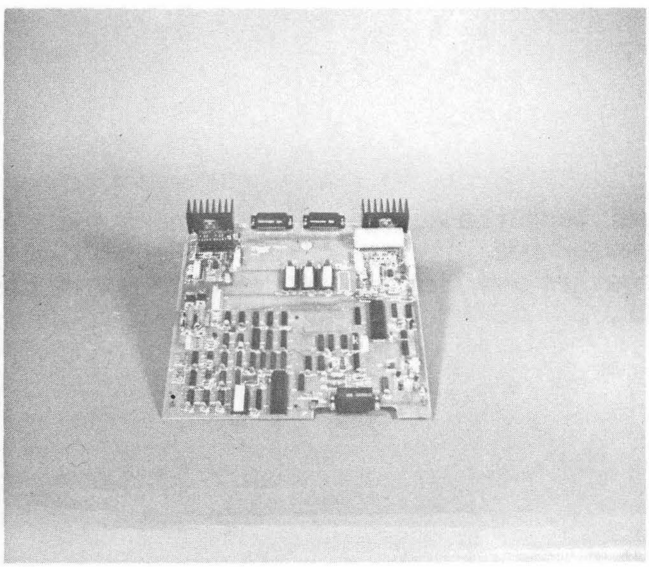
4.3 REMOVING THE LOGIC CONTROL BOARD



Slide the logic board back far enough to expose the monitor connector J5. Unplug J5.



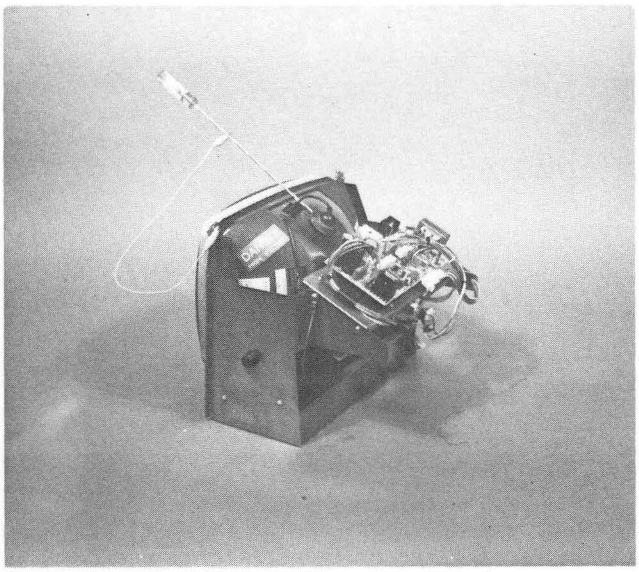
Slide the logic board out toward the rear.



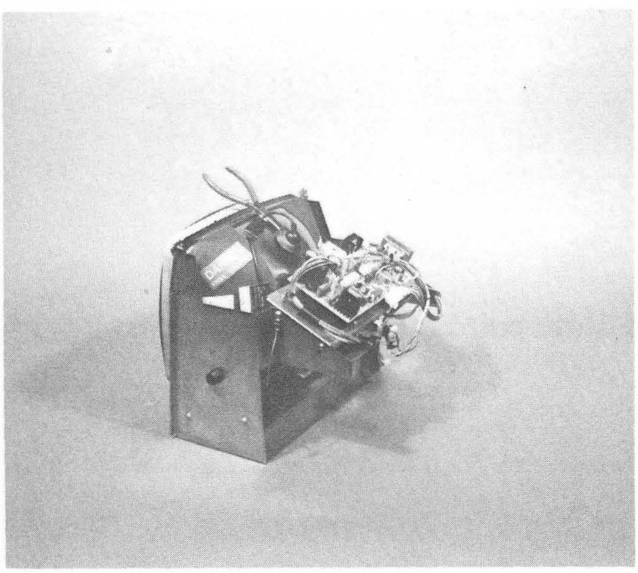
The logic board after removal.

```
*****************************************************************
*                                                               *
*                           WARNING                             *
*                                                               *
*                                                               *
*       THE CRT ANODE MAY CONTAIN A STORED HIGH                 *
*       VOLTAGE. DISCHARGING THE CRT SHOULD ONLY BE             *
*       PERFORMED BY QUALIFIED PERSONNEL USING                  *
*       INSULATED TOOLS. ALL GROUNDS MUST BE CONNECTED          *
*       TO INSURE PROPER AND COMPLETE DISCHARGING.              *
*                                                               *
*****************************************************************
```

4.4 REMOVING THE CRT

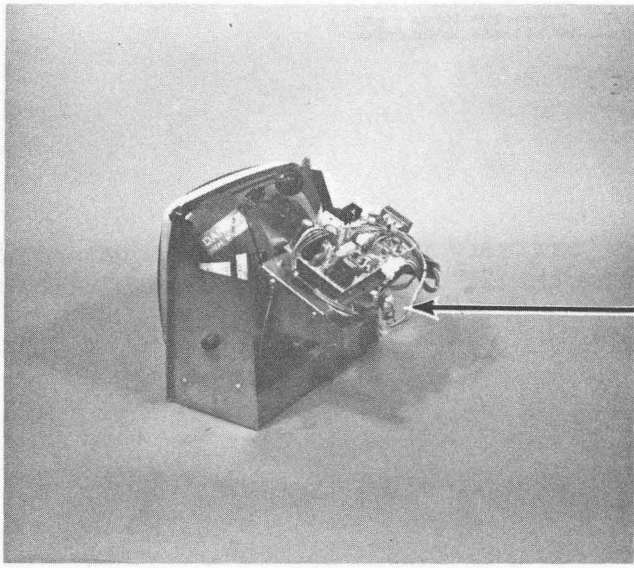


Clip one end of the test lead to the shaft of an insulated handle screwdriver and the other end to one of the CRT mounting brackets. Carefuly slip the tip of the screwdriver under the rubber anode cap. Touch the contact clips and hold in place for a few seconds to allow complete discharging of the CRT.



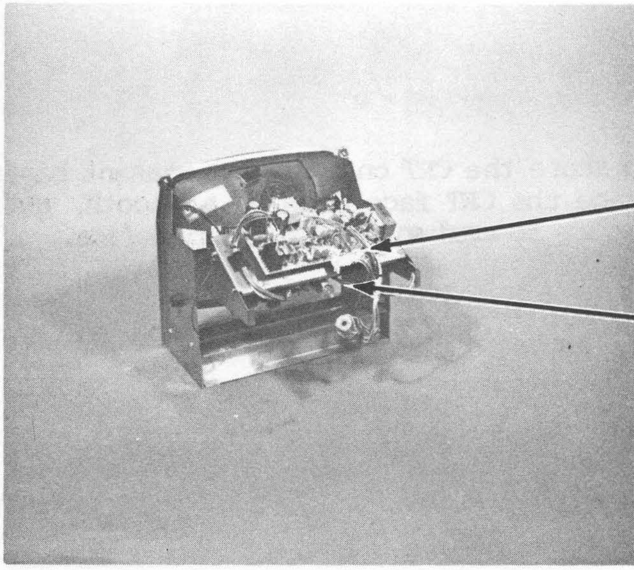
Peel back the rubber cap. Using a pair of needle-node pliers, squeeze the contact clip together and lift the anode lead free of the CRT.

4.4 REMOVING THE CRT (Cont)



CRT Cathode Connector

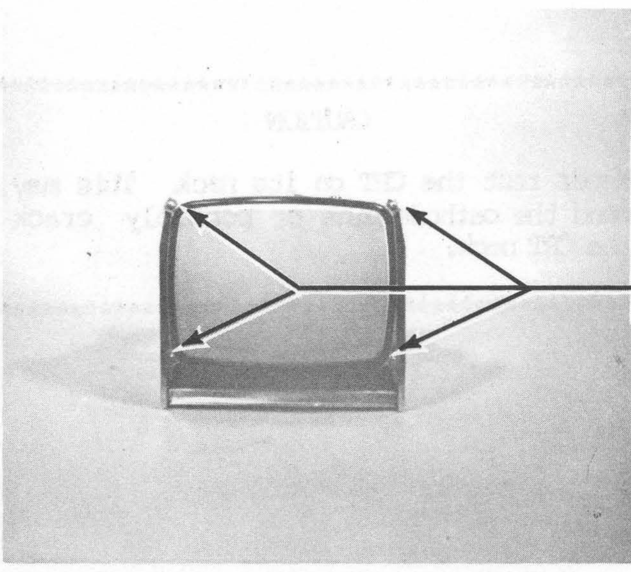
Unplug the CRT cathode connector.



Ground Wire

Yoke Connector

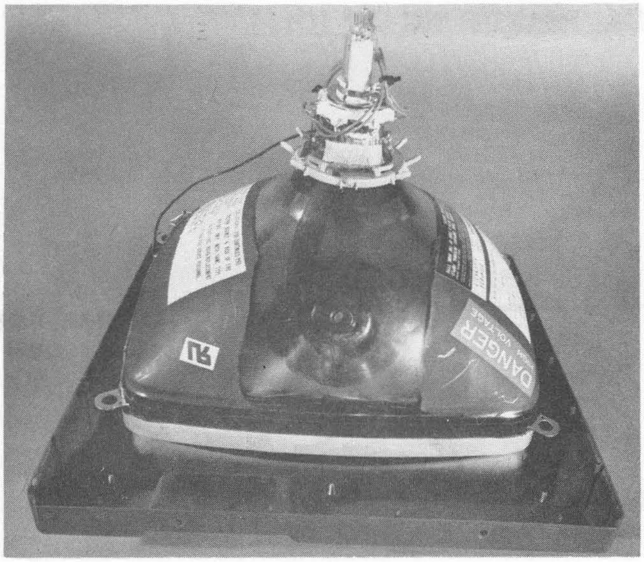
Unplug the yoke cable and the CRT ground wire from the monitor control board.



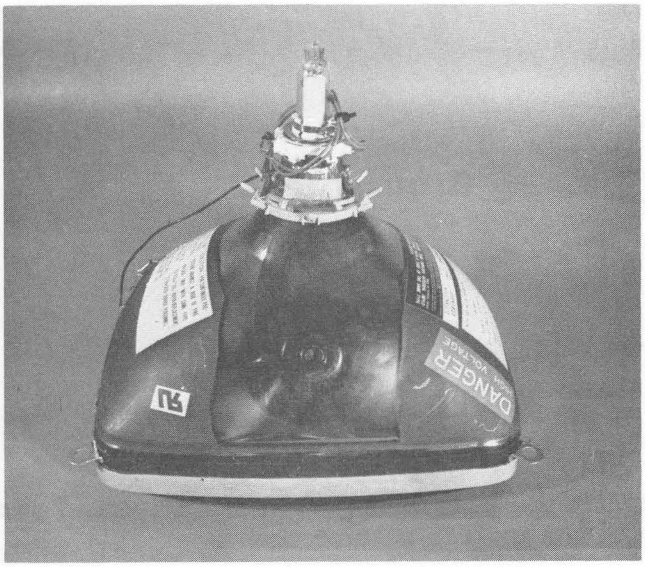
Mounting Screws (4)

Remove the four corner mounting screws holding the CRT in the frame. Be sure the CRT is firmly supported when removing the screws. Avoid banging the neck of the CRT against the frame.

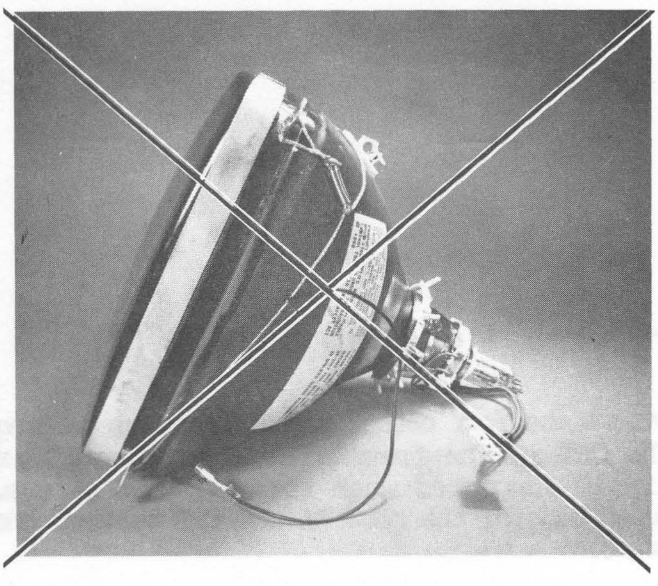
4.5 STORING THE CRT



For temporary storage during terminal repair, place the CRT face down inside the front bezel.



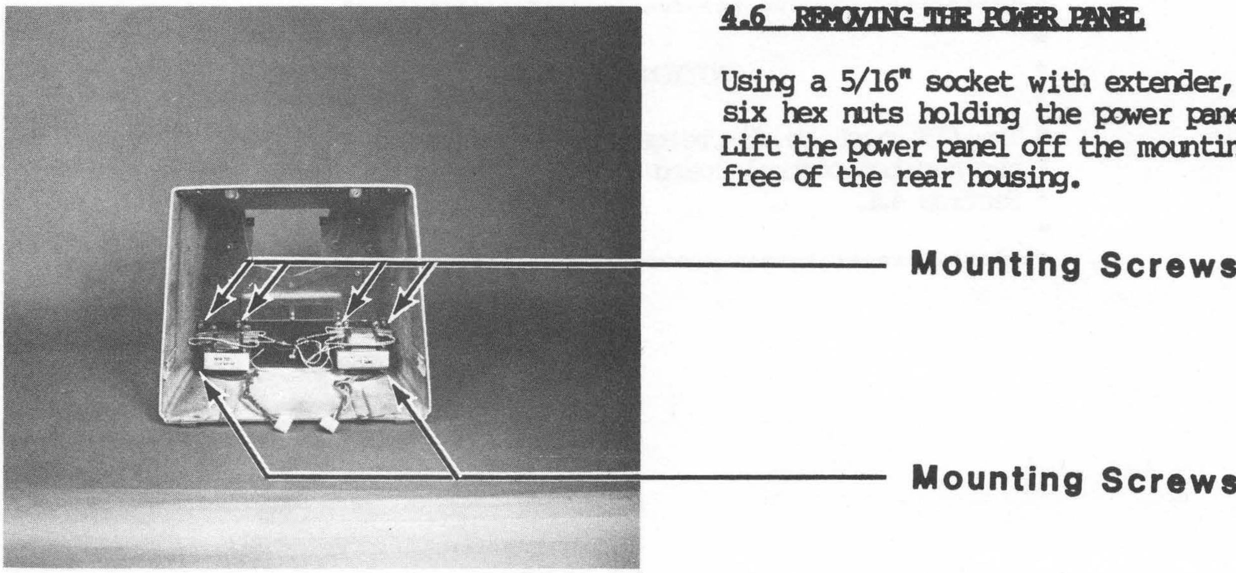
To store the CRT on a more permanent basis, place the CRT face down on a smooth, soft, surface to avod scratching the tube face.

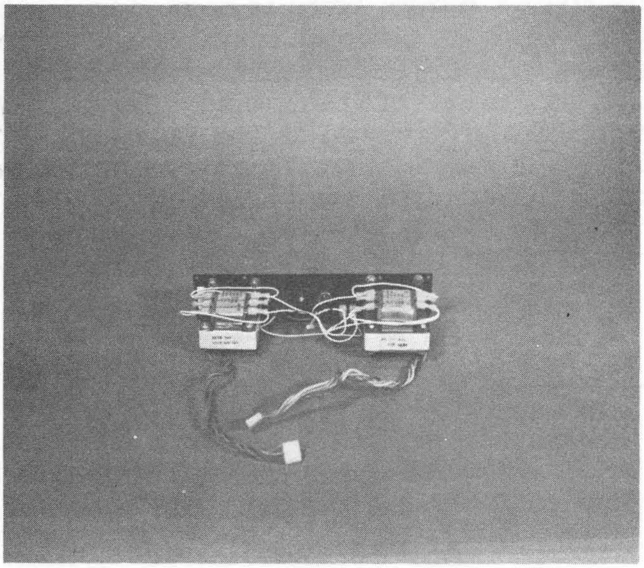


****
*   CAUTION   *
*   *
* Never rest the CRT on its neck. This may *
* bend the cathode pins or possibly crack *
* the CRT neck. *
*   *
****

4.6 REMOVING THE POWER PANEL

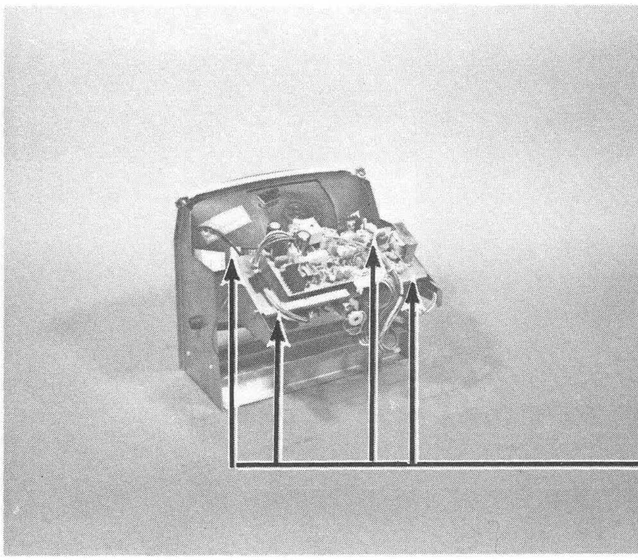
Using a 5/16" socket with extender, remove the six hex nuts holding the power panel in place. Lift the power panel off the mounting posts and free of the rear housing.





The power panel after removal.

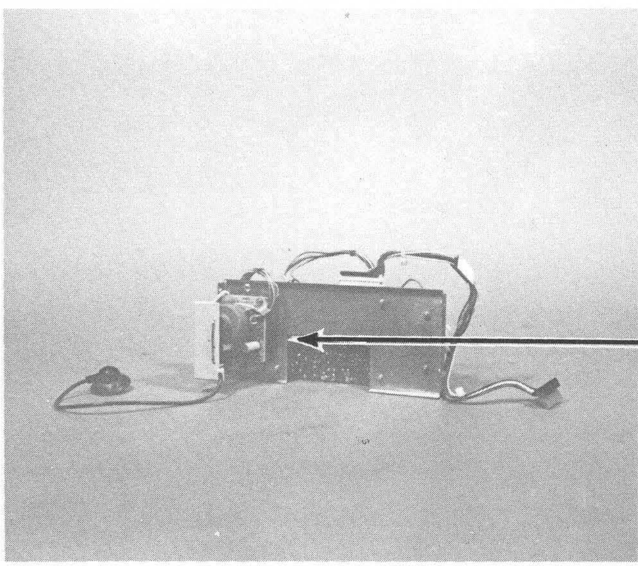
```
**************************************************
*                                                *
*                    CAUTION                     *
*                                                *
* The CRT must be discharged before removing     *
* the monitor control board assembly.  Refer to  *
* Section 4.4.                                   *
*                                                *
**************************************************
```



Mounting Screws

4.7 REMOVING THE MONITOR CONTROL BOARD

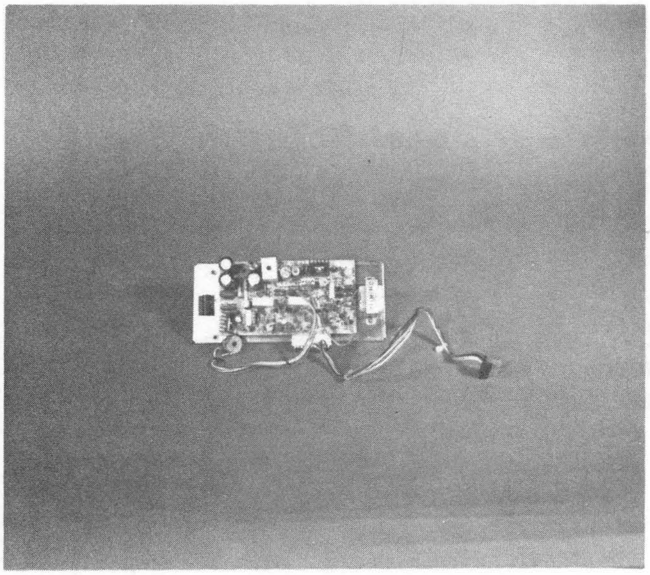
The monitor control board is mounted to a metal plate which is attached to the frame by four screws. The flyback transformer is mounted to the underside of the metal plate. Both assemblies are removed at the same time. The flyback transformer may then be separated from the monitor control board assembly.



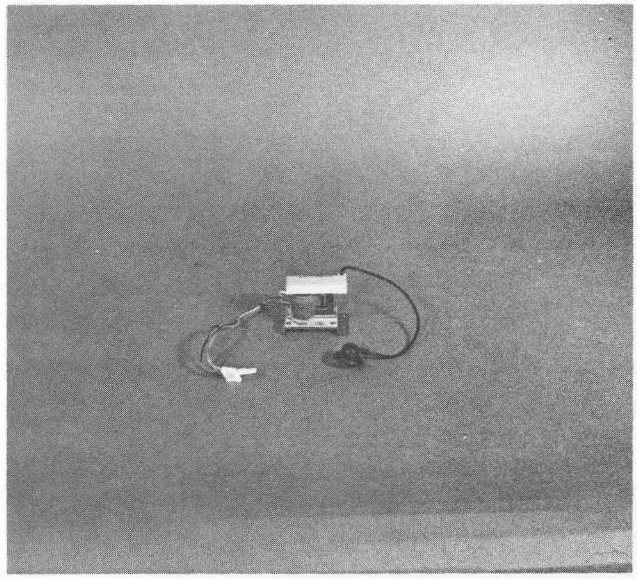
Flyback Transformer

To separate the flyback transformer from the monitor control board, unplug connectors CN3 and CN4. Remove the top screw and loosen the bottom screw. Slip the transformer off the bottom screw.

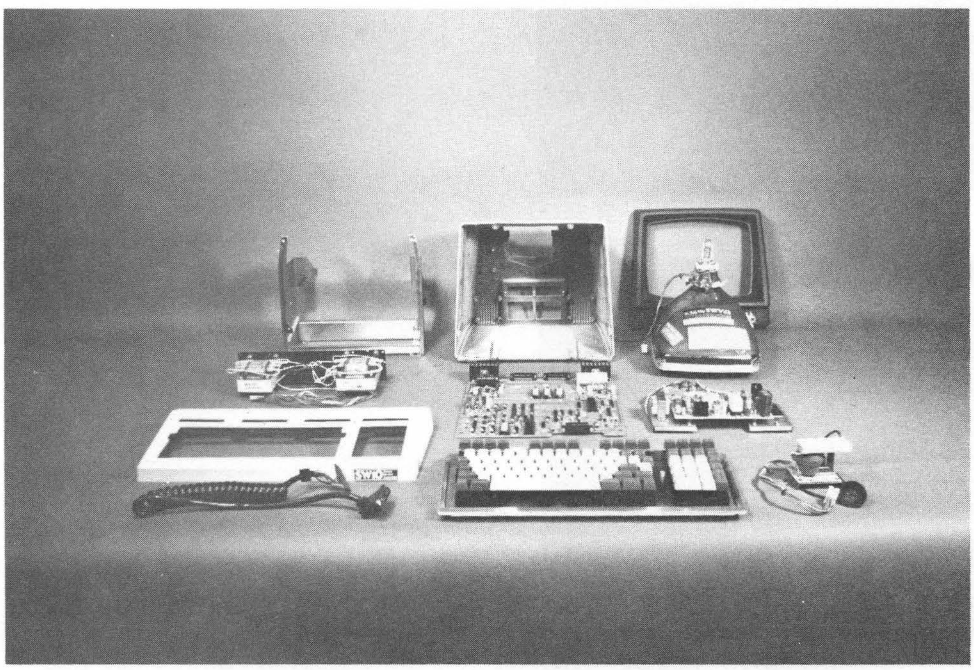
4.7 MONITOR AND CONTROL BOARD (Cont.)



The monitor control board after removal.

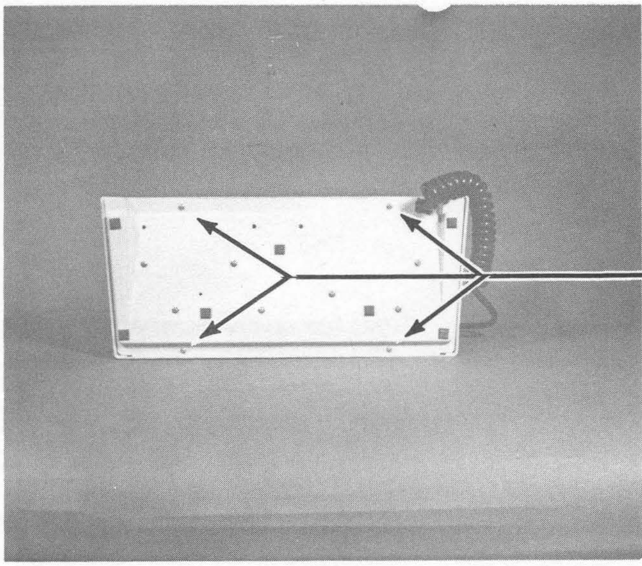


The flyback transformer after removal.



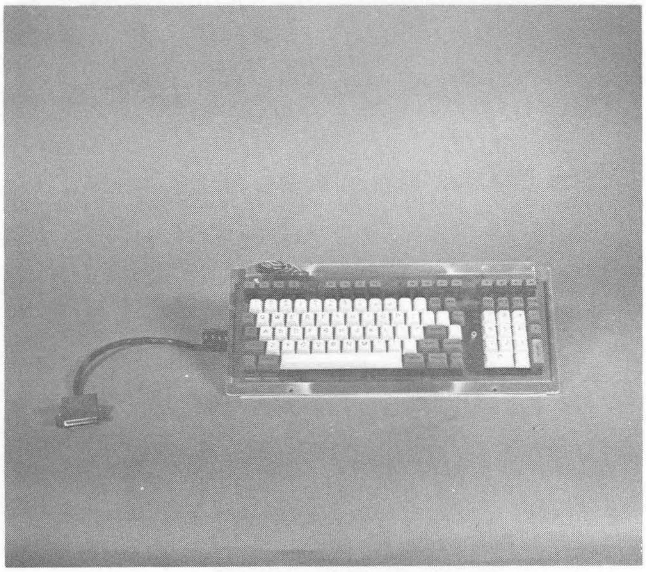
SW10 MAJOR SUB-ASSEMBLIES

4.8 DISASSEMBLY OF THE KEYBOARD

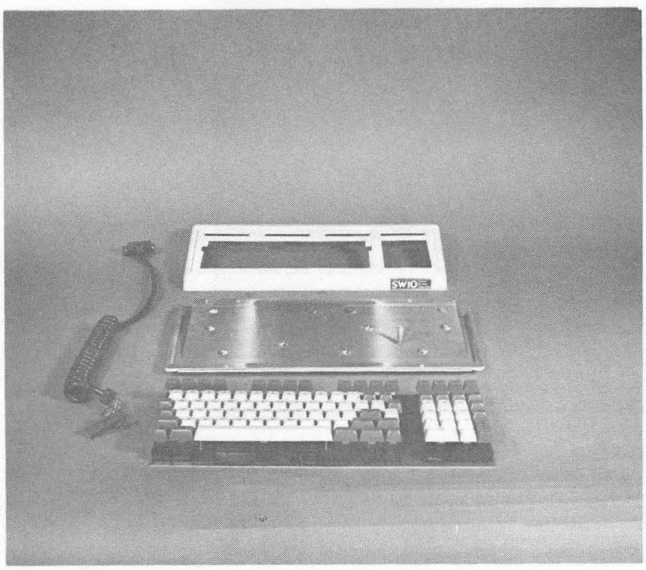


Bezel Screws

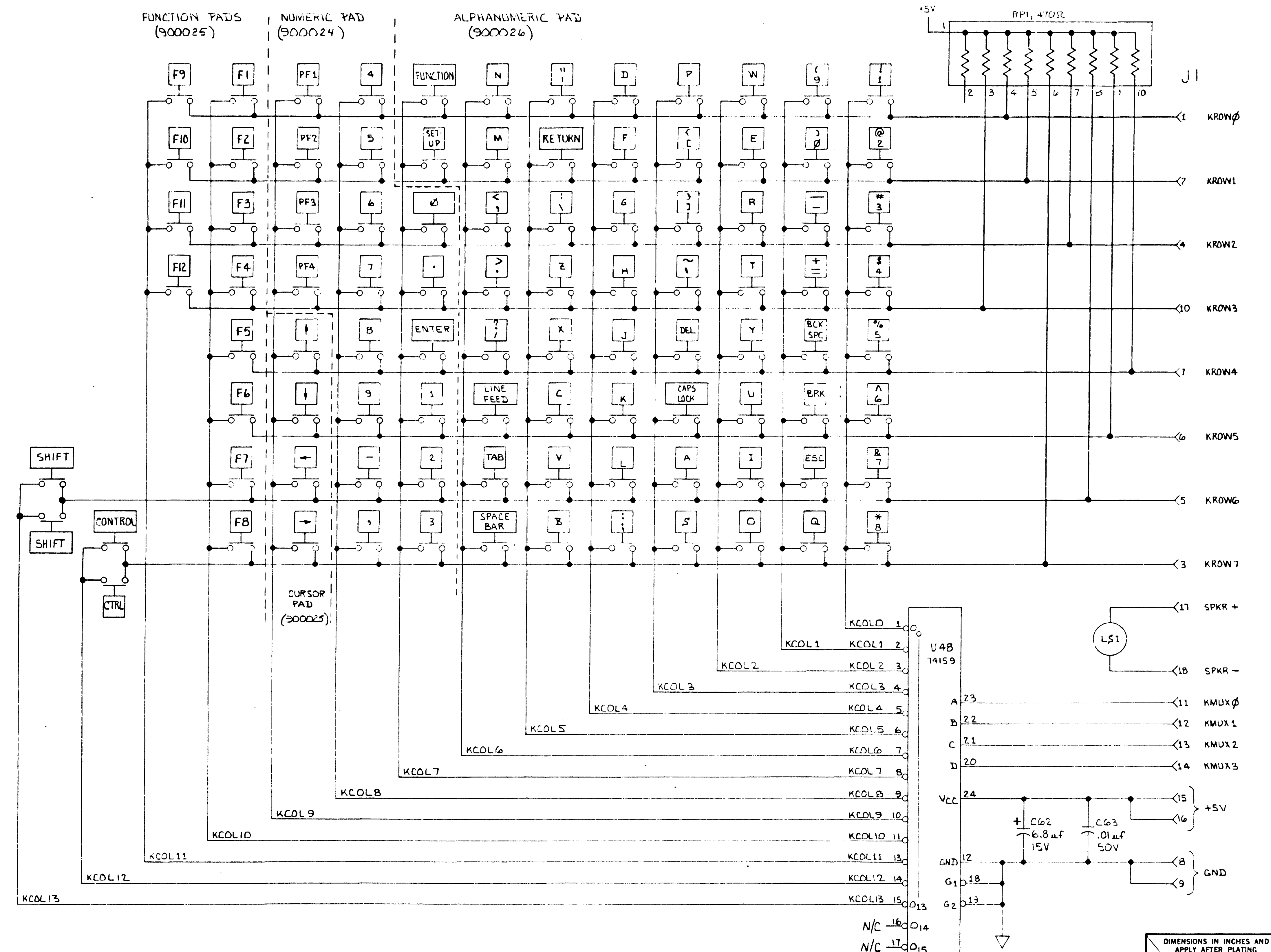
The keyboard bezel is held in place by four screws accessable from the bottom. The keyboard PC board is mounted with seven screws.



The keyboard with the bezel removed.



The disassembled keyboard.



REV	DESCRIPTION	DATE	APPR.
[illegible]	ENGINEERING RELEASE PER DRN 0572	[illegible]	[illegible]
02	[illegible]	[illegible]	[illegible]
03	REVISED PER ECO 2490 DRN 0639	[illegible]	[illegible]
04	REVISED PER ECO [illegible] DRN 0755	[illegible]	[illegible]
05	REVISED PER ECO 2633, DRN 0775	[illegible]	[illegible]
A	PRODUCTION RELEASE PER ECO 2616 DRN 0791	4/82	LB
B	REVISED PER ECO 2650, DRN 0823	[illegible]	[illegible]

DIMENSIONS IN INCHES AND APPLY AFTER PLATING REMOVE BURRS & SHARP EDGES

TOLERANCE UNLESS SPECIFIED
DECIMALS .XX ± .03 .XXX ± .010
ANGLES ± 0°30'

MATERIAL:

FINISH:

DO NOT SCALE DRAWING

DRAWN: [illegible] DATE: [illegible] 12, 81
CHECKED: J BERGE 22APR81
APPR: [illegible] 10-20-81
APPR: [illegible] 10/19/81
MODEL NO. SW10
NEXT ASSY 750002

GTC
General Terminal Corporation

TITLE: SCHEMATIC, SW-10, DETACHED KEYBOARD

SIZE: D
DRAWING NO. 720002-001
REV: B
SCALE: NONE
SHT 1 OF 1

IC NO.	IC TYPE	GND PIN	+5V PIN	LOCATION(S)
U1	LM376	4	—	2D3
U2	LM376	4	—	2C3
U3	74Ø6	7	14	5B1(4), 5B2, 5C2
U4	74LSØ4	7	14	3B6, 346, 4B7, 4A7, 5D5, 5D2
U5	74LSØ8	7	14	1C3, 4C6, 4A6, 5D4
U6	74LSØØ	7	14	4B7, 4B6, 4C3(2)
U7	74LS1Ø	7	14	4B6, 4C8, 4C3
U8	2716	12	24	3C5
U9	2732	12	24	3C4
U10	2732	12	24	3C3
U11	74LS273	10	20	3C6
U12	Z8681	11	1	3C7
U13	74LS139	8	16	3D4
U14	74LSØØ	7	14	5B2, 5D2, 5D4(2)
U15	74LS32	7	14	3B6, 4C5, 5B2, 5A6
U16	MM5Ø34	11	22	5D7
U17	DP83Ø4	10	20	3B2
U18	74LS273	10	20	5B2
U19	MM2114	9	15	4D4
U20	MM2114	9	18	4D5
U21	74LS367	8	16	3D8, 3C8
U22	NC7Ø33	2	—	3D2
U23	MC1489	7	14	5C7, 5B7, 5A7(2)
U24	MCT21Ø	—	—	5B5
U25	74LSØ8	7	14	5A6, 5C3(2), 5D2
U26	74S74	7	14	4A6, 5D4
U27	MM2114	9	18	4A4
U28	MM2114	9	18	4A2
U29	MM2114	9	18	4A3
U30	MM2114	9	18	4A5
U31	74LS367	8	16	4D7
U32	74LS367	8	16	4D6
U33	74LS273	10	20	4D3
U34	74LS32	7	14	3D5
U35	74LS906	7	14	3D3(6)
U36	MC1488	7	—	5A5(2), 5B5(2)
U37	MCT21Ø	—	—	5B7
U38	74S86	7	14	5C3, 5C2(2), 5D4
U39	74S74	7	14	5C4, 5D4
U40	74LS14	7	14	3B8(3), 3C8, 4B6(2)
U41	2716	12	24	3C2
U42	74LS153	8	16	5A6
U43	74LS153	8	16	5B6
U44	74165	8	16	5D5
U45	2716	12	24	5D6
U46	74LS273	10	20	5D7
U47	DP8369	20	40	4A7
U48	74LS05	7	14	1C3(2), 3A8, 3A7(2), 3D6

IC LOCATOR AND POWER MATRIX

REF DESIGNATIONS	
LAST	UNUSED
C63	——
CR23	CR11
E32	——
Q10	——
R57	——

JUMPER LIST

FROM	TO	STD	FUNCTION	
E1	E2		SEE SHT 2 (D1)	
E3	E4		RST1 (CPU ORG AT ØØØØ)	
E4	E5	ETCHED	RST1* (CPU ORG AT Ø8ØØ) (3B7)	
E6	E7		REVERSE VIDEO	CHARACTER ATTRIBUTE OPTIONS (5C4)
E9	E10		REVERSE VIDEO	CHARACTER ATTRIBUTE OPTIONS (5C4)
E6	E8	✓	HALF-INTENSITY	CHARACTER ATTRIBUTE OPTIONS (5C4)
E10	E11	✓	HALF-INTENSITY	CHARACTER ATTRIBUTE OPTIONS (5C4)
E6	E8		REVERSE VIDEO AND HALF-INTENSITY	CHARACTER ATTRIBUTE OPTIONS (5C4)
E9	E10		REVERSE VIDEO AND HALF-INTENSITY	CHARACTER ATTRIBUTE OPTIONS (5C4)
E12	E13	✓	60 HZ	50/60 HZ (4A8)
E12	E14		50 HZ	50/60 HZ (4A8)
E15	E16	✓	STD PRINTER	PRINTER OPTION (5C7)
E15	E17		NEC SPINWRITER	PRINTER OPTION (5C7)
E18	E19	✓	2716	U8 PROGRAM MEMORY (3C5)
E19	E20		2732	U8 PROGRAM MEMORY (3C5)
E21	E22		2716	U9 PROGRAM MEMORY (3C4)
E22	E23	✓	2732	U9 PROGRAM MEMORY (3C4)
E24	E25		2716	U10 PROGRAM MEMORY (3C3)
E25	E26	✓	2732	U10 PROGRAM MEMORY (3C3)
E27	E28	✓	2716	U41 PROGRAM MEMORY (3C2)
E28	E29		2732	U41 PROGRAM MEMORY (3C2)
E30	E31		EXTERNAL CURRENT SOURCE	
E31	E32	✓	INTERNAL CURRENT SOURCE	

J1 (5B8),(5B4)
MAIN PORT

1 FRAME GND
2 XMIT DATA
3 RECV DATA
4 RTS
5 CLEAR TO SEND
6 NC
7 GND
8 NC
9
10
11
12
13
14
15
16 NC
17 CL OUT +
18 NC
19 NC
20 DTR
21 NC
22 NC
23 CL IN +
24 CL OUT −
25 CL IN −

J2 (5C8),(5B4)
PRINTER PORT

1 FRAME GND
2 AUX RECV
3 PRINT DATA
4 NC
5 CTS
6 DSR
7 GND
8 CD
9 NC
10
11
12
13
14
15
16
17
18 NC
19 SC RTS
20 AUX DTR
21 NC
22
23
24
25 NC

J3 (2D4)
T1 XFMR

1 FRAME GND
2 NC
3 T1
4 NC
5 T1

J4 (2C4)
T2 XFMR

1 T2
2 T2
3 T2
4 NC
5 T2

J5 (5D1)
MONITOR CONTROL BOARD

1 FRAME GND
2 +15V
3 GND
4 VIDEO GND
5 VIDEO DATA
6 VERT SYNC
7 HORZ SYNC

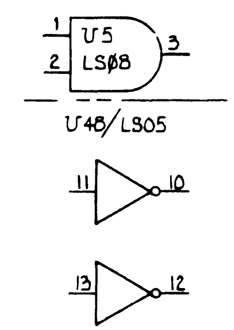
J6 (3D8),(4D1)
KEYBOARD

1 GND
2 KROW 3
3 KMUX 3
4 KMUX 1
5 SPKR −
6 NC
7 NC
8 NC
9 SPKR +
10 KROWØ
11 KROW4
12 KROW6
13 +5V
14 GND
15 KROW2
16 KMUX2
17 KMUXØ
18 FRAME GND
19 NC
20 NC
21 NC
22 KROW 1
23 KROW 5
24 KROW 7
25 +5V

J7

1 FRAME GND

UNUSED ICS



REV	DESCRIPTION	DATE	APPR.
01	ENGINEERING RELEASE PER DRN 0704	[illegible]	LP
02	REVISED PER ECO 2578, DRN 0705	19FEB82	JB
03	REVISED PER ECO 2632, DRN 0768	4/82	LB
04	REVISED PER ECO 2638 DRN 0769	4/82	LB
A	PRODUCTION RELEASE PER ECO 2616 DRN 0791	4/82	LB
B	REVISED PER ECO 2658, DRN 0829		

NOTES: UNLESS OTHERWISE SPECIFIED

1. OMIT E1 TO E2 WIRE JUMPER UNTIL THE +5DC POWER CIRCUIT IS PROPERLY ADJUSTED. (2D1)
2. RESISTORS ARE READ IN OHMS ±5%, 1/4 W.
3. JUMPER SHOW STANDARD VERSION (-001). REFER TO JUMPER LIST.
4. R1 & R8 CAN BE RESISTORS RANGING IN VALUE FROM .619 Ω ±5%, 3W TO .680 Ω ±5%, 3W DEPENDING ON AVAILABILITY.
5. THESE ARE "FACTORY SELECT RESISTORS" REFER TO TEST PROCEDURES.

DIMENSIONS IN INCHES AND APPLY AFTER PLATING
REMOVE BURRS & SHARP EDGES

TOLERANCE UNLESS SPECIFIED
DECIMALS .XX ± .03, .XXX ± .010
ANGLES ± 0°30'

MATERIAL:

FINISH.

DO NOT SCALE DRAWING

DRAWN: JAY S LYNCH — DATE: FEB 17, 82
CHECKED: BERGE — 19FEB82
APPR.: [illegible] — 19 FEB 82
APPR.: [illegible] — 2-19-82
MODEL NO.:
NEXT ASSY: SW

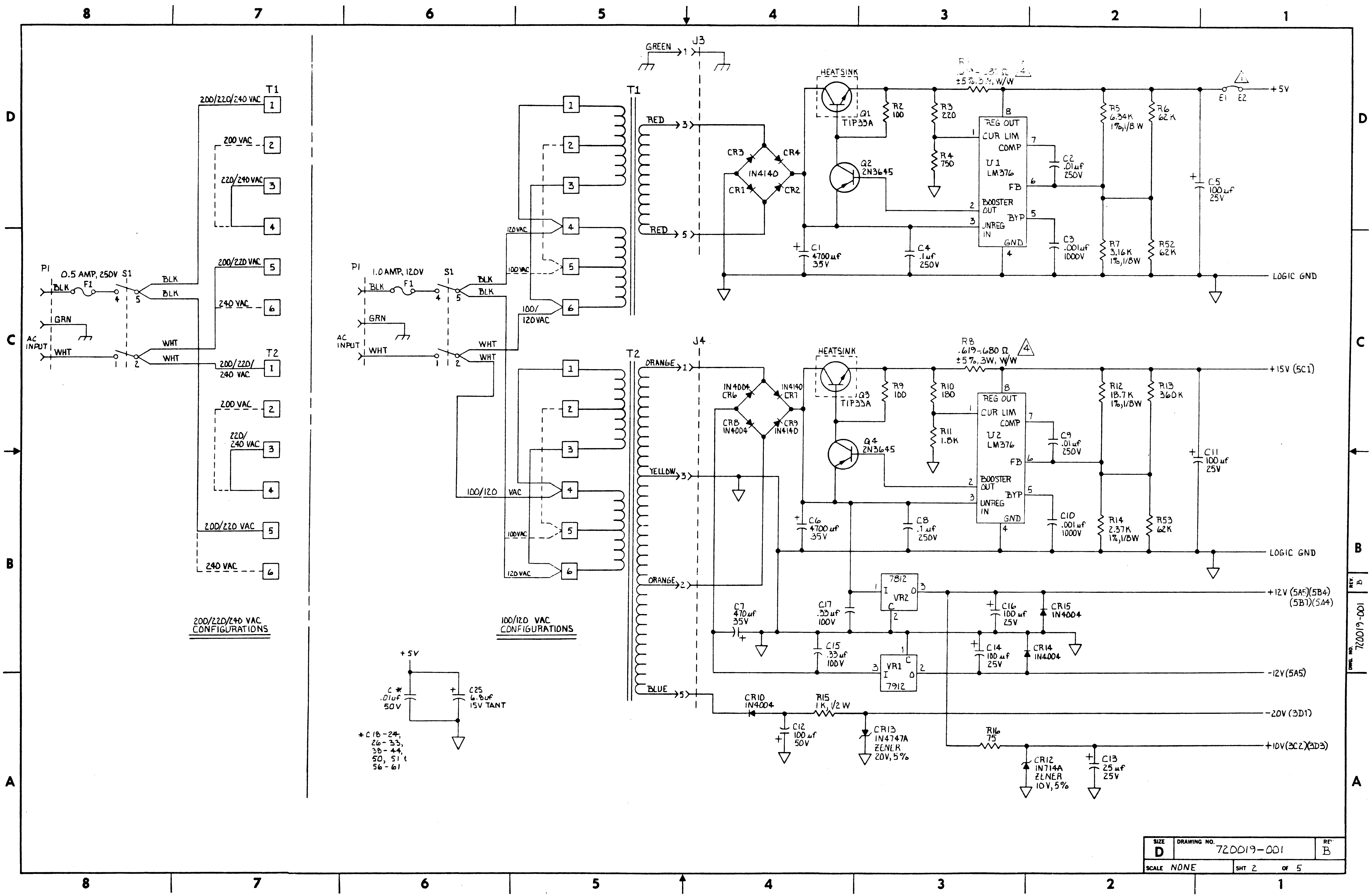
GTC
General Terminal Corporation

TITLE: SCHEMATIC ROMLESS CONTROL PCB SW-10

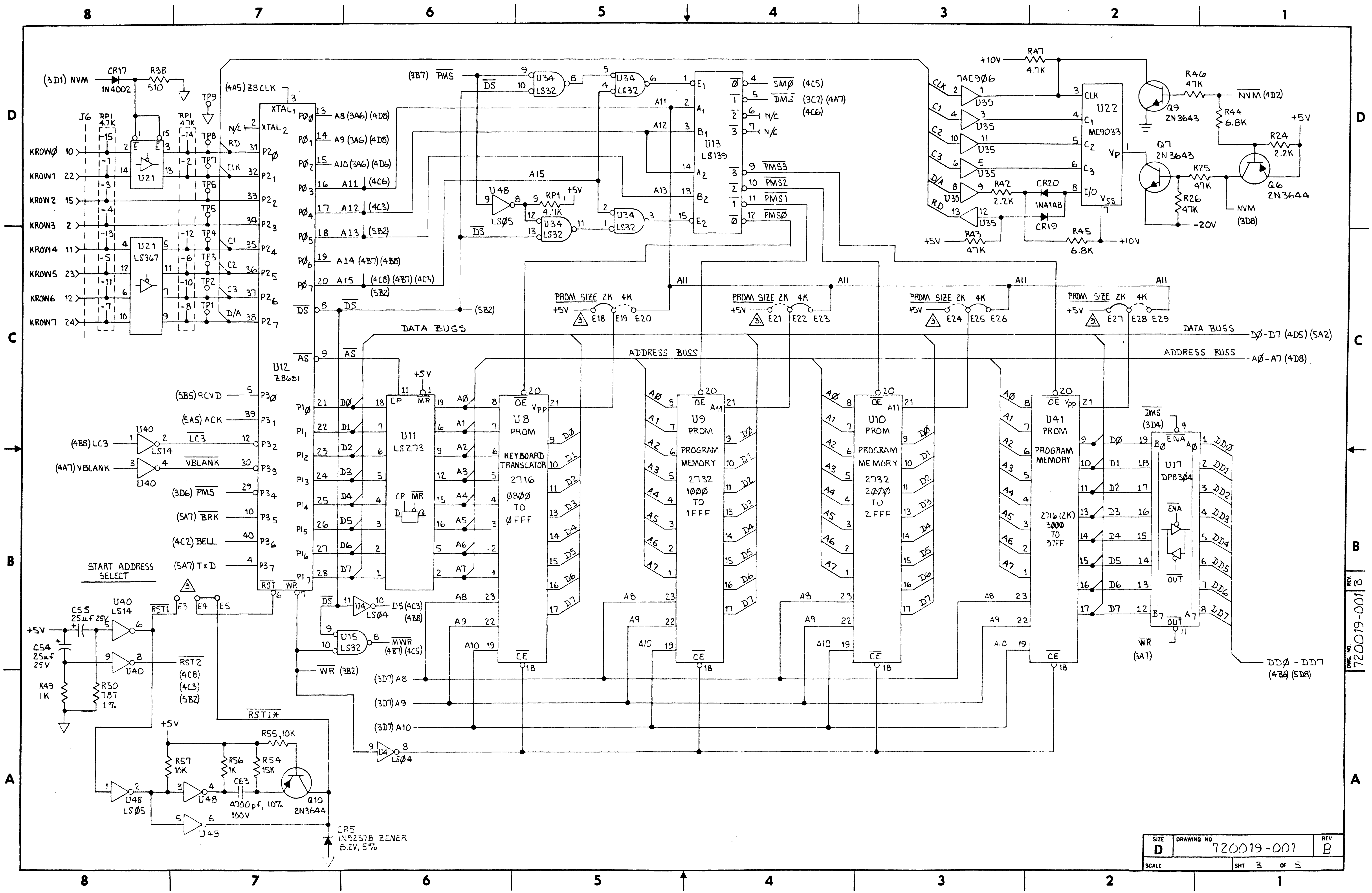
SIZE: D — DRAWING NO. 720019-001 — REV B

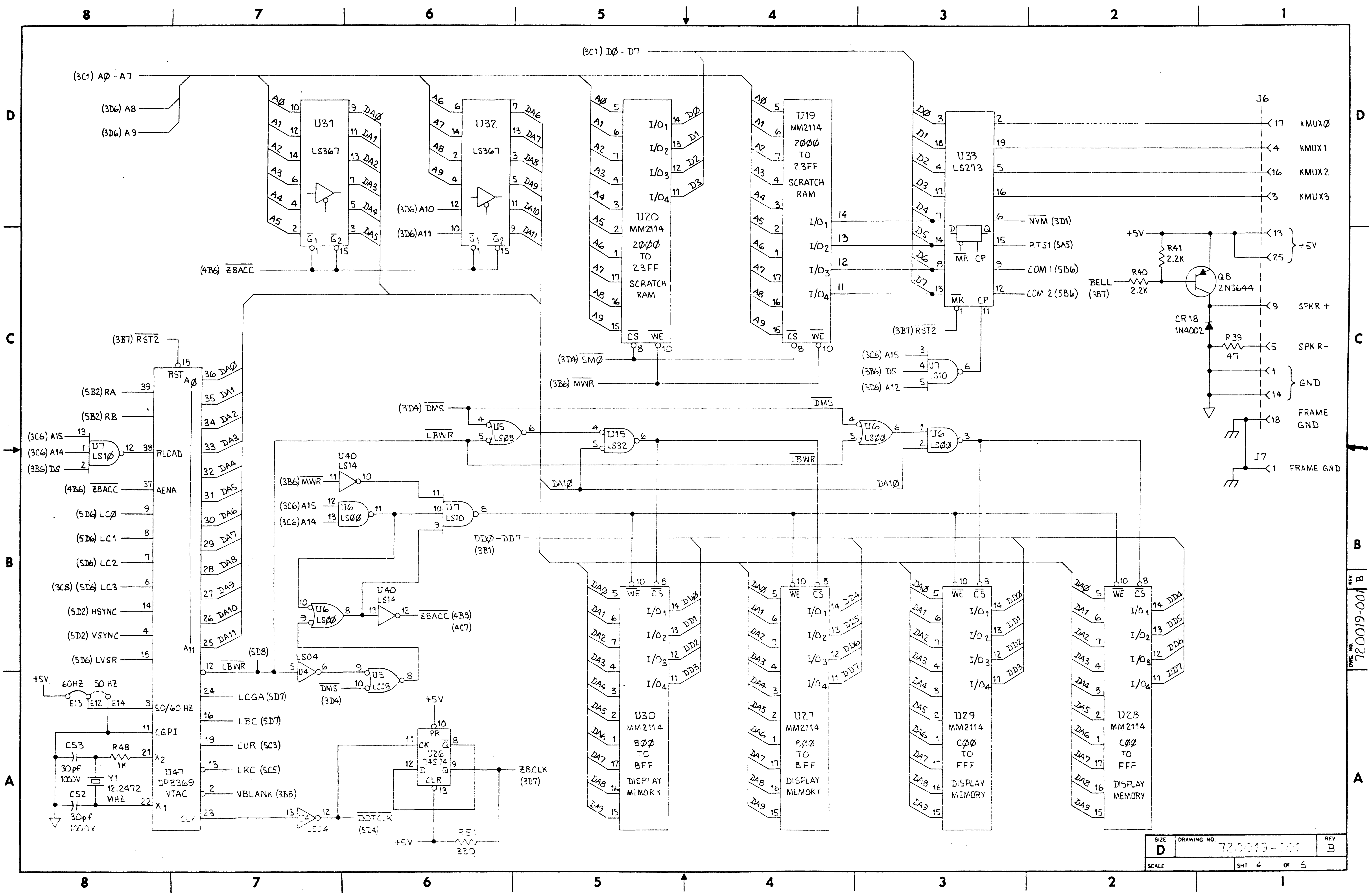
SCALE NONE — SHT 1 OF 5

DWG. NO. 720019-001 REV B

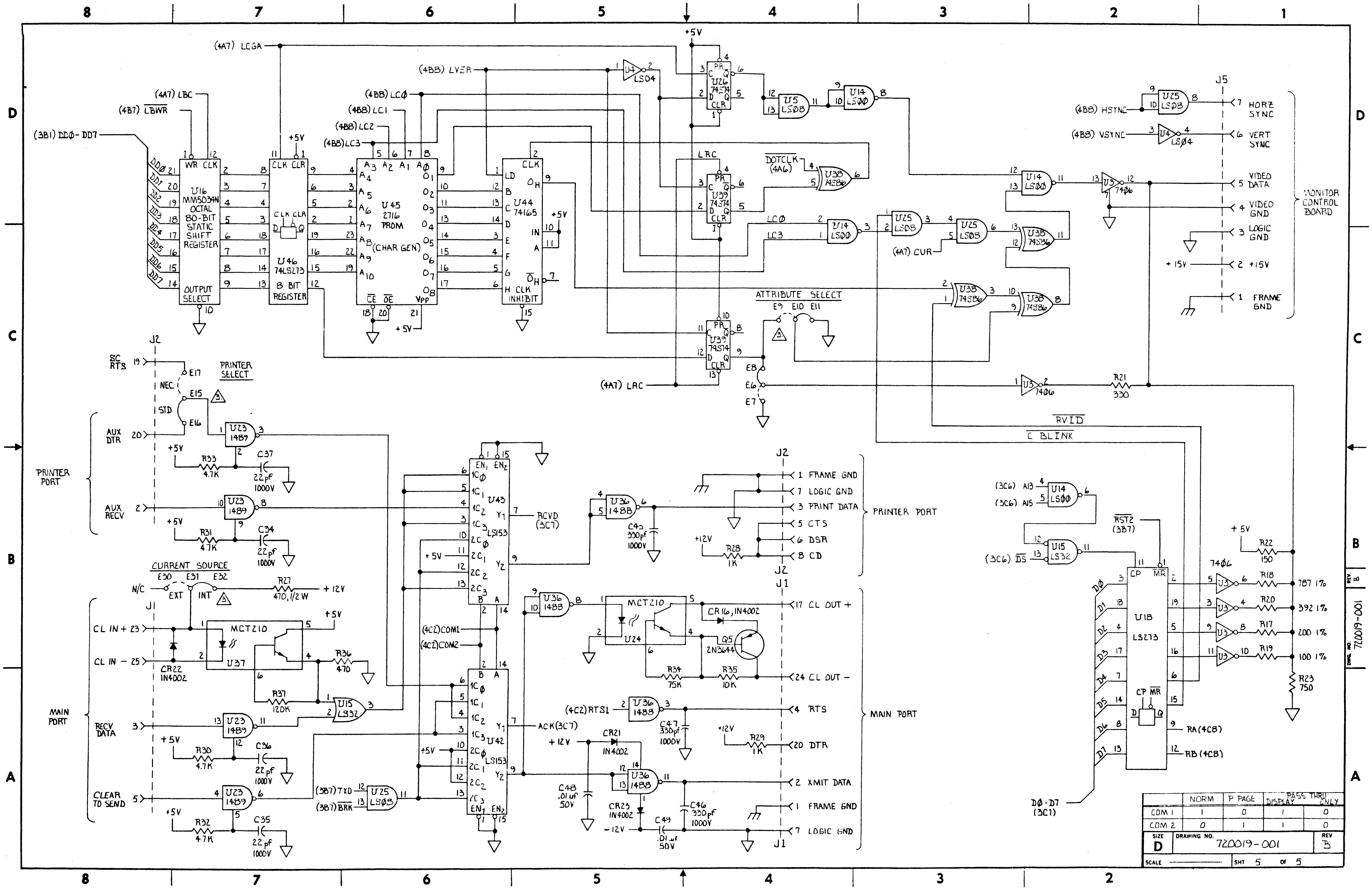


200/220/240 VAC CONFIGURATIONS
100/120 VAC CONFIGURATIONS
P1
0.5 AMP, 250V
1.0 AMP, 120V
S1
F1
BLK
GRN
WHT
AC INPUT
T1
T2
200/220/240 VAC
200 VAC
220/240 VAC
200/220 VAC
240 VAC
200/220/ 240 VAC
220/ 240 VAC
120VAC
100VAC
100/ 120VAC
100/120 VAC
J3
J4
GREEN
RED
ORANGE
YELLOW
BLUE
HEATSINK
Q1 TIP33A
Q2 2N3645
Q3 TIP33A
Q4 2N3645
CR1 CR2 CR3 CR4 IN4140
IN4004 CR6
IN4140 CR7
CR8 IN4004
CR9 IN4140
R1 .619-.680 Ω ±5%, 3W, W/W
R8 .619-.680 Ω ±5%, 3W, W/W
R2 100
R3 220
R4 750
R5 6.34K 1%, 1/8 W
R6 62K
R7 3.16K 1%, 1/8W
R52 62K
R9 100
R10 180
R11 1.8K
R12 18.7K 1%, 1/8W
R13 360K
R14 2.37K 1%, 1/8W
R53 62K
U1 LM376
U2 LM376
REG OUT
CUR LIM
COMP
FB
BOOSTER OUT
UNREG IN
BYP
GND
C1 4700 uf 35V
C2 .01 uf 250V
C3 .001 uf 1000V
C4 .1 uf 250V
C5 100 uf 25V
C6 4700 uf 35V
C8 .1 uf 250V
C9 .01 uf 250V
C10 .001 uf 1000V
C11 100 uf 25V
C7 470 uf 35V
C17 .33 uf 100V
C15 .33 uf 100V
C16 100 uf 25V
C14 100 uf 25V
CR15 IN4004
CR14 IN4004
7812 VR2
VR1 7912
CR10 IN4004
R15 1K, 1/2 W
C12 100 uf 50V
CR13 IN4747A ZENER 20V, 5%
R16 75
CR12 IN714A ZENER 10V, 5%
C13 25 uf 25V
E1 E2
+5V
LOGIC GND
+15V (5C1)
+12V (5A5)(5B4) (5B1)(5A4)
-12V (5A5)
-20V (3D1)
+10V (3C2)(3D3)
+5V
C * .01uf 50V
C25 6.8uf 15V TANT
* C18-24, 26-33, 38-44, 50, 51 & 56-61
SIZE D
DRAWING NO. 720019-001
REV B
SCALE NONE
SHT 2 OF 5


U12 Z8681
U13 LS139
U22 MC9033
U8 PROM KEYBOARD TRANSLATOR 2716 Ø8ØØ TO ØFFF
U9 PROM PROGRAM MEMORY 2732 1ØØØ TO 1FFF
U10 PROM PROGRAM MEMORY 2732 2ØØØ TO 2FFF
U41 PROM PROGRAM MEMORY 2716 (2K) 3ØØØ TO 37FF
U11 LS273
U17 DP8304
U21 LS367
DATA BUSS
ADDRESS BUSS
DØ-D7 (4D5) (5A2)
AØ-A7 (4D8)
DDØ-DD7 (4B4) (5D8)
PROM SIZE 2K 4K
START ADDRESS SELECT
CR5 1N5237B ZENER 8.2V, 5%
SIZE D
DRAWING NO. 720019-001
REV B
SCALE
SHT 3 OF 5



(3C1) AØ - A7
(3D6) A8
(3D6) A9
(3C1) DØ - D7
U31 LS367
U32 LS367
(3D6) A10
(3D6) A11
(4B6) Z8ACC
U20 MM2114 2ØØØ TO 23FF SCRATCH RAM
U19 MM2114 2ØØØ TO 23FF SCRATCH RAM
(3D4) SMØ
(3B6) MWR
U33 LS273
(3B7) RST2
(3C6) A15
(3B6) DS
(3D6) A12
U7 LS10
J6
KMUXØ
KMUX1
KMUX2
KMUX3
NVM (3D1)
RTS1 (5A5)
COM 1 (5B6)
COM 2 (5B6)
+5V
R41 2.2K
R40 2.2K
BELL (3B7)
Q8 2N3644
CR18 1N4002
R39 47
SPKR +
SPKR -
GND
FRAME GND
J7
1 FRAME GND
(3B7) RST2
(5B2) RA
(5B2) RB
(3C6) A15
(3C6) A14
(3B6) DS
(4B6) Z8ACC
(5D6) LCØ
(5D6) LC1
(5D6) LC2
(3C8) (5D6) LC3
(5D2) HSYNC
(5D2) VSYNC
(5D6) LVSR
RST
RLOAD
AENA
50/60 HZ
CGPI
U47 DP8369 VTAC
CLK
60HZ 50 HZ
E13 E12 E14
C53 30pf 100V
R48 1K
Y1 12.2472 MHZ
C52 30pf 100V
LBWR (5D8)
LCGA (5D7)
LBC (5D7)
CUR (5C3)
LRC (5C5)
VBLANK (3B8)
DOTCLK (5D4)
(3D4) DMS
U5 LS08
U15 LS32
U6 LS00
U6 LS00
DMS
LBWR
DA1Ø
U40 LS14
(3B6) MWR
(3C6) A15
(3C6) A14
U6 LS00
U7 LS10
U40 LS14
Z8ACC (4B8) (4C7)
DDØ - DD7 (3B1)
U4 LS04
U5 LS08
DMS (3D4)
+5V
U26 74S74
Z8CLK (3D7)
R51 330
U30 MM2114 8ØØ TO BFF DISPLAY MEMORY
U27 MM2114 8ØØ TO BFF DISPLAY MEMORY
U29 MM2114 CØØ TO FFF DISPLAY MEMORY
U28 MM2114 CØØ TO FFF DISPLAY MEMORY
SIZE D
DRAWING NO. 720019-001
REV B
SCALE
SHT 4 OF 5

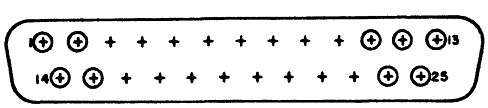


U16 MM5034N OCTAL 80-BIT STATIC SHIFT REGISTER
U46 74LS273 8 BIT REGISTER
U45 2716 PROM (CHAR GEN)
U44 74165
U26 74S74
U39 74S74
U38 74S86
U14 LS00
U25 LS08
U5 LS08
U4 LS04
U3 7406
U18 LS273
U15 LS32
U43 LS153
U42 LS153
U23 1489
U36 1488
U24 MCT210
U37 MCT210
Q5 2N3644
ATTRIBUTE SELECT
PRINTER SELECT
CURRENT SOURCE
PRINTER PORT
MAIN PORT
MONITOR CONTROL BOARD
J5
7 HORZ SYNC
6 VERT SYNC
5 VIDEO DATA
4 VIDEO GND
3 LOGIC GND
2 +15V
1 FRAME GND
J2
1 FRAME GND
7 LOGIC GND
3 PRINT DATA
5 CTS
6 DSR
8 CD
J1
17 CL OUT +
24 CL OUT −
4 RTS
20 DTR
2 XMIT DATA
1 FRAME GND
7 LOGIC GND
CL IN + 23
CL IN − 25
RECV DATA 3
CLEAR TO SEND 5
AUX DTR 20
AUX RECV 2
SC RTS 19
RVID
C BLINK
	NORM	P PAGE	DISPLAY	PASS THRU ONLY
COM 1	1	0	1	0
COM 2	0	1	1	0
SIZE D
DRAWING NO. 720019-001
REV B
SHT 5 OF 5

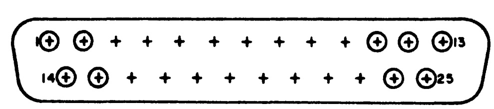
6.0 CABLES AND CONNECTORS

This section shows the internal cables and connectors of the SW10. Connector wiring for the monitor control board to the CRT yoke, cathode and the flyback transformer are shown in the TV Monitor Manual (GTC #05018-001).

Pin	J1 MAIN PORT	Pin	J2 AUX PORT
1	FRAME GND (4A4)	1	FRAME GND (4B4)
2	XMIT DATA (4A4)	2	AUX RECV (4BB)
3	RECV DATA (4AB)	3	PRINT DATA (4B5)
4	RTS (4A4)	4	NC
5	CTS (4AB)	5	CTS (4B4)
6	NC	6	DSR (4B4)
7	GND 4A4	7	GND (4B4)
8	NC	8	CD (4B4)
9	NC	9	NC
10	NC	10	NC
11	NC	11	NC
12	NC	12	NC
13	NC	13	NC
14	NC	14	NC
15	NC	15	NC
16	NC	16	NC
17	CL OUT + (4B4)	17	NC
18	NC	18	NC
19	NC	19	SC RTS (4CB)
20	DTR (4A4)	20	AUX DTR (ACB)
21	NC	21	NC
22	NC	22	NC
23	CL IN + (4BB)	23	NC
24	CL OUT -(4A4)	24	NC
25	CL IN - (5B4)	25	NC

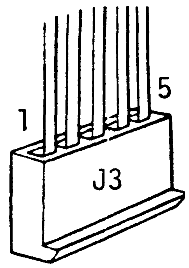


J1



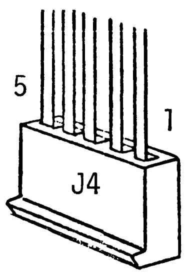
J2

Figure 6-1. Communication Ports



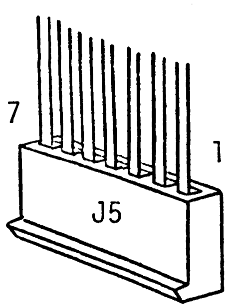
J3 LOGIC BOARD	SIGNAL	LOCATION	T1 POWER PANEL
1	CHASIS GND	2D6	
2	NC		
3	8VAC	2D6	RED
4	NC		
5	8VAC	2D6	RED

Figure 6-2. +5V Transformer to Logic Board



J4 LOGIC BOARD	SIGNAL	LOCATION	T2 POWER PANEL
1	18VAC	2C6	BLACK
2	18VAC	2B6	ORANGE
3	GROUND	2B6	YELLOW
4			NC
5	24VAC	2A6	BLUE

Figure 6-3. +15V Transformer to Logic Board



J5 LOGIC BOARD	SIGNAL	CNØ MONITOR
1	FRAME GROUND	6
2	+15	4
3	LOGIC GROUND	1Ø
4	VIDEO GROUND	1
5	VIDEO DATA	3
6	VERTICAL SYNC	2
7	HORIZONTAL SYNC	5

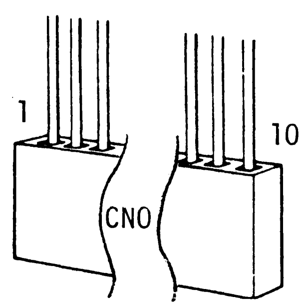
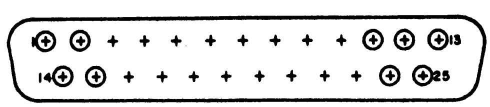


Figure 6-4. Logic Board to Monitor Board

P6 LOGIC BOARD	NAME OF SIGNAL	SCHEMATIC LOCATION	J1 KEYBOARD
1	GROUND	3A1	8
2	KROW3	3D8	10
3	KMUX3	3C1	14
4	KMUX1	3C1	12
5	SPKR-	3A1	18
6	NC		
7	NC		
8	NC		
9	SPKR+	3B1	17
10	KROW0	3D8	1
11	KROW4	3D8	7
12	KROW6	3D8	5
13	+5V	3B1	15
14	GROUND	3A1	9
15	KROW2	3D8	4
16	KMUX2	3C1	13
17	KMUX0	3C1	11
18	NC		
19	NC		
20	NC		
21	NC		
22	KROW1	3D8	2
23	KROW5	3D8	6
24	KROW7	3D8	3
25	+5V	3B1	16



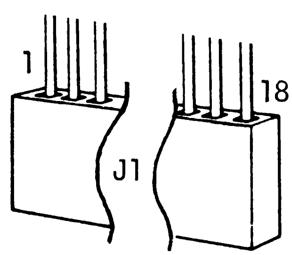


Figure 6-5. Keyboard to Terminal Cable

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7.0 ORDERING AND REPAIRS INFORMATION

This section is divided into four parts: Manual Ordering, Parts Ordering, Items Returned for Repair, and Parts List.

7.1 MANUAL ORDERING

The following manuals on the SW10 are available:

MANUAL NAME	PART #
SW10 Users Manual	970004-001
SW10 Maintenance Manual	970005-002
& TV Monitor Manual (set)	05018-001

Product & pricing information is available from:

General Terminal Corporation
14831 Franklin Avenue
Tustin, CA 92680-7282

(714) 730-0123
(800) 854-6925 (Outside CA)
(800) 432-7006 (Inside CA)
ATTN: Sales Administration

7.2 PARTS ORDERING

Replacement parts may be ordered from GTC. Please provide the following information:

a. Identify our part number and description.
b. Identify part location on PCB.
c. PCB board Assembly No. and Rev. level.
d. Terminal type
e. S/N of terminal.

For example:	Part #	Description
	01000-118	74LS00 NAND GATE

Part Location	PC board Assy & Rev. no.	
U14	750019-001	REV A

f. When ordering PROMs indicate revision level which is typed on the PROM label.

```
For example:                920061-211
                                 :    :
PROM Part No.............:    :
PROM Location & Rev............:
```

g. Parts may be ordered from:

General Terminal Corporation
14831 Franklin Avenue
Tustin, CA 92680-7282

(714) 730-0123
(800) 854-6925 (Outside CA)
(800) 432-7006 (Inside CA)
ATTN: Sales Administration

7.3 ITEMS RETURNED FOR REPAIR

General Terminal Corporation will repair printed circuit boards, subassemblies, or whole terminals under the following guidelines:

GTC has two Field Service Depots. One is located in Tustin, California and the other is in Burlington, Massachusetts.

Items from customers west of the Mississippi River should be sent to the Tustin, CA address and items from customers east of the Mississippi River should be sent to the Massachusetts address.

Both depots are staffed for component level repair of major sub-assemblies or modules. Entire terminals may also be returned for system level repair with the turnaround time for any system or module kept to a MAXIMUM OF SEVEN DAYS in house.

GTC testing includes repair, adjustment and testing at both board and system levels. All modules are put through a 24-hour burn-in cycle. This allows GTC to have a high degree of confidence in all repair work so that a full 90-day warranty is provided on all repairs. Charges for repairs include updating of all equipment returned to our depot facilities.

"In warranty" repair work is done on a no charge basis; however, customers must pay charges for shipping the units to GTC; return transporation is not charged. Out of warranty repair work is billed at current rates. Customers must pay freight charges in both directions. Terms of the warranty are detailed in Figure 7-1.

Limited On-Site Maintenance in specific geographic areas is also available. Terminals may be serviced under a maintenance agreement or on a time and material basis.

Prior to returning any equipment to GTC for repair, customers are required to contact GTC for a return authorization (RA) number. At that time, GTC will need to know the model number of the unit, the serial number of the system (whether a board or an entire system is being returned) and a purchase order number to cover the repair.

Trained technical advisors are on hand to help you determine which element of your terminal is failing and will guide you toward the most expedient repair possible.

If you have concerns about specific maintenance requirements, please contact one of our Field Service Managers and we will custom tailor our service to meet your requirements.

Return Shipment Addresses

WEST COAST:

General Terminal Corporation
14831 Franklin Avenue
Tustin, CA 92680-7282

ATTN: Field Service Manager

EAST COAST:

General Terminal Corporation
12 Esquire Road
North Billerica, MA 01862

ATTN: Field Service Manager

Field Service Telephone Numbers

Inside CA....Field Service.......(714) 730-1659

Inside CA....Main Switchboard....(714) 730-0123

Outside CA and west of
the Mississippi River...........(800) 854-6925

- -

Inside Mass..Main Switchboard....(617) 272-6660

Outside Mass. and east
of the Mississippi River.......(800) 225-0976
(800) 225-0977

WARRANTY

General Terminal Corporation warrants that all the equipment in the Schedule of Equipment, when delivered, will be in good working order per General Terminal Corporation product specification. General Terminal Corporation further warrants the equipment to have been adequately tested and inspected prior to shipment and to be free of all defects in material and workmanship. All component parts of the equipment are warranted for six (6) months from shipment against defects as a result of defective material or workmanship. General Terminal Corporation reserves the right to supply, at its expense, a replacement part to the Customer or return the defective part to General Terminal Corporation's plant for repair. In the event the equipment is to be returned to General Terminal Corporation or a designated Service Center, it must be identified with a Returned Goods Authorization (RGA) number which will be supplied by General Terminal Corporation upon request. Transportation costs for returned equipment and/or parts will be prepaid by the Customer. General Terminal Corporation will pay transportation costs for the return shipment to the Customer of equipment and/or parts repaired. The foregoing warranties are in lieu of all other warranties expressed and/or implied, oral or written, in fact, by operation of law or otherwise, except as herein expressly stated. In no event shall General Terminal Corporation be liable for any indirect, special or consequential damages such as loss of anticipated profits or other economic loss in connection with or arising out of the use or performance of the equipment or services provided for in this Agreement. The Customer and/or Distributor does not have the right to modify the equipment. If the Distributor and/or Customer modifies the equipment, the Warranty and 90-Day Money-Back Guarantee are void.

Figure 7.1 Warranty

7.4 Parts List

The major subassemblies of the SW10 are shown in Figure 7-2. The parts for each subassembly are listed in the associated table.

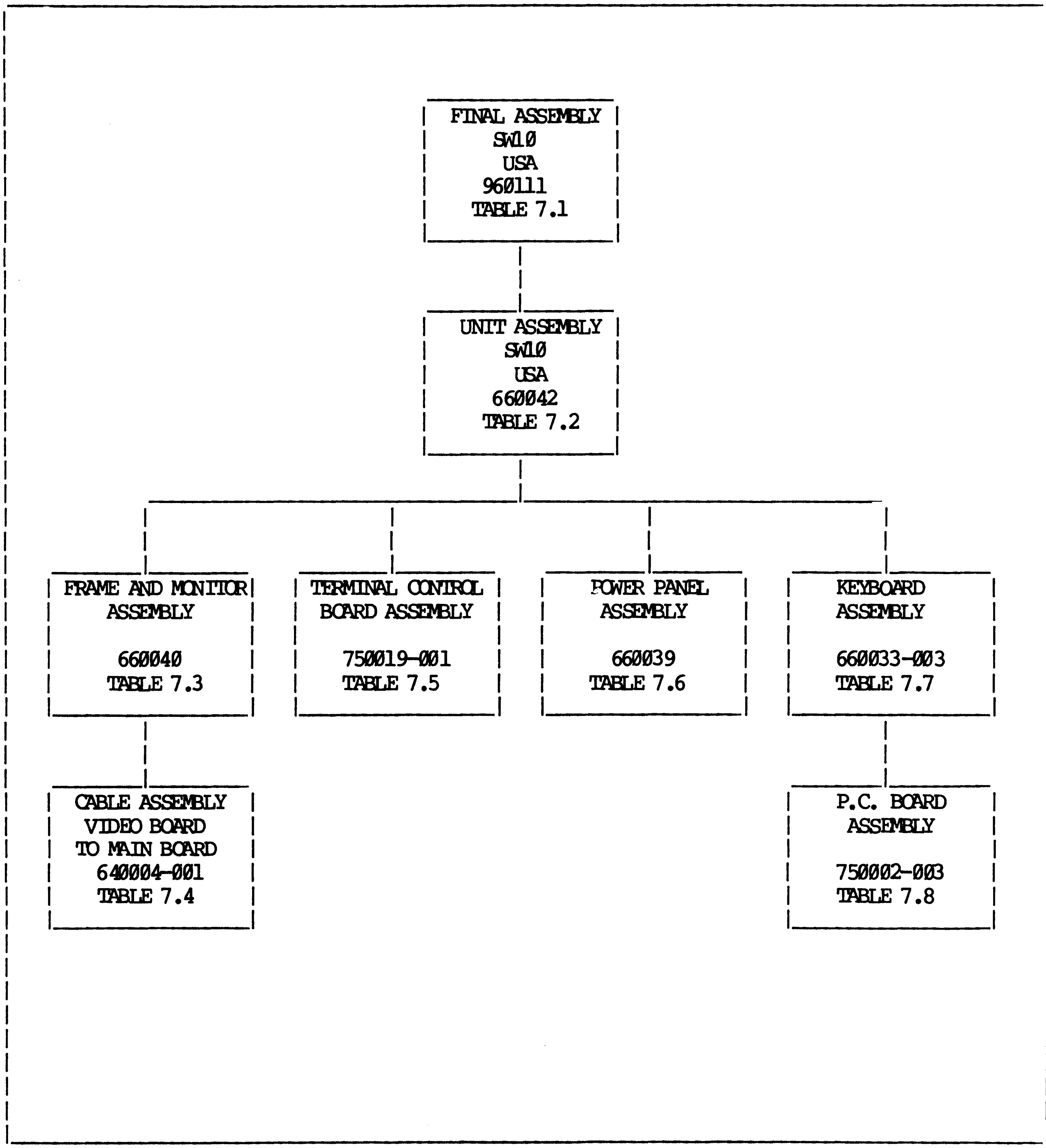

Figure 7.2 SW10 Family Tree

TABLE 7.1 SW1Ø FINAL ASSEMBLY 96Ø111-ØØX*

* ASSY NO 96Ø111-ØØ1 DOMESTIC, GREEN PHOSPHOR
* ASSY NO 96Ø111-ØØ2 DOMESTIC, WHITE PHOSPHOR
* ASSY NO 96Ø111-ØØ4 INTERNATIONAL, GREEN PHOSPHOR
* ASSY NO 96Ø111-ØØ5 INTERNATIONAL, WHITE PHOSPHOR

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER	REF DESIG	ØØ1 ØØ2	ØØ4 ØØ5
1	FINAL ASSY, SW1Ø UNITED STATES	96Ø111-		REF	REF
2	TOP LEVEL DRAWING, SW1Ø	95ØØØ6-ØØ1		REF	REF
3	UNIT ASSY, 11ØV GRN. PHOSPHOR	66ØØ42-ØØ1		1	
3	UNIT ASSY, 11ØV WHT. PHOSPHOR	66ØØ42-ØØ2		1	
3	UNIT ASSY, 22ØV GRN. PHOSPHOR	66ØØ42-ØØ4			1
3	UNIT ASSY, 22ØV WHT. PHOSPHOR	66ØØ42-ØØ5			1
5	I.C. KEYBOARD TRANSLATOR, USA	92ØØ99-ØØ1		1	1
6	I.C. CHARACTER GENERATOR, USA	92ØØ82-ØØ1		1	1
8	NAME PLATE, SW1Ø	62ØØ32-ØØ1		1	1
9	LABEL, KEYBD CABLE CONNECTOR	79ØØ11-ØØ1		1	1
1Ø	DECAL, SERIAL NUMBER	ØØ878-ØØ1		1	1
11	LINE CORD, DOMECTIC	Ø1Ø15-Ø36		1	
11	LINE CORD, INTERNATIONAL	17ØØ24-ØØ1			1
12	USER'S MANUAL, SW1Ø	97ØØØ4-ØØ1		1	1
13	REFERENCE CARD, SW1Ø	97ØØØ8-ØØ1		1	1

TABLE 7.2 UNIT ASSEMBLY 660042-00X*

* ASSEMBLY NO 660042 -001 GREEN PHOSPHOR DOMESTIC
* ASSEMBLY NO 660042 -002 WHITE PHOSPHOR DOMESTIC
* ASSEMBLY NO 660042 -004 GREEN PHOSPHOR INTERNATIONAL
* ASSEMBLY NO 660042 -005 WHITE PHOSPHOR INTERNATIONAL

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER	REF DESIG	QUANTITY -001 -002	-004 -005
1	UNIT ASSEMBLY, SW10	660042			
2	KEYBOARD ASSY, MAX CONFIG.	660033-003		1	1
3	REAR HOUSING, SW10	03579-001		1	1
4	REAR PANEL ASSY, DOMESTIC	660039-001		1	
4	REAR PANEL ASSY, INTERNATIONAL	660039-002			1
5	SCREW, #6-32 X 3/8, INT TTH SEMS	01043-014		6	6
6	FRAME & MONITOR ASSY, GREEN PHOS	660040-001		1	1
6	FRAME & MONITOR ASSY, WHITE PHOS	660040-002		1	1
7	SCREW, #8-32 X 3/4, SEMS	230051-001		4	4
8	FIRMWARE KIT, SW10	930089-011		1	1
9	PC BOARD ASSY, MAIN BOARD	750019-001		1	1
10	BEZEL ASSEMBLY, SW10 FRONT	660041-001		1	1
11	SCREW, #6-32 X 1/2 EXT TTH	230011-001		2	2
12	SCREW, SHEET METAL, #8-32 x 1	230047-001		2	2
13	RUBBER FEET, BROWN, .30 HIGH	150001-001		6	6
14	NUT, TINNERMAN, #6-32	99999-203		2	2
15	ACCESS PANEL	03581-002		1	1
16	SCREW, #6-32 X 3/8, SEMS FLAT	230039-001		2	2
17	LABEL, USER SERVICEABLE CAUTION	790006-001		1	1
18	LABEL, NON-COMPLIANCE TO FCC RLE	790002-001		1	1
19	LABEL, EIA CONNECTIONS	790009-001		1	1

TABLE 7.3 FRAME & MONITOR ASSEMBLY 66040-00X*

* ASSEMBLY NO 660040 -001 GREEN PHOSPHOR
* ASSEMBLY NO 660040 -002 WHITE PHOSPHOR

1	ASSEMBLY, SW10 FRAME & MONITOR	660040-00X		REF	REF
2	TV MONITOR KIT, GREEN PHOSPHOR	890001-001		1	
2	TV MONITOR KIT, WHITE PHOSPHOR	890001-002			1
3	FRAME SW (MONITOR)	620038-001		1	1
4	FRAME SW (VIDEO BOARD)	620038-002		1	1
5	RUBBER BUMPER	01025-005		2	2
6	SCREW #6-32 X 3/8, SEMS TTH	01043-014		6	6
7	CARD GUIDE, 4.50 LONG, NYLON	150004-001		2	2
8	CABLE ASSY, MONITOR BD TO MAIN	640004-001		1	1
9	GROUND WIRE ASSEMBLY	640014-001		1	1
10	WASHER, #6 EXT TOOTH	230050-001		1	1
11	STANDOFF 3/16" LONG	130005-001		4	4
12	SCREW, #8-32 X 1/2, LONG SEMS	230028-001		4	4
13	WASHER, FLAT	230025-001		4	4
14	SCREW, #8-32 X 3/8, SEMS INT TTH	01043-003		2	2
15	SCREW, #4-40 X 1/4 SEMS EXT	230036-001		2	2
16	CABLE CLAMP	01036-006		3	3
17	CABLE TIE TWIST	01042-007		1	1
18	RUBBER BUMPER 1/8 X 1/2	150000-001		1	1

TABLE 7.4 MONITOR TO MAIN BOARD CABLE ASSEMBLY 640004

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER	REF DESIGNATORS	-001
	CABLE ASSY, MONITOR TO MAIN BD	640004-		REF
1	WIRE, 20 AWG, RED	01010-078		1.34'
2	WIRE, 20 AWG, YELLOW	01010-081		1.34'
3	WIRE, 20 AWG, WHITE	01010-074		1.34'
4	WIRE, 20 AWG, BLACK	01010-075		1.34'
5	WIRE, 20 AWG, GREEN	01010-082		1.34'
6	WIRE, 20 AWG, GRAY	01010-079		1.34'
7	WIRE, 20 AWG, VIOLET	01010-080		1.34'
8	CONNECTOR, 7 POS, MASS TERMINAT.	110013-001		1
9	COVER, CONNECTOR, 7 POS	110077-001		1
10	CONNECTOR, P.C. EDGE MT, 10 POS	110045-001		1
13	COVER, CONNECTOR, PC EDGE 10 POS	110046-001		1

TABLE 7.5 SW10 TERMINAL CONTROL BOARD ASSEMBLY 750019

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER	REF DESIGNATORS	QTY
1	PC BOARD ASSEMBLY, SW10	750019		REF
3	PC BOARD MAIN BOARD	740019-001		1
4	PWM, MAIN BOARD	730019-001		REF
5	SCHEMATIC, MAIN BOARD	720019-001		REF
8	IC, LM376	01000-206	U1,U2	2
9	IC, 7406	01000-158	U3	1
10	IC, 74LS04	01000-119	U4	1
11	IC, 74LS08	01000-146	U5,U25	2
12	IC, 74LS00	01000-118	U6,U14	2
13	IC, 74LS10	01000-120	U7	1
14	IC, 74LS273	01000-140	U11,U18,U33,U46	4
15	IC, Z8/40, ROMLESS	010094-001	U12	1
18	IC, 74LS139	010093-001	U13	1
19	IC, 74LS32	01000-175	U15,U34	2
20	IC, MM5034	03516-001	U16	1
21	IC, DP8304	01000-183	U17	1
22	IC, MM2114L	01000-182	U19,U20,U27, U28,U29,U30	6
23	IC, 74LS367	01000-117	U21,U31,U32	3
24	IC, NC7033	01000-178	U22	1
25	IC, MC1489	01000-067	U23	1
26	IC, MCT-210	01038-002	U24,U37	2
27	IC, 74S74	01000-056	U26,U39	2
28	IC, 74C906	01000-181	U35	1
29	IC, MC1488	01000-036	U36	1
30	IC, 74S86	01000-113	U38	1
31	IC, 74LS14	01000-167	U40	1
32	IC, 74LS153	01000-134	U42,U43	2
33	IC, 74165	01000-018	U44	1
34	IC, DP8369 VTAC	03518-001	U47	1
35	IC, 74LS05	01000-188	U48	1
38	REGULATOR, -12V (7912)	01006-014	VR1	1
39	REGULATOR, +12V (7812)	01006-012	VR2	1

TABLE 7.5 SW1Ø TERMINAL CONTROL BOARD ASSEMBLY 75ØØ19 (CONTINUED)

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER	REF DESIGNATORS	QTY
42	DIODE, 1N414Ø	Ø1ØØ7-Ø39	CR1-4,CR7,CR9	6
43	DIODE, 1N5237B ZENER	Ø6ØØ57-ØØ1	CR5	1
44	DIODE, 1N4ØØ4	Ø1ØØ7-Ø37	CR6,8,1Ø,14,15	5
45	DIODE, 1N714A ZENER	Ø1ØØ7-Ø45	CR12	1
46	DIODE, 1N4747A ZENER	Ø1ØØ7-Ø4Ø	CR13	1
47	DIODE, 1N4ØØ2	Ø1ØØ7-ØØ3	CR16,17,18, CR21,22,23	6
48	DIODE, 1N4148 (1N914)	Ø1ØØ7-ØØ8	CR19,CR2Ø	2
51	CAP, 47ØØuf 35V +5Ø%-1Ø%	Ø3ØØ44-ØØ1	C1,C6	2
52	CAP, Ø.Ø1uf 25ØV 1Ø%	Ø1ØØ8-225	C2,C9	2
53	CAP, Ø.ØØ1uf 1ØØØV 2Ø%	Ø1ØØ8-226	C3,C1Ø	2
54	CAP, Ø.1uf 25ØV 1Ø%	Ø1ØØ8-224	C4,C8	2
55	CAP, 1ØØuf 25V +5Ø%-1Ø%	Ø1ØØ8-227	C5,C11,C14,C16	4
56	CAP, 47Øuf 35V +5Ø%-1Ø%	Ø1ØØ8-Ø98	C7	1
57	CAP, 1ØØuf 5ØV +5Ø%-1Ø%	Ø1ØØ8-229	C12	1
58	CAP, 25uf 25V +75%-1Ø%	Ø1ØØ8-Ø83	C13,C54,C55	3
59	CAP, .33uf 1ØØV 2Ø%	Ø1ØØ8-23Ø	C15,C17	2
6Ø				
61	CAP, .Ø1uf 5ØV +8Ø%-2Ø%	Ø1ØØ8-Ø78	C18-C24,C26,C27 C28-33,C38-C44 C48-C51,C56-C62	33
63	CAP, 6.8uf 16V 2Ø% TANT	Ø1ØØ8-128	C25	1
64	CAP, 22pf 1ØØØV 1Ø%	Ø1ØØ8-Ø72	C34-C37	4
65	CAP, 33Øpf 1ØØØV 1Ø%	Ø1ØØ8-Ø9Ø	C45,C46,C47	3
66	CAP, 3Øpf 1ØØØV 1Ø%	Ø1ØØ8-Ø92	C52,C53	2
67	CAP, 47ØØpf 1ØØV 1Ø%	Ø3ØØ77-ØØ1	C63	1
69	RES PACK, 4.7K	Ø1ØØ9-Ø44	RP1	1
71	RES, 47Ø ohm 1/2W 5%	Ø1ØØ9-2ØØ	R27	1
72	RES, Ø.68 ohm 3W 1Ø%	Ø1ØØ9-262	R1,R8	2
73	RES, 1ØØ ohm 1/4W 5%	Ø1ØØ9-Ø57	R2,R9	2
74	RES, 22Ø ohm 1/4W 5%	Ø1ØØ9-Ø62	R3	1
75	RES, 75Ø ohm 1/4W 5%	Ø1ØØ9-261	R4,R23	2
76	RES, 6.34K ohm 1/8W 1%	Ø2ØØØ5-ØØ4	R5	1
77	RES, 62K ohm 1/4W 5%	Ø1ØØ9-138	R6,R52,R53	3
78	RES, 3.16K ohm 1/8W 1%	Ø2ØØØ5-ØØ3	R7	1
79	RES, 18Ø ohm 1/4W 5%	Ø1ØØ9-Ø6Ø	R1Ø	1
8Ø	RES, 1.8K ohm 1/4W 5%	Ø1ØØ9-Ø73	R11	1

TABLE 7.5 SW10 TERMINAL CONTROL BOARD ASSEMBLY 750019 (CONTINUED)

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER	REF DESIGNATORS	QTY
81	RES, 18.7K ohm 1/8W 1%	020005-001	R12	1
82	RES, 360K ohm 1/4W 5%	020000-364	R13	1
83	RES, 2.37K ohm 1/8W 1%	020005-002	R14	1
84	RES, 1K ohm 1/2W 5%	020002-102	R15	1
85	RES, 75 ohm 1/4W 5%	01009-056	R16	1
86	RES, 200 ohm 1/4W 1%	01009-153	R17	1
87	RES, 100 ohm 1/4W 1%	01009-152	R19	1
88	RES, 392 ohm 1/4W 1%	01009-273	R20	1
89	RES, 330 ohm 1/4W 5%	01009-064	R21,R51	2
90	RES, 150 ohm 1/4W 5%	01009-059	R22	1
91	RES, 2.2K ohm 1/4W 5%	01009-075	R24,R40,R41,R42	4
92	RES, 47K ohm 1/4W 5%	01009-095	R25,R26,R43,R46	4
93	RES, 1K ohm 1/4W 5%	01009-070	R28,R29, R48, R49,R56	5
95	RES, 4.7K ohm 1/4W 5%	01009-080	R30-R33,R47	5
96	RES, 75K ohm 1/4W 5%	01009-097	R34	1
97	RES, 10K ohm 1/4W 5%	01009-087	R35,R55,R57	3
99	RES, 470K ohm 1/4W 5%	01009-066	R36	1
100	RES, 120K ohm 1/4W 5%	01009-099	R37	1
101	RES, 510 ohm 1/4W 5%	01009-110	R38	1
102	RES, 47 ohm 1/4W 5%	01009-052	R39	1
103	RES, 6.8K ohm 1/4W 5%	01009-084	R44,R45	2
104	RES, 787 ohm 1/4W 1%	01009-265	R50,R18	2
105	RES, 15K ohm 1/4W 5%	01009-089	R54	1
108	TRANSISTOR, NPN TIP 33A	01006-055	Q1,Q3	2
109	TRANSISTOR, PNP 2N3645 (2N4036)	01006-056	Q2,Q4	2
110	TRANSISTOR, PNP 2N3644	01006-023	Q5,Q6,Q8,Q10	4
111	TRANSISTOR. NPN 2N3643	01006-022	Q7,Q9	2
115	CRYSTAL, 12.2472 MHZ	01030-012	Y1	1
117	CONNECTOR, 3 PIN RT ANG HDR	110052-001		1/12
118	CONNECTOR, MINI-JUMP	110053-001		8
119	CONNECTOR, 3 PIN HEADER	110068-001		8/12
120	WIRE, 22AWG BARE			A/R

TABLE 7.5 SW10 TERMINAL CONTROL BOARD ASSEMBLY 750019 (CONTINUED)

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER	REF DESIGNATORS	QTY
121	IC SOCKET, 24 PIN	01029-004	U8,9,10,41,45	5
122	IC SOCKET, 40 PIN	01029-010	U12,U47	2
124	CONNECTOR, 25 PIN	110075-001	J1,J2,J6	3
125	CONNECTOR, 5 POS	110009-001	J3,J4	2
126	CONNECTOR, 7 POS	110011-001	J5	1
128	SCREW, #4-40 X 3/8, CRES	01043-007	J1,J2,J6	6
129	NUT, #4-40 KEPS EXT	230041-001	J1,J2,J6	6
132	SCREW, #4-40 X 1/4 CRES	01043-008	Q1,Q3	2
133	WASHER, NYLON SHOULDER	230044-001	Q1,Q3	2
134	INSULATOR, TRANSISTOR	200021-001	Q1,Q3	2
136	HEATSINK	99999-281	Q1,Q3	2
137	SCREW, #4-20 X 3/8 SELF TAP	01043-067	Q1,Q3	4
138	WASHER, NYLON #6	230016-001	Q1,Q3	4
142	TERM, MALE QK-DIS	130002-001	J7	1
143	SCREW, MACH. #6-32 X 1/4	230027-001	J7	1
144	NUT, #6-32 KEPS EXT	01043-005	J7	1

NOTE: Firmware is part of unit assembly 66042
Char Gen is part of final assembly 960111

TABLE 7.6 POWER PANEL ASSEMBLY 660021-00X*

* ASSY NO 660021-001 110V DOMESTIC
* ASSY NO 660021-002 220V INTERNATIONAL

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER	REF DESIG	QTY -001	QTY -002
1	ASSY, REAR PANEL	660039		REF	REF
2	REAR PANEL	620010-002		1	1
3	WIRE, WHITE 18 AWG	01010-059		64"	64"
4	WIRE, BLK 18 AWG	01010-050		16"	16"
5	WIRE, GRN 18 AWG	01010-055		28"	28"
6	CONN RECPT, 220V INTN'L	01013-035	P1	1	1
7	CONN RECPT, 220V W/LINE FILTER	99999-133	P1	1	1
8	SWITCH DPST ROCKER	01017-073	S1	1	1
9	LUG,TERMINAL #6, 16-14 AWG	01022-317		2	2
10	CONTACT,18 AWG TIN-PLATE SNAP-IN	01021-097		7	7
11	WASHER, #6 LOCK EXT TTH	230050-001		1	1
12	FUSE HOLDER	99999-139	F1	1	1
13	NUT, HEX #6-32 HEX KEPS	01043-005		9	9
14	SCREW, #4-40 X 3/8	01043-007		2	2
15	NUT, #4 KEPS	230041-001		2	2
16	TRANSFORMER 25W	050016-001	T1	1	1
17	TRANSFORMER 40W	050015-001	T2	1	1
18	SHRINK TUBING 3/16 D	170011-001		2.5"	2.5"
19	CONN HOUSING 5 POS	110030-001	J3,J4	2	2
20	POLARIZING KEY	01021-098		2	2
21	FUSE, 0.5A INTERNATIONAL	120000-001	F1		1
22	FUSE 1.0A DOMESTIC	120002-001	F1	1	
23	TERMINAL 22-18AWG QWIK DISCON'T	01022-326		6	6
24	TERMINAL 16-14AWG QWIK DISCON'T	01022-327		10	10
25	SPACER FIBER 1/2 OD X 5/32 ID	01035-005		4	4
26	SHRINK TUBING 1/2 D	170007-001		1.75	1.75
27	TAPE 1/4" DOUBLE SIDED FILM	9999-085		A/R	A/R
28	INSULATOR WRAP, (POLY) TRANS	62036-001		1	1

TABLE 7.7 KEYBOARD ASSEMBLY 660033-003

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER	REF DESIG	QTY
1	UNIV HOUSING, BOTTOM	03585-002		1
2	UNIV HOUSING, TOP	03585-001		1
3	BEZEL, KEYBOARD	03599-001		1
4	PCB ASSEMBLY, KEYBOARD	750002-003		1
5	ASSEMBLY, CABLE	900006-001		1
6	FOOT, BROWN	150000-001		7
8	SCREW, #6-32 X 3/8, SEMS	01043-014		4
9	WASHER, #4 FLAT	01043-068		7
10	SCREW, #4-20 X 5/8"	01043-062		7
11	WASHER, ROD LOCKING	01043-065		6

TABLE 7.8 SW10 DETACHED KEYBOARD ASSEMBLY 750002-003

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER	REF DESIGNATORS	QTY 003
1	ASSY, PC BD DETACHED KEYBOARD	750002-003		REF
2	ARTWORK MASTER, DETACHED KBD	730002-001		REF
3	SCHEMATIC	720002-001		REF
4	PC BOARD, DETACHED KEYBOARD	740002-001		1
7	I.C., 74159	01000-179	U48	1
8	CAP, .01uf 50V	01008-078	C63	1
9	CAP, 6.8uf 15V, TANT	01008-128	C62	1
10	TRANSDUCER	01048-002	LS1	1
11	SCREW,#4-20 X 3/8,PN HD PLASTIC	01043-067		10
12	SCREW, #6-32 X 1/4, PN HD	230027-001		1
13	ASSEMBLY, HEADER, 18 PIN	110007-001	J1	1
14	TERMINAL, MALE, QUIK - DISC	130002-001		1
15	NUT, #6-32, EXT KEPS	01043-005		1
16	ALPHA-NUMERIC KEYPAD	900026-001		1
17	NUMERIC KEYPAD	900024-001		1
18	CURSOR KEYPAD	900025-001		1
19	FUNCTION KEYPAD, (F1-F4)	900025-002	F1-F4	1
20	FUNCTION KEYPAD, (F5-F8)	900025-003	F5-F8	1
21	FUNCTION KEYPAD, (F9-F12)	900025-004	F9-F12	1
22	RES PACK SIP 10 PIN 470 ohm	020017-001	RPI	1

TABLE 7.9 SW10 OPTIONAL PARTS

ITEM NO.	TITLE / DESCRIPTION	PART NUMBER
1	DATA CABLE (6 FT.)	640011-006
2	DATA CABLE (9 FT.)	640011-009
3	ADAPTER CABLE, FEMALE TO MALE, SW/VT-100	640013-001
4	BASE, SWIVEL/TILT	640018-001

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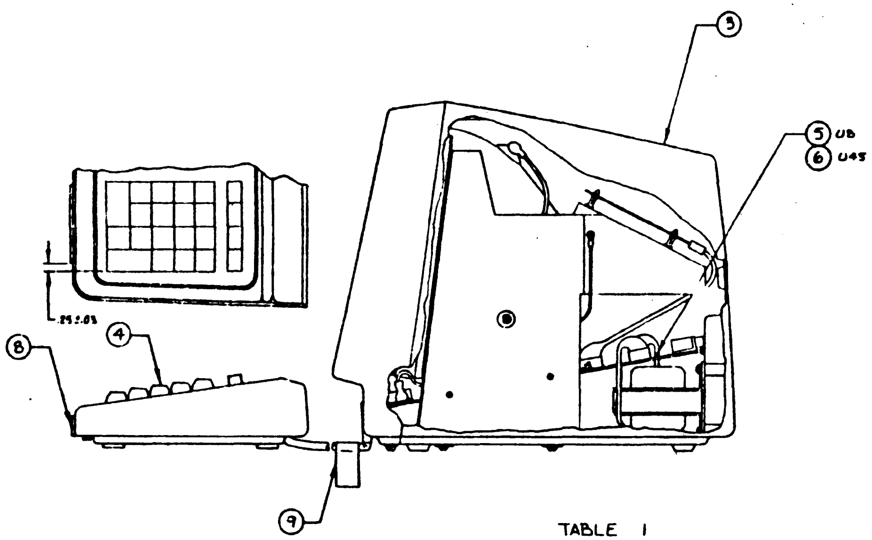
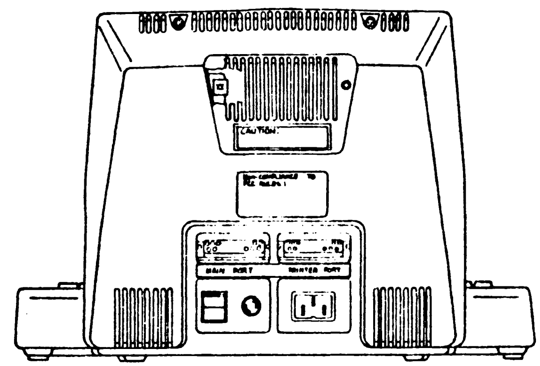
REV	DESCRIPTION	DATE	APPR
01	ENGINEERING RELEASE PER DRN 0656	[illegible]	[illegible]
02	REVISED PER ECO 2593 DRN 0721	3/82	LA
A	PRODUCTION RELEASE PER ECO [illegible] DRN [illegible]	4/82	[illegible]





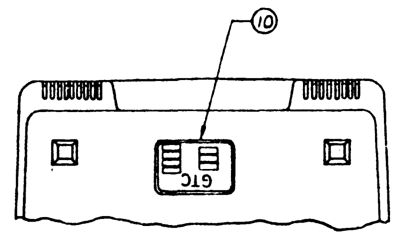


TABLE I

SW-10 FINAL ASSEMBLIES	
960111	SW-10 UNITED STATES
960091	SW-10 GERMAN
960092	SW-10 DANISH
960093	SW-10 SWEDISH / FINNISH
960094	SW-10 SPANISH
960095	SW-10 NORWEGIAN
960096	SW-10 UNITED KINGDOM
960097	SW-10 FRENCH AZERTY
960098	SW-10 INTERNATIONAL AZERTY
960099	SW-10 INTERNATIONAL QWERTZ
960100	SW-10 INTERNATIONAL QWERTY
960103	SW-10 FRENCH TYPEWRITER

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR APPROPRIATE PARTS LIST, SEE TABLE I

DIMENSIONS IN INCHES AND APPLY AFTER PLATING. REMOVE BURRS & SHARP EDGES

TOLERANCE UNLESS SPECIFIED: DECIMALS .XX ± .03, .XXX ± .010; ANGLES ± 0°30'

MATERIAL: —

FINISH: —

DO NOT SCALE DRAWING

DRAWN: [illegible] — DATE: [illegible] 82

CHECKED: [illegible] — [illegible]

APPR: [illegible] — [illegible]

APPR: [illegible] — [illegible]

MODEL NO: SW-10

NEXT ASSY: —

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GTC General Terminal Corporation

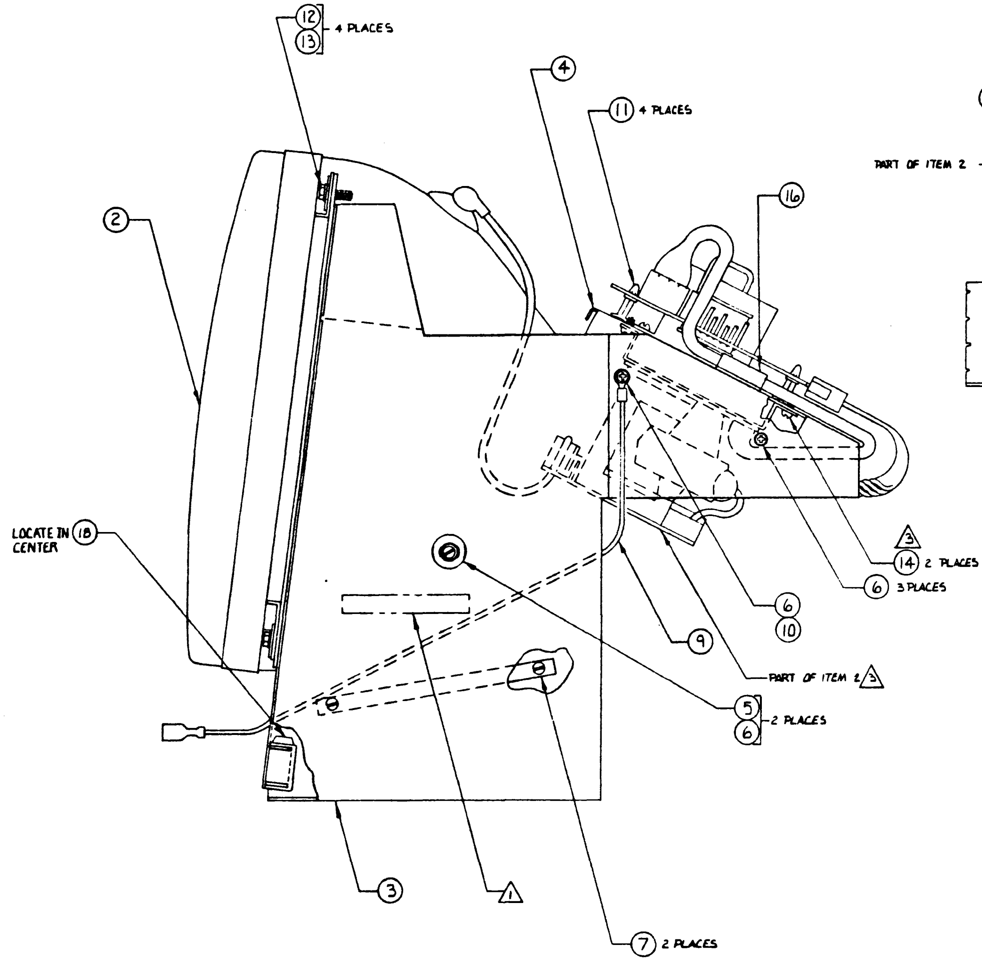
TITLE: TOP LEVEL DRAWING, SW-10 WITH MONITOR FRAME

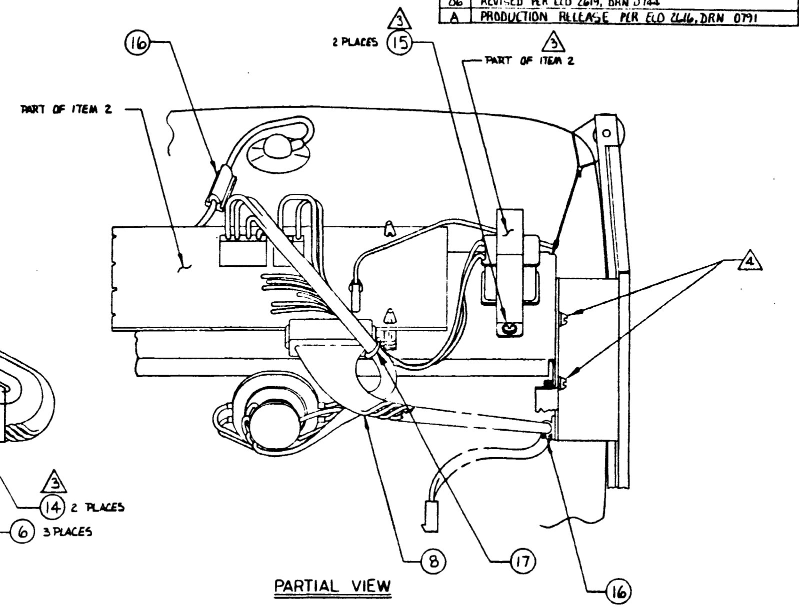
SIZE: D — DRAWING NO: 950006-001 — REV: A

SCALE: 1/2 — SHT 1 OF 1

REV	DESCRIPTION	DATE	APPR
B	REVISED PER ECO 2667, DRN 0814	[illegible]	[illegible]

REV.	DESCRIPTION	DATE	APPR
01	ENGINEERING RELEASE PER DRN 0650	[illegible]	[illegible]
02	REVISED PER ECO 2511, DRN 0109	[illegible]	[illegible]
03	REVISED PER ECO 2558, DRN 0709	[illegible]	[illegible]
04	REVISED PER ECO 2592, DRN 0744	[illegible]	[illegible]
05	REVISED PER ECO 2609, DRN 0744	[illegible]	[illegible]
06	REVISED PER ECO 2619, DRN 0744	[illegible]	[illegible]
A	PRODUCTION RELEASE PER ECO 2616, DRN 0791	[illegible]	[illegible]





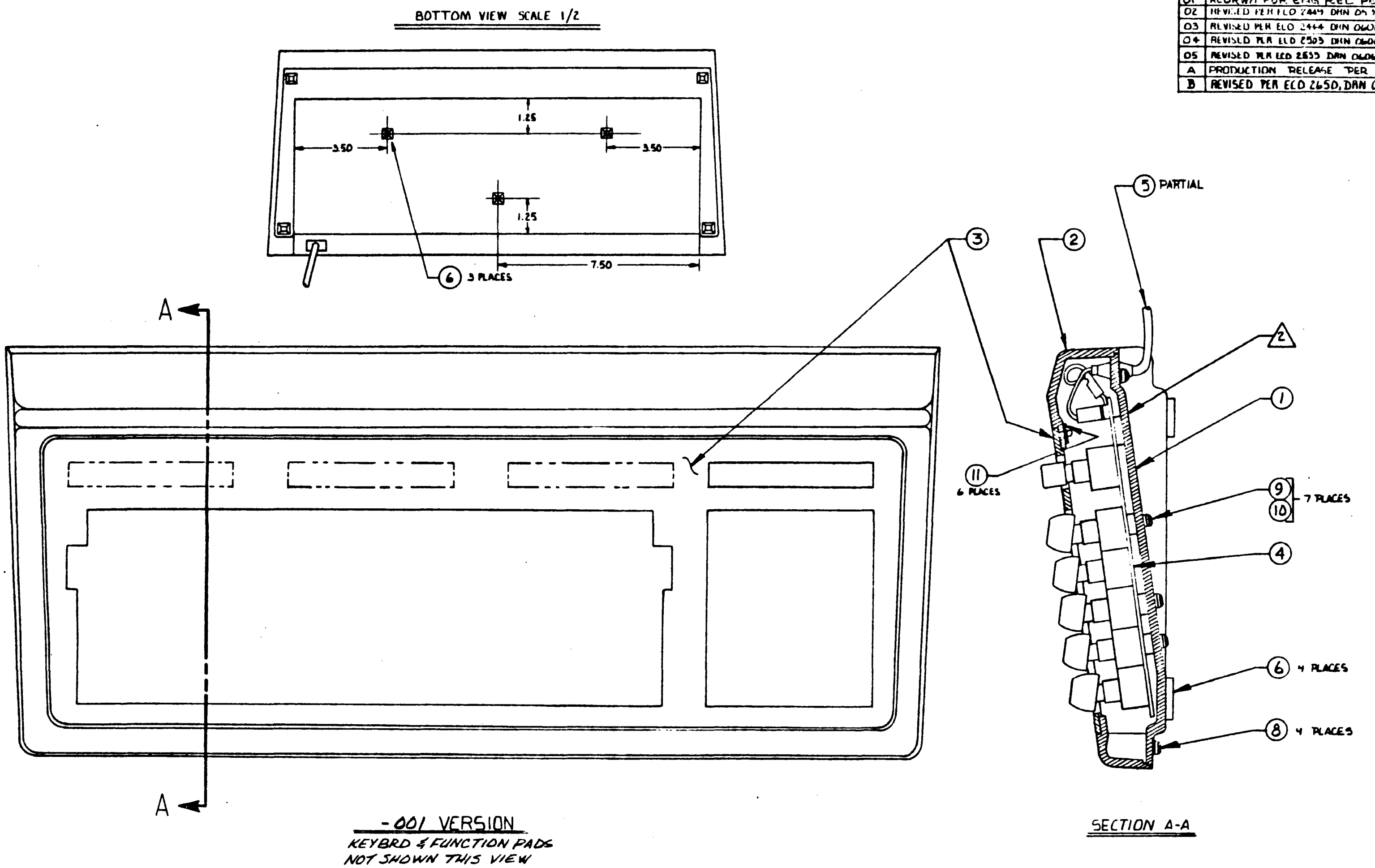
PARTIAL VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

1. IDENTIFY WITH PART NO. AND PART REV LETTER.
2. SEE SEPARATE PARTS LIST 660040.
3. THE VERTICAL CHOKE & FLYBACK TRANSFORMER ARE AN INTEGRAL PART OF THE VIDEO P.C BOARD ON SOME MONITOR UNITS, THEREFORE MOUNTING SCREWS WILL NOT BE NECESSARY.
4. IF VIDEO BOARD IS EQUIPPED WITH SPADE LUGS ON GROUND WIRES, THEN TERMINATE AT THIS POINT.

DIMENSIONS IN INCHES AND APPLY AFTER PLATING REMOVE BURRS & SHARP EDGES	DRAWN [illegible]	DATE [illegible] -82	GTC General Terminal Corporation
TOLERANCE UNLESS SPECIFIED DECIMALS XX 03 .XXX 010 ANGLES 0 30'	CHECKED [illegible]	[illegible]	TITLE: ASSEMBLY, FRAME AND MONITOR SW
	APPR. [illegible]	[illegible]	
	APPR. [illegible]	[illegible]	
MATERIAL: SEE NOTE 2	MODEL NO. SW		
	NEXT ASSY SW-10 FINAL ASSY'S		
FINISH: —	This document contains proprietary information of GTC and such information may not be disclosed to others, reproduced, copied or used without written permission from GTC.		SIZE D — DRAWING NO. [illegible] — REV [illegible]
DO NOT SCALE DRAWING			SCALE 1:1 — SHT OF

REV	DESCRIPTION	DATE	APPR.
01	REDRWN FOR ENG REL PER CRN 0377	[illegible]	[illegible]
02	REVISED PER ECO 2449 DRN 0537	[illegible]	[illegible]
03	REVISED PER ECO 2444 DRN 0606	[illegible]	[illegible]
04	REVISED PER ECO 2503 DRN 0606	[illegible]	[illegible]
05	REVISED PER ECO 2535 DRN 0606	[illegible]	[illegible]
A	PRODUCTION RELEASE PER ECO 2616, DRN 0791	[illegible]	[illegible]
B	REVISED PER ECO 2650, DRN 0823	[illegible]	[illegible]

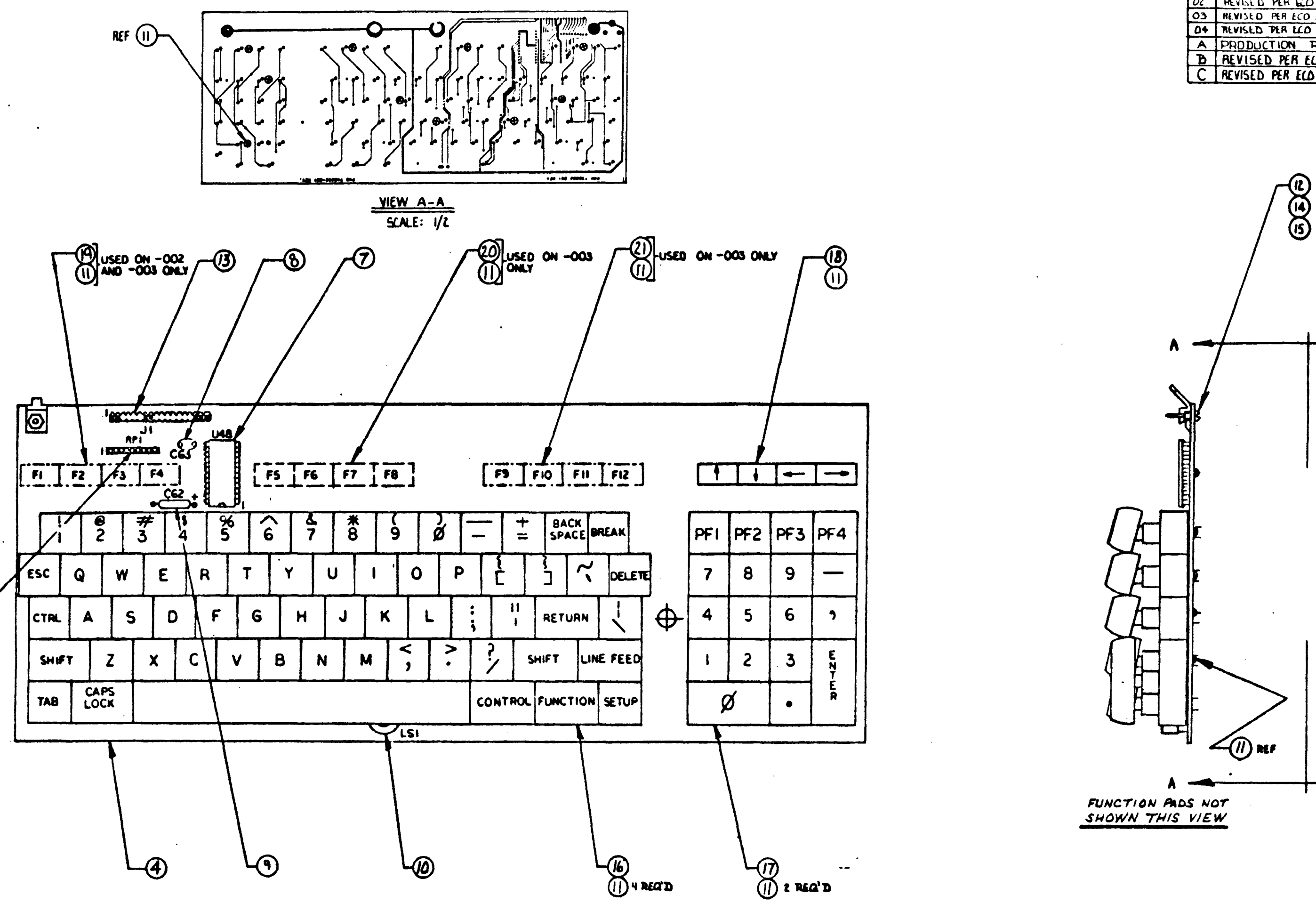


NOTES:

1. SEE SEPERATE PARTS LIST 660033.
2. (△) IDENTIFY WITH PART NO. AND PART REV LETTER ON UNDERSIDE OF ASSEMBLY.

DIMENSIONS IN INCHES AND APPLY AFTER PLATING REMOVE BURRS & SHARP EDGES	DRAWN [illegible]	DATE 4-21-81	General Terminal Corporation
TOLERANCE UNLESS SPECIFIED DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 0 30'	CHECKED [illegible]	10/9/81	TITLE: ASSY- DETACHED KEYBRD
	APPR		
MATERIAL:	APPR		
	MODEL NO SW-10		SMALL WORKER - 10
FINISH:	NEXT ASSY 960047		SIZE D · DRAWING NO. 660033 · REV B
DO NOT SCALE DRAWING	This document contains proprietary information of GTC and such information may not be disclosed to others, reproduced, copied or used without written permission from GTC		SCALE FULL · SHT 1 OF 1

REV	DESCRIPTION	DATE	APPR
01	ENGINEERING RELEASE PER DRN 0572	10/81	LB
02	REVISED PER ECO 2386, DRN 0535	11/81	LB
03	REVISED PER ECO 2451, DRN 0618	2/81	LB
04	REVISED PER ECO 2541, DRN 0753	4/82	LB
A	PRODUCTION RELEASE PER ECO 2616, DRN 0791	4/82	LB
B	REVISED PER ECO 2650, DRN 0823	5/82	LB
C	REVISED PER ECO 2676, DRN 0823	6/82	LB



-001 THRU -003 VERSIONS

NOTES:

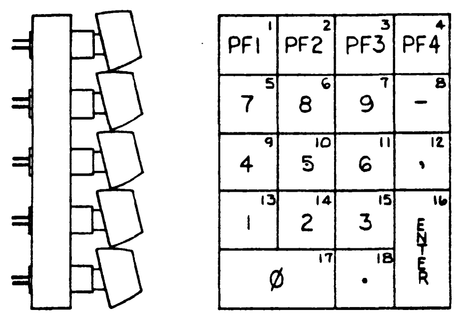
1. SEE SEPARATE PARTS LIST 750002.
2. IDENTIFY WITH PART NO AND PART REV LETTER.

DIMENSIONS IN INCHES AND APPLY AFTER PLATING REMOVE BURRS & SHARP EDGES	DRAWN: Antonelli	DATE: 4-19-81	General Terminal Corporation
TOLERANCE UNLESS SPECIFIED DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 0°30'	CHECKED	10-19-81	TITLE: ASSY- PC BOARD, SW-10 DETACHED KEYBOARD
	APPR.		
MATERIAL:	APPR.	10-19-81	
	MODEL NO. SW-10		
FINISH:	NEXT ASSY		
	This document contains proprietary information of GTC and such information may not be disclosed to others, reproduced, copied or used without written permission from GTC.		SIZE D · DRAWING NO. 750002 · REV C
DO NOT SCALE DRAWING			SCALE FULL · SHT 1 OF 1

REV	DESCRIPTION	DATE	APPR.
01	ENGINEERING RELEASE PER 0301	4-81	LB
02	REVISED PER ECO 2331, DRN 0447	7-81	LB
03	REVISED PER ECO 2371, DRN 0513	9-81	LB
04	REVISED AND REDRAWN PER ECO 2426, DRN 0577	10/81	LB
05	REVISED PER ECO 2502 DRN 0638	1/82	LB
A	PRODUCTION RELEASE PER ECO 2616, DRN 0791	4/82	LF

REF NO.	CAP COLOR	GTC KEYCAP PART NUMBER	SPEC PLASTIC LEGEND NO.
1	FTB/3	600012-011	13-1067C
2	FTB/3	600012-012	13-1068C
3	FTB/3	600012-013	13-1064C
4	FTB/3	600012-015	13-1070C
5	BEB/4	600013-097	01-1033N
6	BEB/4	600013-098	01-1034N
7	BEB/4	600013-099	01-1035N
8	FTB/3	600012-010	01-1038
9	BEB/4	600013-094	01-1030N
10	BEB/4	600013-095	01-1045N
11	BEB/4	600013-096	01-1032N
12	FTB/3	600012-009	01-1037
13	BEB/4	600013-091	01-1027N
14	BEB/4	600013-092	01-1028N
15	BEB/4	600013-093	01-1029N
16	FTB/3	600015-001	17-1002
17	BEB/4	600016-001	17-1001N
18	BEB/4	600013-100	01-1036

TABLE I



-001 VERSION

NOTES: UNLESS OTHERWISE SPECIFIED

1. NUMBERS IN UPPER RIGHT CORNER OF KEYS ARE REFERENCE NUMBERS ONLY. THEY ARE NOT LEGENDS AND DO NOT APPEAR ON PART.
2. ALL KEYS ARE MOMENTARY ACTION AND TILTED.
3. CAP COLOR TO BE FIESTA TAN (CYCOLAC NO. 82027) WITH BLACK (4500) LEGEND.
4. CAP COLOR TO BE BEIGE (CYCOLAC NO. 82359) WITH BLACK (4500) LEGEND.
5. SEE TABLE I FOR INDIVIDUAL KEYCAP SPECIFICATION NUMBERS.

DIMENSIONS IN INCHES AND APPLY AFTER PLATING REMOVE BURRS & SHARP EDGES	DRAWN JAY S. LYNCH	DATE 4-14-81
TOLERANCE UNLESS SPECIFIED DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 0 30'	CHECKED L. BAGGS	4-14-81
	APPR. R. WILSON	4-27-81
	APPR. L. BAGGS	4-27-81
MATERIAL: ABS PLASTIC	MODEL NO. SW 10	
FINISH:	NEXT ASSY	
DO NOT SCALE DRAWING	This document contains proprietary information of GTC and such information may not be disclosed to others, reproduced, copied or used without written permission from GTC.	

GTC
General Terminal Corporation

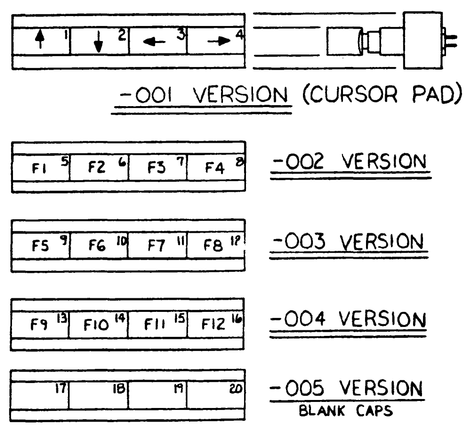
TITLE: SPEC. CONTROL DRAWING, DETACHED KEYBOARD NUMERIC PAD

SIZE	DRAWING NO.	REV
C	900024	A
SCALE	SHT 1 OF 1	

REV	DESCRIPTION	DATE	APPR
01	ENGINEERING RELEASE PER DRN 0569	4-1	LB
02	REVISED AND REDRAWN PER ECO 2426, DRN 0577	10/81	LB
A	PRODUCTION RELEASE PER ECO 2616, DRN 0791	4/82	LB

TABLE I

REF. NO.	CAP COLOR	GTC KEYCAP PART NUMBER	SPEC PLASTIC LEGEND NO.
1	FTB △3	600011-001	TBD (TYP)
2	FTB △3	600011-002	
3	FTB △3	600011-003	
4	FTB △3	600011-004	
5	FTB △3	600011-005	
6	FTB △3	600011-006	
7	FTB △3	600011-007	
8	FTB △3	600011-008	
9	FTB △3	600011-009	
10	FTB △3	600011-010	
11	FTB △3	600011-011	
12	FTB △3	600011-012	
13	FTB △3	600011-013	
14	FTB △3	600011-014	
15	FTB △3	600011-015	
16	FTB △3	600011-016	
17	FTB △3	600011-017	
18	FTB △3	600011-017	
19	FTB △3	600011-017	
20	FTB △3	600011-017	



NOTES: UNLESS OTHERWISE SPECIFIED

1. NUMBERS IN UPPER RIGHT CORNER OF KEYS ARE REFERENCE NUMBERS ONLY. THEY ARE NOT LEGENDS AND DO NOT APPEAR ON PART.
2. ALL KEYS ARE MOMENTARY ACTION
△3 CAP COLOR TO BE FIESTA TAN (CYCOLAC NO. B2027) WITH BLACK (4500) LEGEND.
△4 SEE TABLE I FOR INDIVIDUAL KEYCAP SPECIFICATION NUMBERS.

DIMENSIONS IN INCHES AND APPLY AFTER PLATING
REMOVE BURRS & SHARP EDGES

TOLERANCE UNLESS SPECIFIED
DECIMALS .XX - .03 .XXX - .010
ANGLES - 0 30'

MATERIAL: ABS PLASTIC

FINISH:

DO NOT SCALE DRAWING

DRAWN R SAMFORD DATE 4-14-81
CHECKED LARRY BAGGS 4-14-81
APPR. R WILSON 4-27-81
APPR. LARRY BAGGS 4-14-81
MODEL NO. SW 100
NEXT ASSY

GTC General Terminal Corporation

TITLE: SPEC. CONTROL DRAWING
DETACHED KEYBOARD
FUNCTION KEY CONFIGURATION

SIZE C | DRAWING NO. 900025 | REV A

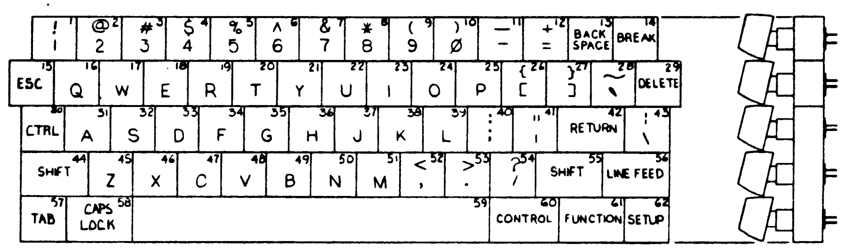
SCALE | SHT 1 OF 1

REV	DESCRIPTION	DATE	APPR.
C1	[illegible]	[illegible]	[illegible]
C2	[illegible]	[illegible]	LB
C3	REVISED PER ECO 2591, DRN 0755	[illegible]	[illegible]
A	PRODUCTION RELEASE PER ECO 2616, DRN 0791	4/12	[illegible]
B	REVISED PER ECO 2650, DRN 0823		

TABLE I

REF NO	CAP COLOR	GTC KEYCAP PART NUMBER	SPEC PLASTIC LEGEND NO.
1	BEB/4	600013-001	03-1013N
2	BEB/4	600013-002	03-1002N
3	BEB/4	600013-003	03-1003N
4	BEB/4	600013-004	03-1004N
5	BEB/4	600013-005	03-1005N
6	BEB/4	600013-006	03-1006N
7	BEB/4	600013-007	03-1007N
8	BEB/4	600013-008	03-1008N
9	BEB/4	600013-009	03-1009N
10	BEB/4	600013-124	03-1041N
11	BEB/4	600013-011	03-1011
12	BEB/4	600013-012	03-1012
13	FTB/3	600012-001	06-1003C
14	FTB/3	600012-002	05-1005C
15	FTB/3	600012-006	05-1002C
16	BEB/4	600013-013	02-1020N
17	BEB/4	600013-014	02-1026N
18	BEB/4	600013-015	02-1008N
19	BEB/4	600013-016	02-1021N
20	BEB/4	600013-017	02-1029N
21	BEB/4	600013-018	02-1028N
22	BEB/4	600013-019	02-1024N
23	BEB/4	600013-020	02-1012N
24	BEB/4	600013-021	02-1018N
25	BEB/4	600013-022	02-1019N
26	BEB/4	600013-023	03-1025
27	BEB/4	600013-024	03-1026
28	BEB/4	600013-025	03-1021
29	FTB/3	600012-003	05-1027C
30	FTB/3	600012-016	05-1001C
31	BEB/4	600013-026	02-1004N

REF NO	CAP COLOR	GTC KEYCAP PART NUMBER	SPEC PLASTIC LEGEND NO.
32	BEB/4	600013-027	02-1022N
33	BEB/4	600013-028	02-1007N
34	BEB/4	600013-029	02-1009N
35	BEB/4	600013-030	02-1010N
36	BEB/4	600013-031	02-1011N
37	BEB/4	600013-032	02-1013N
38	BEB/4	600013-033	02-1014N
39	BEB/4	600013-034	02-1015N
40	BEB/4	600013-035	03-1017
41	BEB/4	600013-036	03-1018
42	FTB/3	600014-001	07-1003N
43	BEB/4	600013-037	03-1014
44	FTB/3	600014-002	07-1001N
45	BEB/4	600013-038	02-1024N
46	BEB/4	600013-039	02-1027N
47	BEB/4	600013-040	02-1006N
48	BEB/4	600013-041	02-1025N
49	BEB/4	600013-042	02-1005N
50	BEB/4	600013-043	02-1017N
51	BEB/4	600013-044	02-1016N
52	BEB/4	600013-045	03-1020
53	BEB/4	600013-046	03-1019
54	BEB/4	600013-047	03-1015
55	FTB/3	600014-002	07-1001N
56	FTB/3	600014-003	07-1013N
57	FTB/3	600012-004	05-1011C
58	FTB/3	600014-009	07-1009N
59	BEB/4	600010-002	25-1000
60	FTB/3	600014-004	07-1012N
61	FTB/3	600014-005	07-1014N
62	FTB/3	600012-007	05-1084C



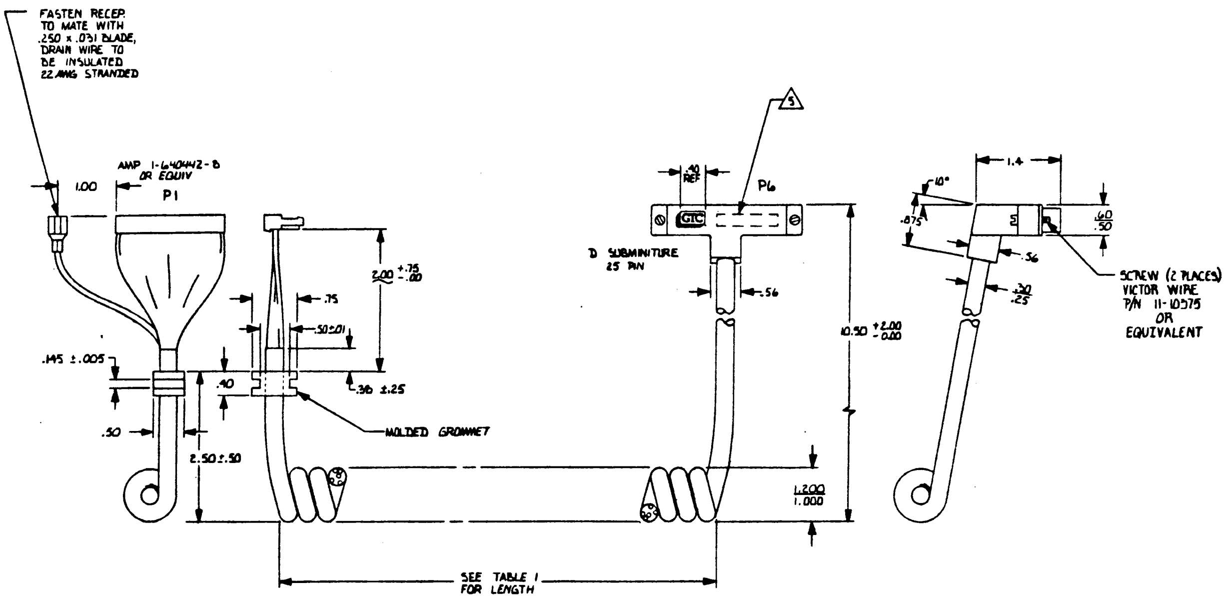
-001 VERSION

NOTES: UNLESS OTHERWSE SPECIFIED

1. NUMBERS IN UPPER RIGHT CORNER OF KEYS ARE REFERENCE NUMBERS ONLY. THEY ARE NOT LEGENDS AND DO NOT APPEAR ON PART.
2. ALL KEYS ARE MONENTARY ACTION AND TILTED.
3. △3 CAP COLOR TO BE FIESTA TAN (CYCOLAC NO 82027) WITH BLACK (4500) LEGEND.
4. △4 CAP COLOR TO BE BEIGE (CYCOLAC NO 82359) WITH BLACK (4500) LEGEND.
5. △5 SEE TABLE I FOR INDIVIDUAL KEYCAP SPECIFICATION NUMBERS.

DIMENSIONS IN INCHES AND APPLY AFTER PLATING REMOVE BURRS & SHARP EDGES	DRAWN JAY S LYNCH	DATE 8-21-81	GTC General Terminal Corporation
TOLERANCE UNLESS SPECIFIED DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 0 30'	CHECKED L BAGGS	10-5-81	
	APPR. R WILSON	10 6 81	TITLE: SPEC. CONTROL DRAWING, SW-10 DETACHED KEYBOARD ALPHANUMERIC PAD
MATERIAL: ABS PLASTIC	APPR. L BAGGS	10 5 81	
	MODEL NO. SW 10		
FINISH: ———	NEXT ASSY		
	This document contains proprietary information of GTC and such information may not be disclosed to others, reproduced, copied or used without written permission from GTC		SIZE D · DRAWING NO. 900026 · REV B
DO NOT SCALE DRAWING			SCALE 1/1 · SHT 1 OF 1

REV	DESCRIPTION	DATE	APPR
01	ENGINEERING RELEASE PER DRN 0072	9/8	L.B.
02	REVISED AND REDRAWN PER ECO 2367, DRN 0497	8/81	L.B.
03	REVISED PER ECO 2467 DRN 0608	11/81	
04	REVISED PER ECO 2600, DRN 0742	3/	
A	PRODUCTION RELEASE PER ECO 2646, DRN 0791	4/82	



NOTES: UNLESS OTHERWISE SPECIFIED

1. CABLE SHALL CONTAIN 18 CONDUCTORS OF #26 AWG INSULATED WIRE CONSISTING OF 10 STRANDS OF #36 GA TINNED COPPER STRANDING.
2. EACH CONDUCTOR TO BE INDIVIDUALLY COLOR CODED.
3. CABLE TO BE COILED IN A COUNTER CLOCKWISE ROTATION AND HAVE A 1.200 ABSOLUTE MAX. COIL DIA.
4. FOR WIRING CONNECTIONS SEE WIRING TABLE.
5. (△) IDENTIFY WITH PART NO. "900006-XXX," IN AREA SHOWN.
6. .035 THK, 80° C, PVC OUTER JACKET TO BE APPLIED OVER THE CABLED CONDUCTORS TO AN O.D. OF MAX .30, MIN .25. COLOR TO MATCH 20040 DAB BROWN PER FED. STD. 595. SURFACE TO BE MATTE FINISH.
7. CABLE TO BE SHIELDED (MIN. 90%) WITH DRAIN CONNECTED TO A PIN OF THE D SUBMINITURE & TERMINATED AS SHOWN ON THE OTHER END.

WIRE TABLE

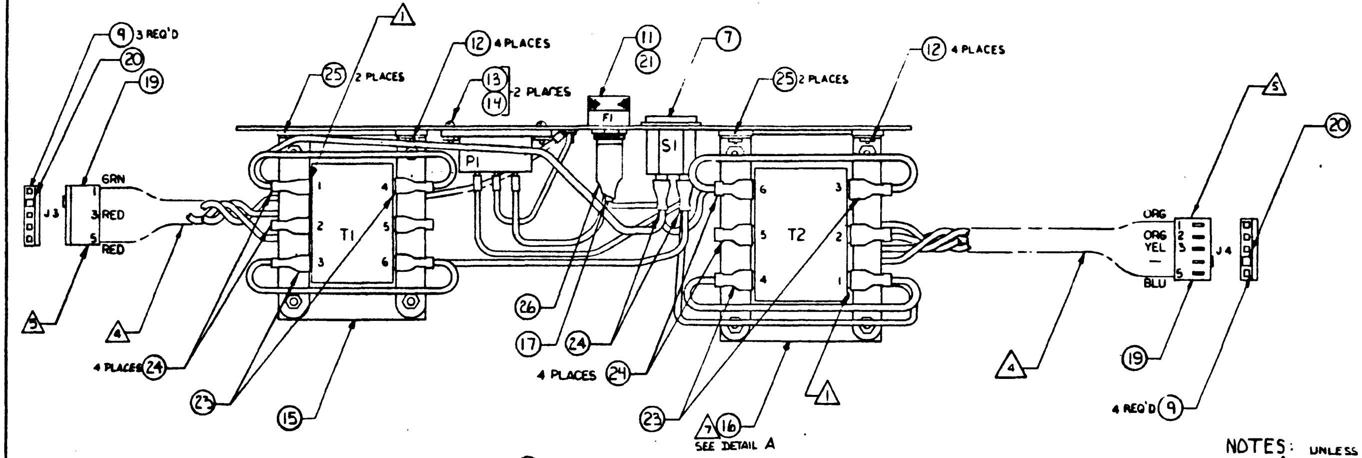
WIRE NO.	FROM	TO	COLOR	SIGNAL NAME
1	P1 - 1	P6 - 10		KROW 0
2	- 2	- 22		KROW 1
3	- 3	- 24		KROW 7
4	- 4	- 15		KROW 2
5	- 5	- 12		KROW 6
6	- 6	- 23		KROW 5
7	- 7	- 11		KROW 4
8	- 8	- 1		GND
9	- 9	- 14	TBD	GND
10	- 10	- 2		KROW 3
11	- 11	- 17		KMUX 0
12	- 12	- 4		KMUX 1
13	- 13	- 16		KMUX 2
14	- 14	- 3		KMUX 3
15	- 15	- 13		+5V
16	- 16	- 25		+5V
17	- 17	- 9		SPKR +
18	P1 - 18	- 5		SPKR -
19	PIG TAIL	P6 - 18	BLK	SHIELD

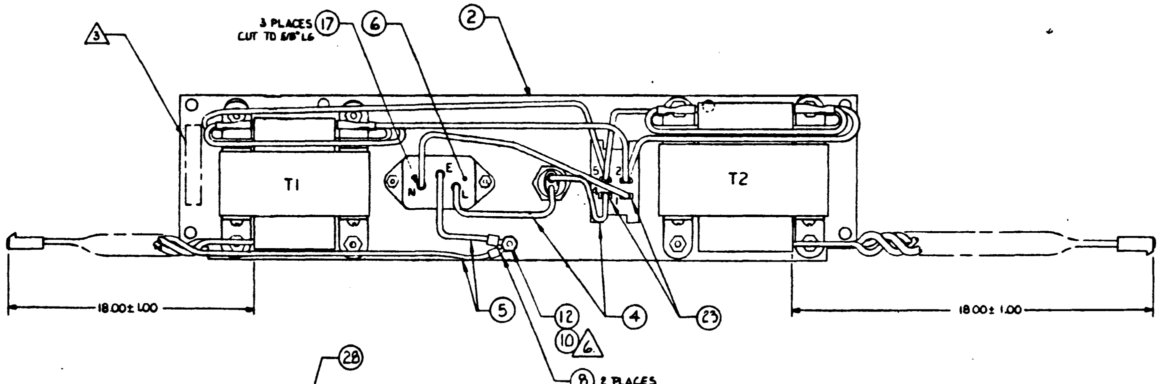
TABLE I

DASH NO	RETRACTED LENGTH	MINIMUM FULLY EXTENDED LENGTH
-001	8.0 +1.5 -0.0	32.0
-002	12.0 +1.5 -0.0	48.0
-003	20.0 +1.5 -0.0	80.0

DIMENSIONS IN INCHES AND APPLY AFTER PLATING. REMOVE BURRS & SHARP EDGES	DRAWN 8/6/80	GTC General Terminal Corporation
TOLERANCE UNLESS SPECIFIED: DECIMALS .XX = .03, .XXX = .010; ANGLES = 0°30'	CHECKED L. BAGGS 8/6/80	TITLE: SPECIFICATION CONTROL DRAWING, KEYBOARD INNERCONNECT CABLE
	APPR. V. CAMPANELLA 8/7/80	
MATERIAL: SEE NOTE 6	MODEL NO. SW-10	
FINISH:	NEXT ASSY	SIZE D; DRAWING NO. 900006; REV A
DO NOT SCALE DRAWING	This document contains proprietary information of GTC and such information may not be disclosed to others, reproduced, copied or used without written permission from GTC.	SCALE 1/1; SHT 1 OF 1

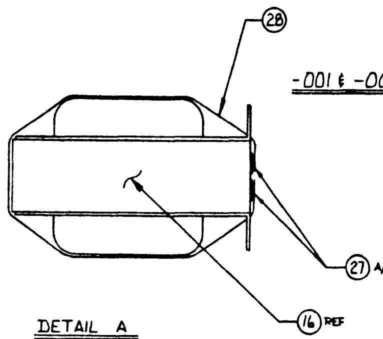
REV	DESCRIPTION	DATE	APPR.
[illegible]	ENGINEERING RELEASE PER DRN 0636	1-82	LB
[illegible]	[illegible] PER ECO 2555 [illegible]	2/82	LB
[illegible]	[illegible] PER ECO [illegible]	2/82	LB
A	PRODUCTION RELEASE PER ECO 2616, DRN 0791	4/82	LG





NOTES: UNLESS OTHERWISE SPECIFIED

1. CUT BLACK WIRE FLUSH AT TRANSFORMER.
2. SEE SEPARATE PARTS LIST 660039.
3. IDENTIFY WITH PART NO AND REV LETTER.
4. CABLE TO BE TWISTED BUT NOT SLEEVED TIED OR CLAMPED.
5. IDENTIFY CONNECTORS J3 & J4 WITH APPROPRIATE REFERENCE DESIGNATOR.
6. LOCK WASHER (ITEM 10) TO BE BETWEEN PANEL (ITEM 2) AND FIRST LUG (ITEM 12).
7. PRIOR TO MOUNTING TRANSFORMER T2 TO REAR PANEL, TAPE (ITEM 27) INSULATOR WRAP (ITEM 28) AROUND TRANSFORMER AS SHOWN IN DETAIL A.



DETAIL A
7 SCALE 1:1

-001 & -003 VERSIONS
120 V

WIRE TABLE			
FROM	TO	DESCRIPTION	ITEM
T1-4	T1-1	WHT, 18 GA, 6 IN	3
T1-1	S1-5	WHT, 10.5 IN	3
S1-5	T2-6	WHT, 5 IN	3
T2-6	T2-3	WHT, 6 IN	3
T2-4	T2-1	WHT, 6 IN	3
T2-1	S1-2	WHT, 6.5 IN	3
S1-2	T1-6	WHT, 9 IN	3
T1-6	T1-3	WHT, 6 IN	3
P1-N	S1-1	WHT, 9 IN	3
S1-4	F1	BLK, 8 IN	4
F1	P1-L	BLK, 8 IN	4
P1-E	GND	GRN, 4 IN	5
J3-1	GND	GRN, 18 GA, 24 IN	5

DIMENSIONS IN INCHES AND APPLY AFTER PLATING
REMOVE BURRS & SHARP EDGES

TOLERANCE UNLESS SPECIFIED
DECIMALS .XX ± .03 .XXX ± .010
ANGLES ± 0°30'

MATERIAL:

FINISH:

DO NOT SCALE DRAWING

DRAWN JAY S LYNCH — DATE JAN 5, '82
CHECKED J. Bagg — 1-19-82
APPR [illegible] — 1-13-82
APPR J. Bagg — 1-13-82
MODEL NO. SW-10
NEXT ASSY

GTC
General Terminal Corporation

TITLE: REAR PANEL ASSY
SMALL WONDER

SIZE D — DRAWING NO 660039 — REV A
SCALE 1/1 — SHT 1 OF 2

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Z8™ Family of Microcomputers Z8611 • Z8612 • Z8613

Product Specification

Zilog

December 1980

Z8611 Single-Chip Microcomputer with 4K ROM
Z8612 Development Device with Memory Interface
Z8613 Prototyping Device with EPROM Interface

Z8™ Family of Microcomputers Z8611 · Z8612 · Z8613

Product Specification

Zilog

December 1980

Z8611 Single-Chip Microcomputer with 4K ROM
Z8612 Development Device with Memory Interface
Z8613 Prototyping Device with EPROM Interface

Features

- Complete microcomputer, 4K bytes of ROM, 128 bytes of RAM, 32 I/O lines, and up to 60K bytes addressable external space each for program and data memory.
- 144-byte register file, including 124 general-purpose registers, four I/O port registers, and 16 status and control registers.
- Average instruction execution time of 2.2 μs, maximum of 4.25 μs.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any of nine working-register groups in 1.5 μs.
- On-chip oscillator which accepts crystal or external clock drive.
- Low-power standby option which retains contents of general-purpose registers.
- Single +5 V power supply—all pins TTL compatible.

General Description

The Z8611 microcomputer introduces a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcomputers, the Z8611 offers faster execution; more efficient use of memory; more sophisticated interrupt, input/output and bit-manipulation capabilities; and easier system expansion.

Under program control, the Z8611 can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 4K bytes of internal ROM, a traditional microprocessor that manages up to 120K bytes of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-BUS. In all configurations, a large number of pins remain available for I/O.

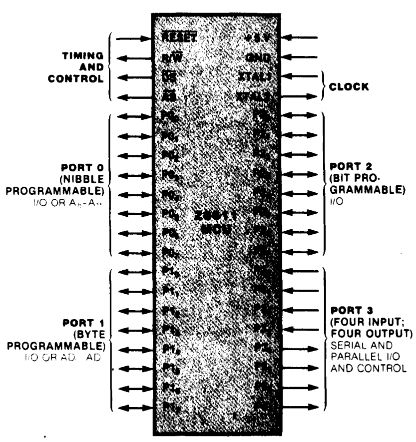

Figure 1. Z8611 MCU Pin Functions

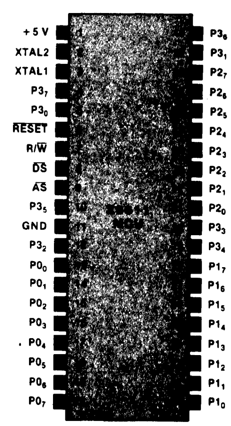

Figure 2. Z8611 MCU Pin Assignments

Architecture

Z8611 architecture is characterized by a flexible I/O scheme, an efficient register and address space structure and a number of ancillary features that are helpful in many applications.

Microcomputer applications demand powerful I/O capabilities. The Z8611 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports of eight lines each and are configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

Because the multiplexed address/data bus is merged with the I/O-oriented ports, the Z8611 can assume many different memory and I/O configurations. These configurations range from a self-contained microcomputer to a microprocessor that can address 120K bytes of external memory (Figure 3).

Three basic address spaces are available to support this wide range of configurations: program memory (internal and external), data memory (external) and the register file (internal). The 144-byte random-access register file is composed of 124 general-purpose registers, four I/O port registers, and 16 control and status registers.

To unburden the program from coping with real-time problems such as serial data communication and counting/timing, an asynchronous receiver/transmitter (UART) and two counter/timers with a large number of user-selectable modes are offered on-chip. Hardware support for the UART is minimized because one of the on-chip timers supplies the bit rate.

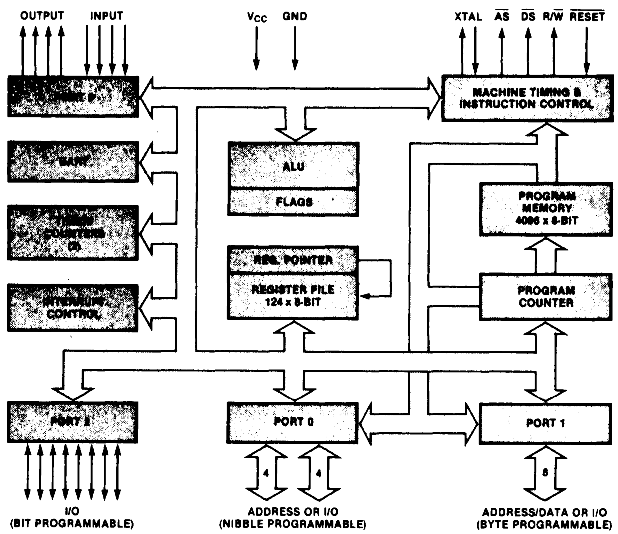

Figure 3. Functional Block Diagram

Pin Description

$\overline{AS}$. *Address Strobe* (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Addresses output via Port 1 for all external program or data memory transfers are valid at the trailing edge of $\overline{AS}$. Under program control, $\overline{AS}$ can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe and Read/Write.

$\overline{DS}$. *Data Strobe* (output, active Low). Data Strobe is activated once for each external memory transfer.

$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$. *I/O Port Lines* (input/outputs, TTL-compatible). These 32 lines are divided into four 8-bit I/O ports that can be configured under program control for I/O or external memory interface.

$\overline{RESET}$. *Reset* (input, active Low). $\overline{RESET}$ initializes the Z8611. When $\overline{RESET}$ is deactivated, program execution begins from internal program location $000C_H$.

R/$\overline{W}$. *Read/Write* (output). R/$\overline{W}$ is Low when the Z8611 is writing to external program or data memory.

XTAL1, XTAL2. *Crystal 1, Crystal 2* (time-base input and output). These pins connect a series-resonant crystal (8 MHz maximum) or an external single-phase clock (8 MHz maximum) to the on-chip clock oscillator and buffer.

Address Spaces

Program Memory. The 16-bit program counter addresses 64K bytes of program memory space. Program memory can be located in two areas: one internal and the other external (Figure 4). The first 4096 bytes consist of on-chip mask-programmed ROM. At addresses 4096 and greater, the Z8611 executes external program memory fetches.

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts.

Data Memory. The Z8611 can address 60K bytes of external data memory beginning at locations 4096 (Figure 5). External data memory may be included with or separated from the external program memory space. $\overline{DM}$, an optional I/O function that can be programmed to appear on pin $P3_4$, is used to distinguish between data and program memory space.

Register File. The 144-byte register file includes four I/O port registers (R0–R3), 124 general-purpose registers (R4–R127) and 16 control and status registers (R240–R255). These registers are assigned the address locations shown in Figure 6.

Z8611 instructions can access registers

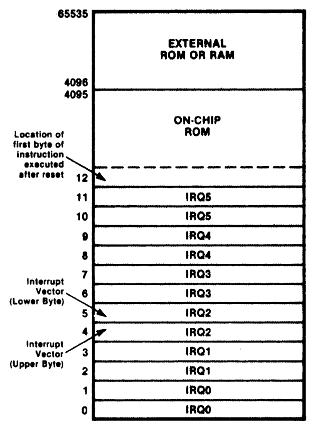

Figure 4. Program Memory Map

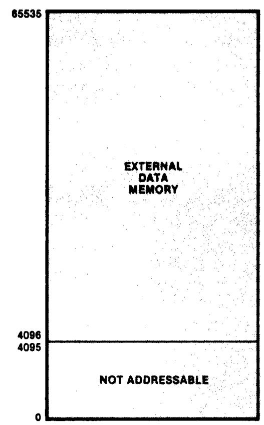

Figure 5. Data Memory Map

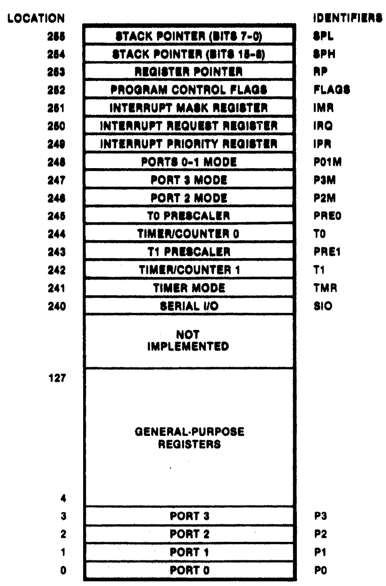

Figure 6. The Register File

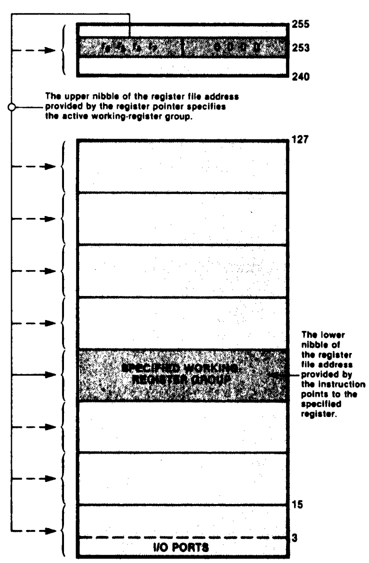

Figure 7. The Register Pointer

Address Spaces (Continued)

directly or indirectly with an 8-bit address field. The Z8611 also allows short 4-bit register addressing using the Register Pointer (one of the control registers). In the 4-bit mode, the register file is divided into nine working-register groups, each occupying 16 contiguous locations (Figure 7). The Register Pointer addresses the starting location of the active working-register group.

Stacks. Either the internal register file or the external data memory can be used for the stack. A 16-bit Stack Pointer (R254 and R255) is used for the external stack, which can reside anywhere in data memory between locations 4096 and 65535. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 124 general-purpose registers (R4–R127).

Serial Input/ Output

Port 3 lines $P3_0$ and $P3_7$ can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer 0, with a maximum rate of 62.5K bits/second.

The Z8611 automatically adds a start bit and two stop bits to transmitted data (Figure 8). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ_4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ_3 interrupt request.

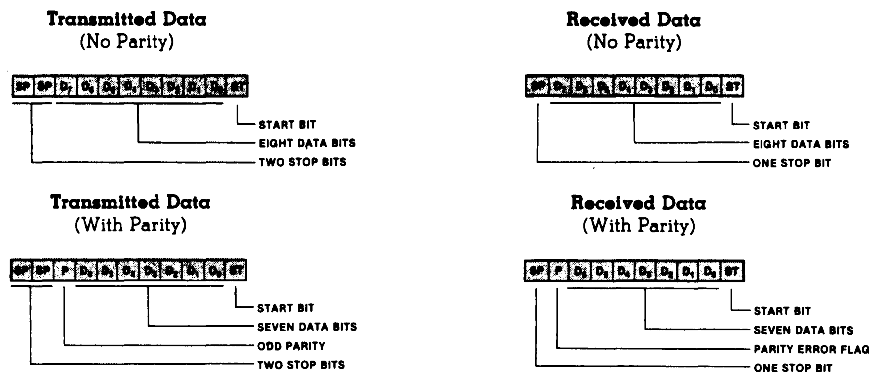

Figure 8. Serial Data Formats

Counter/ Timers

The Z8611 contains two 8-bit programmable counter/timers (T_0 and T_1), each driven by its own 6-bit programmable prescaler. The T_1 prescaler can be driven by internal or external clock sources; however, the T_0 prescaler is driven by the internal clock only.

The 6-bit prescalers can divide the input frequency of the clock source by any number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request—IRQ_4 (T_0) or IRQ_5 (T_1)—is generated.

The counters can be started, stopped, restarted to continue, or restarted from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode). The counters, but not the prescalers, can be read any time without disturbing their value or count mode.

The clock source for T_1 is user-definable and can be the internal microprocessor clock (4 MHz maximum) divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input as an external clock (1 MHz maximum), a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be programmably cascaded by connecting the T_0 output to the input of T_1. Port 3 line $P3_6$ also serves as a timer output (T_{OUT}) through which T_0, T_1 or the internal clock can be output.

I/O Ports

The Z8611 has 32 lines dedicated to input and output. These lines are grouped into four ports of eight lines each and are configurable as input, output or address/data. Under software control, the ports can be programmed to provide address outputs, timing, status signals, serial I/O, and parallel I/O with or without handshake. All ports have active pull-ups and pull-downs compatible with TTL loads.

Port 1 can be programmed as a byte I/O port or as an address/data port for interfacing external memory. When used as an I/O port, Port 1 may be placed under handshake control. In this configuration, Port 3 lines $P3_3$ and $P3_4$ are used as the handshake controls RDY_1 and $\overline{DAV}_1$ (Ready and Data Available).

Memory locations greater than 4096 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$ and $R/\overline{W}$, allowing the Z8611 to share common resources in multiprocessor and DMA applications. Data transfers can be controlled by assigning $P3_3$ as a Bus Acknowledge input, and $P3_4$ as a Bus Request output.

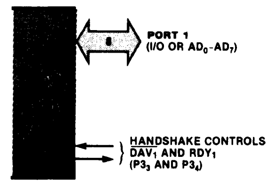

Figure 9a. Port 1

Port 0 can be programmed as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3 lines $P3_2$ and $P3_5$ are used as the handshake controls $\overline{DAV}_0$ and RDY_0. Handshake signal assignment is dictated by the I/O direction of the upper nibble $P0_4$-$P0_7$.

For external memory references, Port 0 can provide address bits A_8–A_{11} (lower nibble) or A_8–A_{15} (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. When Port 0 nibbles are defined as address bits, they can be set to the high-impedance state along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$ and $R/\overline{W}$.

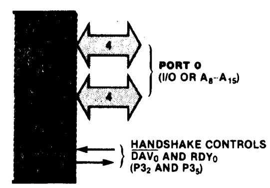

Figure 9b. Port 0

Port 2 bits can be programmed independently as input or output. This port is always available for I/O operations. In addition, Port 2 can be configured to provide open-drain outputs.

Like Ports 0 and 1, Port 2 may also be placed under handshake control. In this configuration, Port 3 lines $P3_1$ and $P3_6$ are used as the handshake controls lines $\overline{DAV}_2$ and RDY_2. The handshake signal assignment for Port 3 lines $P3_1$ and $P3_6$ is dictated by the direction (input or output) assigned to bit 7 of Port 2.

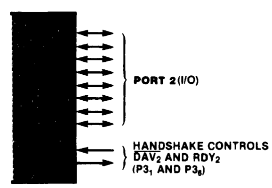

Figure 9c. Port 2

Port 3 lines can be configured as I/O or control lines. In either case, the direction of the eight lines is fixed as four input ($P3_0$-$P3_3$) and four output ($P3_4$-$P3_7$). For serial I/O, lines $P3_0$ and $P3_7$ are programmed as serial in and serial out respectively.

Port 3 can also provide the following control functions: handshake for Ports 0, 1 and 2 ($\overline{DAV}$ and RDY); four external interrupt request signals (IRQ_0-IRQ_3); timer input and output signals (T_{IN} and T_{OUT}) and Data Memory Select ($\overline{DM}$).

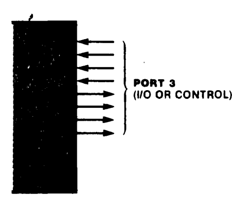

Figure 9d. Port 3

Interrupts

The Z8611 allows six different interrupts from eight sources: the four Port 3 lines $P3_0$-$P3_3$, Serial In, Serial Out, and the two counter/timers. These interrupts are both maskable and prioritized. The Interrupt Mask register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register.

All Z8611 interrupts are vectored. When an interrupt request is granted, an interrupt machine cycle is entered. This disables all subsequent interrupts, saves the Program Counter and status flags, and branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

Polled interrupt systems are also supported. To accommodate a polled structure, any or all of the interrupt inputs can be masked and the Interrupt Request register polled to determine which of the interrupt requests needs service.

Clock

The on-chip oscillator has a high-gain, series-resonant amplifier for connection to a crystal or to any suitable external clock source (XTAL1 = Input, XTAL2 = Output).

The crystal source is connected across XTAL1 and XTAL2, using the recommended capacitors (C_1 = 15 pF) from each pin to ground. The specifications for the crystal are as follows:

- AT cut, series resonant
- Fundamental type, 8 MHz maximum
- Series resistance, $R_s \leq 100\ \Omega$

Power Down Standby Option

The low-power standby mode allows power to be removed without losing the contents of the 124 general-purpose registers. This mode is available to the user as a bonding option whereby pin 2 (normally XTAL2) is replaced by the V_{MM} (standby) power supply input. This necessitates the use of an external clock generator (input = XTAL1) rather than a crystal source.

The removal of power, whether intended or due to power failure, must be preceded by a software routine that stores the appropriate status into the register file Figure 10 shows the recommended circuit for a battery back-up supply system.

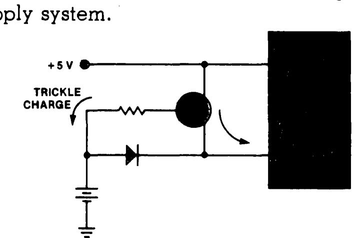

Figure 10. Recommended Driver Circuit for Power Down Operation

Z8612 Development Device

This 64-pin development version of the 40-pin mask-programmed Z8611 (Figure 11) allows the user to prototype the system in hardware with an actual device and to develop the code that is eventually mask-programmed into the on-chip ROM of the Z8611.

The Z8612 is identical to the Z8611 with the following exceptions:

- The internal ROM has been removed.
- The ROM address lines and data lines are buffered and brought out to external pins.
- Control lines for the new memory have been added.

Pin Description. The functions of the Z8612 I/O lines, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, XTAL1, XTAL2 and $\overline{RESET}$ are identical to those of their Z8611 counterparts. The functions of the remaining 24 pins are as follows:

A_0-A_{11}. *Program Memory Address* (outputs). A_0-A_{11} access the first 4K bytes of program memory.

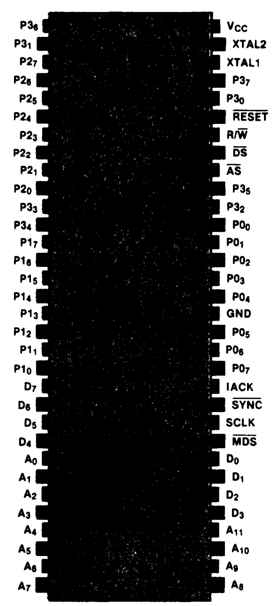

Figure 11. Z8612 Pin Assignments

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National Semiconductor

JUNE 1981

DP8350 Series CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits. Three standard products are available, designated DP8350, DP8352, DP8353. Custom devices, however, are available in a broad range of mask programmable options.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock may be inputted to the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMs, or DM86S64-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, vertical blanking, horizontal sync, and vertical sync.

The DP8350 Series CRTC provides for a wide range of programmablility using internal mask programmable ROMs:

- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame
- Format of Video Outputs

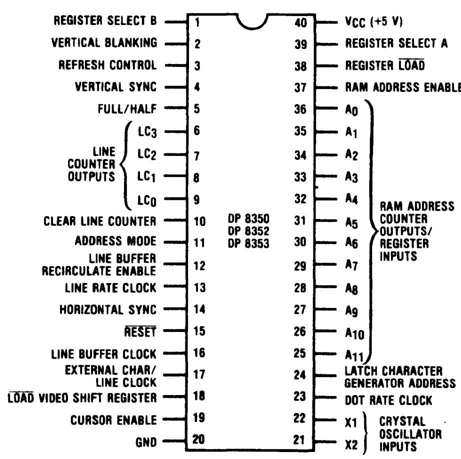
The CRTC also provides system sync and program inputs including Refresh Control, Reset, and Address Mode.

TRI-STATE is a registered trademark of National Semiconductor Corp.

Features

- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Internal top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 2 programmable refresh rates, pin selectable
- Programmable characters/row (128 max.)
- Progammable character field size (up to 16 dots × 16 scan line field size)
- Programmable scan lines/frame (512 max.)
- Programmable character rows/frame
- Single +5V power supply
- Inpu'.s and outputs TTL compatible
- Direct interface with DM86S64 character generator
- Ease of system design/application

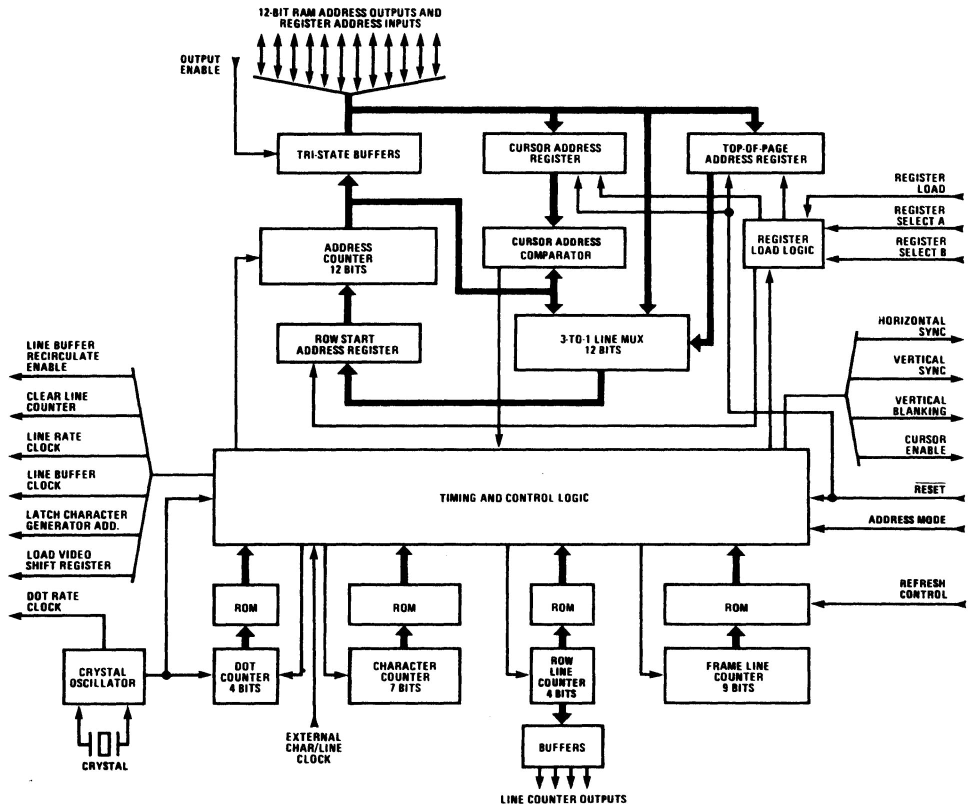
Connection Diagram



Ordering Information:
DP8350N
DP8352N
DP8353N

DA-B25M61/Printed in U.S.A.

Block Diagram



2

The Video Display

Discussion of the CRT Controller necessitates an understanding of the video display as presented by a raster scan monitor. The resolution of the data displayed on the monitor screen is a function of the dot size. As shown in Figure 1, the dot size is determined by the frequency of the system dot clock. The visible size of the dot can be modified to less than 100% by external gating of the serial video data. The CRT Controller organizes the dots into cell groupings that define video rows. These cells are accessed by a specific horizontal address output (4096 maximum) and are resolved by a row scan-line-counter output (16 maximum) as shown in Figure 2. The relation of the video portion of a frame to the horizontal blanking and vertical blanking intervals is shown in Figure 3 in a two-dimensional format.

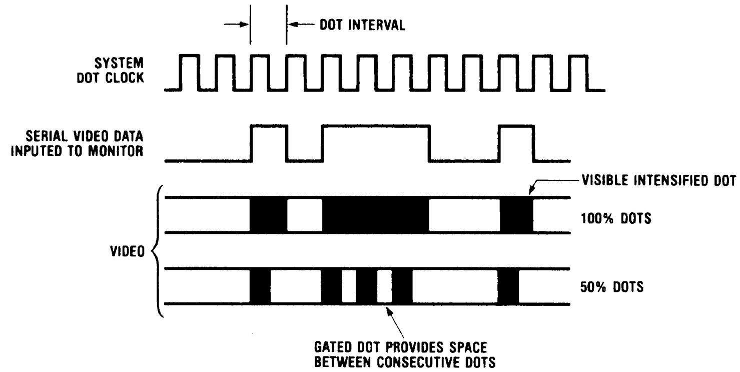


Figure 1. Dot Definition

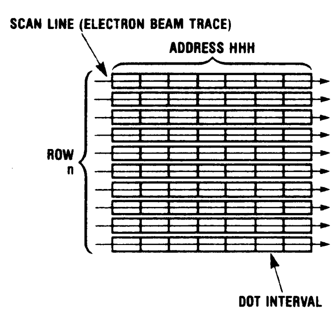


Figure 2. Character Cell Definition (Example Shown is a 7 x 10 Character Cell)

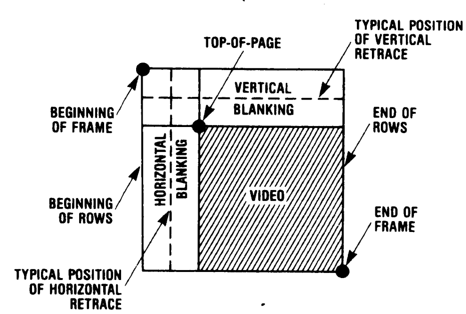


Figure 3. Frame Format Definition

3

Character Generation/Timing Outputs

The CRT controller provides 11 interface timing outputs for line buffers, character generator ROMs, DM86S64-type latch/ROM/shift register combination character generators, and system status timing. All outputs are buffered to provide TTL compatible direct interface to popular system circuits such as:

- DM86S64 Series Character Generators
- MM52116 Series Character ROMs
- DM74166 Dot Shift Register
- MM5034, MM5035 Octal 80-Bit Shift Registers (Line Buffers)

Dot Rate Clock: This output is provided for use in system synchronization and interface to the dot shift register used in character generation. This output is non-inverting with respect to an external clock applied to the X1 oscillator input (see Figure 6). The dot rate clock output exhibits a 50% duty cycle. All CRTC output logic transitions are synchronous with the rising edge of the Dot Rate Clock output.

Latch Character Generator Address (Character Rate Clock): This output provides an active clock pulse at character rate frequency which is active at all times. The rising edge of this pulse is synchronous with the beginning of each character cell. This output is intended for direct interface to character/video generation data latch registers.

Line Rate Clock: This output provides an active clock pulse at scan-line rate frequency (horizontal frequency), which is active at all times. The falling edge of this pulse is synchronous with the beginning of horizontal blanking. This output is intended for direct interface to character generation scan line counters.

Load Video Shift Register: This output provides a character rate signal intended for direct interface to the video dot shift register used in character generation. Active low pulses are outputted only during video time. As a result of the inactive time, horizontal and vertical video blanking can be derived from this output signal.

Clear Line Counter: This output signal is active only during the first scan line of all rows. It exhibits an active low pulse identical and synchronous to the Line Rate Clock and is provided for direct interface to character generation scan line counters.

Line Counter Outputs (LC_0 to LC_3): These outputs clock at line rate frequency, synchronous with the falling edge of the line rate clock, and provide a consecutive binary count for each scan line within a row. These outputs are provided for system designs that require decoded information indicating the present scan line position within a row. These outputs are always active, however, the next to the last row during vertical blanking will exhibit an invalid line count as a function of internal frame synchronization.

Line Buffer Clock: This output directly interfaces to data shift registers when they are incorporated as line buffers in a system design (see Figure 16). This signal is active at character rate frequency and is intended for shift registers that shift on a falling edge clock. This output is inactive during all horizontal blanking intervals yielding the number of active clocks per scan line equal to the number of video characters per row. For custom requirements, the duty cycle of this output is mask programmable.

Line Buffer Recirculate Enable: This output is provided to control the input loading mode of the data shift register (line buffer) when used in a system design. The format of this output is intended for shift registers that load external data into the input with the mode control in the low state, and load output data into the input (recirculate) with the mode control in the high state. This output will transition to the low state, synchronous with the line rate clock falling edge, for one complete scan line of each row. The position of this scan line will either be the first scan line of the addressed row, or the last scan line of the previous row depending upon the logic level of the address mode input (pin 11), tabulated in Table 3.

Memory Address Outputs/Inputs and Registers

Address Outputs (A_0–A_{11}): These 12 address bits (4k) are bi-directional TRI-STATE® outputs that directly interface to the system RAM memory address bus.

In the output mode (enabled), these outputs will exhibit a specific 12-bit address for each video character cell to be displayed on the CRT screen. This 12-bit address increments sequentially at character rate frequency and is valid at the address bus 2 character times prior to the addressed character appearing as video on the CRT screen. This pipelining by 2 characters is provided to allow sufficient time for first, accessing the RAM memory, and second, accessing the character generation memory with the RAM memory data. Since a character cell is comprised of several scan lines of the CRT beam, the sequential address output string for a given video row is identically repeated for each scan line within the row. The starting address for each video scan line is stored within an internal 12-bit register called the Row Start Register. At the beginning of each video scan line, the internal address counter logic is preset with the contents of the Row Start Register (see Figure 4). To accomplish row by row sequential addressing, internal logic updates the Row Start Register at the beginning of the first scan line of a video row with the last address + 1 of the last scan line of the previous video row. Since the number of address locations on the video screen display is typically much less than the 4k dimension of the 12-bit address bus, an internal 12-bit register called the Top Of Page Register, contains the starting address of the first video row. Internal logic loads the contents of this top of page register into the Row Start Register at the beginning of the first scan line of the first video row. The Top Of Page Register is loaded with address zero whenever the Reset input is pulsed to the logic "0" state.

In the input mode (disabled), external addresses can be loaded into the internal 12-bit registers by external control of the register select A, register select B, and register $\overline{\text{load}}$ inputs (see Table 1). As a result of specific external loading of the contents of the Row Start Register, Top Of Page Register, and the Cursor Register, row by row page scrolling, non-sequential row control, and cursor location control, can easily be accomplished.

During the non-video intervals, the address output operation is modified. During all horizontal blanking intervals, the incrementing of the address counter is inhibited and the address count is held constant at the last video address + 1. For example, if a video row has an 80 character cell format and addressing for the video portion of a given scan line starts at address 1, the address counter will increment up through address 81. Address 81 is held constant during the horizontal blanking interval until 3 character times before the next video scan line. At this point, the address counter is internally loaded with the contents of the Row Start Register which may contain address 1 or 81 as a function of internal control, or a new address that was loaded from the external bus. During vertical blanking, however, this loading of the internal address counter with the contents of the Row Start Register is inhibited providing scan line by scan line sequential address incrementing. This allows minimum access time to the CRTC when the address counter outputs are being used for dynamic RAM refresh.

RAM Address Enable Input: At all times the status of the bi-directional address outputs is controlled externally by the logic level of the enable input. A 'low' logic level at this input places the address outputs in the TRI-STATE® (disabled) input mode. A 'high' logic level at this input places the address outputs in the active (enabled) output mode.

Register Load/Select Inputs: When the Register Load input is pulsed to the logic 'low' state, the Top Of Page, Row Start, or Cursor Register will be loaded with a 12-bit address which originates from either the internal address counter or the external address bus (refer to discussion on register loading constraints). The destination register is selected prior to the load pulse by setting the register select inputs to the appropriate state as defined in Table 1.

Table 1. Register Load Truth Table

Register Select A (Pin 39)	Register Select B (Pin 1)	Register Load Input (Pin 38)	Register Loading Destination
0	0	0	No Select
0	1	0	Top-of-Page
1	0	0	Row-Start*
1	1	0	Cursor
X	X	1	No Load

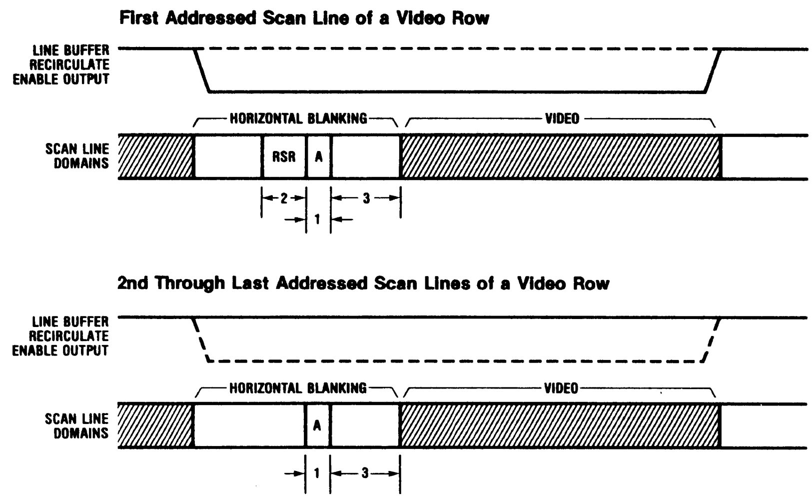
*During the vertical blanking interval, a load to this register is internally routed to the Top-Of-Page register.

Internal Registers and Loading Constraints: There are 3 internal 12-bit registers that facilitate video screen management with respect to row-by-row page scrolling, non-sequential row control and cursor location. These registers can be loaded with addresses from the external address bus while the address outputs are disabled (RAM address enable inut in the low state), by controlling the register select and load inputs within the constraints of each register.

The Row-Start Register (RSR) holds the starting address for each scan line of the video portion of a frame. The video addressing format is completely determined by the contents of this register. With no external loading, the RSR is automatically loaded by internal control such that row-by-row sequential addressing is achieved. Referring to Figure 4, the RSR is loaded automatically once for each video row during the first addressed scan line. The source of the loaded address is internally controlled such that the RSR load for the first video row comes from the Top-Of-Page Register. The RSR load for all subsequent video rows comes from the address counter which holds the last displayed address + 1. If non-sequential row formatting is desired, the RSR can be loaded externally with a 12-bit address. However, this external load must be made prior to the internal automatic load. Generally speaking, the external load to the RSR should be made during the video domain of the last addressed scan line of the previous row. Figure 4 indicates the internal automatic loading intervals which must be avoided, if the load must be made during the horizontal blanking interval. Once an external address has been loaded to the RSR, the next occurring internal automatic RSR load will be inhibited by internal detection logic. If an external load is made to the RSR during the vertical blanking interval, the 12-bit address is loaded into the Top-Of-Page Register instead of the RSR as a result of internal control. This internal function is performed due to the fact that the address loaded into the RSR for the first video row can only come from the Top-Of-Page Register.

The Top-Of-Page register (TOPR) holds the address of the first character of the first video row. As a function of internal control the contents of this register are loaded into the RSR at the beginning of the first addressed scan line of the first video row (see Figure 4). This loading operation is strictly a function of internal control and cannot be overridden by an external load to the RSR. For this reason, any external load to the RSR during the vertical blanking interval is interpreted internally as a TOPR load. When the Reset input is pulsed to the logic "0" state, the TOPR register is loaded with address zero by internal control. This yields a video page display with the first row of sequential addressing beginning at zero. Page scrolling can be accomplished by externally loading a new address into the TOPR. This loading operation can be performed at any time during the frame prior to the interval where the TOPR is loaded automatically into the RSR (see Figure 4). Once the TOPR has been loaded, it does not have to be accessed again until the contents are to be modified.

The Cursor Register (CR) holds the present address of the cursor location. A true comparison of the address counter outputs and the contents of the CR results in a Cursor Enable output signal delayed by two character times. When the Reset input is pulsed to the logic "0" state, the contents of the CR are set to address zero by internal control. Modifying the contents of the CR is accomplished by external loading at any time during this frame. Typically, loading is performed only during intervals when the address outputs are not actively controlling the video display. Once the CR has been loaded, it does not have to be accessed again until the contents are to be modified.



Note 1: Dimensions are in character time intervals.

Note 2: "A" denotes the interval that the address counter is preset with the contents of the Row Start Register.

Note 3: "RSR" denotes the interval that the Row Start Register is internally loaded with either the contents of the Top-Of-Page Register (1st video row) or the last video address + 1 from the address counter.

Figure 4. Automatic Internal Loading Intervals

Video-Related Outputs

Horizontal Sync: This output provides the necessary scan line rate sync signal for direct interface to either three-terminal or composite sync monitors. The pulse width, position, and logic polarity are mask programmable, in character time increments, for custom requirements. This output may also be mask programmed to have RS-170 compatible serration pulses during the vertical sync interval (refer to DP8352 format and Figure 15).

Vertical Sync: This output provides the necessary frame rate sync signal for direct interface to either three-terminal or composite sync monitors. The pulse width, position, and logic polarity are mask programmable, in scan line increments, for custom requirements.

Cursor Enable: This output provides a signal that is intended to be combined with the video signal to display a cursor attribute which serves as a visual pointer for video RAM location. Internally, the 12-bit address count is continuously being compared with the 12-bit address stored in the Cursor Register. When a true compare is detected, an active high level signal will be present at the Cursor Enable output, delayed by 2 character times after the corresponding address bus output. The signal is delayed by 2 character times so that it will be coincident with the video information resulting from the corresponding address. Mask programmability allows the cursor enable output signal to be formatted such that a signal will be outputted for all addressed scan lines of a video character cell or any single scan line of that cell. The cursor enable output signal is inhibited during the horizontal and vertical blanking intervals so that video blanking is maintained. When the addressing is advanced by setting the address mode input (pin 11) in the logic "0" state, the cursor enable signal will also be shifted with respect to the scan line count. Specifically, for a character cell with the cursor output active on all addressed scan lines of the cell, the first scan line of the cursor signal will occur at the last scan line count of the previous video row, and the last scan line count of the addressed character cell will have no cursor output signal. This mode of operation gives rise to a unique situation for the first video row where the first addressed scan line of a character cell has no cursor output signal since its advanced scan line position is inhibited by the vertical blanking interval.

6

CRT System Control Functions

Refresh Control Input: This input provides a logic level selectable CRT system refresh rate. Typically, this input will select either a 60 Hz or 50 Hz refresh rate to provide geographical marketing flexibility. However, mask programmability provides the capability of a wide range of frequencies for custom requirements. For definition of the input logic truth table and the refresh rate format, refer to Table 2 and the standard device type format tables.

Table 2. Refresh Rate Select Truth Table

Refresh Control (Pin 3) Logic Level	Frame Refresh Rate			
	Symbol	DP8350	DP8352	DP8353
1	f1	60 Hz	60 Hz	60 Hz
0	f0	50 Hz	50 Hz	50 Hz

Vertical Blanking Output: This output provides a signal that transitions at the end of the last video scan line of the last video row and indicates the beginning of the vertical blanking interval. This signal transitions back to the inactive state during the row of scan lines just prior to the first video row. The transition position within this last row of vertical blanking, as well as the active logic polarity, is a function of the particular device format (item 21 of the format tables) or is mask programmable for custom requirements.

Address Mode: When a system utilizes a line buffer shift register, the first scan line of addressing for a row is used to load the shift register. As a result of this loading operation, addressing for a particular row will not begin accessing the video RAM until the second scan line of addressing for the row. It also follows that the first scan line of a row can only exhibit addressed data for the previous video row that is in the shift register. This offset in addressing becomes a problem for character generation designs that output video on the first scan line of a row (with respect to the line counter outputs). The result is invalid data being displayed for the first scan line. One solution would be to utilize a character generation design that began outputting video on the second scan line of a row. However, since most single chip character generators begin video on the first scan line, the DP8350 series CRT controller provides a pin selectable advanced addressing mode which will compensate for addressing shifts resulting from shift register loading. Referring to Table 3, a high logic level at this input will cause addressing to be coincident with the scan line counter positions of a row, and a low logic level at this input will cause addressing to start on the last scan line counter position of the previous row. This shifted alignment of the addressing, with respect to the designated scan lines of a row, is diagrammed in Figure 5. Characteristically, it follows that, when addressing is advanced by one scan line, the Line Buffer Recirculate Enable output and the Cursor Enable output are also advanced by one scan line. This advanced position of the Cursor Enable output may deserve special consideration depending upon the system design.

Table 3. Address Mode Truth Table

Address Mode Input (Pin 11) (Logic Level)	New Row Addressing At Address Outputs and Line Buffer Recirculate Enable Logic Low Level (Scan Line Position)
0	Last scan line of previous row
1	First scan line of row

Full/Half Row Control: This control input is provided for applications that require the option of half-page addressing. As an example, if the normal video page format is 80 characters/row by 24 rows, setting this input to the logic "0" state will cause the video format to become evenly spaced at 80 characters/row by 12 rows. Specifically, when this input is in the logic "0" state, row addressing is repeated for every other row. This yields successive groups of two rows of identical addressing. The second row of addressing, however, has the Load Video Shift Register output and the Cursor Enable output internally inhibited to provide the necessary video blanking. Setting this input to the logic "1" state yields normal frame addressing.

External Character/Line Rate Clock: This input is intended to aid testing of the CRTC and is not meant to be used as an active input in a CRT system. When this input is left open, it is guaranteed not to interfere with normal operation.

Reset Input: This input is provided for power-up synchronization. When brought to the logic "0" state, device operation is halted. Internal logic is set at the beginning of vertical blanking, and the Top-Of-Page Register and the Cursor Register are loaded with address zero. When this input returns to the logic "1" state, device operation resumes at the vertical blanking interval followed by video addressing which begins at zero. This input has hysteresis and may be connected through a resistor to V_{CC} and through a capacitor to ground to accomplish a power-up Reset. The logic "0" state should be maintained for a minimum of 250 ns.

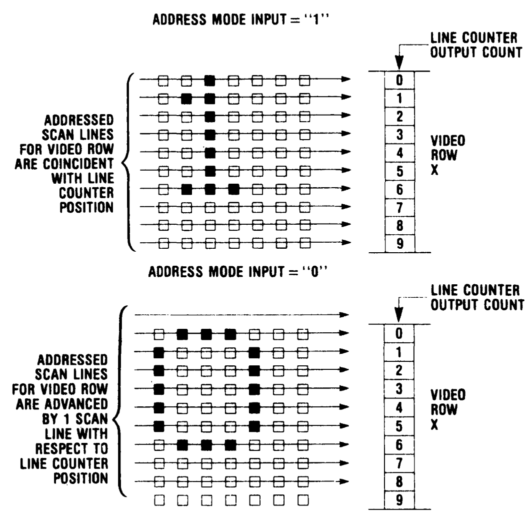


Figure 5. Address Mode Functionality

7

Crystal Inputs X1 and X2: The "Pierce"-type oscillator is controlled by an external crystal providing parallel resonant operation. Connection of external bias components is made to pin 22 (X1) and pin 21 (X2) as shown in Figure 6. It is important that the crystal be mounted in close proximity to the X1 and X2 pins to ensure that printed circuit trace lengths are kept to an absolute minimum. Typical specifications for the crystal are shown in Table 4 for each of the standard products, DP8350, DP8352, and DP8353. When customer mask options require higher frequencies, it may be necessary to change the crystal specifications and biasing components. If the CRTC is to be clocked by an external system dot clock, pin 22 (X1) should be driven directly by Schottky family logic while pin 21 (X2) is left open. The typical threshold for pin 22 (X1) is $V_{CC}/2$.

Table 4. Typical Crystal Specifications

Parameter	Specification		
	DP8350	DP8352	DP8353
Type	At-Cut		
Frequency	10.92 MHz	7.02 MHz	17.6256 MHz
Tolerance	0.005% at 25°C		
Stability	0.01% from 0°C to +70°C		
Resonance	Fundamental, Parallel		
Maximum Series Resistance	50Ω		
Load Capacitance	20 pF		

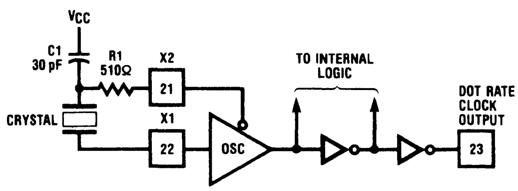


Figure 6. Dot Clock Oscillator Configuration with Typical External Bias Circuitry Shown

Custom Order Mask Programmability: The DP8350 Series CRT controller is available in three standard options designated DP8350, DP8352, and DP8353. The functional format of these devices was selected to meet the typical needs of CRT terminal designs. In order to accommodate specific customer formats, the DP8350 series CRT controller is mask programmable with a diverse range of options available. The items listed in the program table worksheet indicate the available options, while Table 5 tabulates the programming constraints.

Table 5. Mask Programming Limitations

Designation	Parameter	Min. Value	Max. Value
f_{DOT}	Dot Rate Frequency	DC	30 MHz
f_{CHAR}	Character Rate Frequency	DC	2.5 MHz
—	Line Buffer Clock Logic "0" Width (Item 20 × Item 24)	200 ns	
Item 3	Dots per Character Field Width	4	16
Item 4	Scan Lines per Character Field	2	16
Item 12	Scan Lines per Frame		512
Item 14	Character Times per Row — Video	5	122
	Character Times per Row — Blanking	6	123
Item 11	Scan Lines per Vertical Blanking	(Item 4) +2	

If the cursor enable output, Item 22, is active on only one line of a character row, then Item 21 value must be either "1" or "0" or equivalent to the line selected for the cursor enable output.

DP8350 Series Custom Order Format Table

This table is provided as a worksheet to aid in determining the programmed configuration for custom mask options. Refer to Table 5 for a list of programming limitations.

Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	7	
2		Scan Lines per Character (Height)	10	
3	Character Field Block Size	Dots per Character (Width)	7	
4		Scan Line per Character (Height)	10	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		25	
7	Number of Video Scan Lines (Item 4 × Item 6)		250	
8	Frame Refresh Rate (Hz) (two pin selectable frequencies allowed) (Item 13 ÷ Item 12)		f1= 60	f0= 50
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)		4	30
10	Vertical Sync Width (Number of Scan Lines)		10	10
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)		20	74
12	Total Scan Lines per Frame (Item 7 + Item 11)		270	324
13	Horizontal Scan Frequency (Line Rate) (kHz) (Item 8 × Item 12)		16.2	
14	Number of Character Times per Scan Line		108	
15	Character Clock Rate (MHz) (Item 13 × Item 14)		1.7496	
16	Character Time (ns) (1 ÷ Item 15)		571.6	
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)		0	
18	Horizontal Sync Width (Character Times)		48	
19	Dot Frequency (MHz) (Item 3 × Item 15)		12.2472	
20	Dot Time (ns) (1 ÷ Item 19)		81.65	
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)		0	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?		YES	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		NO	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments) (Typically ½ Item 3 rounded up)		3	
25	Serration Pulse Width, if used (Character Times) (See Figure 13)		-	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		1	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		0	

Video Monitor: Manufacturer and Model No. (For Engineering Reference)

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National Semiconductor

March 1980

MM5034, MM5035 Octal 80-Bit Static Shift Register

General Description

The MM5034 octal 80-bit shift register is a monolithic MOS integrated circuit utilizing N-channel low threshold enhancement mode and ion-implanted depletion mode devices.

The MM5034 is designed for use in computer display peripherals. All inputs and outputs are TTL compatible. The clocks and recirculate logic are internal to reduce system component count, and TRI-STATE® output buffers provide bus interface. Because of its N-channel characteristics, single 5V power supply operation is required.

Simple interface to the NSC CRT DP8350 controller and character generator to incorporate an entire CRT terminal is feasible with the MM5034.

The MM5034 is available in a 22-lead dual-in-line package.

The MM5035 is a 20-pin version of the MM5034 with the TRI-STATE output select feature omitted, for a simple data in/data out operation.

Features

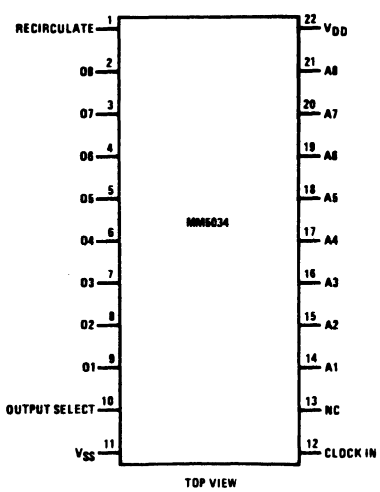
- Single 5V power supply
- Internal clocks
- High speed and static operation
- TRI-STATE output buffer
- Recirculate and output select independent
- TTL compatible

Applications

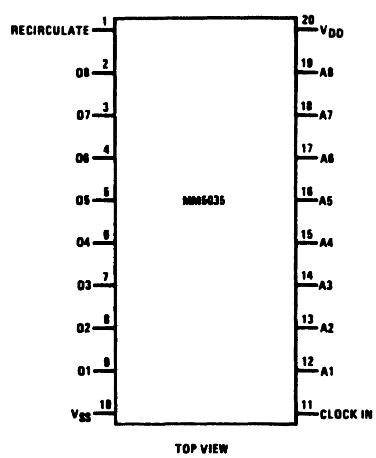
- CRT displays
- Computer peripherals

Connection Diagrams

Dual-in-Line-Package



Dual-in-Line-Package



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MM5034, MM5035 Recirculate and TRI-STATE Operation

Recirculate is used to maintain data in the shift register after it has been loaded. While the shift register is being loaded, Recirculate must be at a logical "0". When the loading is completed, Recirculate should be brought to a logical "1". This disables the data input and feeds the output of the last shift cell back to the input of the first shift cell for each of the 8 registers.

For the output to be in the TRI-STATE mode Output-Select should be at the logical '1' level.

Typical Application

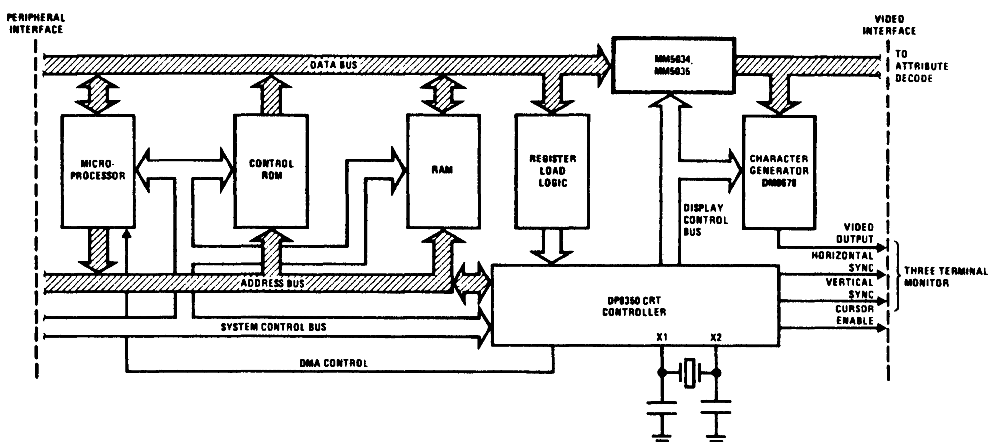


FIGURE 2. CRT System Diagram Using the MM5034, MM5035 as a Line Buffer with DMA

NC7033 MNOS EAROM 21 x 16 (336 BIT)

GENERAL DESCRIPTION

The NC7033 is a low-cost 21 word by 16-bit electrically alterable nonvolatile memory designed especially for use in those systems which require secure, yet alterable, data storage. Data integrity is maintained for a minimum of one year between rewrites and is immune to sudden power outages.

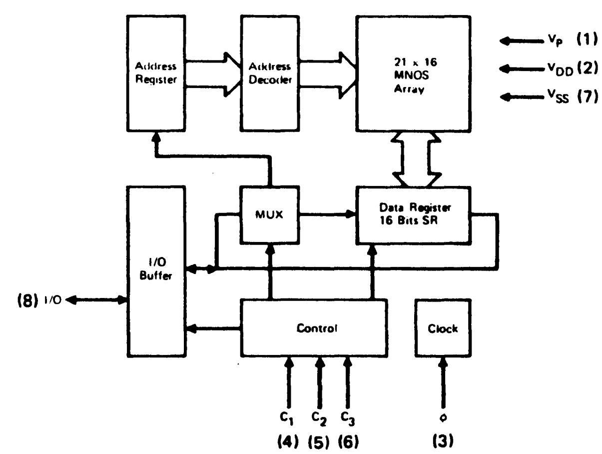
FEATURES

- 21 x 16 Organization
- Low-cost Packaging
- Serial Input/Output
- Fully Decoded Addressing
- Single-word Alterable
- Simple Interface Requirements
- Simple Refresh Capability
- Typical 10-year Unpowered Retention

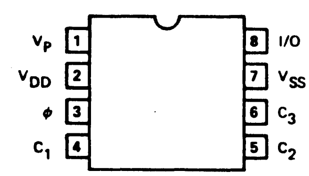
APPLICATIONS

- Microprocessor Peripheral Memory
- Backup Memories
- Preset Frequency Tuning for TVs
- Numerical Machine Controls
- Process Controllers
- Remote or Portable Data Acquisition Systems
- Storage of Calibration or Test Constants
- Programmable Locks/Security Systems
- Non-Volatile Counters, Odometers
- Programmable Games
- Appliance Timer/Controllers
- Event Monitors
- Automatic Telephone Dialers
- Traffic Lights
- Utility Meters

BLOCK DIAGRAM



PIN CONNECTION



NC7033 Nitron

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
Storage Temperature (Power Off) (NC7033L)	−55°C to +150°C
Storage Temperature (Power Off) (NC7033P)	−55°C to +125°C
Non-Powered Data Storage	−20°C to +100°C
Voltage, any Pin except V_P	V_{SS} +0.3V to V_{SS} −20V
Voltage at V_P, all others to V_{SS}	V_{SS} +0.3V to V_{SS} −38V

DC OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS} = 10V ±1.0V, V_{DD} = 0V, V_P = −20V ±1.0V

SYMBOL	PARAMETER	PIN	UNITS	MIN	TYP	MAX	TEST CONDITIONS
I_{SS}	V_{SS} Supply Current	V_{SS}	mA			20	All Modes
I_P	V_P Supply Current	V_P	mA			8	All Modes
V_{OH}	Output High Voltage	I/O	V	V_{SS}−0.8			I_{OH} = 0.4mA, V_P = V_P, V_{DD}
V_{OL}	Output Low Voltage	I/O	V			V_{DD}+0.8	I_{OL} = 0.25mA, V_P = V_P
					V_{DD}+3.5		V_P = V_{DD}
I_{OHS}	Output Short Circuit	I/O	mA	6.0		12	V_{IH} = V_{DD}
I_{OLS}	Drive Capability			−8.0		−20	V_{IL} = V_{SS}
	Pull-Ups to V_{SS}	C_1, C_2, C_3, ϕ	µA	15			V_{IH} = V_{SS} − 0.8V
						300	V_{IL} = V_{DD}
V_{IH}	Input High Voltage	I/O, C1, C2, C3, ϕ	V	V_{SS}−0.8		V_{SS}+0.3	
V_{IL}	Input Low Voltage			V_{DD}		V_{SS} −4.6	
	Pin Capacitance	I/O, C_1, C_2, C_3, ϕ	pF			10	Pin to V_{SS}
N_H	Data Retention (Power Off or Standby Modes)	–		1.0 yr.	3.0 yr.		≤10^5 E/W cycles
				2.5 yr.	10 yr.		≤ 10^2 E/W cycles

AC OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS} = 10V ±1.0V, V_{DD} = 0V, V_P = −20V ±1.0V

SYMBOL	PARAMETER	PIN	UNITS	MIN	TYP	MAX	CONDITIONS
FCL	Clock Frequency FCL = 1/TCL	ϕ	kHz			100	
t_{CLH}	Clock High Level Hold Time	ϕ	µs	5		$10^{(1)}$	See Figure 1A
t_{CLL}	Clock Low Level Hold Time	ϕ	µs	5			
t_{CL}	Clock Fall Time and Rise Time	ϕ	µs			1	
t_{ERASE}	Erase Time	–	ms	150	300	450	See Figure 1E
t_{WRITE}	Write Time	–	ms	2.0	4.0	6.0	
t_E/t_W	Erase to Write Time Ratio	–		50	75	100	
t_{READ}	Read Access Time (First Bit)	I/O		1 clock cycle			
$t_1^{(2)}$	Data Out Delay	I/O		50ns		5.0 µs	See Figure 1A
t_2	Data In Setup	I/O	µs	2			See Figures 1A, 1B
t_3	Instruction Setup Lead	C_1, C_2, C_3	µs	2			See Figures 1B, 1C, 1D, 1E
t_4	Input Setup Lag		ns	50			
	V_P Slew Rate	V_P	V/µsec			1	Power On, Off
N_R	Number of Read Cycles	–		10^9	10^{10}		
N_E	number of Erase Cycles	–		10^5	10^6		
N_W	Number of Write Cycles	–		10^5	10^6		

NOTES: 1. Independent of clock frequency t_{CLH} maximum is 10µsec.
2. t_1 applies only during data transition.
3. Output external loading capacitance will be 10pF.

Nitron

NC7033

FUNCTIONAL DESCRIPTION

The NC7033 336-bit Metal-Nitride-Oxide Semiconductor (MNOS) array is organized into 21 rows of 16 bits. Each bit of storage is actually a dual-transistor pair, differentially sensed, one of which is charged to represent a logic "1" or "0". Each entire 16-bit row, or word, is individually addressable and alterable by means of three control lines (C_1, C_2 and C_3) and a serial input/output port. In addition, the NC7033 utilizes advanced MNOS technology by eliminating the need for programming voltage (V_P) for all but ERASE and WRITE operations.

Each operation is initiated by the proper sequencing of control lines followed by the appropriate 5-bit binary address code presented to the I/O port. The corresponding operation is then completed by the external clock. When not in use the NC7033 should be left OFF or in either a SETUP or STANDBY condition for maximum data retention. Pull up resistors and protection diodes are on C_1, C_2, C_3 and clock inputs. I/O pull up is active only during SERIAL ADDRESS IN and SERIAL DATA IN. During SERIAL DATA OUT, I/O operates in a push-pull mode. All other modes I/O is high impedance. The following mode control functions are provided:

TABLE 1

C_1(1)	C_2(1)	C_3(1)	Instruction	V_P Pin(2)
0	0	0	SETUP	V_P
0	0	1	ERASE	V_P
0	1	0	WRITE	V_P
0	1	1	SERIAL DATA OUT	V_P, V_{DD}(3)
1	0	0	SERIAL ADDRESS IN	V_P, V_{DD}, Hi Z
1	0	1	SERIAL DATA IN	V_P, V_{DD}, Hi Z
1	1	0	READ	V_P, V_{DD}
1	1	1	STANDBY	V_P, V_{DD}, Hi Z

NOTES: 1. $V_H = 1$, $V_L = 0$.
2. V_P can remain at its nominal voltage, or be switched to one of the conditions indicated.
3. Speed and output level will be degraded with V_P held at V_{DD}.

Read Mode

1. The (3-bit parallel) SERIAL ADDRESS IN instruction code is presented on C_1, C_2 and C_3 while the 5-bit serial address is shifted in on the I/O bus by five clocks. The 5-bit serial address utilizes a binary decoding scheme to address all 21 words. The most significant bit enters the chip first.
2. The READ instruction is presented for one clock time. This catches the word from the new address in the NVM array and parallel-loads it into a shift register. During READ the I/O port has an active tri-state output.
3. The SERIAL DATA OUT instruction is presented for 16 clock pulses, causing the data to be shifted out on the I/O bus. Data is handled on a first-in, first-out basis. If, after 16 bits of data has been read out the control lines are left in a SERIAL DATA OUT instruction code, the data will be circulated internally to allow further readout of the same data without access to the NVM array.

Erase/Write Mode

An ERASE must preceed a WRITE for any location for data to be valid. However, a location can be pre-erased and left in an erased state anytime prior to the next write.

1. The address is changed, if necessary, in the same manner as in the read mode.
2. Data is serially loaded onto the chip by presenting the SERIAL DATA IN instruction for 16 clock pulses.
3. The SETUP instruction is presented for one clock pulse.
4. The ERASE instruction is presented for a nominal 300msec: this erases only the addressed word.
5. The SETUP instruction is presented again for one clock pulse.
6. The WRITE instruction is presented for nominal 4 milliseconds. This transfers the data to the selected address in the NVM.

If a location is written without an intervening erase cycle and with different data the result will be a random readout because both transistors in the bit-pair will be in a high state.

Erase Mode

In addition to the ERASE/WRITE sequence described above for an individual word address, all or part of the NC7033 can be pre-erased and left ready to initiate a WRITE sequence. Such would be the case if the NC7033 were to be used as a backup memory and data transferred in the event of a power failure.

1. The address is changed in the same manner as in the readout.
2. SETUP instruction is presented for one clock pulse.
3. ERASE instruction is presented for a nominal 300msec.
4. SETUP instruction presented again for one clock pulse.
5. Address is changed again as in #1 above and process repeated as often as desired.

It should be noted that because the ERASE mode brings both transistors in the bit-pair to a low state, it does not return the data to an all-logic "0" state but rather acts as a preconditioning to the array for the next WRITE pulse. If a READ is performed after a location has been erased but not rewritten the result will be a random pattern readout.

Standby

The STANDBY instruction puts the memory in a quiescent state where the output is high impedance and the clock is ignored.

Clock

The clock performs two functions; it enables mode changes and moves address and data information on the I/O line. A clock pulse is necessary only to enter or exit a mode and can be turned off during Erase, Write, Setup and Standby. Clock can stop during any of the remaining modes (SERIAL ADDRESS IN, SERIAL DATA IN, SERIAL DATA OUT) but data movement will be halted.

Setup

The SETUP instruction is necessary for the ERASE and WRITE modes. It isolates the particular addressed row and prevents adjoining rows or words from being inadvertently disturbed. The NC7033 can be left in SETUP without any loss of performance.

Retention

Data retention is a measurement of data validity between refresh (rewrite) cycles. The ability to alter data yet retain it during power interruptions is unique to MNOS-LSI. Both features of alterability and retention are interrelated and require clarification. The time in which data remains valid is inversely related to the number of rewrite/refresh cycles (see Figure 2). Excessive overstress of the nitride layer by too many erase and write cycles diminishes its ability to retain a charge.

Typically, long retention is not required for most applications. Data is normally altered or rewritten long before there is any danger of loss.

NC7033

Nitron

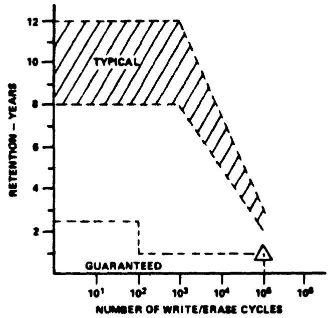


Figure 2. Retention Characteristics of MNOS.

INSTRUCTION SEQUENCES

With the exception of the ERASE mode, instructions may be presented in any random sequence without disturbance of data stored in the MNOS array. For the Erase mode the instruction sequence SETUP–ERASE must be followed.

Normal sequence of operation is as follows:

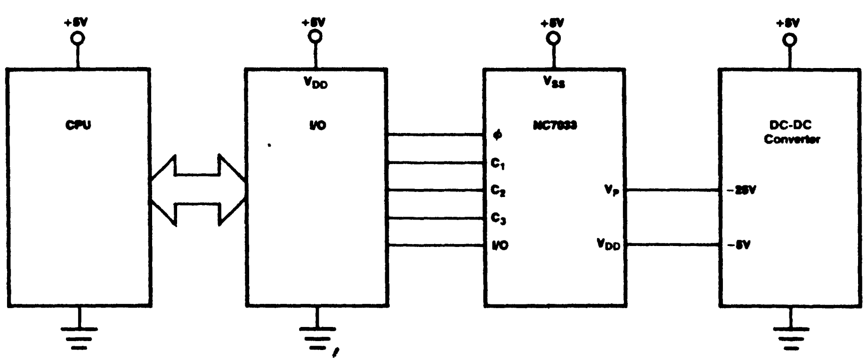
1. Power On (and Off) should be made in the absence of SETUP, ERASE or WRITE instruction codes. The power supplies then can be turned on or off in any sequence without disturbance of the data. Note that when V_P is open circuit or at V_{DD} the data in the array is always protected indpendent of the instruction being clocked in.
2. Select SERIAL ADDRESS IN command.
3. Chip is addressed for five clocks to enter five bits of address. The 5-bit binary address code (00000 to 10100) shifts the MSB into the chip first (see Figure 1B).
4. Other functions on the selected address can be performed as shown in Figures 1C, 1D and 1E.

SERIAL ADDRESS IN DECODING

WORD	MSB B5	B4	B3	B2	LSB B1
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0
8	0	0	1	1	1
9	0	1	0	0	0
10	0	1	0	0	1
11	0	1	0	1	0
12	0	1	0	1	1
13	0	1	1	0	0
14	0	1	1	0	1
15	0	1	1	1	0
16	0	1	1	1	1
17	1	0	0	0	0
18	1	0	0	0	1
19	1	0	0	1	0
20	1	0	0	1	1
21	1	0	1	0	0

B5 ENTERS THE CHIP FIRST
B1 ENTERS THE CHIP LAST

TYPICAL INTERFACE SCHEMATICS



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