HP 12897A
DUAL CHANNEL
PORT CONTROLLER

THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and F-Series Computers Engineering and Reference Documentation and is not available separately.

CONTENTS

12897 DUAL CHANNEL PORT CONTROLLER OPTION

Theory of Operation

1.0 INTRODUCTION

This document provides a Theory of Operation for the 12897 Dual Channel Port Controller (called DMA in this document) option board for the 2105 , 2108 , and 2112 computers. Discussion is conducted on the functional block, programming, and detailed operation levels. Block diagrams, logic diagrams, and timing diagrams are used to show operation. A thorough understanding of this document is essential when performing maintenance or troubleshooting on the 12897 option.

2.0 GENERAL DESCRIPTION

The 12897 DMA option consists of a single 2100-size board which is inserted into the top connector of the memory backplane of the 2105, 2108, or 2112 computers. A 50-connector flat-cable connects between it and the power crossover PCA to provide additional signals.

The 12897A DMA option is functionally equivalent to the DMA option for the 2100A, and is programmed exactly the same.

The DMA option allows the user to initiate block word transfers between selected I/O devices and memory. DMA then controls the I/O device during the transfers, stealing memory and I/O cycles from the CPU, but not requiring CPU intervention until completion of the transfer.

DMA is capable of stealing every consecutive I/O cycle, (about 1.62 usec) and can therefore transfer around 616,666 words per second. There are two channels of DMA, each of which may be separately assigned to operate with any I/O interface, including those in the 12979 I/O Extender. When both channels are operating simultaneously, channel 1 has priority over channel 2. The combined total transfer rate is 616,666 words/second,

so channel 2's maximum rate is 616,666 minus channel 1's actual rate.

When DMA is operating, it takes priority over the CPU for both memory accesses and control of the I/O system. The CPU may not access memory nor initiate an I/O cycle while DMA is cycle-stealing. The CPU can normally complete a memory operation in 976 nanoseconds, (read and obtain data) which need not be synchronized with the I/O system. The transfer rate available to the CPU is about 1.6 times the difference between 616,666 words per second and the combined total transfer rate of both DMA channels.

DMA transfers are initiated by an initialization routine and then hardware controls the transfers automatically. The initialization routine tells DMA which direction to transfer the data (in or out), where in memory to put the data, which I/O channel to use and how much data to transfer. completion of the transfer is signalled by an interrupt to location 6 (channel 1) or 7 (channel 2), if the interrupt system is enabled. It is also possible to check for completion by testing the status of the flag of select code 6 (channel 1) or select code 7 (channel 2). A block transfer can be aborted by an STF 06 or STF 07 instruction.

2.1 Basic Block Diagram

Refer to figure 1 for the following discussion of the basic organization of the DMA option.

2.1.1 Interrupt and I/O Control Logic

The functions of this logic are: to decode I/O signals from the CPU and control other elements of the DMA logic; to decode timing signals which control DMA operation; to generate interrupt requests; to fit DMA to the I/O system as a standard interface card.

2.1.2 Initialization logic

This logic contains the three oeprator control words which determine the nature of the transfers to be done.

The word count, memory address, select code of the I/O device, and control information are stored there during the initialization routine. The word count and memory address are incremented during DMA cycles. This logic notifies the interrupt and cycle stealing logic when a block transfer is completed.

2.1.3 Cycle Stealing Logic

This logic determines if a device is to be serviced by DMA, and generates the proper signals to control the CPU, memory, and the I/O device during a cycle-steal.

2.2 Interface Signal Descriptions

This section describes the main signals which are important in operation of the 12897 DMA option. Standard I/O signals and busses are not included. All signals are TTL-compatible, ground true unless otherwise specified.

2.2.1 Input Signals

SRQ10-SRQ25 "Service Request". Positive true. CTL compatible. Generated by devices requesting service, synchronously or asynchronously with T2. If the particular I/O device has been assigned a DMA channel, the its SRQ alerts logic to initiate a DMA cycle.

$\overline{\text{DMARQ1}}$, $\overline{\text{DMARQ2}}$ "DMA Request". CTL compatible, ground true. Generated by an I/O Extender when an I/O device in the Extender has been assigned a DMA channel, and requests service on it. $\overline{\text{DMARQ1}}$ is a request for channel 1

(select code 6), and $\overline{\text{DMARQ2}}$ is a request for DMA channel 2 (select code 7).

2.2.2 Output Signals

$\overline{\text{DMACYC}}$. "DMA Cycle". True through periods T6-T5 if a DMA cycle is being done. Used to notify the system that a DMA cycle is in progress.

$\overline{\text{DMALO}}$/$\overline{\text{RACLO}}$. "DMA/Random Access Channel Lockout". Identical signals, both OR-tieable. True during T5-T2 if a DMA/RAC cycle has been requested. Used to assure DMA of unhindered access to memory and I/O system.

$\overline{\text{DMAEN}}$. "DMA Enable". Sent to CPU to switch control of M-bus to DMA during a DMA cycle, and to enable the DMA Memory Address Registers onto the M-bus.

$\overline{\text{DMAREAD}}$. "DMA Read". To memory, to allow memory to time refresh around DMA, if necessary. True during T6-T5 of DMA output transfer.

$\overline{\text{READ}}$. "Read". To memory. True during T2 of Read cycle. Downward edge initiates a Read cycle in memory. OR-tieable.

$\overline{\text{DMAIOO}}$. "DMA I/O Output" to CPU. Gates S-bus onto I/O Bus during T3 of output transfer.

$\overline{\text{DMAFRZ}}$ "DMA Freeze" to the CPU. Freezes CPU clocks and prevents CPU from using the S-BUS while DMA uses it. True during T3.

$\overline{\text{DMAIOI}}$ "DMA I/O Input" to CPU board. Gates the I/O-bus onto the S-bus. True during T2-T3 of a DMA input transfer.

$\overline{\text{DMALCH}}$ "DMA Latch" to CPU board. Holds data on the I/O-bus through completion of DMA output transfer. True during T4-T5.

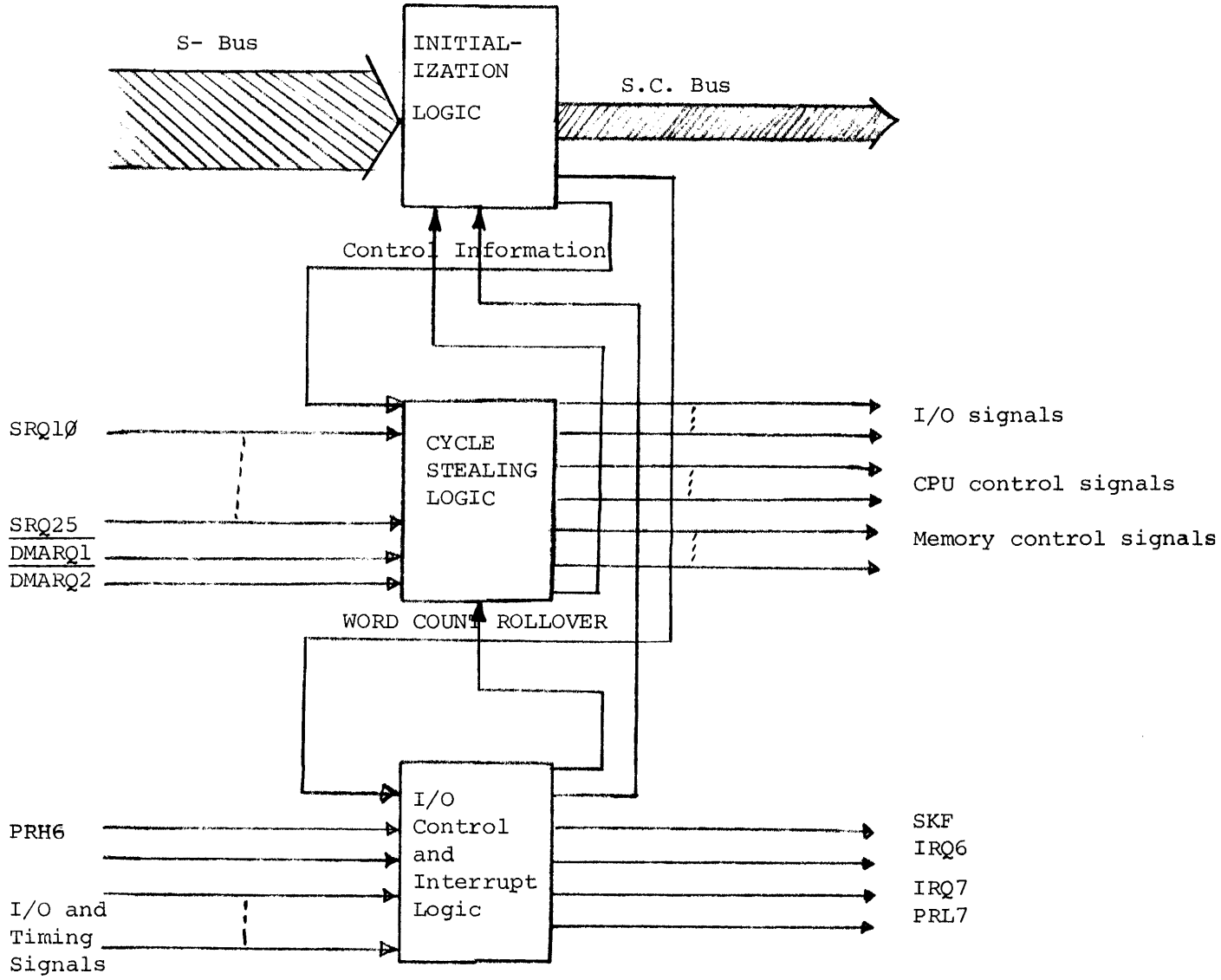


FIGURE 1

DMA OPTION BLOCK DIAGRAM

$\overline{\text{TEN}}$ "T Register Enable" to memory. Gates the T-register in memory onto the S-bus. True during T3 of DMA output transfers. OR-tieable.

$\overline{\text{TST}}$ "T Register Store" to memory. Informs memory to clock data on S-bus into the T-register. True during T3 of DMA input transfers. OR-tieable.

$\overline{\text{WRITE}}$ to memory. Downward edge initiates a write cycle in memory. True during T4 of input transfers. OR-tieable.

3.0 PROGRAMMING

The 12897 DMA option is programmed in exactly the same manner as the DMA option for the 2100A computer. Included below is only a brief summary of the actions performed by the I/O instructions affecting the 12897 DMA operation. Select codes 2 and 6 refer to DMA channel 1, while select codes 3 and 7 refer to channel 2.

3.1 Initialization Instructions

OT*	06	Load the A or B register via the S-bus into the Service
OT*	07	Select Register (bits 0-5, 13, 15). This is Control Word 1.
STC	02	Set the CTL2FF or CTL3FF high. Used to prepare
STC	03	DMA to receive Control Word 2.
CLC	02	Set the CTL2FF or CTL3FF low. Used to prepare DMA to receive Control Word 3.
OT*	02	Load the A or B register via the S-bus into the DMA
OT*	03	Memory Address Register (Control Word 2) if STC__FF is low or into the Word Count Register (Control Word 3) if STC__FF is high. Each channel has its own such registers.

3.2 Control Instructions

STC	06	Turns on DMA to look for SRQ's from I/O devices
STC	07	specified to begin the transfer described by the control words.
STF	06	**Set** the channel Flag Buffer flip-flop, which disables
STF	07	further DMA cycles on that channel, and will set the flag at the proper time.
CLF	06	Clears the Flag flip-flop, Flag Buffer flip-flop, and
CLF	07	IRQ flip-flop for that channel.

3.3 Status Instructions

SFS	06	SKIP next instruction if flag flip-flop is set (or clear)
STS	07	on that channel. If set, the block transfer has been
SFC	06	completed.
SFC	07	
LI*	02	READS the remaining word count (2's complement of it)
LI*	03	for the channel. May be used to determine how much of a DMA block transfer has been completed.

4.0 DETAILED THEORY OF OPERATION

The following discussion describes each functional section in operational detail, followed by a discussion of overall DMA operation during initiation, input and output transfers, and interrupt request generation. Logic for channel 1 is identical to that for channel 2, so only channel 1 will be discussed. It is not difficult to discover the channel 2 counterparts to channel 1.

4.1 Initialization Logic

Information from Control Words 1, 2 and 3 are loaded into registers in this logic, and used for transfer control when DMA is activated. The registers are loaded from the S-bus during the I/O instructions listed in section 3.1. The S-bus is buffered (U53, U93) before being distributed to the six registers (3 per channel). Refer to figures 2 and 3.

4.1.1 Control Word 1: register and logic

During I00 of a OT* 06, Control Word 1 is loaded into the Service Select Register (U64), Bits 0-5 contain the select code of the device under control of channel 1, and are designated SSR1-0 through SSR1-5. Bit 13 of the S-bus is stored as CLCSEL1, and is used to specify whether CLC is to be issued to the I/O device at the end of a block transfer. Bit 15 of the S-bus is stored as STCSEL1, and is used to specify if a STC is to be issued to the I/O device at the end of each word transfer (except the last, if it is an input transfer).

When DCYC1 is high (cycle in progress on channel 1) the Service Select Register is buffered (U63) onto the Select Code Bus to select the specified device for DMA control. This buffer also outputs the signals $\overline{\text{INCWC1}}$ at T2, and $\overline{\text{INCMR1}}$ at P5 of T5 during DCYC1. These signals increment the Word Count Register and Memory Address Register, respectively.

4.1.2 Control Word 2: register and logic

CTL2FF (U115, pin 13) must be low in order to load the second control word into the Memory Address Register (MAR). This is assured by executing a CLC 02 instruction which clears the R-S flip-flop CTL2FF.

A succeeding OT* 02 instruction will load the A or B register into the Memory Address Register (U11, 12, 131, 132) with the negative edge of $\overline{\text{LOADMAR1}}$. The MAR is a 15 bit register containing a 15-bit ripple counter (loaded from bits 0-14 of the S-bus) and a single D flip-flop (loaded from bit 15 of the S-bus) called INFF1 (U11-pin 5). If INFF1 is high, then a DMA input transfer is to be done on channel 1. If low, then an output transfer. This flip-flop does not change once the MAR is loaded. The MAR counter is incremented by the downward edge of $\overline{\text{INCMR1}}$ at the start of P5 of T5 during a DMA cycle on channel 1 (DCYC1).

The MAR is enabled onto the M-bus through a set of buffers (U13, 133) during DMAEN in DCYC1. DMAEN also disables the CPU M-register from using the M-bus.

Note that M-bus bit 15 is forced low during DMAEN in DCYC1, and that it is forced high during DMAEN in DCYC2. Bit 15 is monitored by the Memory Management option board for distinguishing DMA channels during transfers

4.1.3 Control Word 3: register and logic

CTL2FF (U115 pin 13) must be high to be able to load the third control word into Word Count Register 1. This is effected by issuing an STC 02 instruction, which sets the R-S flip-flop.

A succeeding OT* 02 instruction will enable the A or B register into the Word Count Register (U41, 42, 101, 102) via the S-bus on the downward edge of $\overline{\text{LOADWC1}}$, and latch the data on the rising edge. The Word Count Register is a 16-bit synchronous counter loaded with the two's complement of the number of words to be transferred under DMA channel 1 control. It performs a carry-look-ahead for each group of four bits while

$\overline{\text{INCWC1}}$ is low. If all outputs of the low order bits are high when $\overline{\text{INCWC1}}$ goes low, then the carry output, pin 12, goes low, which goes to pin 5 of the next group, performing the same function. If all bits of the Word Count Register are high, then $\overline{\text{INCWC1}}$ going low will result in WCR1 (Word Count rollover) going high, indicating that the current transfer is the last. The register increments at the rising edge of $\overline{\text{INCWC1}}$. $\overline{\text{INCWC1}}$ is low during T2 of a channel 1 cycle (DCYC1).

The Word Count Register is enabled onto the S-bus through the buffer (U43, 103) during LI* 02 instructions, and stored onto the A or B register on the CPU.

4.2 I/O Control and Interrupt Logic

4.2.1 Timing Decoders

To generate I/O signals at the proper times, DMA needs to have a way to generate T2-T6 in sync with the CPU. To do this, DMA receives the TA, TB, TC signals from the CPU, and decodes them (U47, U46) to provide the required time periods.

4.2.2 I/O Instruction Decoding

DMA decodes the Select Code Bus to SCL2, SCL3, SCL6, SCL7, which are high if the appropriate DMA channel is referenced on the bus. ANDed with IOG, they generate SSL2, SSL3, SSL6, SSL7, respectively, which are high during I/O instructions for the specified DMA select codes. These signals are used as described below:

SSL2 (a) in conjunction with STC or CLC, set or clear the
SSL3 STC2FF or STC3FF.

(b) in conjunction with IOG, generate $\overline{\text{LOADWC}}$ or $\overline{\text{LOADMAR}}$

(c) in conjunction with IOI, gate the Word Count Register onto the S-bus.

SSL6 (a) enable buffer U134 or U136, respectively, which
SSL7 then enables STC, CLC, CLF, and STF to the appropriate DMA channel flip-flop. The buffers OR-tie the status of the two channel flags for the skip logic (pins 1, 2). Only one channel flag status is selected for test during SFS or SFC, since only one buffer may be enabled at a time.

(b) in conjunction with IOG, load the Service Select Register.

4.2.3 Interrupt logic

When DMA is turned on, an STC 06, C instruction sets the Channel Control, CONT6FF (U115), and clears the Flag, Flag Buffer, and IRQ flip-flops (U125).

The interrupt generating sequence may be initiated in two ways. It is assumed that CONT6FF is high, the interrupt system is enabled (IEN5 is high), and the priority chain is intact to DMA (PRH6 is high). Refer to figure 4. If any one of these conditions is not met, no interrupt will be requested.

a. WCR1 (Word Count Rollover) is high. This indicates that the last word transfer is in progress. This sets FBFF1 and clears the transfer enable flip-flop (TRENFF1).

b. Issuing an STF 06 instruction. This sets FBFF1.

T2 following setting of the Flag Buffer, the Flag (FLG6FF) is set high. T5 following setting of FBFF1, TRENFF1 is set low, disabling further channel 1 cycles.

The T5 following setting of FLG6FF, IRQ6FF is set. IRQ6FF is high during T5-T6 and low T2-T4 until the interrupt is granted. However, if a higher priority device (Powerfail, Parity, or Memory Protect) sets its flag, then PRH6 will go low, preventing DMA from interrupting until the other device has been serviced and PRH6 is high again.

When the DMA interrupt request is acknowledged, IAK occurs at P3, 4, 5 of T6. IAK in conjunction with IRQ6FF clears FBFF1.

4.3 Cycle Stealing Logic

The cycle stealing logic compares the Service Select Register to the SRQ lines coming from I/O interface cards to determine if a cycle is to be requested. It resolves access priorities between the two DMA channels, initiates the cycle, and controls the generation of various signals to memory, the CPU, and the I/O interface to effect the desired transfer. Refer to figure 5.

4.3.1 Cycle Request Logic

This consists primarily of a 16-to-1 multiplexor (U51). SSR1-0 to SSR1-5 select a SRQ line to monitor. When that SRQ line goes high, indicating the Flag has been set on the interface card with the select code specified in the SSR, then the REQ1 line goes high. $\overline{\text{DMARQ1}}$ indicates a request for DMA channel 1 from the I/O Extender. It also sets REQ1 high.

4.3.2 Cycle Initiating Logic

The Cycle Request Register (U16) is the focal point for initiating DMA cycles on either channel. Refer to figure 5. It is clocked every trailing edge of P5.

When an STC 06 instruction is executed, the Transfer Enable flip-flop (TRENFF1) is set. This allows the cycle initiating logic to monitor the REQ1 line (U35A). If there is no power failure (PRH5 is high), then when REQ1 goes high, the Cycle Request 1 flip-flop, CYCRQ1, will be set at the end of T4. As long as CYCRQ1 is high, DMA channel 2 cannot take a cycle (gate U26B). Once CYCRQ1 goes high, it is kept high until the end of the next T4. The NOR of CYCRQ1 and CYCRQ2 during T5 through T2 is $\overline{\text{DMALO}}$.

$\overline{\text{DMALO}}$ goes to the CPU to perform the following functions:

a. Prevent setting the I/O Group Enable flip-flop.

b. Freeze the CPU if it attempts to access memory, perform I/O instructions, or load the central Interrupt Register.

c. Set the Interrupt Override ff on the CPU to prevent interrupt recognition during the cycle.

The DCYC1 flip-flop follows CYCRQ1, delayed by one T-period. It is valid T6-T5, and enables the signal generation logic for a DMA transfer. The DCYC2 flip-flop may not be set until the end of T5 after CYCRQ1 goes low, if CYCRQ2 is high. Channel 2 may thus take a cycle immediately after channel 1. The NOR of DCYC1 and DCYC2 is $\overline{\text{DMACYC}}$, which is sent to the CPU to prevent granting of interrupt requests until DMA has prevented its controlled device from requesting CPU service.

When FB6FF is set, then TRENFF1 is set low on the next T5, to give control of the Select Code Bus to DMA and to prevent CPU I/O signals.

4.3.3 Signal Generation Logic (Figure 5)

DCYC1 controls two multiplexers (U24, 34) which select transfer control information from one or the other DMA channel's initialization logic (INFF__, STCSEL__, and CLCSEL__) and Flag Buffer status. These signals determine the exact combination of output signals necessary to execute a DMA transfer. Six flip-flops are used to assist in this generation (U14, U17, U27). See sections 4.4, 4.5 for timed signals for input and output transfers. The signal "IN" (U34) selects the proper set of signals for input or output transfers.

4.4 DMA Input Transfers

The following table describes the algorithm for executing an input transfer on DMA channel 1. Refer to figure 6 for a diagram of timing signals for (a) normal cycle and (b) end-of-block-transfer cycle. It is assumed that TRENFF1 is high initially and that SRQ is asserted in time to generate REQ1 by P5 of T4.

Time	Signals Initiated	Action
T5	$\overline{\text{DMALO}}$	Prevent CPU from interfering with upcoming cycle. Prevent interrupt service in the CPU.
T6	$\overline{\text{DMACYC}}$	Start cycle, enable signals, give DMA control of Select Code Bus, servicing in CPU.
	$\overline{\text{DMAEN}}$	Spilling MAR1 onto M-bus, removing CPU from M-bus.
T2	$\overline{\text{INCWC1}}$	Check for word count rollover, increment word count on trailing edge. If WCR1 occurs, set FBFF1 high.
	IOI	Tel I/O card to spill buffer onto I/O bus.
T3	$\overline{\text{DMAFRZ}}$	Freeze CPU, free the S-bus.
	$\overline{\text{DMAIOI}}$	Gate I/O bus onto the S-bus.
	$\overline{\text{TST}}$	Clock S-bus into T-register.
	STC	Issue STC to interface card if STCSEL1 is high and FBFF1 is low.
	CLC	Issue CLC to interface card if CLCSEL1 is high and FBFF1 is high.
	CLF	Issue CLF to interface card if FBFF1 is low.

Time	Signals Initiated	Action
T4	$\overline{\text{WRITE}}$	Initiate write cycle in memory at address on M-bus.
	EDT	Issue to interface card if FBFF1 is high.
T5	$\overline{\text{INCMR1}}$	Increment the Memory Address Register. Set TRENFF1 low if FBFF1 is set.

4.5 DMA Output Transfers

The following table describes the algorithm for executing an output transfer on DMA channel 1. Refer to figure 7 for a diagram of the Timing signals. It is assumed that TRENFF1 is high initially, and that SRQ is asserted in time to generate REQ1 by P5 of T4. Both the case of (a) normal cycles and (b) end-of-transfer cycles are illustrated

Time Period	Signal Initiated	Action
T5	$\overline{\text{DMALO}}$	Prevent CPU from interfering with upcoming cycle.
T6	$\overline{\text{DMACYC}}$	Start cycle, enable signals, prevent CPU interrupt servicing.
	$\overline{\text{DMAREAD}}$	Tell memory to schedule refresh during T4-T5.
	$\overline{\text{DMAEN}}$	Enable DMA Memory Address Register 1 onto M-bus.
T2	$\overline{\text{INCWC1}}$	Check for Word Count Rollover. If WCR1 high, **then** set FBFF1 Increment Word Count at trailing edge.
	$\overline{\text{READ}}$	Initiate Read cycle.
T3	$\overline{\text{DMAFRZ}}$	Freeze CPU while DMA uses S-bus.
	$\overline{\text{TEN}}$	Enable data in T-register onto S-bus.
	$\overline{\text{DMAIOO}}$	Enable S-bus onto I/O-bus.
	$\overline{\text{DMALCH}}$	Hold data on I/O-bus. This signal allows S-bus to be used by CPU during following time periods.
	IOO	Clock I/O-bus into input buffer on I/O interface card.
	CLF	Issue CLF to interface card.
	STC	Issue STC to interface card if STCSEL1 is high.
	CLC	Issue CLC to interface card if FBFF1 is high and CLCSEL1 is high.

Time Period	Signal Initiated	Action
T4	EDT	Issue to interface card if FBFF1 is high.
T5	$\overline{\text{INCMR1}}$	Increment Memory Address Register Set TRENFF1 low if FBFF1 is high.

4.6 System Reset Signals

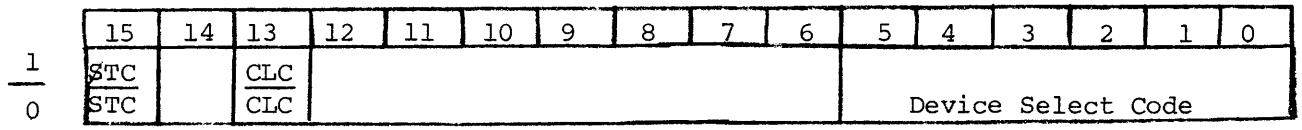
4.6.1 POPIO

POPIO occurs during power-up or by pressing the Preset button on the front panel in the HALT mode. POPIO clears the Flag buffers on both channels (FBFF1, FBFF2). This terminates any block transfers in progress.

4.6.2 CRS

CRS occurs during POPIO or during STC 0 instructions. CRS clears CTL2FF, CTL3FF, CTL6FF, CTL7FF, TRENFF1, and TRENFF2, which disables DMA from interrupting and terminates any block transfers in progress.

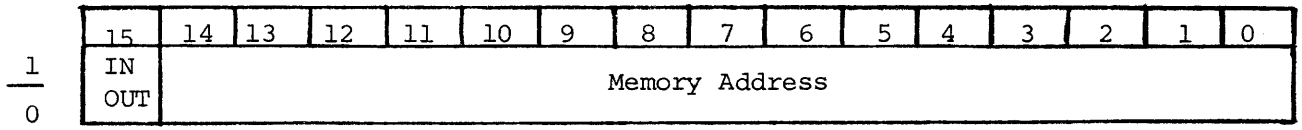
CONTROL WORD 1



STC: issue STC at the end of every cycle, except the last, if input.

CLC: issue CLC at the end of last word transfer.

CONTROL WORD 2



CONTROL WORD 3

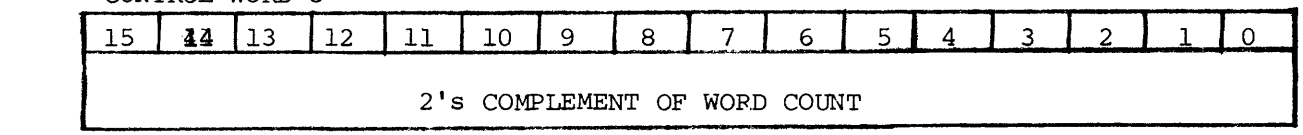


FIGURE 2

DMA CONTROL WORD FORMATS

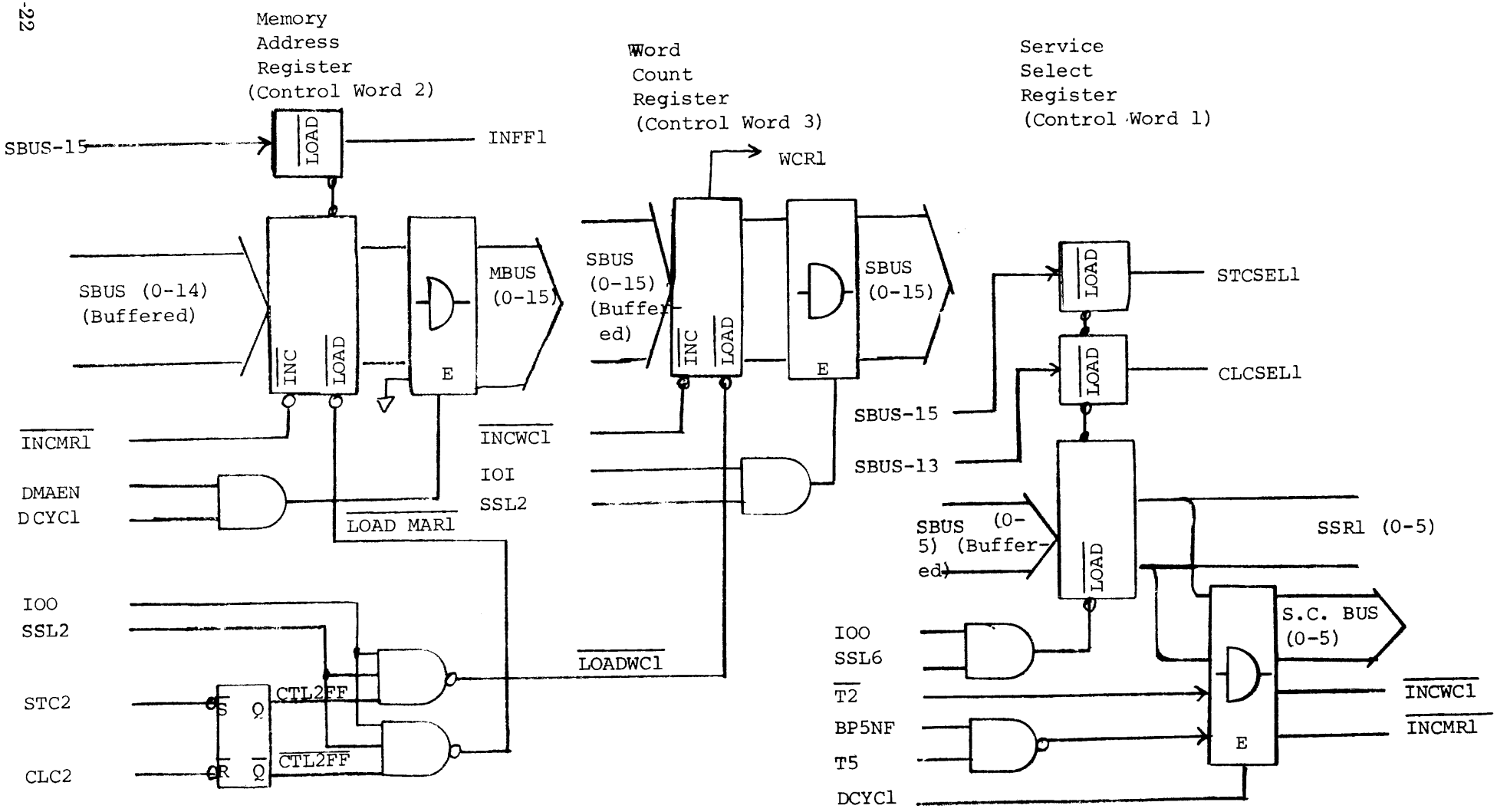


FIGURE 3

INITIALIZATION LOGIC

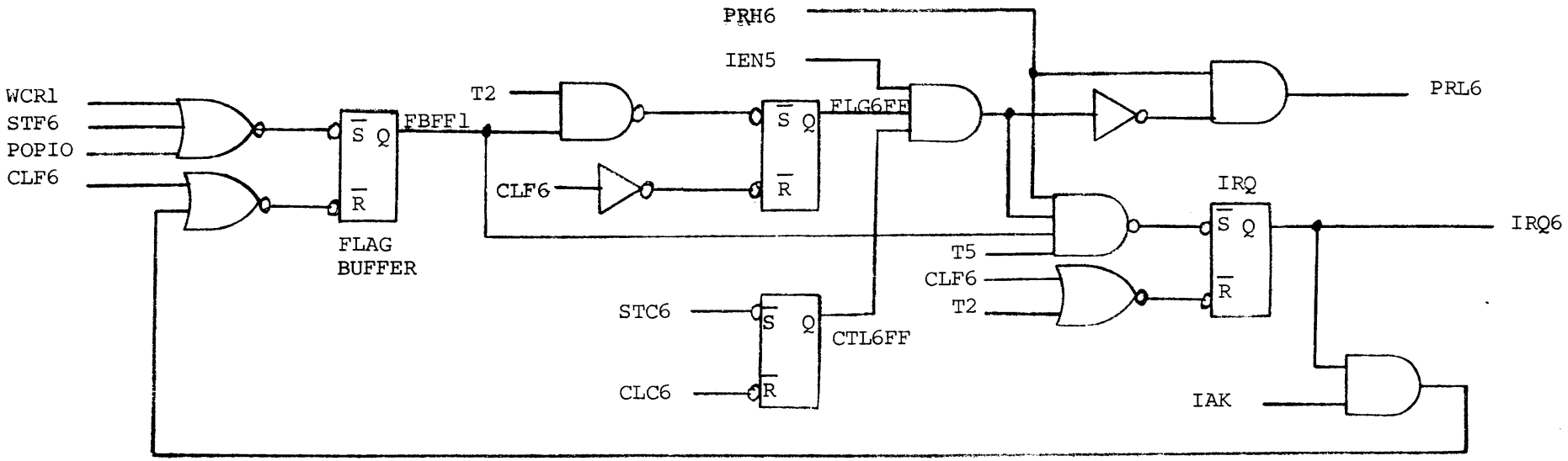


FIGURE 4

INTERRUPT AND PRIORITY LOGIC

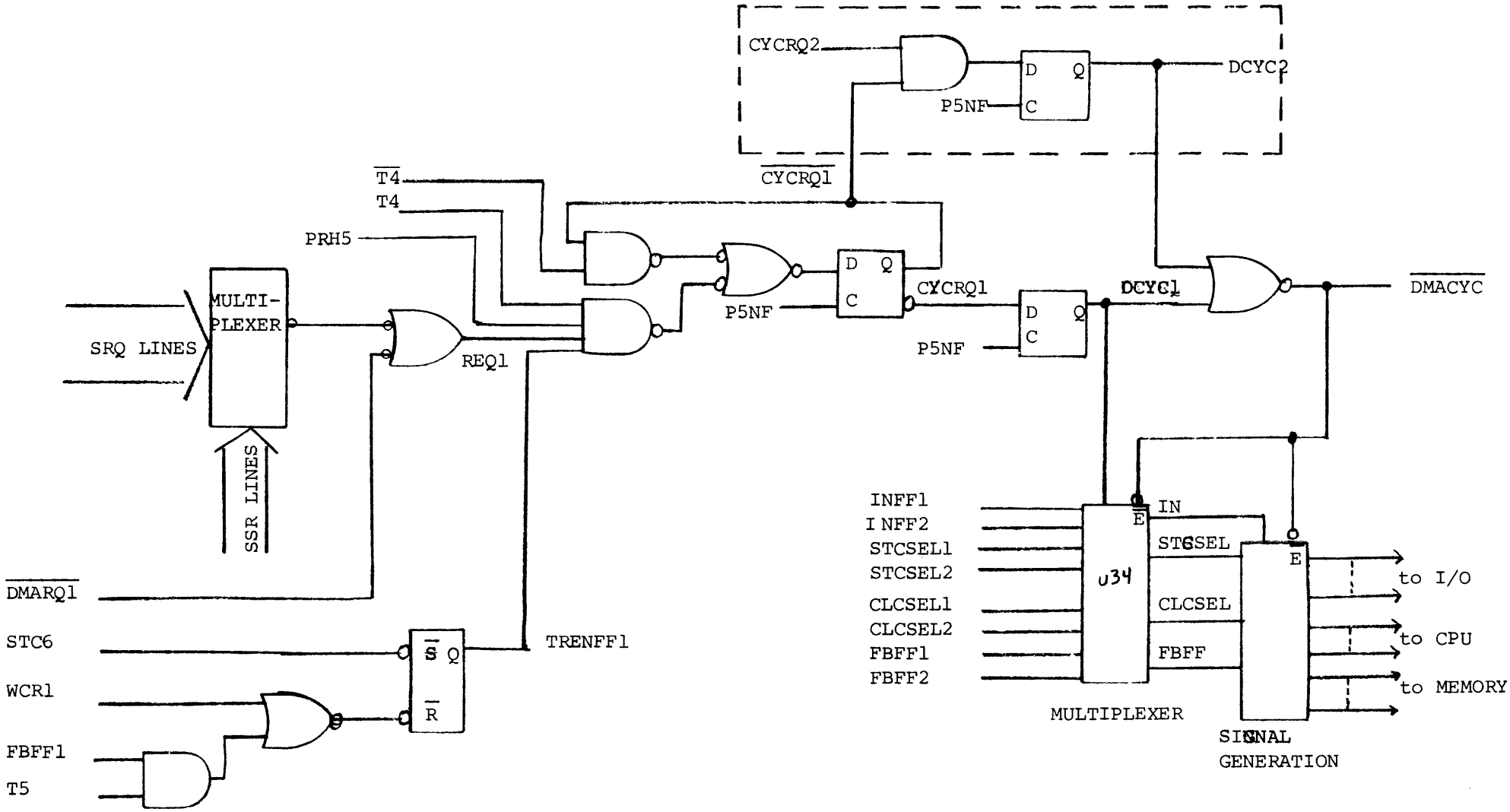


FIGURE 5

CYCLE STEALING LOGIC, CHANNEL 1

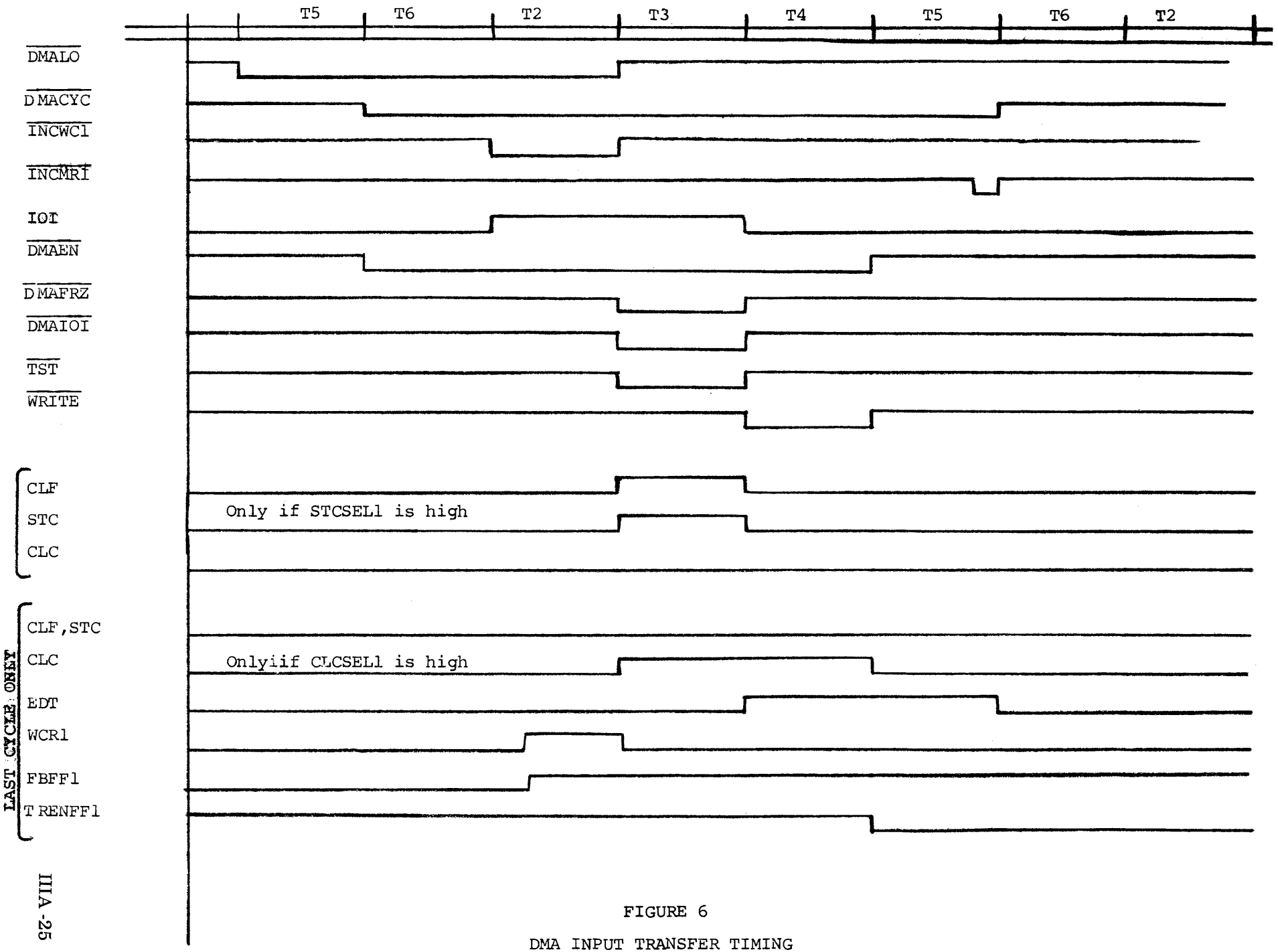


FIGURE 6

DMA INPUT TRANSFER TIMING

CHANNEL 1 ILLUSTRATED

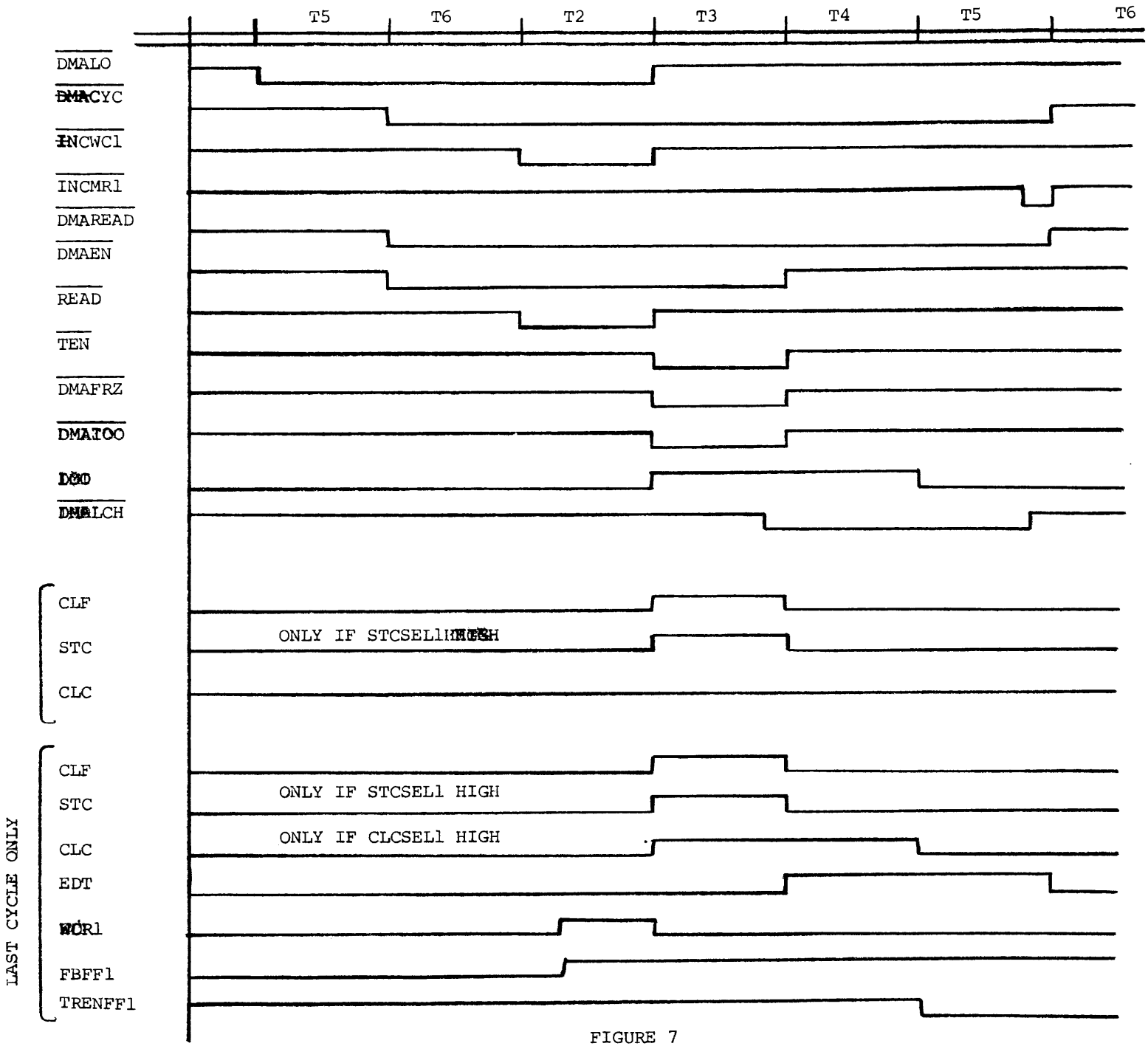
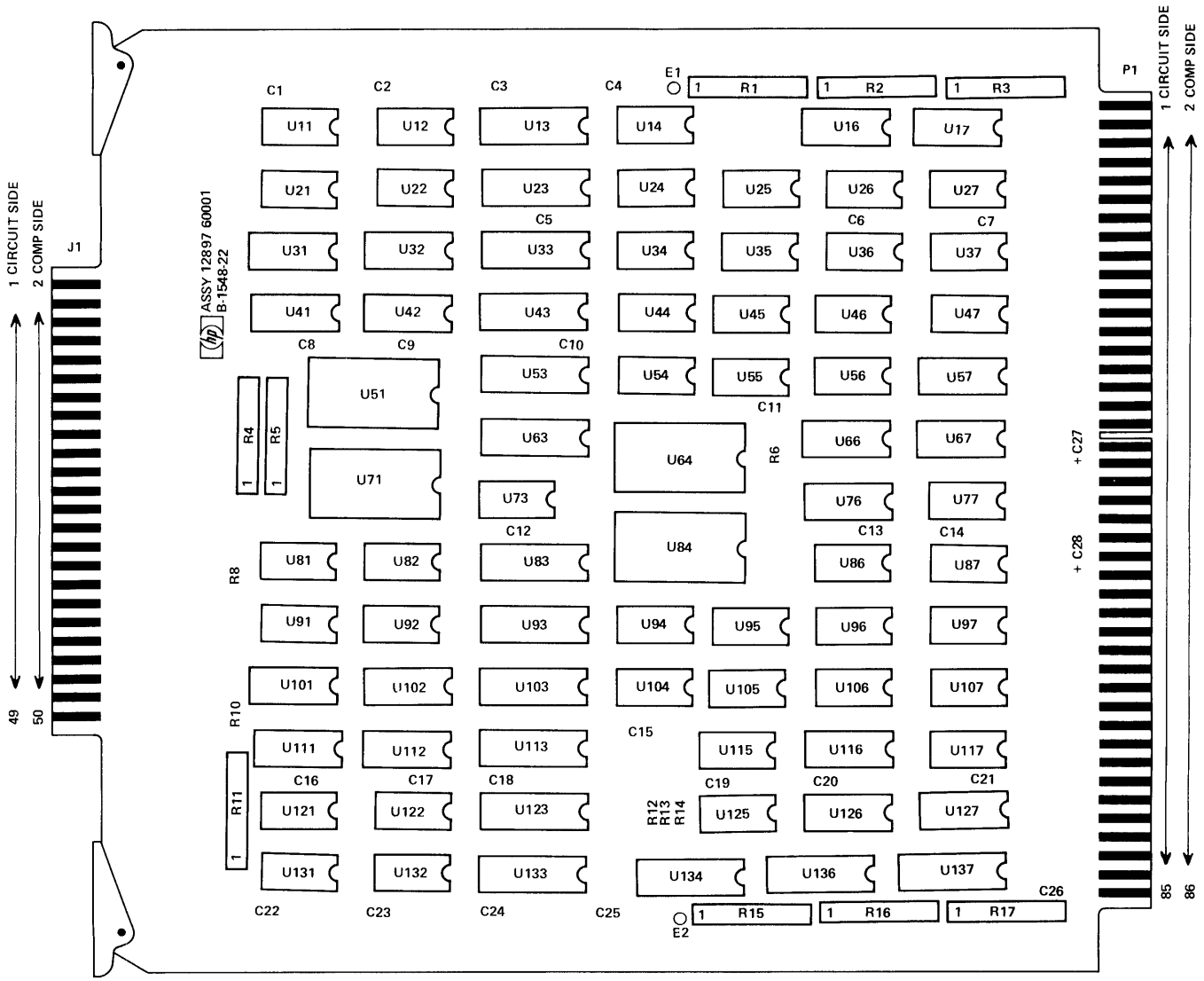


FIGURE 7

DMA OUTPUT TRANSFER TIMING, CHANNEL 1



Dual Channel Port Controller Assembly
12897-60001

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
00	C1-26	CAP .01UF		0160-2055		U	26
01	C27,28	CAP 10UF 10%		0180-0374		D	2
00	E1,2	STUD SOLDER TERM		0360-0294		U	2
01	R13,14	RES 147 1%.125		0698-3438		D	2
01	R8,10,12	RES 1K 1%.125		0757-0280		D	3
00	R6	RES 1.5K 1%.125		0757-0427		U	1
01	R24,115	SOCKET 16 DIP LO		1200-0482		U	2
		PIN GRV .062X.25		1480-0116		U	2
01	R2,4,5,11,16,17	RES NET 7X1.5K		1810-0020		U	6
00	R1,15	RES NET 7X1K		1810-0030		U	2
00	R3	RES NET 7X500		1810-0080		U	1
01	U26,44,46,94,97	IC MC3001P		1820-0141		U	5
00	U81	L/T BUY RES. USE		1820-0205		U	1
01 03	U31,32,41,42,101 102,111,112	IC SN74193N		1820-0233		U	8
00	U86	IC SN7402N		1820-0328		U	1
01 03	U36,56,82 105,106	IC SN74H00N		1820-0370		U	5
		IC SN74H10N		1820-0371		U	2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
00	U95,96			1820-0371			
01	U45,55	IC SN74H11N		1820-0372		U	2
01	U54,104	IC SN74H04N		1820-0424		U	2
01	U24,34	IC 9322PC		1820-0616		U	2
00	U91	L/T BUY RES. USE		1820-0617		U	1
00	U35	IC SN74H22N		1820-0619		U	1
01	U115,116,125,126	IC 9314PC		1820-0626		U	4
01	U51,71	IC SN74150N		1820-0640		U	2
00	U25	IC SN74S03N		1820-0682		U	1
01	U47,77	IC SN74S04N		1820-0683		U	2
00	U37	IC SN74S05N		1820-0684		U	1
00	U117	IC SN74S10N		1820-0685		U	1
00	U92	IC SN74S11N		1820-0686		U	1
01	U14,27	IC SN74S74N		1820-0693		U	2
00	U17	IC SN74H106N		1820-0715		U	1
01	U64,84	IC 9308PC		1820-0742		U	2
01 03 05	U13,23,33,43, 63,83,103 113,123,133,137	IC HP147A		1820-0755		U	11
		IC HP147B		1820-0756		U	2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01	U134,136			1820-0756			
01	U53,93	IC HP106A		1820-0759		U	2
00	U107	IC SN7406N		1820-0761		U	1
01 03	U11,12,21,22,121 122,131,132	IC SN74197N		1820-0765		U	8
00	U73	IC SN7427N		1820-0782		U	1
00	U16	IC SN74175N		1820-0839		U	1
01	U57,66,67,76,127	IC 8T13B		1820-1080		U	5
00	U87	IC SN74S38N		1820-1451		U	1
		LABEL-USA		7120-6830		L	1
00	W1	WIRE JUMPERS		8159-0005		D	1
		EXTRACTOR-PC		5040-6001		W	1
		EXTRACTOR-BLACK		5040-6068		W	1

DWG	REVISION
-51	A B C D E F G
-52	A B C D D E G
-53	A B B C C C
-54	A B C D D E G

REV	REF	SERIES/PREFIX	DWGS AFFECTED
A	ORIG	1353	ALL
B	22-2098	1415	ALL
C	22-2301	1435	ALL
D	ERRATA	NA	ALL
E	22-2620	1515	-51
F	22-2652	1520	-51,-52,-54
G	22-3011	1548	-51,-52,-54

TIMING LOGIC

DMA CONTROL LOGIC

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITANCE VALUES ARE IN MICROFARADS AND ALL RESISTANCE VALUES ARE IN OHMS.
2. RESISTOR NETWORKS R2,R4,R5,R11,R16 AND R17 ARE 1.5K.

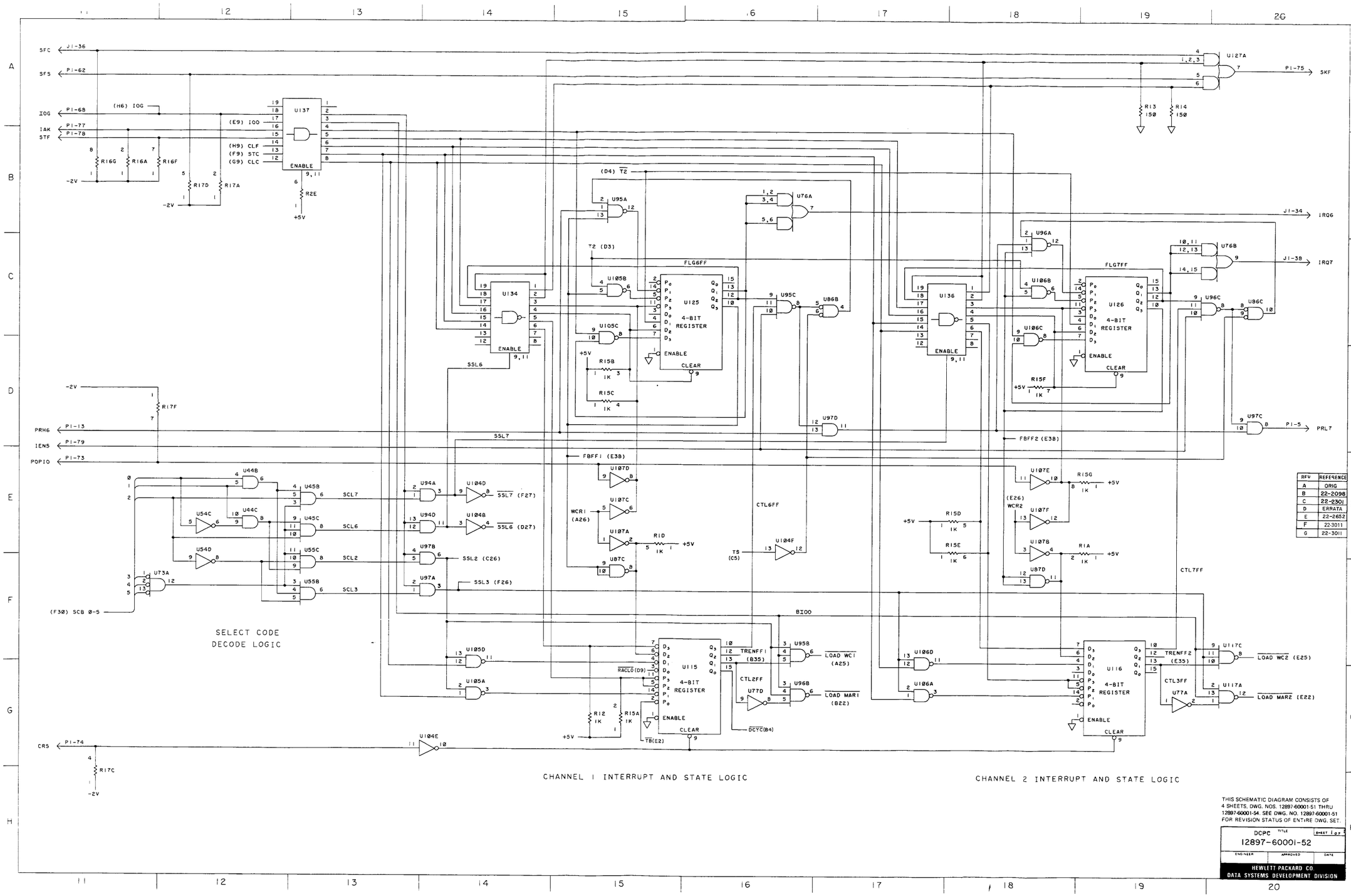
THIS SCHEMATIC DIAGRAM CONSISTS OF 4 SHEETS, DWG. NOS. 12897-60001-51 THRU 12897-60001-54

DCPC

12897-60001-51

ENGINEER | APPROVED | DATE

HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION



RFV	REFERENCE
A	ORIG
B	22-2098
C	22-2301
D	ERRATA
E	22-2652
F	22-3011
G	22-3011

REV	REFERENCE
A	ORIG
B	22-2098
C	ERRATA

CHANNEL 1 MEMORY ADDRESS REGISTER

CHANNEL 1 WORD COUNT REGISTER

CHANNEL 2 MEMORY ADDRESS REGISTER

CHANNEL 2 WORD COUNT REGISTER

THIS SCHEMATIC DIAGRAM CONSISTS OF 4 SHEETS, DWG. NOS. 12897-60001-51 THRU 12897-60001-54. SEE DWG. NO. 12897-60001-51 FOR REVISION STATUS OF ENTIRE DWG. SET.

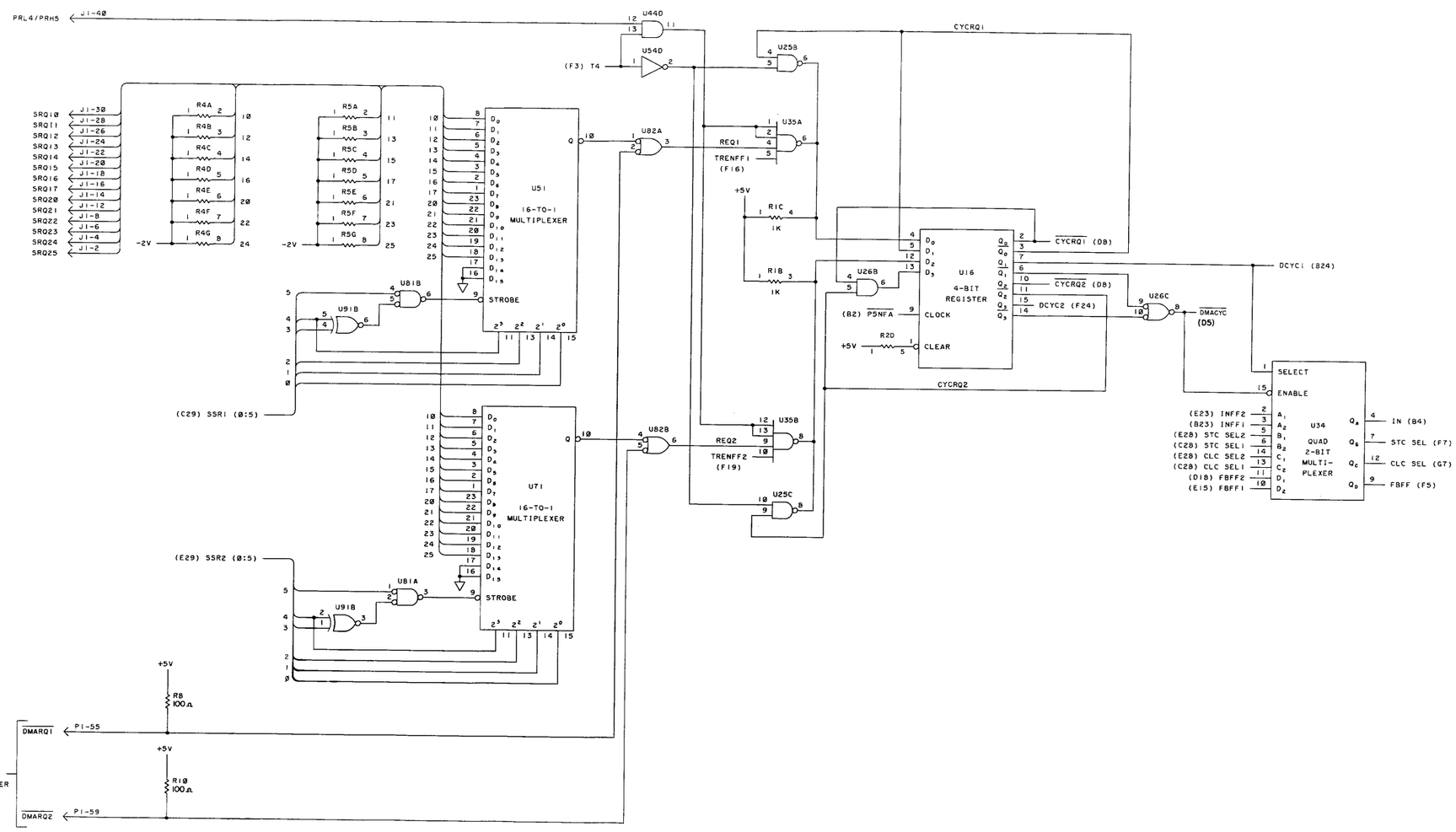
DCPC 12897-60001-53 SHEET 1 OF 2

ENGINEER	APPROVED	DATE

HEWLETT PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

REV	REFERENCE
A	ORIG
B	22-2098
C	22-2301
D	ERRATA
E	22-2652
F	22.3011
G	22-3010

CYCLE REQUEST LOGIC



THIS SCHEMATIC DIAGRAM CONSISTS OF 4 SHEETS, DWG. NOS. 12897-60001-51 THRU 12897-60001-54. SEE DWG. NO. 12897-60001-51 FOR REVISION STATUS OF ENTIRE DWG. SET.

DCPC	SHEET 1 OF 4
12897-60001-54	
ENGINEER	APPROVED / DATE

HEWLETT PACKARD CO
DATA SYSTEMS DIVELOPMENT DIVISION

HP 12897B
DUAL CHANNEL
PORT CONTROLLER

THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and F-Series Computers Engineering and Reference Documentation and is not available separately.

TABLE OF CONTENTS

12897B DUAL CHANNEL PORT CONTROLLER OPTION

Theory of Operation

1.0 INTRODUCTION

This document provides a Theory of Operation for the 12897 Dual Channel Port Controller (called DMA in this document) accessory for the 21MX Series computers. Discussion is conducted on the functional block, programming, and detailed operation levels. Block diagrams, logic diagrams, and timing diagrams are used to show operation. A thorough understanding of this document is essential when performing maintenance or troubleshooting on the 12897B accessory.

2.0 GENERAL DESCRIPTION

The 12897 DMA consists of a single 2100-size board which is inserted into the top connector of the memory backplane of the 21MX Series computers. A 50-connector flat-cable connects between it and the power crossover PCA to provide additional signals.

The 12897B DMA is functionally equivalent to the DMA for the 2100A, and is programmed exactly the same.

The DMA allows the user to initiate block word transfers between selected I/O devices and memory. DMA then controls the I/O device during the transfers, stealing memory and I/O cycles from the CPU, but not requiring CPU intervention until completion of the transfer.

DMA is capable of stealing every consecutive I/O cycle. There are two channels of DMA, each of which may be separately assigned to operate with any I/O interface, including those in the 12979 I/O Extender. When both channels are operating simultaneously, channel 1 has priority over channel 2.

In the 21MX E-series, the CPU may not access memory nor initiate an I/O cycle while DMA is cycle stealing. The 21MX M-series CPU may not initiate an I/O cycle but, is permitted one memory cycle per DMA cycle while DMA is cycle stealing.

DMA transfers are initiated by an initialization routine and then hardware controls the transfers automatically. The initialization routine tells DMA which direction to transfer the data (in or out), where in memory to put the data, which I/O channel to use and how much data to transfer. Completion of the transfer is signalled by an interrupt to location 6 (channel 1) or 7 (channel 2), if the interrupt system is enabled. It is also possible to check for completion by testing the status of the flag of select code 6 (channel 1) or select code 7 (channel 2). A block transfer can be aborted by an STF 06 or STF 07 instruction.

2.1 Basic Block Diagram

Refer to figure 1 for the following discussion of the basic organization of the DCPC accessory.

2.1.1 Interrupt and I/O Control Logic

The functions of this logic are: to decode I/O signals from the CPU and control other elements of the DMA logic; to decode timing signals which control DMA operation; to generate interrupt requests; to fit DMA to the I/O system as a standard interface card.

2.1.2 Initialization logic

This logic contains the three operator control words which determine the nature of the transfers to be done.

The word count, memory address, select code of the I/O device, and control information are stored there during the initialization

routine. The word count and memory address are incremented during DMA cycles. This logic notifies the interrupt and cycle stealing logic when a block transfer is completed.

2.1.3 Cycle Stealing Logic

This logic determines if a device is to be serviced by DMA, and generates the proper signals to control the CPU, memory, and the I/O device during a cycle-steal.

2.2 Interface Signal Descriptions

This section describes the main signals which are important in operation of the 12897 DCPC accessory. Standard I/O signals and busses are not included. All signals are TTL-compatible, ground true unless otherwise specified.

2.2.1 Input Signals

SRQ10-SRQ25 "Service Request". Positive true. CTL compatible. Generated by device requesting service, synchronously with T2. If the particular I/O device has been assigned a DMA channel, then its SRQ alerts logic to initiate a DMA cycle.

$\overline{\text{DMARQ1}}$, $\overline{\text{DMARQ2}}$ "DMA Request". OR-tieable, ground true. Generated by an I/O Extender when an I/O device in the Extender has been assigned a DMA channel, and requests service on it. $\overline{\text{DMARQ1}}$ is a request for channel 1 (select code 6), and $\overline{\text{DMARQ2}}$ is a request for DMA channel 2 (select code 7).

2.2.2 Output Signals

$\overline{\text{DMACYC}}$. "DMA Cycle". Used to notify the system that a DMA cycle is in progress. True from P4 of T5 to P4 of the next T5 in the E-series. True T6 through T5 in the M-series.

$\overline{\text{DMALO}}$. "DMA Lockout". OR-tieable. Used to assure DMA of unhindered access to memory and the I/O system. True from P4 of T4 to P4 of the next T4 in the E-series. True during T5 through T2 in the M-series.

$\overline{\text{DMAEN}}$. "DMA Enable". Sent to the CPU to switch control of the M-bus to DMA during a DMA cycle, and to enable the DMA Memory Address Registers onto the M-bus. True from P4 of T6 to P4 of T4 in the E-series. In the M-series, $\overline{\text{DMAEN}}$ is true from T6 through T3 during output transfers and T6 through T4 during input transfers.

$\overline{\text{DMAREAD}}$. "DMA Read". To memory, to allow memory to time refresh around DMA, if necessary. True during $\overline{\text{DMACYC}}$ of DMA output transfer.

$\overline{\text{READ}}$. "Read". To memory. True during T2 of Read cycle. Downward edge initiates a Read cycle in memory. OR-tieable.

$\overline{\text{DMAIOO}}$. "DMA I/O Output" to CPU. Gates S-bus onto I/O Bus during T3 of output transfer.

$\overline{\text{DMAFRZ}}$. "DMA Freeze". OR-tieable. Freezes CPU clocks and prevents the CPU from using the S-bus while DMA uses it. True during T3 in the M-series. True during T2 and T3 in an E-series.

$\overline{\text{DMAIOI}}$. "DMA I/O Input" to CPU board. Gates the I/O-bus onto the S-bus. True during T3 of a DMA input transfer.

$\overline{\text{DMALCH}}$. "DMA Latch" to CPU board. Holds data on the I/O-bus through completion of DMA output transfer. True from P4 of T3 through P4 of T5.

$\overline{\text{TEN}}$ "T Register Enable" to memory. Gates the T-register in memory onto the S-bus. True during T3 of DMA output transfers. OR-tieable.

$\overline{\text{TST}}$ "T Register Store" to memory. Informs memory to clock data on S-bus into the T-register. True during T3 of DMA input transfers. OR-tieable.

$\overline{\text{WRITE}}$ to memory. Downward edge initiates a write cycle in memory. True during T4 of input transfers. OR-tieable.

EDT "END-DATA-TRANSFER" Positive true. CTL compatible. Informs I/O interface that this is the last transfer. Asserted during T4.

IOO. "I/O Output". Positive true. CTL compatible. To I/O interfaces to clock the I/O Bus data into the interface output register. True during T3 and T4 of all DMA output transfers.

IOI. "I/O Input". Positive true. CTL compatible. To I/O interface to enable input data onto the I/O Bus. True during T2 and T3 of all DMA input transfers.

NOTE: During a programmed Ll*/Ml*, IOI is true during T4 and T5.

STC. "Set Control". Positive true. CTL compatible. To I/O interface to initiate an input or output data transfer. If specified (See Control Word 1) STC is true during T3 of all DMA transfers except the last transfer of an input block.

NOTE: During a programmed STC, STC is true during T4.

CLC. "Clear Control". Positive true. CTL compatible. If specified (see Control Word 1), to I/O interface during T3 and T4 of last transfer of a block to inhibit an unwanted interrupt.

NOTE: During a programmed CLC, CLC is true during T4.

CLF. "Clear Flag". Positive true. CTL compatible. To I/O interface to reset the FLAG and FLAG BUFFER, and thereby acknowledge the SRQ. True during T3 of all DMA transfers except the last transfer of an input block.

NOTE: During a programmed CLF, CLF is true during T4.

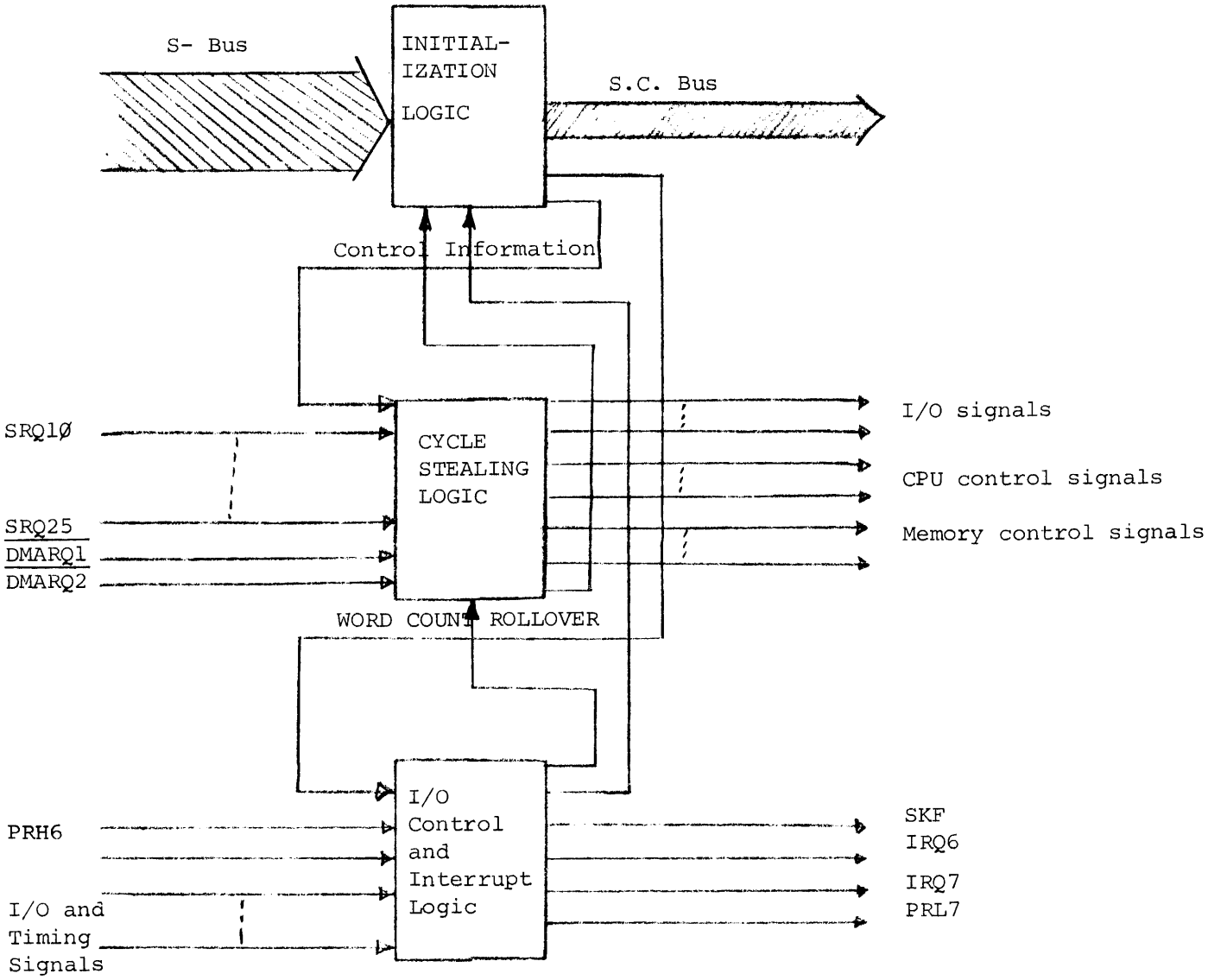


FIGURE 1

DCPC ACCESSORY BLOCK DIAGRAM

3.0 PROGRAMMING

The 12897 DCPC accessory is programmed in exactly the same manner as the DMA option for the 2100A computer. Included below is only a brief summary of the actions performed by the I/O instructions affecting the 12897 DMA operation. Select codes 2 and 6 refer to DMA channel 1, while select codes 3 and 7 refer to channel 2.

3.1 Initialization Instructions

OT*	06	Load the A or B register via the S-bus into the Service
OT*	07	Select Register (bits 0-5, 13, 15). This is Control Word 1.
CLC	02	Set the CTL2FF or CTL3FF high. Used to prepare
CLC	03	DMA to receive Control Word 2.
STC	02	Set the CTL2FF or CTL3FF low. Used to prepare
STC	03	DMA to receive Control Word 3.
OT*	02	Load the A or B register via the S-bus into the DMA
OT*	03	Memory Address Register (Control Word 2) if CLC__FF is low or into the Word Count Register (Control Word 3) if CLC__FF is high. Each channel has its own such registers.

3.2 Control Instructions

STC	06	Turns on DMA to look for SRQ's from I/O devices
STC	07	specified to begin the transfer described by the control words.
STF	06	Set the channel Flag Buffer flip-flop, which disables
STF	07	further DMA cycles on that channel, and will set the flag at the proper time.
CLF	06	Clears the Flag flip-flop, Flag Buffer flip-flop, and
CLF	07	IRQ flip-flop for that channel.

3.3 Status Instructions

SFS	06	SKIP next instruction if flag flip-flop is set (or clear)
SFS	07	on that channel. If set, the block transfer has been
SFC	06	completed.
SFC	07	

LI* 02 READS the remaining word count (2's complement of it)
LI* 03 for the channel. May be used to determine how much of a DMA block transfer has been completed.

4.0 DETAILED THEORY OF OPERATION

The following discussion describes each functional section in operational detail, followed by a discussion of overall DMA operation during initiation, input and output transfers, and interrupt request generation. Logic for channel 1 is identical to that for channel 2, so only channel 1 will be discussed. It is not difficult to discover the channel 2 counterparts to channel 1.

4.1 Initialization Logic

Information from Control Words 1, 2 and 3 are loaded into registers in this logic, and used for transfer control when DMA is activated. The registers are loaded from the S-bus during the I/O instructions listed in section 3.1. The S-bus is buffered (U17, U107) before being distributed to the six registers (3 per channel). Refer to figures 2 and 3.

4.1.1 Control Word 1: register and logic

During I00 of a OT* 06, Control Word 1 is loaded into the Service Select Register (U113, U115), Bits 0-5 contain the select code of the device under control of channel 1, and are designated SSR1-0 through SSR1-5. Bit 13 of the S-bus is stored as CLCSEL1, and is used to specify whether CLC is to be issued to the I/O device at the end of a block transfer. Bit 15 of the S-bus is stored as STCSEL1, and is used to specify if a STC is to be issued to the I/O device at the end of each word transfer (except the last, if it is an input transfer).

When DCYC1 is high (cycle in progress on channel 1) the Service Select Register is buffered (U116, U117) onto the Select Code Bus to select the specified device for DMA control. This buffer also outputs the signals $\overline{\text{INCWC1}}$ at T62, and $\overline{\text{INCMR1}}$ during DMAEN. These signals increment the Word Count Register and Memory Address Register, respectively.

4.1.2 Control Word 2: register and logic

CTL2FF (U64, pin 13) must be low in order to load the second control word into the Memory Address Register (MAR). This is assured by executing a CLC 02 instruction which clears the R-S flip-flop CTL2FF.

A succeeding OT* 02 instruction will load the A or B register into the Memory Address Register (U16, 26, 96, 106) with the negative edge of $\overline{\text{LOADMAR1}}$. The MAR is a 15 bit register containing a 15-bit ripple counter (loaded from bits 0-14 of the S-bus) and a single D flip-flop (loaded from bit 15 of the S-bus) called INFF1 (U16-pin 5). If INFF1 is high, then a DMA input transfer is to be done on channel 1. If low, then an output transfer. This flip-flop does not change once the MAR is loaded. The MAR counter is incremented by the downward edge of $\overline{\text{INCMR1}}$ at the trailing edge of DMAEN.

The MAR is enabled onto the M-bus through a set of buffers (U47, 57) during DMAEN in DCYC1. DMAEN also disables the CPU M-register from using the M-bus.

Note that M-bus bit 15 is forced low during DMAEN in DCYC1, and that it is forced high during DMAEN in DCYC2. Bit 15 is monitored by the Memory Management option board to distinguish between channel 1 and channel 2 during transfers.

4.1.3 Control Word 3: register and logic

$\overline{\text{CTL2FF}}$ (U64 pin 9) must be low to be able to load the third control word into Word Count Register 1. This is effected by issuing an STC 02 instruction, which sets the R-S flip-flop.

A succeeding OT* 02 instruction will enable the A or B register into the Word Count Register (U14, 24, 94, 104) via the S-bus on the downward edge of $\overline{\text{LOADWC1}}$, and latch the data on the rising edge. The Word Count Register is a 16-bit synchronous counter loaded with the two's complement of the number of words to be transferred under DMA channel 1 control. It performs a carry-look-ahead for each group of four bits while $\overline{\text{INCWC1}}$ is low. If all outputs of the low order bits are high when $\overline{\text{INCWC1}}$ goes low, then the carry output, pin 12, goes low, which goes to pin 5 of the next group, performing the same function. If all bits of the Word Count Register are high, then $\overline{\text{INCWC1}}$ going low will result in WCR1 (Word Count rollover) going high, indicating that the current transfer is the last. The register increments at the rising edge of $\overline{\text{INCWC1}}$. $\overline{\text{INCWC1}}$ is low during T62 of a channel 1 cycle (DCYC1).

The Word Count Register is enabled onto the S-bus through the buffer (U27, 37) during LI* 02 instructions, and stored onto the A or B register on the CPU.

4.2 I/O Control and Interrupt Logic

4.2.1 Timing Decoders

To generate I/O signals at the proper times, DMA needs to have a way to generate T2-T6 in sync with the CPU. To do this, DMA receives the TA, TB, TC signals from the CPU, and decodes them (U66, U53, U73, U82) to provide the required time periods. Several timing signals must be different for the M-series than for the E-series; U32, controlled by W1, selects the timing required for each CPU type.

4.2.2 I/O Instruction Decoding

DMA decodes the Select Code Bus with IOG, they generate $\overline{SC2}$, $\overline{SC3}$, $\overline{SC6}$, $\overline{SC7}$, respectively, which are low during I/O instructions for the specified DMA select codes. These signals are used as described below:

$\overline{SC2}$ / $\overline{SC3}$
- (a) in conjunction with STC or CLC, set or clear the STC2FF or STC3FF.
- (b) in conjunction with IOG, generate $\overline{LOADWC}$ or $\overline{LOADMAR}$
- (c) in conjunction with IOI, gate the Word Count Register onto the S-bus.

$\overline{SC6}$ / $\overline{SC7}$
- (a) enable buffer U45 or U55, respectively, which then enables STC, CLC, CLF, and STF to the appropriate DMA channel flip-flop. The buffers OR-tie the status of the two channel flags for the skip logic (pins 1, 2). Only one channel flag status is selected for test during SFS or SFC, since only one buffer may be enabled at a time.
- (b) in conjunction with IOO, load the Service Select Register.

4.2.3 Interrupt logic

When DMA is turned on, an STC 06, C instruction sets the Channel Control, CONT6FF (U64), and clears the Flag, Flag Buffer, and IRQ flip-flops (U44).

The interrupt generating sequence may be initiated in two ways. It is assumed that CONT6FF is high, the interrupt system is enabled (IEN5 is high), and the priority chain is intact to DMA (PRH6 is high). Refer to figure 4. If any one of these conditions is not met, no interrupt will be requested.

a. WCR1 (Word Count Rollover) is high. This indicates that the last word transfer is in progress. This sets FBFF1 and clears the transfer enable flip-flop (TRENFF1).

b. Issuing an STF 06 instruction. This sets FBFF1 and clears the transfer enable flip-flop (TRENFF1).

T2 following setting of the Flag Buffer, the Flag (FLG6FF) is set high.

The T5 following setting of FLG6FF, IRQ6FF is set. IRQ6FF is high during T5-T6 and low T2-T4 until the interrupt is granted. However, if a higher priority device (Powerfail, Parity, or Memory Protect) sets its flag, then PRH6 will go low, preventing DMA from interrupting until the other device has been serviced and PRH6 is high again.

When the DMA interrupt request is acknowledged, IAK occurs at P3, 4, 5 of T6. IAK in conjunction with IRQ6FF clears FBFF1.

4.3 Cycle Stealing Logic

The cycle stealing logic compares the Service Select Register to the SRQ lines coming from I/O interface cards to determine if a cycle is to be requested. It resolves access priorities between the two DMA channels, initiates the cycle, and controls the generation of various signals to memory, the CPU, and the I/O interface to effect the desired transfer. Refer to figure 5.

4.3.1 Cycle Request Logic

This consists primarily of a 16-to-1 multiplexor (U51). SSR1-0 to SSR1-5 select a SRQ line to monitor. When that SRQ line goes high, indicating the Flag has been set on the interface card with the select code specified in the SSR, then the REQ1 line (U111-6) goes high. $\overline{\text{DMARQ1}}$ indicates a request for DMA channel 1 from the I/O Extender. It also sets REQ1 high.

4.3.2 Cycle Initiating Logic

The Cycle Request Register (U46) is the focal point for initiating DMA cycles on either channel. Refer to figure 5. It is clocked every trailing edge of P5 in M-series and Leading edge of P4 in E-series.

When an STC 06 instruction is executed, the Transfer Enable flip-flop (TRENFF1) is set. This allows the cycle initiating logic to monitor the REQ1 line (U41B). If there is no power failure (PRH5 is high), then when REQ1 goes high, the Cycle Request 1 flip-flop, CYCRQ1, will be set at the end of T4. As long as CYCRQ1 is high, DMA channel 2 cannot take a cycle (gate U53B). Once CYCRQ1 goes high, it is kept high until the end of the next T4. The NOR of CYCRQ1 and CYCRQ2 during T5 through T2 is $\overline{\text{DMALO}}$.

$\overline{\text{DMALO}}$ goes to the CPU to perform the following functions:

a. Prevent setting the I/O Group Enable flip-flop.

b. Freeze the CPU if it attempts to access memory, perform I/O instructions, or load the central Interrupt Register.

c. Set the Interrupt Override ff on the CPU to prevent interrupt recognition during the cycle.

The DCYC1 flip-flop follows CYCRQ1, delayed by one T-period. It enables the signal generation logic for a DMA transfer. The DCYC2 flip-flop may not be set until the T5 after CYCRQ1 goes low, if CYCRQ2 is high. Channel 2 may thus take a cycle immediately after channel 1. The NOR of DCYC1 and DCYC2 is $\overline{\text{DMACYC}}$, which is sent to the CPU to prevent granting of interrupt requests until DMA has prevented its controlled device from requesting CPU service.

4.3.3 Signal Generation Logic (Figure 5)

DCYC1 controls a multiplexer (U85) which selects transfer control information from one or the other DMA channel's initialization logic (INFF__, STCSEL__, and CLCSEL__) and Flag Buffer status. These signals determine the exact combination of output signals necessary to execute a DMA transfer. Four flip-flops are used to assist in this generation (U62, 72). See sections 4.4, 4.5 for timed signals for input and output transfers. The signal "IN" (U85) selects the proper set of signals for input or output transfers.

4.4 Input Transfers

Tables 1 and 2 describe the algorithm for executing an input transfer on DMA channel 1. Refer to figure 6 and 7 for a diagram of timing signals for (a) normal cycle and (b) end-of-block-transfer cycle. It is assumed that TRENFF1 is high initially and that SRQ is asserted in time to generate REQ1.

Table 1. M-Series Input Transfers

Time	Signals Initiated	Action
T5	$\overline{\text{DMALO}}$	Prevent CPU from interfering with upcoming cycle. Prevent interrupt service in the CPU.
T6	$\overline{\text{DMACYC}}$	Start cycle, enable signals, give DMA control of Select Code Bus, servicing in CPU.
	$\overline{\text{DMAEN}}$	Low at P4, enabling MAR1 onto M-bus, removing CPU from M-bus.
	$\overline{\text{INCWC1}}$	Check for word count rollover, increment word count on trailing edge. If WCR1 occurs, set FBFF1 high.
T2	IOI	Tell I/O card to enable data buffer onto I/O bus.
T3	$\overline{\text{DMAFRZ}}$	Freeze CPU, free the S-bus.
	$\overline{\text{DMAIOI}}$	Gate I/O bus onto the S-bus.
	TST	Clock S-bus into T-register.
	STC	Issue STC to interface card if STCSEL1 is high and FBFF1 is low.
	CLC	Issue CLC to interface card if CLCSEL1 is high and FBFF1 is high.
	CLF	Issue CLF to interface card if FBFF1 is low.

Table 1. M-Series Input Transfers (Continued)

Time	Signals Initiated	Action
T4	$\overline{\text{WRITE}}$	Initiate write cycle in memory at address on M-bus.
	EDT	Issue to interface card if FBFF1 is high.

Table 2. E-Series Input Transfers

Time	Signals Initiated	Action
P4 of T4	$\overline{\text{DMALO}}$	Prevent CPU from interfering with upcoming cycle. Prevent interrupt service in the CPU.
P4 of T5	$\overline{\text{DMACYC}}$	Start cycle, enable signals, give DMA control of Select Code Bus, servicing in CPU.
T6	IOG	Enable DMA select code onto select code bus.
	$\overline{\text{INCWC}}$	Check for word count roll-over, increment word count on trailing edge. If WCR1 occurs, set FBFF1.
P4 of T6	$\overline{\text{DMAEN}}$	Enables MAR1 onto M-bus, removes CPU from the M-bus. Increment MAR1 on trailing edge.
T2	IOI	Tell I/O card to enable data onto I/O bus.
	$\overline{\text{DMAFRZ}}$	Freeze CPU, free the S-bus for use by DMA.
T3	$\overline{\text{DMAIOI}}$	Gate I/O-bus onto the S-bus.
	$\overline{\text{TST}}$	Clock S-bus into T register.
	STC	Issue STC to interface card if STCSEL1 is high and FBFF1 is low.
	CLC	Issue CLC to interface card if CLCSEL1 is high and FBFF1 is high.

Table 2. E-Series Input Transfers (Continued)

Time	Signals Initiated	Action
T3 (cont.)	CLF	Issue CLF to interface card if FBFF1 is low.
T4	$\overline{\text{WRITE}}$	Initiate write cycle into memory at address on M-bus.
	EDT	Issue EDT to interface card if FBFF1 is high.

4.5 Output Transfers

Tables 3 and 4 describe the algorithm for executing an output transfer on DMA channel 1. Refer to figure 7 and 8 for a diagram of the Timing signals. It is assumed that TRENFF1 is high initially, and that SRQ is asserted in time to generate REQ1 by P5 of T4. Both the case of (a) normal cycles and (b) end-of-transfer cycles are illustrated.

Table 3. M-Series Output Transfers

Time Period	Signal Initiated	Action
T5	$\overline{\text{DMALO}}$	Prevent CPU from interfering with upcoming cycle.
T6	$\overline{\text{DMACYC}}$	Start cycle, enable signals, prevent CPU interrupt servicing.
	$\overline{\text{DMAREAD}}$	Tell memory to schedule refresh during T4-T5.
	$\overline{\text{DMAEN}}$	Enable DMA Memory Address Register 1 onto M-bus. Increment MAR1 on trailing edge.
	$\overline{\text{INCWC1}}$	Check for Word Count Rollover. If WCR1 high, then set FBFF1 Increment Word Count at trailing edge.
T2	$\overline{\text{READ}}$	Initiate Read cycle.
T3	$\overline{\text{DMAFRZ}}$	Freeze CPU while DMA uses S-bus.
	$\overline{\text{TEN}}$	Enable data in T-register onto S-bus.
	$\overline{\text{DMAIOO}}$	Enable S-bus onto I/O-bus.

Table 3. M-Series Output Transfers (Continued)

Time Period	Signal Initiated	Action
P4 of T3	$\overline{\text{DMALCH}}$	Hold data on I/O-bus. This signal allows S-bus to be used by CPU during following time periods.
T3	IOO	Clock I/O-bus into input buffer on I/O interface card.
	CLF	Issue CLF to interface card.
	STC	Issue STC to interface card if STCSEL1 is high.
	CLC	Issue CLC to interface card if FBFF1 is high and CLCSEL1 is high.
T4	EDT	Issue to interface card if FBFF1 is high.

4.6 System Reset Signals

4.6.1 POPIO

POPIO occurs during power-up or by pressing the Preset button on the front panel in the HALT mode. POPIO sets the Flag buffers on both channels (FBFF1, FBFF2). This terminates any block transfers in progress.

4.6.2 CRS

CRS occurs during POPIO or during CLC 0 instructions. CRS clears CTL2FF, CTL3FF, CTL6FF, CTL7FF, TRENFF1, and TRENFF2, which disables DMA from interrupting and terminates any block transfers in progress.

Table 4. E-Series Output Transfers

Time	Signals Initiated	Action
P4 of T4	$\overline{\text{DMALO}}$	Prevent CPU from interfering with upcoming cycle.
P4 of T5	$\overline{\text{DMACYC}}$	Start cycle, enable signals, prevent CPU interrupt servicing.
	$\overline{\text{DMAREAD}}$	Tell memory to schedule refresh during T4-T5.
T6	IOG	Enable DMA select code onto select code bus.
	$\overline{\text{INCWC}}$	Check for word count roll-over, increment word count on trailing edge. If WCR1 occurs set FBFF1.
P4 of T6	$\overline{\text{DMAEN}}$	Enables MAR1 onto M-bus, remove CPU from M-bus. Increment MAR1 on trailing edge.
T2	$\overline{\text{READ}}$	Initiate Read cycle.
	$\overline{\text{DMAFRZ}}$	Freeze CPU while DMA uses S-bus.
T3	$\overline{\text{TEN}}$	Enable data in T-register onto S-bus.
	$\overline{\text{DMAIOO}}$	Enable S-bus onto I/O-bus.
	IOO	Clock I/O-bus into input buffer on I/O interface card.
	CLF	Issue CLF to interface card.

Table 4. E-Series Output Transfers (Continued)

Time	Signals Initiated	Action
T3 (cont.)	STC	Issue STC to interface card if STCSEL1 is high.
	CLC	Issue CLC to interface card if FBFF1 is high and CLCSEL1 is high
P4 of T3	$\overline{\text{DMALCH}}$	Hold data on I/O-bus. This signal allows S-bus to be used by CPU during following time periods.
T4	EDT	Issue to interface card if FBFF1 is high.

CONTROL WORD 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	STC		CLC								Device Select Code					
0	STC		CLC													

STC: issue STC at the end of every cycle, except the last, if input.

CLC: issue CLC at the end of last word transfer.

CONTROL WORD 2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	IN	Memory Address														
0	OUT															

CONTROL WORD 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2's COMPLEMENT OF WORD COUNT															

FIGURE 2

DCPC CONTROL WORD FORMATS

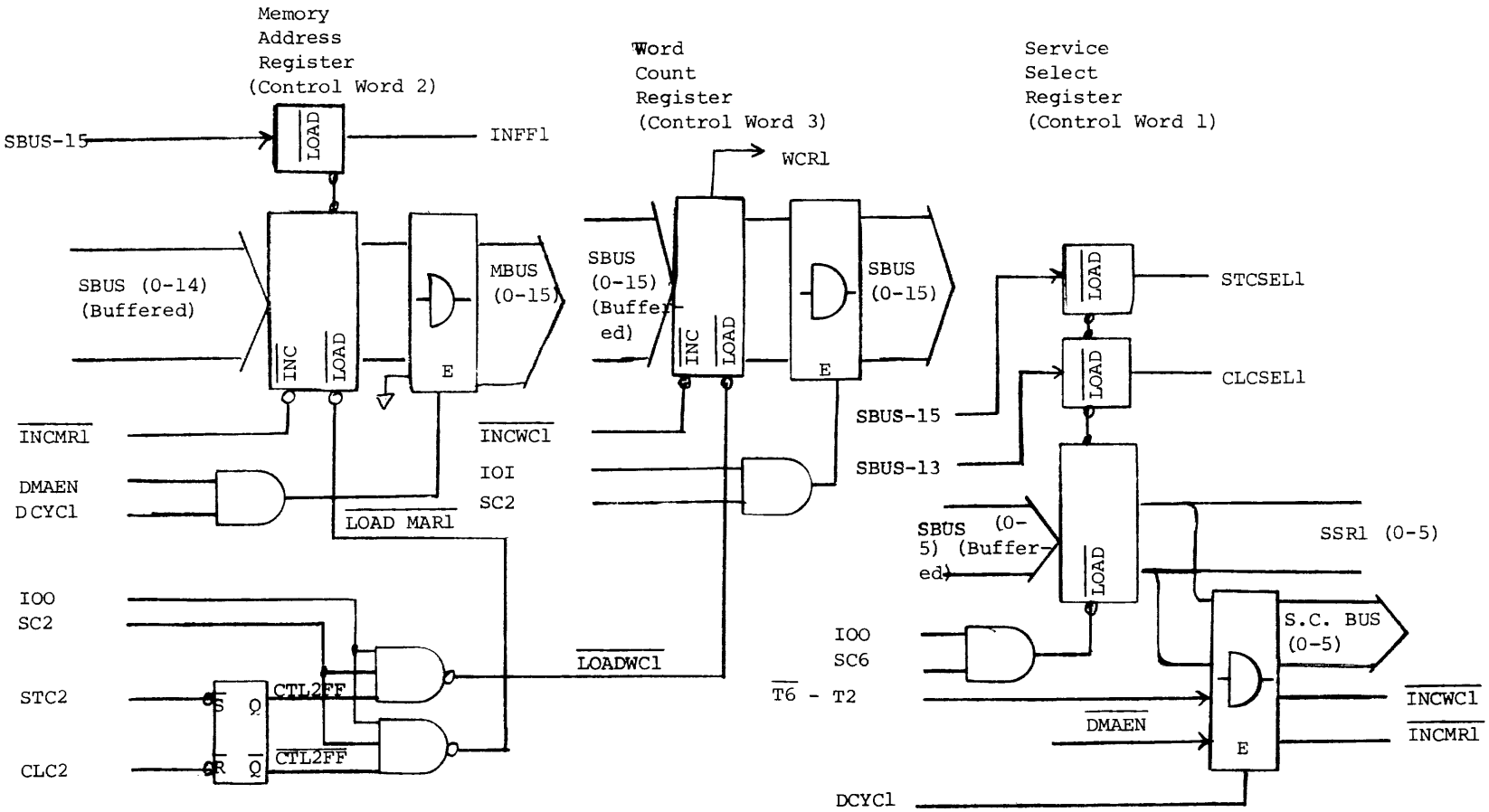


FIGURE 3

INITIALIZATION LOGIC

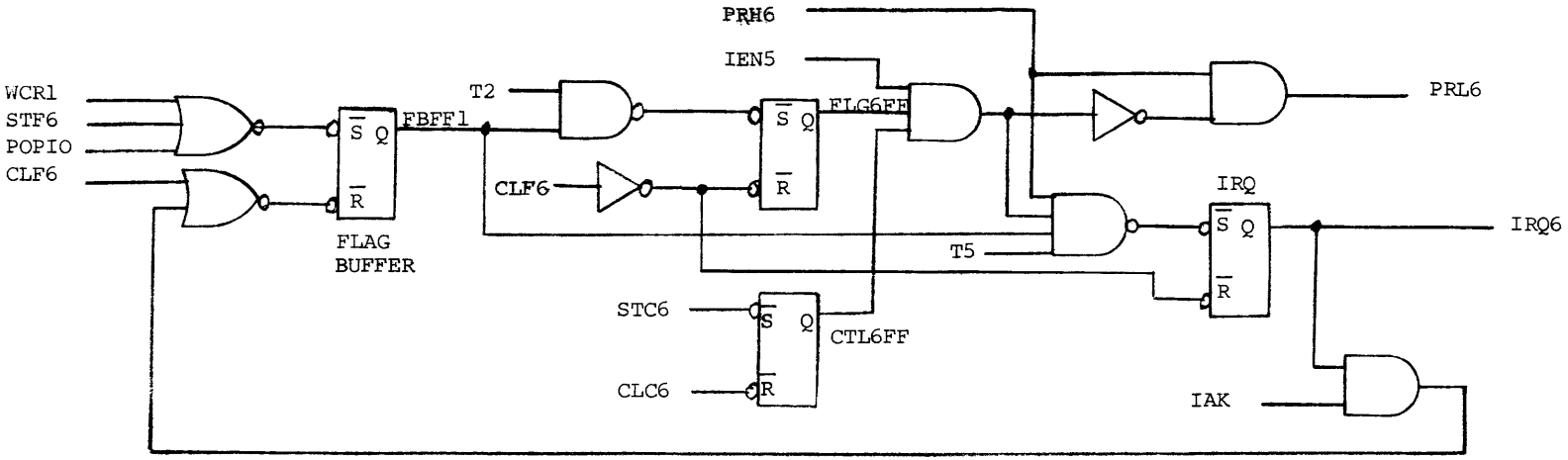


FIGURE 4

INTERRUPT AND PRIORITY LOGIC

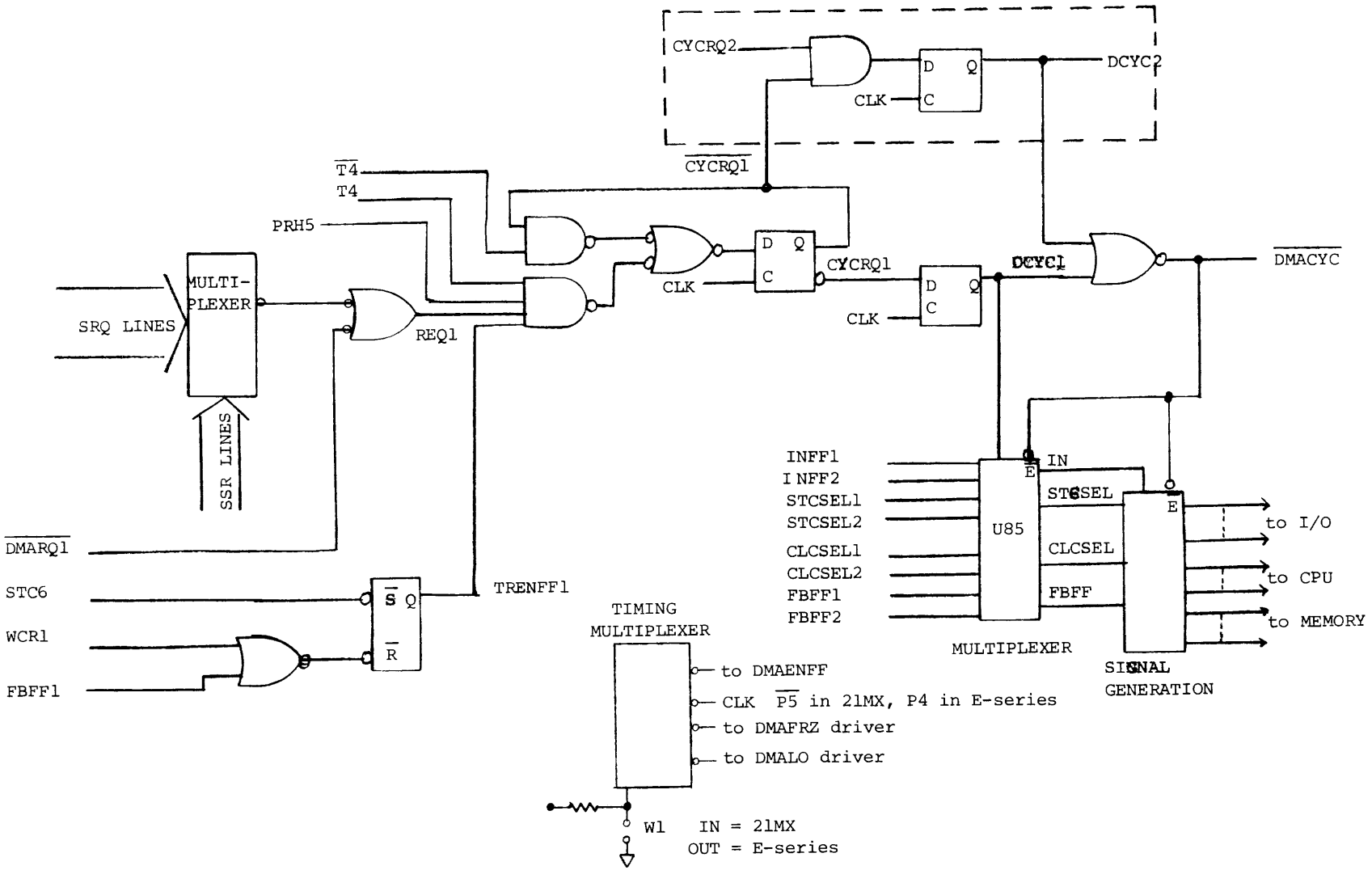


FIGURE 5
CYCLE STEALING LOGIC, CHANNEL 1

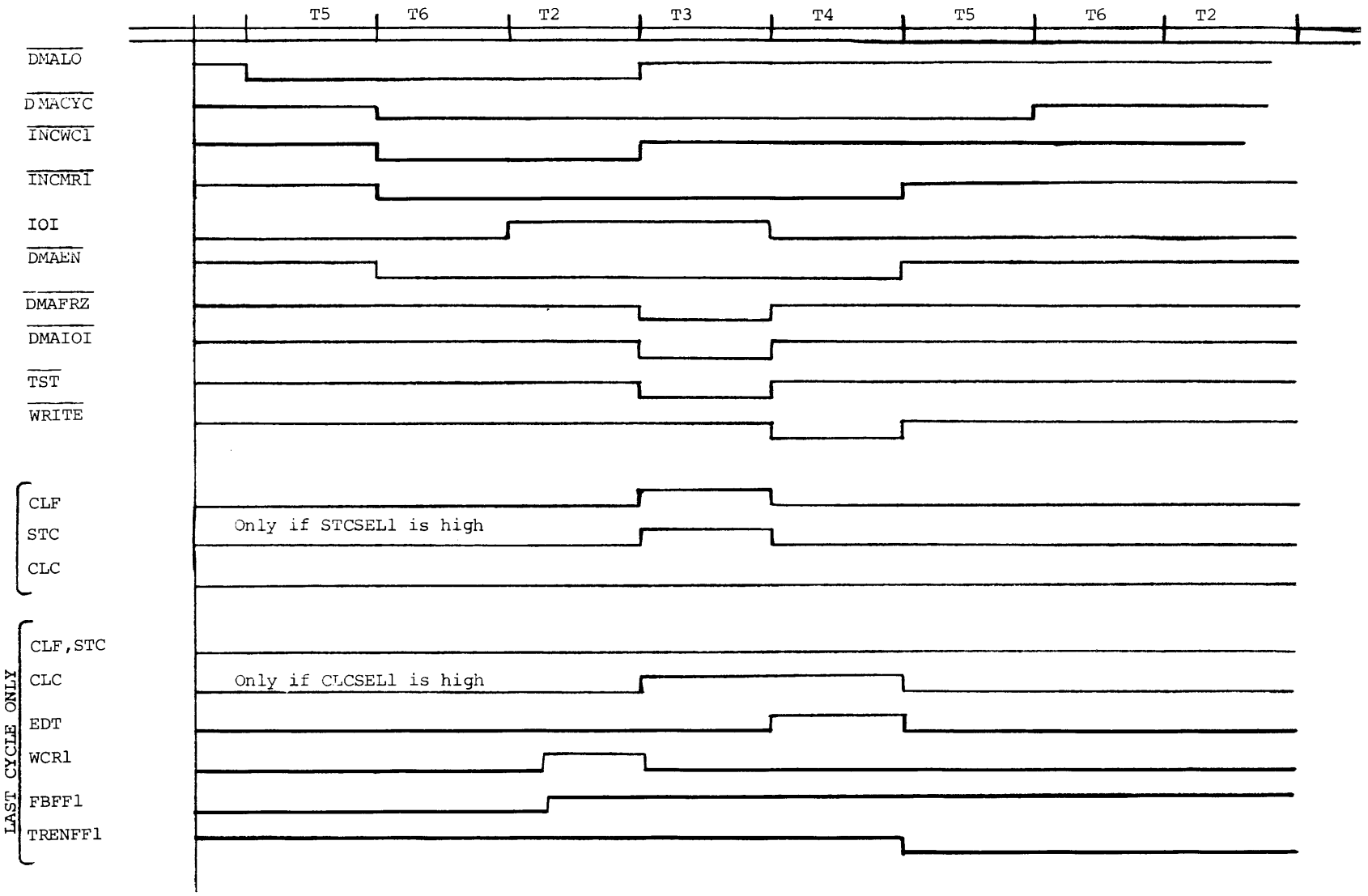


FIGURE 6

M-SERIES DMA INPUT TRANSFER TIMING

CHANNEL 1 ILLUSTRATED (MX JUMPER INSTALLED)

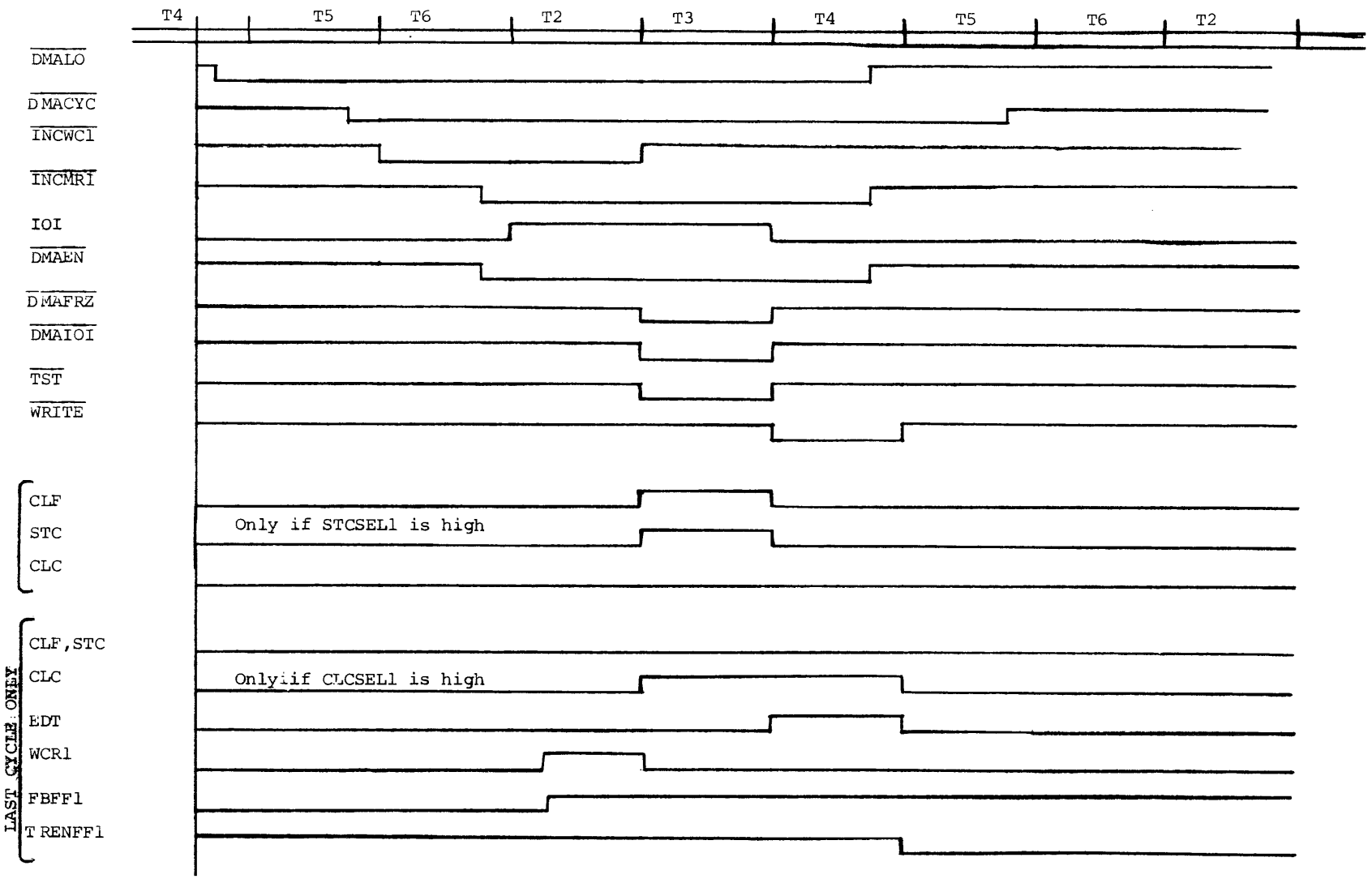


FIGURE 7

E-SERIES DMA INPUT TRANSFER TIMING

CHANNEL 1 ILLUSTRATED (MX JUMPER REMOVED)

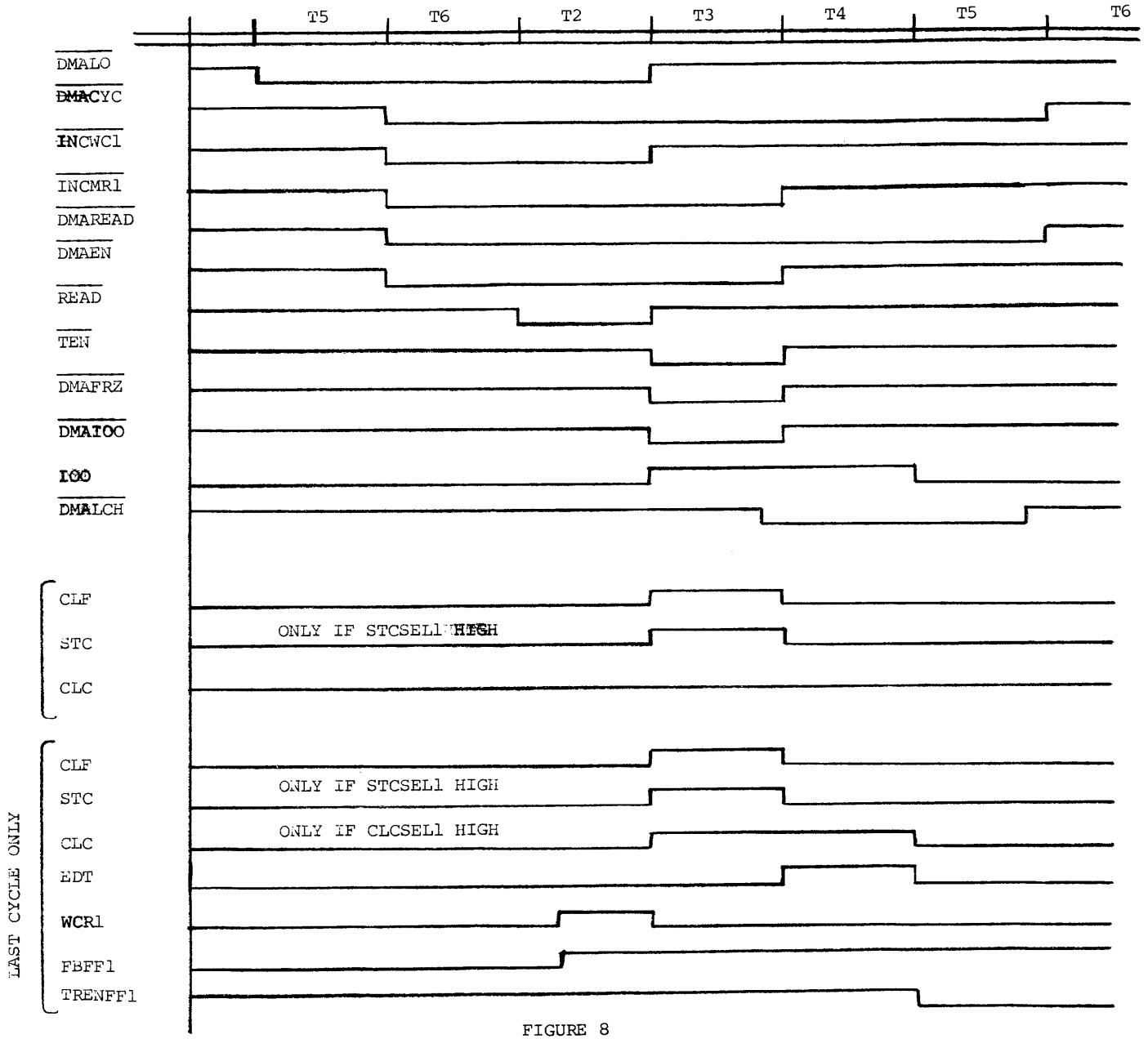


FIGURE 8

M-SERIES DMA OUTPUT TRANSFER TIMING, CHANNEL 1 (MX JUMPER INSTALLED)

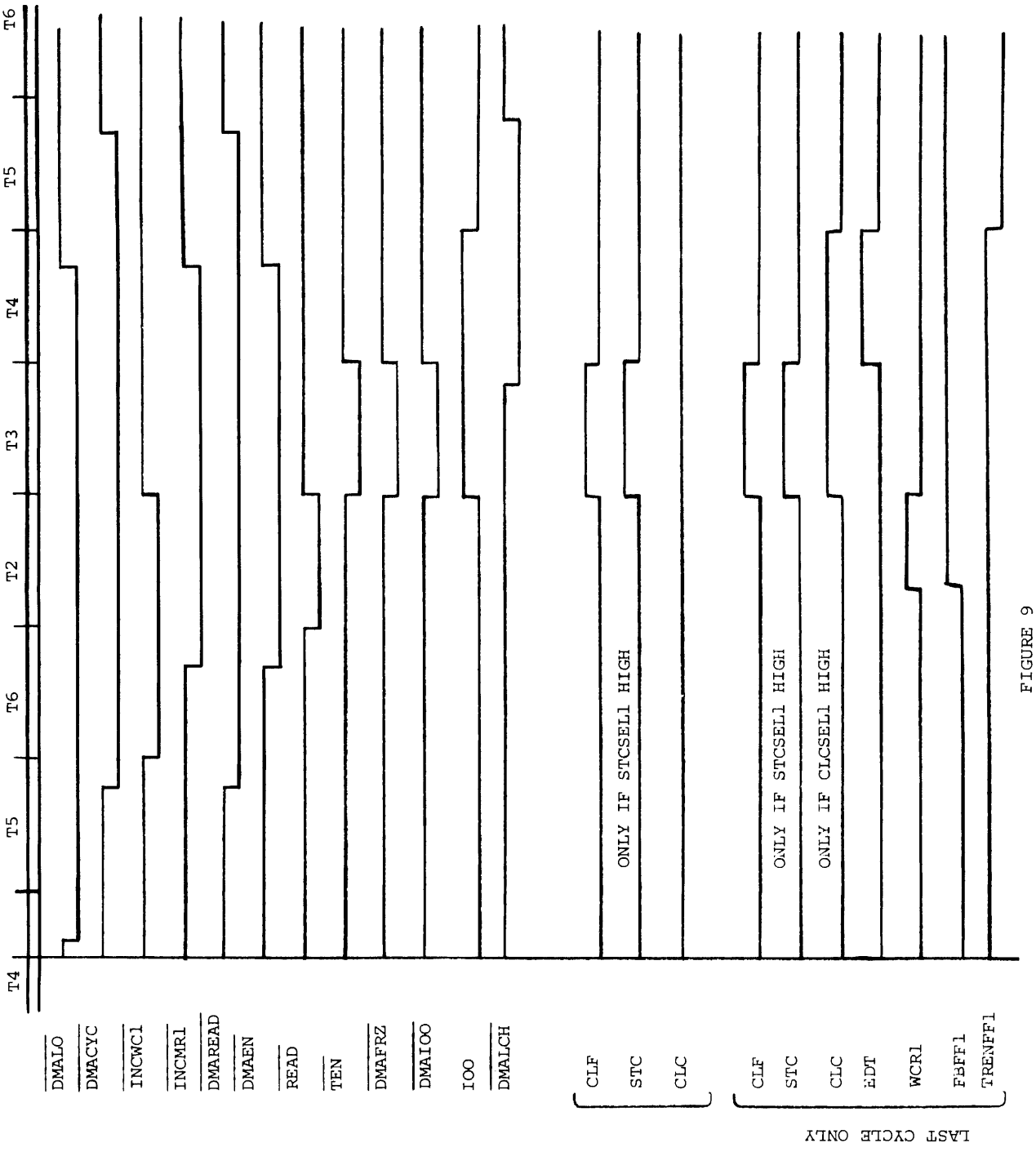
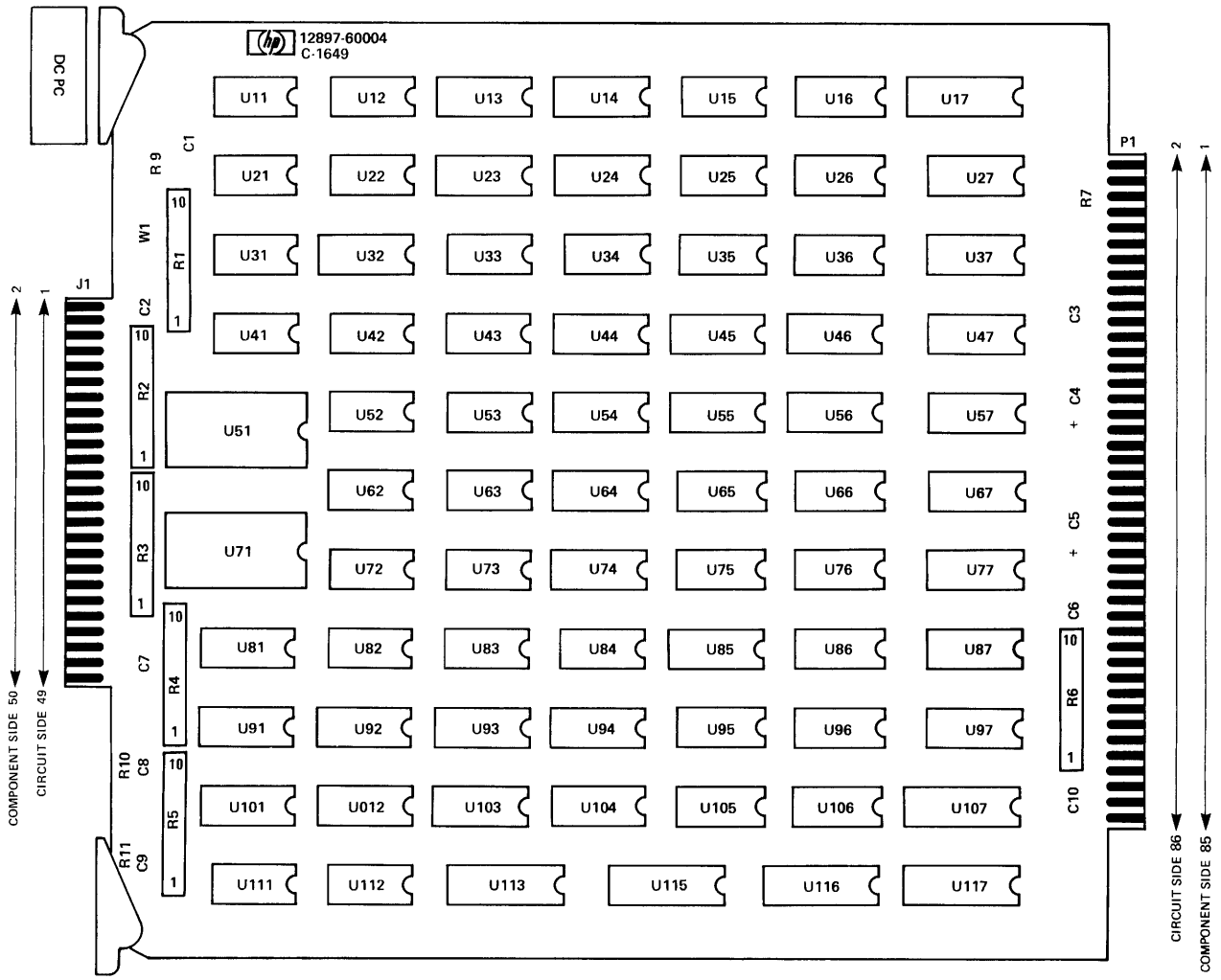


FIGURE 9

E-SERIES DMA OUTPUT TRANSFER TIMING, CHANNEL 1 (MX JUMPER REMOVED)



Dual Channel Port Controller Assembly
12897-60004

12897B DCPC Assembly Parts List (12897-60004) Sht. 1 of 3

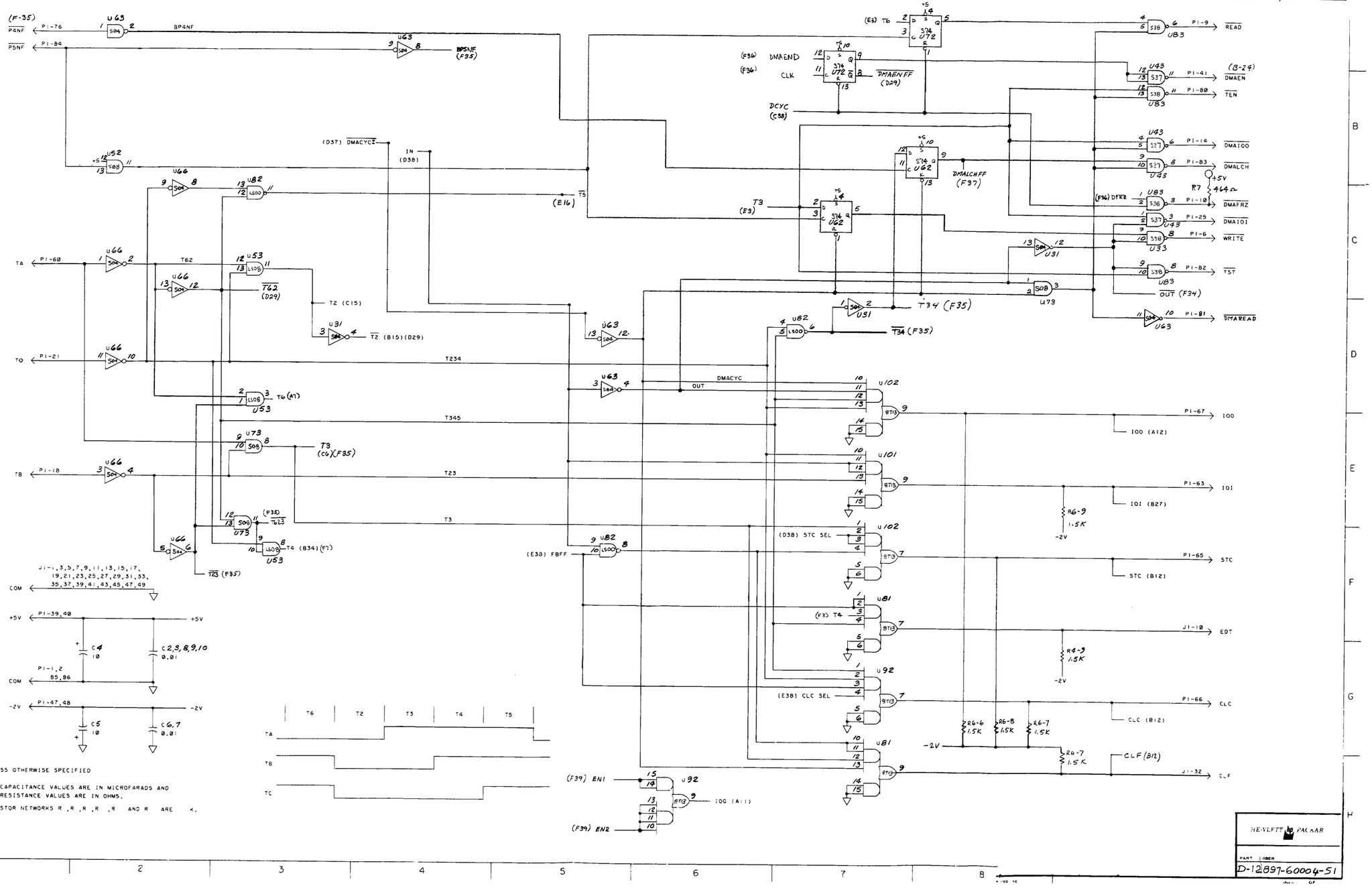
ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01	C1-3,6-10	CAP .01UF		0160-2055		U	8
00	C4,5	CAP 10UF 10%		0180-0374		D	2
00	E1,2	STUD SOLDER TERM		0360-0474		U	2
00	R9	RES 1.0K 5% .25		0683-1025		D	1
01	R10,11	RES 330 5% .25		0683-3315		U	2
00	R7	RES 464 1%.125		0698-0082		D	1
		SOCKET PC SINGLE		1251-1556		U	3
		JMPR PLUG .3"C-C		1258-0124		U	1
		PIN GRV .062X.25		1480-0116		U	2
00	R2,3	NTWK RES 9X500		1810-0274		U	2
00	R1,5	NTWK RES 9X1K		1810-0275		U	2
00	R4,6	NTWK RES 9X1.5K		1810-0276		U	2
01	U51,71	IC SN74150N		1820-0640		U	2
00	U111	IC SN74S00N		1820-0681		U	1
01	U31,63,66	IC SN74S04N		1820-0683		U	3
00	U36	IC SN74S10N		1820-0685		U	1
00	U41	IC SN74S22N		1820-0689		U	1
		IC SN74S74N		1820-0693		U	2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01	U62,72			1820-0693			
01 03	U15,16,25,26,95,96, 105,106	IC SN74197N		1820-0765		U	8
00	U32	IC SN74S158N		1820-1015		U	1
01	U81,91,92,101,102	IC 8T13B		1820-1080		U	5
00	U11	IC SN74LS02N		1820-1144		U	1
00	U42	IC SN74S51N		1820-1158		U	1
00	U46	IC SN74S175N		1820-1191		U	1
01 03	U13,14,23,24,93,94, 103,104	IC SN74LS193N		1820-1194		U	8
01	U34,75,82	IC SN74LS00N		1820-1197		U	3
00	U35	IC SN74LS04N		1820-1199		U	1
00	U76	IC SN74LS05N		1820-1200		U	1
00	U53	IC SN74LS08N		1820-1201		U	1
00	U22	IC SN74LS27N		1820-1206		U	1
01	U12,21,65,84	IC SN74LS32N		1820-1208		U	4
00	U112	IC SN74LS86N		1820-1211		U	1
00	U56	IC SN74LS138N		1820-1216		U	1
01	U45,55	IC DM8095N		1820-1254		U	2
		IC SN74S257N		1820-1301		U	8

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
				1820-1301			
01 03	U27,37,47,57,67,77, 87,97						
		IC SN74S08N		1820-1367		U	2
01	U52,73						
		IC SN74LS14N		1820-1416		U	1
00	U86						
		IC SN74LS279N		1820-1440		U	4
01	U44,54,64,74						
		IC SN74S37N		1820-1450		U	1
00	U43						
		IC SN74S38N		1820-1451		U	2
01	U33,83						
		IC SN74273N		1820-1461		U	2
01	U113,115						
		IC SN74LS157N		1820-1470		U	1
00	U85						
		ICSN74S241N		1820-1624		U	4
01	U17,107,116,117						
		LABEL-USA		7120-6830		L	1
		EXTRACTOR-PC		5040-6001		W	1
		EXTRACTOR-BLACK		5040-6068		W	1
		DTS-70 TEST ADP		ET13460		1	0
01	TEST	FIXTURE					

SYM	REVISION
A	AS ISSUED
B	PER PRCR U, BC, AK
C	PER PCO-72-7696 [C-7669]
D	ADD. TITLE BLOCK AND REV. DETAIL

TIMING LOGIC



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITANCE VALUES ARE IN MICROFARADS AND ALL RESISTANCE VALUES ARE IN OHMS.
2. RESISTOR NETWORKS R ,R ,R ,R AND R ARE K.

HEWLETT PACKARD

PART NUMBER D-12897-60004-51

D-12897-60004-52			
A	AS ISSUED		11-2-76
B	ADD. TITLE & REV. DECAL	C-4	2-27-77

SFC J1-36
SFS P1-62
IOG P1-68
IAK P1-77
STF P1-78
(H6) IOG
R4-1 1.5K
R6-10 1.5K
R6-4 1.5K
R4-4 1.5K
R6-5 1.5K
-2V
U86 LS14
(H-2) CLF
(F-9) STC
(G-9) CLC
(E-9) IOO
U35 LS04
U86 LS14
U86 LS14
U86 LS14
$\overline{STC}$ (G14)(G17)
$\overline{CLC}$ (F14)(F17)
$\overline{IOO}$ (F-27) (F15) (F19)
-2V
1.5K R6-2
PRH6 P1-13
IEN5 P1-79
POP10 P1-73
(F-30) SCB5
SCB4
SCB3 (F-30)
SCB2
SCB1
SCB0 (F-30)
U65 LS32
U56 74LS138
$\overline{SC7}$ (F27)
$\overline{SC6}$ (D27)
$\overline{SC3}$ (G17)(E28)
$\overline{SC2}$ (G14)
SELECT CODE DECODE LOGIC
CRS P1-74
1.5K R6-3
-2V
U86 LS14
U31 LS04
(D4) $\overline{T2}$
T2 (D3)
U36 LS10
U35 LS04
U35 LS04
U45 8095
(STF6)
(CLF6)
FLG6FF
U44 4-BIT REGISTER LS279
FB 1Q
FLG 2Q
IRQ 3Q
FB 4Q
U75 LS00
U38 LS00
+5V
1K R1-5
1K R5-7
U91 BT13
U95 LS04
U55 8095
(STF7)
(CLF7)
FLG7FF
U54 4-BIT REGISTER LS279
U86 LS10
U34 LS00
U75 LS00
+5V
1K R1-6
U91 BT13
U101 BT13
1.5K R4-5
1.5K R4-3
-2
P1-75 SKF
J1-34 IRQ6
J1-38 IRQ7
U11 LS02
U65 LS32
U52 S08
FBFF1 (E38)
FBFF2 (E38)
(C-5) $\overline{T5}$
$\overline{CTL6FF}$
$\overline{CTL7FF}$
U76 LS05
U22 LS27
WCR1 (A26)
(E26) WCR2
1K R1-7
1K R5-9
1K R5-10
+5V
(D13) $\overline{IOO}$
(F13) $\overline{SC2}$
U84 LS32
U64 4-BIT REGISTER LS279
$\overline{CTL2}$
$\overline{CTL3}$
U74 4-BIT REGISTER LS279
$\overline{CTL9}$
+5
R1-9 1K
R1-10 1K
TRENFF1 (B35)
TRENFF2 (E35)
(CLC6)
(STC6)
(CLC7)
(STC7)
U21 LS32
U12 LS32
LOAD WC1 (A25)
LOAD MAR1 (B22)
LOAD WC2 (E25)
LOAD MAR2 (E22)
CTL2FF
CTL3FF
(C13) $\overline{CLC}$
(F13) $\overline{SC2}$
(C13) $\overline{STC}$
$\overline{CLC}$ (C13)
$\overline{SC3}$ (F13)
$\overline{STC}$ (C13)
1K R1-3
1K R1-2
+5V

CHANGE	REFERENCE
A	ORIG
B	
C	

CHANNEL 1 INTERRUPT AND STATE LOGIC

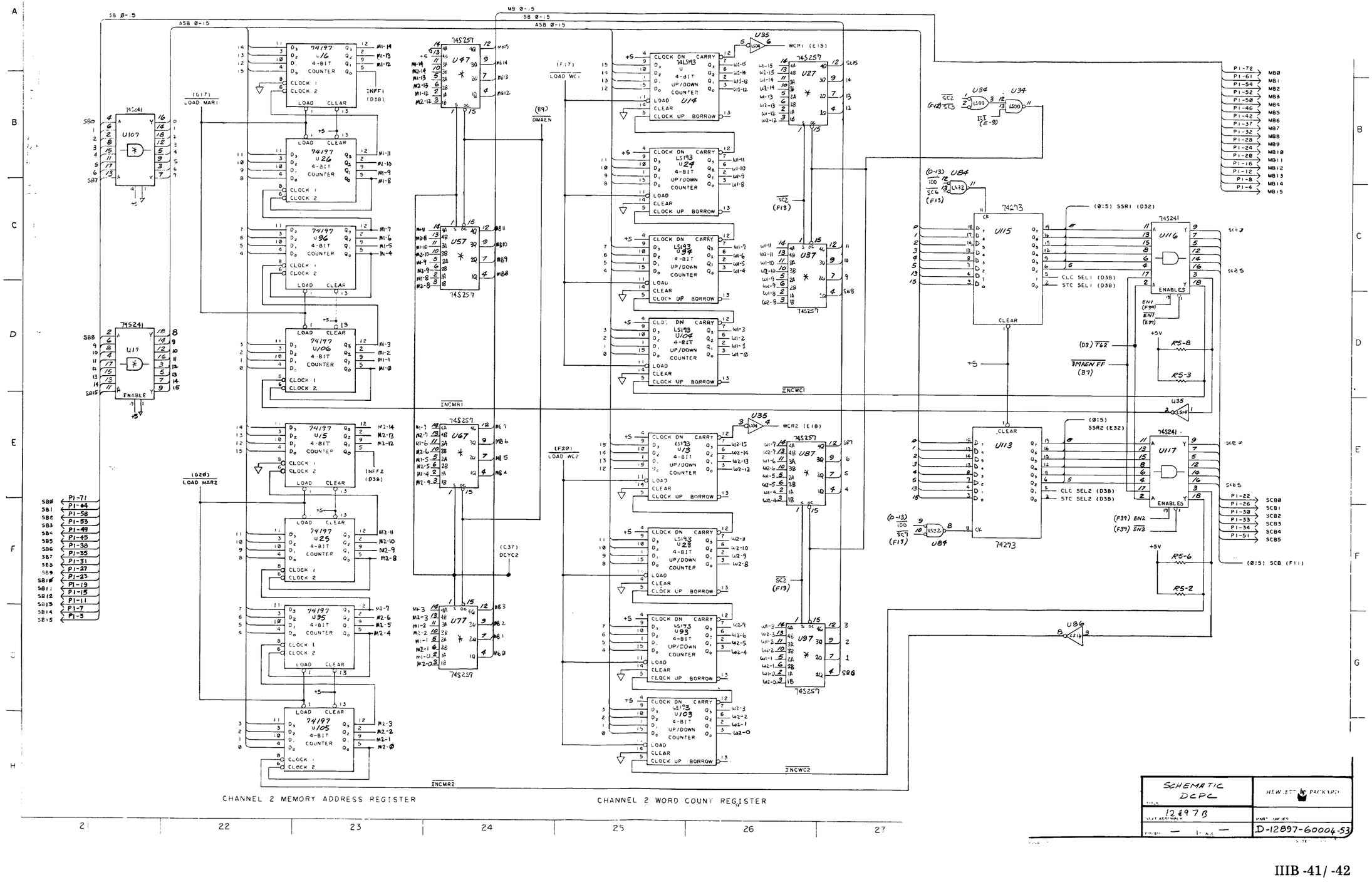
CHANNEL 2 INTERRUPT AND STATE LOGIC

SCHEMATIC DCPC (TITLE)	HEWLETT PACKARD
NEXT ASSEMBLY 12897B	PART NUMBER D-12897-60004-52

CHANNEL 1 MEMORY ADDRESS REGISTER

CHANNEL 1 WORD COUNT REGISTER

D-12897-60004-53
A AS ISSUED
B ADD TITLE & REV. DECNL.



CHANNEL 2 MEMORY ADDRESS REGISTER

CHANNEL 2 WORD COUNT REGISTER

SCHEMATIC DCPC	HEWLETT PACKARD
SIZE 12897B	PART NUMBER D-12897-60004-53

D-12897-60004-54

REVISIONS			
LTR	DESCRIPTION	APPROVED	DATE
A	AS ISSUED		11-3-76
B	ADD. TITLE & REV. DBCHG.		2-24-77

CYCLE REQUEST LOGIC

PR_4/PRN5 J1-46

SRQ10 J1-30
SRQ11 J1-28
SRQ12 J1-26
SRQ13 J1-24
SRQ14 J1-22
SRQ15 J1-20
SRQ16 J1-18
SRQ17 J1-16
SRQ20 J1-14
SRQ21 J1-12
SRQ22 J1-10
SRQ23 J1-8
SRQ24 J1-6
SRQ25 J1-4

R3-6 500 Ω
R3-8
R3-10
R2-3
R2-5
R2-7
R2-9
R3-7 500 Ω
R3-9
R2-2
R2-4
R2-6
R2-8
R2-10
-2V
500

U51 74150 16-TO-1 MULTIPLEXER
STROBE

(C29) SSR1 (0:5)

U71 74150 16-TO-1 MULTIPLEXER
STROBE

(E29) SSR2 (0:5)

+5V
U112 LS86
U111 S00
U31 S04

(F3) T4

U33 S38
U41 S22
REQ1
TRNFF1
(F17)

U41 S22
REQ2
TRNFF2
(F20)

U33 S38

CYCRQ1
CYCRQ2

R1-8 1K
R1-6 1K

U53 LS08

U46 74S175 4-BIT REGISTER
(F36) CLK
CLEAR
DCYC1
DCYC2 (F24) (B38)
DEVC1

U78 S08
DMACYC1 (B4)

U42 S51
DMALOI (F36)
P1-57 DMALO

U42 S51
DCYC2 (D37)
P1-54 DMACYC

U36 S10
DCYC (D7)

U85 74LS157 QUAD 2 BIT MULTI-PLEXER
SELECT
ENABLE
(E23) INFF2
(B23) INFF1
(E28) STC SEL2
(C28) STC SEL1
(E28) CLC SEL2
(C28) CLC SEL1
(D18) FBFF2
(E15) FBFF1
IN (B4) (F35)
STC SEL (F7)
CLC SEL (G7)
FBFF (F5)

U52 S08
(T4)
DMAEND (B6)

U32 74S158
(D9) OUT
(D7) T34
(F3) T623
(A4) BPSNF
(A1) F4NF
(E4) T3
(F2) T23
(D7) T34
ENABLE
SELECT
CLK (B4)(D36)
DFRZ (C9)
DMALOZ (C39)

R1-9 1K
+5
"MX" "E"
W1

(PCYC1)
(PCYC2)
(C5) T5
(B8) DMALCHFF
U65 S32
U11 LS02
U63 S04
U82 LS00
EN1 (D29)
EN1 (D29)(H5)
EN2 (F29)
EN2 (F29)(H5)

R11 330 Ω
R10 330 Ω
DMARQ1 P1-55
DMARQ2 P1-59
FROM I/O EXTENDER

SCHEMATIC DCPC	
12897B	
—	D-12897-60004-54